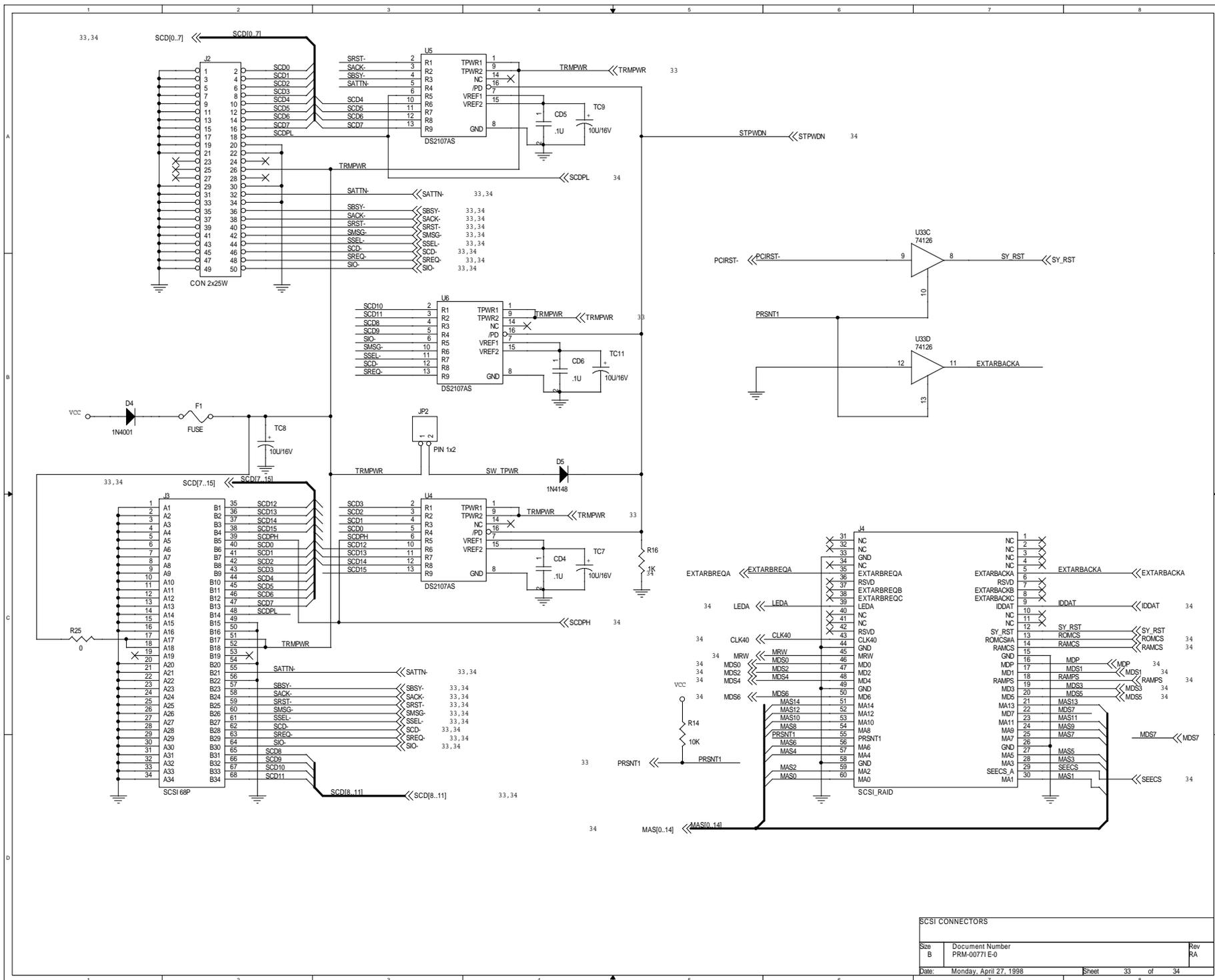


# SINGLE CPU 440LX CUSTOMER REFERENCE DESIGN

TITLE	PAGE	COMPONENT	PLACEMENT	PAGE
COVER SHEET	1	CPU SLOT1	JP1	2 , 3
KLAMATH	2 - 3	Clock Generator	U1, U2	4
CLK SYNTHESIZER	4	74HC74	U3	4, 18
PAC(82443LX)	5, 6	82443LX	U4	5, 6
MEMORY BUFFER	7	74LV245	U5	5
DIMM1, 2	8, 9	74FCT3245	U6 - U11	7
DIMM3, 4	10, 11	PIIX4	U12	12, 13
KEYB / MOUSE		74LVC14	U13	13, 18
PIIX4	12, 13	D221ET	U14	30
AGP CONN.	14	74HCT14	U15	18
PCI CONN.	15, 16	74ALS05	U16	18, 22
ISA CONN.	17	7407	U17, U22	14, 18, 22
PALEL	18	74HC00	U18	18
IDE CONN.	19	FLASH BIOS	U19	20
USB / FLASH BIOS	20	74ALS245	U20	20
KEYBOARD/MOUSE	21	SC1151CS	U21	21
DC TO DC CONVERTER	21	74FCT3244	U23	22
CPU FREQUENCE RATE	22	SMC672	U24	27
CHIP GTL TERM.	23	74F32	U25	27
PCI/AGP PULLUPS	24	75C185	U27, U28	29
ISA/PAC DECOUP	25	UM661	U29	30
VREF PAGE	26	LM78	U30	30
SMC CHIP	27	LM75	U31	30
SERIAL/FLOPPY	28			
TEMPLATER SENOR	29			

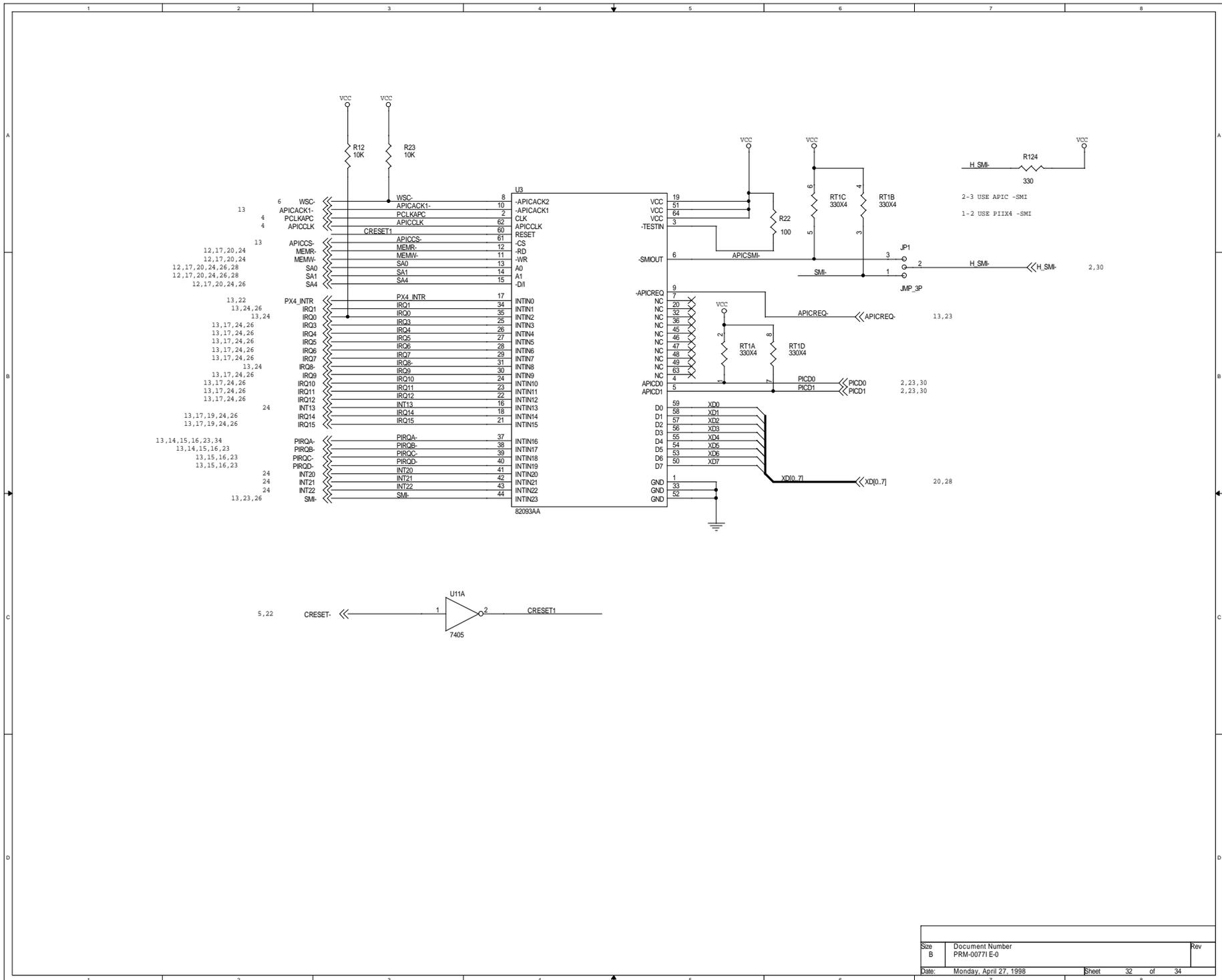
LINK  
 2.SCH  
 3.SCH  
 4.SCH  
 5.SCH  
 6.SCH  
 7.SCH  
 8.SCH  
 9.SCH  
 10.SCH  
 11.SCH  
 12.SCH  
 13.SCH  
 14.SCH  
 15.SCH  
 16.SCH  
 17.SCH  
 18.SCH  
 19.SCH  
 20.SCH  
 21.SCH  
 22.SCH  
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 24.SCH  
 25.SCH  
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 27.SCH  
 28.SCH  
 29.SCH  
 30.SCH  
 31.SCH  
 32.SCH  
 33.SCH  
 34.SCH





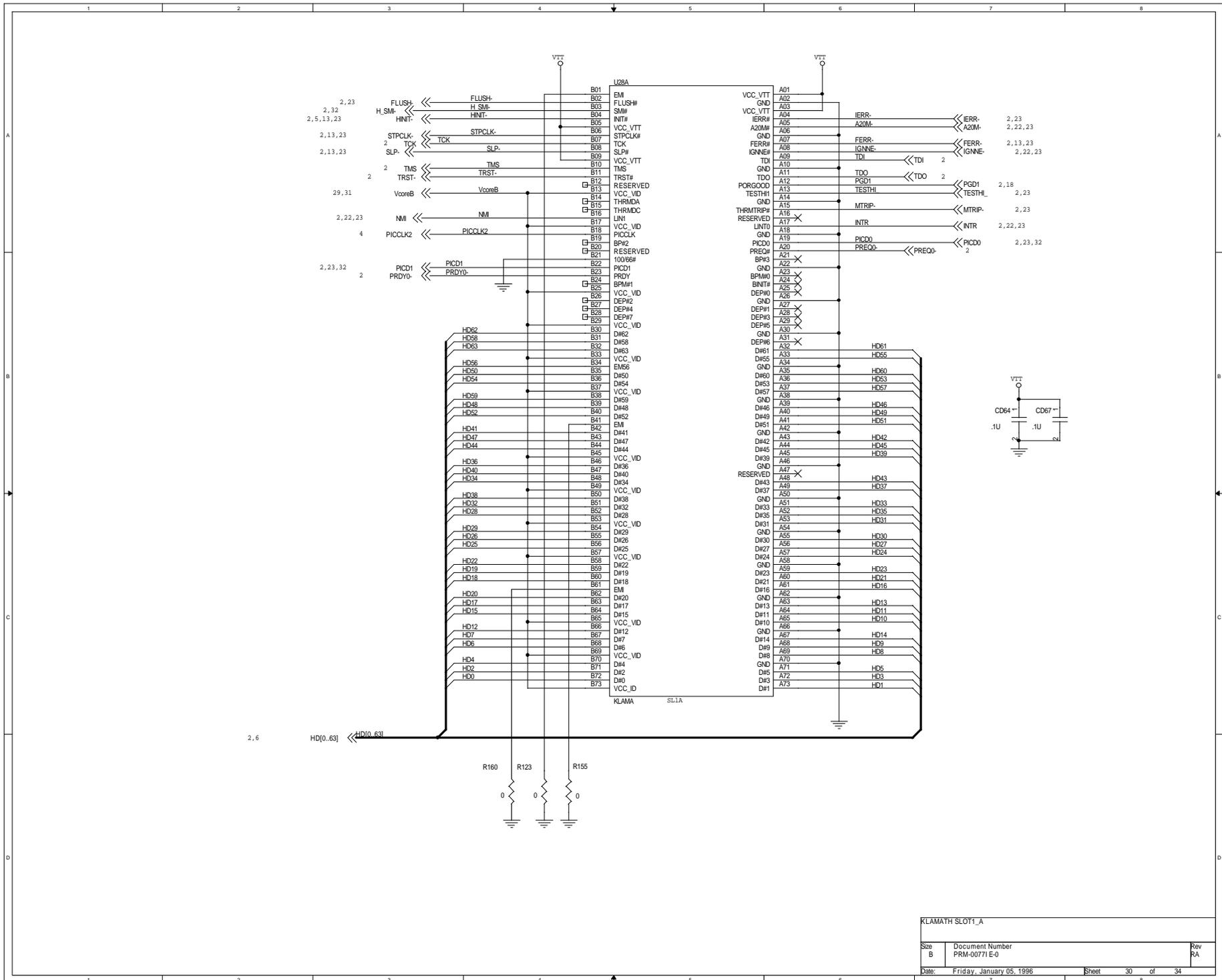
SCSI CONNECTORS

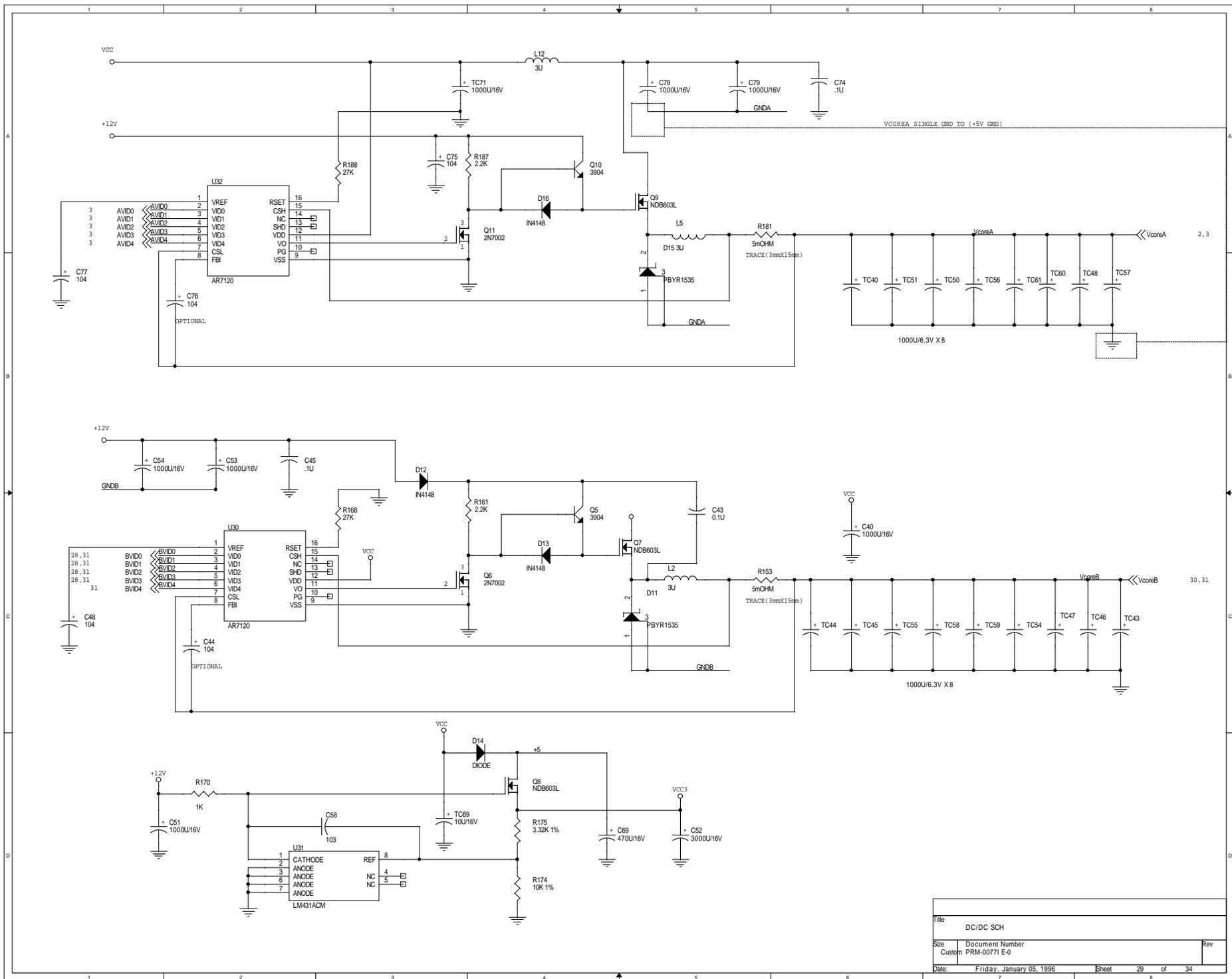
Size	Document Number	Rev
B	PRM-00771 E-0	RA
Date:	Monday, April 27, 1998	Sheet 33 of 34



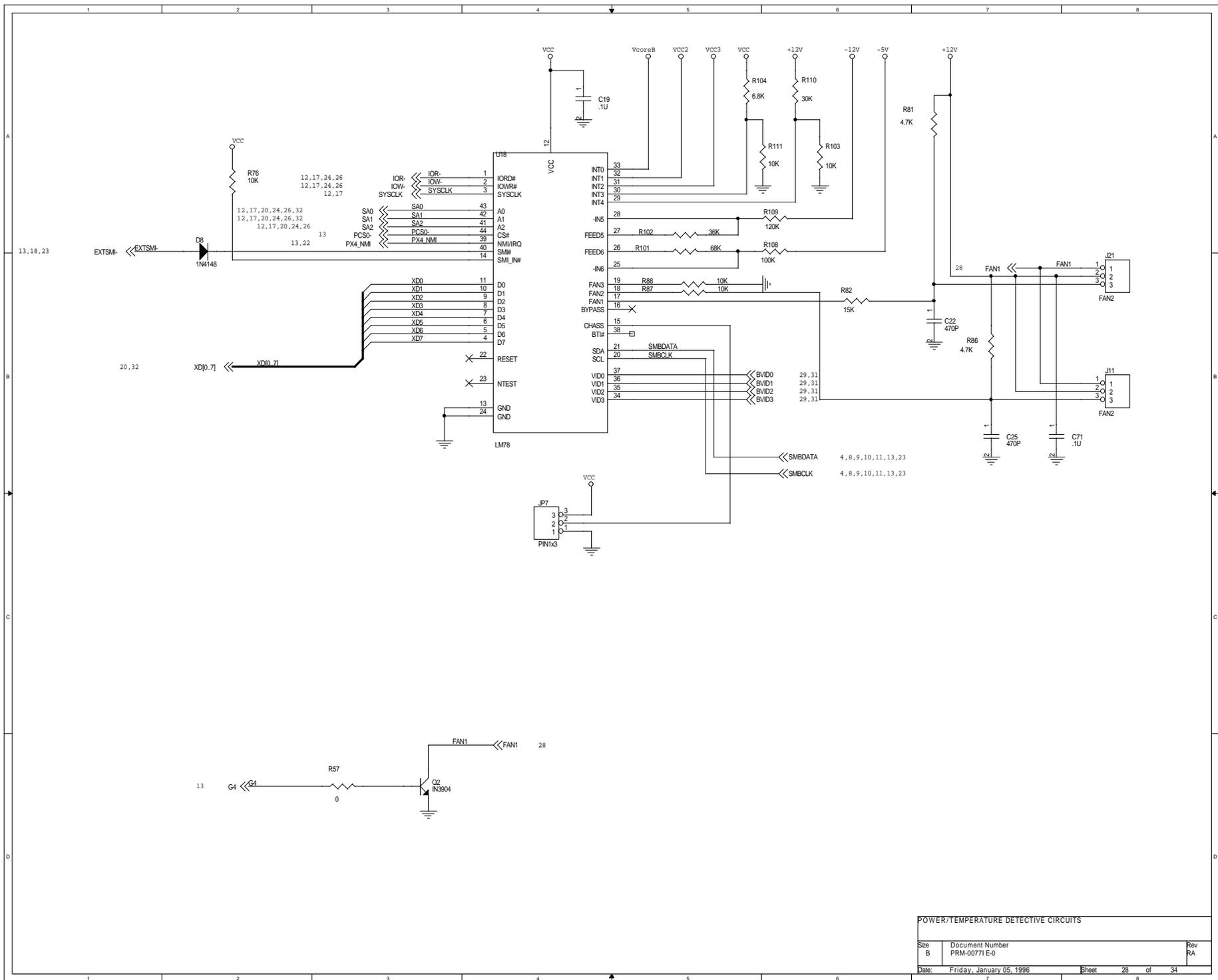
Size B	Document Number PRM-00771 E-0	Rev
Date: Monday, April 27, 1998	Sheet 32	of 34





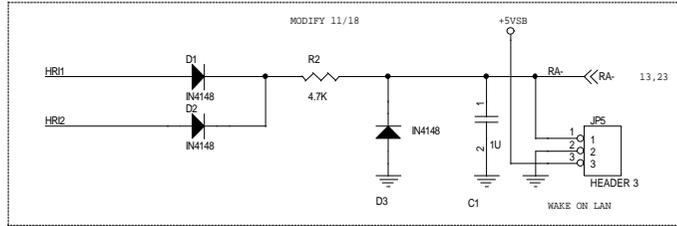


Title		
DC/DC SCH		
Size	Document Number	Rev
Custom	PRM-00771 E-0	
Date:	Friday, January 05, 1996	Sheet 29 of 34

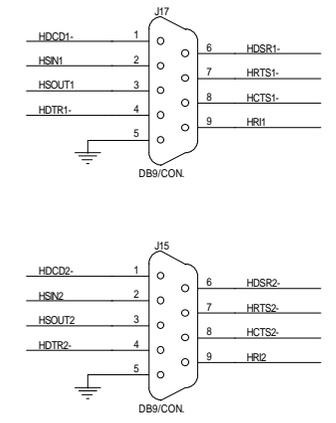
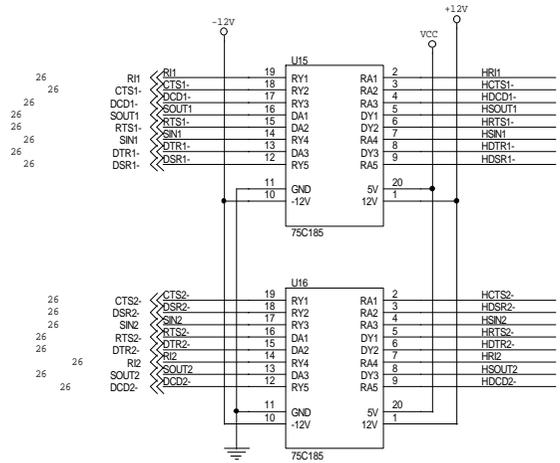
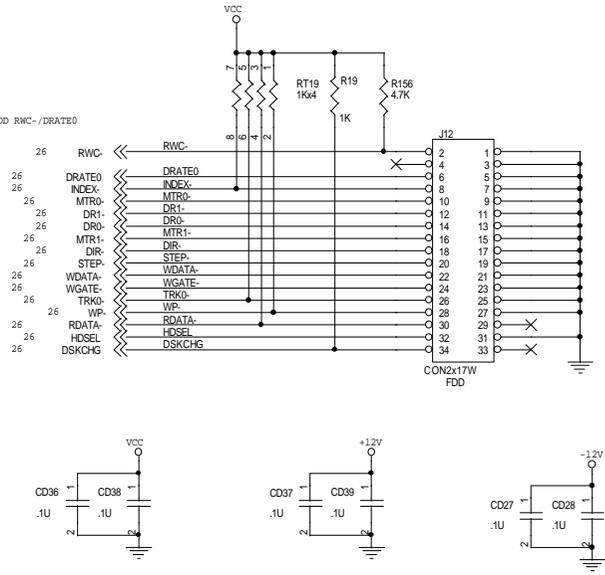


In order to minimize the crosstalk in ECP mode, the termination circuits shown below are recommended. Place all termination circuits close to the connector to avoid EMI.

ALL RNC CHANGE TO 0603 CAP

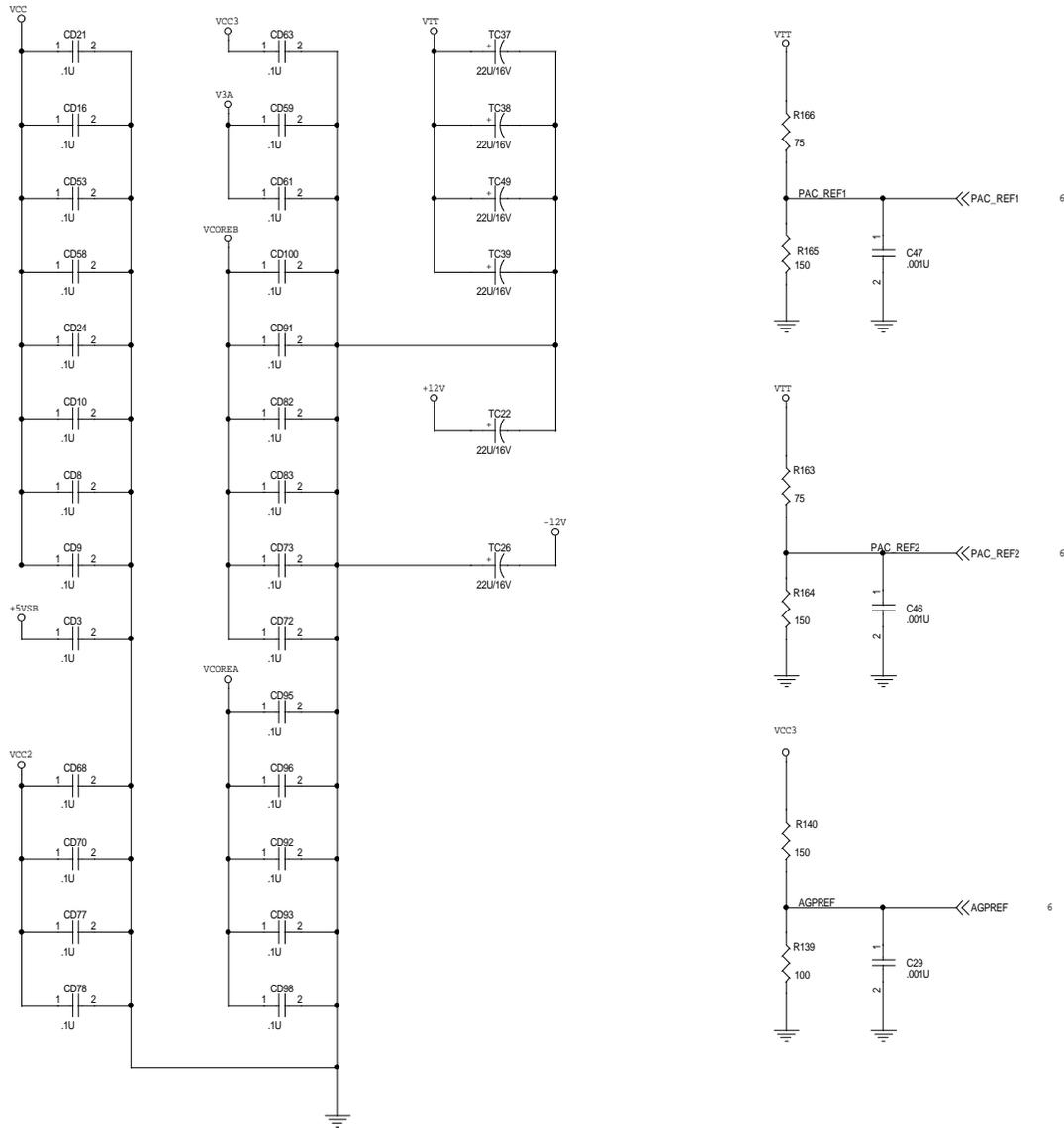


ADD RWC-/DRATE0





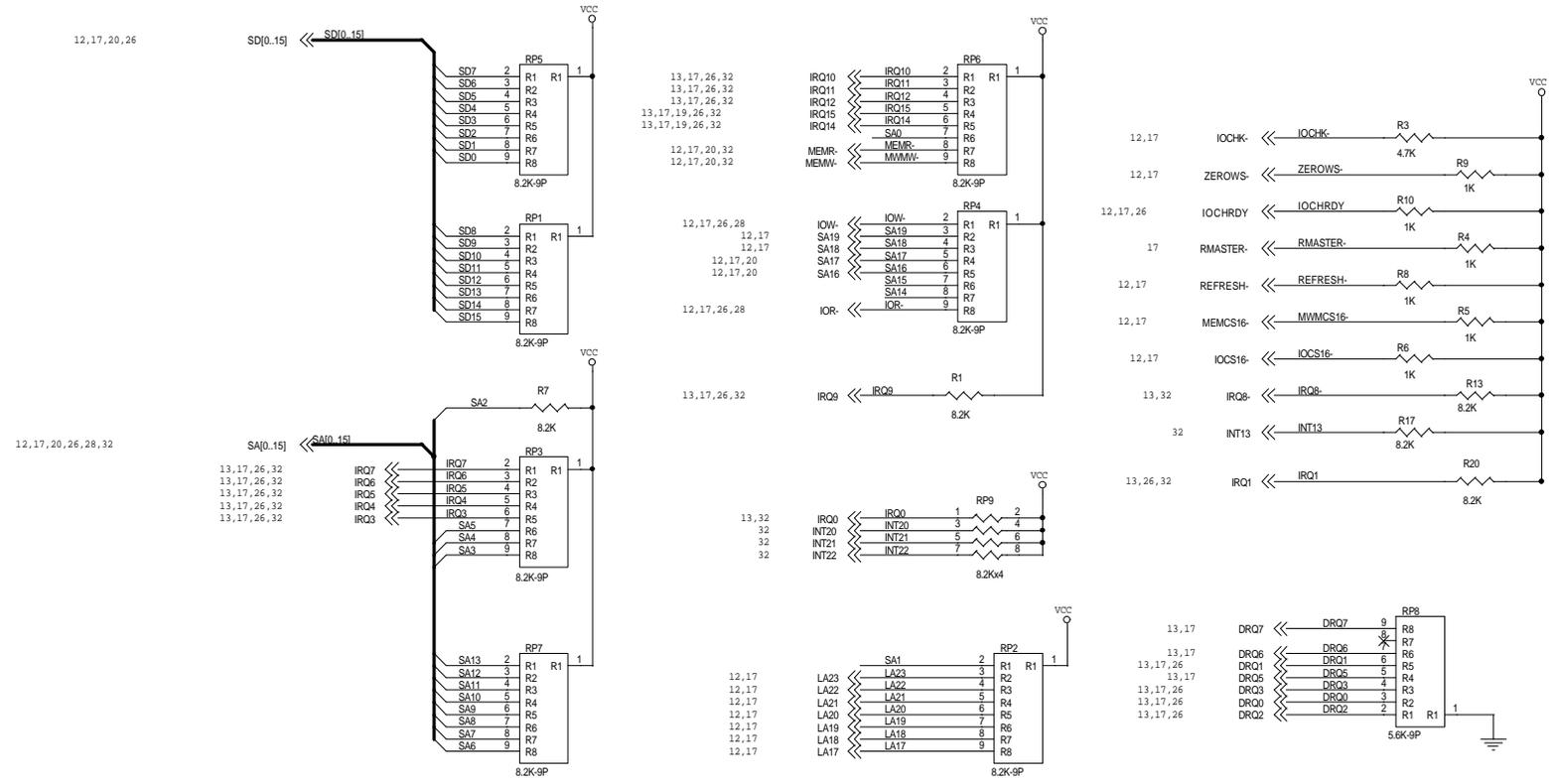
# TERMINATION VOLTAGE DECOUPLING



## VTT BYPASS CAPACITORS

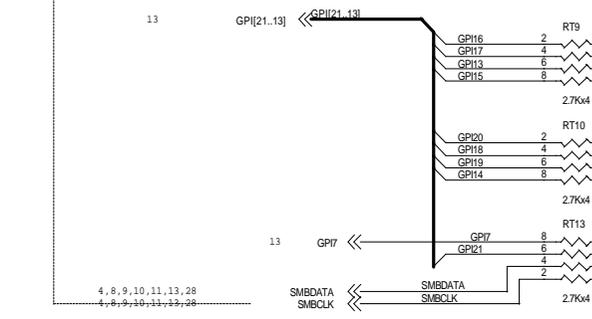
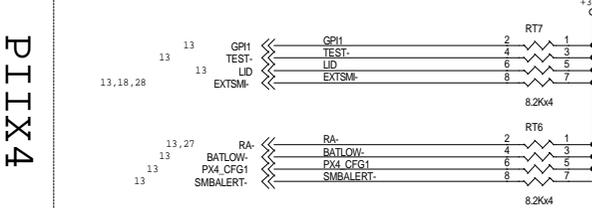
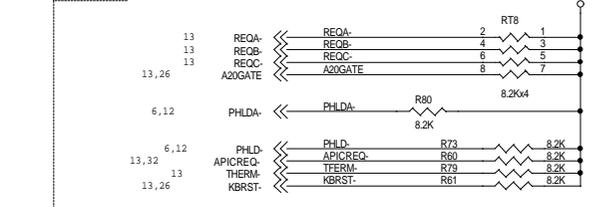
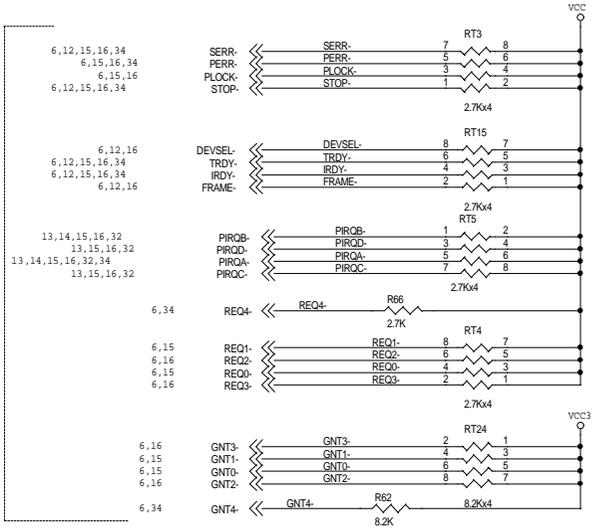
Size	Document Number	Rev
B	PRM-00771 E-0	RA
Date:	Friday, January 05, 1996	Sheet 25 of 34

### ISA BUS RESISTORS

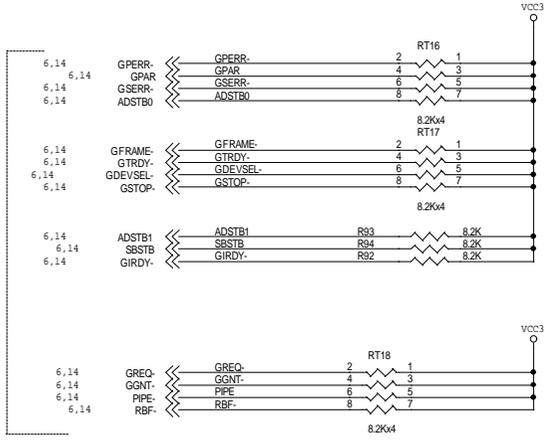
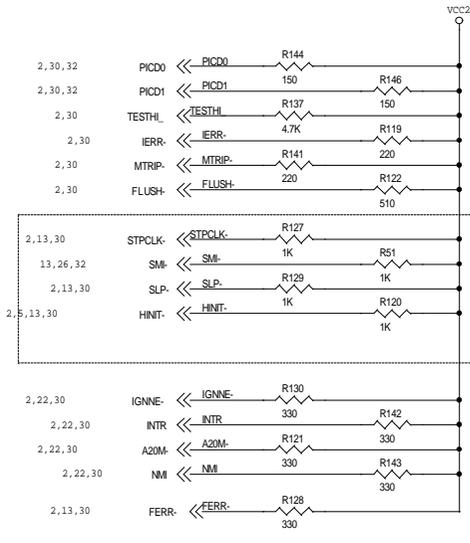


PULL UPS & PULL DOWNS		
Size B	Document Number PRM-00771 E-0	Rev RA
Date: Friday, January 05, 1996	Sheet 24	of 34

# PCI BUS



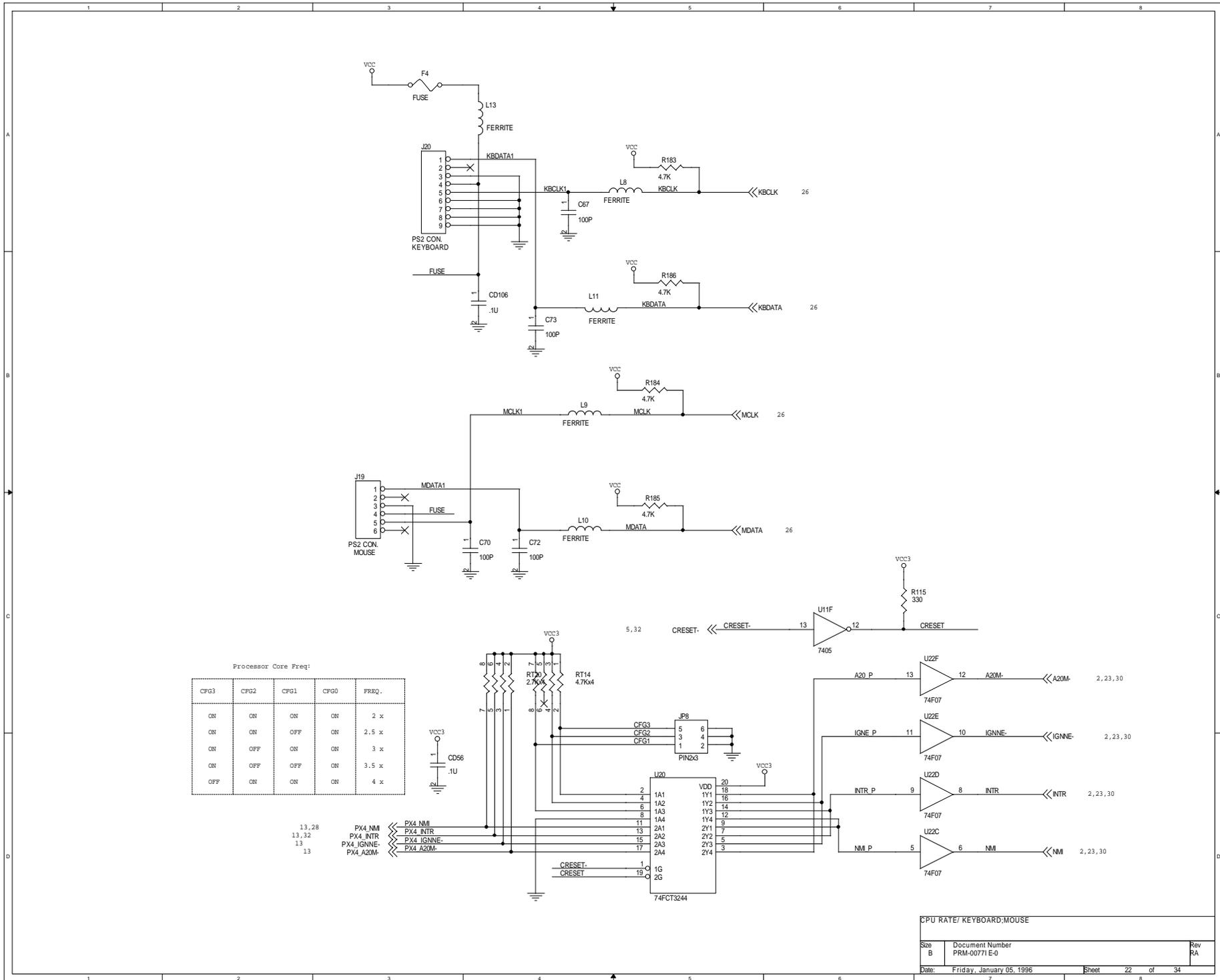
# AGP



NOTE :  
RESISTOR VALUES ON SIGNALS  
STPCLK#, SM#, SLP#, & HINT#  
ENABLE AN LAI TO BE USED FOR  
BOARD DEBUG. IF AN LAI WILL  
NOT BE USED FOR DEBUG THEN  
THE RESISTOR VALUES SHOULD  
BE CHANGED TO 1K OHM.

410  
220  
330

BUS RESISTORS		
Size	Document Number	Rev
B	PRM-00771 E-0	RA
Date:	Friday, January 05, 1996	Sheet 23 of 34



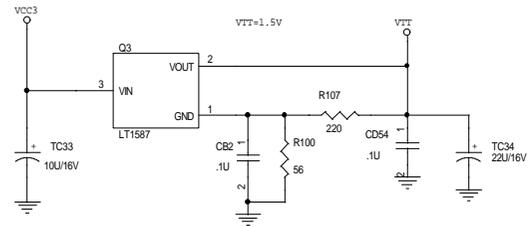
Processor Core Freq:

CFG3	CFG2	CFG1	CFG0	FREQ.
ON	ON	ON	ON	2 x
ON	ON	OFF	ON	2.5 x
ON	OFF	ON	ON	3 x
ON	OFF	OFF	ON	3.5 x
OFF	ON	ON	ON	4 x

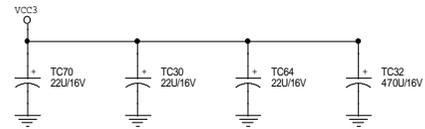
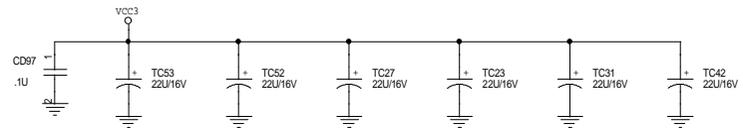
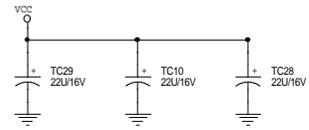
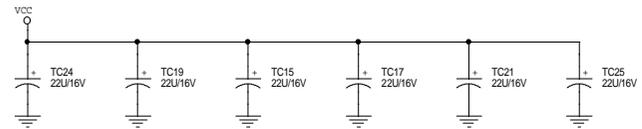
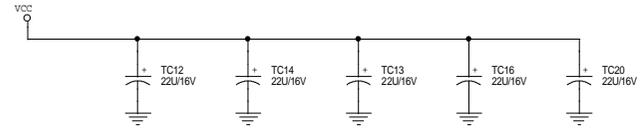
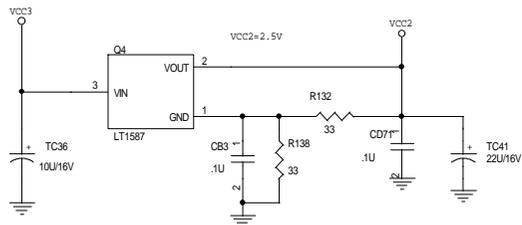
13, 28  
13, 32  
13

PX4 NMI  
PX4 INTR  
PX4 IGNE  
PX4 A20M

PX4 NMI  
PX4 INTR  
PX4 IGNE  
PX4 A20M

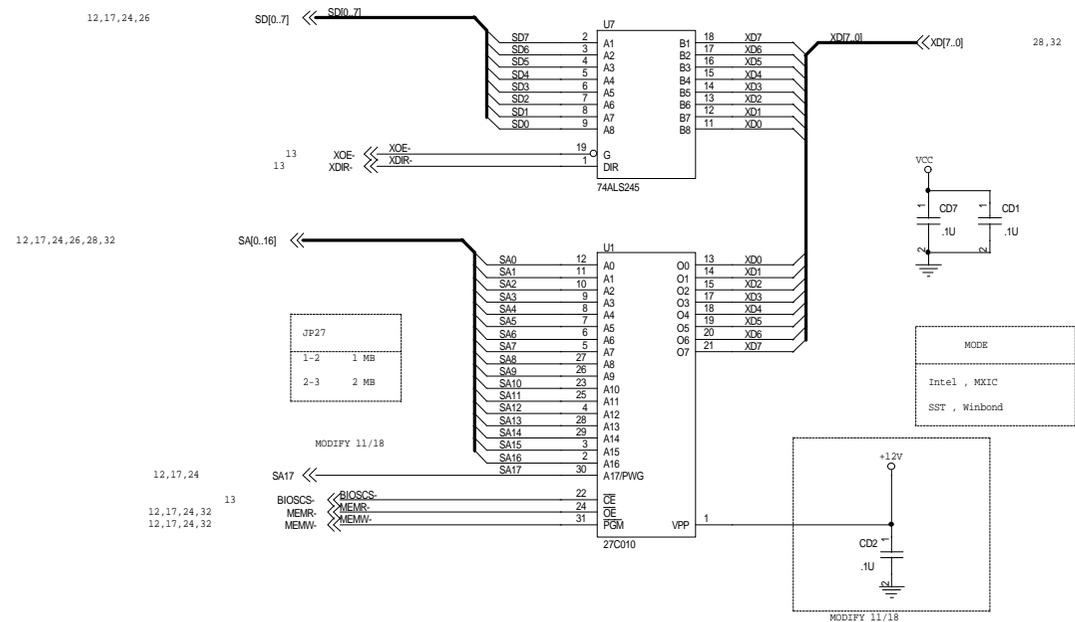
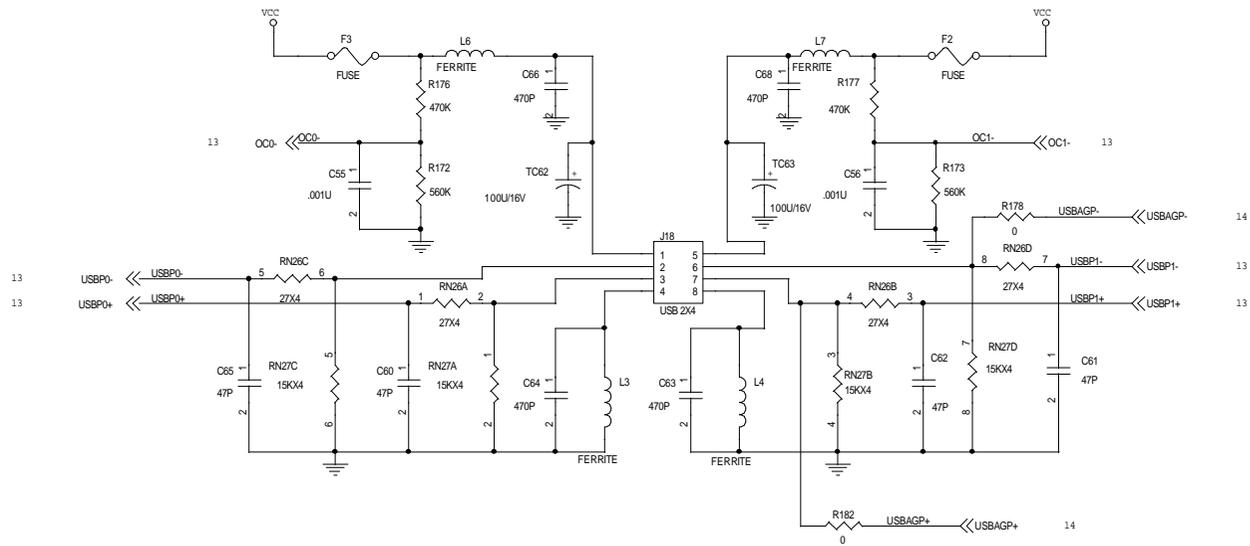


NOTE:  
VOLTAGE REGULATOR SHOULD  
BE LOCATED NEAR THE PAC



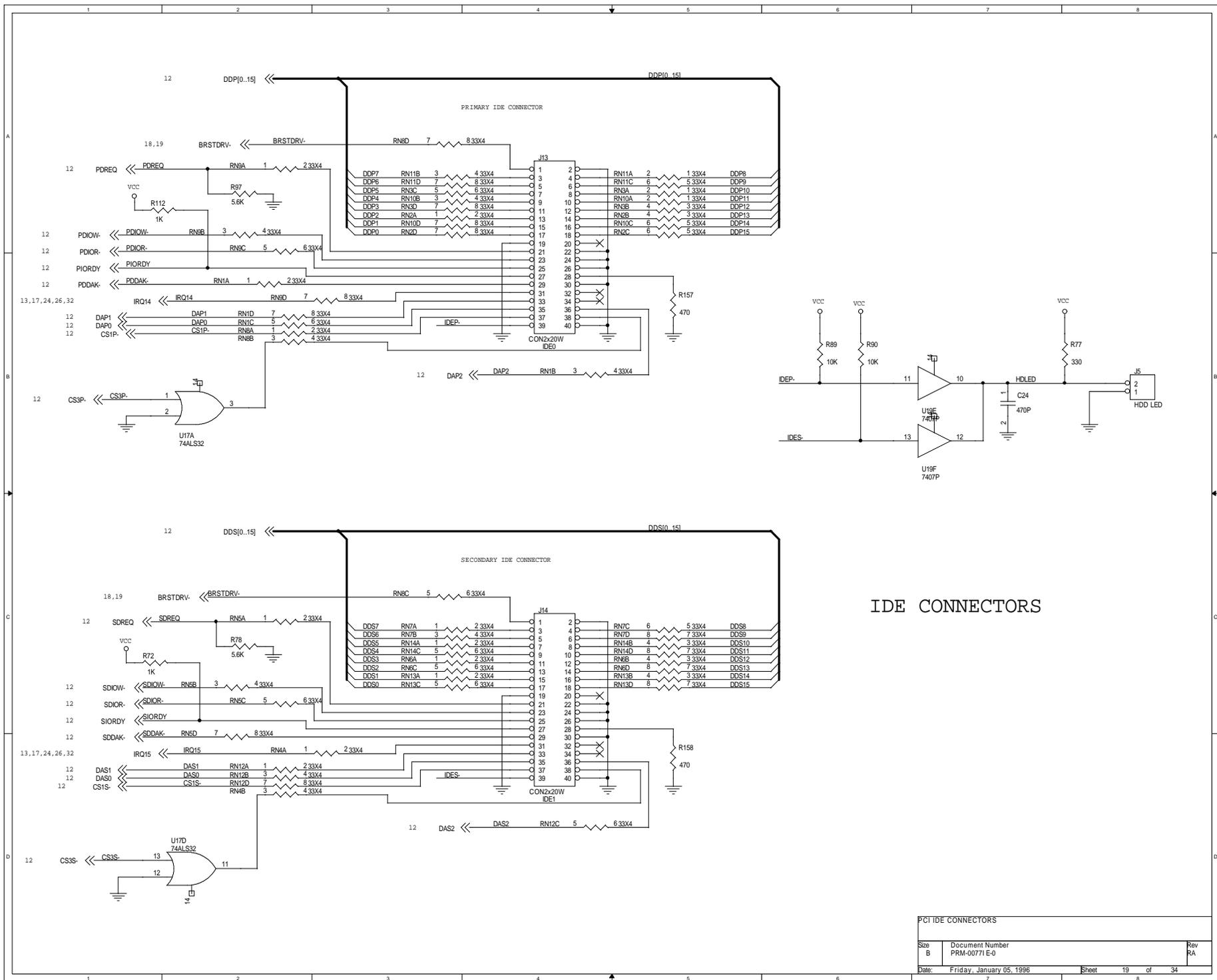
DC to DC CONVERTER CIRCUITS

Size B	Document Number PRM-00771 E-0	Rev RA
Date: Friday, January 05, 1996	Sheet 21	of 34



USB FOR PIIX4 / FLASH BIOS

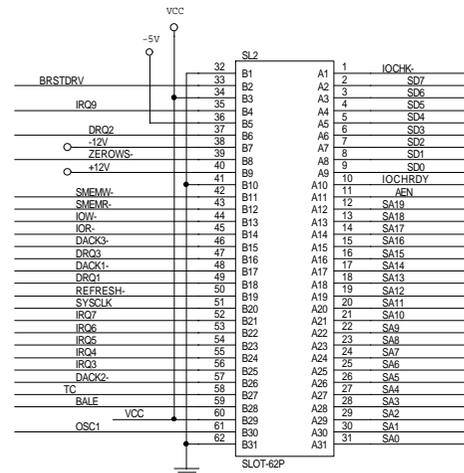
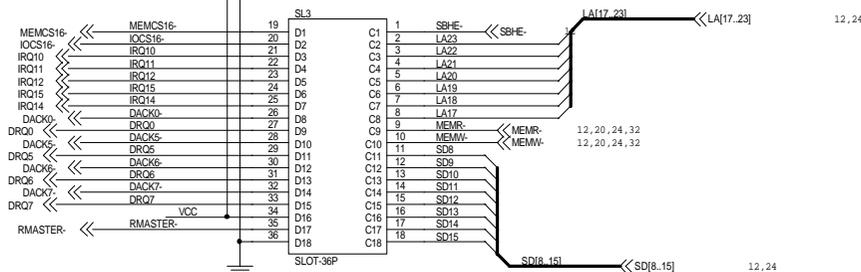
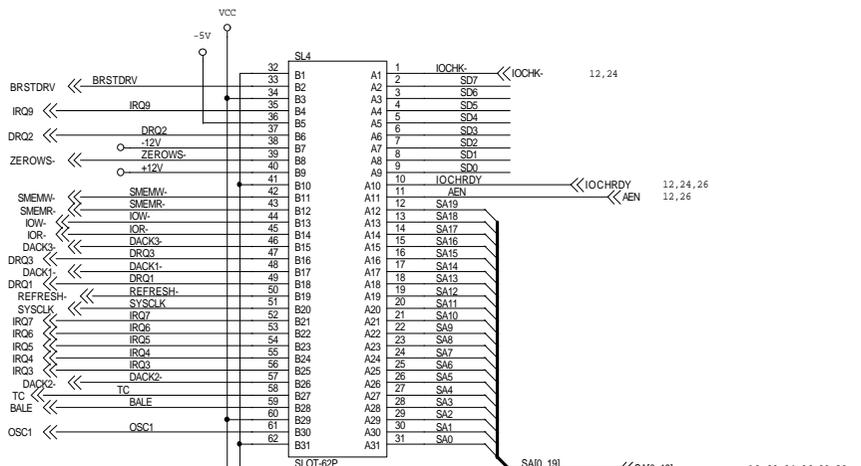
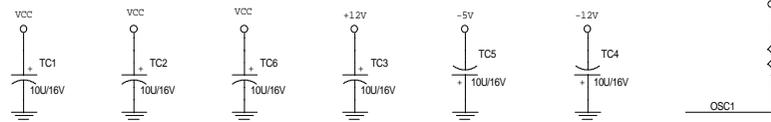
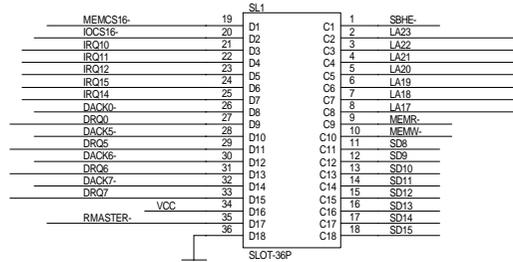
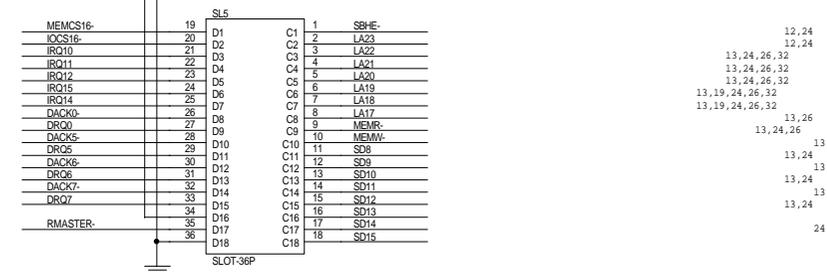
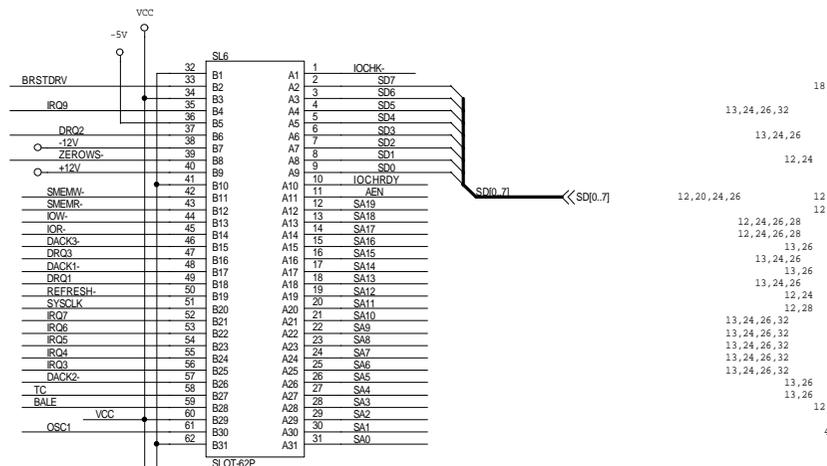
Size B	Document Number PRM-00771 E-0	Rev RA
Date: Friday, January 05, 1996	Sheet 20	of 34



IDE CONNECTORS

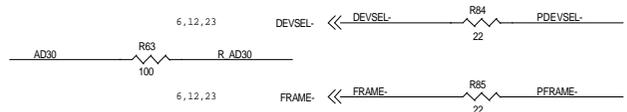
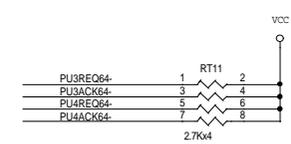
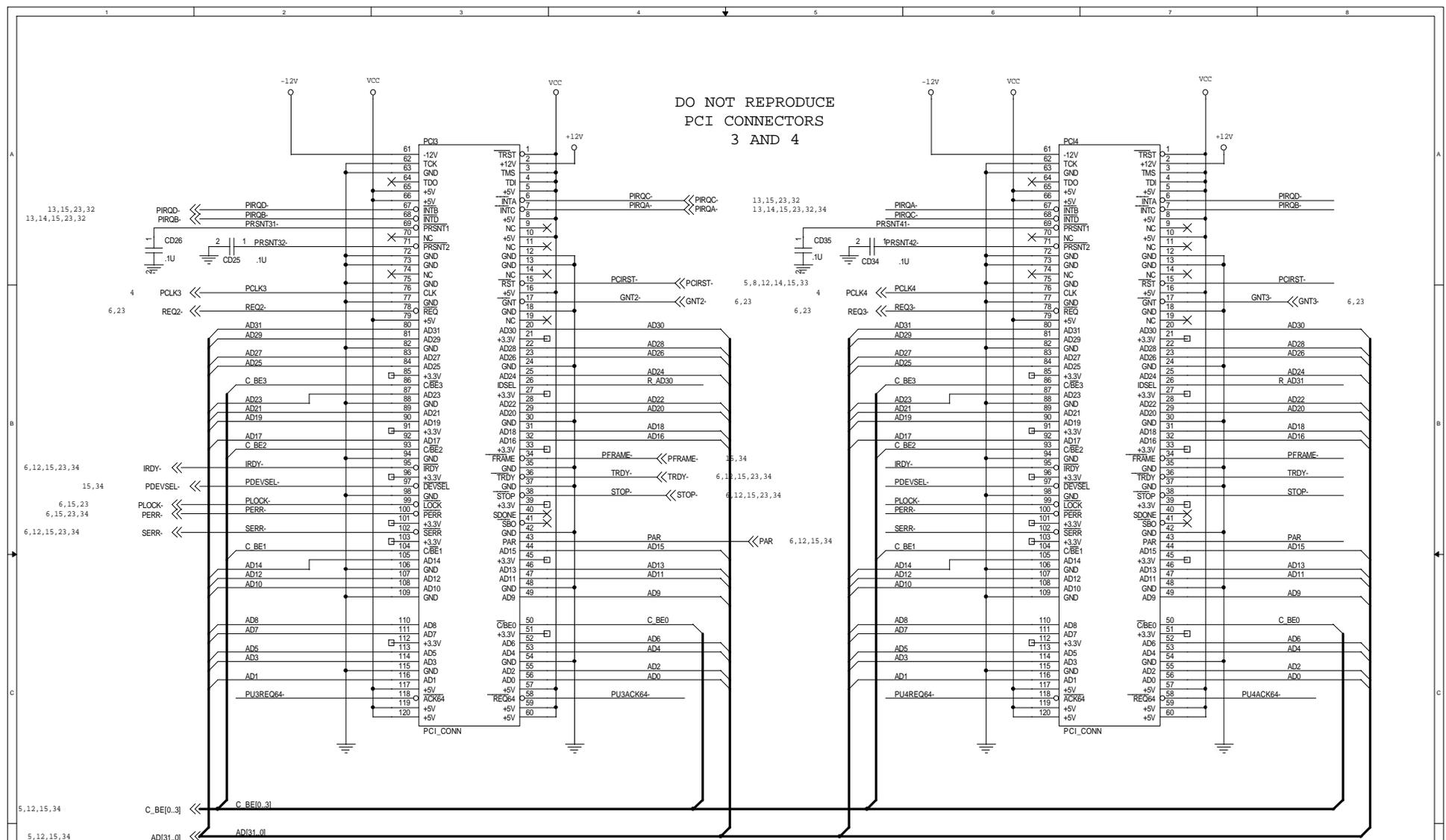
PCI IDE CONNECTORS		
Size B	Document Number PRM-00771 E-0	Rev RA
Date: Friday, January 05, 1996	Sheet 19	of 34



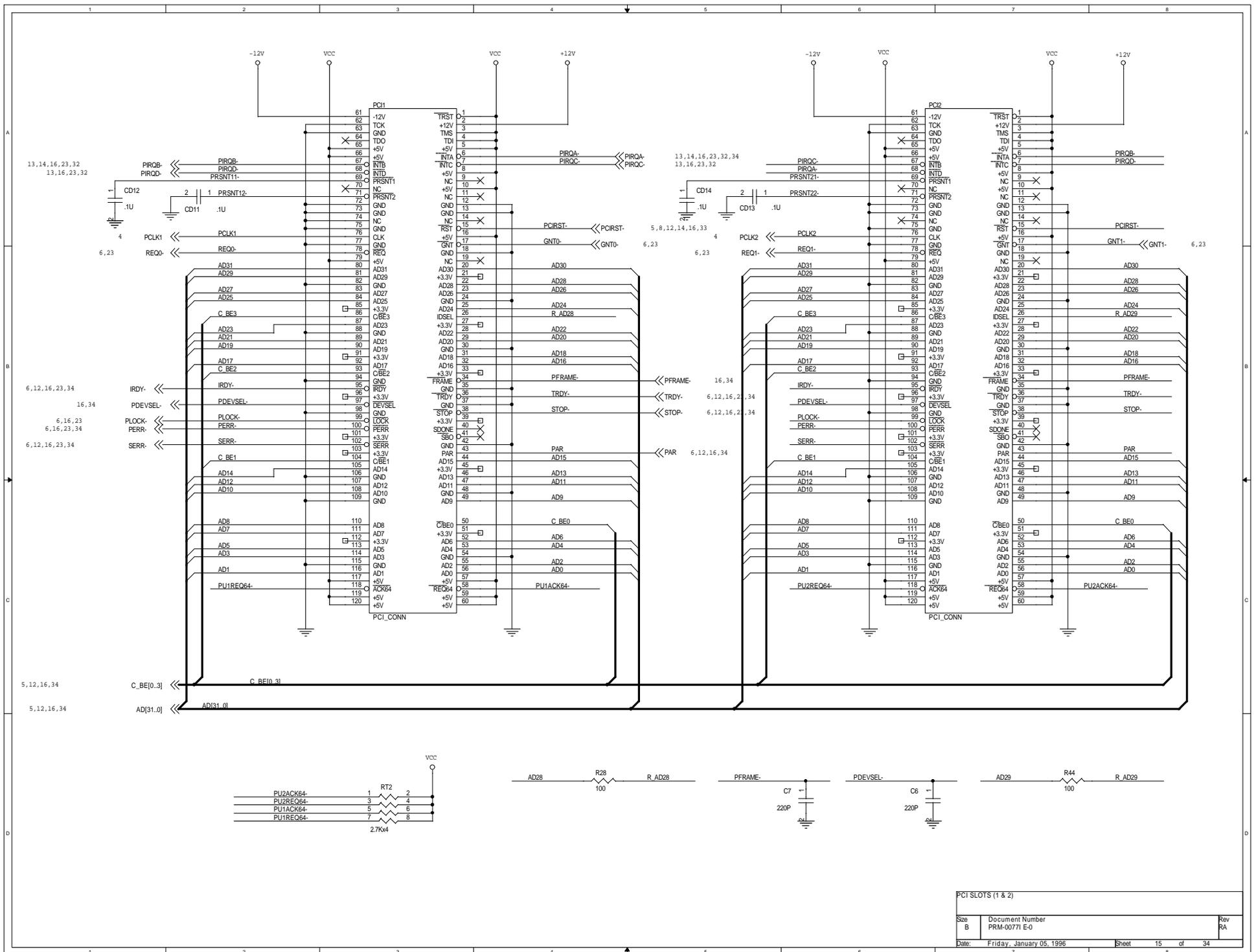


AT-BUS SLOTS		
Size	Document Number	Rev
B	PRM-00771 E-0	RA
Date:	Friday, January 05, 1996	Sheet 17 of 34

DO NOT REPRODUCE  
PCI CONNECTORS  
3 AND 4

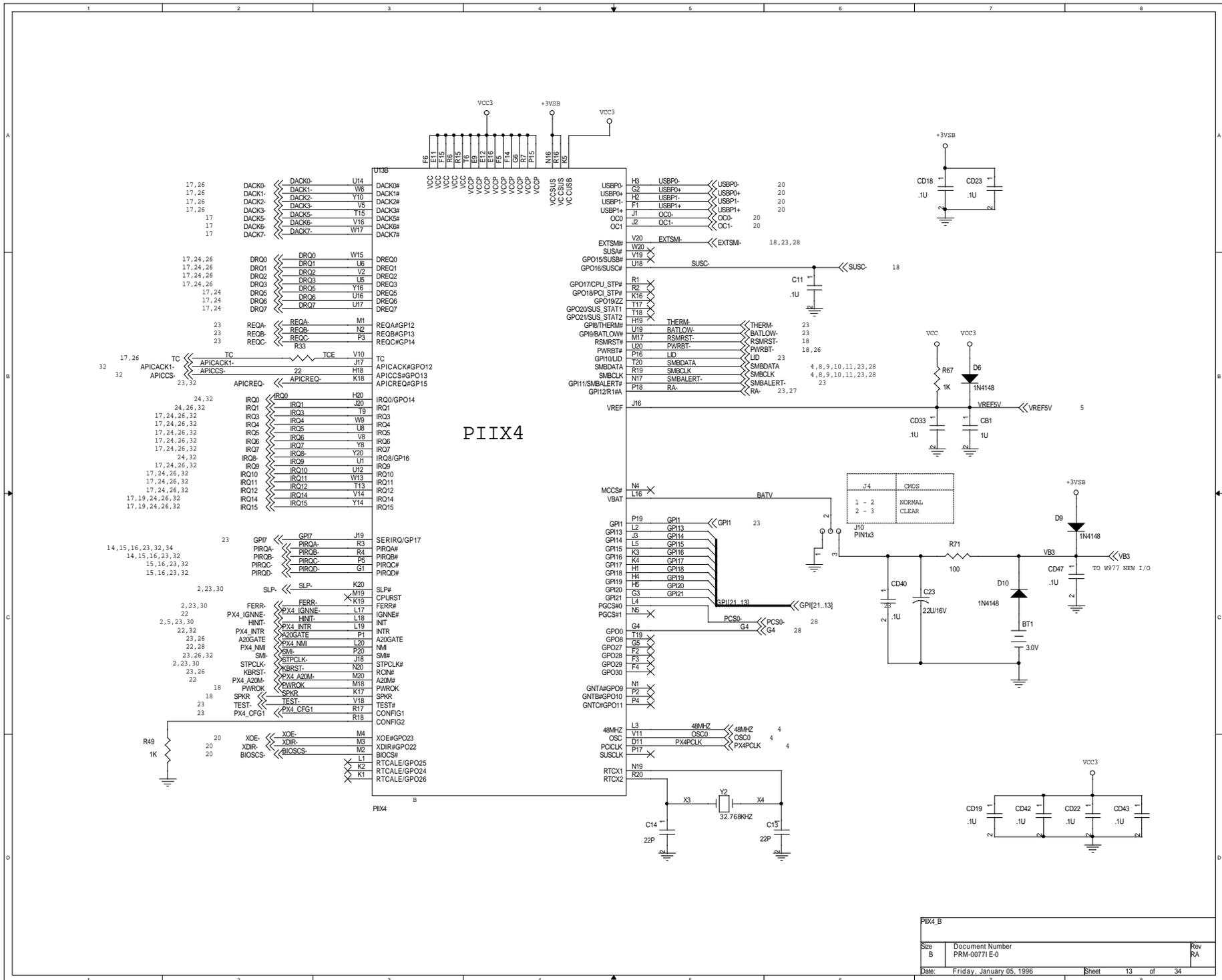


PCI SLOTS (3 & 4)		
Size B	Document Number PRM-00771 E-0	Rev RA
Date:	Friday, January 05, 1996	Sheet 16 of 34

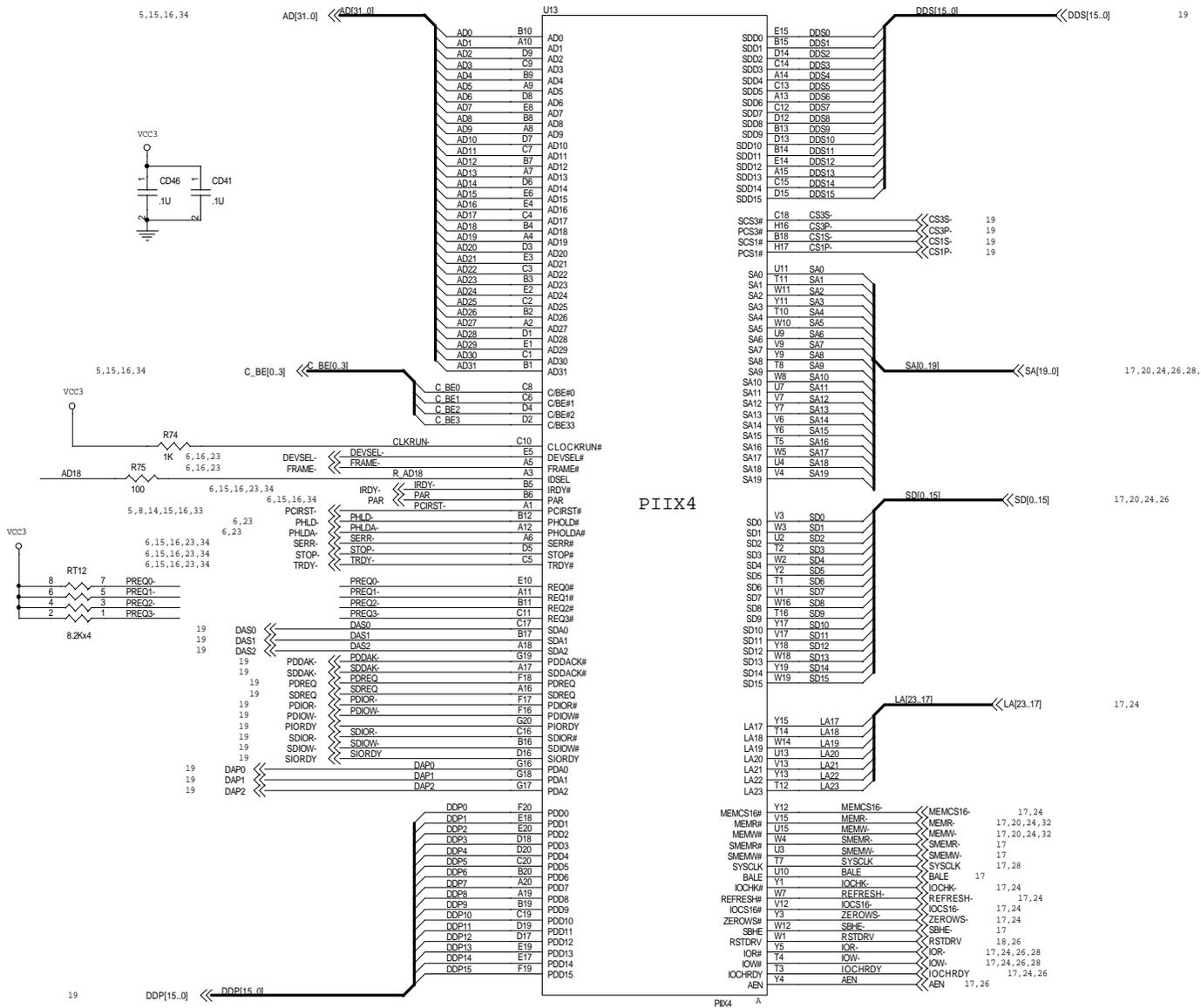


PCI SLOTS (1 & 2)		
Size B	Document Number PRM-00771 E-0	Rev RA
Date:	Friday, January 05, 1996	Sheet 15 of 34





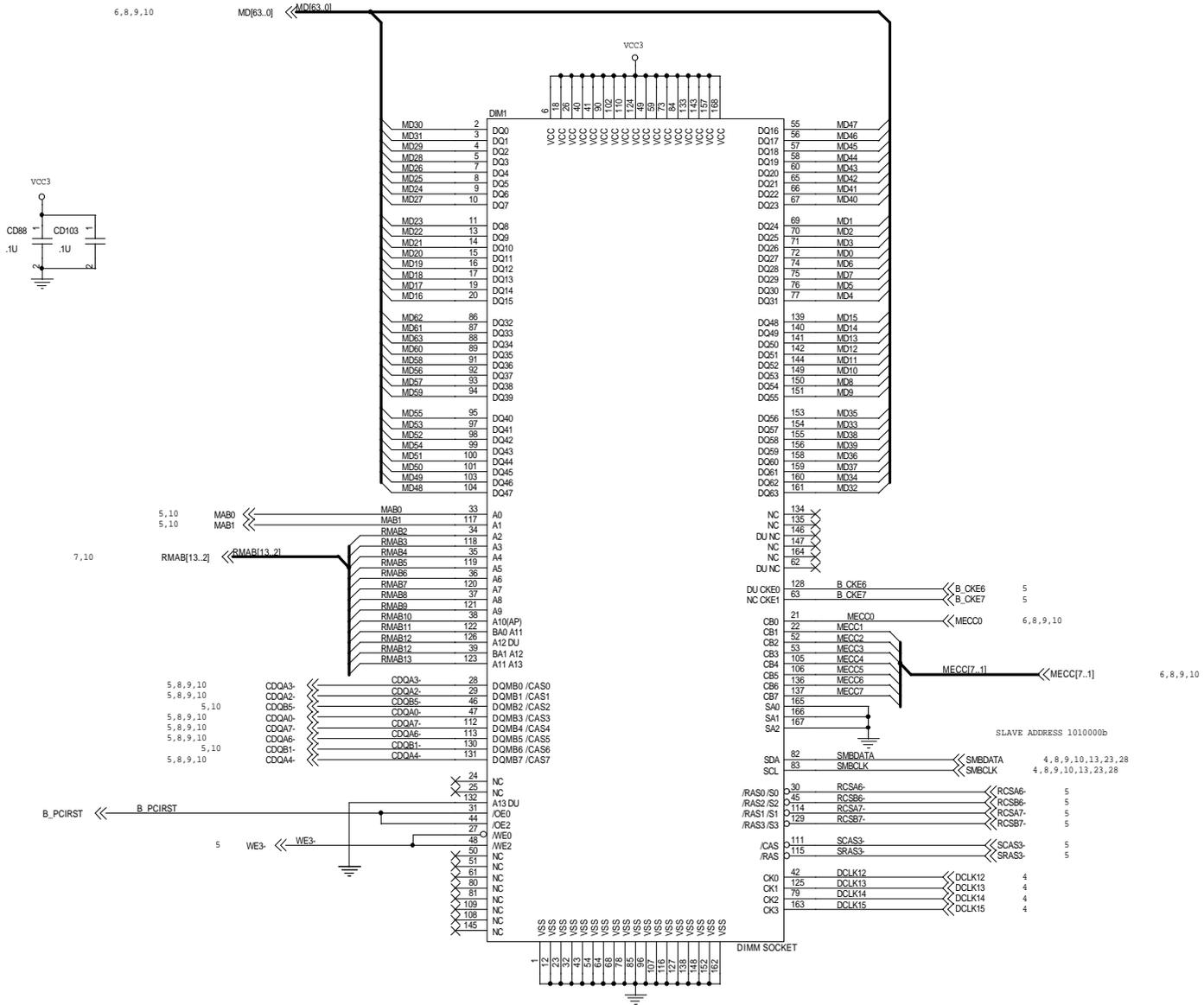
PIIX4 B		
Size	Document Number	Rev
B	PRM-00771 E-0	RA
Date:	Friday, January 05, 1996	Sheet 13 of 34



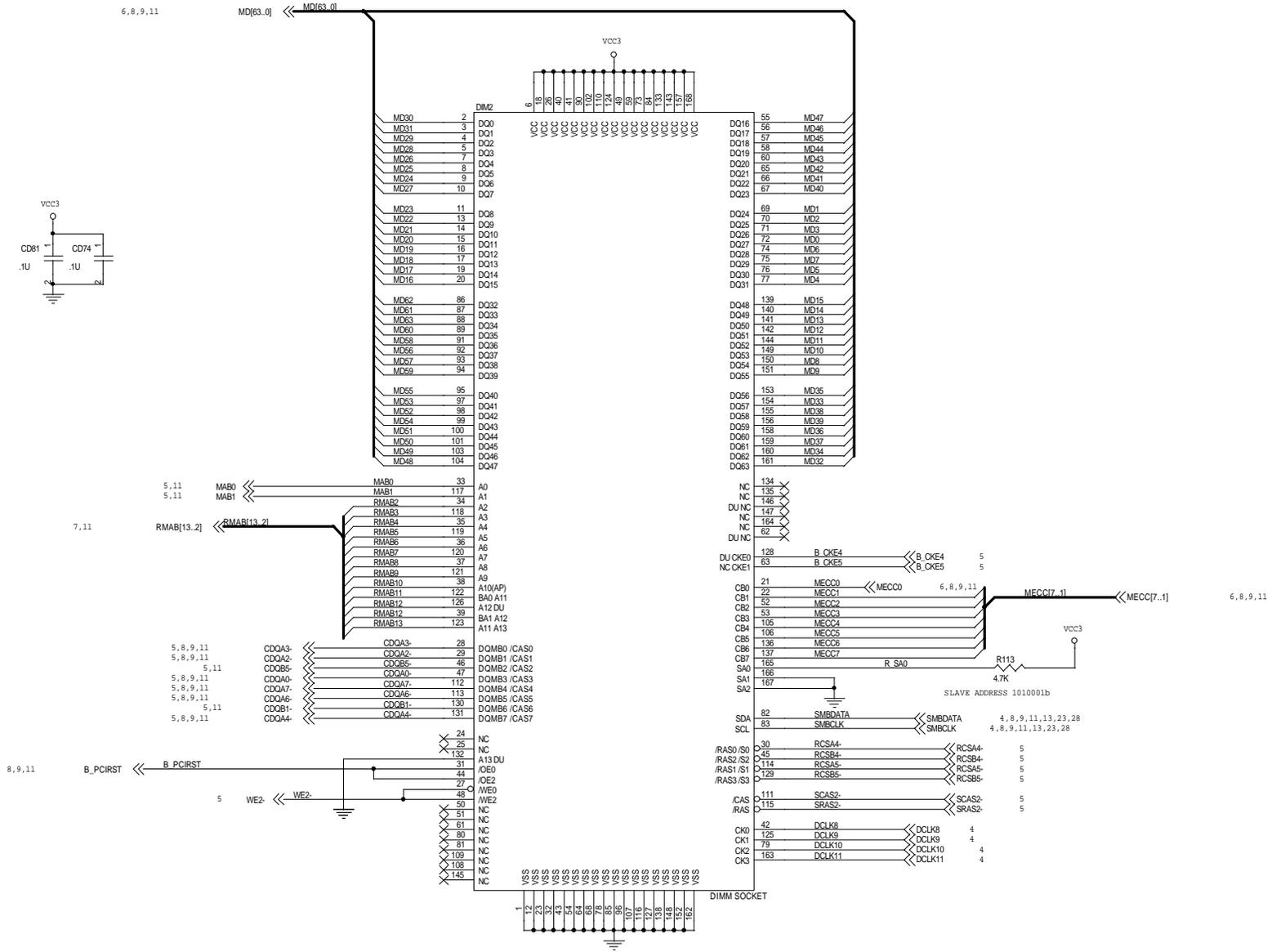
PIX4

PIX4 A		
Size	Document Number	Rev
B	PRM-00771 E-0	RA
Date:	Friday, January 05, 1996	Sheet 12 of 34

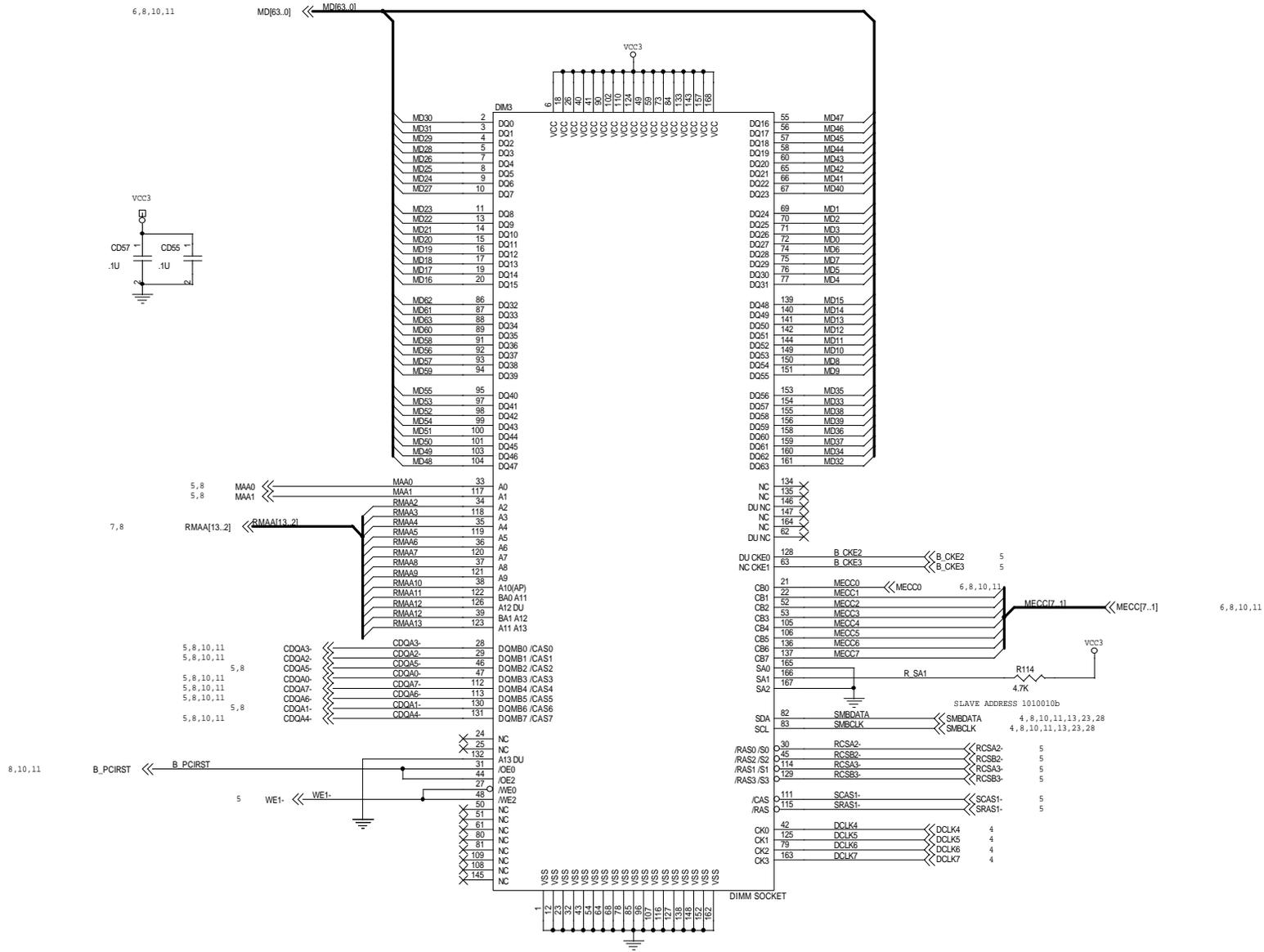
# DIMM CONNECTOR 3



# DIMM CONNECTOR 2

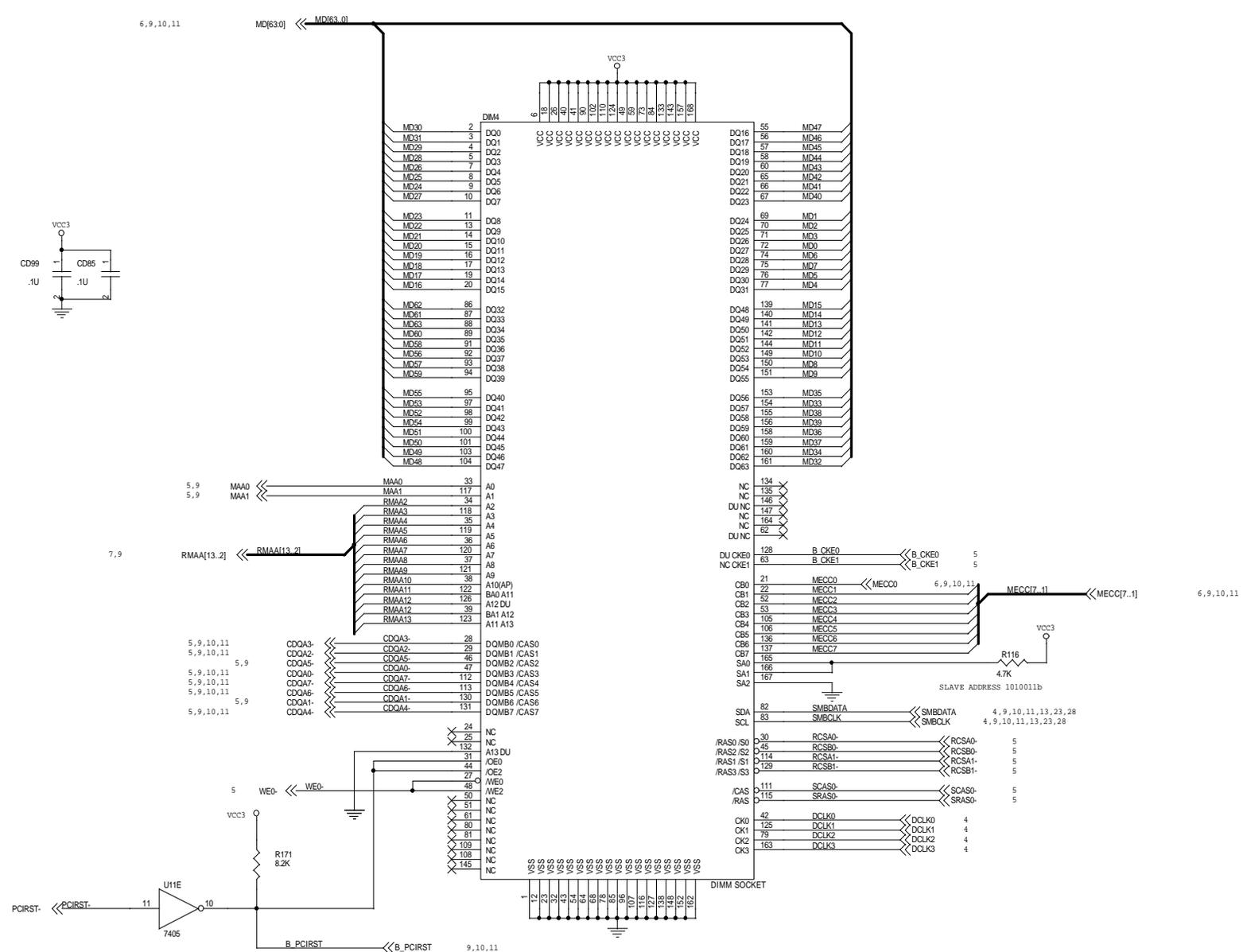


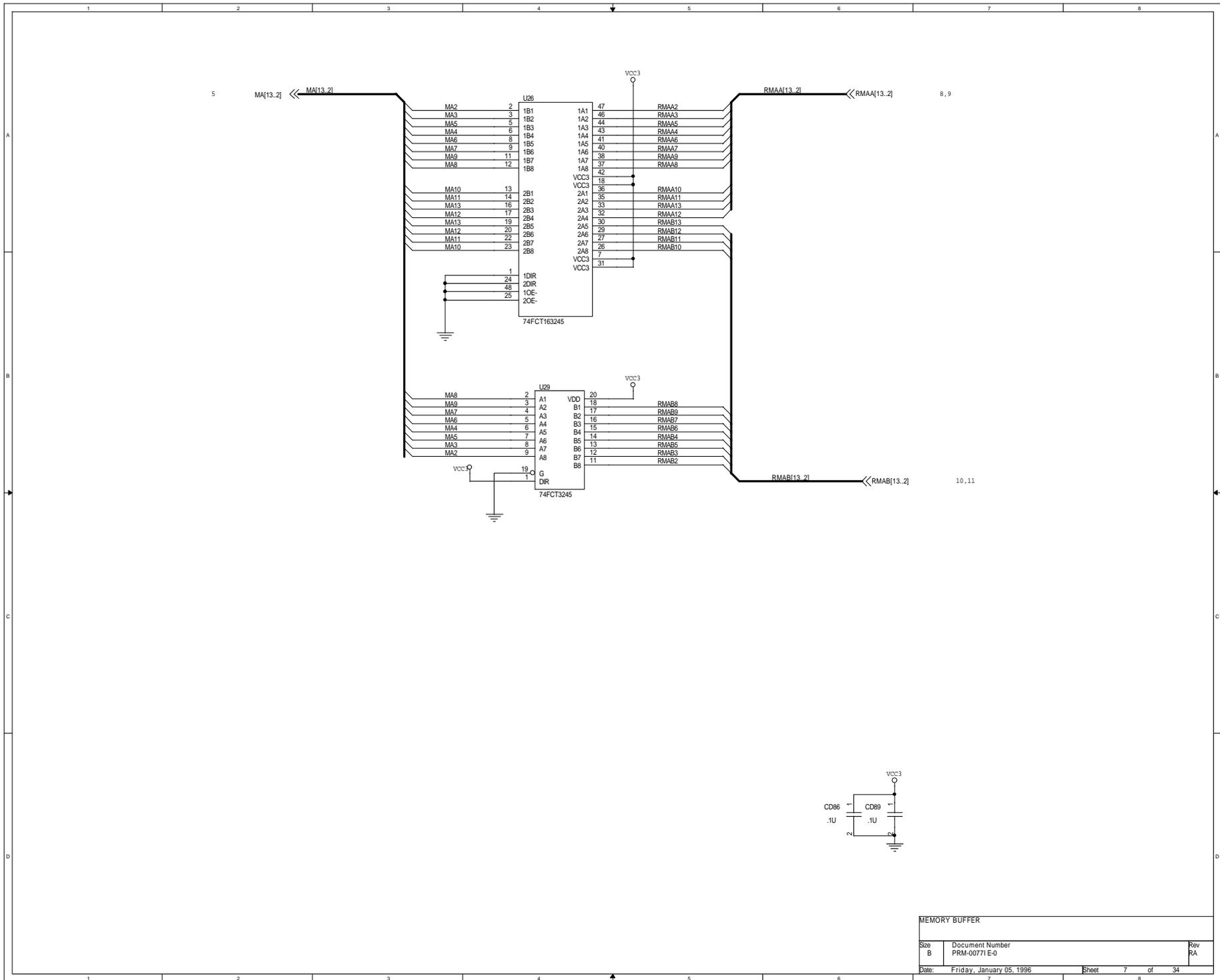
# DIMM CONNECTOR 1



2nd DIMM SOCKET (BANK1)		
Size	Document Number	Rev
B	PRM-00771 E-0	RA
Date:	Friday, January 05, 1996	Sheet 9 of 34

# DIMM CONNECTOR 0

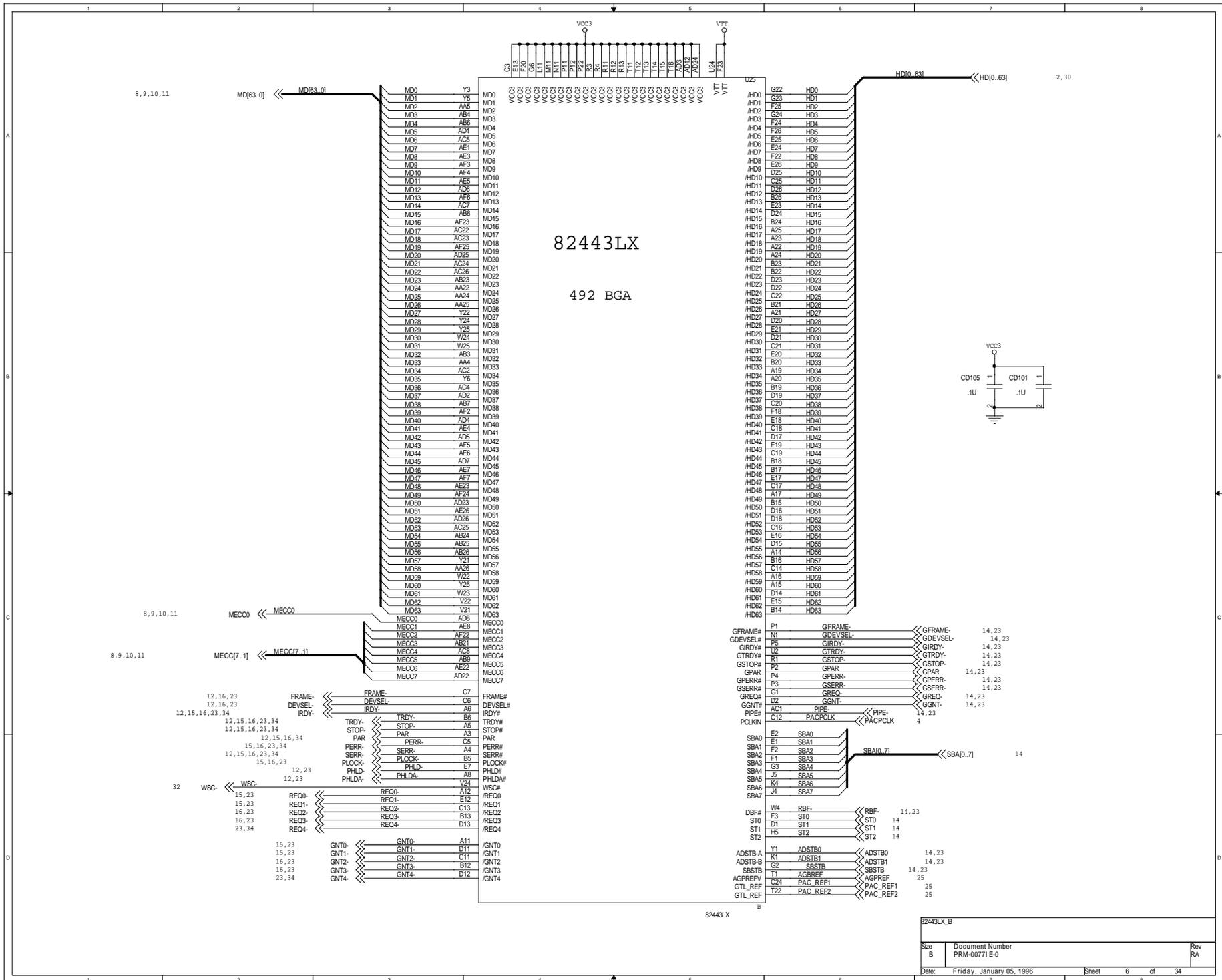




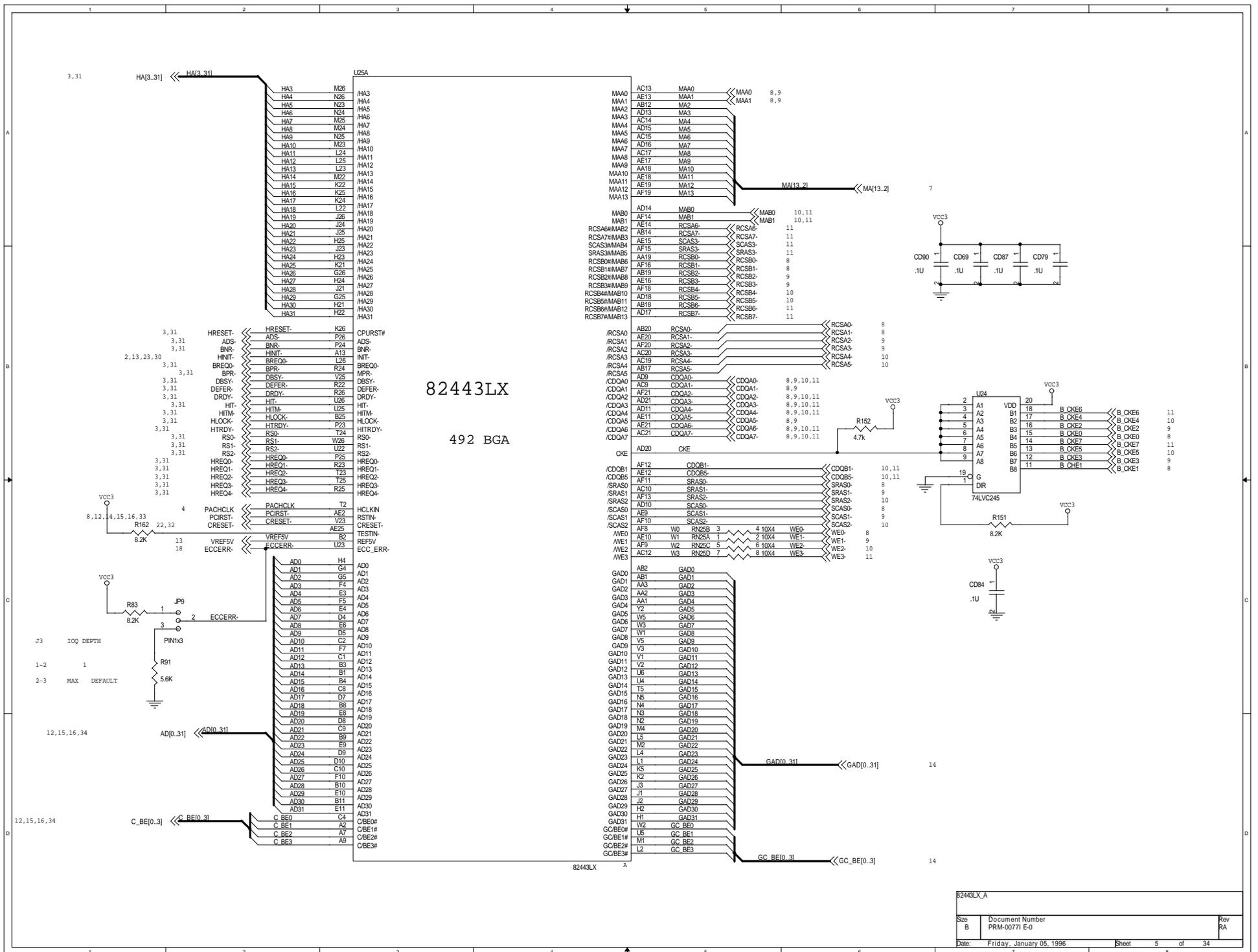
MEMORY BUFFER		
Size	Document Number	Rev
B	PRM-00771 E-0	RA
Date:	Friday, January 05, 1996	Sheet 7 of 34

82443LX

492 BGA



82443LX_B		
Size	Document Number	Rev
B	PRM-00771 E-0	RA
Date:	Friday, January 05, 1996	Sheet 6 of 34



82443LX_A		
Size	Document Number	Rev
B	PRM-00771 E-0	RA
Date:	Friday, January 05, 1996	Sheet 5 of 34



