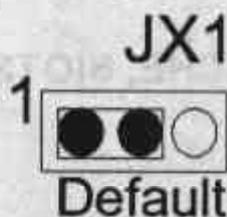


Chapter 2

- Position the notched corner of microprocessor over the notched corner of the ZIF socket and align the pins of CPU over the socket.
- Carefully insert the aligned CPU into the ZIF socket and press firmly. After CPU inserted, press ZIF retaining arm downwards.
- Examine the installed CPU to ensure it is installed in the correct direction and pin aligned properly.

□ 2.3 Set The CPU Relevant Jumpers To Correctly Configure The CPU Type, CPU Clock And CPU Voltage

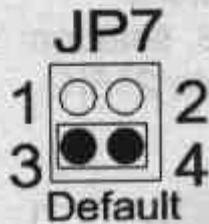


JX1: Select CPU Voltage 3.3v and 3.45v.
2-3 short for 3.3v CPU (default), 1-2 short for 3.45v CPU.

CLOCK/ CPU Mhz	JP7 (CLOCK)	JP8 (BUS)	J1 (BF0)	J3 (BF1)	CN1 (VRM)
50/75Mhz	1-2, 3-4	1-2	OPEN	OPEN	A4-A5, A6-A7
60/90Mhz	1-2	2-3	OPEN	OPEN	"
66/100Mhz (Default)	3-4	2-3	OPEN	OPEN	"
60/120Mhz	1-2	2-3	SHORT	OPEN	"
66/133Mhz	3-4	2-3	SHORT	OPEN	"
60/150Mhz	1-2	2-3	SHORT	SHORT	"
66/166Mhz	3-4	2-3	SHORT	SHORT	"
60/180Mhz	1-2	2-3	OPEN	SHORT	"
66/200Mhz	3-4	2-3	OPEN	SHORT	"

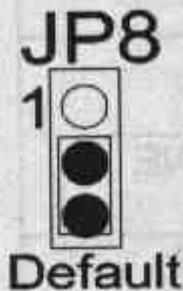
☞ Clock is System Clock, Bus Speed. CPU Mhz means Core Speed, and CPU operation at 75, 90, 100 etc.

☞ CN1 is a socket of VRM. We have put a Plug to make A4-A5, A6-A7 short. If the CPU is 2.5v or Intel offers you a daughter board with CPU, please take off the Plug and insert the daughter board in CN1.

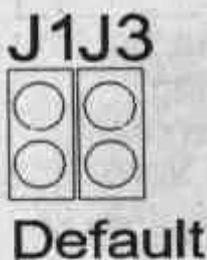


JP7: It is used to set the CPU Bus Clock.

JP7	CPU Bus Clock
3-4 short	66Mhz (Default)
1-2 short	60Mhz
1-2, 3-4 short	50Mhz



JP8: Select system AT BUS CLOCK .
2-3 short for 60/66Mhz (default).
 1-2 short for 50MHz.



J1/J3: They are used to set CPU frequency:

CLOCK CHIP FREQUENCY	J1(BF0)	J3(BF1)
1.5 TIMES (Default)	OPEN	OPEN
2.0 TIMES	SHORT	OPEN
2.5 TIMES	SHORT	SHORT
3.0 TIMES	OPEN	SHORT

For example, Pentium 100 Mhz CPU is 66Mhz Speed time 1.5. So J1 and J2 have to be set OPEN.

CN1



CN1: VRM Socket - A4-A5, A6-A7 for Intel Pentium P54C, P54CS, default. We have put a simple plug on CN1 for default setting. If you lose the plug, you can put jumpers at A4-A5 and A6-A7. When you use P55C, 2.5v, over 150Mhz, included, please take off the plug and insert a daughter board from Intel into VRM socket.

2.4 Install And Configure The System Level Two Cache Memor

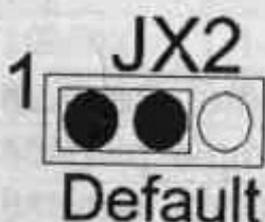
The second level (L2) of cache is installed on the board to increase the system performance. It supports asynchronous, 28/32-pin, DIP

type SRAM, U8-U15, and synchronous pipeline burst mode cache module, CN2. The COAST (Cache on A Stick), cache module, solution provides on board flexibility, allowing onboard to accommodate 256K and 512K. Please refer to the following table:

CACHE SIZE	Asynchronous / Dip Type		Synchronous/Cache Module	
	256K (Default)	512K	256K	512K
TAG SRAM (U2)	8K*8	32K*8	NO	NO
DATA SRAM	32K*8 *8	64K*8 *8	NONE	NONE
CACHE MODULE	NO	NO	YES	YES
JX2 (TAG RAM)	1-2 SHORT	2-3 SHORT	1-2 SHORT	2-3 SHORT

☞ When you plug a cache module into a 160-pin dual-readout slot, you must take off the onboard's DIP asynchronous data and tag SRAM.

SOCKET: If you use Asynchronous, DIP type 28-32pin Cache RAM. Please insert them at U8-U15 and Tag RAM at U2. But when you use Synchronous Cache, you have to take off the DIP Type Cache from U8-U15 and U2. And insert a Burst Mode Cache Module at CN2.



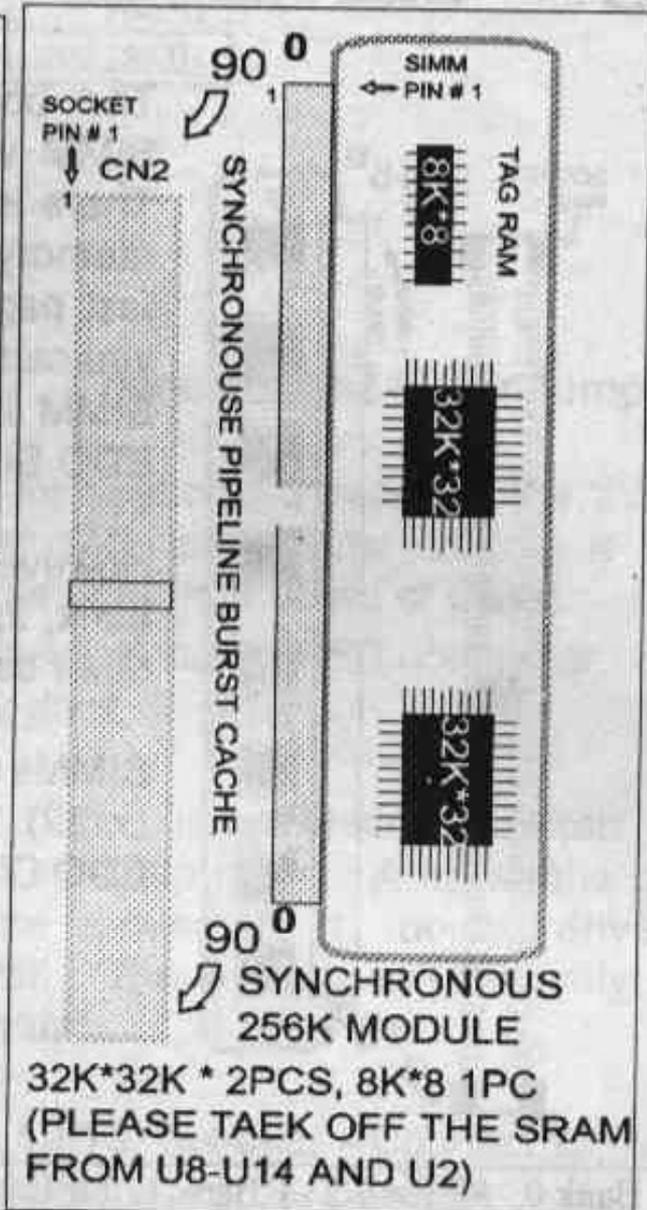
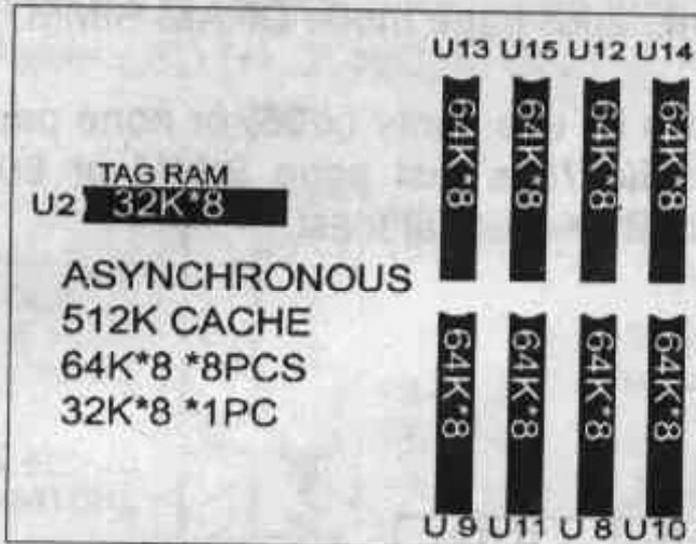
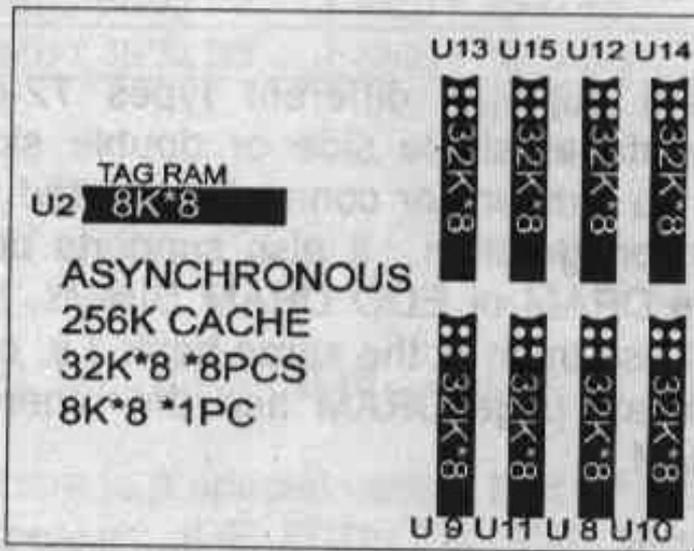
JX2: Decide Tag RAM size.

256K: 1-2 short for 256K, default.

512K: 2-3 short.

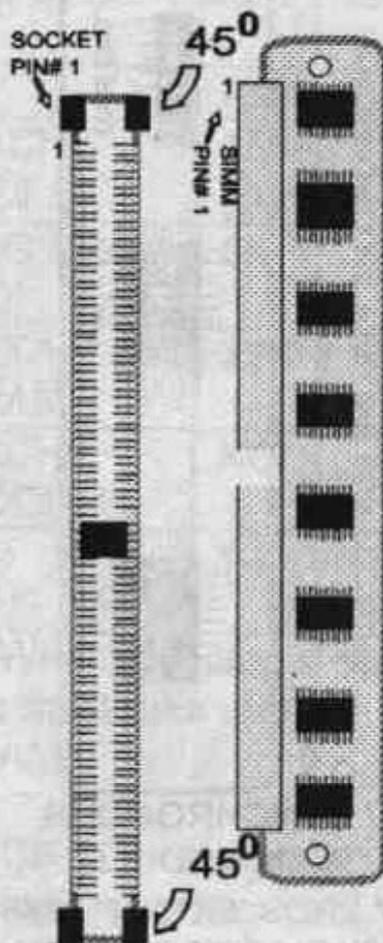
☞ If there is a Tag RAM on standard synchronous cache module, please take off the component on U2 (Tag RAM) and it is useless on JX2.

☞ If there is no Tag RAM on standard synchronous cache module, please insert a DIP type asynchronous Cache RAM on U2, and JX2 set as Tag RAM size 256K/512K.



- ☛ 256K synchronous cache module: 2pcs 32K*32 + 1pc 8K*8, single side.
- ☛ 512K synchronous cache module: 4pcs 32K*32 + 1pc 32K*8, double side (two pieces synchronous 32K*32 each side.)

2.5 Install System DRAM Memory.



The board supports different types 72-pin SIMM whatever single side or double side. There is no jumper nor connector needed for memory configuration. It also supports both fast page DRAM or EDO DRAM SIMMs, but you can't use them at the same bank, i.e. one SIMM is fast page DRAM and the other is EDO SIMM.

However, it is no problem that you use one bank, 2pcs EDO mode DRAM SIMM and the other bank, 2pcs page mode DRAM SIMM.

SIMMs can be use parity (x 36) or none parity (x 32). The 70ns fast page SIMM or 60ns EDO DRAM needed, at least.

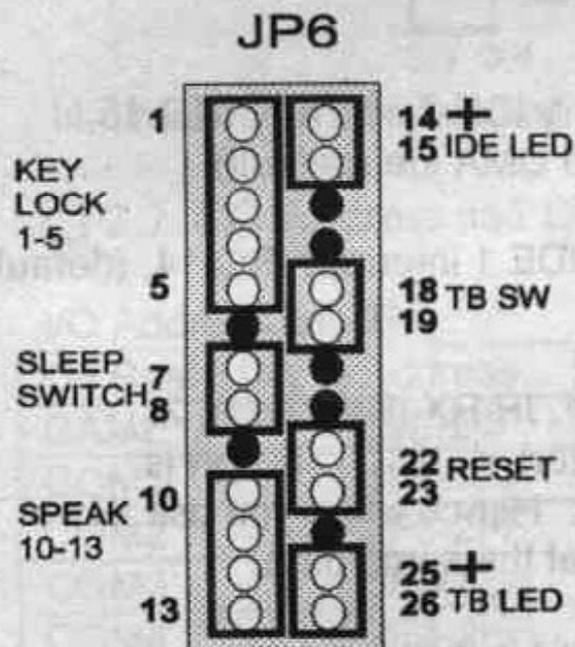
Bank 0, SIMM 1/2	Bank 1, SIMM 3/4	TOTAL
1MB * 36/32 SS	X	8MB
1MB * 36/32 SS	1MB * 36/32 SS	16MB
1MB * 36/32 SS	2MB * 36/32 DS	24MB
1MB * 36/32 SS	4MB * 36/32 SS	40MB
1MB * 36/32 SS	8MB * 36/32 DS	72MB
2MB * 36/32 DS	X	16MB
2MB * 36/32 DS	1MB * 36/32 SS	24MB
2MB * 36/32 DS	2MB * 36/32 DS	32MB
2MB * 36/32 DS	4MB * 36/32 SS	48MB
2MB * 36/32 DS	8MB * 36/32 DS	80MB
4MB * 36/32 SS	X	32MB
4MB * 36/32 SS	1MB * 36/32 SS	40MB
4MB * 36/32 SS	2MB * 36/32 DS	48MB
4MB * 36/32 SS	4MB * 36/32 SS	64MB
4MB * 36/32 SS	8MB * 36/32 DS	96MB
8MB * 36/32 DS	X	64MB
8MB * 36/32 DS	1MB * 36/32 SS	72MB

8MB * 36/32 DS	2MB * 36/32 DS	80MB
8MB * 36/32 DS	4MB * 36/32 SS	96MB
8MB * 36/32 DS	8MB * 36/32 DS	128MB

□ 2.6 Install IDE , Enhanced I/O Connector and Other Jumpers

There is a special design that JP6 is for KeyLock, Sleep/Resume SW, Speaker, IDE LCD, TB SW, Reset SW, and Turbo LED. It is convenient for you to connect the cable from front board of Case.

JP6: 1-5, KeyLock - Keyboard lock switch & power LED connector. 1. Power LED (+), 2. N/C, 3. GND, 4. Keylock, 5. GND



JP6: 7-8, Sleep/Resume Switch - Short to sleep mode. A keystroke or mouse movement (mouse driver exists). The system will instantly "wake up".

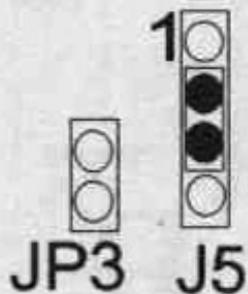
JP6: 10-13, Speaker - Connect to the system's speaker for beeping. 10. Speaker, 11. N/C, 12. GND, 13. GND.

JP6: 14-15, IDE LED Indicator - LED ON when on board PCI IDE HDD activities.

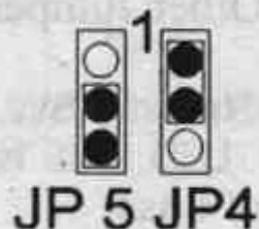
JP6: 18-19, Turbo Switch - Open for slower speed. Short for high speed. A hot key <CTRL><ALT><+> also brings system to a high speed while <CTRL><ALT><-> set system to a slow speed

JP6: 22-23, Reset - Short to restart system.

JP6: 25-26, Turbo LED Indicator - LED ON when high speed is selected



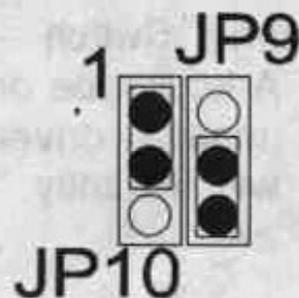
JP3/J5: Select battery clear.
JP3: Short for Dallas 1287A RTC clear.
J5: Normal RTC operation 2-3 short (default),
 3-4 short for M5818 RTC clear.



JP4: Select EPROM function - 1-2 Flash BIOS read only, 2-3 Flash BIOS writeable (AWARD 4.5PG BIOS).

JP5: Select EPROM BIOS - 2-3 for 5v flash EPROM or read only, 1-2 for 12v flash EPROM writeable.

Factory normally uses 5v flash ROM, not recommend 12v . Upgrade program on disk AWARD.BIO, subdirectory file name AWDFLASH.EXE, BIOS file *.BIN or get newest BIOS files from BBS!



JP9: Onboard IDE 2:

1-2 to enable Secondary IDE 2 interrupt IRQ 15,
 2-3 MIRQ0 for PIO and DMA ide (default)

JP10: Onboard IDE 1:

1-2 to enable Primary IDE 1 interrupt IRQ 14, (default)
 2-3 no IRQ.



JP13: Infrared (IR) port - 1. IR RX (Receiver), 2. GND, 3. IR TX (Transmitter), 4. VCC. IR port is using COM2 port function. Hence when you use IR, you can't use COM2 port at the same time.



J2: CPU NA - always short for CPU piple line .
 (Non installed)



Mouse: PS/2 mouse port.

5-pin Mouse:

Pin #	Pin 1	Pin 2	Pin 3	Pin 5
Pin Name	Data	Clock	GND	VCC
Cable Color	Red	Blue	Green	Yellow