ADLINK TECHNOLOGY INC.

CoreModule® 745
Single Board Computer
Reference Manual

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Notice Page

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REVISION HISTORY

Revision	Reason for Change	Date
1000	Initial Release	Nov/10
1010	Replaced N450, D410, and D510 CPUs with N455 and D525; added JP3 and JP4 to Table 2-3 and removed JP1 (CMOS reset); changed J10 to J19 in Table 3-10 caption; revised Table 3-9 caption to J10; revised voltage of battery in Table 3-17 from 5V to 3.3V; changed width in Table 2-4 from 3.76" to 3.8"; added heatsink dwg and table; changed pitch in Table 3-15 to 0.079"; revised Ethernet Interface description on page 27; added Gb Ethernet controller to table Table 3-14; revised Appendix A address information	Mar/12
1020	Added airflow diagrams to "Thermal/Cooling Requirements" on page 16; added details to descriptions of Copper and Aluminum heatsink qualifications in Table 2-7; changed Serial Console to Remote Access in Chapter 3; changed voltage of battery header to +3.0; updated contact addresses in Appendix A	Oct/13

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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

Contents

List of Figures

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Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the CoreModule® 745 Single Board Computer (SBC). This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- Product Overview
- Hardware Specifications
- BIOS Setup information
- Technical Support Contact Information

Information not provided in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals
- Pinout definitions for industry standard interfaces

References

The following list of references may help you successfully complete your custom design.

Specifications

- PC/104 Specification, Revision 2.5, November, 2003
- PC/104-Plus Specification, Revision 2.0, November, 2003

  For latest revision of the PC/104 specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org
- PCI 2.3 Compliant Specifications, Revision 2.3, March 29, 2002

  For latest revision of the PCI specifications, contact the PCI Special Interest Group at:

  Web site: http://www.pcisig.com
- AMI BIOS Core 8 User's Guide

  Web site: http://www.ami.com/support/doc/MAN-EZP-80.pdf

Chip Specifications

The following integrated circuits (ICs) are used in the CoreModule 745 single board computer:

- Intel® Corporation and the Atom™ N400 and D500 series processors

  Web site: http://www.intel.com/p/en_US/embedded/hwsw/hardware/atom-400-500/hardware
- Intel Corporation and the ICH8-M chip, used for the I/O Hub (Southbridge)

  Data sheet: http://www.intel.com/assets/pdf/datasheet/313056.pdf
- SMSC and the Super I/O SCH3112I-NU chip used for the Super I/O controller

  Data sheet: http://www.smsc.com/media/Downloads_Public/Data_Briefs/311xdb.pdf

- Intel Corporation and the 82574IT chip used for the Gigabit Ethernet controller

  Datasheet: http://download.intel.com/design/network/datashts/82574.pdf

- Linear Technology and the LTC1334CG, RS-232/422/485 Serial Port transceiver

  Web site: http://www.linear.com/products/rs485%7C422_transceivers

- Analog devices and the ADM213EARSZ, RS-232 Serial Port transceiver

  Web site: http://www.analog.com/en/interface/rs-232/adm213e/products/product.html

- Greenliant and the GLS85LP1004P Solid State Drive (SSD)

  Web site: http://www.greenliant.com/products/?inode=46780

- Integrated Technology Express, Inc. and the PCI-to-ISA bridge, IT8888G-L

  Web site: http://www.iteusa.com or http://www.ite.com.tw

NOTE	If you are unable to locate the datasheets using the links provided, go to the manufacturer's web site where you can perform a search using the chip datasheet number or name listed.

Chapter 2 Product Overview

This introduction presents general information about the PC/104 architecture and the CoreModule 745 Single Board Computer (SBC). After reading this chapter you should understand:

- PC/104 architecture
- Product description
- CoreModule 745 features
- Major components (ICs)
- Headers and Connectors
- Specifications

PC/104 Architecture

The PC/104 architecture affords a great deal of flexibility in system design. You can build a simple system using only a CoreModule 745 SBC, input/output devices connected to the serial, USB, or SATA ports, and the on-board Solid State Disk storage device. To expand a simple CoreModule system, simply add self-stacking PC/104 and PC/104-Plus expansion boards to provide additional capabilities, such as:

- Additional serial and parallel ports
- Analog or high-speed digital I/O
    - Data Acquisition (Analog In/Out)
    - USB 2.0 expansion modules
    - IEEE 1394 (FireWire) expansion modules
    - Standard VGA video output

PC/104 or PC/104-Plus expansion modules can be stacked with the CoreModule 745 avoiding the need for large, expensive card cages and backplanes. The PC/104-Plus expansion modules can be mounted directly to the PC/104 and PC/104-Plus connectors of the CoreModule 745. PC/104-compliant modules can be stacked with an inter-board spacing of ~0.6 inches, so that a 3-module system fits in a 3.6" x 3.8" x 2.4" space. See Figure 2-1.

One or more MiniModule products or other PC/104 modules can be installed on the CoreModule expansion connectors, so that the expansion modules fit within the CoreModule outline dimensions. Most MiniModule products have stackthrough connectors compatible with the PC/104-Plus Version 2.0 specification. Several modules can be stacked on the CoreModule headers. Each additional module increases the thickness of the package by ~17mm (0.66"). See Figure 2-1.

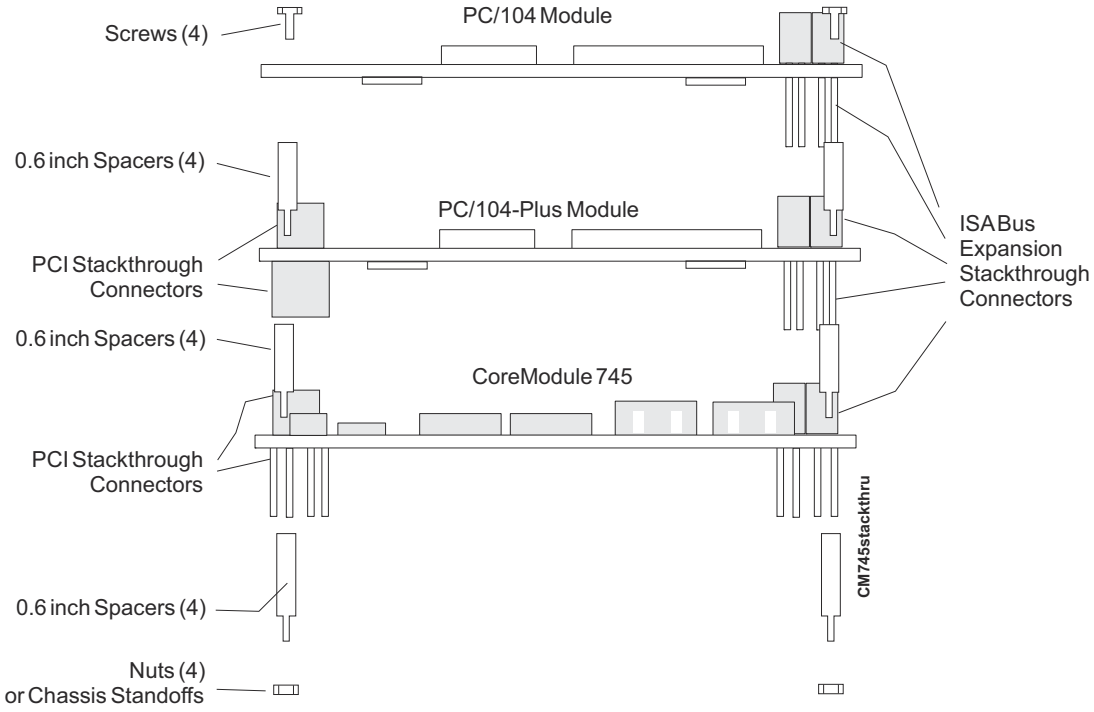


Figure 2-1. Stacking PC/104-Plus Modules with the CoreModule 745

Product Description

The CoreModule 745 SBC is an exceptionally high integration, high performance, Intel® Atom™ N455 or D525 processor based system, compatible with the PC/104 standard. This rugged and high quality single-board system contains all the component subsystems of an ATX motherboard plus the equivalent of several PCI expansion boards.

The Intel Atom N400 and D500 series CPUs integrate processor cores with Graphics and Memory Hubs (GMHs), providing low-power, high-performance processors, memory controllers for up to 2GB DDR3 memory, and graphics controllers which provide LVDS and VGA signals for most LCD video panels and CRT monitors.

The ICH8-M chipset provides controllers for the I/O Hub (Southbridge) featuring four USB ports, two SATA ports, one Ultra DMA 33/66/100 IDE port supporting two IDE devices, one SMBus port, one SPI port, one GPIO port, one PCIe bus for Gigabit Ethernet, and one PCI bus for PC/104 and PC/104-plus devices. The CoreModule 745 provides legacy interfaces through the SMSC SCH3112I-NU Super I/O featuring three serial ports and a PS/2 keyboard and mouse port.

The CoreModule 745 can be expanded through the PCI expansion bus using the PC/104 and PC/104-Plus connectors for additional system functions. This bus offers compact, self-stacking, modular expandability. The PC/104 bus is an embedded system version of the signal set provided on a desktop PC's ISA bus. The PC/104-Plus bus includes this signal set plus additional signals implementing a PCI bus, available on a 120-pin (4 rows of 30 pins) PCI expansion bus connector. This PCI bus operates at a clock speed of 33MHz.

The CoreModule 745 is particularly well suited to either embedded or portable applications and meets the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with ADLINK MiniModules™ or other PC/104-compliant expansion modules, or it can be used as a powerful computing engine. The CoreModule 745 requires a single +5V AT power source.

Module Features

- CPU
  - Provides an Intel Atom 1.67GHz N455 or 1.83GHz D525 processor core
  - DMI (Direct Media Interface) with 1 GB/s of bandwidth in each direction
  - Enhanced SpeedStep® technology
  - On die 512-kB, 8-way L2 cache
- Memory
  - Single standard 204-pin DDR3 SODIMM socket
  - Supports +1.5V DDR3, 800MHz RAM up to 2GB
  - Supports non-ECC, unbuffered memory
- Interface Buses
  - PC/104 and PC/104-Plus Interfaces
  - PC/104 bus speeds up to 8MHz (16-bit ISA Bus)
  - PC/104-Plus bus speed at 33MHz (32-bit PCI Bus)
  - PCI 2.2 compliant
- IDE Channel
  - Supports one enhanced IDE controller
  - Supports on-board Solid State Drive (SSD) with default 4GB capacity
- SATA
  - Supports two SATA ports from the ICH8-M I/O Hub
  - Provides two standard SATA connectors
- Serial Ports
  - Provide three buffered serial ports with full handshaking
  - Provide 16550-equivalent controllers, each with a built-in 16-byte FIFO buffer
  - Support full modem capability
  - Support RS-232 operation
  - Support RS-232, RS-485, or RS-422 operation on two ports (COM1 and COM2)
  - Support programmable word length, stop bits, and parity
  - Support 16-bit programmable baud-rate generator and an interrupt generator
- USB Interface
  - Provides two root USB hubs
  - Provides up to four USB ports
  - Supports USB boot devices
  - Supports USB v2.0 EHCI and v1.1 UHCI
  - Supports over-current detection status
- Keyboard/Mouse Interface
  - Provides PS/2 keyboard interface
  - Provides PS/2 mouse interface

- Ethernet Interface
  - Provides one fully independent Ethernet port
  - Provides integrated LEDs (Link/Activity and Speed)
  - Provides one Intel 82574IT controller chips
  - Provides header for LAN LED signals (gigabit only)
  - Supports IEEE 802.3 10/100BaseT and 10/100/1000BaseT compatible physical layers
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full duplex mode
    - Half-duplex mode supports enhanced proprietary collision reduction mode
- Video Interfaces (VGA and LVDS)
  - Provide VGA outputs (resolutions up to 1400x1050 @ 60Hz for the N455 CPU and 2048x1536 @ 60Hz for the D525 CPU)
  - Provide LVDS flat panel outputs (resolutions up to 1280x800 for the N455 CPU and 1366x768 for the D525 CPU) [single channel, three differential signals]
- Utility Interface
  - Power Button
  - Reset Switch
  - Speaker
- Miscellaneous
  - Battery-less boot
  - Oops! Jumper support
  - Remote Access support
  - Watchdog Timer
  - Logo Screen (Splash)

Block Diagram

Figure 2-2 shows the functional components of the CoreModule 745.

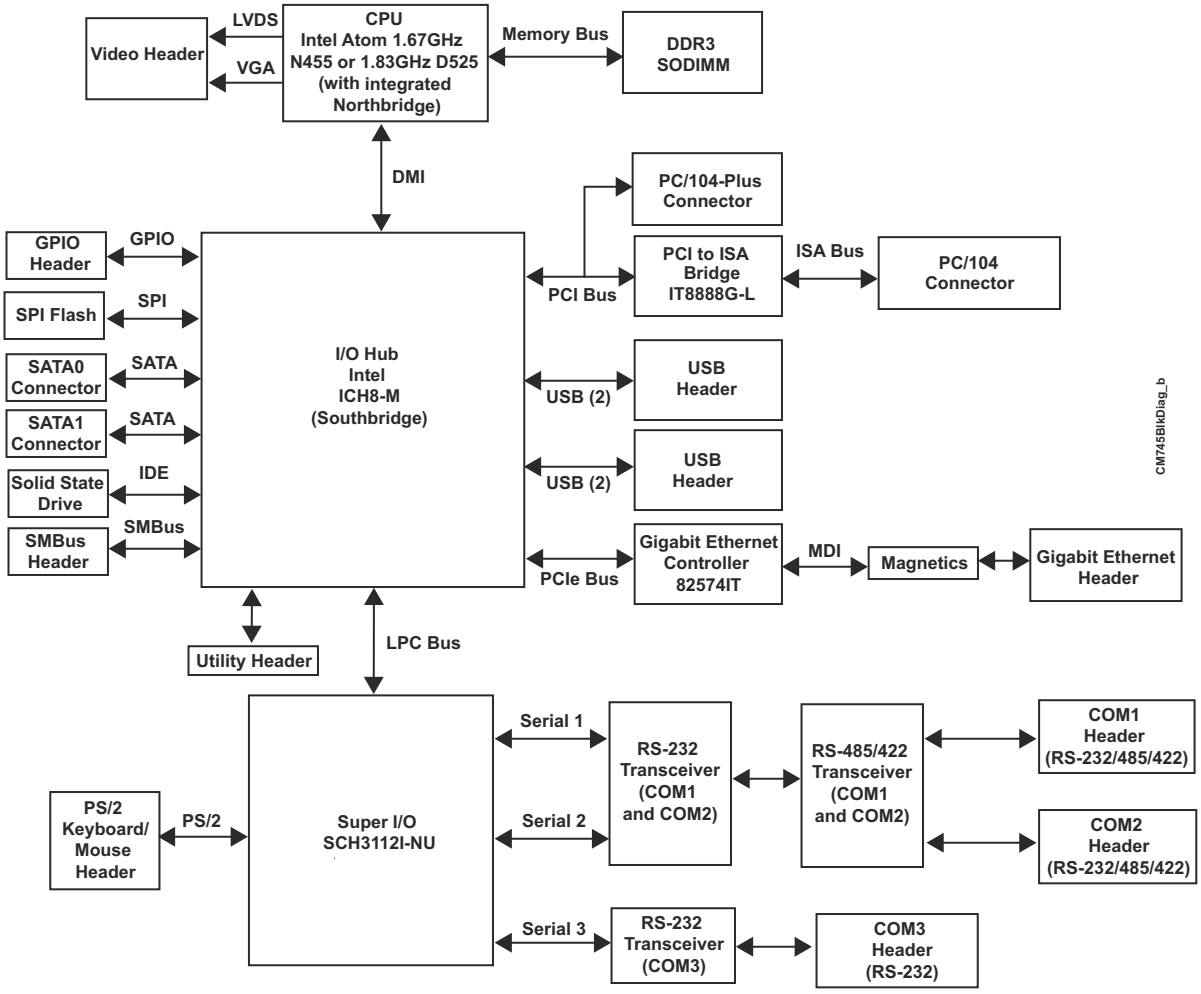


Figure 2-2. Functional Block Diagram

Major Component (ICs) Definitions

Table 2-1 lists the major ICs, including a brief description of each, on the CoreModule 745. Figures 2-3 and 2-4 show the locations of the major ICs.

Table 2-1. Major Component Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel	Atom N455 or D525	1.67GHz or 1.83GHz processor with 8-way L2 cache	Integrates Processor core and Graphics Memory Controller Hub
I/O Hub (U2)	Intel	82801HBM (ICH8-M)	I/O Hub for some common user interfaces	Provides Southbridge interfaces and off loads some Northbridge functions from the CPU
Gigabit Ethernet Controller (U4)	Intel	82574IT	Gigabit Ethernet controller	Generates PCIe 10T/100TX/ 1000T Ethernet signals
PCI-to-ISA Bridge (U8)	ITE	ITE8888G-L	Interface between PCI bus and ISA bus	Migrates legacy ISA bus
Super I/O Hub (U9)	SMSC	SCH3114I-NU	Super I/O controller	Provides complete legacy Super I/O functionality
RS-232 Transceiver (U11 - on bottom side) [see Figure 2-4]	Analog Devices	ADM213EARSZ	Transceiver for Serial 1 and Serial 2 RS-232 signals	Transmits and receives RS-232 signals for COM1 and COM2
RS-422/485 Transceiver (U12 - on bottom side) [see Figure 2-4]	Linear Technology	LTC1334CG	Transceiver for Serial 1 and Serial 2 RS-485/ 422 signals	Transmits and receives RS-485/422 signals for COM1 and COM2
CPLD (U17 - on bottom side) [see Figure 2-4]	Xilinx	XC9536XL	Complex Programmable Logic Device (not user programmable)	Provides control for Power Sequencing
SPI Flash (U32) - on bottom side [see Figure 2-4]	Winbond	W25Q64BVSSIG	Serial Peripheral Interface Flash Memory chip (for firmware)	Stores BIOS in Flash Memory
SSD (Solid State Drive, U33 - on bottom side [see Figure 2-4])	Greenliant	GLS85LP1004P	Industrial-grade, soldered solid-state storage module	Provides solid state storage through the IDE channel

Table 2-1. Major Component Descriptions and Functions (Continued)

RS-232 Transceiver (U38 - on bottom side) [see Figure 2-4]	Analog Devices	ADM213EARSZ	Transceiver for Serial 3 RS-232 signals	Transmits and receives RS-232 signals for COM3
Ethernet Transformer (T1)	Wurth Elektronik	7490200110	Gigabit Ethernet Magnetics	Provides electrical isolation for Gigabit Ethernet controller

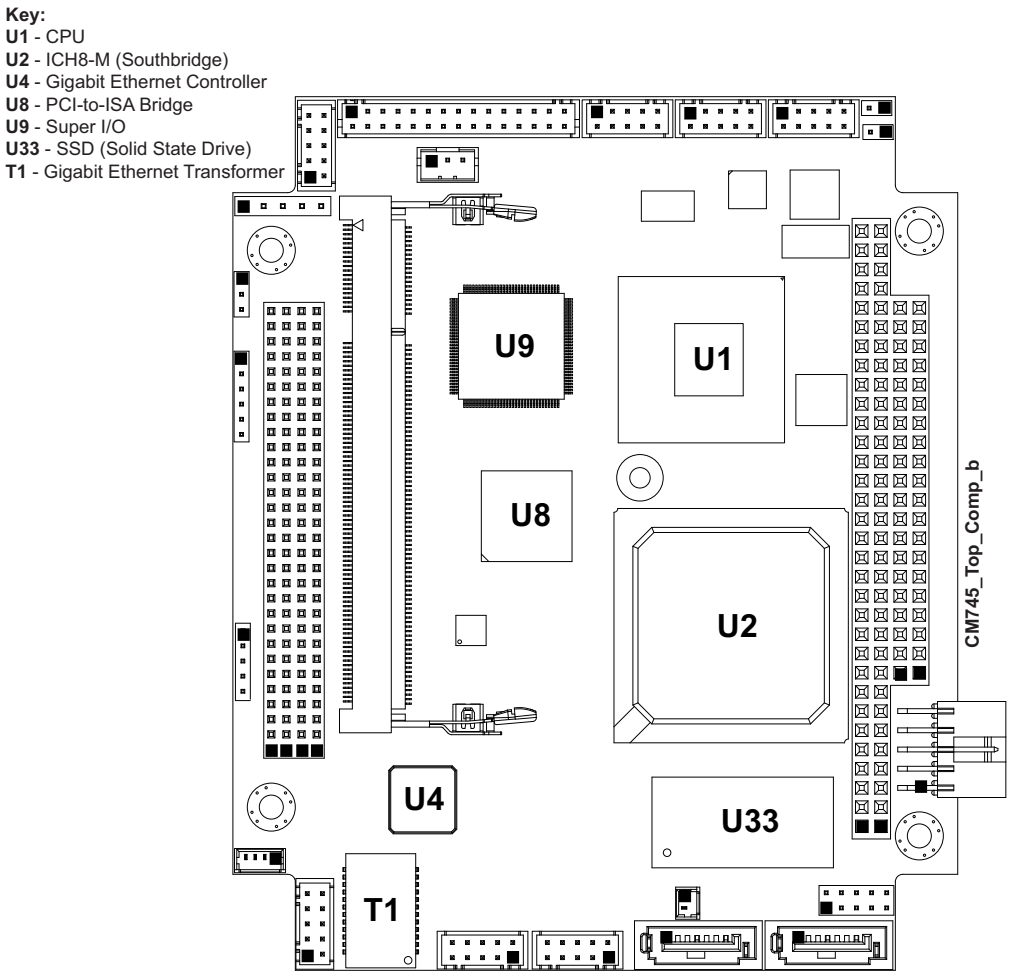


Figure 2-3. Component Locations (Top Side)

Key:
U11 - RS-232 Transceiver (COM1 and COM2)
U12 - RS-422/485 Transceiver (COM1 and COM2)
U17 - CPLD (Complex Programmable Logic Device)
U32 - SPI Flash
U38 - RS-232 Transceiver (COM3)

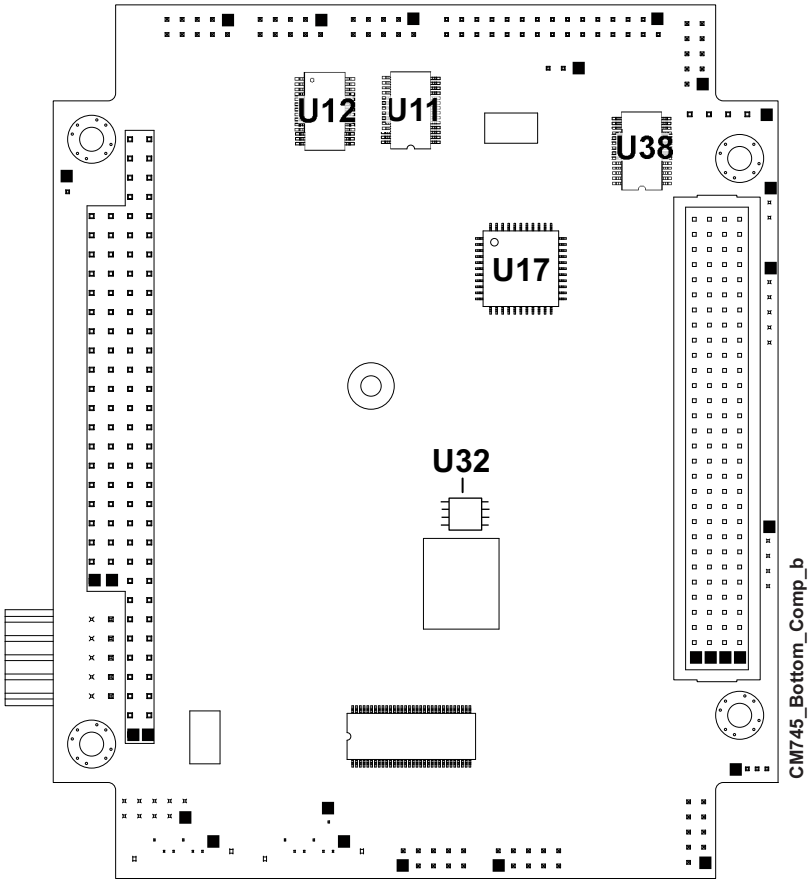


Figure 2-4. Component Locations (Bottom Side)

Header, Connector, and Socket Definitions

Table 2-2 describes the headers and connectors of the CoreModule 745 shown in Figure 2-6.

Table 2-2. Module Header, Connector, and Socket Descriptions

Header #	Board Access	Description
J1 A, B, C, D – PC/104-Plus	Top/Bottom	120-pin, 0.079" (2mm) connector used for PC/104-Plus signals
J2 A, B, C, D – PC/104	Top/Bottom	104-pin, connector used for PC/104 signals
J3 – COM1 Serial	Top	10-pin, 0.079" (2mm) shrouded header used for COM1 signals
J4 – COM2 Serial	Top	10-pin, 0.079" (2mm) shrouded header used for COM2 signals
J5 – COM3 Serial	Top	10-pin, 0.079" (2mm) shrouded header used for COM3 signals
J6 – Battery	Top	2-pin, 0.049" (1.25mm) shrouded header for power from external battery

Table 2-2. Module Header, Connector, and Socket Descriptions (Continued)

J7 – Power	Top	10-pin, 0.100" (2.54mm), right-angle, shrouded header used for external power connection
J8 – SATA0	Top	7-pin, 0.050" (1.27mm) standard connector used for SATA devices
J9 – SATA1	Top	7-pin, 0.050" (1.27mm) standard connector used for SATA devices
J10 – Ethernet	Top	10-pin, 0.079" (2mm) shrouded header used for Gigabit Ethernet signals
J11 – Ethernet LED	Top	4-pin, 0.049" (1.25mm) shrouded header used for Gigabit Ethernet LED signals
J12 – NS	Bottom	Not Supported
J14 – DNP	Top	Do Not Populate
J15 – Keyboard/Mouse	Top	10-pin, 0.079" (2mm), shrouded header for PS/2 keyboard and mouse signals
J16 – USB0 and USB1	Top	10-pin, 0.079" (2mm), shrouded header for USB0 and USB1 signals
J17 – USB2 and USB3	Top	10-pin, 0.079" (2mm), shrouded header for USB2 and USB3 signals
J18 – GPIO	Top	10-pin, 0.079" (2mm) header for General Purpose IO signals
J19 – Video	Top	30-pin, 0.079" (2mm), shrouded header for LVDS and VGA video signals
J20 – SMBUS	Top	5-pin, 0.079" (2mm), single-row header for SMBus signals
J22 – Fan	Top	3-pin, 0.079" (2mm), shrouded header for System Fan signals
J23 – Utility	Top	5-pin, 0.100" (2.54mm), single-row header for Power Button, Reset Switch, and Speaker signals
J24 – DDR3 SODIMM	Top	204-pin, standard socket for DDR3 SODIMM

NOTE The pinout tables in Chapter 3 of this manual identify pin sequence using the following method: A 30-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as 30-pin, 2 rows, odd/even (1, 2) sequence. The second number in the parenthesis is always directly across from pin 1. See Figure 2-5.

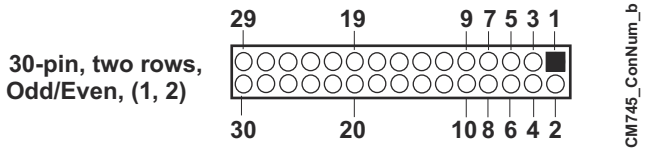
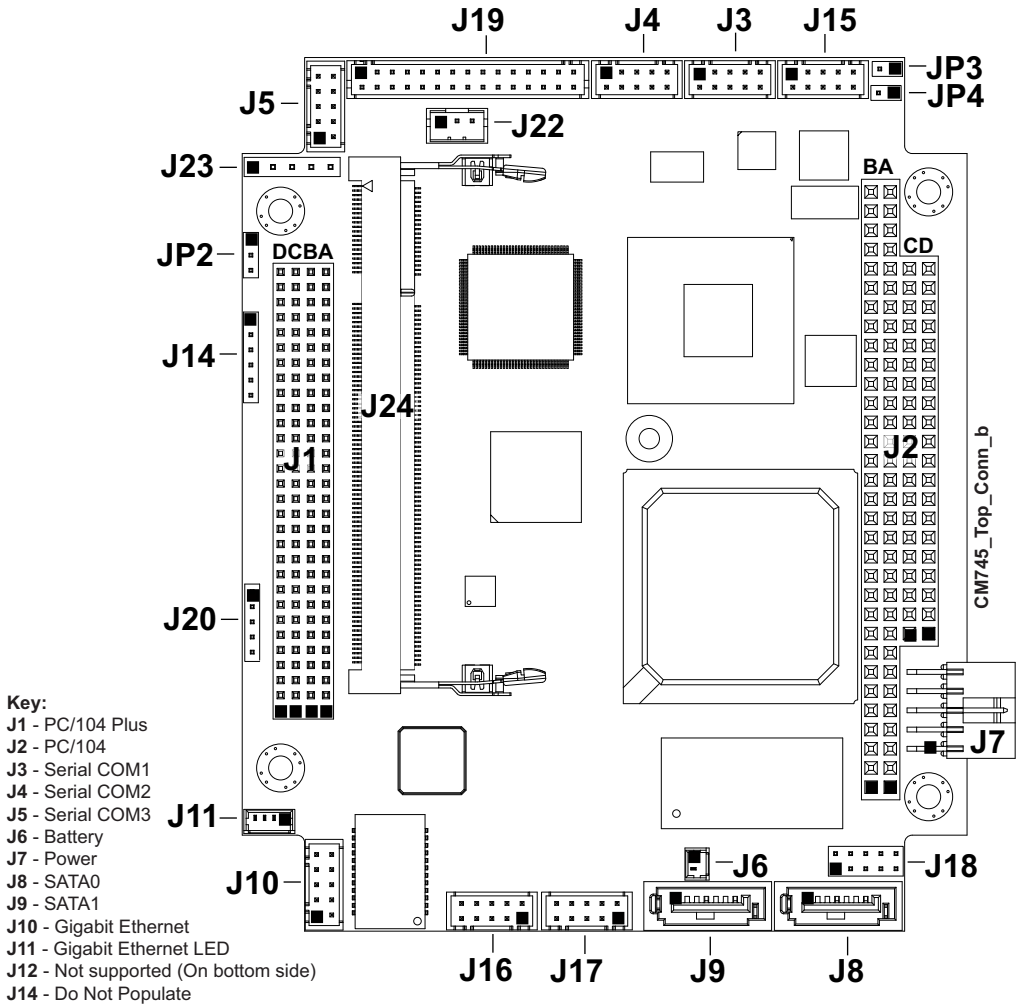


Figure 2-5. Connector Pin Sequences



Key:
J1 - PC/104 Plus
J2 - PC/104
J3 - Serial COM1
J4 - Serial COM2
J5 - Serial COM3
J6 - Battery
J7 - Power
J8 - SATA0
J9 - SATA1
J10 - Gigabit Ethernet
J11 - Gigabit Ethernet LED
J12 - Not supported (On bottom side)
J14 - Do Not Populate
J15 - Keyboard and Mouse
J16 - USB0 and USB1
J17 - USB2 and USB3
J18 - GPIO
J19 - Video (LVDS and VGA)
J20 - SMBus
J22 - Fan
J23 - Utility
J24 - DDR3 SODIMM
JP2 - LVDS Voltage Select (See jumper table)
JP3 - Serial 2 RS-485/422 Termination (See jumper table)
JP4 - Serial 1 RS-485/422 Termination (See jumper table)

Figure 2-6. Header, Connector, and Socket Locations (Top Side)

Jumper Header Definitions

Table 2-3 describes the jumper headers shown in Figure 2-7. All jumper headers provide 0.079" (2mm) pitch.

Table 2-3. Jumper Settings

Jumper Header	Installed	Removed/Installed
JP2 – LVDS Voltage Selection	Enable +3.3V (Pins 1-2) **[Default]**	Enable +5V (Pins 2-3)
JP3 – Serial 2 RS-485/422 Termination	Enable Termination (Pins 1-2)	Disable Termination (Removed) **[Default]**
JP4 – Serial 1 RS-485/422 Termination	Enable Termination (Pins 1-2)	Disable Termination (Removed) **[Default]**

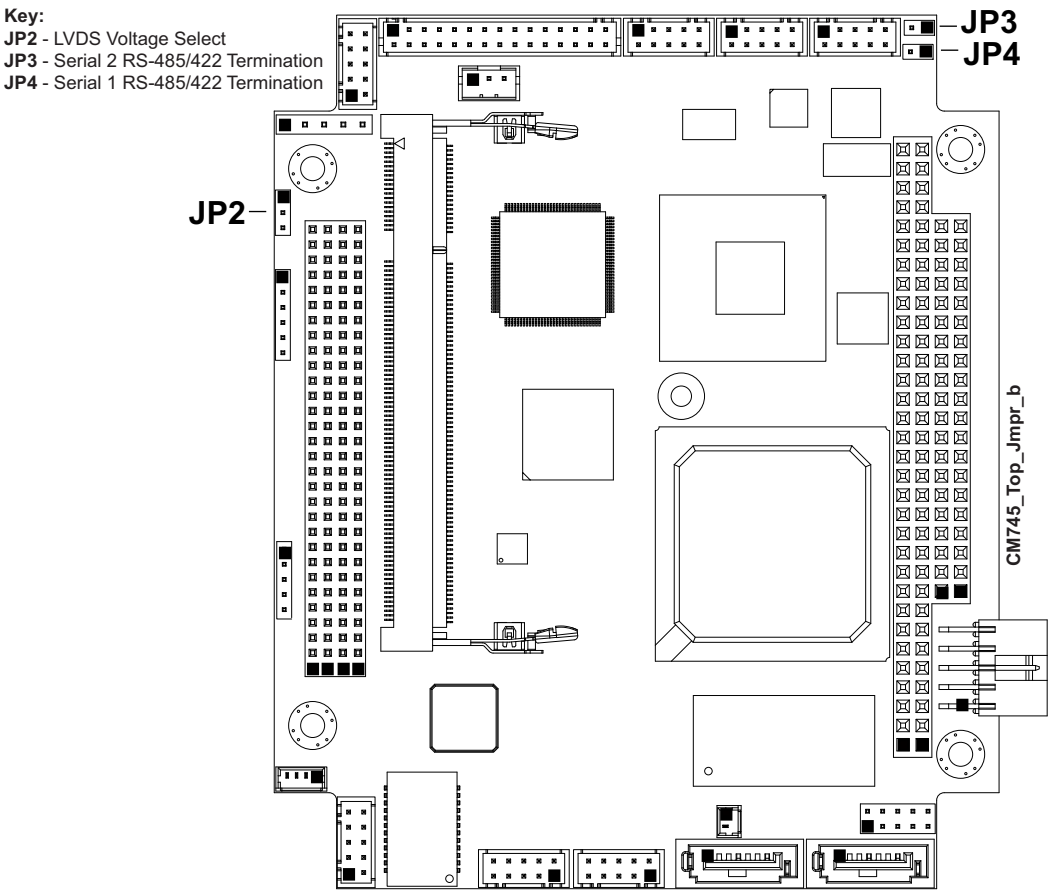


Figure 2-7. Jumper Header Locations (Top Side)

Specifications

Physical Specifications

Table 2-4 provides the physical dimensions of the CoreModule 745.

Table 2-4. Weight and Footprint Dimensions

Item	Dimension
Weight	0.12 kg (0.25 lbs)
Height (overall)	11.05 mm (0.435 inches)
Board thickness	2.362 mm (0.093 inches)
Width	96.01 mm (3.78 inches)
Length	115.57 mm (4.55 inches)

NOTE Overall height is measured from the upper board surface to the highest permanent component (PC/104 bus connector) on the upper board surface. This measurement does not include the heatsink, which can vary. The heatsink could increase this dimension. Component height should not exceed 0.345" (8.763mm) from the upper surface of the board and 0.190" (4.826mm) from the lower surface of the board. See Figure 2-9 for the stack heights of the heatsinks on the board.

Mechanical Specifications

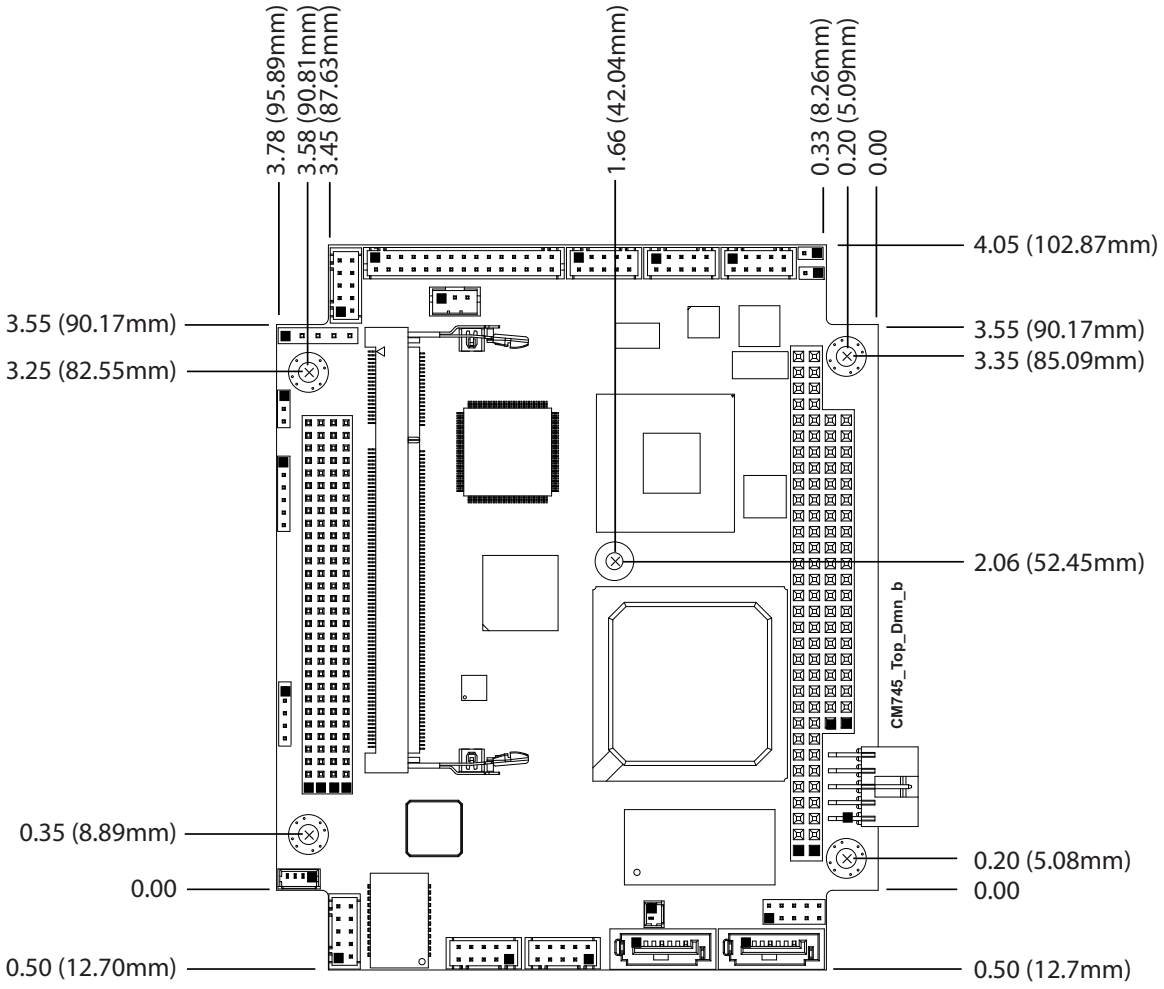


Figure 2-8. Mechanical Overview (Top Side)

NOTE	All dimensions are given in inches. Pin 1 is shown as a black square on headers and connectors. Black squares on right-angle headers indicate pin 2 in top-side views and pin 1 in bottom-side views.

Power Specifications

Table 2-5 provides the power requirements for the CoreModule 745.

Table 2-5. Power Supply Requirements

Parameter	1.67GHz N455 Characteristics	1.83GHz D525 Characteristics
Input Type	Regulated DC voltages	Regulated DC voltages
Typical In-rush Current (Peak)	8.00A (40.00W)	8.00A (40.00W)
Typical Idle Current	1.59A (7.96W)	2.20A (10.98W)
BIT Current	2.76A (13.82W)	3.73A (18.65W)

Operating configurations:

- In-rush operating configuration includes video, 2GB DDR3 RAM, and power.
- Idle operating configuration includes In-rush configuration as well as connected one external SATA HDD (Windows XP), one PS/2 keyboard, and one PS/2 mouse.
- BIT (Burn-In-Test) operating configuration includes Idle configuration as well as a second SATA HDD, one Ethernet connection, two USB loop-back testers, one external USB CF reader, one USB flash thumb drive, and three serial loop backs.

Environmental Specifications

Table 2-6 provides the most efficient operating and storage condition ranges required for this module.

Table 2-6. Environmental Requirements

Parameter	Conditions
Temperature	
Operating	–20° to +70° C (–4° to +158° F)
Extended (Optional)	–40° to +85° C (–40° to +185° F)
Storage	–55° to +85° C (–67° to +185° F)
Humidity	
Operating	5% to 90% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing

Thermal/Cooling Requirements

The CPU and PCH are the primary sources of heat on the board. The CoreModule 745 is designed to operate at the maximum speed of the CPU and requires various cooling solutions, depending on the CPU model. See Table 2-7 for descriptions of the cooling solution options. Figure 2-10 provides simulation charts of airflow requirements for both heatsinks.

Table 2-7. ADLINK Optional Cooling Solutions

Cooling Solution	Description
Passive Heatsink - Copper (without fan)	Qualified to maintain optimal performance between -40°C and +85°C. CPU throttles to 1000MHz. (**Note**: The D525 CPU is qualified only for -20°C to +70°C with a copper heatsink.)
Passive Heatsink - Aluminum (without fan)	Qualified to maintain optimal performance between -20°C and +70°C. Airflow requirement: 2 m/s. (**Note**: The D525 CPU is not qualified to use an aluminum heatsink.)
Active Heatsink (with fan)	Qualified to maintain optimal performance between -40°C and +85°C. (**Note**: The D525 CPU requires an active heatsink for temperatures between +70°C and +85°C.)

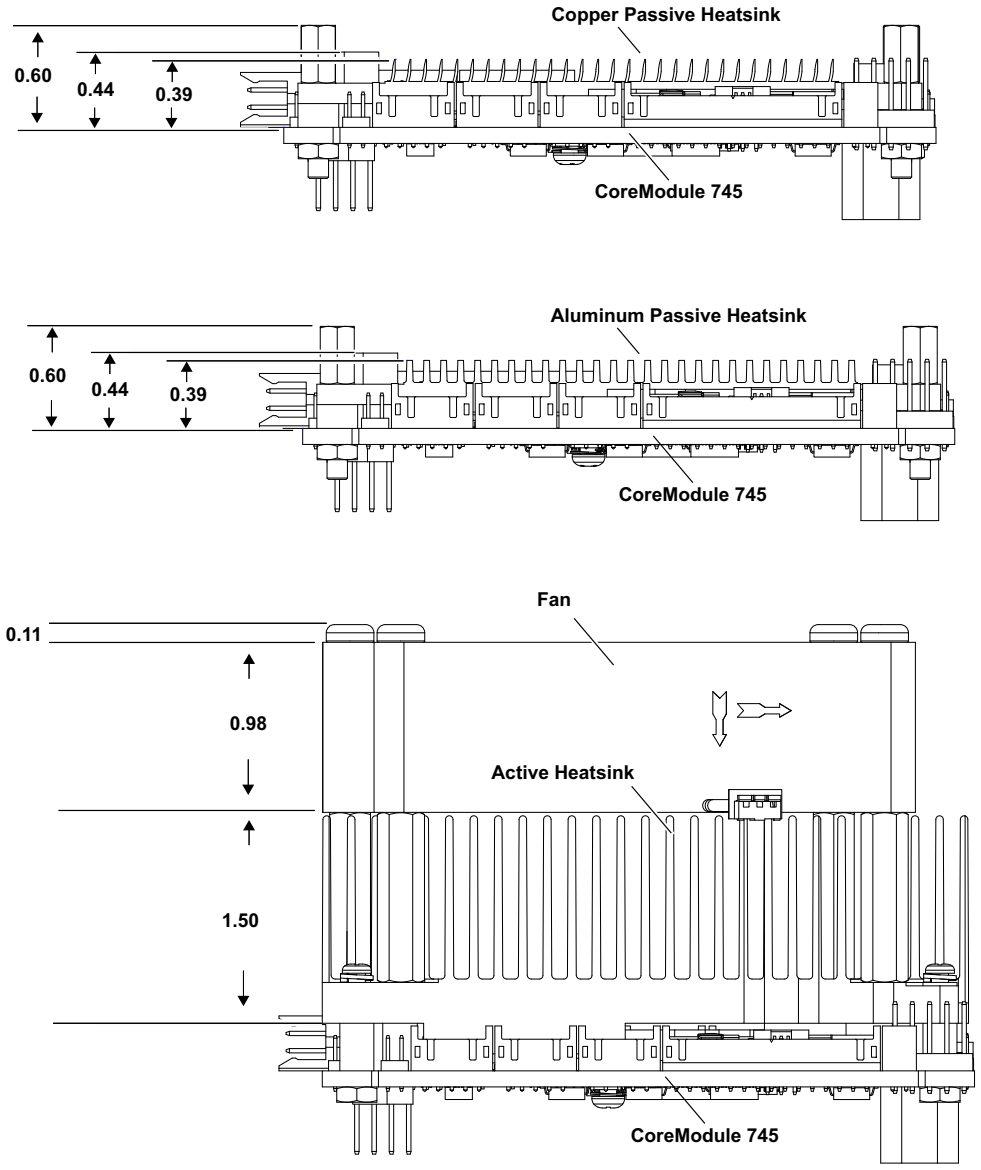
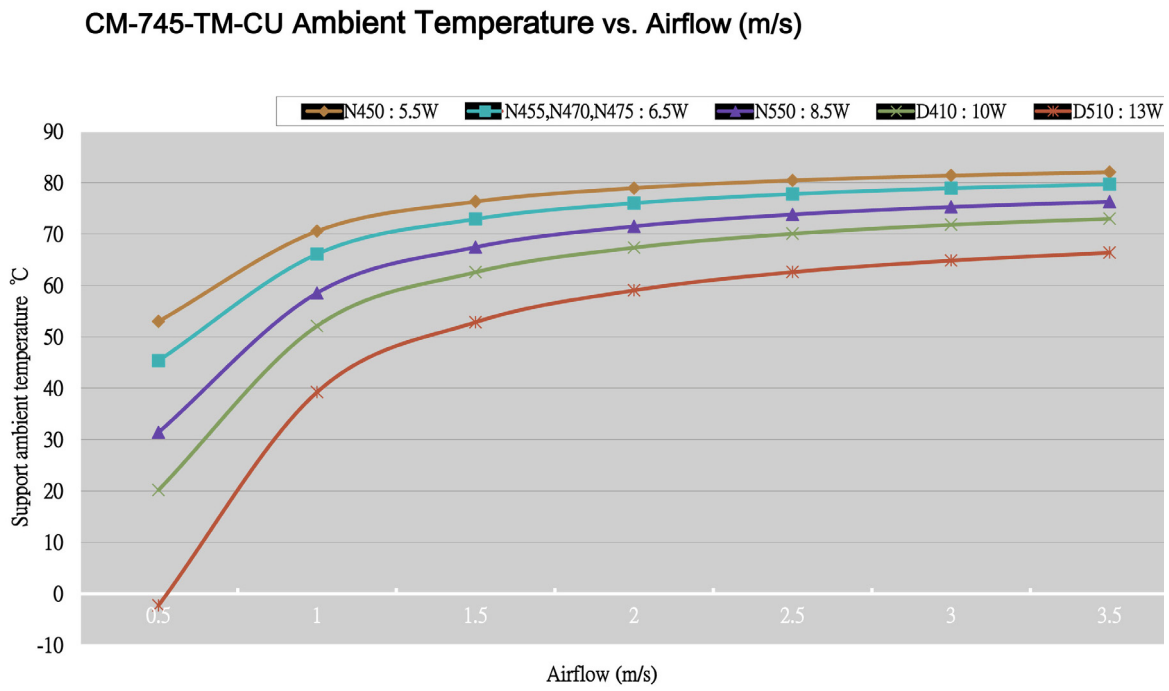


Figure 2-9. Stack Height of Cooling Assembly

NOTE All heights are given in inches.



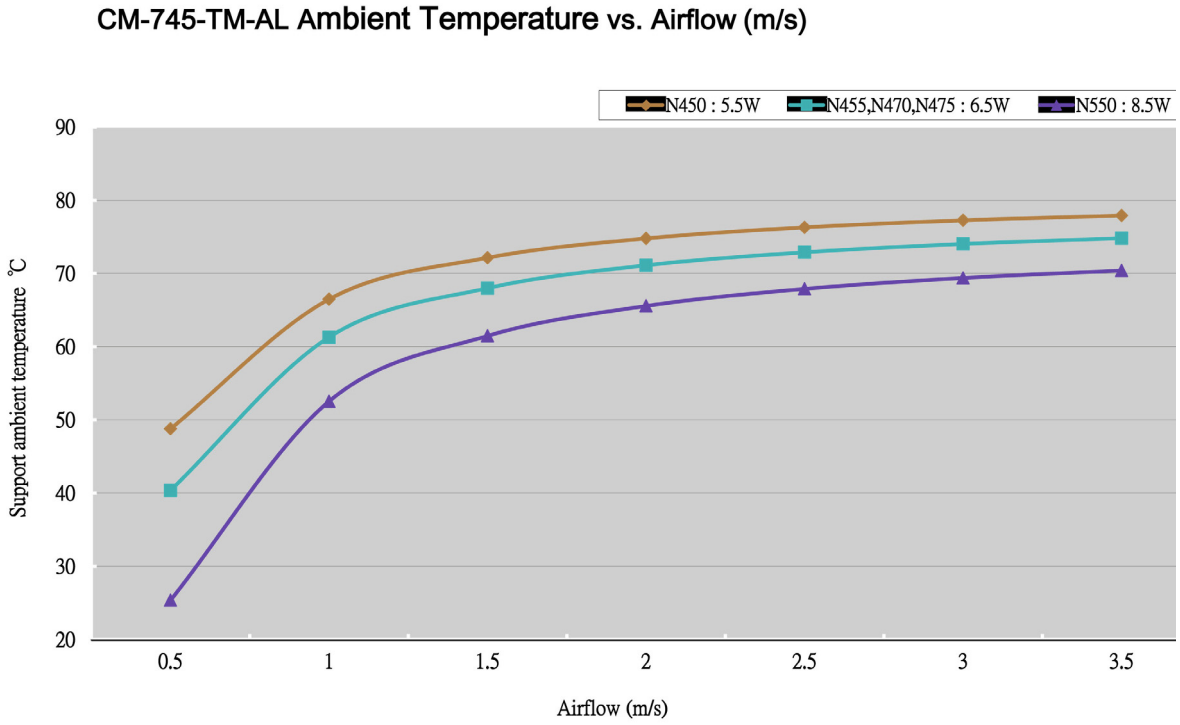


Figure 2-10. Airflow Requirements

NOTE	Airflow directions are from Top to Bottom.

Chapter 3 Hardware

Overview

This chapter discusses the chips and connectors of the module features in the following order:

- CPU
- Graphics
- Memory
- Interrupt Channel Assignments
- Memory Map
- I/O Address Map
- Serial Port Interfaces
- USB Interfaces
- Keyboard and Mouse Interface
- Ethernet Interface
- Video Interface
  - VGA
  - LVDS
- Power Interface
- GPIO Interface
- Utility Interface
  - Power Button
  - Reset Switch
  - Speaker
- SMBus Interface
- System Fan Interface
- Battery Interface
- Ethernet LED Interface
- Miscellaneous
  - SSD (IDE Solid State Drive)
  - Time of Day/RTC
  - Oops! Jumper
  - Remote Access
  - Watchdog Timer

NOTE ADLINK Technology, Inc. only supports the features/options tested and listed in this manual. The main chips used in the CoreModule 745 may provide more features or options than are listed for the CoreModule 745, but some of these features/options are not supported on the module and will not function as specified in the chip documentation.

The pin-out tables only of non-standard headers and connectors are included in this chapter. This chapter does not include pinout tables for standard headers and connectors such as SATA, PC/104, and PC/104-Plus. Refer to references in Chapter 1 for PC/104 and PC/104 Plus pin outs.

CPU

The CoreModule 745 offers two versions of the Intel® Atom™ N400/D500 series CPU—the N455 and D525—operating at 1.67GHz with 6.5W TDP, and 1.83GHz with 13W TDP, respectively. The N400/D500 integrates a low-power and high-performance x86 Processor Core with Memory Controller and 3D Graphics Engine. This single chip is based on 45-nm, Hi-K process technology, ideal for deeply embedded applications.

Graphics

The N400/D500 CPU provides a refresh of the Intel third generation graphics core—a 2D/3D graphics engine that performs pixel shading and vertex shading within a single hardware accelerator, which minimizes access to memory and improves render performance.

Memory

The CoreModule 745 supports one DDR3 SODIMM for up to 2GB of RAM. One 64-bit access channel supports single- or double-sided DIMMs, allowing for up to two device ranks. Enhanced memory technology on the board provides optimized bandwidth and reduced latency, increased efficiency of system memory protocol, and a near continuous data flow to the processor.

Interrupt Channel Assignments

The interrupt channel assignments are shown in Table 3-1.

Table 3-1. Interrupt Channel Assignments

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	X															
PS/2 Keyboard		X														
Secondary Cascade			X													
COM1				O	D											
COM2				D	O											
COM3											O	D				
RTC									X							
IDE															D	
Math Coprocessor														X		
PS/2 Mouse													X			
PCI INTA	Automatically Assigned															
PCI INTB	Automatically Assigned															
PCI INTC	Automatically Assigned															
PCI INTD	Automatically Assigned															
USB	Automatically Assigned															
Video	Automatically Assigned															

Legend: D = Default, O = Optional, X = Fixed

NOTE The IRQs for USB and Video are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

Memory Map

The following table provides the common PC/AT memory allocations. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

Table 3-2. Memory Map

Base Address			Function
00000000h	-	0009FFFFh	Conventional Memory
000A0000h	-	000AFFFFh	Graphics Memory
000B0000h	-	000B7FFFh	Mono Text Memory
000B8000h	-	000BFFFFh	Color Text Memory
000C0000h	-	000CFFFFh	Standard Video BIOS
000D0000h	-	000DFFFFh	DVMT Memory
000E0000h	-	000EFFFFh	PCI Express Base Memory
000F0000h	-	000FFFFFh	System Flash and PCI Resources

I/O Address Map

Table 3-3 shows the I/O address map. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
0000-00F	Primary DMA Controller
0020-0021	Master Interrupt Controller
002E-002F	SIO Configuration Ports
0040-0043	Programmable Interrupt Timer (Clock/Timer)
0060-006F	Keyboard Controller
0070-007F	CMOS RAM, NMI Mask Reg, RT Clock
0080-009F	DMA Page Registers
00A0-00BF	Slave Interrupt Controller
00C0-00DF	Slave DMA Controller #2
00F0-00FF	Math Coprocessor
01F0-01F8	IDE Hard Disk Controller
02F8-02FF	Serial Port 2 (COM2)
03B0-03BB	Video (monochrome)
03C0-03DF	VGA
03E8-03EF	Serial Port 3 (COM3)
03F8-03FF	Serial Port 1 (COM1)
0400-041F	SMBus Configuration Ports
0500-053F	ICH8 GPIO Configuration Ports
0800-087F	ICH8 Power Management Ports
0A79h	ISA PnP Ports
0B00-0B7F	SIO Runtime Registers
0CF8-0CFF	PCI bus Configuration Address and Data

NOTE 0A79h is the ISA PnP port used by the BIOS and an OS that supports this feature to recognize ISA PnP (Plug and Play) cards.

The Intel I/O hub ICH-8 (ICH-6 or later) does not support ISA DMA.

Serial Interfaces

The CoreModule 745 provides three serial ports: two RS-232/485/422 ports (COM1 and COM2) and one RS-232 port (COM3). The SCH3114I-NU SIO contains the circuitry for all three serial ports and delivers the signals through three transceivers. The two RS-232/485/422 ports require two transceivers: one ADM213EARSZ (U11) for RS-232 signals and one LTC1334CG (U12) for RS-485/422 signals. The third serial port requires only one ADM213EARSZ transceiver (U38) for RS-232 signals. The serial ports support the following features:

- Three individual high-speed NS16C550A-compatible UARTs
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Three individual 16-bit FIFOs
- Serial Port Headers
  - J3 - Serial Port 1 (COM1) supports RS-232/RS-485/RS-422 and full modem support
  - J4 - Serial Port 2 (COM2) supports RS-232/RS-485/RS-422 and full modem support
  - J5 - Serial Port 3 (COM3) supports RS-232 and full modem support

NOTE The RS-485/RS-422 mode can be selected for the COM1 and COM2 serial ports in BIOS Setup under the *Advanced>Super IO Configuration* menu. However, the RS-232 mode is the default selection (Standard) for any serial port.

To implement the two-wire RS-485 mode on any serial port, you must tie together the equivalent pins for each port.

For example, on Serial Port 1, tie pin 3 to 5 and pin 4 to 6 at the J3 header as shown in Figure 3-1. As an alternate, tie pin 2 to 3 and pin 7 to 8 at the DB9 serial connector for Serial Port 1 as shown in Figure 3-1. Refer also to the following tables for the specific pin signals on each connector.

NOTE The RS-422 mode uses a four-wire interface and does not require any pins tied together, but you must select RS-485 in BIOS Setup and make sure the termination jumper is removed.

Figure 3-1. RS485 Serial Port Implementation

Table 3-4 defines the pins and corresponding signals for serial ports 1 and 2 headers (J3 and J4), which each consist of 10 pins, 2 rows, odd/even sequence (1, 2), and 0.079" (2mm) pitch.

Table 3-4. Serial Ports 1 & 2 Interface Pin Signal Descriptions (J3 and J4)

Pin #	Signal	DB9 #	Description
1	DCD*	1	Data Carrier Detect – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR as part of the DTR/DSR handshake.
2	DSR*	6	Data Set Ready – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR for overall readiness.
3	RXD Rx Data –	2	Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS line to allow the transmission to complete. Serial Port 1 or 2 – If in RS-485 mode, this pin is Rx Data Negative.
4	RTS* Tx Data +	7	Request To Send – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS for low level flow control. Serial Port 1 or 2 – If in RS-485 mode, this pin is Tx Data Positive.
5	TXD Tx Data –	3	Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS, CTS, DSR, and DTR before data can be transmitted on this line. Serial Port 1 or 2 – If in RS-485 mode, this pin is Tx Data Negative.
6	CTS* Rx Data +	8	Clear To Send – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS for low level flow control. Serial Port 1 or 2 – If in RS-485 mode, this pin is Rx Data Positive.
7	DTR*	4	Data Terminal Ready – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR for overall readiness.
8	RI*	9	Ring Indicator – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	5	Ground
10	Key/NC	NC	Key Pin/Not connected

Note: The shaded table cell denotes power or ground. The * symbol indicates the signal is Active Low.

Table 3-5 describes the pin signals of the serial port 3 header, which consists of 10 pins, two rows, odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

Table 3-5. Serial Port 3 Interface Pin Signal Descriptions (J5)

Pin #	Signal	DB9 #	Description
1	DCD*	1	Data Carrier Detect – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR as part of the DTR/DSR handshake.
2	DSR*	6	Data Set Ready – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR for overall readiness.
3	RXD	2	Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS line to allow the transmission to complete.
4	RTS*	7	Request To Send – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS for low level flow control.
5	TXD	3	Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS, CTS, DSR, and DTR before data can be transmitted on this line.
6	CTS*	8	Clear To Send – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS for low level flow control.
7	DTR*	4	Data Terminal Ready – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR for overall readiness.
8	RI*	9	Ring Indicator – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	5	Ground
10	Key/NC	NC	Key Pin – Not connected

Note: The shaded table cell denotes power or ground. The * symbol indicates the signal is Active Low.

USB Interface

The CoreModule 745 contains two root USB hubs and four functional USB ports. The ICH8-M provides the USB function including the following features:

- Supports USB v.2.0 EHCI and USB v.1.1 UHCI
- Provides over-current detection status
- Provides a fuse on board for over current protection

Table 3-6 describes the pin signals of the USB0 and USB1 header which consists of 10 pins, in two rows, with odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

Table 3-6. USB0 and USB1 Interface Pin Signals (J16)

Pin #	Signal	Description
1	USB-PWR_0	USB0 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
2	USB-PWR_1	USB1 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
3	CONN_USB0_N	USB0 Port Data Negative

Table 3-6. USB0 and USB1 Interface Pin Signals (J16) (Continued)

4	CONN_USB1_N	USB1 Port Data Negative
5	CONN_USB0_P	USB0 Port Data Positive
6	CONN_USB1_P	USB1 Port Data Positive
7	USB_GND0	USB0 Ground
8	USB_GND1	USB1 Ground
9	USB_GND0	USB0 Ground
10	USB_GND1	USB1 Ground

Note: The shaded table cells denote power or ground.

Table 3-7 describes the pin signals of the USB2 and USB3 header, which consists of 10 pins in two rows, with odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

Table 3-7. USB2 and USB3 Interface Pin Signals (J17)

Pin #	Signal	Description
1	USB-PWR_2	USB2 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
2	USB-PWR_3	USB3 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
3	CONN_USB2_N	USB2 Port Data Negative
4	CONN_USB3_N	USB3 Port Data Negative
5	CONN_USB2_P	USB2 Port Data Positive
6	CONN_USB3_P	USB3 Port Data Positive
7	USB_GND2	USB2 Ground
8	USB_GND3	USB3 Ground
9	USB_GND2	USB2 Ground
10	USB_GND3	USB3 Ground

Note: The shaded table cells denote power or ground.

Keyboard/Mouse Interface

The SCH3114I-NU super I/O provides the signals for the PS/2 keyboard and mouse header.

Table 3-8 describes the pin signals of the keyboard/mouse header, which consists of 10 pins in two rows with odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

Table 3-8. Keyboard/Mouse Interface Pin/Signal Definitions (J15)

Pin #	Signal	Description
1	KEY VCC	+5 Volts
2	KEY DATA	Keyboard data
3	KEY CLK	Keyboard clock
4	KEY GND	Keyboard ground
5	KEY GND	Keyboard ground
6	KEY GND	Keyboard ground
7	KEY VCC	+5 Volts
8	CON DAT MOUSE	Mouse data

Table 3-8. Keyboard/Mouse Interface Pin/Signal Definitions (J15) (Continued)

9	CON CLK MOUSE	Mouse clock
10	KEY GND	Keyboard ground

Note: The shaded table cells denote power or ground.

Ethernet Interface

The CoreModule 745 supports one Gigabit Ethernet interface. The Ethernet interface is implemented from the 82574IT Ethernet controller and provides one GLAN interface, which occupies PCI Express port 2. The Ethernet function supports multi-speed operation at 10/100/1000 Mbps and operates in full-duplex at all supported speeds or half duplex at 10/100 Mbps while adhering to the IEEE 802.3x flow control specification.

The Ethernet interface offers the following features:

- Full duplex or half duplex support at 10 Mbps, 100 Mbps, or 1000 Mbps
- In full duplex mode, the Ethernet controller adheres to the IEEE 802.3x Flow Control specification
- In half duplex mode, performance is enhanced by a proprietary collision reduction mechanism
- IEEE 802.3 compatible physical layer to wire transformer
- IEEE 802.3u Auto-Negotiation support
- Fast back-to-back transmission support with minimum interframe spacing (IFS)
- IEEE 802.3x auto-negotiation support for speed and duplex operation
- On-board magnetics (Ethernet isolation transformer)

Table 3-9 describes the pin signals of the Ethernet header which consists of 10 right-angle pins, two rows, odd/even (1,2) pin sequence, and 0.079" (2mm) pitch.

Table 3-9. Ethernet Interface Pin Signal Descriptions (J10)

Pin #	Signal	Description
1	GND	Ground
2	GND	
3	MDI0+	Media Dependent Interface 0 +/-
4	MDI0-	
5	MDI1+	Media Dependent Interface 1 +/-
6	MDI1-	
7	MDI2+	Media Dependent Interface 2 +/-
8	MDI2-	
9	MDI3+	Media Dependent Interface 3 +/-
10	MDI3-	

Note: The shaded table cells denote ground.

NOTE The magnetics (isolation transformer, T1) for the Ethernet header is included on the CoreModule 745.

Video (VGA/LVDS) Interface

The CPU provides the graphics control and video signals to the traditional glass CRT monitors and LCD flat panel displays. The video features are listed below:

VGA features:

- Supports maximum resolutions of 1400x1050 at 60Hz or 2048x1536 at 60Hz
- Provides 2D registers for added color, depth, resolution, and hardware acceleration
- Provides integrated 3 x 8-bit DAC with R, G, and B signals to the monitor

LVDS features:

- Integrated single LVDS channel supporting resolution up to 1280x800 or 1366x768
- Supports 1 x 18 data format
- Supports transmit clock frequency ranges from 25 MHz to 112 MHz

Table 3-10 lists the pin signals of the video (LVDS/VGA) header, which provides 30 pins, 2 rows, odd/even pin sequence (1, 2) with 0.079" (2mm) pitch.

Table 3-10. Video Interface Pin Signals (J19)

Pin #	Signal	Description
1	+12V	+12 volts for flat panel and backlight
2	VCC_LVDS_CONN	JP2 determines LVDS voltage (+3.3V or +5V)
3	GND	Ground
4	GND	Ground
5	LA_CLK_P	LVDS Clock Positive
6	LA_CLK_N	LVDS Clock Negative
7	LA_DAT2_P	LVDS DATA Positive Line 2
8	LA_DAT2_N	LVDS DATA Negative Line 2
9	LA_DAT1_P	LVDS DATA Positive Line 1
10	LA_DAT1_N	LVDS DATA Negative Line 1
11	LA_DAT0_P	LVDS DATA Positive Line 0
12	LA_DAT0_N	LVDS DATA Negative Line 0
13	LBKLT_CTL	Panel Backlight Control
14	LVDD_EN	Enable Panel Power
15	LDDC_CLK	Display Data Channel Clock
16	LDDC_DATA	Display Data Channel Data
17	LBKLT_EN	Enable Backlight Inverter
18	NC	Not Connected
19	CON_DAC_SDA	Digital to Analog Converter DDC (Display Data Channel) - Data
20	CON_DAC_SCL	Digital to Analog Converter DDC (Display Data Channel) - Clock
21	CON_DAC_RED	Digital to Analog Converter – Red Output to the CRT
22	RED_RETURN	VGA Ground for Red Output
23	CON_DAC_GREEN	Digital to Analog Converter – Green Output to the CRT
24	GREEN_RETURN	VGA Ground for Green Output
25	CON_DAC_BLUE	Digital to Analog Converter – Blue Output to the CRT
26	BLUE_RETURN	VGA Ground for Blue Output
27	CRT_HSYNC	Horizontal Sync – Digital Horizontal Sync Output to the CRT

Table 3-10. Video Interface Pin Signals (J19) (Continued)

Pin #	Signal	Description
28	GND VGA	VGA Ground
29	CRT_VSYNC	Vertical Sync – Digital Vertical Sync Output to the CRT
30	VCC_CON_DAC	+5V Power and Ground for Digital to Analog Converter

Note: The shaded table cells denote power or ground.

Power Interface

The CoreModule 745 requires one +5 volt DC power source and provides a shrouded 10-pin, right-angle header with 2 rows, odd/even pin sequence (1, 2), and 0.100" (2.54mm) pitch. If the +5VDC power drops below ~4.65V, a low voltage reset is triggered, resetting the system.

The power input header (J7) supplies the following voltage and ground directly to the module:

- 5.0VDC +/- 5%

Table 3-11. Power Interface Pin Signals (J7)

Pin	Signal	Descriptions
1	GND	Ground
2	+5V	+5 Volts
3	GND	Ground
4	+12V	+12 Volts routed to PC/104, PC/104-Plus, and LVDS interfaces
5	GND	Ground
6	+3.3V_PCI	+3.3 Volts routed to PCI
7	GND	Ground
8	+5V	+5 Volts
9	GND	Ground
10	+5V	+5 Volts

Note: The shaded table cells denote power or ground.

User GPIO Interface

The CoreModule 745 provides GPIO pins for customer use, routing the signals from the ICH8-M chipset to the J18 header. An example test application and source code reside in each BSP directory of the CoreModule 745 Support Software QuickDrive.

For instructions on using the example applications, refer to the GPIO Readme in each BSP directory of the QuickDrive. For more information about the GPIO pin operation, refer to the ICH8-M datasheet at:

http://www.intel.com/assets/pdf/datasheet/313056.pdf

Table 3-12 describes the pin signals of the GPIO interface, which consists of a 10-pin header with 2 rows, odd/even pin sequence (1, 2), and 0.079" (2mm) pitch.

Table 3-12. User GPIO Interface Pin Signal Descriptions (J18)

Pin #	Signal from ICH8-M	Description
1 - GPI1	GPIO1	User defined
2 - GPO1	GPIO17	User defined
3 - GPI2	GPIO6	User defined
4 - GPO2	GPIO18	User defined
5 - GPI3	GPIO7	User defined
6 - GPO3	GPIO20	User defined
7 - GPI4	GPIO8	User defined
8 - GPO4	GPIO27	User defined
9	GND	Ground
10	GND	Ground

Note: The shaded table cells denote ground.

Utility Interface

The Utility interface provides three I/O signals on the module and consists of a 5-pin, 0.100" (2.54mm), single-row header (J23). The ICH8-M drives the Power Button and Speaker signals on the Utility interface. A separate Power Management microprocessor drives the Reset Switch signal. Table 3-13 provides the signal definitions.

- Power Button
- Reset Switch
- Speaker

Power Button

The Utility header provides a signal for an external Power Button through pins 1 and 2. The Power Button allows the user to shut down and power on the system. To shut down the system, press and hold the Power Button for four seconds. Press the Power Button for one second to power on the system.

Reset Switch

Pins 2 and 3 on the Utility header provide the signal for an external reset button which allows the user to re-boot the system.

Speaker

The speaker signal provides sufficient signal strength to drive a 1W 8 Ω “Beep” speaker at an audible level through pins 4 and 5 on the Utility header. The speaker signal is driven from an on-board amplifier and the ICH8-M.

Table 3-13 describes the pin signals of the Utility interface, which uses a 5-pin, single-row header with 0.100" (2.54mm) pitch.

Table 3-13. Utility Interface Pin Signals (J23)

Pin #	Signal	Description
1	/PWR_BTN*	External Power Button (Pins 1-2)
2	GND	Ground
3	/RESET SW*	External Reset Switch signal (Pins 2-3)
4	5V	+5 Volts Power
5	SPKR_CONN	Speaker Output (Pins 4-5)

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

System Management Bus (SMBus)

The ICH8-M chip contains a host SMBus port. The host port allows the CPU access to the SMBus slaves through header, J20. The SMBus slaves include the SODIMM EPROM, Clock Buffer, Clock Generator, and the Gb Ethernet Controller. Table 3-14 lists the device names and corresponding reserved binary addresses on the SMBus. Table 3-15 lists the SMBus pin signals, which are routed through a 5-pin, single-row header with 0.049" (2 mm) pitch.

Table 3-14. SMBus Reserved Addresses

Component	Address Binary
SODIMM EPROM	$1010,000x_b$
Clock Generator	$1101,001x_b$
Clock Buffer	$1101,110x_b$
Gb Ethernet Controller	$1100,001x_b$

Table 3-15. SMBus Pin Signals (J20)

Pin #	Signal	Description
1	SMB_CLK	SMBus Clock
2	GND	Ground
3	SMB_DATA	SMBus Data
4	VSM	+3.3V standby voltage
5	/SMB_ALERT*	SMBus Alert

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

System Fan

Table 3-16 lists the pin signals of the optional System Fan header, which provides 3 pins with 0.079" (2mm) pitch.

Table 3-16. Optional System Fan Pin Signals (J22)

Pin #	Signal	Description
1	VCC	+5.0 volts DC +/- 5%
2	NC	Not Connected
3	GND	Ground

Note: The shaded table cells denote power or ground.

Battery

Table 3-17 lists the pin signals of the External Battery Input header for backup CMOS RAM and RTC (Real Time Clock), which uses 2 pins, single row, with 0.049" (1.25mm) pitch.

Table 3-17. External Battery Input Header (J6)

Pin #	Signal	Description
1	VBAT_EXT	+3.0 volts DC
2	GND	Ground

Note: The shaded table cells denote power or ground.

Ethernet External LED

This header provides signals for an external LED that indicates Ethernet links and activity using a single row of 4 pins with 0.049" (1.25mm) pitch.

Table 3-18. Ethernet External LED Pin Signals (J11)

Pin #	Signal	Description
1	V3.3_CONN	+3 volts – Provides +3 volts to external LED (Pins 1-2 for Green LED)
2	ETH_ACT_LED	Ethernet Activity
3	ETH_LINK100_LED	Fast Ethernet Link with +3 volts power (Pins 3-4 for Bi-Color LED)
4	ETH_LINK1000_LED	Gigabit Ethernet Link

Note: The shaded table cell denotes power.

Miscellaneous

SSD (Solid State Drive)

The CoreModule 745 provides a standard SSD, which is a storage IC soldered directly onto the board. For more information, refer to the SSD data sheet: http://www.greenliant.com/products/?inode=46780.

Real Time Clock (RTC)

The CoreModule 745 contains a Real Time Clock (RTC). The RTC can be backed up with a battery. If the battery is not present, the board BIOS has a battery-less boot feature to complete the boot process.

Oops! Jumper (BIOS Recovery)

The Oops! jumper function is provided in the event the BIOS settings you have selected prevent you from booting the system. By using the Oops! jumper you can prevent the current BIOS settings in flash from being loaded, allowing you to boot using default settings.

Use a jumper to connect the DTR pin (4) to the RI pin (9) on Serial Port 1 (COM 1) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and return to BIOS Setup. You must now load factory defaults by selecting *Load Optimal Defaults* from the *Exit* menu. Then select *Save Changes and Exit* to reboot the system. Now you can modify the default settings to your desired values. Ensure you save the changes before rebooting the system.

To convert a standard DB9 connector to an Oops! jumper, short together the DTR (4) and RI (9) pins on the front of the connector as shown in Figure 3-2 on the Serial Port 1 DB9 connector.

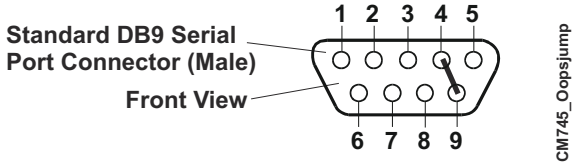


Figure 3-2. Oops! Jumper Serial Port (DB9)

Remote Access

The CoreModule 745 BIOS supports Remote Access (or console redirection). This I/O function can be utilized through an ANSI-compatible serial terminal or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Remote Access Setup

The Remote Access feature is implemented by connecting a standard null modem cable or modified serial cable ("Hot Cable") between one of the serial ports (Serial 1 or 2) and the serial terminal or a PC with communications software. The BIOS Setup Utility controls the Remote Access settings on the CoreModule 745. Refer to "Remote Access Configuration" on page 40 for the settings of the Remote Access feature.

Hot (Serial) Cable

To convert a standard serial cable to a "Hot Cable", certain pins must be shorted together at the Serial port header or on the DB9 connector. Short together the RTS (7) and RI (9) pins on either serial port DB9 connector as shown in Figure 3-3.

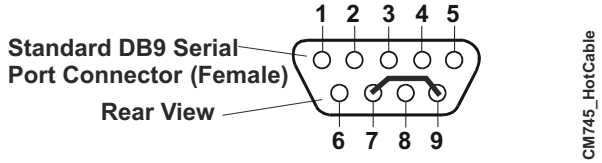


Figure 3-3. Remote Access Jumper

Watchdog Timer

The Watchdog Timer (WDT) restarts the system if a mishap occurs, ensuring proper start-up after the interruption. Possible problems include failure to boot properly, the application software's loss of control, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (Watchdog Timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT using *Boot Settings Configuration* of the Boot menu in BIOS Setup. Set the WDT for a time-out interval in seconds, between 1 and 255, in one-second increments in the Boot Setting Configuration screen. Ensure you allow enough time for the boot process to complete and for the OS to boot. The OS or application must tickle the WDT as soon as it comes up. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some ADLINK Board Support Packages provide an API interface to the WDT. The application must tickle the WDT in the time set when the WDT is initialized or the system will be reset. You can use a BIOS call to tickle the WDT or access the hardware directly.

  The BIOS implements interrupt 15 function 0C3h to manipulate the WDT.

- Watchdog Code examples – ADLINK has provided source code examples on the CoreModule 745 Support Software QuickDrive illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file on the CoreModule 745 Support Software QuickDrive.

Chapter 4 BIOS Setup

Introduction

This section assumes the user is familiar with general BIOS Setup. Refer to the appropriate PC reference manuals for information about the on-board ROM-BIOS software interface. If ADLINK has added to or modified the standard functions, these functions will be described.

Entering BIOS Setup (Local Video Display)

To enter BIOS Setup using a local video display for the CoreModule 745:

1. Turn on the display and the power supply to the CoreModule 745.
2. Start Setup by pressing the [Del] key when the following message appears on the boot screen.

```
Press DEL to run Setup
```

> **NOTE** If the setting for *Quick Boot* is [Enabled], you may not see this prompt appear on screen. If this happens, press the <Del> key early in the boot sequence to enter BIOS Setup.

3. Follow the instructions on the right side of the screen to navigate through the selections and modify any settings.

Entering BIOS Setup (Remote Access)

This section describes how to enable the Remote Access in VGA mode and enter the BIOS setup through a serial terminal or PC.

1. Turn on the power supply to the CoreModule 745 and enter the BIOS Setup Utility in VGA mode.
2. Set the BIOS feature *Remote Access* to [Enabled] under the **Advanced** menu.
3. Accept the default options or make your own selections for the balance of the Remote Access fields and record your settings.
4. Ensure you select the type of remote serial terminal you will be using and record your selection.
5. Select *Save Changes and Exit* and then shut down the CoreModule 745.
6. Connect the remote serial terminal (or the PC with communications software) to the COM port you selected and recorded earlier in the BIOS Setup Utility.
7. Turn on the remote serial terminal or PC and set it to the settings you selected in the BIOS Setup Utility.

   The default settings for the CoreModule 745 are:

   - COM1
   - 115200
   - 8 bits
   - no parity
   - 1 stop bit
   - no flow control (None)
   - [Always] for *Redirection After BIOS POST*
8. Restore power to the CoreModule 745.

9. Press the F4 key to enter Setup (early in the boot sequence if *Quick Boot* is set to [Enabled].)

   If *Quick Boot* is set to [Enabled], you may never see the screen prompt.

10. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen.

> **NOTE** The serial console port is not hardware protected. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

PCI-ISA Bridge Mapping

The CoreModule 745 supports ISA bus based modules with an on-board PCI-ISA bridge. The PCI-ISA bridge optionally maps the IRQs to ISA based modules.

The CoreModule 745 system BIOS, maps the above resources based on information provided in the BIOS Setup screens. By default, IRQs to be mapped to ISA modules must be explicitly specified by the user in the BIOS Setup screens.

The IRQs are mapped with the "PCIPnP/IRQx" fields in BIOS setup (where x specifies the IRQ number.) The IRQs 3, 4, 5, 7, 9, 10, 11, 14, and 15 can be mapped to ISA based modules by changing the default setting for these IRQs from "Available" to "Reserved".

OEM Logo Utility

The CoreModule 745 BIOS supports a graphical logo utility, which can be customized by the user and displayed when enabled through the BIOS Setup Utility. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image on screen and remain there while the OS boots, depending on the options selected in BIOS Setup.

Logo Image Requirements

The user's image may be customized with any image editing tool, and the system will automatically convert the image into an acceptable format to the tools (files and utilities) provided by ADLINK. The CoreModule 745 OEM Logo utility supports the following image formats:

- Bitmap image
  - 16-Color, 640x480 pixels
  - 256-Color, 640x480 pixels
- JPG image
  - 16-Color, 640x480 pixels
- PCX image
  - 256-Color, 640x480 pixels
- A file size no larger than the sample image

BIOS Setup Menus

This section provides illustrations of the six main setup screens in the CoreModule 745 BIOS Setup Utility. Below each illustration is a bullet list of the screen's submenus and setting selections. The setting selections are presented in brackets after each submenu or menu item and the optimal default settings are presented in bold. For more detailed definitions of the BIOS settings, refer to the AMIBIOS8 manual: http://www.ami.com/support/doc/MAN-EZP-80.pdf.

Table 4-1. BIOS Setup Menus

BIOS Setup Utility Menu	Item/Topic
Main	Date and Time
Advanced	CPU, IDE, USB, Chipset, Video Function, Super IO, PCI PnP, Remote Access, Watchdog Timer
Power	Power Management (APM) and Resume Power conditions
Boot	Boot up Settings, Boot Order, Removable Drives
Security	Setting or changing Passwords, Boot Sector Virus Protection
Exit	Exiting with or without changing settings, Loading Optimal or Failsafe conditions

BIOS Main Setup Screen

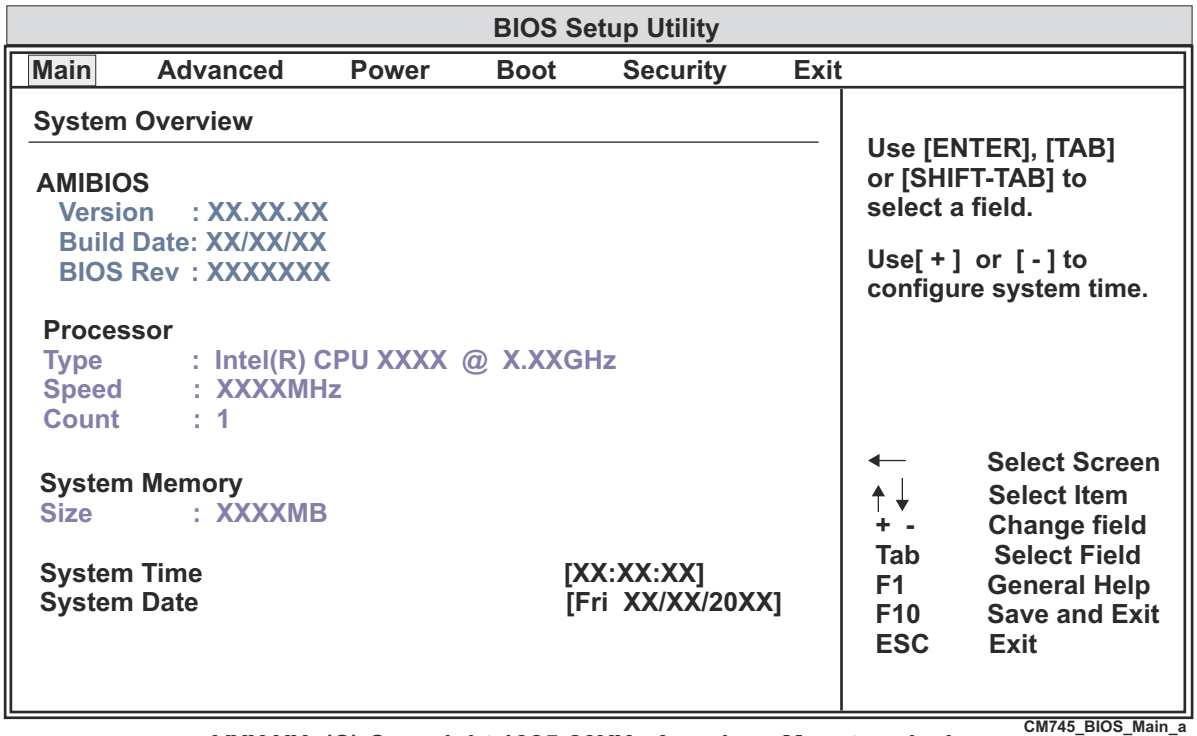


Figure 4-1. BIOS Main Setup Screen

- **Date & Time**
  - System Time (hh:mm:ss) – This is a 24-hour clock setting in hours, minutes, and seconds.
  - System Date (day of week, mm:dd:yyyy) – This field requires the alpha-numeric entry of the day of week, day of the month, calendar month, and all 4 digits of the year, indicating the century plus year (*Fri XX/XX/20XX*).

BIOS Advanced Setup Screen

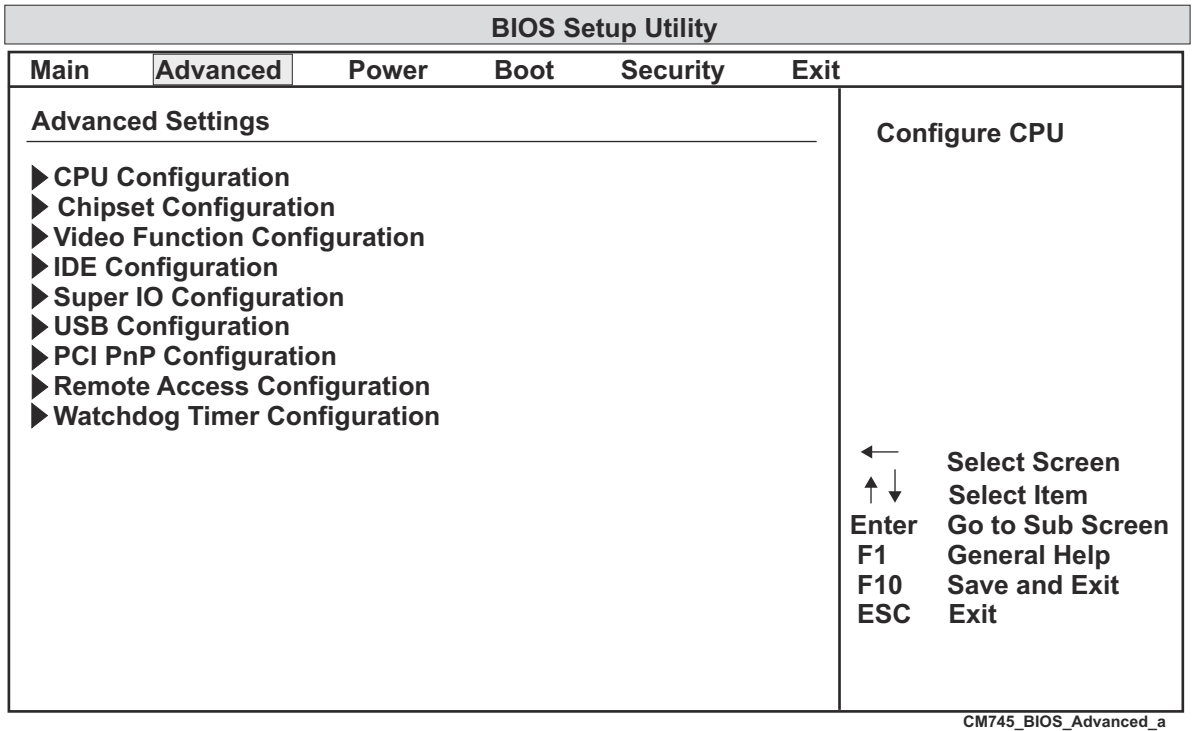


Figure 4-2. BIOS Advanced Setup Screen

- **CPU Configuration**
  - Manufacture: Intel
  - Brand String: Intel® Atom processor X.XXGHz
  - Frequency: X.XXGHz
  - FSB Speed: XXXMHz
  - Cache L1: XXkB
  - Cache L2: XXXXkB
  - Ratio Actual Value: XX
  - Max CPUID Limit [**Disabled**; Enabled]
  - Execute - Disable Bit Capability [Disabled; **Enabled**]
  - Hyper Threading Technology [Disabled; **Enabled**]
  - Intel (R) Speed Step (TM) Technology [Disabled; **Enabled**] - (Available only on the N455 model)
  - Intel (R) C-State Technology [Disabled; **Enabled**] - (Available only on the N455 model)
  - Enhanced C-States [Disabled; **Enabled**] - (Available only on the N455 model)
- **Chipset Configuration**
  - North Bridge Chipset Configuration
    - PCIMMIO Allocation: XGB to XXXXMB
    - DRAM Frequency [**Auto**; Max MHz]
    - Configure DRAM Timing by SPD [**Enabled**; Disabled]

- South Bridge Chipset Configuration
  - SMBUS Controller [**Enabled**; Disabled]
  - Onboard Ethernet Controller [**Enabled**; Disabled]

- **Video Function Configuration**
  - Initiate Graphic Adapter [**PCI/IGD**; IGD]
  - Internal Graphics Mode Select [**Enabled, 8MB**]
  - DVMT Mode Select [**DVMT Mode**; Fixed Mode]
    - DVMT/Fixed Memory [128MB; **256MB**; Maximum DVMT]
  - Boot Display Device [CRT; LVDS; **CRT + LVDS**]
  - Flat Panel Type [640x480; **800x600**; 1024x768; 1280x800; 1366x768]
  - Spread Spectrum Clock [**Disabled**; Enabled]
- **IDE Configuration**
  - ATA/IDE Configuration [Disabled; **Compatible**; Enhanced]
  - Legacy IDE Channels [SATA Only; **SATA Pri, PATA Sec**]
  - Primary IDE Master [Not Detected]
  - Primary IDE Slave [Not Detected]
  - Secondary IDE Master [XGB NANDrive]
    - Type [Not Installed; **Auto**; CD/DVD; ARMD]
    - LBA/Large Mode [Disabled; **Auto**]
    - Block (Multi-Sector Transfer) [Disabled; **Auto**]
    - PIO Mode [**Auto**; 0; 1; 2; 3; 4]
    - DMA Mode [**Auto**; SWDMA0; SWDMA1; SWDMA2; MWDMA0; MWDMA1; MWDMA2; UDMA0; UDMA1; UDMA2; UDMA3; UDMA4]
    - S.M.A.R.T. [**Auto**; Disabled; Enabled]
    - 32Bit Data Transfer [Disabled; **Enabled**]
  - Secondary IDE Slave [Not Detected]
  - Third IDE Master [Not Detected]
  - Third IDE Slave [Not Detected]
  - AHCI Settings
    - AHCI Port0 [Not Detected]
    - AHCI Port2 [Not Detected]
- **Super IO Configuration**
  - Serial Port1 Address [Disabled; **3F8**; 3E8; 2E8]
    - Serial Port1 IRQ [3; **4**; 10; 11]
    - RS-485 Control for SP1 [**Disabled**; Enabled]
  - Serial Port2 Address [Disabled; **2F8**; 3E8; 2E8]
    - Serial Port2 IRQ [**3**; 4; 10; 11]
    - RS-485 Control for SP2 [**Disabled**; Enabled]

- Serial Port3 Address [Disabled; 3F8; 2F8; **3E8**; 2E8; 2F0; 2E0]
  - Serial Port3 IRQ [3; 4; 10; **11**]

- **USB Configuration**
  - Module Version - X.XX.X - XX.X
  - USB Devices Enabled: None
  - USB Functions [Disabled; USB Port 0; USB Ports 0-1; USB Ports 0-2; **USB Ports 0-3**]
  - USB 2.0 Controller [**Enabled**]
  - Legacy USB Support [Disabled; **Enabled**; Auto]
  - USB 2.0 Controller Mode [FullSpeed; **HiSpeed**]
  - BIOS EHCI Hand-Off [Disabled; **Enabled**]
- **PCI/PnP Configuration**
  - Clear NVRAM [**No**; Yes]
  - PCI Latency Timer [32; **64**; 96; 128; 160; 192; 224; 248]
  - Palette Snooping [**Disabled**; Enabled]
  - IRQ3 [**Available**; Reserved]
  - IRQ4 [**Available**; Reserved]
  - IRQ5 [**Available**; Reserved]
  - IRQ7 [**Available**; Reserved]
  - IRQ9 [**Available**; Reserved]
  - IRQ10 [**Available**; Reserved]
  - IRQ11 [**Available**; Reserved]
  - IRQ14 [**Available**; Reserved]
  - IRQ15 [**Available**; Reserved]
  - Reserved Memory Size [**Disabled**; 16k; 32k; 64k]
- **Remote Access Configuration**
  - Remote Access [**Hot Cable**; Enabled]
  - Serial Port Number [**COM1**; COM2]
    - Base Address, IRQ [**3F8h, 4**]
  - Serial Port mode [**115200 8, n, 1**; 57600 8, n, 1; 38400 8, n, 1; 19200 8, n, 1; 09600 8, n, 1]
  - Flow Control [**None**; Hardware; Software]
  - Redirection After BIOS POST [Disabled; Boot Loader; **Always**]
  - Terminal Type [**ANSI**; VT100; VT-UTF8]
  - VT-VTF8 Combo Key Support [Disabled; **Enabled**]
  - Sredir Memory Display Delay [**No Delay**; Delay 1 Sec; Delay 2 Sec; Delay 4 Sec]
- **Watchdog Timer Configuration**
  - Watchdog Timer [**Disabled**; Enabled]
- **GPIO Configuration**
  - GPOs Configuration

- Set GPO1 State [**High**; Low]
- Set GPO2 State [**High**; Low]
- Set GPO3 State [**High**; Low]
- Set GPO4 State [**High**; Low]

♦ GPIs state monitoring

- Current GPI1 State High
- Current GPI2 State High
- Current GPI3 State High
- Current GPI4 State High

BIOS Power Management Setup Screen

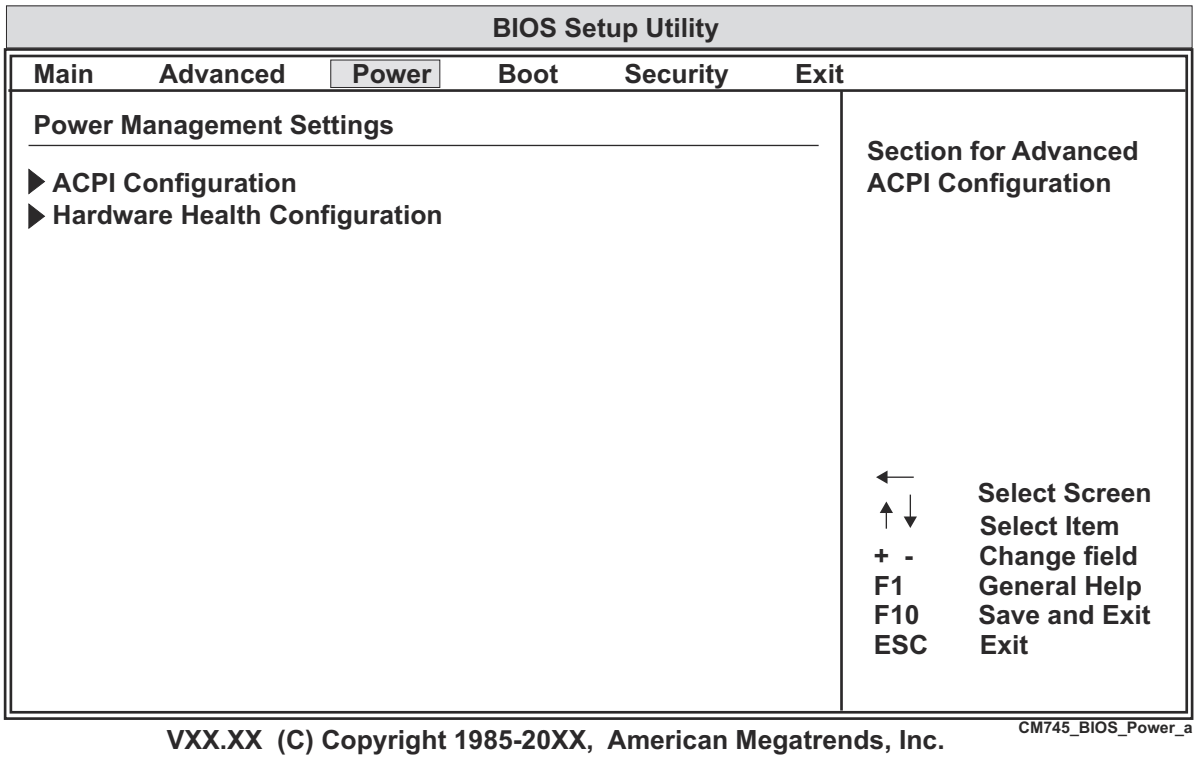


Figure 4-3. Power Management Setup Screen

- **Power Management Settings**

♦ ACPI Configuration

- ACPI Version Features [ACPI v1.0; **ACPI v2.0**; ACPI v3.0]
- ACPI APIC Support [Disabled; **Enabled**]
- APIC ACPI SCI IRQ [**Disabled**; Enabled]
- High Performance Event Timer [Disabled; **Enabled**]
- HPET Memory Address [**FED00000h**; FED01000h; FED02000h; FED03000h]

♦ Hardware Health Configuration

- CPU Temperature XX°C / XXX°F

BIOS Boot Setup Screen

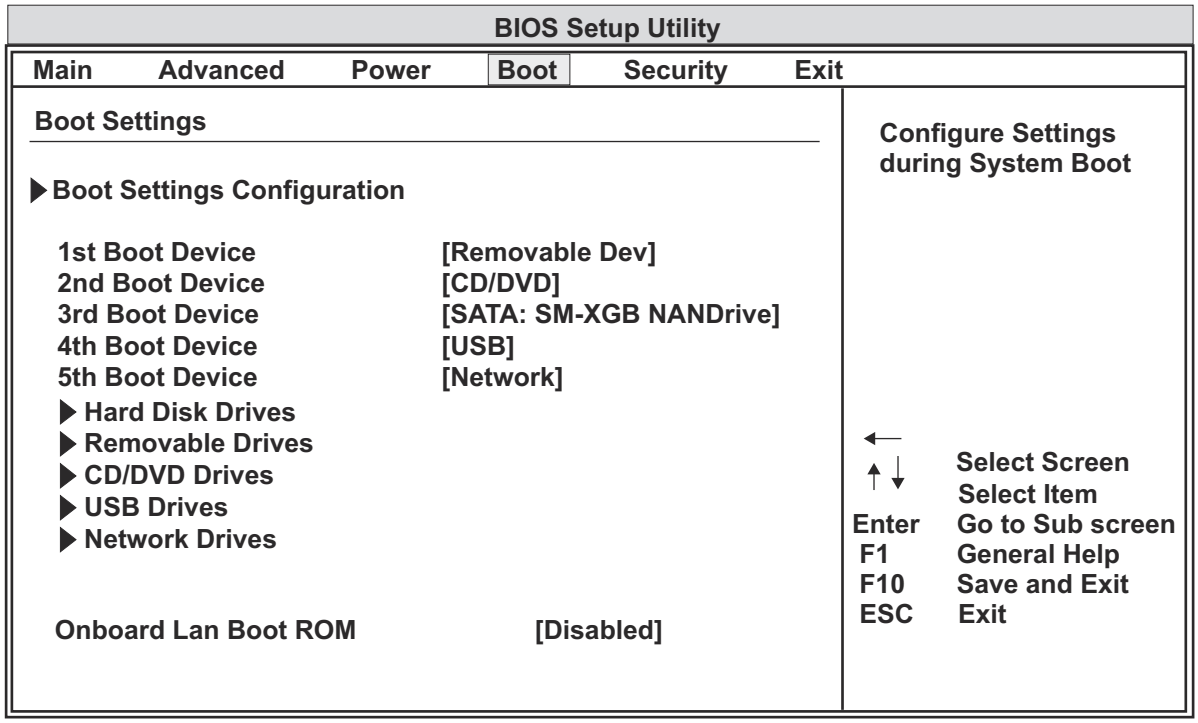


Figure 4-4. BIOS Boot Setup Screen

- **Boot Settings**
  - Boot Settings Configuration
    - Quick Boot [Disabled; **Enabled**]
    - Quiet Boot [**Disabled**; Enabled]
    - AddOn ROM Display Mode [**Force BIOS**; Keep Current]
    - Bootup Num-Lock [Off; **On**]
    - PS/2 Mouse Support [Disabled; Enabled; **Auto**]
    - Wait for 'F1' If Error [Disabled; **Enabled**]
    - Hit 'DEL' Message Display [Disabled; **Enabled**]
    - Interrupt 19 Capture [**Disabled**; Enabled]
  - 1st Boot Device [**Removable Dev**; CD/DVD; HDD: SM-XGB NANDrive; USB; Network; Disabled]
  - 2nd Boot Device [Removable Dev; **CD/DVD**; HDD: SM-XGB NANDrive; USB; Network; Disabled]
  - 3rd Boot Device [Removable Dev; CD/DVD; **HDD: SM-XGB NANDrive**; USB; Network; Disabled]
  - 4th Boot Device [Removable Dev; CD/DVD; HDD: SM-XGB NANDrive; **USB**; Network; Disabled]
  - 5th Boot Device [Removable Dev; CD/DVD; HDD: SM-XGB NANDrive; USB; **Network**; Disabled]
  - Hard Disk Drives
    - 1st Drive [**SATA: SM-XGB NANDri**; Disabled]

- Removable Drives
  - 1st Drive [Not Installed]
- CD/DVD Drives
  - 1st Drive [Not Installed]
- USB Drives
  - 1st Drive [Not Installed]
- Network drives
  - 1st Drive [Not Installed]
- Onboard Lan Boot ROM [**Disabled**; Enabled]

BIOS Security Setup Screen

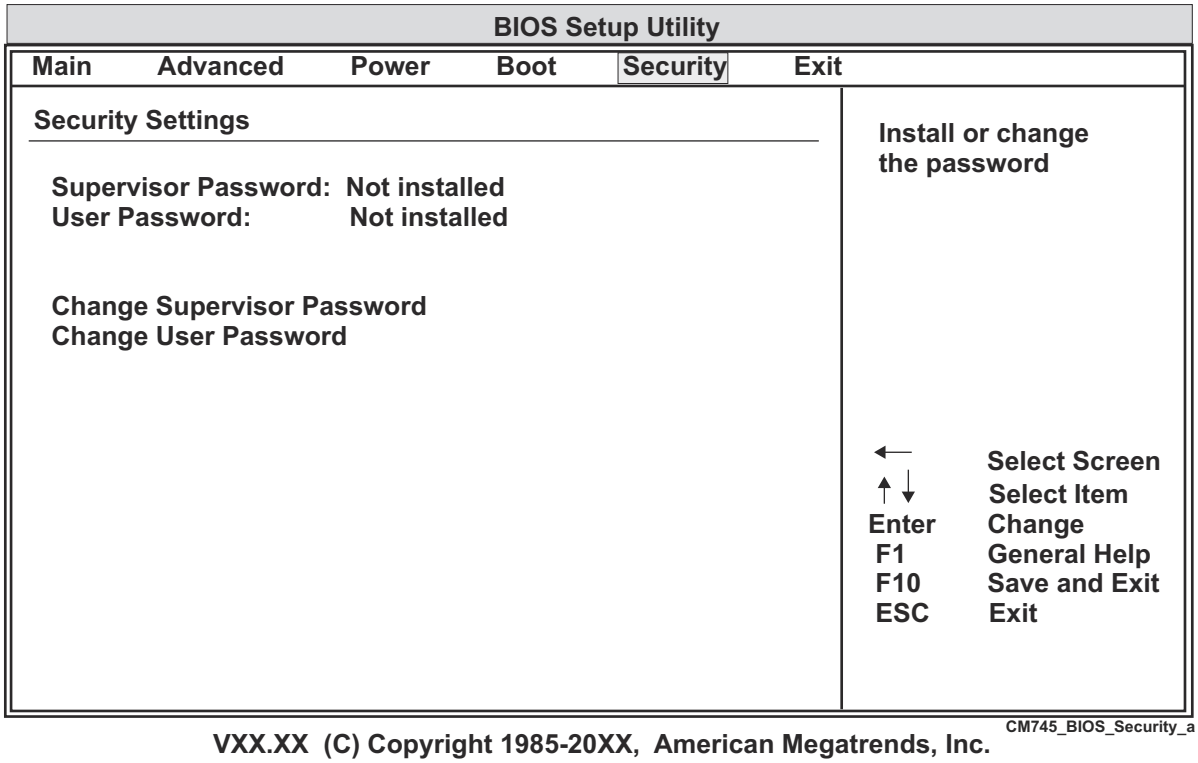


Figure 4-5. BIOS Security Setup Screen

- **Security Settings**
  - Supervisor Password [Not Installed]
  - User Password [Not Installed]
  - Change Supervisor Password
  - Change User Password

BIOS Exit Setup Screen

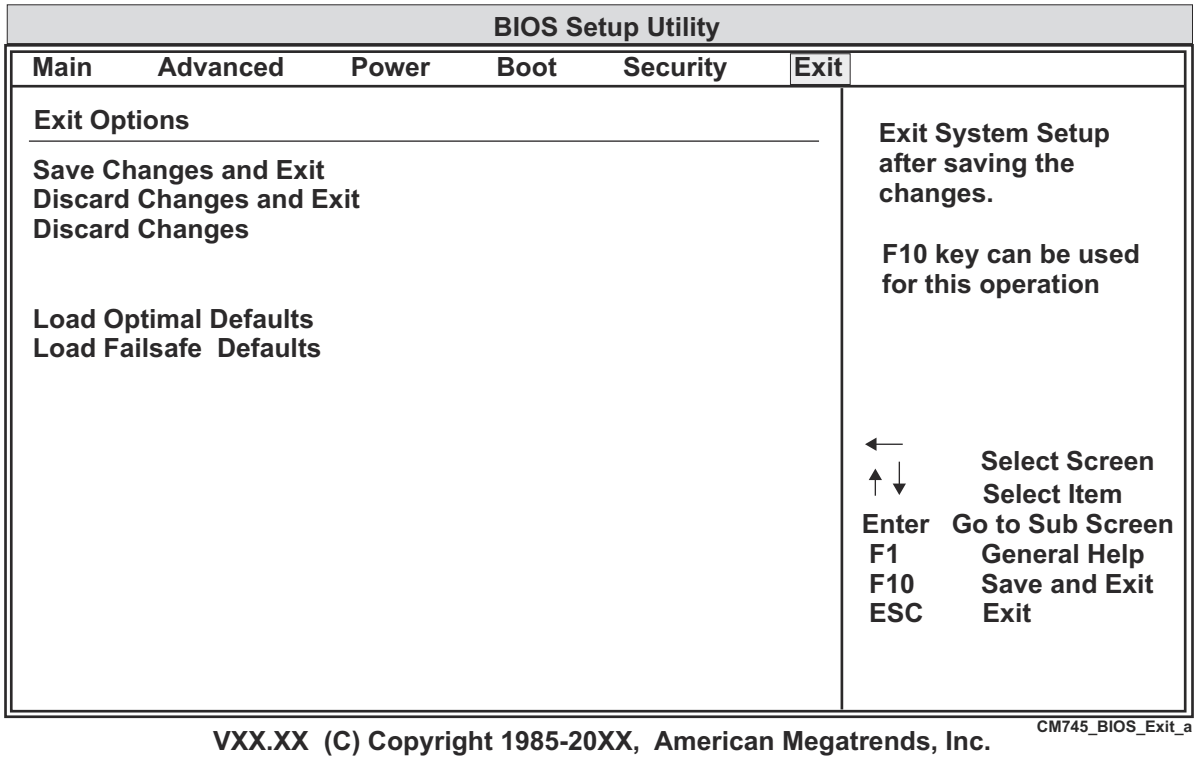


Figure 4-6. BIOS Exit Setup Screen

- **Exit Options**
  - Save Changes and Exit (F10 key can be used for this operation.)
  - Discard Changes and Exit (ESC key can be used for this operation.)
  - Discard Changes (F7 key can be used for this operation.)
  - Load Optimal Defaults (F9 key can be used for this operation.)
  - Load Failsafe Defaults (F8 key can be used for this operation.)

Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed below in Table A-1. Requests for support through the Ask an Expert are given the highest priority, and usually will be addressed within one working day.

- ADLINK's Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web page at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

  ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called "My ADLINK" unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to My Stuff area where you can check status, update your request, and access other features.

- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1. Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	Contact us should you require any service or assistance. **ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

Table A-1. Technical Support Contact Information (Continued)

	ADLINK Technology Beijing Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085) Rm. 801, Power Creative E, No. 1, Shang Di East Rd., Beijing, 100085 China Tel: +86-10-5885-8666 Fax: +86-10-5885-8626 Email: market@adlinktech.com **ADLINK Technology Shenzhen** Address: 深圳市南山区科技园南区高新南七道 数字技术园 A1 栋 2 楼 C 区 (518057) 2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7, High-Tech Industrial Park S., Shenzhen, 518054 China Tel: +86-755-2643-4858 Fax: +86-755-2664-6353 Email: market@adlinktech.com **LiPPERT ADLINK Technology GmbH** Address: Hans-Thoma-Strasse 11, D-68163, Mannheim, Germany Tel: +49-621-43214-0 Fax: +49-621 43214-30 Email: emea@adlinktech.com **ADLINK Technology, Inc. (French Liaison Office)** Address: 15 rue Emile Baudot, 91300 Massy CEDEX, France Tel: +33 (0) 1 60 12 35 66 Fax: +33 (0) 1 60 12 35 66 Email: france@adlinktech.com **ADLINK Technology Japan Corporation** Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4 神田 374 ビル 4F KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho, Chiyoda-ku, Tokyo 101-0045, Japan Tel: +81-3-4455-3722 Fax: +81-3-5209-6013 Email: japan@adlinktech.com **ADLINK Technology, Inc. (Korean Liaison Office)** Address: 서울시 서초구 서초동 1675-12 모인터빌딩 8 층 8F Mointer B/D,1675-12, Seocho-Dong, Seocho-Gu, Seoul 137-070, Korea Tel: +82-2-2057-0565 Fax: +82-2-2057-0563 Email: korea@adlinktech.com **ADLINK Technology Singapore Pte. Ltd.** Address: 84 Genting Lane #07-02A, Cityneon Design Centre, Singapore 349584 Tel: +65-6844-2261 Fax: +65-6844-2263 Email: singapore@adlinktech.com **ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)** Address: 1st Floor, #50-56 (Between 16th/17th Cross) Margosa Plaza, Margosa Main Road, Malleswaram, Bangalore-560055, India Tel: +91-80-65605817, +91-80-42246107 Fax: +91-80-23464606 Email: india@adlinktech.com

Table A-1. Technical Support Contact Information (Continued)

	ADLINK Technology, Inc. (Israeli Liaison Office) Address: 6 Hasadna St., Kfar Saba 44424, Israel Tel: +972-9-7446541 Fax: +972-9-7446542 Email: israel@adlinktech.com

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