

# **486-GVT-2**

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## **MAIN BOARD User's Guide**

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## HANDLING PRECAUTIONS



**Static electricity may cause damage to the integrated circuits on the mainboard. Before handling any mainboard outside of its protective packaging, ensure that there is no static electric charge in your body.**

Observe any or all of these basic precautions when handling the mainboard or other computer components:

- Wear a static wrist strap which fits around your wrist and is connected to a natural earth ground.
- Touch a grounded or anti-static surface or a metal fixture such as a water pipe.
- Avoid contact with the components on add-on cards, boards and modules and with the “golden finger” connectors plugged into the expansion slot. It is best to handle system components by their mounting bracket.

Above methods either prevent static build-up or cause it to be discharged properly.

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## ABOUT THIS MANUAL

This manual is designed to guide you and facilitate your use of the 486-GVT-2 mainboard. It is divided into chapters and appendix. The chapters contain the main body of information normally referred to by users. The appendix provide more detailed technical information for reference.

- Chapter 1** gives an overview and introduces the basic parts and features of the mainboard.
- Chapter 2** gives information on the jumper and connector settings on the mainboard.
- Chapter 3** provides information on the mainboard's memory subsystem consisting of SIMMs and Cache memory and describes how you can upgrade memory.
- Chapter 4** briefly explains the mainboard's Award BIOS system Setup in general and tells you how to run it and change the system configuration settings.
- Appendix A** provides relevant technical information.

**NOTE : The material in this manual is for information only and is subject to change without notice. We reserve the right to make changes in the product design without reservation and without notification to its users. We shall not be liable for technical or editorial omissions made herein; nor for incidental or consequential damages resulting from the furnishing, performance, or use of this material.**

## Overview

Based on an ISA/VL-bus, the 486-GVT-2 mainboard empowers any high-end system to exploit a wide-range of hardware and software capabilities and applications. The board's special feature is the VIA GMC chipset, a highly integrated single chipset that supports write-back and SMM (System Management Mode) CPUs, multi-master operations and provides built-in power management features ideal for Green PCs. This chapter gives you a brief overview of this mainboard, providing basic information on its major parts and components.

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## Specifications

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The 486-GVT-2 mainboard comes with the following features:

- Supports Intel 80486SX/DX/DX2/486 SL-Enhanced/Cyrix Cx486S/DX/Intel Pentium Overdrive™ microprocessor in PQFP and PGA packages.
- VIA GMC VT82C486A PC/AT chipset includes built-in 8042 keyboard controller.
- Award BIOS.
- Supports 64/128/256K direct-mapped write-back/write-through cache memory.
- 30- and 72-pin SIMM sockets support 1 up to 96MB DRAM for 486 system, and provides page mode DRAM operation.
- Supports system and video BIOS cacheable and shadow.
- Supports decoupled DRAM refresh.
- Optional built-in ZIF socket that accepts Intel's OverDrive™ processors.
- Six 16-bit and one 8-bit ISA expansion slots.
- Supports two VESA bus slots for Local bus master or slave.

- Dallas DS1287/DS12885Q/VIA VT82885V real time clock/calendar.
- Provides built-in power management features ideal for Green PCs.

# Mainboard Layout

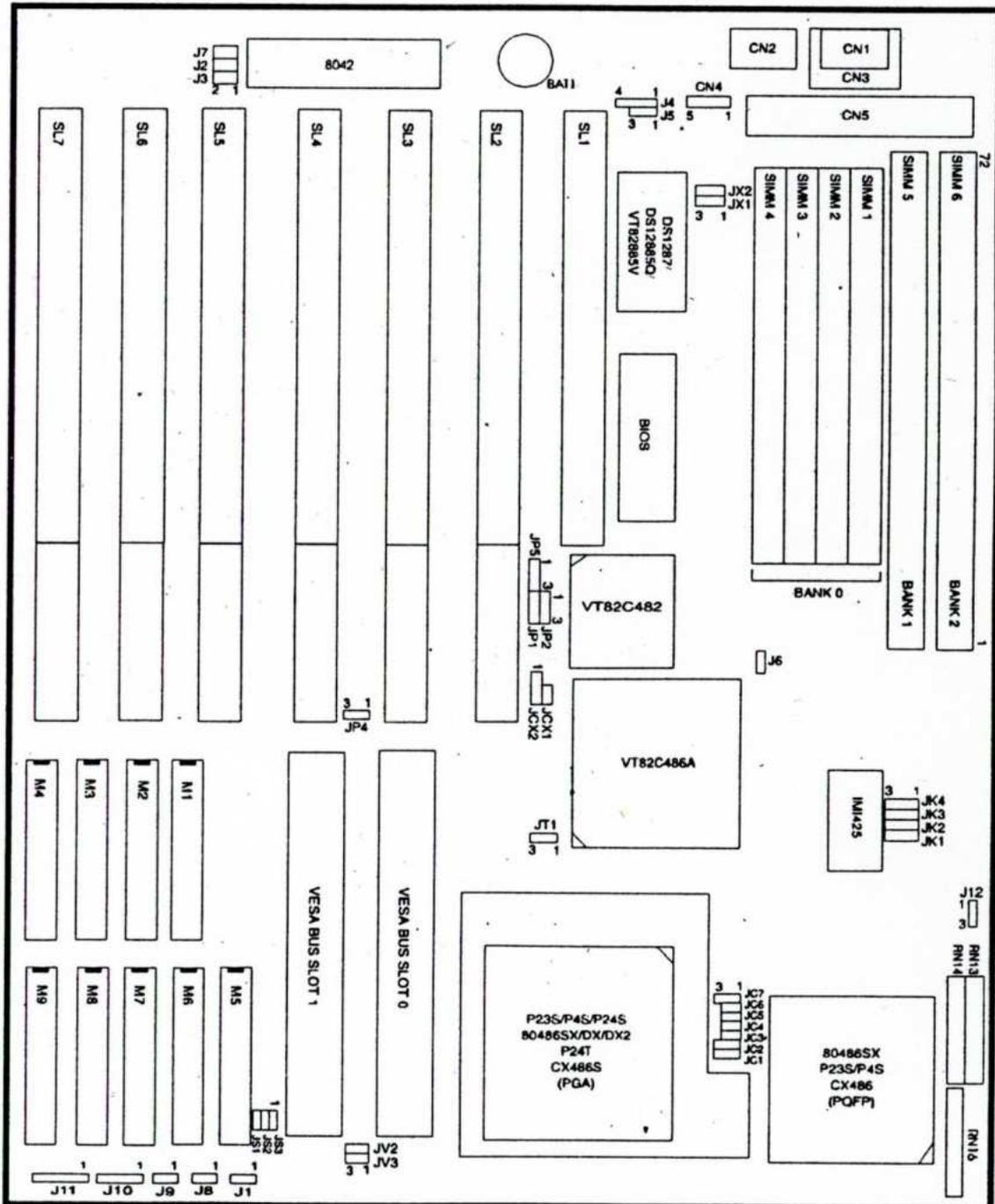


Figure 1-1. Mainboard Layout

# System Block Diagram

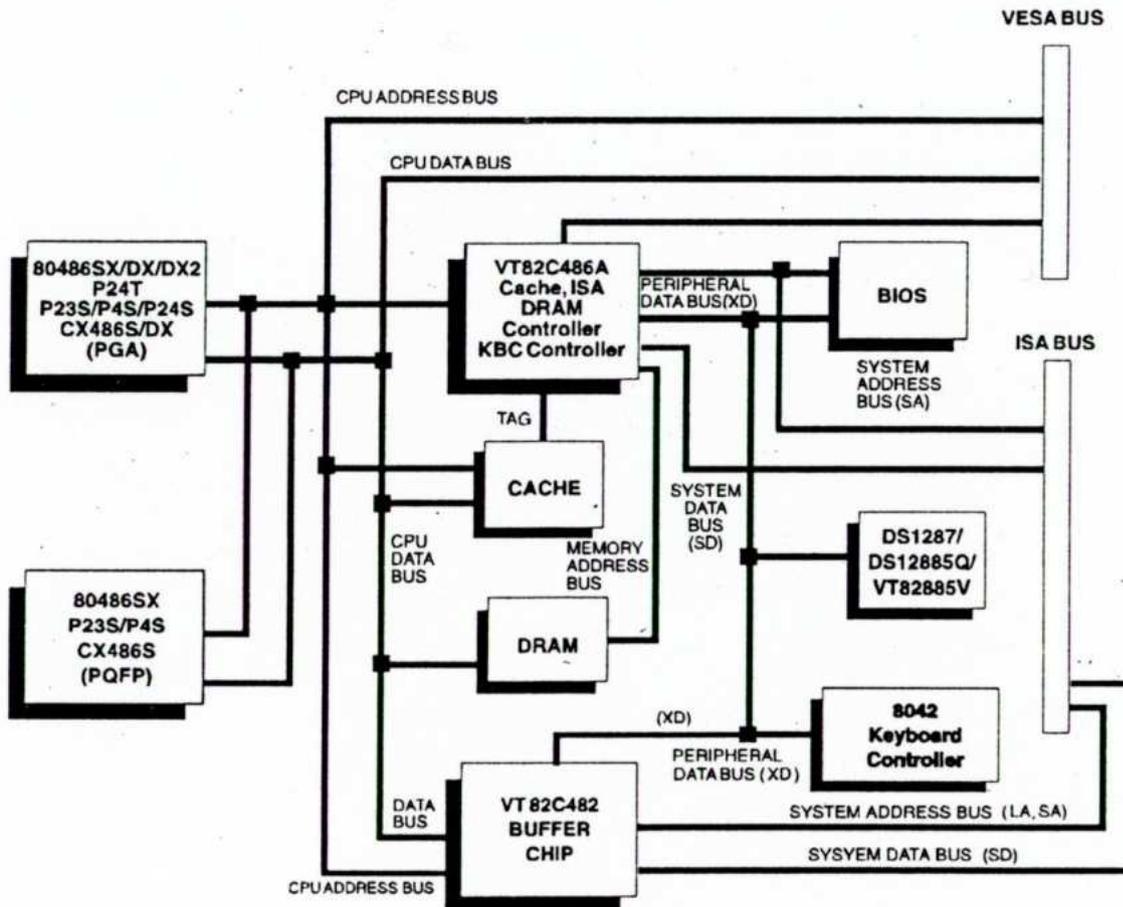


Figure 1-2. System Block Diagram

## Mainboard Settings

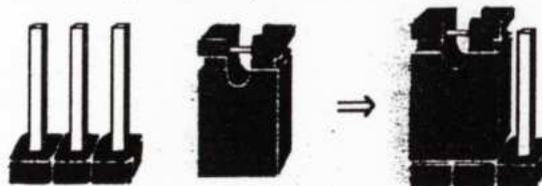
The 486-GVT-2 has several user-adjustable jumpers and connectors on the board that allow you to configure your system to suit your every need. This chapter contains information on the various jumper and connector settings you can make on your mainboard.

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### Jumpers

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Jumpers are used to select the operation modes for your system. Some jumpers on the board have three metal pins with each pin representing a different function. To “set” a jumper, a black cap containing metal contacts is placed over the jumper pin/s according to the required configuration. A jumper is said to be “shorted” when the black cap has been placed on one or two of its pins, as shown in the figure below:



*Table 2-1. Jumper with Pins Shorted*

### CPU Selector Jumpers

To allow your system to be used with a variety of CPU's, 486-GVT-2 provides jumpers that can be set according to the CPU you want installed. Follow the diagrams found in the lower-middle area of the board to determine the proper arrangement for the CPU you are using.

The next three tables summarizes the settings of the CPU Selector jumpers:

JUMPER	486SX/P23S* (PGA)	P24S*/P4S*/ 486DX/DX2 (PGA)	P24T* (PGA)	Cx486S (M6) (PGA)	Cx486DX (M7) Cx486S+ Cx487S (M6+C6) (PGA)
JC1	2-3 shorted	1-2 shorted	1-2 shorted	2-3 shorted	1-2 shorted
JC2	2-3 shorted	1-2 shorted	1-2 shorted	2-3 shorted	1-2 shorted
JC3	open	shorted	open	shorted	shorted
JC4	open	open	shorted	open	open
JC5	shorted	shorted	open	open	open
JC7	1-2 shorted	1-2 shorted	2-3 shorted	1-2 shorted	1-2 shorted

\* P23S, P24S, and P4S are the SL-enhanced CPUs while P24T is the Pentium Overdrive Processor.

JUMPER (RP 0Ω 10p5R)	P23S/P4S/P24S (PGA)	486DX/DX2/SX (PGA)	Cx486S Cx486S+Cx487S Cx486DX (M6, M6+C6, M7) (PGA)	P23S/P4S/Cx486S (PQFP)
RN13	inserted	empty	empty	empty
RN14	empty	empty	empty	inserted
RN16	empty	empty	inserted	empty

JUMPER	PIN DEFINITION	
JC6	80486SX/P23S/P4S/Cx486S PQFP Select	Short Open Disable Enable
JCX1	Short Open	Cyrix Cx486S/DX Intel S-series CPU, others (default)
JCX2	1-2 2-3	Intel S-series CPU, others (default) Cyrix Cx486S/DX
JX2, JP2	1-2 * 2-3	IRQ15 (Regular CPUs -- default) -- SMI (Cyrix or Intel S-series CPUs)

\* IRQ15 is no longer available for the other devices when SMI is selected.

Table 2-1. Jumper Settings for CPU Selector

JUMPER	PIN DEFINITION	
J2	Display Type Select Open Short	Mono/EGA/VGA (default) Color
J5	External, Internal Battery Select 1-2 2-3	External battery Internal battery (default)
J6	Short Open	Adaptec ISA Master 1542B/C SCSI card only (Transfer rate $\geq$ 5.7MB/s) Default (Transfer rate $<$ 5.7MB/s)
J7	Password Clear (Award/AMI BIOS Select) Short Open	Clear password (default)
J12	Cyrix CPU 2 X Clock Mode Select 1-2 2-3	2 X 1 X (default)
JP1, JP5	JP1 1-2	JP5 1-2 (factory default)
JP4	Local IDE 1-2 2-3	Default For VESA Local VGA Card installed at VESA slot 0 only
JT1	P24T Write-back/Write-through Select 1-2 2-3	Write-back Write-through
JX1	Regular CPU Clock Select 1-2 2-3	1 X (default) 2 X

*Table 2-2. Jumper Definitions*



**NOTE :** Users are not encouraged to change the jumper settings not listed in this manual as they are considered factory defaults which may adversely affect system performance.

**CPU Clock Jumper JK1-JK4 (VT8225N)**

CLK 2	JK1	JK2	JK3	JK4
100 MHz	1-2	2-3	1-2	2-3
80 MHz	1-2	1-2	2-3	2-3
66.6 MHz	2-3	2-3	1-2	2-3
50 MHz	2-3	1-2	2-3	2-3
40 MHz	1-2	1-2	2-3	1-2
33.3 MHz	2-3	2-3	1-2	1-2
25 MHz	2-3	1-2	2-3	1-2

*Table 2-3. CPU Clock Jumper Selection JK1-JK4 (VT8225N)*

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**Connectors**

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The connectors allow the mainboard to connect electronically with other parts of the system. Some connectors have two pins, others have four or five pins. Some malfunction problems encountered with your system may be caused by loose or improper connections. Ensure that all connections are in place and firmly attached.

CONNECTOR	PIN OUTS	SIGNAL NAME
J1 Turbo Switch	1 2	Turbo Signal Ground
J3 * Green Power Supply Connector	1 2	Enable/Disable power supply outlet Ground
J4 External Battery Connector	1 2, 3 4	Anode+ NC Cathode -
J8 Turbo LED	1 2	VCC LED
J9 Hardware Reset	1 2	Ground Reset signal
J10 Speaker Connector	1 2 3 4	Speaker signal NC Ground +5V
J11 Keylock and Power LED Connector	1 2 3, 5 4	Power signal Spare Ground Keylock
CN1 PS/2 Keyboard Connector	1 2, 6 3 4 5	Keyboard data NC Ground +5V Keyboard clock
CN2 PS/2 Mouse Connector	1 2, 6 3 4 5	Mouse data NC Ground +5V Mouse clock
CN3 Keyboard Connector	1 2 3 4 5	Keyboard clock Keyboard data NC Ground +5V
CN4 Mouse Connector	1 2 3 4 5	Mouse data NC Ground +5V Mouse clock
CN5 Power Connector	1 2, 10, 11, 12 3 4 5, 6, 7, 8 9	Power good +5V +12V -12V Ground -5V

Table 2-4. Connector Pin Definitions

\* Insert two pin connector wire from Green Power Supply into Connector J3.

### VESA Bus Connector

The cache system board provides two high-performance VESA bus connectors, SL14 and SL15, for use with VESA peripherals. These connectors can be utilized for one Local Bus Master and one Local Bus Slave, either (SL14) or (SL15).

The following tables give the pin assignments for SL14 and SL15. Side A of the connector are pin outs on the board's component side while Side B are pin outs on the board's solder side. Jumpers JV2 and JV3 give more information on settings on the mainboard and the VL-bus controller.

JUMPER	PIN DEFINITION
JV2	CPU Speed Select 1-2 > 33 MHz 2-3 ≤ 33 MHz
JV3	High Speed Write Select 1-2 One wait write 2-3 Zero wait write (default)



**NOTE :** The two VESA Local Bus slot can accommodate either one VESA Master with one VESA Slave or two VESA Slaves.

CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
SL15 — Local Bus Connector	01	DAT01	01	DAT00
	02	DAT03	02	DAT02
	03, 10, 17, 24, 35, 43, 51	Ground	03	DAT04
	04	DAT05	04	DAT06
	05	DAT07	05	DAT08
	06	DAT09	06, 14, 22, 29, 38, 49, 55	Ground
	07	DAT11	07	DAT10
	08	DAT13	08	DAT12
	09	DAT15	09, 20, 32, 57	VCC
	11	DAT17	10	DAT14
	12, 27, 40, 53	VCC	11	DAT16
	13	DAT19	12	DAT18
	14	DAT21	13	DAT20
	15	DAT23	15	DAT22
	16	DAT25	16	DAT24
	18	DAT27	17	DAT26
	19	DAT29	18	DAT28
	20	DAT31	19	DAT30
	21	ADR30	21	ADR31
	22	ADR28	23	ADR29
	23	ADR26	24	ADR27
	25	ADR24	25	ADR25
	26	ADR22	26	ADR23
	28	ADR20	27	ADR21
	29	ADR18	28	ADR19
	30	ADR16	30	ADR17
	31	ADR14	31	ADR15
	32	ADR12	33	ADR13
	33	ADR10	34	ADR11
	34	ADR08	35	ADR09
	36	ADR06	36	ADR07
	37	ADR04	37	ADR05
	38	WBACK#	39	ADR03
39	BE0#	40	ADR02	
41	BE1#	41	NC	
42	BE2#	42	RESET#	
44	BE3#	43	D/C#	
45	ADS#	44	M/IO#	
48	LRDY#	45	W/R#	
49	LDEV0#	48	RDYRTN#	
50	LREQ#	50	IRQ9	
52	LGNT#	51	BRDY#	
54, 55, 56	ID2, 3, 4	52	BLAST#	
57	LKEN#	53, 54	ID0, 1	
58	LEADS#	56	LCLK0	
		58	LBS16#	

Table 2-5. Local Bus Connector Pin Assignment (Continued)

CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
SL14 — Local Bus Connector	01	DAT01	01	DAT00
	02	DAT03	02	DAT02
	03, 10, 17, 24, 35, 43, 51	Ground	03	DAT04
	04	DAT05	04	DAT06
	05	DAT07	05	DAT08
	06	DAT09	06, 14, 22, 29, 38, 49, 55	Ground
	07	DAT11	07	DAT10
	08	DAT13	08	DAT12
	09	DAT15	09, 20, 32, 57	VCC
	11	DAT17	10	DAT14
	12, 27, 40, 53	VCC	11	DAT16
	13	DAT19	12	DAT18
	14	DAT21	13	DAT20
	15	DAT23	15	DAT22
	16	DAT25	16	DAT24
	18	DAT27	17	DAT26
	19	DAT29	18	DAT28
	20	DAT31	19	DAT30
	21	ADR30	21	ADR31
	22	ADR28	23	ADR29
	23	ADR26	24	ADR27
	25	ADR24	25	ADR25
	26	ADR22	26	ADR23
	28	ADR20	27	ADR21
	29	ADR18	28	ADR19
	30	ADR16	30	ADR17
	31	ADR14	31	ADR15
	32	ADR12	33	ADR13
	33	ADR10	34	ADR11
	34	ADR08	35	ADR09
	36	ADR06	36	ADR07
	37	ADR04	37	ADR05
	38	WBACK#	39	ADR03
39	BE0#	40	ADR02	
41	BE1#	41	NC	
42	BE2#	42	RESET#	
44	BE3#	43	D/C#	
45	ADS#	44	M/IO#	
48	LRDY#	45	W/R#	
49	LDEV1#	48	RDYRTN#	
50	LREQ#	50	IRQ9	
52	LGNT#	51	BRDY#	
54, 55, 56	ID2, 3, 4	52	BLAST#	
57	LKEN#	53, 54	ID0, 1	
58	LEADS#	56	LCLK1	
		58	LBS16#	

Table 2-5. Local Bus Connector Pin Assignment

## Memory Subsystem

The 486-GVT-2 is equipped with the memory necessary for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two kinds of memory and gives instructions on how to install each kind on the mainboard.

### Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:

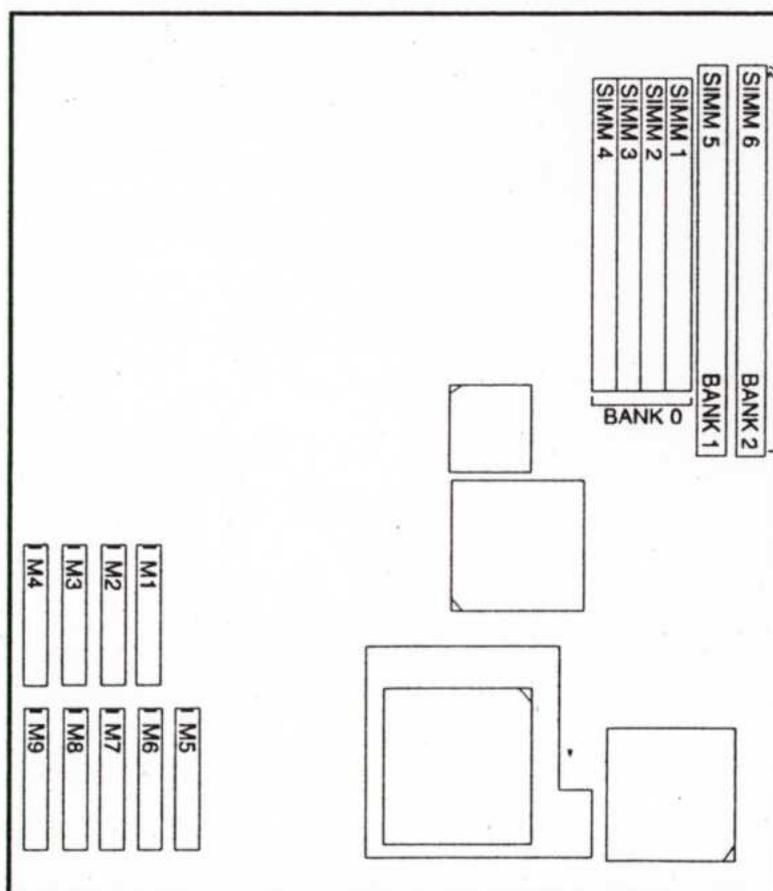


Figure 3-1. Cache and Memory Locations

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## Installing DRAM

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### SIMM Banks

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The 486-GVT-2 can accommodate on-board memory from 1 to 96MB using SIMMs (Single-In-Line Memory Modules). The mainboard has three memory banks — Bank 0, 1, 2. Each bank can accept either a 256KB, 1MB, 4MB, or 16MB SIMM in each socket.

### DRAM Configuration

---

Memory can be installed in a variety of configurations, as shown in the next table:

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
1MB	256K x 4		
		1M x 1	
			1M x 1
2MB	256K x 4	1M x 1	
		1M x 1	1M x 1
	256K x 4		1M x 1
3MB	256K x 4	1M x 1	1M x 1
4MB	1M x 4		
		4M x 1	
			4M x 1
5MB	256K x 4	4M x 1	
	256K x 4		4M x 1
	1M x 4	1M x 1	
	1M x 4		1M x 1
		1M x 1	4M x 1
		4M x 1	1M x 1

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
6MB	256K x 4	4M x 1	1M x 1
	256K x 4	1M x 1	4M x 1
	1M x 4	1M x 1	1M x 1
8MB	1M x 4	4M x 1	
	1M x 4		4M x 1
		4M x 1	4M x 1
9MB	256K x 4	4M x 1	4M x 1
	1M x 4	1M x 1	4M x 1
	1M x 4	4M x 1	1M x 1
12MB	1M x 4	4M x 1	4M x 1
16MB	4M x 4		
		16M x 1	
			16M x 1
17MB	256K x 4	16M x 1	
	256K x 4		16M x 1
		1M x 1	16M x 1
		16M x 1	1M x 1
	4M x 4	1M x 1	
	4M x 4		1M x 1
18MB	256K x 4	1M x 1	16M x 1
	256K x 4	16M x 1	1M x 1
	4M x 4	1M x 1	1M x 1
20MB	1M x 4	16M x 1	
	1M x 4		16M x 1
	4M x 4	4M x 1	
	4M x 4		4M x 1
		4M x 1	16M x 1
		16M x 1	4M x 1

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
21MB	256K x 4	4M x 1	16M x 1
	256K x 4	16M x 1	4M x 1
	1M x 4	1M x 1	16M x 1
	1M x 4	16M x 1	1M x 1
	4M x 4	1M x 1	4M x 1
	4M x 4	4M x 1	1M x 1
24MB	1M x 4	4M x 1	16M x 1
	1M x 4	16M x 1	4M x 1
	4M x 4	4M x 1	4M x 1
32MB	4M x 4	16M x 1	
	4M x 4		16M x 1
		16M x 1	16M x 1
33MB	256K x 4	16M x 1	16M x 1
	4M x 4	1M x 1	16M x 1
	4M x 4	16M x 1	1M x 1
36MB	1M x 4	16M x 1	16M x 1
	4M x 4	4M x 1	16M x 1
	4M x 4	16M x 1	4M x 1
48MB	4M x 4	16M x 1	16M x 1
64MB	16M x 4		
65MB	16M x 4	1M x 1	
	16M x 4		1M x 1
66MB	16M x 4	1M x 1	1M x 1
68MB	16M x 4	4M x 1	
	16M x 4		4M x 1
69MB	16M x 4	1M x 1	4M x 1
	16M x 4	4M x 1	1M x 1
72MB	16M x 4	4M x 1	4M x 1
80MB	16M x 4	16M x 1	
	16M x 4		16M x 1

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
81MB	16M x 4	1M x 1	16M x 1
	16M x 4	16M x 1	1M x 1
84MB	16M x 4	4M x 1	16M x 1
	16M x 4	16M x 1	4M x 1
96MB	16M x 4	16M x 1	16M x 1

Table 3-1. DRAM Configurations

→ **NOTE :** When using double-sided SIMM modules, it is advised that Bank 2 be used instead of Bank 1. If Bank 1 contains a double-sided SIMM module, then Bank 0 (30-pin) is rendered inoperative.

## Installation Instructions

→ **NOTE :** Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.

1. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.
2. Insert the SIMM edge connector at a 90-degree angle onto the socket.

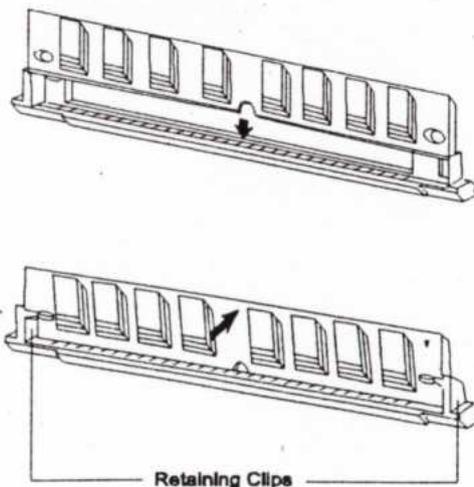


Figure 3-2. Installing SIMMs

- Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.

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## Cache Memory

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The 486-GVT-2 can accept cache memory of 64, 128 or 256KB.

→ **NOTE : Be sure to use the correct chips for the amount of cache memory you want to add. You must install both the correct Cache and Tag SRAM.  
Alter RAM type is always the same as Tag RAM.**

## Installing Cache Memory

---

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the beginning of this manual.**

If you do not have the confidence to make the installation, better consult a service technician for assistance.

- Locate the cache memory on the mainboard.  
See Figure 3-1 again.
- Be guided by the Cache SRAM settings depending on your desired SRAM configuration.

Correct orientation of the chips is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

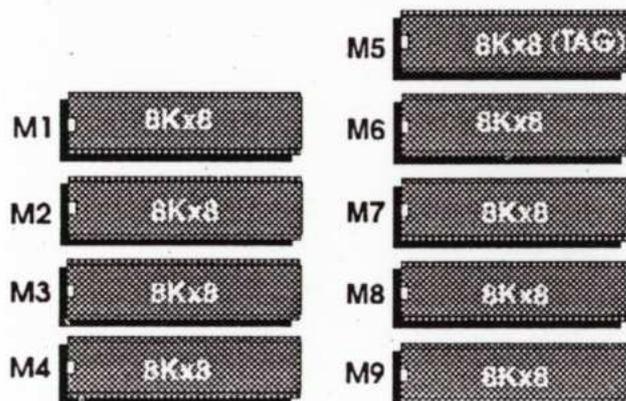
3. Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.
4. Carefully apply enough pressure to partially seat the chip into the socket.

Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.

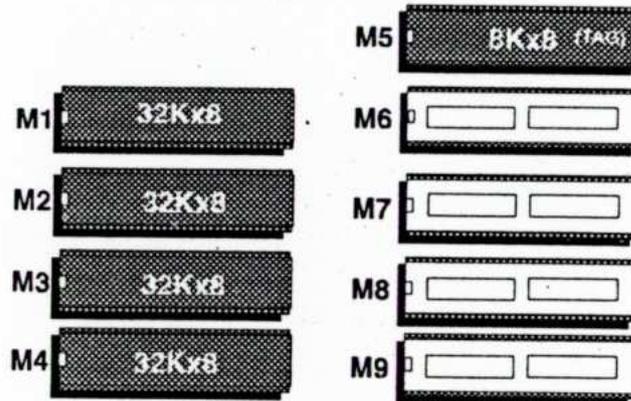
5. Press the chip completely into the socket so that the pins are properly seated.

## Cache SRAM Specifications and Settings

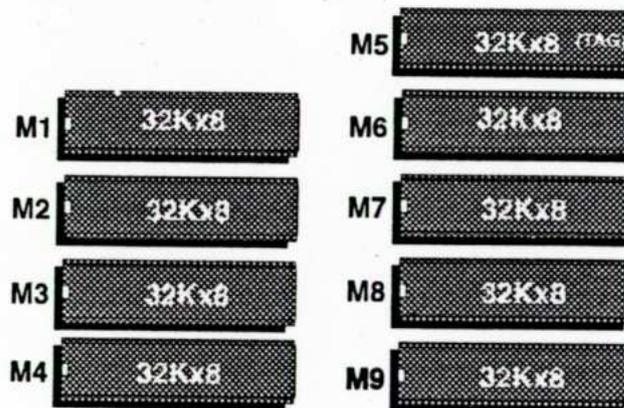
### 64K Cache SRAM



### 128K Cache SRAM



### 256K Cache SRAM



The cache size is jumper selectable. M1 - M4 are assigned as Bank 0 and M6 - M9 are assigned as Bank 1.

	64K	128K	256K
Bank 0	8K x 8	32K x 8	32K x 8
Bank 1	8K x 8	Empty	32K x 8
Tag RAM (M5)	8K x 8	8K x 8	32K x 8
JS1 (Jumper)	1-2	1-2	2-3
JS2 (Jumper)	1-2	2-3	2-3
JS3 (Jumper)	1-2	2-3	1-2

Table 3-2. Cache Configuration Size

## Award BIOS Setup

The 486-GVT-2 comes with the Award BIOS chip that contains the ROM Setup information of your system. This chip serves as an interface between the CPU and the rest of the mainboard's components. This chapter explains the information contained in the Setup program and tells you how to modify the settings according to your system configuration.

### System Setup

A Setup program, built into the system BIOS, is stored in the CMOS RAM that allows the configuration settings to be changed. This program is executed when:

1. User changes system configuration.
2. User changes system backup battery.
3. System detects a configuration error and asks the user to run the Setup program.

After power-on RAM testing, the message "TO ENTER SETUP BEFORE BOOT, PRESS CTRL-ALT-ESC or <DEL>" appears. After pressing the afore mentioned keys, the following screen appears:

ROM ISA BIOS (214L2000) CMOS SETUP UTILITY AWARD SOFTWARE, INC.	
STANDARD CMOS SETUP BIOS FEATURES SETUP CHIPSET FEATURES SETUP POWER MANAGEMENT SETUP LOAD BIOS DEFAULTS LOAD SETUP DEFAULTS	SET CMOS PASSWORD SET POWER ON PASSWORD IDE HDD AUTO DETECTION SAVE AND EXIT SETUP EXIT WITHOUT SAVE
Esc : Quit F10 : Save and Exit Setup	↑ ↓ → ← : Select Item (Shift) F2 : Change Color
Time, Date, Hard Disk Type	

Use the arrow keys to select and press **<Enter>** to run the selected program.

## Standard CMOS Setup

The Standard CMOS Setup has ten items for setting. Each item may have one or more option settings. Use the arrow keys to highlight the item and then use the **<PgUp>**, or **<PgDn>** keys to select the value you want in each item.

ROM ISA BIOS (214L2000)					
STANDARD CMOS SETUP					
AWARD SOFTWARE, INC.					
Date (mm: dd: yy)	: Tues., August 31 1993				
Time (hh: mm: ss)	: 12 : 37 : 05				
DAYLIGHT SAVING	: Disabled				
	CYLS.	HEADS	PRECOMP	LANDZONE	SECTORS
Drive C: User (81MB)	: 611	16	0	0	17
Drive D: None (0MB)	: 0	0	0	0	0
Drive A	: 1.2MB, 5.25 in.		Base Memory : 640K		
Drive B	: 1.44MB, 3.5 in.		Extended Memory : 7168K		
Video	: EGA/VGA		Expanded Memory : 0K		
			Other Memory : 384K		
Halt on	: All Errors		Total Memory : 8192K		
Esc : Quit	↑ ↓ → ← : Select Item		PgUp/PgDn/+/- : Modify		
F1 : Help	(Shift) F2 : Change Color		F3 : Toggle Calendar		

The Standard CMOS Setup screen is displayed above. System BIOS automatically detects memory size, thus no changes are necessary. Press "**F3**" function key to show the calendar.

### Daylight Saving

When enabled, this field allows user to set the clock one hour in advance. When disabled, it subtracts one hour when standard time begins. After the changes are made, press **<Esc>** to return to main menu.

## BIOS Features Setup

ROM ISA BIOS (214L2000) BIOS FEATURES SETUP AWARD SOFTWARE, INC.	
Virus Warning : Enabled	System BIOS Shadow : Enabled
CPU Internal Cache : Enabled	Video BIOS Shadow : Enabled
External Cache : Enabled	C8000-CBFFF Shadow : Disabled
Quick Power-On Self-Test : Disabled	CC000-CFFFF Shadow : Disabled
Boot Sequence : A:, C:	D000-D3FFF Shadow : Disabled
Boot Up Floppy Seek : Enabled	D4000-D7FFF Shadow : Disabled
Boot Up Numlock Status : On	D8000-DBFFF Shadow : Disabled
Boot Up System Speed : High	DC000-DFFFF Shadow : Disabled
IDE HDD Block Mode : Disabled	E0000-EFFFF Shadow : Disabled
Gate A20 Option : Fast	
Memory Parity Check : Disabled	
Typeomatic Rate Setting : Disabled	
Typeomatic Rate (Chars/Sec) : 6	
Typeomatic Delay (Msec) : 250	
Esc : Quit F1 : Help F5 : Old Values F6 : Load BIOS Defaults F7 : Load Setup Defaults	
↑ ↓ → ← : Select Item PgUp/PgDn/+/- : Modify (Shift) F2 : Change Color	

## Chipset Features Setup

ROM ISA BIOS (214L2000) CHIPSET FEATURES SETUP AWARD SOFTWARE, INC.	
Decoupled Refresh : Enabled	
Relocate 256K/384K : Disabled	
Video BIOS Cacheable : Enabled	
System BIOS Cacheable : Enabled	
External Cache Scheme : Write Back	
Memory Hole At 15Mb Addr : Disabled	
Cache Timing Control : Turbo	
DRAM Timing Control : Fast	
Fast DRAM : Enabled	
Esc : Quit F1 : Help F5 : Old Values F6 : Load BIOS Defaults F7 : Load Setup Defaults	
↑ ↓ → ← : Select Item PgUp/PgDn/+/- : Modify (Shift) F2 : Change Color	

Moving around the BIOS and Chipset Features Setup programs shown works the same way as moving around the Standard CMOS Setup program. Users are not encouraged to run the BIOS and Chipset Features Setup programs. Your system should have been fine-tuned before shipping. Improper Setup may cause the system to fail, consult your dealer before making any changes.

## Power Management Setup

Many PC users never turn their computers off because of delays in reloading their operating system or applications. An energy efficient mainboard combats such energy waste by using System Management Mode (SMM), static technology, and processor clock control to conserve energy.

During periods of system inactivity, SMM automatically initiates a "Sleep" mode, reducing both system and monitor power. Power Management Setup allows you to blank out the VGA display, slowdown or turn off CPU speed, and turn off HDD spindle motor during a set period of time.

### Regular CPU

ROM ISA BIOS (214L2000) POWER MANAGEMENT SETUP AWARD SOFTWARE, INC.	
Power Management : Disabled Doze Timer : 4 min.	
Sleep Timer : 8 min. Sleep Mode : Sleep	
HDD Power Management : Disabled VGA Activity Wakeup : Enabled	
Esc : Quit F1 : Help F5 : Old Values F6 : Load BIOS Defaults F7 : Load Setup Defaults	
↑ ↓ → ← : Select Item PgUp/PgDn/+/- : Modify (Shift) F2 : Change Color	

FULL-ON CPU SPEED	DOZE MODE CPU SPEED	SLEEP MODE CPU SPEED
50 MHz	16 MHz	16 MHz
40 MHz	20 MHz	20 MHz
33 MHz	8 MHz	8 MHz
25 MHz		

Table 4-1. Regular CPU Slowdown Speed

ITEM	FUNCTION
Power Management	Choices are "Enabled" and "Disabled". Allows you to use the Power Management features when "Enabled".
VGA Activity Wakeup	Choices are "Enabled" and "Disabled". When "Enabled", it allows the Doze Timer to start counting when no activity is detected on the VGA display. Otherwise, when "Disabled", Doze Timer will start counting immediately even if there is activity on the VGA display.
Doze Timer	Choices are "1, 4, 16, and 32min." after which, CPU speed will slowdown and enter "Doze Mode" assuming there is no operation during the selected period (refer to the previous table for the corresponding CPU slowdown speed). Normal CPU speed is resumed upon pressing any key.
Sleep Mode	Choices are "Sleep" and "Disabled". When set at "Disabled", it renders the Sleep Timer inoperative.
Sleep Timer *	Choices are "2, 8, 16, and 32min." after which VGA display will blank out and enter "Sleep Mode" assuming there is no operation during the selected period. (E.g., If Doze Timer = 1min. and Sleep Timer = 8min., then VGA display blanks out after 9min.) CPU speed is the same as that under "Doze Mode". Normal VGA display is resumed upon pressing any key.
HDD Power Management	Choices are "Enabled" and "Disabled". When "Enabled", HDD spindle motor will turn off after a certain time period. This feature would depend on the HDD type used.

\* When using a Green Power Supply, VGA display not only blanks out but power to display monitor would be cut thereby, conserving more electricity. Insert two pin connector wire into Connector J3 of the mainboard.

Table 4-2. Power Management Setup Screen Features

**SMM  
CPU**

ROM ISA BIOS (214L2000) POWER MANAGEMENT SETUP AWARD SOFTWARE, INC.	
Power Management : Disabled Doze Timer : 4 min. Doze Mode Speed : CLKIN/4	
Sleep Timer : 8 min. Sleep Mode : Suspend HDD Power Management : Disabled VGA Activity Wakeup : Enabled	
Esc : Quit F1 : Help F5 : Old Values F6 : Load BIOS Defaults F7 : Load Setup Defaults	↑ ↓ → ← : Select Item PgUp/PgDn/+/- : Modify (Shift) F2 : Change Color

FULL-ON CPU SPEED	DOZE MODE CPU SPEED	SLEEP MODE CPU SPEED	SUSPEND MODE CPU SPEED
33 MHz	8 MHz	8 MHz	0 MHz
25 MHz	12.5 MHz	12.5 MHz	0 MHz

*Table 4-3. SMM CPU Slowdown Speed*

Same features as that of regular CPUs Power Management Setup screen except for an additional "Doze Mode Speed" which allows you the benefit of setting the CPU slowdown speed (e.g., CLKIN/4 = normal SMM CPU speed divided by four). Choices are CLKIN/2 and CLKIN/4. SMM CPUs include a "Suspend" feature in Sleep Mode which stops the CPU clock completely (0MHz) after the CPU remains non-operational during the selected period. Follow the same procedure in setting Sleep Timer for regular CPUs (see Table 4-2).



**NOTE :** When VGA Activity Wakeup is set "Disabled", always divide the Doze Timer value by two (e.g., Doze Timer : 4 min., CPU speed will slowdown after 2 min.). Some Operating Systems may not maintain the correct computer clock time during "Suspend Mode".

## **Load BIOS Default**

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BIOS defaults contain the most appropriate values of the system parameters that allow minimum system performance. The OEM manufacturer may change the defaults through MOD-BIN before the binary image burns into the ROM.

## **Load Setup Default**

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Selecting this field loads the factory defaults for BIOS and Chipset Features which the system automatically detects.

## Password Setting

When you select this function, you can create a password. Type your password up to eight characters and press **<Enter>**. You will be asked to confirm the password. Type the password again and press **<Enter>**. You may also press **<Esc>** to abort the selection and not enter a password. To disable password, press **<Enter>** when you are prompted to enter password. A message appears, confirming the password is disabled. When the password is disabled, the system boots and you can enter Setup freely.

### Security Option

If you select **System** under this field, you will be prompted for the password every time your system is rebooted or any time you try to enter Setup. If you select **Setup**, you will be prompted only when you try to enter Setup.

### Clear Password

If you forget your password, turn off the system power first and remove the system unit cover. Locate Jumper J7 and cap it. Turn the system power back on and screen will display the message below:

**PASSWORD IS SET DISABLED  
PLEASE REMOVE JUMPER (J7) BEFORE  
SETTING UP NEW PASSWORD**

This message indicates that the password is disabled. Remove Jumper J7 and enter CMOS Setup to set new password.

## Exiting Setup

After you have made changes under Setup, press **<Esc>** to return to the main menu. Move cursor to **"Save and Exit Setup"** or press **"F10"** and then press **"Y"** to change the CMOS Setup. If you did not change anything, press **<Esc>** again or move cursor to **"Exit Without Saving"** and press **"Y"** to retain the Setup settings.

ROM ISA BIOS (214L2000) CMOS SETUP UTILITY AWARD SOFTWARE, INC.	
STANDARD CMOS SETUP	SET CMOS PASSWORD
BIOS FEATURES SETUP	SET POWER ON PASSWORD
CHIPSET FEATURES SETUP	IDE HDD AUTO DETECTION
POWER MANAGEMENT SETUP	SAVE AND EXIT SETUP
LOAD BIOS DEFAULTS	EXIT WITHOUT SAVING
LOAD SETUP	SAVE to CMOS and EXIT (Y/N)? Y
Esc : Quit	↑ ↓ → ← : Select Item
F10 : Save and Exit Setup	(Shift) F2 : Change Color
SAVE DATA TO CMOS and EXIT SETUP	



**NOTE : Default values of the various Setup items on this chapter may not necessarily be the same ones shown on your screen.**

## Hard Disk Specifications

This appendix contains some technical information about the different IDE hard disks drives which can be installed with your 486-GVT-2 mainboard.

### CONNER

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
CP-30124	120MB	895	5	55
CP-30174	170MB	903	8	46
CFS-210A	213MB	685	16	38
CP-30344	340MB	904	16	46

### MAXTOR

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
7120A	120MB	1023	14	17
7131A	131MB	1002	8	32
7213A	213MB	683	16	38
7245A	245MB	967	16	31
7345A	345MB	790	15	57

### QUANTUM

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
LPS-120AT	120MB	901	5	53
LPS-240AT	240MB	723	13	51
LPS-270AT	270MB	944	14	40
LPS-540AT	540MB	1120	16	59
ELS-127AT	127MB	919	16	17
ELS-170AT	170MB	1011	15	22

**SEAGATE**

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
ST3144A	130MB	1001	15	17
ST3283A	240MB	978	14	35

**WESTERN DIGITAL**

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
AC2120	120MB	872	8	35
AC2170	170MB	1010	6	55
AC2200	212MB	989	12	35
AC2250	256MB	1010	9	55
AC2340	340MB	1010	12	55

**PRIAM**

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
S19	152MB	1024	15	17