486-GIO-VT2

MAIN BOARD MANUAL

Correction Note

User Manual 486-GIO-VT2 Rev. B0 Dated July 1994, Page 3-7

Dear Users:

The "M1-M4" in the first line paragraph is changed to "M2-M5".

The "(M5)" in the third row Table 3-2 is changed to "(M1)".

Thank for your attention.

The cache size is jumper selectable. M2-M5 are assigned as Bank 0 and M6-M9 are assigned as Bank1.

	64K	128K	256K
Bank 0	8K x 8	32K x 8	32K x 8
Bank 1	8K x 8	Empty	32K x 8
Tag RAM (M1)	8K x 8	8K x 8	32K x 8
JS1 (Jumper)	1-2	1-2	2-3
JS2 (Jumper)	1-2	2-3	2-3
JS3 (Jumper)	1-2	2-3	1-2

486-GIO-VT2

MAIN BOARD
User's Guide

DOC No. : 13369
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HANDLING PRECAUTIONS

→ **Static electricity may cause damage to the integrated circuits on the mainboard. Before handling any mainboard outside of its protective packaging, ensure that there is no static electric charge in your body.**

Observe any or all of these basic precautions when handling the mainboard or other computer components:

- Wear a static wrist strap which fits around your wrist and is connected to a natural earth ground.
- Touch a grounded or anti-static surface or a metal fixture such as a water pipe.
- Avoid contact with the components on add-on cards, boards and modules and with the "golden finger" connectors plugged into the expansion slot. It is best to handle system components by their mounting bracket.

Above methods either prevent static build-up or cause it to be discharged properly.

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ABOUT THIS MANUAL

This manual is designed to guide you and facilitate your use of the 486-GIO-VT2 mainboard. It is divided into chapters and appendices. The chapters contain the main body of information normally referred to by users. The appendices provide more detailed technical information for reference.

Chapter 1 gives an overview and introduces the basic parts and features of the mainboard.

Chapter 2 gives information on the jumper and connector settings on the mainboard.

Chapter 3 provides information on the mainboard's memory subsystem consisting of SIMMs and Cache memory and describes how you can upgrade memory.

Chapter 4 briefly explains the mainboard's Award BIOS system Setup in general and tells you how to run it and change the system configuration settings.

Appendix A provides relevant technical information.

Appendix B provides information on the VIA VT83C461 or Promise PDC20230 local bus IDE controller device driver installation (option).

NOTE : The material in this manual is for information only and is subject to change without notice. We reserve the right to make changes in the product design without reservation and without notification to its users. We shall not be liable for technical or editorial omissions made herein; nor for incidental or consequential damages resulting from the furnishing, performance, or use of this material.

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Overview

Based on an ISA/VL-bus, the 486-GIO-VT2 mainboard empowers any high-end system to exploit a wide-range of hardware and software capabilities and applications. The board's special feature is the VIA GMC chipset, a highly integrated single chipset that supports write-back and SMM (System Management Mode) CPUs, multi-master operations and provides built-in power management features ideal for Green PCs. This chapter gives you a brief overview of this mainboard, providing basic information on its major parts and components.

Specifications

The 486-GIO-VT2 mainboard comes with the following features:

- Supports Intel 80486SX/DX/IntelDX2™/IntelDX4™/486 SL-Enhanced/Cyrix Cx486S/DX microprocessor in PGA packages.
- VIA GMC VT82C486A PC/AT chipset includes built-in 8042 keyboard controller.
- Award BIOS.
- Supports 64/128/256K direct-mapped write-back/write-through cache memory.
- 72-pin SIMM sockets supports 1 up to 64MB DRAM, provides page mode DRAM operation.
- Supports system and video BIOS cacheable and shadow.
- Supports decoupled DRAM refresh.
- Optional built-in ZIF socket that accepts Intel's OverDrive™ processors.
- Five 16-bit and one 8-bit ISA expansion slots.
- Supports two VESA bus slots for Local bus master or slave.

- Dallas DS12887/DS12885Q/VIA VT82885 real time clock/calendar.
- Built-in IDE HDD/FDD and Local Bus IDE interface with enhanced PIO mode-3 (VT83C461 only) (can support two channel IDE connector).
- Two serial/one parallel (support EPP/ECP for W83787/83777 only) / and one game port.
- Optional Flash ROM.
- VIA VT83C461/PDC20230/Local Bus IDE Controller (optional)
- Provides built-in power management features ideal for Green PCs.

Mainboard Layout

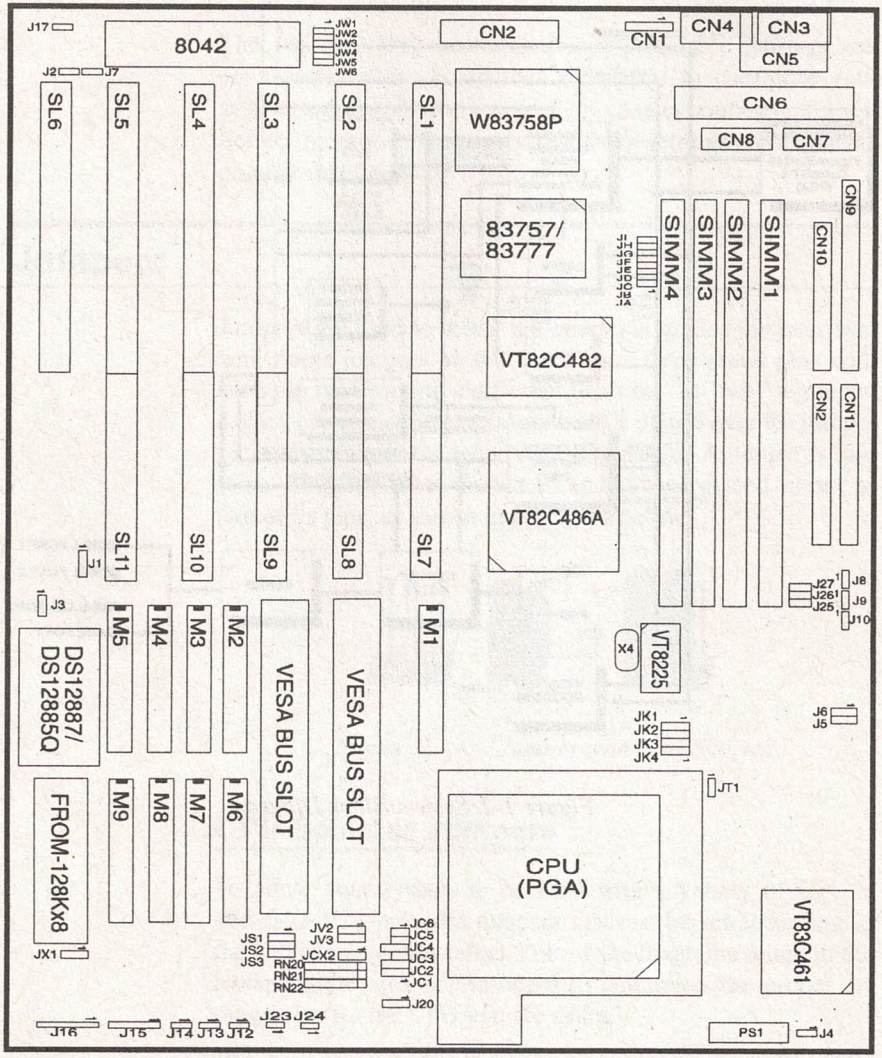

Figure 1-1. Mainboard Layout

System Block Diagram

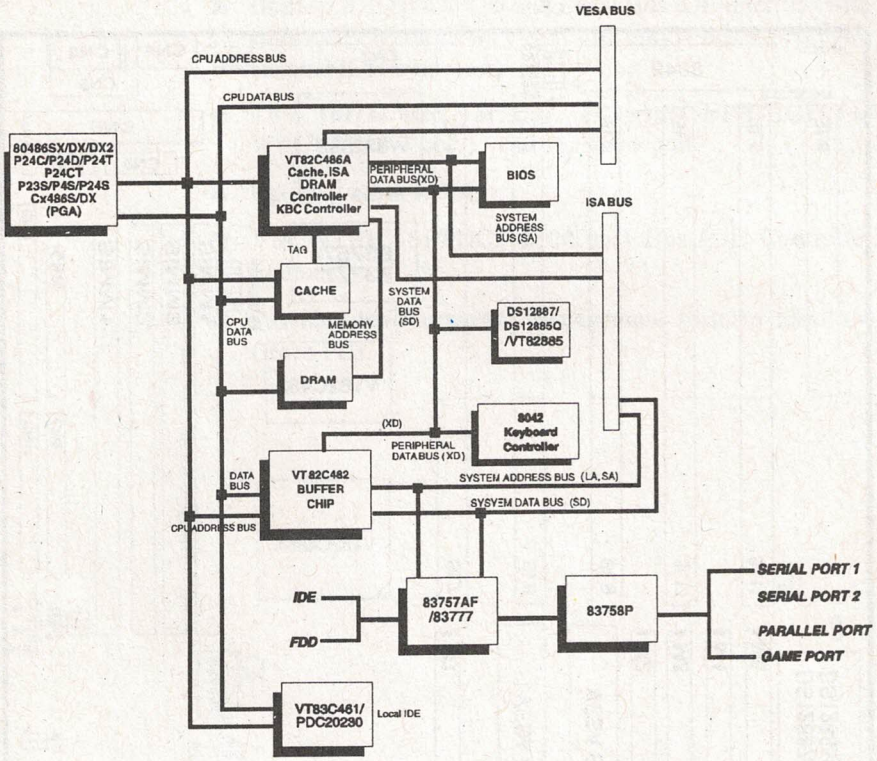

Figure 1-2. System Block Diagram

Mainboard Settings

The 486-GIO-VT2 has several user-adjustable jumpers and connectors on the board that allow you to configure your system to suit your every need. This chapter contains information on the various jumper and connector settings you can make on your mainboard.

Jumpers

Jumpers are used to select the operation modes for your system. Some jumpers on the board have three metal pins with each pin representing a different function. To "set" a jumper, a black cap containing metal contacts is placed over the jumper pin/s according to the required configuration. A jumper is said to be "shorted" when the black cap has been placed on one or two of its pins, as shown in the figure below:

Figure 2 - 1 Jumper with Pins Shorted

CPU Selector Jumpers

To allow your system to be used with a variety of CPU's, 486-GIO-VT2 provides jumpers that can be set according to the CPU you want installed. Follow the diagrams found in the lower-middle area of the board to determine the proper arrangement for the CPU you are using.

The next three tables summarizes the settings of the CPU Selector jumpers:

JUMPER	486SX/ P23S* (PGA)	P24S*/P4S* P24C#/ 486DX/ IntelDX2™ (PGA)	P24CT/P24T (PGA)	Cx486S (M6) (PGA)	Cx486DX (M7) Cx486S+ Cx487S (M6+C6) (PGA)	P24D* (PGA)
JC1, JC2	2-3	1-2	1-2	2-3	1-2	1-2
JC3	open	open	shorted	open	open	open
JC4	1-2	1-2	2-3	1-2	1-2	2-3

* P23S, P24S, P24D, and P4S are the SL-enhanced CPUs while P24T is the Overdrive Processor.

→ **# NOTE : When the onboard 3.3 volt regulator is not present, the 3.3 volt daughter board should be installed. If not, please refer to page 2-13 installation of the 3.3 volt regulator daughterboard.**

JUMPER (RP0 Ω8P4R)	P23S/P4S/ P24S/P24T (PGA)	486SX/DX/ IntelDX2™ (PGA)	Cx486S/DX (PGA)	P24C/P24D/ P24CT (PGA)
JC5, JC6	shorted	open	open	shorted
RN20	empty	empty	empty	empty
RN21	empty	empty	empty	inserted
RN22	empty	empty	inserted	empty

JUMPER	PIN DEFINITION
J20	P24C Clock Mode Select Open 3 X mode (default) 1-2 2 X mode 2-3 2.5 X mode
JCX2	1-2 Intel SL-enhanced CPU, others (default) 2-3 Cyrix Cx486S/DX/P24D For Internal Write back CPU
JX1	2-3 (factory default)
JP2	2-3 (factory default)
JP1	2-3 (factory default)

Table 2-1. Jumper Settings for CPU Selector

JUMPER	PIN DEFINITION
J2	Display Type Select Open Mono/EGA/VGA (default) Short Color
J3	External, Internal Battery Select 1-2 External battery 2-3 Internal battery (default)
J4	Local IDE Select 1-2 Enable (default) 2-3 Disable
J5, J6	HDD Speed Select (VT83C461/PDC 20230 Only) IDE Type J5 J6 Speed 0 2-3 2-3 Speed 1 1-2 2-3 (default) Speed 2 1-2 1-2
J7	Password Clear Short Clear password Open (default)
J9	Local HDD_BALE Short Enable Open Disable (default)
J10	Local HDD_IOCHRDY Short Enable Open Disable (default)
J26	ISA HDD_BALE Short Enable Open Disable (default)
J27	ISA HDD_IOCHRDY Short Enable Open Disable (default)
JT1	P24T/P24CT/P24D Write-back/Write-through Select Short Write-back Open Write-through (default)

Table 2-2. Jumper Definitions

→ **NOTE : Users are not encouraged to change the jumper settings not listed in this manual as they are considered factory defaults which may adversely affect system performance.**

On-board I/O Jumper

JUMPER	FUNCTION	SETTINGS		DESCRIPTION
JA, JB	RS-232-I	JA	JB	
		1-2 Short	1-2 Short	Disable
		1-2 Short	2-3 Short	3E8
		2-3 Short	1-2 Short	3F8 (default)
		2-3 Short	2-3 Short	2E8
JC, JD	RS-232-II	JC	JD	
		1-2 Short	1-2 Short	Disable
		1-2 Short	2-3 Short	2E8
		2-3 Short	1-2 Short	2F8 (default)
		2-3 Short	2-3 Short	3E8
JE, JF	LPT1	JE	JF	
		1-2 Short	1-2 Short	Disable
		1-2 Short	2-3 Short	378 (default)
		2-3 Short	1-2 Short	278
		2-3 Short	2-3 Short	3BC
JG	IDE	2-3 Short		Enable (default)
		1-2 Short		Disable
JH	FDC	2-3 Short		Enable (default)
		1-2 Short		Disable
JI	LPT OE	Short		O/P Port (default)
		Open		Bi-directional
*JW3,JW4	PRT mode	JW3	JW4	
		2-3	2-3	PRINTER
		2-3	1-2	EPP/SPP
		1-2	2-3	EPP/ECP
		1-2	1-2	EXT2FDD
*JW5,JW6	ECP mode	JW5	JW6	
		1-2	1-2	DMA1
		2-3	2-3	DMA3

*JW3, JW4, JW5 and JW6 are the enhanced parallel port (EPP) and Extended Capabilities port (ECP) for W83787/83777 only.

Table 2-3. On-board I/O Jumper Definition

CPU Clock Jumper JK1-JK4 (VT8225N)

CLK 2	JK1	JK2	JK3	JK4
50 MHz	2-3	1-2	2-3	2-3
40 MHz	1-2	1-2	2-3	1-2
33.3 MHz	2-3	2-3	1-2	1-2
25 MHz	2-3	1-2	2-3	1-2

Table 2-4. CPU Clock Jumper Selection JK1-JK4 (VT8225N)

Connectors

The connectors allow the mainboard to connect electronically with other parts of the system. Some connectors have two pins, others have four or five pins. Some malfunction problems encountered with your system may be caused by loose or improper connections. Ensure that all connections are in place and firmly attached.

CONNECTOR	PIN OUTS	SIGNAL NAME
CN1 Mouse Connector	1 2 3 4 5	Mouse data NC Ground + 5V Mouse clock
CN2 Game Port Connector	1, 8, 9, 15 2 3 4, 5, 12 6 7 10 11 13 14 16	VCC D4 D0 Ground D1 D5 D6 D2 D3 D7 Not used
CN3 PS/2 Keyboard Connector	1 2, 6 3 4 5	Keyboard data NC Ground + 5V Keyboard clock

Table 2-5. Connector Pin Definitions (Continued)

CN4 PS/2 Mouse Connector	1 2, 6 3 4 5	Mouse data NC Ground + 5V Mouse clock
CN5 Keyboard Connector	1 2 3 4 5	Keyboard clock Keyboard data NC Ground +5V
CN6 Power Connector	1 2, 10, 11, 12 3 4 5, 6, 7, 8 9	Power good +5V +12V –12V Ground –5V
CN8, CN7 Serial Port 1, 2 Connector	1 2 3 4 5 6 7 8 9	Data carrier detect Receive data Transmit data Data transmit ready Signal ground Ready to receive data Request to send data Clear to send Ring indicator
CN9 FDD Connector	2 4, 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33	Density selection NC Index detection Select motor A Select drive A Select drive B Select motor B Direction control Step pulse Write data Write enable Track 0 Write protect Read data Head select Disk change Ground

Table 2-5. Connector Pin Definitions (Continued)

CONNECTOR	PIN OUTS	SIGNAL NAME
CN10 Parallel Port Connector	1	LPT strobe
	2	Data bit 0
	3	Data bit 1
	4	Data bit 2
	5	Data bit 3
	6	Data bit 4
	7	Data bit 5
	8	Data bit 6
	9	Data bit 7
	10	LPT acknowledge
	11	LPT busy
	12	Paper end
	13	Selected status
	14	Auto line feed
	15	LPT error
	16	Initiate printer
	17	Select printer
	18-25	Ground
CN11 Primary IDE HDD Conector	1	Reset hard disk
	2, 19, 22, 24, 26, 30, 40	Ground
	3	HDD7
	4	HDD8
	5	HDD6
	6	HDD9
	7	HDD5
	8	HDD10
	9	HDD4
	10	HDD11
	11	HDD3
	12	HDD12
	13	HDD2
	14	HDD13
	15	HDD1
	16	HDD14
	17	HDD0
	18	HDD15
	20, 21, 29, 34	NC
	23	HDD I/O write
	25	HDD I/O read
	27	IOCHRDY
	28	HDD address latch
	31	IRQ14
	32	IOCS16
	33	HDD A1
	35	HDD A0
	36	HDD A2
	37	HDD chip select 0
	38	HDD chip select 1
	39	HDD active

CONNECTOR	PIN OUTS	SIGNAL NAME
CN12 Secondary IDE HDD Conector	1	Reset hard disk
	2, 19, 22, 24, 26, 30, 40	Ground
	3	HDD7
	4	HDD8
	5	HDD6
	6	HDD9
	7	HDD5
	8	HDD10
	9	HDD4
	10	HDD11
	11	HDD3
	12	HDD12
	13	HDD2
	14	HDD13
	15	HDD1
	16	HDD14
	17	HDD0
	18	HDD15
	20, 21, 29, 34	NC
	23	HDD I/O write
	25	HDD I/O read
	27	IOCHRDY
	28	HDD address latch
	31	IRQ15
	32	IOCS16
	33	HDD A1
	35	HDD A0
	36	HDD A2
	37	HDD chip select 0
	38	HDD chip select 1
	39	HDD active

Table 2-5. Connector Pin Definitions (Continued)

CONNECTOR	PIN OUTS	SIGNAL NAME
J1 External Battery Connector	1	Anode+
	2, 3	NC
	4	Cathode –
J8 Primary HDD_LED Connector	1	VCC
	2	LED
J25 Secondary HDD_LED Connector	1	VCC
	2	LED
J12 Turbo Switch	1	Turbo Signal
	2	Ground

J13 Turbo LED	1 2	VCC LED
J14 Hardware Reset	1 2	Ground Reset signal
J15 Speaker Connector	1 2 3 4	Speaker signal NC Ground + 5V
J16 Keylock and Power LED Connector	1 2 3, 5 4	Power signal Spare Ground Keylock
J17 * Green Power Supply Connector	1 2	Enable/Disable power supply outlet Ground
J23 Suspend LED	1 2	VCC LED
J24 Suspend Switch	1 2	Suspend Signal Ground
PS1 3.3V Daughter Board Connector	1, 3, 14, 16 2, 4, 13, 15 6, 11 7, 8, 9, 10	+ 3.3V + 5V + 12V Ground

* Insert two pin connector wire from Green Power Supply into Connector J17.

Table 2-5. Connector Pin Definitions

CPU Power Connector

PS1 CONNECTOR	SETTINGS	DESCRIPTION
For 5V CPU	1-2 3-4 13-14 15-16	Short
For 3.3V CPU	3.3V Daughter Board	install

Table 2-6. CPU Power Connector

VESA Bus Connector

The cache system board provides two high-performance VESA bus connectors, SL12 and SL13, for use with VESA peripherals. These connectors can be utilized for one Local Bus Master and one Local Bus Slave, either (SL12) or (SL13).

The following tables give the pin assignments for SL12 and SL13. Side A of the connector are pin outs on the board's component side while Side B are pin outs on the board's solder side. Jumpers JV2 and JV3 give more information on settings on the mainboard and the VL-bus controller.

JUMPER	PIN DEFINITION
JV2	CPU Speed Select 1-2 > 33 MHz 2-3 ≤ 33 MHz
JV3	High Speed Write Select 1-2 One wait write 2-3 Zero wait write (default)

Table 2-7. ISA/VESA Bus Connector

CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
SL12 — Local Bus Connector	01	DAT01	01	DAT00
	02	DAT03	02	DAT02
	03, 10, 17, 24, 35, 43, 51	Ground	03	DAT04
	04	DAT05	04	DAT06
	05	DAT07	05	DAT08
	06	DAT09	06, 14, 22, 29, 38, 49, 55	Ground
	07	DAT11	07	DAT10
	08	DAT13	08	DAT12
	09	DAT15	09, 20, 32, 57	VCC
	11	DAT17	10	DAT14
	12, 27, 40, 53	VCC	11	DAT16
	13	DAT19	12	DAT18
	14	DAT21	13	DAT20
	15	DAT23	15	DAT22
	16	DAT25	16	DAT24
	18	DAT27	17	DAT26
	19	DAT29	18	DAT28
	20	DAT31	19	DAT30
	21	ADR30	21	ADR31
	22	ADR28	23	ADR29
	23	ADR26	24	ADR27
	25	ADR24	25	ADR25
	26	ADR22	26	ADR23
	28	ADR20	27	ADR21
	29	ADR18	28	ADR19
	30	ADR16	30	ADR17
	31	ADR14	31	ADR15
	32	ADR12	33	ADR13
	33	ADR10	34	ADR11
	34	ADR08	35	ADR09
	36	ADR06	36	ADR07
	37	ADR04	37	ADR05
	38	WBACK#	39	ADR03
	39	BE0#	40	ADR02
	41	BE1#	41	NC
	42	BE2#	42	RESET#
	44	BE3#	43	D/C#
	45	ADS#	44	M/IO#
	48	LRDY#	45	W/R#
	49	LDEV0#	48	RDYRTN#
	50	LREQ#	50	IRQ9
	52	LGNT#	51	BRDY#
	54, 55, 56	ID2, 3, 4	52	BLAST#
	57	LKEN#	53, 54	ID0, 1
	58	LEADS#	56	LCLK0
			58	LBS16#

Table 2-8. Local Bus Connector Pin Assignment (Continued)

CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
SL13 — Local Bus Connector	01	DAT01	01	DAT00
	02	DAT03	02	DAT02
	03, 10, 17, 24, 35, 43, 51	Ground	03	DAT04
	04	DAT05	04	DAT06
	05	DAT07	05	DAT08
	06	DAT09	06, 14, 22, 29, 38, 49, 55	Ground
	07	DAT11	07	DAT10
	08	DAT13	08	DAT12
	09	DAT15	09, 20, 32, 57	VCC
	11	DAT17	10	DAT14
	12, 27, 40, 53	VCC	11	DAT16
	13	DAT19	12	DAT18
	14	DAT21	13	DAT20
	15	DAT23	15	DAT22
	16	DAT25	16	DAT24
	18	DAT27	17	DAT26
	19	DAT29	18	DAT28
	20	DAT31	19	DAT30
	21	ADR30	21	ADR31
	22	ADR28	23	ADR29
	23	ADR26	24	ADR27
	25	ADR24	25	ADR25
	26	ADR22	26	ADR23
	28	ADR20	27	ADR21
	29	ADR18	28	ADR19
	30	ADR16	30	ADR17
	31	ADR14	31	ADR15
	32	ADR12	33	ADR13
	33	ADR10	34	ADR11
	34	ADR08	35	ADR09
	36	ADR06	36	ADR07
	37	ADR04	37	ADR05
	38	WBACK#	39	ADR03
	39	BE0#	40	ADR02
	41	BE1#	41	NC
	42	BE2#	42	RESET#
	44	BE3#	43	D/C#
	45	ADS#	44	M/IO#
	48	LRDY#	45	W/R#
	49	LDEV1#	48	RDYRTN#
	50	LREQ#	50	IRQ9
	52	LGNT#	51	BRDY#
	54, 55, 56	ID2, 3, 4	52	BLAST#
	57	LKEN#	53, 54	ID0, 1
	58	LEADS#	56	LCLK1
			58	LBS16#

Table 2-8. Local Bus Connector Pin Assignment

3.3 Volt regulator board installation

This section describes the installation of the 3.3 volt regulator board used for the IntelDX4 CPU.

The IntelDX4 CPU is a new member of the Intel 486 processor family based on the Intel 486DX2 microprocessor core. It offers features such as System management mode (SMM) and stop Clock Mode ideal for power managememt function. It's internal core frequency can operate to maximum of 100MHZ. It also operates with a 3.3 volt (Vcc) supply.

If the on board 3.3 volt regulator is not present, the 3.3 volt regulator must be installed before using the InterDX4 CPU. Please also refer to the steps below on how to install the 3.3 volt regulator.

Please also refer to page 2-2 for the correct CPU jumper selection.

1. Remove jumpers from connector PS1.

2. Please the 3.3 volt regulator board as shown on the figure below with the correct pin orientation.

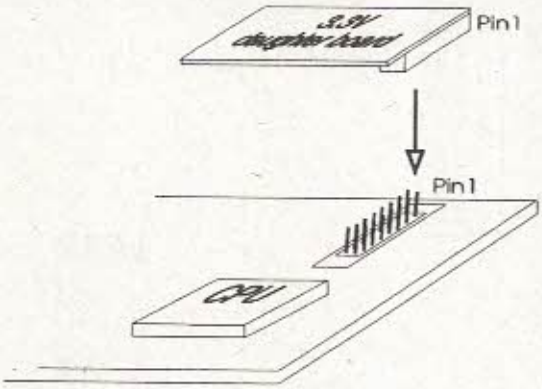

Figure 2 - 1. 3.3 Volt regulator board installation

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Memory Subsystem

The 486-GIO-VT2 is equipped with the memory necessary for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two kinds of memory and gives instructions on how to install each kind on the mainboard.

Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:

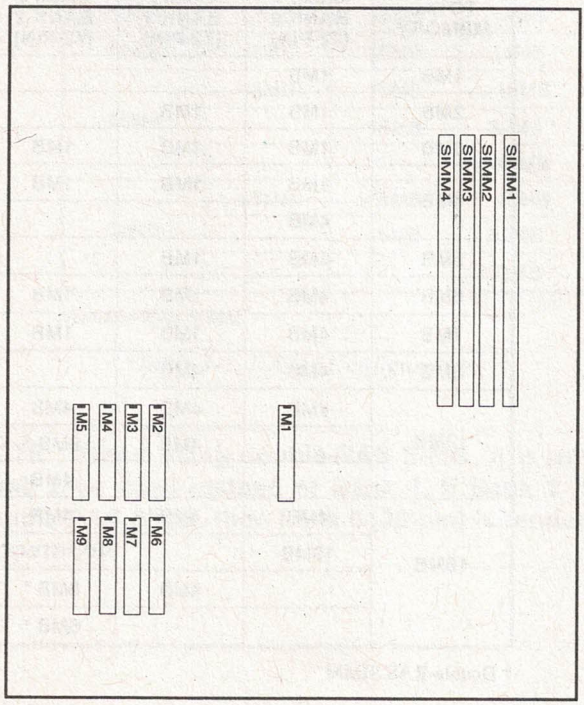


Figure 3-1. Cache and Memory Locations

Installing DRAM

SIMM Banks

The 486-GIO-VT2 can accommodate on-board memory from 1 to 64MB using SIMMs (Single-In-Line Memory Modules). The mainboard has four memory banks — Bank 0, 1, 2, 3. Each bank can accept either a 256KB, 1MB, 4MB, or 16MB SIMM in each socket.

DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table:

TOTAL MEMORY	SIMM 1 BANK 0 (72-PIN)	SIMM 2 BANK 1 (72-PIN)	SIMM 3 BANK 2 (72-PIN)	SIMM 4 BANK 3 (72-PIN)
1MB	1MB			
2MB	1MB	1MB		
3MB	1MB	1MB	1MB	
4MB	1MB	1MB	1MB	1MB
	4MB			
5MB	4MB	1MB		
6MB	4MB	1MB	1MB	
7MB	4MB	1MB	1MB	1MB
8MB	4MB	4MB		
12MB	4MB	4MB	4MB	
		4MB	8MB *	
			4MB	8MB *
16MB	4MB	4MB	4MB	4MB
	16MB			
		4MB	8MB *	4MB
			8MB *	8MB *

* Double-RAS SIMM

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	SIMM 1 BANK 0 (72-PIN)	SIMM 2 BANK 1 (72-PIN)	SIMM 3 BANK 2 (72-PIN)	SIMM 4 BANK 3 (72-PIN)
17MB	16MB	1MB		
18MB	16MB	1MB	1MB	
19MB	16MB	1MB	1MB	1MB
20MB	16MB	4MB		
21MB	16MB	4MB	1MB	
22MB	16MB	4MB	1MB	1MB
24MB	16MB	4MB	4MB	
28MB	16MB	4MB	4MB	4MB
32MB	16MB	16MB		
			32MB *	
33MB	16MB	16MB	1MB	
34MB	16MB	16MB	1MB	1MB
36MB	16MB	16MB	4MB	
40MB	16MB	16MB	4MB	4MB
48MB	16MB	16MB	16MB	
		16MB	32MB *	
			16MB	32MB *
64MB	16MB	16MB	16MB	16MB
		16MB	32MB *	16MB
			32MB *	32MB *

*Double-RAS SIMM

Table 3-1. DARM Configurations

→ **NOTE : When using double-RAS SIMM, it is advised that Bank 2 be used instead of Bank 1. If Bank 1 contains a double-RAS SIMM, then Bank 0 (30-pin) is rendered inoperative.**

Installation Instructions

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.**

1. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.
2. Insert the SIMM edge connector at a 90-degree angle onto the socket.

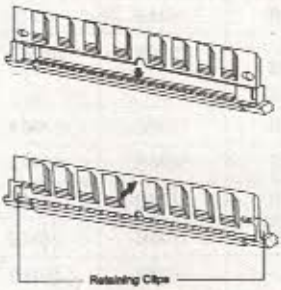


Figure 3-2. Installing SIMMs

3. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.

Cache Memory

The 486-GIO-VT2 can accept cache memory of 64, 128 or 256KB.

→ **NOTE : Be sure to use the correct chips for the amount of cache memory you want to add. You must install both the correct Cache and Tag SRAM.**
Alter RAM type is always the same as Tag RAM.

Installing Cache Memory

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the beginning of this manual.**

If you do not have the confidence to make the installation, better consult a service technician for assistance.

1. Locate the cache memory on the mainboard. See Figure 3-1 again.
2. Be guided by the Cache SRAM settings depending on your desired SRAM configuration.

Correct orientation of the chips is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

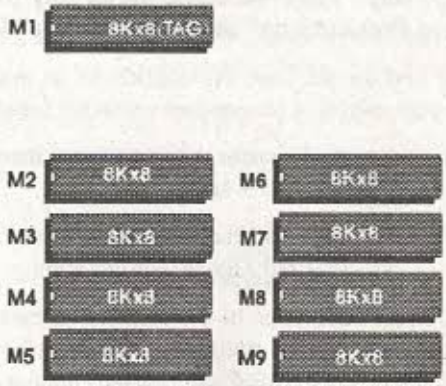
3. Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.
4. Carefully apply enough pressure to partially seat the chip into the socket.

Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.

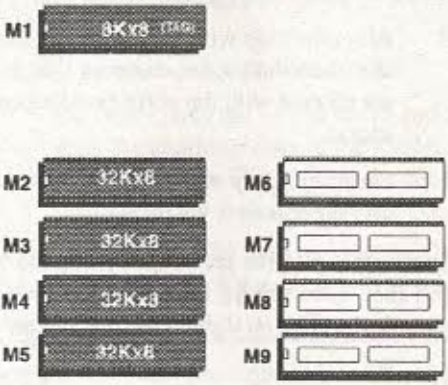
5. Press the chip completely into the socket so that the pins are properly seated.

Cache SRAM Specifications and Settings

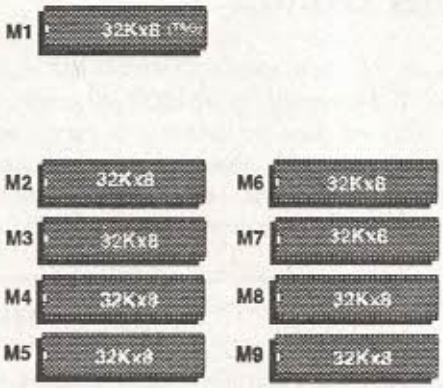
64K Cache SRAM



128K Cache SRAM



256K Cache SRAM



The cache size is jumper selectable. M1 - M4 are assigned as Bank 0 and M6 - M9 are assigned as Bank 1.

	64K	128K	256K
Bank 0	8K x 8	32K x 8	32K x 8
Bank 1	8K x 8	Empty	32K x 8
Tag RAM (M5)	8K x 8	8K x 8	32K x 8
JS1 (Jumper)	1-2	1-2	2-3
JS2 (Jumper)	1-2	2-3	2-3
JS3 (Jumper)	1-2	2-3	1-2

Table 3-2. Cache Configuration Size

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Award BIOS Setup

The 486-GIO-VT2 comes with the Award BIOS chip that contains the ROM Setup information of your system. This chip serves as an interface between the CPU and the rest of the mainboard's components. This chapter explains the information contained in the Setup program and tells you how to modify the settings according to your system configuration.

System Setup

A Setup program, built into the system BIOS, is stored in the CMOS RAM that allows the configuration settings to be changed. This program is executed when:

1. User changes system configuration.
2. User changes system backup battery.
3. System detects a configuration error and asks the user to run the Setup program.

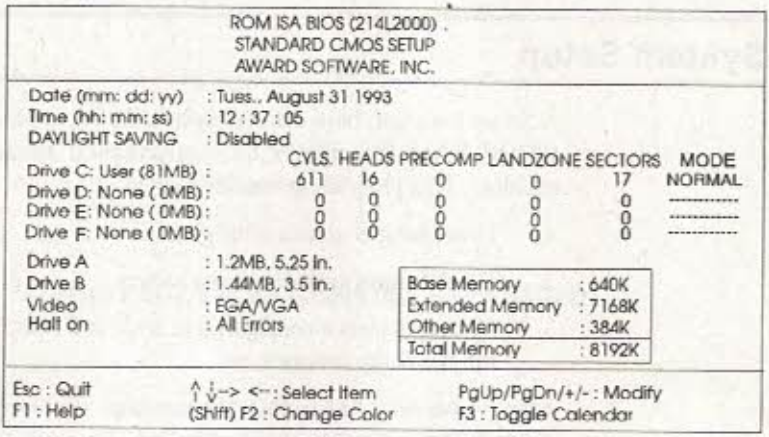
After power-on RAM testing, the message "**Press <DEL> to enter Setup**" appears. After pressing the afore mentioned keys, the following screen appears:

ROM ISA BIOS (214L2000) CMOS SETUP UTILITY AWARD SOFTWARE, INC.	
STANDARD CMOS SETUP	SUPERVISOR PASSWORD
BIOS FEATURES SETUP	USER PASSWORD
CHIPSET FEATURES SETUP	IDE HDD AUTO DETECTION
POWER MANAGEMENT SETUP	SAVE AND EXIT SETUP
LOAD BIOS DEFAULTS	EXIT WITHOUT SAVE
LOAD SETUP DEFAULTS	
Esc : Quit	↑ ↓ –> <– : Select Item
F10 : Save and Exit Setup	(Shift) F2 : Change Color
Time, Date, Hard Disk Type	

Use the arrow keys to select and press **<Enter>** to run the selected program.

Standard CMOS Setup

The Standard CMOS Setup has several items for setting. Each item may have one or more option settings. Use the arrow keys to highlight the item and then use the **<PgUp>**, or **<PgDn>** keys to select the value you want in each item.



The Standard CMOS Setup screen is displayed above. System BIOS automatically detects memory size, thus no changes are necessary. Press "**F3**" function key to show the calendar.

Daylight Saving

When enabled, this field allows user to set the clock one hour in advance. When disabled, it subtracts one hour when standard time begins. After the changes are made, press **<Esc>** to return to main menu.

BIOS Features Setup

ROM ISA BIOS (214L2000)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

Virus Warning	: Enabled	System BIOS Shadow	: Enabled
CPU Internal Cache	: Enabled	Video BIOS Shadow	: Enabled
External Cache	: Enabled	C8000-CBFFF Shadow	: Disabled
Quick Power On Self Test	: Disabled	CC000-CFFFF Shadow	: Disabled
Boot Sequence	: A, C	D0000-D3FFF Shadow	: Disabled
Swap Floppy Drive	: Disabled	D4000-D7FFF Shadow	: Disabled
Boot Up Floppy Seek	: Enabled	D8000-DBFFF Shadow	: Disabled
Boot Up NumLock Status	: On	DC000-DFFFF Shadow	: Disabled
Boot Up System Speed	: High		
IDE HDD Block Mode	: Disabled		
Fast A20 Port 92H	: Enabled		
Memory Parity Check	: Disabled		
Typematic Rate Setting	: Disabled		
Typematic Rate (Chars/Sec)	: 6		
Typematic Delay (Msec)	: 250		
Security Option	: Setup		

Esc : Quit	↑↓–> <– : Select Item
F1 : Help	PgUp/PgDn/+/- : Modify
F5 : Old Values	(Shift) F2 : Change Color
F6 : Load BIOS Defaults	
F7 : Load Setup Defaults	

Chipset Features Setup

ROM ISA BIOS (214L2000)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

Decoupled Refresh	: Enabled
Relocate 256K/384K	: Disabled
Video BIOS Cacheable	: Enabled
System BIOS Cacheable	: Enabled
External Cache Scheme	: Write Back
Combine Alter & Tag Bits	: Disabled
CHRDY for ISA Master	: Disabled
Memory Hole At 15MB Addr.	: Disabled
Cache Timing Control	: Fast
DRAM Timing Control	: Fast
Fast DRAM	: Enabled
Burst Write	: Disabled
CPU Write Back Cache	: Disabled
P24T Cache Replace BLAST	: Disabled

Esc : Quit	↑↓–> <– : Select Item
F1 : Help	PgUp/PgDn/+/- : Modify
F5 : Old Values	(Shift) F2 : Change Color
F6 : Load BIOS Defaults	
F7 : Load Setup Defaults	

Moving around the BIOS and Chipset Features Setup programs shown works the same way as moving around the Standard CMOS Setup program. Users are not encouraged to run the BIOS and Chipset Features Setup programs. Your system should have been fine-tuned before shipping. Improper Setup may cause the system to fail, consult your dealer before making any changes.

Power Management Setup

Many PC users never turn their computers off because of delays in reloading their operating system or applications. An energy efficient mainboard combats such energy waste by using System Management Mode (SMM), static technology, and processor clock control to conserve energy.

During periods of system inactivity, the system automatically initiates a "Sleep" mode, reducing both system and monitor power. Power Management Setup allows you to blank out the VGA display, slowdown or turn off CPU speed, and turn off HDD spindle motor during a set period of time.

Regular CPU

ROM ISA BIOS (214L2000)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

Power Management	: Disabled
Doze Timer	: 2 min.
Sleep Timer	: 8 min.
Sleep Mode	: Sleep
HDD Power Management	: Disabled
VGA Activity Wakeup	: Enabled
RTC Alarm Wakeup	: Disabled
INTR Enabled PMI	: Disabled
IO Activity	: Disabled

Esc : Quit
F1 : Help
F5 : Old Values
F6 : Load BIOS Defaults
F7 : Load Setup Defaults

↑ ↓ -> <- : Select Item
PgUp/PgDn/+/- : Modify
(Shift) F2 : Change Color

FULL-ON CPU SPEED	DOZE MODE CPU SPEED	SLEEP MODE CPU SPEED
50 MHz	16 MHz	16 MHz
40 MHz	20 MHz	20 MHz
33 MHz	8 MHz	8 MHz
25 MHz		

Table 4-1. Regular CPU Slowdown Speed

→ **NOTE : If your mainboard supports four sets of hard disk drives, the Regular CPU Sleep mode is not available.**

ITEM	FUNCTION
Power Management	Choices are "Enabled" and "Disabled". Allows you to use the Power Management features when "Enabled".
VGA Activity Wakeup	Choices are "Enabled" and "Disabled". When "Enabled", it allows the Doze Timer to start counting when no activity is detected on the VGA display. Otherwise, when "Disabled", Doze Timer will start counting immediately even if there is activity on the VGA display.
Doze Timer	Choices are "1, 4, 16, and 32min." afterwhich, CPU speed will slowdown and enter "Doze Mode" assuming there is no operation during the selected period (refer to the previous table for the corresponding CPU slowdown speed). When VGA Activity Wakeup is set "Disabled", always divide the Doze Timer value by two (e.g., Doze Timer : 4min., CPU speed will slowdown after 2min.). Normal CPU speed is resumed upon pressing any key.
Sleep Mode	Choices are "Sleep" and "Disabled". When set at "Disabled", it renders the Sleep Timer inoperative.
Sleep Timer *	Choices are "2, 8, 16, and 32min." afterwhich VGA display will blank out and enter "Sleep Mode" assuming there is no operation during the selected period. (E.g., If Doze Timer = 1min. and Sleep Timer = 8min., then VGA display blanks out after 9min.) CPU speed is the same as that under "Doze Mode". Normal VGA display is resumed upon pressing any key.
HDD Power Management	Choices are "Enabled" and "Disabled". When "Enabled", HDD spindle motor will turn off after a certain time period. This feature would depend on the HDD type used.

* When using a Green Power Supply, VGA display not only blanks out but power to display monitor would be cut thereby, conserving more electricity. Insert two pin connector wire into Connector J1 of the mainboard.

Table 4-2. Power Management Setup Screen Features

SMM CPU

ROM ISA BIOS (214L2000)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

Power Management	: Disabled
Doze Timer	: 2 min.
Doze Mode Speed	: CLKIN/4
Sleep Timer	: 8 min.
Sleep Mode	: Suspend
HDD Power Management	: Disabled
VGA Activity Wakeup	: Enabled
RTC Alarm Wakeup	: Disabled
INTR Enabled PMI	: Disabled
IO Activity	: Disabled

Esc : Quit
F1 : Help
F5 : Old Values
F6 : Load BIOS Defaults
F7 : Load Setup Defaults

↑ ↓ -> <- : Select Item
PgUp/PgDn/+/- : Modify
(Shift) F2 : Change Color

FULL-ON CPU SPEED	DOZE MODE CPU SPEED	SLEEP MODE CPU SPEED	SUSPEND MODE CPU SPEED
33 MHz	8 MHz	8 MHz	0 MHz
25 MHz	12.5 MHz	12.5 MHz	0 MHz

Table 4-3. SMM CPU Slowdown Speed

Same features as that of regular CPUs Power Management Setup screen except for an additional "Doze Mode Speed" which allows you the benefit of setting the CPU slowdown speed (e.g., CLKIN/4 = normal SMM CPU speed divided by four). Choices are CLKIN/2 and CLKIN/4. SMM CPUs include a "Suspend" feature in Sleep Mode which stops the CPU clock completely (0MHz) after the CPU remains non-operational during the selected period. Follow the same procedure in setting Sleep Timer for regular CPUs (see Table 4-2).

→ **NOTE : Some Operating Systems may not maintain the correct computer clock time during "Suspend Mode".**

Load BIOS Default

BIOS defaults contain the most appropriate values of the system parameters that allow minimum system performance. The OEM manufacturer may change the defaults through MODBIN before the binary image is programmed into the ROM.

Load Setup Default

Selecting this field loads the factory defaults for BIOS and Chipset Features which the system automatically detects.

Password Setting

When you select this function, you can create a password. Type your password up to eight characters and press **<Enter>**. You will be asked to confirm the password. Type the password again and press **<Enter>**. You may also press **<Esc>** to abort the selection and not enter a password. To disable password, press **<Enter>** when you are prompted to enter password. A message appears, confirming the password is disabled. When the password is disabled, the system boots and you can enter Setup freely.

SUPERVISOR & USER Password

X : The selection in Award Setup screen "BIOS Features Setup", item "Secturity Option".

Y : The action that BIOS will monitor while Dual Password are set to enable.

Y \ X	Setup	System
Entry Setup	Supervior Password	Supervior password
Before Booting	No Password be Requested	Supervior or User's password

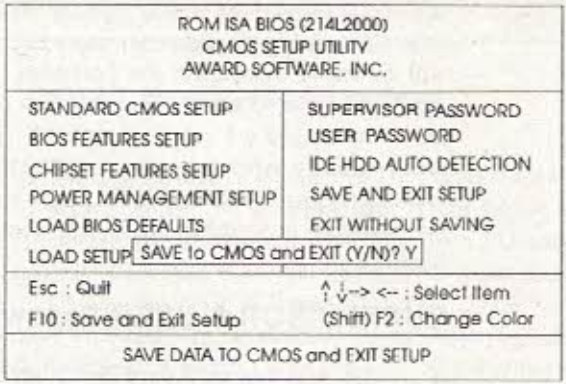
Clear Password

If you forget your password, turn off the system power first and remove the system unit cover. Locate Jumper J7 and cap it. Turn the system power back on and screen will display the message below:

PASSWORD IS SET DISABLED
PLEASE REMOVE JUMPER (J7) BEFORE
SETTING UP NEW PASSWORD

This message indicates that the password is disabled. Remove Jumper J7 and enter CMOS Setup to set new password.

Exiting Setup



After you have made changes under Setup, press **<Esc>** to return to the main menu. Move cursor to "**Save and Exit Setup**" or press "**F10**" and then press "**Y**" to change the CMOS Setup. If you did not change anything, press **<Esc>** again or move cursor to "**Exit Without Saving**" and press "**Y**" to retain the Setup settings.

→ **NOTE : Default values of the various Setup items on this chapter may not necessarily be the same ones shown on your screen.**

Hard Disk Specifications

This appendix contains some technical information about the different IDE hard disks drives which have be installed with your 486-GIO-VT2 mainboard.

CONNER

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
CP-30124	120MB	895	5	55
CP-30174	170MB	903	8	46
CFS-210A	213MB	685	16	38
CP-30344	340MB	904	16	46
CFN-340A	340MB	667	16	63
CFA-270A	270MB	524	16	63
CFA-540A	540MB	1048	16	63

MAXTOR

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
7120A	120MB	1023	14	17
7131A	131MB	1002	8	32
7213A	213MB	683	16	38
7245A	245MB	967	16	31
7345A	345MB	790	15	57

QUANTUM

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
LPS-120AT	120MB	901	5	53
LPS-240AT	240MB	723	13	51
LPS-270AT	270MB	944	14	40
LPS-340AT	340MB	1011	15	44
LPS-540AT	540MB	1120	16	59
ELS-127AT	127MB	919	16	17
ELS-170AT	170MB	1011	15	22

SEAGATE

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
ST3144A	130MB	1001	15	17
ST3283A	240MB	978	14	35

WESTERN DIGITAL

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
AC2120	120MB	872	8	35
AC2170	170MB	1010	6	55
AC2200	212MB	989	12	35
AC2250	256MB	1010	9	55
AC2340	340MB	1010	12	55

PRIAM

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
S19	152MB	1024	15	17

IDE Controller Device Driver and Utility (Optional)

→ **NOTE : Device drivers for VIA VT83C461 Local IDE disk controller are copied in the supplied floppy. Please refer to the README file for the installation of the drivers.**

The following device drivers for DOS, Windows and NetWare are found in the drivers diskette (For Promise PDC20230 Local IDE Driver install) :

VLIDE.EXE (Version 1.10) is the installation utility.
VLIDE.SYS (Version 2.20) is the driver for DOS.
VLIDE.386 (Version 2.20) is the driver for Microsoft Windows 3.1.
VLIDE.ADD (version 2.10) is the driver for IBM OS/2 2.0 and 2.1.
VLIDE310.DSK (version 2.20) is the driver for Netware 386 3.10
VLIDE311.DSK (version 2.20) is the driver for Netware 386 3.11.
VLIDE401.DSK (version 2.30) is the driver for Netware 386 4.01.
VLIDE401.DDI is the installation information file for Netware 386 4.01.
VLIDENT.SYS (version 2.10) is the driver for Microsoft Windows NT 3.1.
NTINS.BAT is the installation batch file for Windows NT 3.1.
NTUNINS.BAT is the removal batch file for Windows NT 3.1.
PTIREG.EXE is the internal utility for Windows NT 3.1.
PTIUREG.EXE is the internal utility for Windows NT 3.1.
CITURBO.EXE is the set mode utility for Windows NT 3.1.

→ **NOTE : You should have made backup copies of the original diskettes and should be using the backup ones.**

These device drivers enhance the performance by 32-bit VL-Bus I/O and read/write multiple commands. Two operating modes, *Turbo(T)* and *Fast(F)*, are supported by these device drivers. In *Turbo(T)* mode (default), the system will use 32-bit VL-Bus I/O and the read/write multiple commands supported by most new IDE drives. The *Fast(F)* operation uses the 32-bit VL-Bus I/O. However, it does not use the read/write multiple commands.

→ **NOTE : Not all IDE drives support the read/write multiple commands. Usually, you may set your VL-IDE controller to run under the Turbo mode. If your system is installed with DOS, when your system is brought up and the DOS driver VLIDE.SYS is well installed, the driver will automatically issue an Identify Drive command to check if the attached IDE drive(s) support the read/write multiple commands. In the case your drive(s) does not support the read/write multiple commands, the VL-IDE disk controller will automatically be forced to run under the Fast mode.**

The device drivers for DOS, Windows, Windows NT and NetWare all have an internal table that contains the optimal speed setting parameters for the most popular IDE drives. When the system is brought up, appropriate speed setting parameters in the table are used to program the VL-IDE controller automatically.

VLIDE.EXE

The VLIDE.EXE provides the following functions:

1. To analyze your hard drive:
   When executing the VLIDE.EXE, this utility will identify the hard drives attached on the VL-IDE controller. If the drive(s) can be found in the table, the utility will select the parameter in the device drivers. If not, the utility will perform a real speed test to determine the optimal parameters, and reconfigure the device drivers for DOS, Windows and NetWare automatically.

2. To install the device drivers for DOS and Windows. VLIDE.EXE provides a friendly interface and procedure to install the device drivers for DOS and Windows.

→ **NOTE : Refer to the README file on the drivers diskette for related installation procedures and news of more recent updates.**