386 - 25/33M

ASIC
Mainbaord
User's Manual

DOC. NO. : 10539 REV. : A
DATE : January, 1991

Notice

The information contained in this document is subject to change without notice.

Warning

IMPORTANT

POWER SUPPLIES for 386 COMPUTERS

As with all computer products, a clean steady power source is necessary to get reliable performance from the system.

With the high clock speeds of the CPU (running either 16Mhz or 20MHz and above) the quality of the Power Supply becomes even more important. *Most Power Supplies in the market meet the standards required by the CPU, however some have been found to be out of specifications.* To be certain of the highest performance by your system, be sure your Power Supply provides a **voltage range of 5.25 volts maximum to 4.95 volts minimum.**

In areas with noisy power transmission, we suggest the use of a line noise filter between the power and the computer.

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Section I
Introduction

INTRODUCTION

1. Introduction

The 386-25/33M ASIC Cache System Motherboard

The 386-25/33M ASIC Cache system board is a high performance system board utilizing Micronics' ASIC chip array that offers outstanding features and performance for building advanced personal computers or workstations. **It contains an Intel 80386 microprocessor, an Intel 82385 cache controller, 32-bit access to data, and an option to accommodate the Intel 80387 coprocessor as well as the Weitek 3167 numeric coprocessor.**

The High-Speed Memory

The 386-25/33M ASIC Cache system board is capable of accomodating one or four megabytes on board and will accept a companion high-speed memory board which accomodates up to a total of 16 megabytes of memory using SIMMs.

2. Features

The 386-25/33M ASIC Cache comes with the following features:

- Intel 80386 microprocessor: 32-bit architecture
- Intel 82385 Cache Controller for fast caching
- Direct Map or Two-way set associative cache option with 8Kx8 -20 ns SRAM for 33 MHz units, and 8Kx8 -35 ns SRAM for 25/20 MHz units

- Socket for Intel 80387 math coprocessor or Weitek 3167 math coprocessor
- Three Speed Selection by special utility software (6, 8, and full speed)
- System BIOS and EGA BIOS relocatable to 32-bit high speed RAM for enhanced execution
- One 32-bit expansion slot, eight 16-bit expansion slots
- User-friendly BIOS
- Real time clock
- Turbo Switch
- One or four megabytes of memory on the system board expandable to 16MB with the use of the M710 companion memory expansion board
- MICEMM (Lotus*/Intel*/Microsoft* Expanded Memory) software included

*Lotus is trademark of Lotus Dev. Corp; Intel is a trademark of Intel Corp.; Microsoft is a trademark of Microsoft Corp.

3. Performance of the 386-25/33M ASIC Cache board

System Speed	20 MHz	25 MHz	33 MHz
Landmark Speed Rating*	33.4 MHz	43.5 MHz	53.7 MHz
Power Meter MIPS**	4.860	6.00	7.583

* Landmark ver. 1.10; ** Power Meter Ver. 1.3

Section II
Configuration

CONFIGURATION

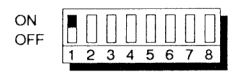
1. Preliminary

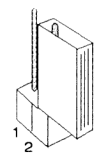
After unpacking the system motherboard, place it on a raised surface and carefully inspect the board for any damage that might have occured during shipment. *Ground the board and exercise extreme care to prevent damage to the board from static electricity.* Examine all integrated circuits, particularly the *BIOS, CPU and keyboard controller chip* to ensure that they are firmly seated.

Switch and Jumpers

The 386-25/33M ASIC Cache system board has switch and various jumpers, which are set before bootup to configure various functions of the system. One switch or dip switch block usually includes several positions; each position may be set to ON or OFF to convey certain information to the computer. A jumper is two or more gold pins which may or may not be covered by a plastic connector plug.

Figure 1: Switch and jumper





The 386-25/33M ASIC Cache system board was designed to be flexible by using one switch and jumpers on the motherboard to change system configuration when enhancement or special needs are required.

The following options can be selected by a switch or jumper:

- Math coprocessor
- ROM size
- Relocation of EGA and System BIOS
- Monitor type
- Activation of Cache
- Reset Connection
- Keyboard lock
- Bus Speed Selection
- Turbo Switch

Setting board options involves placing the jumpers on the designated pins as shown in Figure 4 or sometimes removing a jumper altogether.

2. Configuring DIP Switch SW1

Table 1 - Motherboard DIP switch settings (SW1)

Switch	Configuration	Setting	Switch Position
1	Reserved	On	*Default*
2	80387 Coprocessor installed	On	
	80387 Coprocessor not installed	Off	*Default*
3	System Bus Speed Select	See Table 2	
4	BIOS Relocate	On	
	BIOS Not Relocate	Off	*Default*
5	Reserved	Off	*Default*

- Continued -

Switch	Configuration	Setting	Switch Position
6	CGA/EGA/VGA Video board	On	*Default*
	MONO Video card	Off	
7	Cache activated	On	*Default*
	Cache not activated	Off	
8	System Bus Speed Select	See Table 2	

Table 2 - System Bus Speed Select

Bus Speed	SW1-3	SW1-8	System Recommended
System Speed/4	Off	Off	33 MHz
System Speed/3	On	Off	25 MHz
System Speed/2	On	On	20 MHz
Reserved	Off	On	

3. Configuring the Jumpers

Table 3 - Chassis Jumper Wire Connections

Jumper	Function	Pin Assignment
J7	Keyboard Connector	See Figure 2
J9	External 6V Battery	1 Battery Positive 2 N/C* 3 Ground 4 Ground
J3&J4	Power Supply Connectors	See Figure 3
J5	Keylock and Power LED	1 Power LED 2 N/C* 3 Ground 4 Keyboard Lock 5 Ground
J8	Speaker	1 Speaker 2 N/C* 3 Ground 4 +5 VDC

- Continued -

Jumper	Function	Pin Assignment
J6	External Keyboard Connector	1 Keyboard Clock 2 Keyboard Data 3 N/C* 4 Ground 5 +5 VDC
W1	Reset	1 Reset Signal 2 Ground
W4	Turbo Light Connection	1 Turbo light signal 2 Ground
W5	Turbo Switch Connection**	1 Turbo Signal 2 Ground

* No connection

** Run the SETSYS utility software to slow down the system speed. Use the TURBO SWITCH to bring the system speed back to the full non-cache speed

Figure 2 : Keyboard Connector Pin Assignment

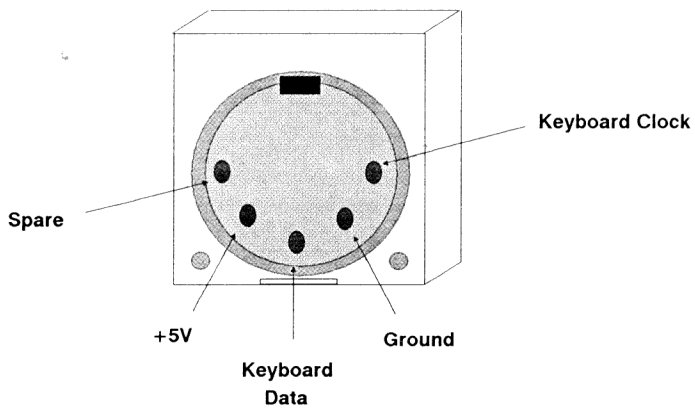


Figure 3 : Power Supply Connector Pin Assignment

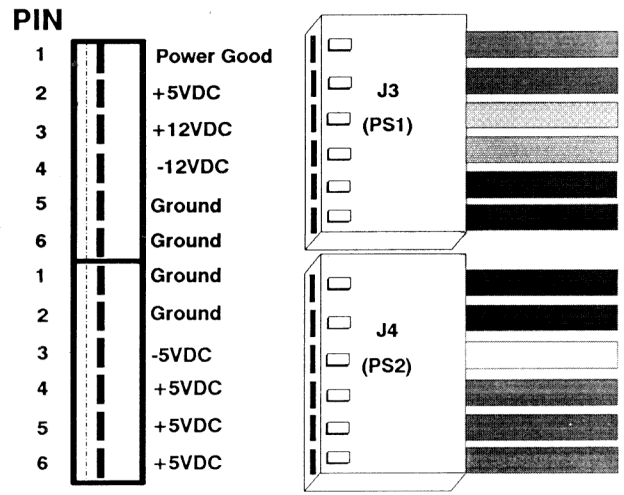


Table 4 - Cache Operation

Jumper	Pin Connection	Cache Operation
W14	1-2 No Connection	Direct Map Two-way Set Associative
W15	1-2 2-3	Direct Map Two-way Set Associative

See Section III part 6 for more installation details

Table 5 - Non-cacheable Region Selection

Jumper	Pin Connection	Non-cacheable Region
W9	1-2 No Connection	E00000 to EFFFFF D00000 to DFFFFF

See Section III part 2 for more details.

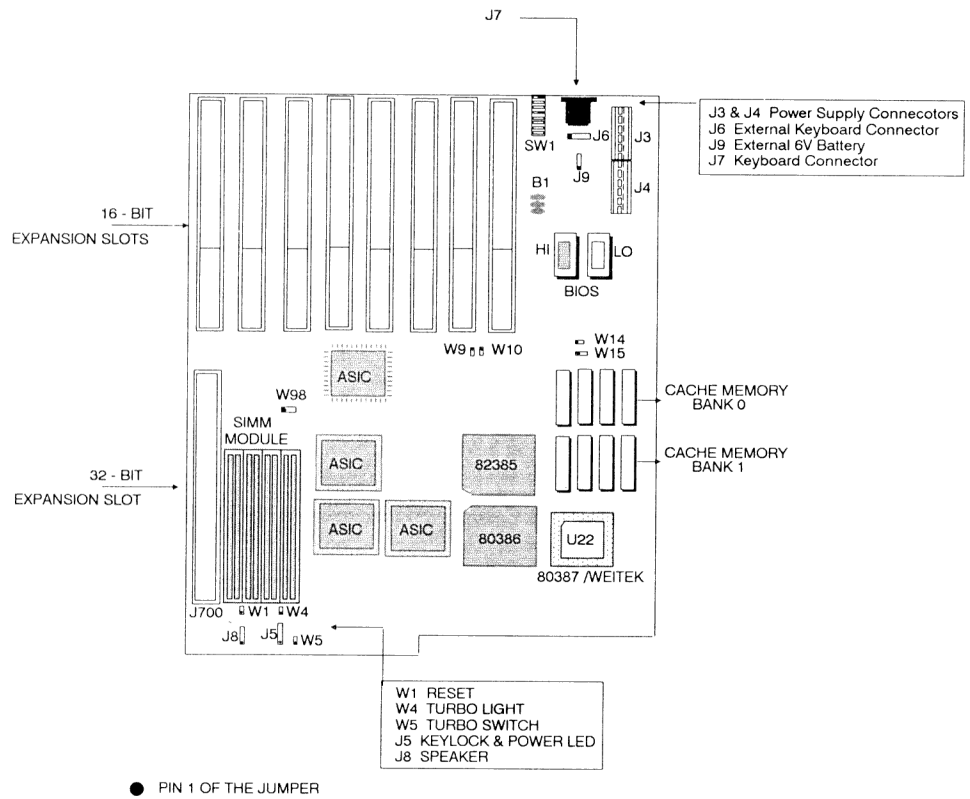
Table 6 - System Board Functional Jumpers

Jumper	Pin Connection	Configuration
W30	Pin 1-2	Video BIOS Cache
	No Shunt	Video BIOS not Cache
W98	Pin 1-2	DRAM 256Kx9
	Pin 2-3	DRAM 1Mx9
W10	No Shunt	640K Base Memory
	Pin 1-2	512K Base Memory

4. Layout of the 386-25/33M ASIC Cache System Board

Figure 4:

Switch and Jumper Positions on the 80386 ASIC Cache System Board



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Section III
Installation

INSTALLATION

Before you begin to install the 386-25/33M ASIC Cache board, you should have a large clear space on which to work. Manufacturer recommends to have the following:

- Small Phillips and flat blade screwdrivers
- A small pair of scissors or diagonal cutter
- Tweezers or small needle-nose pliers
- A ballpoint pen
- A tray to hold loose screws
- A grounded power outlet (3-prong)

1. Required Parts

The following parts is necessary to build an advanced system based on the 386-25/33M ASIC Cache system board:

- Chassis with standard hardware. The 386-25/33M ASIC Cache board measures 8.5 inches by 13.3 inches (215.9 mm by 337.8 mm), so a chassis similar in size to the one used with an IBM AT is appropriate. The mounting holes on the 386-25/33M ASIC Cache system board are the same and are in exact locations as on the IBM AT system board.
- Standard AT 220W power supply that is capable of providing continuous power within a 4.95 to 5.25 volt range. A power line filter may be added for areas with noisy transmission.

- 6V battery to sustain the clock/calendar chip. If a rechargeable battery is already installed at location B1, the external 6V battery is not necessary.
- 8 ohm speaker to provide sound capabilities
- One floppy drive (360K or 1.2M)
- Hard disk drive
- Combination hard disk drive and floppy drive controller card
- Video card (Monochrome, CGA, EGA, and VGA)
- Flat ribbon cables between the HD/floppy controller and the drives
- Serial/Parallel card
- AT-compatible keyboard (84 or 101 Keyboard)
- Monitor

WARNING: Due to high speed of the microprocessor, a chassis with good ventilation is recommended.

2. Optional Parts

- Intel 80387 math coprocessor and/or Weitek 3167 coprocessor
- Modem/FAX boards
- Tape back up drive
- Intelligent Serial Card

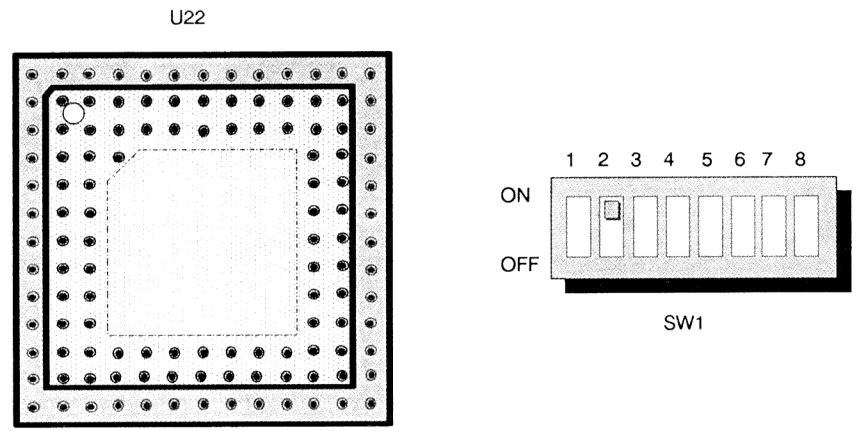
Interfacing with Intelligent Serial Card

Most of the intelligent serial cards have an on board buffer, the buffer starting location is usually switch selectable. The starting adddress of the intelligent serial card should be set at a non-cacheable region. The non-cacheable region on the system board is selectable by jumper W9. See Section VI part 6 for more technical information.

3. Installing the Intel 80387 Math Coprocessor

An 80387 math coprocessor chip may be inserted in the center of the 121 pin PGA Extended Math Coprocessor (EMC) socket at location U22. This socket can contain the Intel 80387 chip, the Weitek 3167 chip, or the Weitek 3167 math coprocessor adapter board. Refer to figure 5 for proper installation of the 80387 coprocessor.

Figure 5 : Installing the 80387 Coprocessor



NOTE:
Set switch SW1-2 to ON to indicate that an Intel 80387 math coprocessor is present. The factory setting of SW1-2 is OFF indicating that a 80387 math coprocessor is not present.

4. Weitek Coprocessor

The 386-25/33M ASIC Cache system board is also designed to accommodate the Weitek 3167 math coprocessor, as well as the Weitek 3167 math coprocessor daughter board.

The Weitek WTL 3167 coprocessor is a single chip which plugs into the 121-pin pin grid array socket at U22. It offers 5.6 single-precision megawhetstones. When the Weitek 3167 coprocessor chip is used, the system will not be able to support

software or compilers based on the Intel 80387. *A small Weitek WTL 3167 daughter board is available for users who wish to make use of both the Intel 80387, and the Weitek 3167.* This daughter board plugs into the 121-pin PGA socket while the Intel 80387 plugs into the center of the 121-pin socket on the Weitek 3167 daughter board.

Set switch SW1-2 on the system board to OFF if only a Weitek WTL 3167 coprocessor is present.

5. Installing Memory

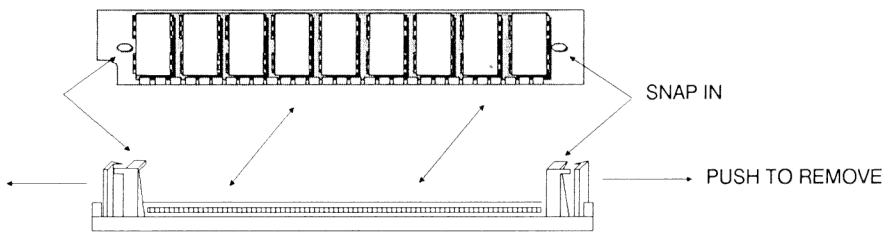
The 386-25/33M ASIC Cache system board can accomodate one or four megabytes of memory on board and has a 32-bit slot which will accept an M710 high speed memory board to achieve a total of 16 megabytes of memory.

NOTE:

Extreme care must be taken when removing or installing SIMM into the socket.

- Insert the SIMM into the socket as shown on figure 6. The component side of the SIMM must face the CPU

Figure 6 : Installing SIMM Memory

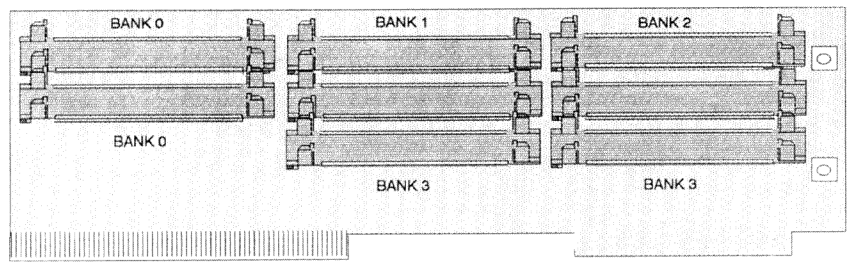


- Gently press the SIMM toward the 32-bit memory connector (J700) until the module snaps against the edge of the socket.
- To remove the module, use a small screw-driver to release the latches at the two holes in the sides of the SIMM, and gently lift the module.

5.1 M710 Memory Board

The M710 memory board is capable of supporting a minimum of 1 megabyte of memory up to a total of 16 megabytes using 256Kx9 - 80 ns SIMM or 1Mx9 - 80 ns SIMM. Refer to Figure 7 for the layout of the M710 memory board.

Figure 7 : Lay Out of the M710 Memory Board



The M710 memory expansion board plugs into slot J700 on the system board. This memory expansion board can be used with or without memory installed on the system board. Refer to table 7 for jumper setting, and table 8 for memory configuration.

Table 7 - Jumper Settings for the M710 Memory Board

Jumper	Position	Configuration
W1	Pin 1-2 Pin 2-3	1Mx9 SIMM in Bank 0 256Kx9 SIMM in Bank 0
W2	Pin 1-2 Pin 2-3	1Mx9 SIMM in Bank 1 256Kx9 SIMM in Bank 1
W3	Pin 1-2	1Mx9 SIMM in Bank 2
W4	Pin 1-2	1Mx9 SIMM in Bank 3.

Table 8 M710 Memory Board Configurations

Memory Size	Sytem Board Bank 0	M710 Bank 0	Bank 1	Bank 2	Bank 3
1 MB	256Kx9	-----	-----	-----	-----
1 MB	-----	256Kx9	-----	-----	-----
2 MB	256Kx9	-----	256Kx9	-----	-----
2 MB	-----	256Kx9	256Kx9	-----	-----
4 MB	1Mx9	-----	-----	-----	-----
4 MB	-----	1Mx9	-----	-----	-----
5 MB	256Kx9	-----	1Mx9	-----	-----
5 MB	-----	256Kx9	1Mx9	-----	-----
6 MB	256Kx9	-----	256Kx9	1Mx9	-----
6 MB	-----	256Kx9	256Kx9	1Mx9	-----

- Continued -

Memory Size	Sytem Board Bank 0	M710 Bank 0	Bank 1	Bank 2	Bank 3
8 MB	1Mx9	-----	1Mx9	-----	-----
8 MB	-----	1Mx9	1Mx9	-----	-----
9 MB	256Kx9	-----	1Mx9	1Mx9	-----
9 MB	-----	256Kx9	1Mx9	1Mx9	-----
10 MB	256Kx9	-----	256Kx9	1Mx9	1Mx9
10 MB	-----	256Kx9	256Kx9	1Mx9	1Mx9
12 MB	1Mx9	-----	1Mx9	1Mx9	-----
12 MB	-----	1Mx9	1Mx9	1Mx9	-----
13 MB	256Kx9	-----	1Mx9	1Mx9	1Mx9
13 MB	-----	256Kx9	1Mx9	1Mx9	1Mx9
16 MB	1Mx9	-----	1Mx9	1Mx9	1Mx9
16 MB	-----	1Mx9	1Mx9	1Mx9	1Mx9

* Static Column DRAM and Page Mode DRAM

WARNING: Switch settings on the memory board must correspond to the above table. Inaccurate switch settings may affect proper function of the system.

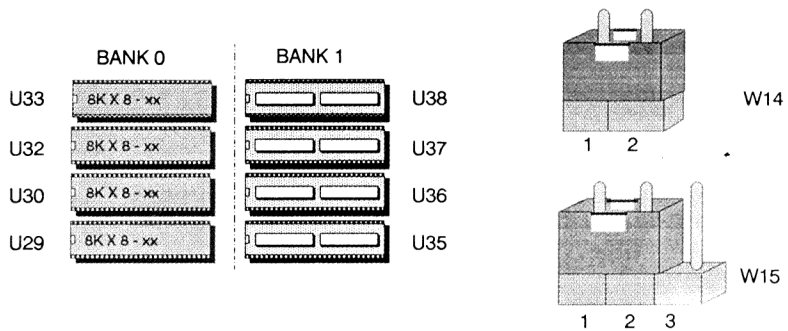
6. Installing the Cache Memory

The 386-25/33M ASIC Cache system board provides the options of 32K Direct Mapped Cache or 32K Two-way Set Associative Cache. See section VI part 3 for more technical information.

32K Bytes Direct Mapped Cache

The 32 Kbytes Direct Mapped Cache option is achieved by installing four 8Kx8-SRAMs in bank 0 at U29, U30, U32, U33. 35ns SRAMs are used for 20 and 25 MHz system boards, while 20 ns SRAMs are used for 33 MHz system boards. Install jumper block between pin 1 & 2 of jumper W14 and W15. Refer to figure 8 below.

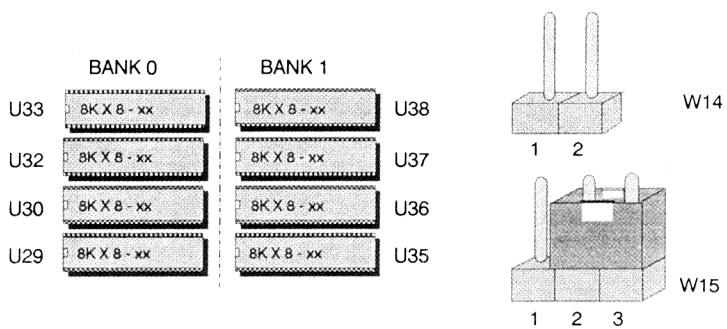
Figure 8 : 32 Kbytes Direct Map Cache



32K Bytes Two-way Set Associative Cache

The 32 Kbytes Two-way Set Associative cache option is achieved by installing an additional four 8Kx8 SRAMs in bank 1 at U35, U36, U37, and U38. Install jumper block between pin 2 & 3 of W15. Remove jumper block on W14. Refer to Figure 9 below.

Figure 9 : 32 Kbytes Two-way Associative Cache



Section IV
Setup

SETUP

After the 386-25/33M ASIC Cache System hardware is assembled and the keyboard, monitor, and peripherals are installed, power up the completed system and begin the SETUP procedure. Note that this may be done with or without the system being installed in the case. Any subsequent troubleshooting and problem identification can be done more easily if the system is not installed.

SETUP can be performed by using the SETUP program built into the system BIOS.

1. SETUP from the SYSTEM BIOS

Recent advancements in chip design have enabled manufacturers to integrate the SETUP program into the system as part of its BIOS. The result is that the SETUP program is always available and it is no longer necessary to run the SETUP program from a floppy diskette.

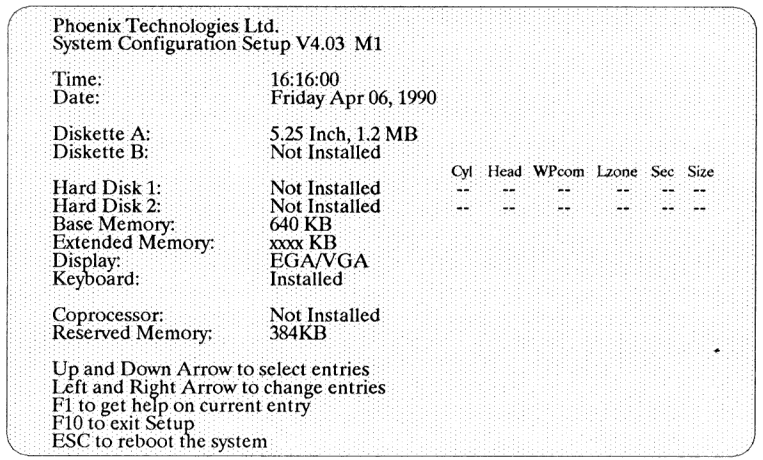
The following message is displayed on the screen when you power up your system for the first time if you have a set of Phoenix BIOS:

```
Phoenix 80386 ROM BIOS Plus Version 1.10
640K Base, xxxxK Extended

CMOS RAM ERROR, CHECK BATTERY/RUN SETUP
PRESS F1 TO CONTINUE, F2 FOR SETUP UTILITY
```

Step 1: Insert a formatted disk (DOS3.0 or higher) into the floppy drive and turn on the power to boot the system. Press F2.

CMOS Setup Screen



Step 2: When the CMOS SETUP screen above appears, *use the arrow keys to set the date and time.* Then use the arrow keys to cycle and make selections for:

Diskette: Indicates type and number of diskette drives in the system.

Fixed Disk: Selects the correct type of fixed disk being used. *Note that the type number is NOT the same as the number of megabytes of memory.*
Type is based on such technical parameters as number of heads, cylinders, sectors, etc., and is available from the fixed disk manufacturer. *To see a list of hard-disk drive types, move the highlighted block to the hard-disk 1 area and press <F1>.*

Phoenix BIOS does not support any drive that has more than 1024 cylinders.

Amount of Memory: Determine the amount of memory you have installed, and enter this number in the respective selections.

Monitor Type: Use the arrow keys to select the type of monitor used.

Step 3: After all necessary optional parameter selections have been made and PRIOR to exiting the SETUP program, insert a formatted diskette in diskette drive A.

Step 4: Use the command indicated on the SETUP screen to exit the program and reboot the system.

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Section V
Operational Options

OPERATIONAL OPTIONS

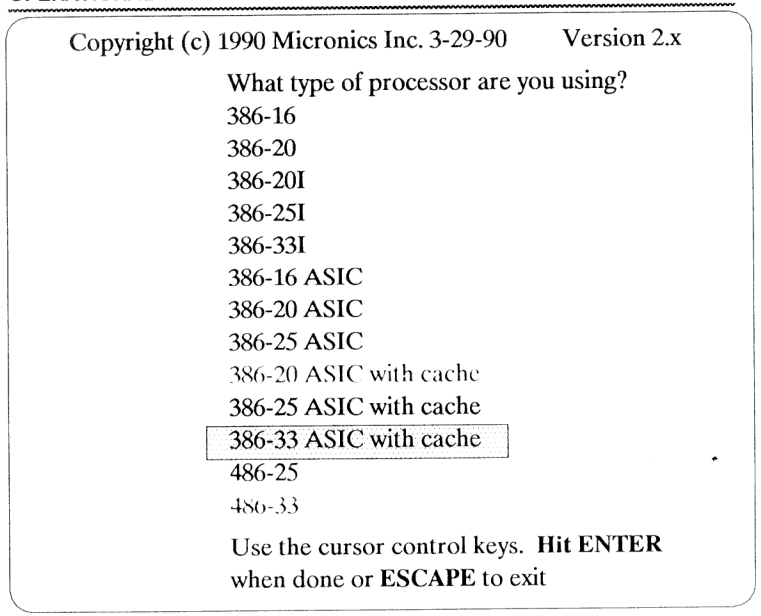
Included with each 386-25/33M ASIC Cache system board is a floppy diskette containing a number of *optional utility programs.* This chapter contains brief information about enabling/disabling cache, changing the 386 CPU speed, relocating the BIOS and EGA BIOS into RAM, and using Expanded Memory Management (MICEMM).

1. Enable or Disable Cache

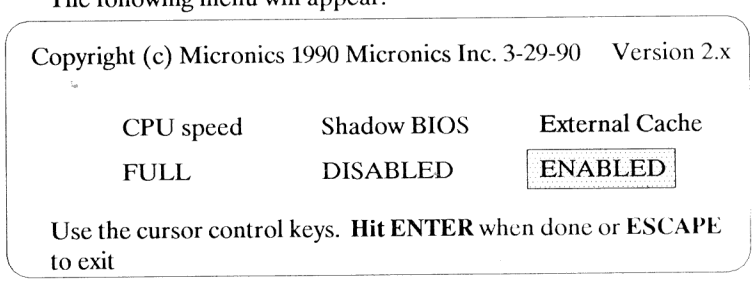
The 386-25/33M ASIC system board has an option of 32 Kbytes Direct Mapped Cache or 32 Kbytes Two-way Set Associative Cache. This cache is always enabled if DIP switch SW1-7 is ON. The SETSYS utility may be used to enable or disable this cache.

After booting up the system, insert the distribution diskette into drive A and type SETSYS at the A> prompt. If a hard disk is available, copy the SETSYS.EXE file from the distribution diskette into drive C, and type SETSYS at the C> prompt. Be certain the current drive contains the SETSYS.EXE file before attempting to execute this program.

A menu screen will appear confirming you have an 80386 ASIC cache system with the correct operating frequency. For example, the menu screen below indicates that you have an 386-25/33M ASIC with cache system board installed. Press <ENTER> to verify and continue.



The following menu will appear:



Use the **LEFT** or **RIGHT** arrow key to highlight the area below EXTERNAL CACHE.

Use the **UP** or **DOWN** arrow key to select **ENABLE** or **DISABLE**. Press <**ENTER**> to select and exit.

The cache can also be enabled or disabled at a command line in the DOS mode. To enable the cache at the command line, type SETSYS CACHE = ON at the DOS prompt. Similarly, to disbale the cache, type SETSYS CACHE = OFF.

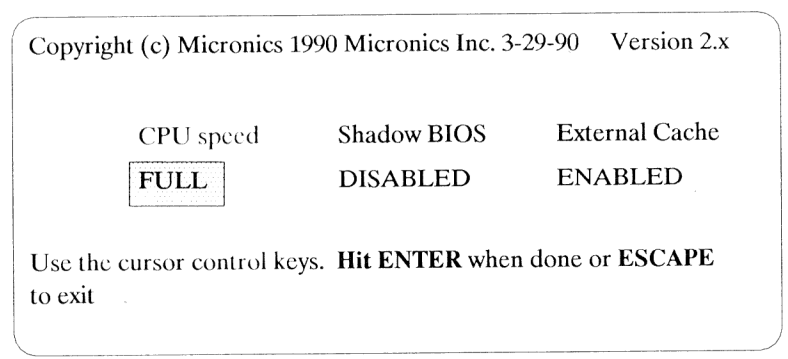
2. Changing the CPU Speed

To maximize software compatibility, the 386-25/33M ASIC Cache system board may be operated at 6MHz, 8MHz, or 386 speed. Changing speeds is accomplished by software and keyboard control utilizing a file on the distribution diskette called SETSYS.

Whenever it is powered on, the system is automatically set to operate at 386 speed. *The SETSYS utility does not change the bus speed.*

To change the speed, in the current drive that contains the SETSYS.EXE file, type SETSYS at the DOS prompt. A menu will appear confirming you have an 80386 ASIC cache system with the correct operating frequency. Press <ENTER> to verify and proceed.

The following menu will appear:



Use the **LEFT** of the **RIGHT** arrow key to highlight the area below the **CPU SPEED**.

Use the **UP** or **DOWN** arrow key to select **FULL, 8MHz** or **6MHz** speed.

When you have completed your selection, press <**ENTER**>.

The system speed may also be changed at a command line without entering into the menu option. This is achieved by:

To Change to a Speed of:	At the DOS prompt, Type:
6.00 MHz	SETSYS AT6
8.00 MHz	SETSYS AT8
386 SPEED	SETSYS 386

Resetting or repowering the system will also change the speed back to CPU speed.

NOTE:
The *SETSYS 386 command will bring the system speed back to the full non-cache speed.*

3. BIOS Relocation

To take advantage of the extremely high speed of the 32-bit bus and 80 nanosecand RAM of the 386-25/33M ASIC Cache system, the operator may place the system BIOS into RAM for execution. Furthermore, both the system BIOS and EGA BIOS can be relocated into RAM for execution. This relocation is accomplished using a file named SETSYS.EXE included in the distribution diskette shipped with each 386-25/33M ASIC Cache system board. This utility may be used to relocated the system BIOS as well as the EGA BIOS if the EGA BIOS is relocatable. See section VI part 3 for more technical information.

Be certain the SETSYS.EXE file is present in the current drive. Type SETSYS at the DOS prompt.

A menu will appear confirming you have an 386-25/33M ASIC Cache system with the correct operating frequency. Press < ENTER > to verify this is correct and proceed.

The following menu will appear:

Copyright (c) Micronics 1990 Micronics Inc. 3-29-90 Version 2.x

CPU speed	Shadow BIOS	External Cache
FULL	DISABLED	ENABLED

Use the cursor control keys. **Hit ENTER** when done or **ESCAPE** to exit

Use the LEFT or RIGHT arrow key to highlight the area below SHADOW BIOS. Use the UP or DOWN arrow key to select ENABLED or DISABLED BIOS shadowing. Press < ENTER > to select the option.

The BIOS may also be relocated or unrelocated at a command line. At the DOS prompt, type SETSYS BIOS = ON to relocate the BIOS, or SETSYS BIOS = OFF to unrelocate the BIOS.

4. FLPBOOT Utility

This Flpboot utility enables the user to install OS/2 operating system from the floppy. Due to high speeds of this system, the cache controller has to be deactivated when installing OS/2 operating system, using certain disk controller cards.

1. Insert the utility diskette with **FLPBOOT.EXE** into drive A.

2. At the DOS prompt, type: **FLPBOOT** < Enter >

3. Insert OS/2 Install System Disk into dirve A.* < Enter >

* The system will reboot from the OS/2 system disk.

5. Installing MICEMM

MICEMM, a proprietary Expanded Memory Management program included in the distribution diskette provided with each 80386 system board enables the system to use extended memory to emulate expanded memory and run any Lotus/Intel/Microsoft based expanded memory application. A few of the supported programs are:

Reflex 1.1 (Borland)

Framework II (Ashton-Tate)

Lotus 123 version 2.01 HAL, Symphony (Lotus Development Corp.)

Turbo Power Extender, Lightning (PC Support Group)

Personal Rexx (Mansfield Software)

Ready, Thinktank (Living Videotest)

Note-It (Turner Hall)

NOTE:
Your distribution diskette contains additional information regarding MICEMM in a file named MICEMM.DOC. At the DOS prompt, type **MICEMM.DOC** <Enter>.

6. Compatiblity List

The following products have been tested with the 386-25/33M ASIC Cache board.

Video Boards	*Hard disk/Floppy Controller Boards*
Video 7 VEGA Deluxe VGA	Adaptec ACB-2322 ESDI controller
Video 7 VRAM VGA	Adaptec ACB-2372 RLL controller
Genoa EGA	DTC-5280 MFM controller
Orchid VGA (8-bit card)	OMTI-8240 MFM controller
Paradise VGA Plus	Western Digital WA3 MFM controller
Paradise EGA	Western Digital WA7000 SCSI controller

For a complete compatibility list, please contact your distributor.

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Section VI
Technical Reference

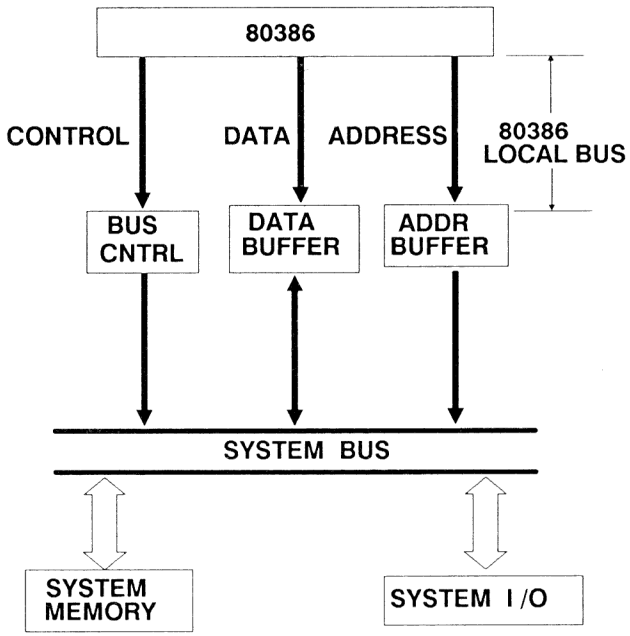
TECHNICAL REFERENCE

1. 80386 Microprocessor

The Intel 80386 Microprocessor is an advanced 32-bit microprocessor designed for application needing very high performance and optimized for multitasking operating systems. The 32-bit registers and data paths support 32-bit addresses and data types. The processor addresses up to four gigabytes of physical memory and 64 terabytes (2**46) of virtual memory. The intergrated memory management and protection architecture includes address translation registers, advanced multitasking hardware and a protection mechanism to support operating systems. In addition, the 80386 allows the simultaneous running of multiple operating systems. Instruction pipelining, on-chip address translation, and high bus bandwidth ensure short average instruction execution times and high system throughput.

Object-code compatibility with all 8086 family members (8086, 8088, 80186, 80188, 80286) means the 80386 offers imitated access to the world's largest microprocessor software base.

Figure 10 : 80386 System Bus Structure



2. 80387 Math CoProcessor

The Intel 80387 math coprocessor is an extension to the 80386 microprocessor architecture. The combination of the 387 with the 386 microprocessor dramatically increases the processing speed of the computer application software which utilizes mathematical operations. This makes an ideal computer workstation platform for applications such as financial modeling and spread sheets, CAD/CAM, or graphics.

The 80387 math coprocessor adds over seventy mnemonics to the 80386 microprocessor instruction set. Specific 80387 math operations include logarithmic, arithmetic, exponential, and trigonometric functions. The 80387 supports integer, extended integer, floating point and BCD data formats, and fully conforms to the ANSI/IEEE floating point standard.

3. 82385 32-bit Cache Controller

The 82385 Cache Controller is a high performance 32-bit peripheral for the Intel 80386 Microprocessor. It stores a copy of frequently accessed code and data from main memory in a zero wait state local cache memory. The 82385 enables the 80386 to run at its full potential by reducing the average number of CPU wait states to nearly zero. The dual bus architecture of the 82385 allows other masters to access system resources while the 80386 operates locally out of its cache. In this situation, the 82385 "bus watching" mechanism preserves cache coherency by monitoring the system bus address lines at no cost to system or local throughput. Refer to Figure 11.

The 82385 has flexible cache mapping and can support either Direct Mapped or Two-way Associative Cache. The cache memory system anticipates the CPU's need of DATA or CODE in main storage and copies it into the cache memory. DATA is the information in a particular file. CODE is the application or operating system program. Once a piece of memory is in the cache the CPU need not make repeated accesses to main memory. If the needed data resides in the cache (called a *cache hit*), it is returned to the processor without incurring wait states. If the needed data is not in the cache (called a *cache miss*) the reference is forwarded to the system and the data retrieved from the main memory.

The *hit rate* is the percentage of all accesses that are hits; that is, either the code or data is found in the cache memory. The cache hit rate is affected by the cache algorithm, cache size, and the program being run. The cache algorithm is the formula by which the cache controller picks the memory to load in to the cache and when and how to change the memory in the cache. If cache is organized so that the code and data the processor needs most often is in cache, the cache significantly reduces average memory access time. Programs execute more rapidly when most operations are transfer to and from the faster cache memory.

Direct Mapped Cache

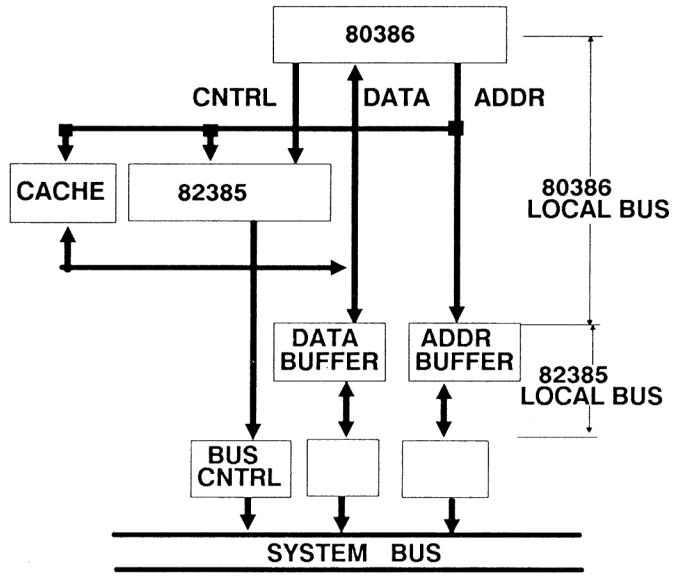
In the direct mapped cache, each block from main memory can be stored in a single cache location. The direct mapped cache has its drawbacks if the processor makes frequent request from a pair of locations where two pieces of memory are mapped to the same cache. The controller must then access main memory frequently because only one of these locations can be in the cache at a time. When two pieces of memory are mapped to the same cache, the controller must overwrite the data in the cache location and constantly update it with the other memory which is competing for the same cache location. The code jumps back and forth to the same cache location which results in a low hit rate. This result is also called *thrashing*.

Two-way Set Associative Cache

The excessive main memory traffic that is a drawback of a direct mapped cache organization is reduced and the hit rate increased in the two-way set associative cache organization because in this cache organization there are two locations where each block of memory can be stored. This structure can be thought of as two half-size direct mapped caches in parallel. The two-way set associative cache is organized as two banks (bank A and bank B).

The performance advantage of the two-way set associative cache over the direct mapped cache is that it reduces the potential for thrashing. Two pieces of memory are now able to be mapped to two different locations in the cache area. It is not necessary for the controller to constantly overwrite any data in one cache location thereby reducing the necessity for the code to jump back and forth to the same cache location. This results in a higher hit rate.

Figure 11: 80386 CPU/82385 System Bus Structure



4. System Board I/O MAP

Port	Address Bits										Device
	0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	
000H-00FH	R	R	R	R	X	0	0	0	0	0	8237A-5 Byte DMA controller
020H-021H	R	X	X	X	X	1	0	0	0	0	8259A Interrupt ontroller 1
040H	0	0	0	0	X	0	1	0	0	0	Programmable Interval Timer 1 8254-2 System Clock (Counter 0)
041H	1	0	0	0	X	0	1	0	0	0	Programmable Interval Timer 1 8254-2 Refresh Request (Counter 1)
042H	0	1	0	0	X	0	1	0	0	0	Programmable Interval Timer 1 8254-2 Speaker Tone (Counter 2)
043H	1	1	0	0	X	0	1	0	0	0	Programmable Interval Timer 1 8254-2 Command Mode Register
049H	1	0	0	1	X	0	1	0	0	0	Programmable Interval Timer 2 8254-2 Not Used (Counter 1)
04AH	0	1	0	1	X	0	1	0	0	0	Programmable Interval Timer 2 8254-2 Refresher request extend speed control (Counter 2)

- Continued -

Port	Address Bits										Device
	0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	
04BH	1	1	0	1	X	0	1	0	0	0	Programmable Interval Timer 2 8254-2 Command Mode Register
060H	0	X	0	0	0	1	1	0	0	0	8042 Data I/O Register
061H	1	X	X	0	0	1	1	0	0	0	NMI Status
064H	0	X	1	0	0	1	1	0	0	0	8042 Status/Command Register
068H	0	0	0	1	0	1	1	0	0	0	Tubo LED ON
070H	0	X	X	0	1	1	1	0	0	0	RTC Address Register Data (Bits <6...0>)
070H	0	X	X	0	1	1	1	0	0	0	NMI Register Data (Bit <7> = 0)
071H	1	X	X	0	1	1	1	0	0	0	RTC Data I/O Register
080H	0	0	0	0	X	0	0	1	0	0	DMA Page Register Reserved
081H	1	0	0	0	X	0	0	1	0	0	DMA Page Register CH 2 Page
082H	0	1	0	0	X	0	0	1	0	0	DMA Page Register CH 3 Page
083H	1	1	0	0	X	0	0	1	0	0	DMA Page Register CH1 Page
084H	0	0	1	0	X	0	0	1	0	0	DMA Page Register Reserved
085H	0	1	0	1	X	0	0	1	0	0	DMA Page Register Reserved
086H	0	1	1	0	X	0	0	1	0	0	DMA Page Register Reserved
087H	1	1	1	0	X	0	0	1	0	0	DMA Page Register CH0 Page

- Continued -

Port	Address Bits										Device
	0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	
088H	0	0	0	1	X	0	0	1	0	0	DMA Page Register Spare
089H	1	0	0	1	X	0	0	1	0	0	DMA Page Register CH6 Page
08AH	0	1	0	1	X	0	0	1	0	0	DMA Page Register CH7 Page
08BH	1	1	0	1	X	0	0	1	0	0	DMA Page Register CH5 Page
08CH	0	0	1	1	X	0	0	1	0	0	DMA Page Register Reserved
08DH	1	0	1	1	X	0	0	1	0	0	DMA Page Register Reserved
08EH	0	1	1	1	X	0	0	1	0	0	DMA Page Register Reserved
08FH	1	1	1	1	X	0	0	1	0	0	DMA Page Register Refresh Page
0A0H-0A1H	R	X	X	X	X	1	0	1	0	0	8259A Interrupt Controller 2
0C0H-0CFH	X	R	R	R	R	0	1	1	0	0	8237A-5 Word DMA controller
0F0H	0	X	X	0	X	1	1	1	0	0	Clear 80387 Busy
0F8H-0FFH or 800000F8H-800000FFH	X	R	R	1	1	1	1	1	0	0	80387 Command Ports
092H											Fast Gate A20

X = Don't Care, R = Register Dependent

5. EPROM Shadowing for the 386-26/33M ASIC Cache System

The 386-25/33M ASIC system is designed to speed up memory access to BIOS with the shadow option. This option copies data from slower memory devices such as ROMs and EPROMs into RAM, since access to local RAM is much faster than ROM. Section V part 3 describes setting the shadowing option in detail.

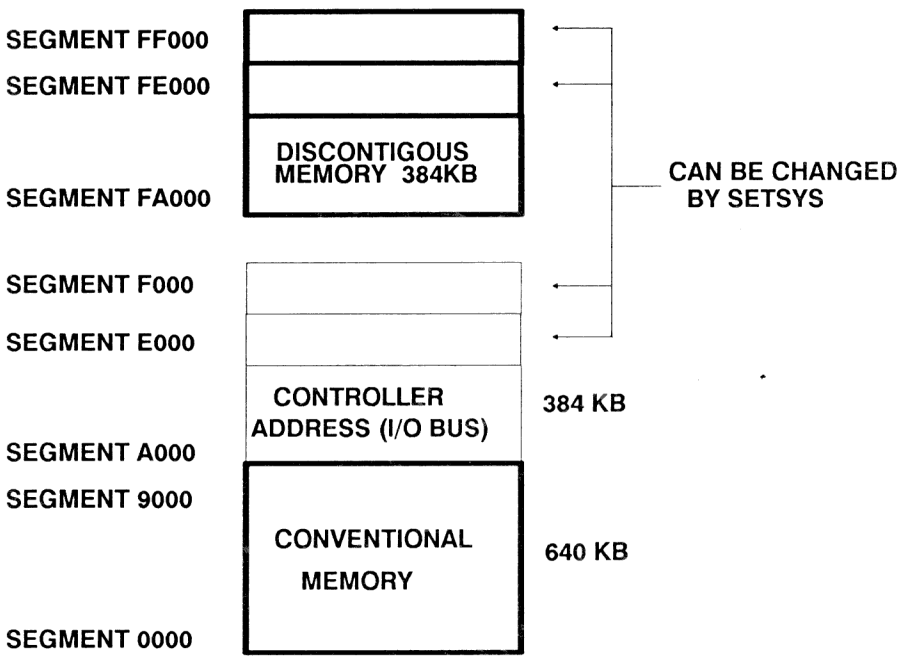
There are three areas where the shadow features stores the BIOS ROM, adapter ROM, and video ROM. Figure 12 shows the memory address ranges available for shadowing.

When shadowing the BIOS ROM, the ROM contents must be copied to the shadow RAM area before the lock bit is set in the configuration register. Once the lock bit is set, bits of these RAM areas become read only. If video RAM shadowing has been enabled and the "video read only" in the configuration register is set, then the video shadow area will also become read only.

The advantage of the shadowing option is to speed up memory access to BIOS, and the disadvantage of this option is it occupies too much memory space (depends on the size of ROM installed).

If ROM or video RAM shadowing is not selected, then any addresses generated in these areas will access the ROM or system video RAM. Any local DRAM with the same physical addresses as the ROM or video RAM cannot be directly addressed.

Figure 12 : Memory Map for 640KB of Memory



6. SETSYS UTILITY

Memory

The 386-25/33M ASIC cache system has a unique memory system that offers features that will optimize the use of memory beyond the 640K base memory. The 128KB-block starting at address FE0000 may be mapped (shadowed) via hardware registers to replace the 128KB area assigned to the system ROM at addresses between 0E0000 to 0FFFFF. When the 128KB block is mapped, it can be addressed at either FE0000 or E0000. The *Setsys.exe* utility provided offers the option of this relocation. The memory mapped I/O address reference is at 80C00000. In addition to relocation, the 128KB block of RAM begining at address FE0000 can be write-protected. These options offered allows the system ROM to be relocated to the high-speed RAM for significant improvements in performance furing the execution of the BIOS. Video display cards that may be relocated, and have address residing at C000 will have its BIOS mapped to FE000:0. This feature allows the system to have faster video speed as a result of executing the video bios in high speed RAM. Bit 22 of address 80C00000 is used for the cache enable and cache disable feature of the 80386 ASIC system.

The following describes the memory mapped address at 80C00000:

Bit 0	-0 Relocate -1 Non-relocate
Bit 1	-0 Write Protect -1 Non write protect
Bit 22	-0 Cache off -1 Cache on

The non-cacheable regions are:

1) The 384K region between 640K and 1024K.

2) The 384K region below the 16,384K boundary.

3) The region between D00000 to DFFFFF or E00000 to EFFFFF.

This region is non-cacheable to enable the support of intelligent I/O cards.

System Speed

The Setsys utility controls the system speed by extending refresh cycles to reduce the amount of time the CPU is executing. The CPU is kept in a HOLD state while the refresh cycle is extended, and will wait until the completion of the the refresh cycle to resume execution. As a result of this, the CPU has lass time for execution which results in slower program execution speed.

An interval timer, at I/O address 4AH is used for this feature. The Setsys utility uses port 4A to setup the value for the counter, and port 4B to setup the mode. A one-shot mode (Mode 1) is used to produce a variable lenght signal.

The turbo port that is used to set the system to full speed is at PORT 68H bit 7.

Bit 7 = 0 Turbo LED on

Bit 7 = 1 Turbo LED off