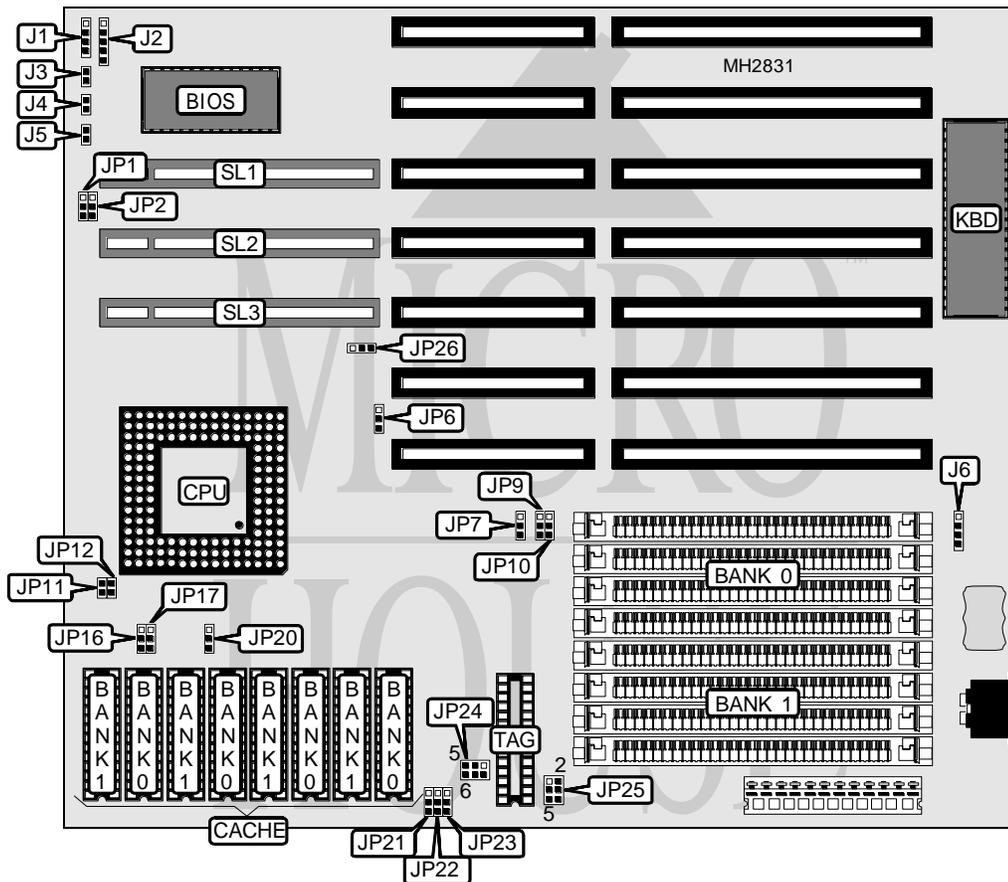


SER 486 - V L A

Processor	CX486M6/80486SX/80487SX/80486DX/80486DX2
Processor Speed	25/33/40/50(internal)/50/66(internal)MHz
Chip Set	ALI
Max. Onboard DRAM	32MB
Cache	64/128/256KB
BIOS	AMI
Dimensions	254mm x 218mm
I/O Options	32-bit VESA local bus slots (3)
NPU Options	None



CONNECTIONS			
Purpose	Location	Purpose	Location
Speaker	J1	Turbo switch	J5
Power LED & keylock	J2	External battery	J6
Reset switch	J3	32-bit VESA local bus slots	SL1 - SL3
Turbo LED	J4		

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SER

486-VLA

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DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CACHE CONFIGURATION			
Size	Bank 0	Bank 1	TAG
64KB	(4) 8K x 8	(4) 8K x 8	(1) 8K x 8
128KB	(4) 32K x 8	NONE	(1) 8K x 8
256KB	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8

CACHE JUMPER CONFIGURATION				
Size	JP21	JP22	JP23	JP24
64KB	1 & 2	1 & 2	Open	3 & 4
128KB	2 & 3	1 & 2	Open	1 & 2, 3 & 4, 5 & 6
256KB	1 & 2	1 & 2	1 & 2	1 & 2, 3 & 4, 5 & 6

Note: Pins designated should be in the closed position.

CPU TYPE CONFIGURATION							
Type	JP7	JP9	JP11	JP12	JP16	JP17	JP20
CX486M6	2 & 3	2 & 3	Open	Open	1 & 2	Open	1 & 2
80486SX	1 & 2	1 & 2	Closed	Closed	1 & 2	Open	1 & 2
80487SX	1 & 2	1 & 2	Closed	Closed	2 & 3	1 & 2	1 & 2
80486DX	1 & 2	1 & 2	Closed	Closed	2 & 3	2 & 3	1 & 2
80486DX2	1 & 2	1 & 2	Closed	Closed	2 & 3	2 & 3	1 & 2

Note: Pins designated should be in the closed position.

CPU SPEED CONFIGURATION				
Speed	JP6	JP10	JP25	JP26
25MHz	1 & 2	1 & 2	3 & 4	1 & 2
33MHz	1 & 2	1 & 2	1 & 2, 5 & 6	1 & 2
40MHz	2 & 3	2 & 3	1 & 2, 3 & 4	2 & 3
50iMHz	1 & 2	1 & 2	3 & 4	1 & 2
50MHz	2 & 3	2 & 3	3 & 4	2 & 3
66iMHz	1 & 2	1 & 2	1 & 2, 5 & 6	1 & 2

Note: Pins designated should be in the closed position.

VESA WAIT STATE CONFIGURATION	
Wait states	JP1
0 wait states	pins 1 & 2 closed
1 wait state	pins 2 & 3 closed

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SER

486-VLA

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BUS SPEED CONFIGURATION	
CPU speed	JP2
<= 33MHz	pins 1 & 2 closed
> 33MHz	pins 2 & 3 closed