INTEGRATED WORKSTATIONS, INC.
C O M M U N I Q U E   2 8 6

Processor	80286
Processor Speed	12/16MHz
Chip Set	Zymos POACH
Max. Onboard DRAM	4MB
Cache	None
BIOS	Award
Dimensions	121mm x 365mm
I/O Options	Multifunction DB-44 port, network interface controller
NPU Options	80287
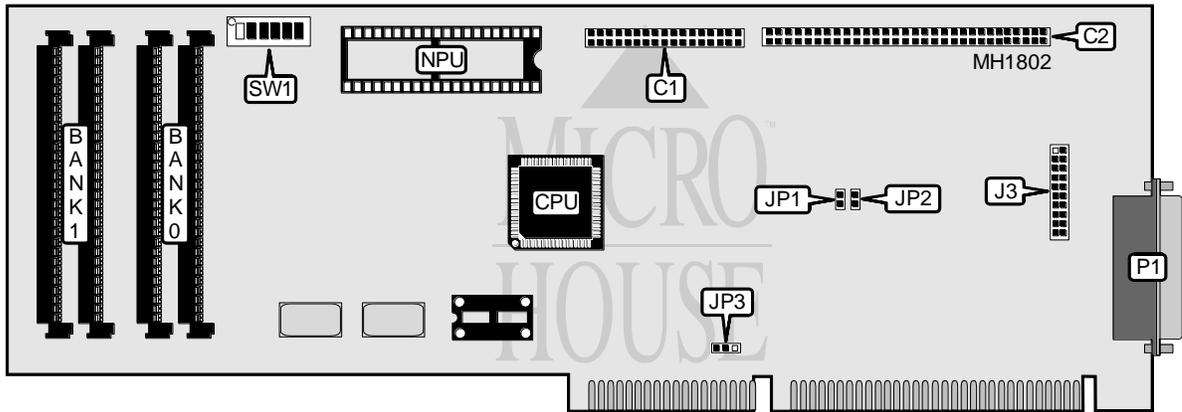
CONNECTIONS	
Purpose	Location
Primary daughterboard or local backplane	C1 & C2
Secondary daughterboard	J3
Multifunction DB-44 port & LAN connection	P1

USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Host attention interrupt select IRQ10 at OA Hex	JP3	pins 1 & 2 closed
Host attention interrupt select IRQ12 at OC Hex	JP3	pins 2 & 3 closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
512KB	(2) 256K x 9	NONE
1MB	(2) 256K x 9	(2) 256K x 9
2MB	(2) 1M x 9	NONE
4MB	(2) 1M x 9	(2) 1M x 9

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NODE ID ADDRESS						
Node	SW1/1	SW1/2	SW1/3	SW1/4	SW1/5	SW1/6
0	Off	Off	Off	Off	Off	Off
1	On	Off	Off	Off	Off	Off
2	Off	On	Off	Off	Off	Off
3	On	On	Off	Off	Off	Off
4	Off	Off	On	Off	Off	Off
59	On	On	Off	On	On	On
60	Off	Off	On	On	On	On
61	On	Off	On	On	On	On
62	Off	On	On	On	On	On
63	On	On	On	On	On	On
Note:	A total of 63 node address settings are available. The switches are a binary representation of the decimal node addresses, and have the following decimal values: 1=1, 2=2, 3=4, 4=8, 5=16, 6=32. Switches in the off position maintain a zero value. Sum total the switches in the on position to obtain the correct node address. Node 0 is a non-valid address.					

BASE MEMORY ADDRESS		
Address	JP1	JP2
í DC000h	Closed	Open
CC000h	Closed	Closed