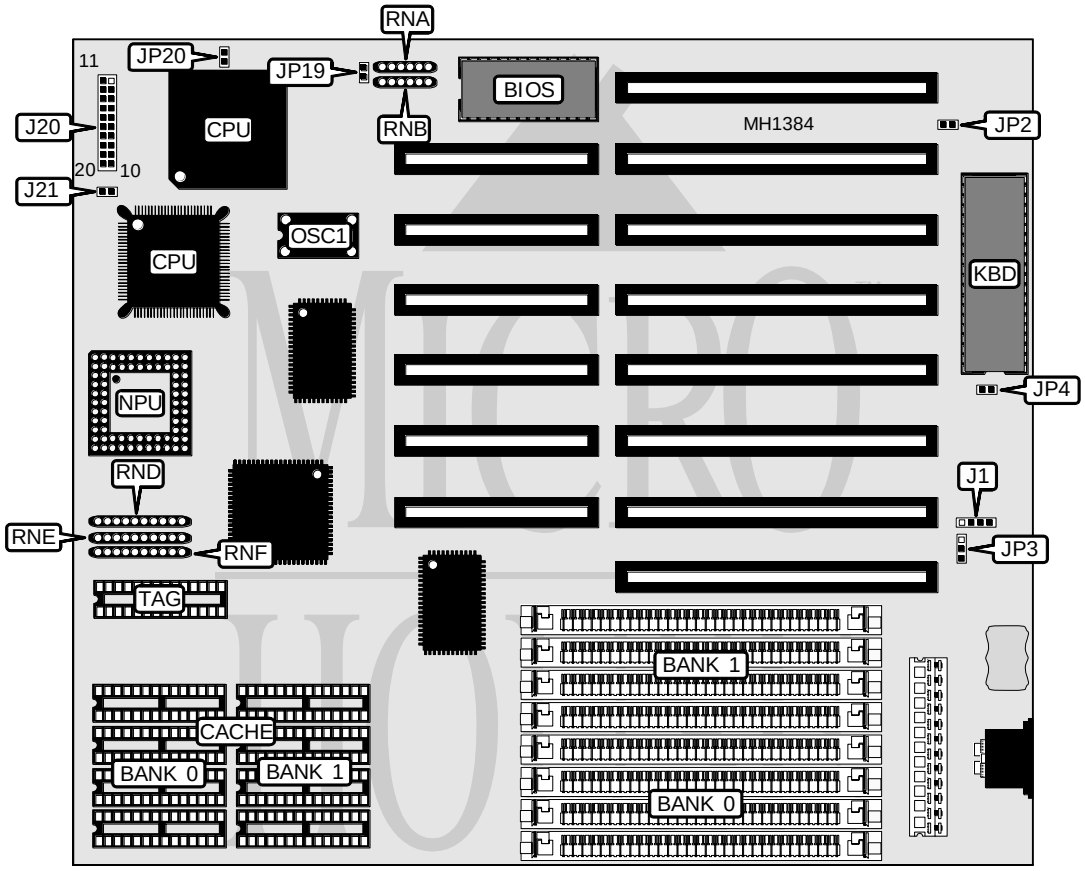
TMC RESEARCH CORPORATION
P A T 3 8 P M

Processor	80386DX/CX486DLC
Processor Speed	33/40MHz
Chip Set	OPTI
Max. Onboard DRAM	32MB
SRAM Cache	64/128/256KB
BIOS	AMI
Dimensions	254mm x 220mm
I/O Options	None
NPU Options	80387/CX83D87



CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	J1	Reset switch	J20/pins 9 & 19
Speaker	J20/pins 1-4	IDE interface LED	J20/pins 10 & 20
Turbo switch	J20/pins 7 & 17	IDE interface LED	J21
Turbo LED	J20/pins 8 & 18		

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TMC RESEARCH CORPORATION
P A T 3 8 P M

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
AT bus clock select CPU/4 (CPU 33MHz)	JP2	open
AT bus clock select CPU/5 (CPU 40MHz)	JP2	closed
í CMOS memory normal operation (internal battery)	JP3	pins 1 & 2 closed
CMOS memory normal operation (external battery)	JP3	open
CMOS memory clear	JP3	pins 2 & 3 closed
í Monitor type select color	JP4	closed
Monitor type select monochrome	JP4	open
í NPU synchronous with CPU	JP20	open
NPU synchronous with oscillator installed at OSC1	JP20	closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

SRAM CONFIGURATION			
Size	Cache	Location	TAG
64KB	(8) 8K x 8	Banks 0 & 1	(1) 8K x 8
128KB	(4) 32K x 8	Bank 0	(1) 8K x 8
256KB	(8) 32K x 8	Banks 0 & 1	(1) 32K x 8

SRAM JUMPER CONFIGURATION			
Resistor	64KB	128KB	256KB
RND	closed	open	open
RNE	open	closed	open
RNF	open	open	closed

CPU RESISTTOR NETWORK CONFIGURATION				
CPU(PQFP)	CPU(PGA)	JP19	RNA	RNB
80386DX	***CX486DLC***	closed	open	closed
NONE	***CX486DLC***	N/A	open	closed
80386DX	***80386DX***	closed	closed	open
NONE	***80386DX***	N/A	closed	open
80386DX	NONE	open	closed	open
Note: The CPUs in bold-italic are the active CPUs.				