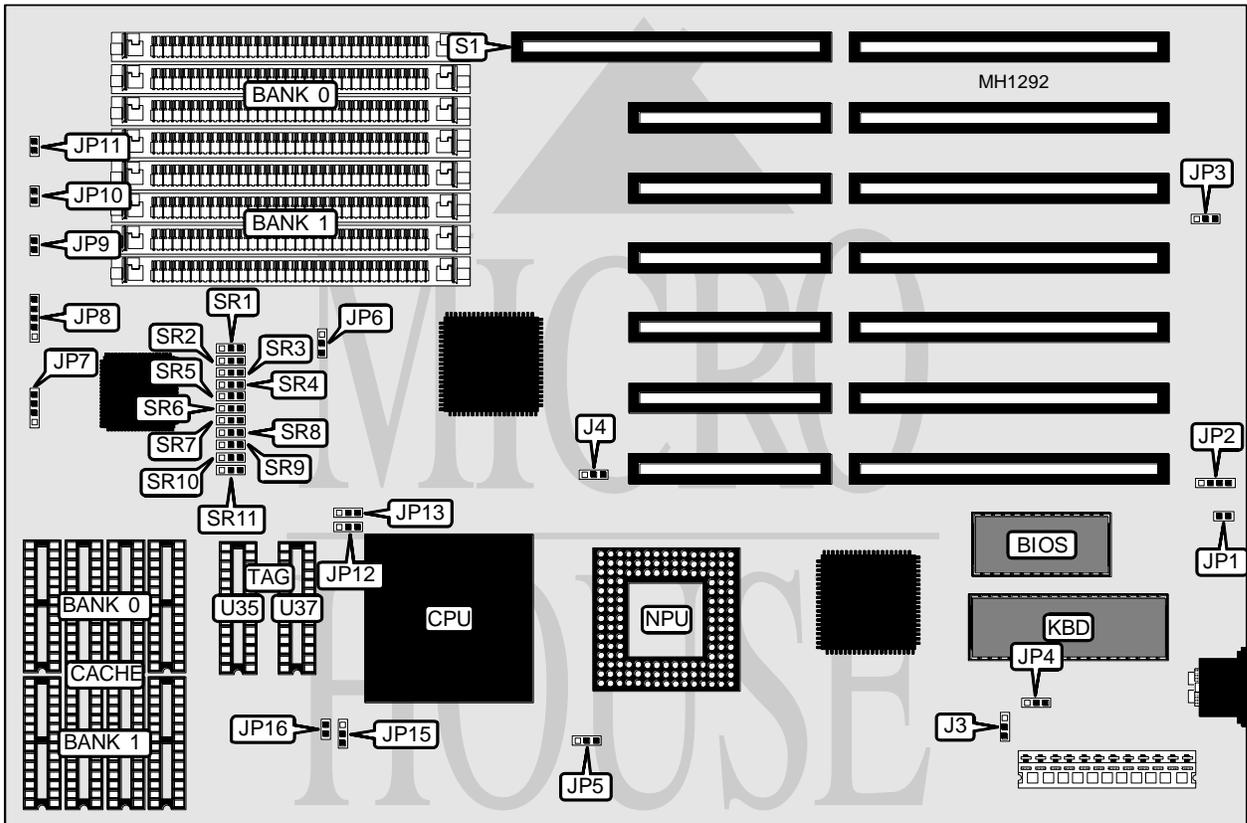


UNIDENTIFIED

486TC4

Processor	80486SX/80487SX/80486DX
Processor Speed	20/25/33MHz
Chip Set	C & T
Max. Onboard DRAM	32MB
SRAM Cache	64/128/256KB
BIOS	AMI
Dimensions	330mm x 218mm
I/O Options	32-bit external memory card slot
NPU Options	4167



CONNECTIONS			
Purpose	Location	Purpose	Location
External battery	JP2	Turbo LED	JP10
Speaker	JP7	Turbo switch	JP11
Power LED & keylock	JP8	32-bit external memory card	S1
Reset switch	JP9		

Continued on next page . . .

UNIDENTIFIED

486TC4

... continued from previous page

USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Factory configured - do not alter	J3	unknown
í Factory configured - do not alter	J4	unknown
í Battery select internal	JP1	closed
Battery select external	JP1	open
í CMOS memory normal operation	JP3	pins 1 & 2 closed
CMOS memory clear	JP3	pins 2 & 3 closed
í Monitor type select color	JP4	pins 1 & 2 closed
Monitor type select monochrome	JP4	pins 2 & 3 closed
í Factory configured - do not alter	JP5	unknown
í Factory configured - do not alter	JP15	unknown

CPU JUMPER CONFIGURATION			
CPU	JP12	JP13	JP16
80486DX	pins 2 & 3 closed	pins 2 & 3 closed	closed
80487SX	pins 1 & 2 closed	pins 2 & 3 closed	closed
80486SX	pins 2 & 3 closed	pins 1 & 2 closed	open

SRAM JUMPER CONFIGURATION			
Jumper	64KB	128KB	256KB
SR1	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
SR2	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
SR3	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
SR4	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
SR5	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
SR6	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
SR7	pins 2 & 3 closed	pins 2 & 3 closed	pins 1 & 2 closed
SR8	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed
SR9	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
SR10	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
SR11	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed

Continued on next page ...

UNIDENTIFIED

486TC4

... continued from previous page.

SRAM CONFIGURATION				
Size	Cache SRAM	Location	TAG (U35)	TAG (U37)
32KB	(4) 8K x 8	Bank 0	(1) 8K x 8	NONE
64KB	(8) 8K x 8	Banks 0 & 1	(1) 8K x 8	(1) 8K x 8
128KB	(4) 32K x 8	Bank 0	(1) 8K x 8	NONE
256KB	(8) 32K x 8	Banks 0 & 1	(1) 8K x 8	(1) 8K x 8

DRAM CONFIGURATION			
Size	Bank 0	Bank 1	JP6
1MB	(4) 256K x 9	NONE	pins 1 & 2 closed
2MB	(4) 256K x 9	(4) 256K x 9	pins 1 & 2 closed
4MB	(4) 1M x 9	NONE	pins 1 & 2 closed
5MB	(4) 1M x 9	(4) 256K x 9	pins 2 & 3 closed
8MB	(4) 1M x 9	(4) 1M x 9	pins 1 & 2 closed
16MB	(4) 4M x 9	NONE	pins 1 & 2 closed
17MB	(4) 4M x 9	(4) 256K x 9	pins 2 & 3 closed
20MB	(4) 4M x 9	(4) 1M x 9	pins 2 & 3 closed
32MB	(4) 4M x 9	(4) 4M x 9	pins 1 & 2 closed