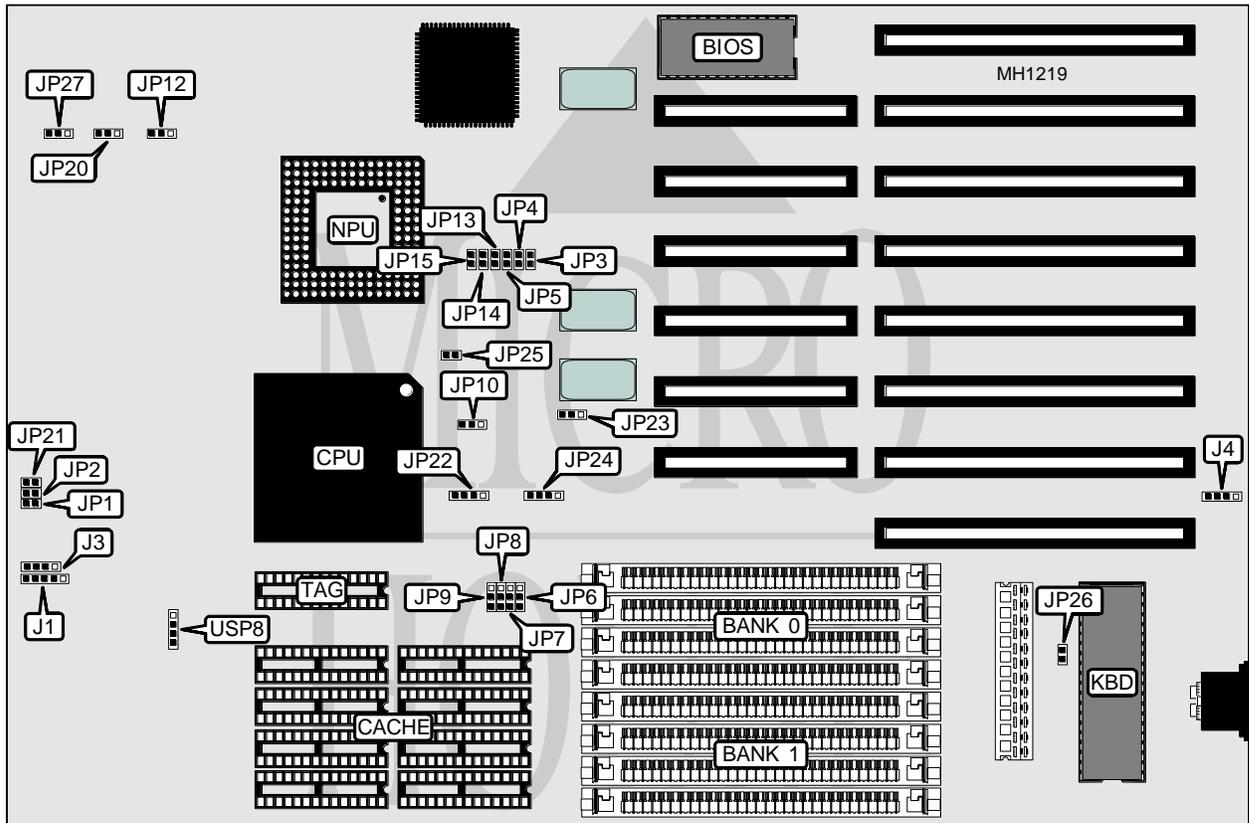


ISA/EISA, INC. 486B

Processor	80486SX/80487SX/80486DX
Processor Speed	20/33MHz
Chip Set	OPTI
Max. Onboard DRAM	32MB
SRAM Cache	64/256KB
BIOS	AMI
Dimensions	330mm x 218mm
I/O Options	None
NPU Options	4167



CONNECTIONS			
Purpose	Location	Purpose	Location
Power LED & keylock	J1	Turbo switch	JP2
Speaker	J3	Turbo LED	JP21
External battery	J4	Cooling fan switch	JP25
Reset switch	JP1	Cooling fan power	USP8

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486B

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USER CONFIGURABLE SETTINGS		
Function	Jumper	Position
í Factory configured - do not alter	JP10	unknown
í CPU speed select switchable at keyboard	JP12	pins 1 & 2 closed
CPU speed select switchable at turbo switch	JP12	pins 2 & 3 closed
í Factory configured - do not alter	JP26	open
í Video BIOS shadow before initialization	JP27	pins 1 & 2 closed
Video BIOS shadow after initialization	JP27	pins 2 & 3 closed

CPU JUMPER CONFIGURATION			
CPU	JP22	JP23	JP24
80486DX (33MHz)	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 and 3 & 4 closed
80487SX (20MHz)	pins 3 & 4 closed	pins 2 & 3 closed	pins 1 & 2 and 3 & 4 closed
80486SX (20MHz)	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed

DRAM CONFIGURATION		
Size	Bank 0	Bank 1
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 1M x 9	(4) 256K x 9
8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
17MB	(4) 4M x 9	(4) 256K x 9
20MB	(4) 1M x 9	(4) 4M x 9
20MB	(4) 4M x 9	(4) 1M x 9
32MB	(4) 4M x 9	(4) 4M x 9

SRAM JUMPER CONFIGURATION					
Size	JP6	JP7	JP8	JP9	JP20
64KB	pins 1 & 2				
256KB	pins 2 & 3	pins 1 & 2			
Disabled	N/A	N/A	N/A	N/A	pins 2 & 3

Note: Pins designated should be in the closed position.

SRAM CONFIGURATION		
Size	Cache SRAM	TAG
64KB	(8) 8K x 8	(1) 8K x 8
256KB	(8) 32K x 8	(1) 32K x 8

I/O BUS SPEED JUMPER CONFIGURATION						
Bus Speed	JP3	JP4	JP5	JP13	JP14	JP15
CPU/8	open	open	open	open	open	closed
CPU/6	open	open	open	open	closed	open
CPU/5	open	open	open	closed	open	open
CPU/4	open	open	closed	open	open	open
CPU/3	open	closed	open	open	open	open
CPU/2	closed	open	open	open	open	open