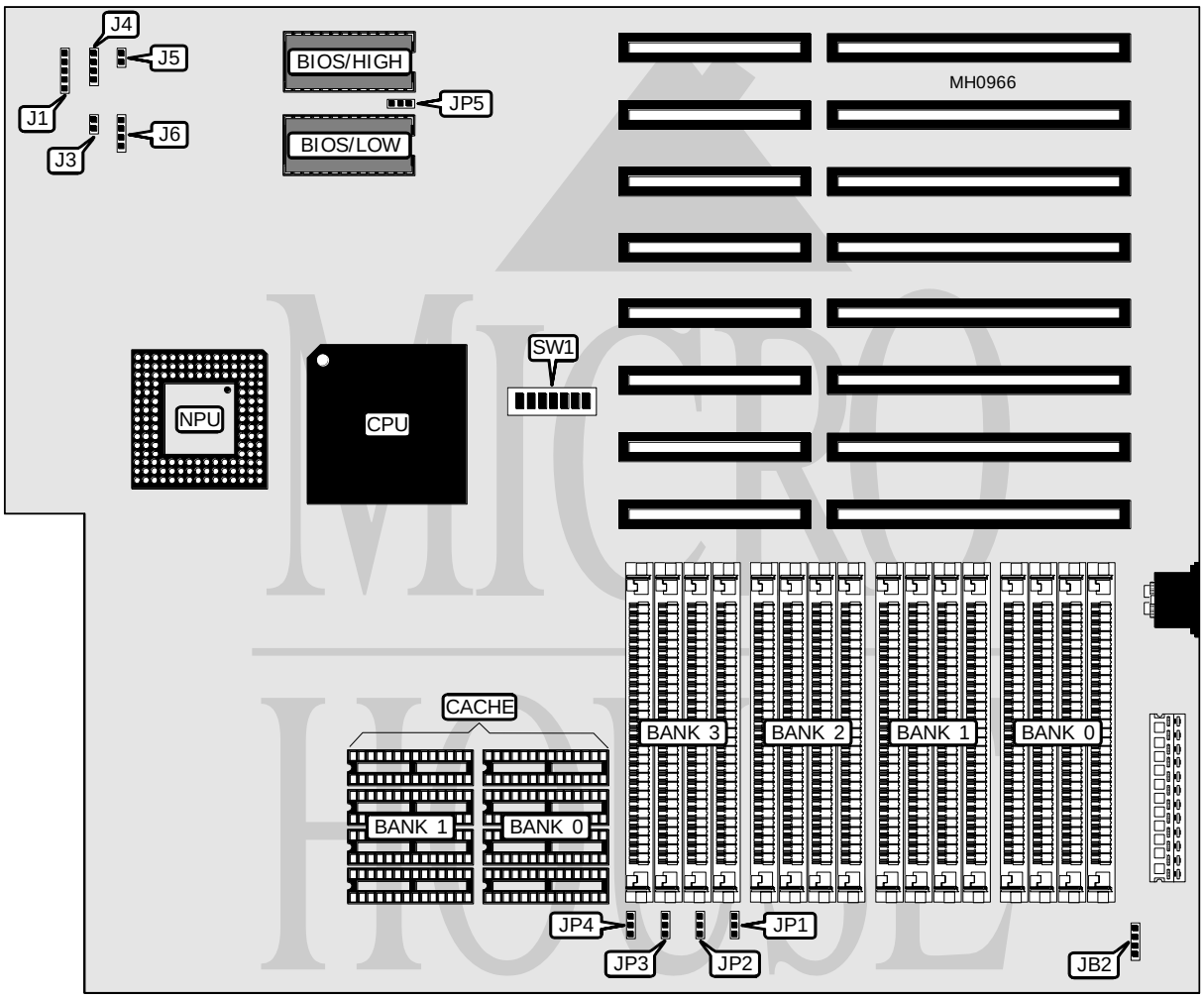
UNIDENTIFIED
486LC25/33

Processor	80486DX
Processor Speed	25/33MHz
Chip Set	Intel
Max. Onboard DRAM	16MB
Cache	128/256KB
BIOS	AMI/Award/Phoenix
Dimensions	335mm x 277mm
I/O Options	None
NPU Options	4167



CONNECTIONS			
Purpose	Location	Purpose	Location
Power LED & keylock	J1	Reset switch	J5
Turbo switch	J3	Turbo LED	J6
Speaker	J4	External battery	JB2
Note: Pin one locations are unidentified.			

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USER CONFIGURABLE SETTINGS		
Function	Jumper/Switch	Position
í DRAM speed select 80ns or 100ns (for 25Mhz CPU)	JP4	pins 2 & 3 closed
DRAM speed select 60ns or 80ns (for 33MHz CPU)	JP4	pins 1 & 2 closed
í Factory configured - do not alter	SW1/1	N/A
í Operating system select other than SCO UNIX Open Desktop	SW1/2	Off
Operating system select SCO UNIX Open Desktop	SW1/2	On
í Monitor type select color	SW1/5	On
Monitor type select monochrome	SW1/5	Off
í DRAM 32-bit access enabled	SW1/6	On
DRAM 32-bit access disabled	SW1/6	Off

DRAM CONFIGURATION				
Size	Bank 0	Bank 1	Bank 2	Bank 3
1MB	(4) 256K x 9	NONE	NONE	NONE
2MB	(4) 256K x 9	(4) 256K x 9	NONE	NONE
3MB	(4) 256K x 9	(4) 256K x 9	(4) 256K x 9	NONE
4MB	(4) 256K x 9	(4) 256K x 9	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE	NONE	NONE
8MB	(4) 1M x 9	(4) 1M x 9	NONE	NONE
12MB	(4) 1M x 9	(4) 1M x 9	(4) 1M x 9	NONE
16MB	(4) 1M x 9	(4) 1M x 9	(4) 1M x 9	(4) 1M x 9

DRAM JUMPER CONFIGURATION			
Size	JP1	JP2	JP3
1MB	pins 1 & 2 closed	pins 1 & 2 closed	pins 1 & 2 closed
2MB	pins 2 & 3 closed	pins 1 & 2 closed	pins 1 & 2 closed
3MB	pins 1 & 2 closed	pins 2 & 3 closed	pins 1 & 2 closed
4MB[1]	pins 2 & 3 closed	pins 2 & 3 closed	pins 1 & 2 closed
4MB[2]	pins 1 & 2 closed	pins 1 & 2 closed	pins 2 & 3 closed
8MB	pins 2 & 3 closed	pins 1 & 2 closed	pins 2 & 3 closed
12MB	pins 1 & 2 closed	pins 2 & 3 closed	pins 2 & 3 closed
16MB	pins 2 & 3 closed	pins 2 & 3 closed	pins 2 & 3 closed

Note [1] : Use this setting when (4) 256K x 9 SIMMs are populating all four banks.
Note [2] : Use this setting when (4) 1M x 9 SIMMs are populating Bank 0.

CACHE CONFIGURATION		
Size	Bank 0	Bank 1
128KB	(4) 32K x 8	NONE
256KB	(4) 32K x 8	(4) 32K x 8

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CACHE SWITCH CONFIGURATION		
Function	Switch SW1	Position
í SRAM cache enabled	SW1/3	On
SRAM cache disabled	SW1/3	Off
í DRAM installed between 12MB and 16MB is cached	SW1/4	On
DRAM installed between 12MB and 16MB is not cached	SW1/4	Off

BIOS CONFIGURATION		
Size	JP5	SW1/7
27256	pins 1 & 2 closed	Off
27512	pins 2 & 3 closed	On