µPD70320(V25),70322,70325(V25+),70327(V25S),79011
µPD70330(V35),70332,70335(V35+),70337(V35S),79021

V25™/V35™ FAMILY
16/8-BIT SINGLE CHIP MICROCOMPUTER

The V25/V35 family members are single chip microcomputers integrating a 16-bit CPU, internal RAM, serial interfaces, timers, DMA controllers, interrupt controllers, ports, etc. Their instruction set is software upward compatible to the 16/8-bit microprocessors µPD70108H/70116H (V20H™/V30H™) in native mode. The application area of this microcomputer is very wide, e.g. data processing, terminals, networks, printers, ECR, etc., and with use of the security function of V25S™/V35S™ applications like on-line money collection systems or game machines are safer protected. Where high speed DMA transfers are requested, V25+™/V35+™ are the right candidates.

PROCESSOR OVERVIEW

µPD70320, µPD70320(A)	V25™ ROMless, 8-bit data bus, 8 MHz system frequency
µPD70322, µPD70322(A)	V25™ with 16k mask ROM
µPD70325, µPD70325(A)	V25+™,same as V25™, high speed DMA,10MHz system frequency
µPD70327	V25S™, same as V25™, code translation table
µPD79011	V25™ with Realtime OS kernel in 16k internal ROM
µPD70330, µPD70330(A)	V35™ ROMless, 16-bit data bus, 8 MHz system frequency
µPD70332, µPD70332(A)	V35™ with 16k mask ROM
µPD70335, µPD70335(A)	V35+™, same as V35™, high speed DMA, 10 MHz system frequency
µPD70337	V35S™, same as V35™, code translation table
µPD79021	V35™ with Realtime OS kernel in 16k internal ROM

Available packages:	84-pin PLCC
	94-pin plastic QFP

FEATURES

* Internal 16-Bit architecture

* maximum internal system frequency: 8 MHz (μPD70320, μPD70322, μPD70327, μPD79011 and
μPD70330, μPD70332, μPD70337, μPD79021)
9 MHz (μPD70325(A) and μPD70335(A))
10 MHz (μPD70325 and μPD70335)

* Three-step pipelining

* External 8-Bit data bus (only μPD7032x and μPD79011)

* External 16-Bit data bus (only μPD7033x and μPD79021)

* Built-in RAM: 256 words x 8 bits

* Built-in ROM: 16384 words x 8 bits (only μPD70322, μPD70332, μPD79011 and μPD79021)

* Realtime OS software implemented in built-in ROM (only μPD79011 and μPD79021)

* Built-in instruction code translation function to protect program code from software piracy
(only μPD70327 and μPD70337)

* I/O lines (input port: 4 bits, input/output port: 20 bits)

* Comparator port (Port T): 8 bits

* Serial interface (with internal baud rate generator): 2 channels
    - Asynchronous mode
    - I/O Interface mode

* Interrupt controller
    - Programmable software priority (8 levels)
    - Vector interrupt function
    - Register bank switch response
    - Macro service function

* DRAM and pseudo SRAM refreshing function

* DMA controller: 2 channels
    - High speed DMA transfers up to 4 MBytes/sec and linear address pointers (only μPD70325
    and μPD70335)

* 16-Bit timer: 2 channels

* Time base counter (20-Bit): 1 channel

* On-chip clock generator

* Programmable wait state function

* Stand-by function (STOP/HALT)

ORDERING INFORMATION

Part Number	Package	External Clock	On-chip ROM	Quality Grade
µPD70320L-8	84-pin PLCC	16 MHz	None	Standard
µPD70322L-8-xxx	84-pin PLCC	16 MHz	Masked ROM	Standard
µPD70320GJ-8-5BG	94-pin plastic QFP	16 MHz	None	Standard
µPD70322GJ-8-xxx-5BG	94-pin plastic QFP	16 MHz	Masked ROM	Standard
µPD70320GJ(A)-8-5BG	94-pin plastic QFP	16 MHz	None	Special
µPD70322GJ(A)-8-xxx-5BG	94-pin plastic QFP	16 MHz	Masked ROM	Special
µPD70330L-8	84-pin PLCC	16 MHz	None	Standard
µPD70332L-8-xxx	84-pin PLCC	16 MHz	Masked ROM	Standard
µPD70330GJ-8-5BG	94-pin plastic QFP	16 MHz	None	Standard
µPD70332GJ-8-xxx-5BG	94-pin plastic QFP	16 MHz	Masked ROM	Standard
µPD70330GJ(A)-8-5BG	94-pin plastic QFP	16 MHz	None	Special
µPD70332GJ(A)-8-xxx-5BG	84-pin plastic QFP	16 MHz	Masked ROM	Special
µPD70325L-8	84-pin PLCC	16 MHz	None	Standard
µPD70325L-10	84-pin PLCC	20 MHz	None	Standard
µPD70325GJ-8-5BG	94-pin plastic QFP	16 MHz	None	Standard
µPD70325GJ-10-5BG	94-pin plastic QFP	20 MHz	None	Standard
µPD70325GJ(A)-9-5BG	94-pin plastic QFP	18 MHz	None	Special
µPD70335L-8	84-pin PLCC	16 MHz	None	Standard
µPD70335L-10	84-pin PLCC	20 MHz	None	Standard
µPD70335GJ-8-5BG	94-pin plastic QFP	16 MHz	None	Standard
µPD70335GJ-10-5BG	94-pin plastic QFP	20 MHz	None	Standard
µPD70335GJ(A)-9-5BG	94-pin plastic QFP	18 MHz	None	Special
µPD70327L-8-xxx	84-pin PLCC	16 MHz	None	Standard
µPD70327GJ-8-xxx-5BG	94-pin plastic QFP	16 MHz	None	Standard
µPD70337L-8-xxx	84-pin PLCC	16 MHz	None	Standard
µPD70337GJ-8-xxx-5BG	94-pin plastic QFP	16 MHz	None	Standard
µPD79011L	84-pin PLCC	16 MHz	RTOS kernel	Standard
µPD79011GJ-5BG	94-pin plastic QFP	16 MHz	RTOS kernel	Standard
µPD79011GJ(A)-5BG	94-pin plastic QFP	16 MHz	RTOS kernel	Special
µPD79021L	84-pin PLCC	16 MHz	RTOS kernel	Standard
µPD79021GJ-5BG	94-pin plastic QFP	16 MHz	RTOS kernel	Standard
µPD79021GJ(A)-5BG	94-pin plastic QFP	16 MHz	RTOS kernel	Special

COMPARISON BETWEEN V25, V35, V25+ and V35+

		V25	V35	V25+	V35+
		uPD70322	uPD70332	uPD70325	uPD70335
DMA func- tions	Transfer processing method	By microprogram		By dedicated hardware	
	Max. transfer rate (at 8 MHz operation)	0.6M bytes/sec	0.8M bytes/sec	4M bytes/sec	5.3M bytes/sec
	DMA requested sampling timing	During instruction execution cycle		During bus cycle	
	DMA service channel	In the internal RAM area		In the special function register	
	Transfer address specification method	Segment method		Linear method	
	Single-step mode execution format	1 DMA transfer/1 instruction execution		1 DMA transfer/1 bus cycle	
	Interrupt request during DMA transfer (demand release mode)	Only NMI to be acknowledged		Not acknowledged	
	Number of waits required for stop control by $\overline{DMARQ}$ (demand release mode)	Not required		2-wait	
	Transfer processing unit	Byte/word	Byte/word	Byte	Byte/word
	TC (terminal counter) set value	DMA transfer times		(DMA transfer times) - 1	
	Terminal count generation timing	TC = 0		TC = FFFFH	
	TC output low-level width	Fixed		Expansion by wait insertion	

(to be continued)

(cont'd)

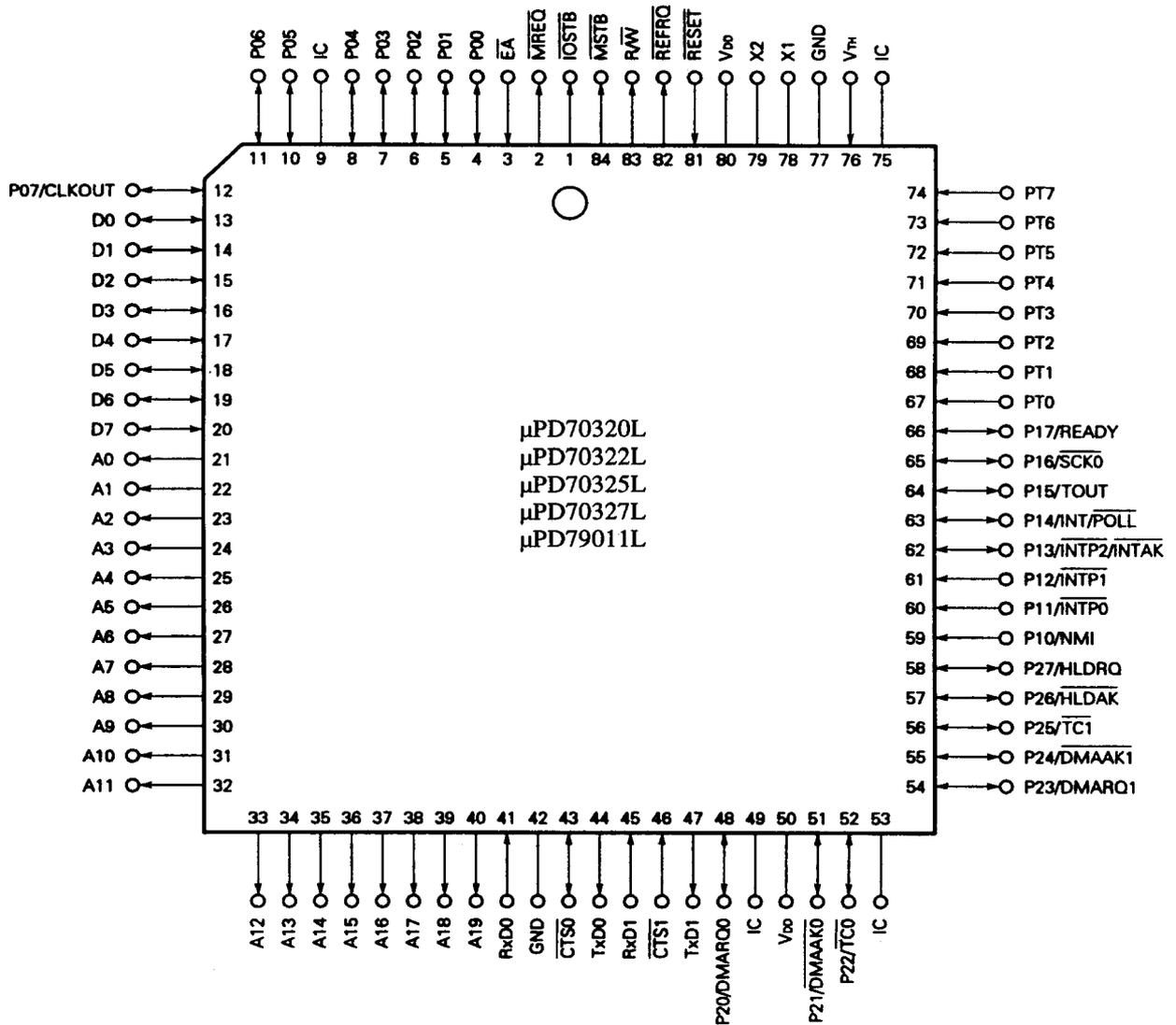|		V25	V35	V25+	V35+
		uPD70322	uPD70332	uPD70325	uPD70335
Serial inter-face	Transmit clock output in the asynchronous mode (channel 0)	Disable		Enable ($\overline{\text{SCKO}}$ pin)	
	Serial error register	Yes		Serial status register	
	Receive buffer full flag	None		In the serial status register	
	Transmit buffer empty flag	None		In the serial status register	
	All sent flag	None		In the serial status register	
Inter-rupt func-tion	Interrupt source register	None		Yes	
Internal ROM for users		Yes		None	
Max. operation frequency		8 MHz		10 MHz	

OUTLINE OF RTOS FUNCTION OF µPD79011 and µPD79021

Item	Description
A variety of system calls	. Task management : 5 types . Synchronization/ communication management : 9 types . Memory management : 2 types . Time management : 2 types . Interrupt management: 7 types 25 types in total
System call interface	. Assembly language . C language (interface library used)
Task management	. Scheduling according to priority levels . Number of tasks: 64 (resident in banks: 6, non-resident in banks: 58) . Priority: 64 levels (tasks resident in banks: 6 levels, tasks not resident in banks: 58 levels)
Synchronization/ communication management	. Synchronizing functions by semaphores (number of semaphores: 256) . Communication functions by mail boxes (number of mail boxes: 256)
Memory management	Management by memory blocks
Time management	By using the on-chip time base counter
Interrupt management	External interrupt controller (uPD71059 or equivalent) can be added.
High speed task switching	By using the on-chip register banks
System calling time	. Tasks resident in banks: 41 to 123 us (when operated at 8 MHz) . Tasks not resident in banks: 41 to 294 us (when operated at 8 MHz)
Hardware configuration	Same as V25 (except for internal ROM contents)
Max. operation frequency	8 MHz

PIN CONFIGURATION (Top View)

84-Pin PLCC

Top-side pins (left to right): P06 (11), P05 (10), IC (9), P04 (8), P03 (7), P02 (6), P01 (5), P00 (4), EA (3), MREQ (2), IOSTB (1), MSTB (84), R/W (83), REFRQ (82), RESET (81), V$_{DD}$ (80), X2 (79), X1 (78), GND (77), V$_{TH}$ (76), IC (75)

Left-side pins:
- P07/CLKOUT — 12
- D0 — 13
- D1 — 14
- D2 — 15
- D3 — 16
- D4 — 17
- D5 — 18
- D6 — 19
- D7 — 20
- A0 — 21
- A1 — 22
- A2 — 23
- A3 — 24
- A4 — 25
- A5 — 26
- A6 — 27
- A7 — 28
- A8 — 29
- A9 — 30
- A10 — 31
- A11 — 32

Center label:
μPD70320L
μPD70322L
μPD70325L
μPD70327L
μPD79011L

Right-side pins:
- 74 — PT7
- 73 — PT6
- 72 — PT5
- 71 — PT4
- 70 — PT3
- 69 — PT2
- 68 — PT1
- 67 — PT0
- 66 — P17/READY
- 65 — P16/SCK0
- 64 — P15/TOUT
- 63 — P14/INT/POLL
- 62 — P13/INTP2/INTAK
- 61 — P12/INTP1
- 60 — P11/INTP0
- 59 — P10/NMI
- 58 — P27/HLDRQ
- 57 — P26/HLDAK
- 56 — P25/TC1
- 55 — P24/DMAAK1
- 54 — P23/DMARQ1

Bottom-side pins (left to right): A12 (33), A13 (34), A14 (35), A15 (36), A16 (37), A17 (38), A18 (39), A19 (40), RxD0 (41), GND (42), CTS0 (43), TxD0 (44), RxD1 (45), CTS1 (46), TxD1 (47), P20/DMARQ0 (48), IC (49), V$_{DD}$ (50), P21/DMAAK0 (51), P22/TC0 (52), IC (53)
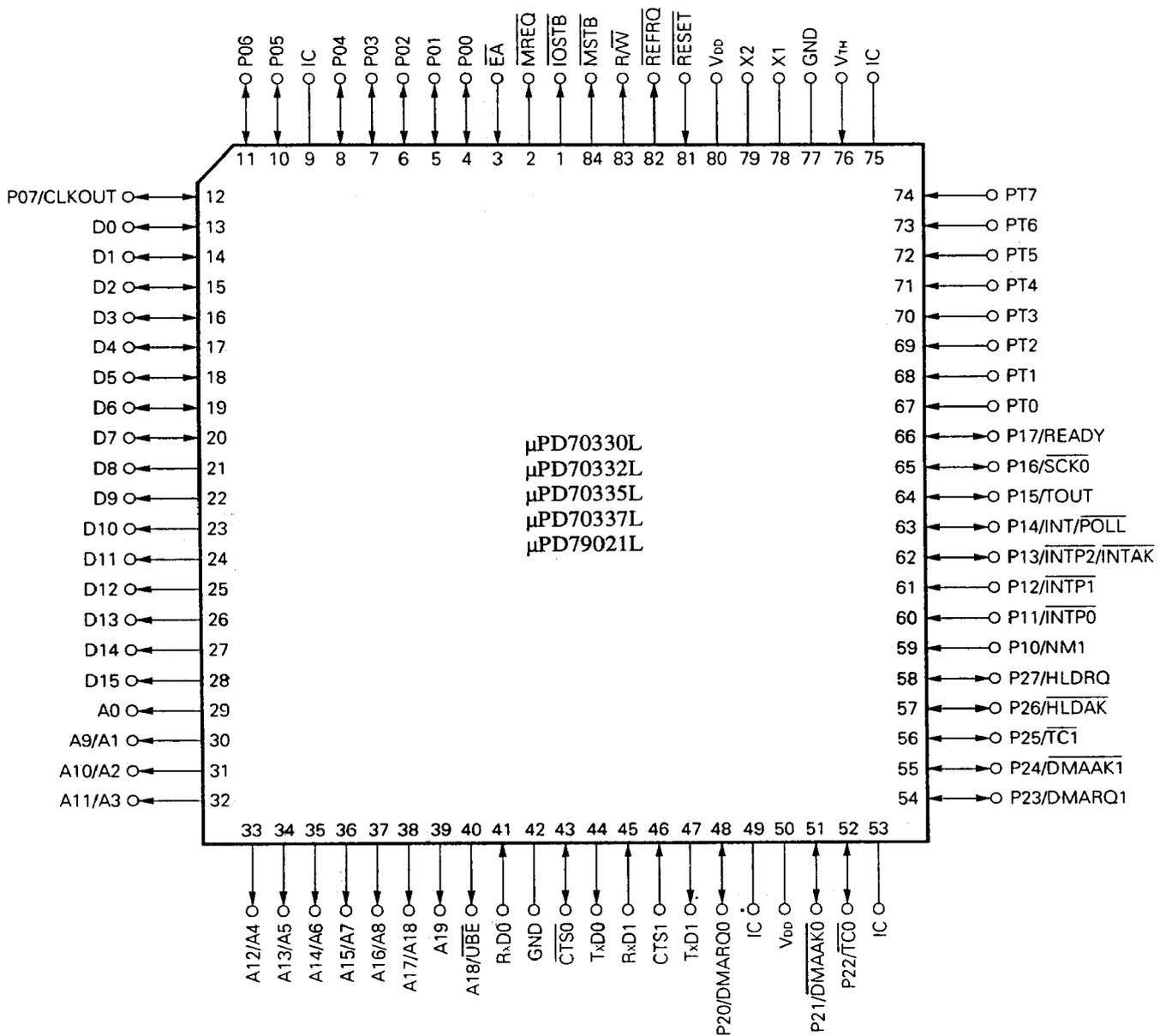
Remarks: IC: Internally Connected

Notes:
* Fix each IC pin to 'H' level via a pull-up resistor from outside
* EA pin should be fixed to low for μPD70320 and μPD70325
* EA pin should be fixed to high for μPD70327 and μPD79011
* Only for μPD70327L: pin no.53 has N/S function

84-pin PLCC
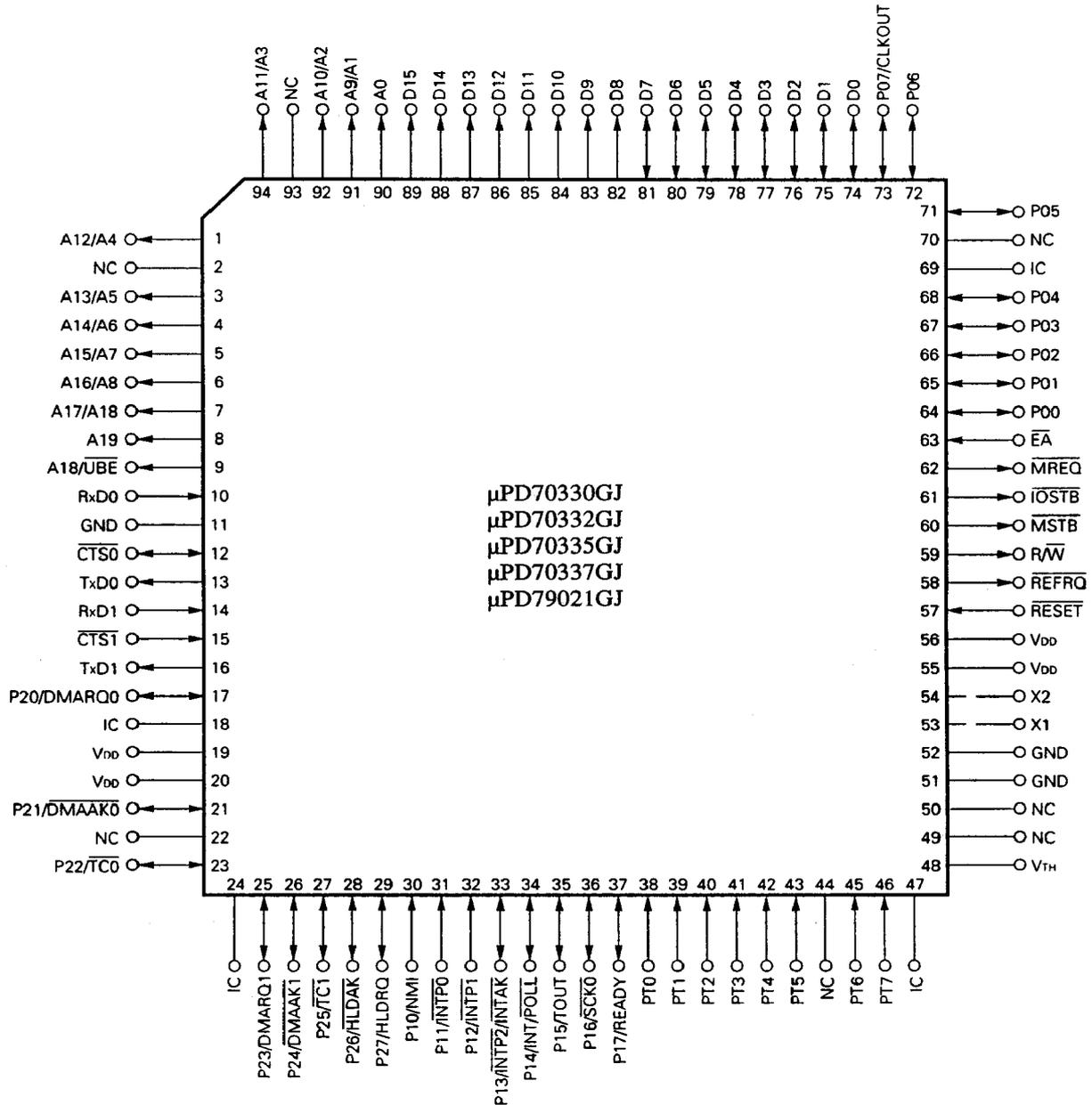
Top pins (left to right): PO6 (11), PO5 (10), IC (9), PO4 (8), PO3 (7), PO2 (6), PO1 (5), PO0 (4), EA (3), MREQ (2), IOSTB (1), MSTB (84), R/W (83), REFRQ (82), RESET (81), V$_{DD}$ (80), X2 (79), X1 (78), GND (77), V$_{TH}$ (76), IC (75)

Left pins:

Pin	Signal
12	PO7/CLKOUT
13	D0
14	D1
15	D2
16	D3
17	D4
18	D5
19	D6
20	D7
21	D8
22	D9
23	D10
24	D11
25	D12
26	D13
27	D14
28	D15
29	A0
30	A9/A1
31	A10/A2
32	A11/A3

Center labels:

μPD70330L
μPD70332L
μPD70335L
μPD70337L
μPD79021L

Right pins:

Pin	Signal
74	PT7
73	PT6
72	PT5
71	PT4
70	PT3
69	PT2
68	PT1
67	PT0
66	P17/READY
65	P16/SCK0
64	P15/TOUT
63	P14/INT/POLL
62	P13/INTP2/INTAK
61	P12/INTP1
60	P11/INTP0
59	P10/NM1
58	P27/HLDRQ
57	P26/HLDAK
56	P25/TC1
55	P24/DMAAK1
54	P23/DMARQ1

Bottom pins (left to right): A12/A4 (33), A13/A5 (34), A14/A6 (35), A15/A7 (36), A16/A8 (37), A17/A18 (38), A19 (39), A18/UBE (40), RxD0 (41), GND (42), CTS0 (43), TxD0 (44), RxD1 (45), CTS1 (46), TxD1 (47), P20/DMARQ0 (48), IC (49), V$_{DD}$ (50), P21/DMAAK0 (51), P22/TC0 (52), IC (53)

Remarks: IC: Internally Connected

Notes: * Fix each IC pin to 'H' level via a resistor from outside, except pin 9 to be fixed to 'L' level
     * EA pin should be fixed to low for μPD70330 and μPD70335
     * EA pin should be fixed to high for μPD70337 and μPD79021
     * Only for μPD70337L: pin no.53 has N/S function

94-Pin Plastic QFP
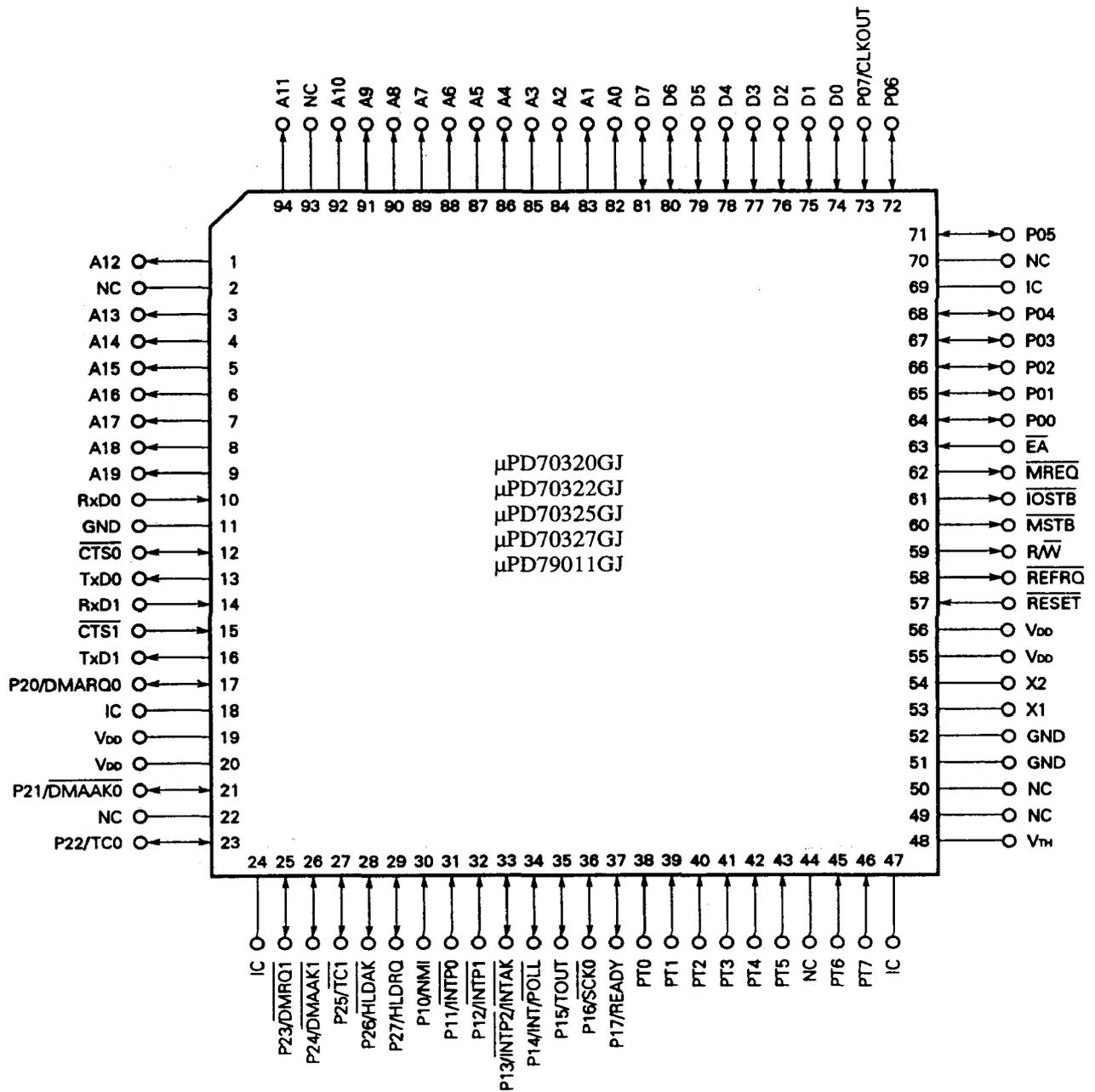
μPD70320GJ
μPD70322GJ
μPD70325GJ
μPD70327GJ
μPD79011GJ

Remarks: IC: Internally Connected
            NC: Non-Connection

Notes: * Fix each IC pin to 'H' level via a pull-up resistor from outside
            * EA pin should be fixed to low for μPD70320 and μPD70325
            * EA pin should be fixed to high for μPD70327 and μPD79011
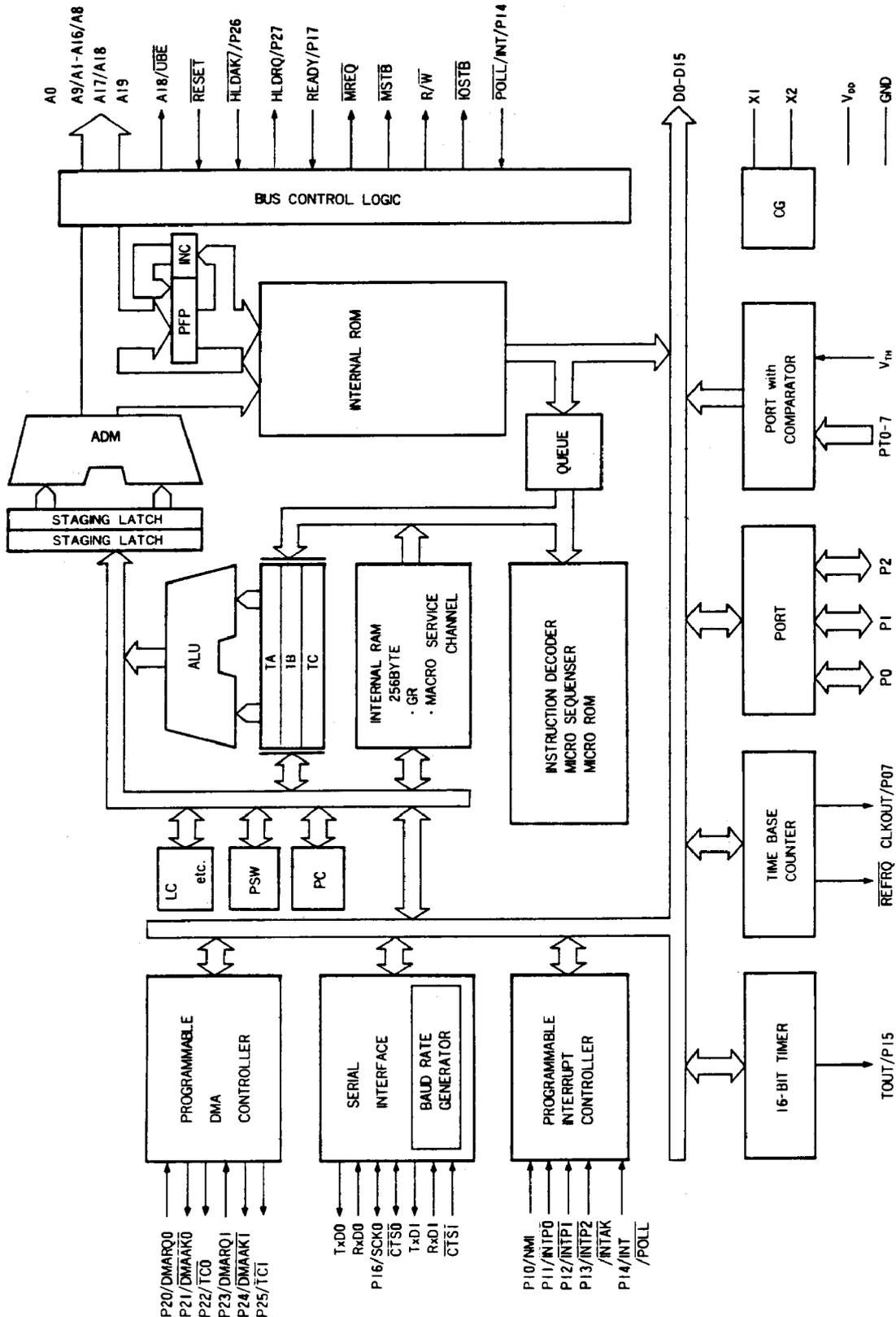   * Only for μPD70327GJ: pin no.24 has N/S function

94-pin plastic QFP

Top pins (left to right, 94–72):
A11/A3, NC, A10/A2, A9/A1, A0, D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0, P07/CLKOUT, P06

Left pins (1–23):
- 1 A12/A4
- 2 NC
- 3 A13/A5
- 4 A14/A6
- 5 A15/A7
- 6 A16/A8
- 7 A17/A18
- 8 A19
- 9 A18/UBE
- 10 RxD0
- 11 GND
- 12 CTS0
- 13 TxD0
- 14 RxD1
- 15 CTS1
- 16 TxD1
- 17 P20/DMARQ0
- 18 IC
- 19 VDD
- 20 VDD
- 21 P21/DMAAK0
- 22 NC
- 23 P22/TC0

Center chip labels:
µPD70330GJ
µPD70332GJ
µPD70335GJ
µPD70337GJ
µPD79021GJ

Right pins (71–48):
- 71 P05
- 70 NC
- 69 IC
- 68 P04
- 67 P03
- 66 P02
- 65 P01
- 64 P00
- 63 EA
- 62 MREQ
- 61 IOSTB
- 60 MSTB
- 59 R/W
- 58 REFRQ
- 57 RESET
- 56 VDD
- 55 VDD
- 54 X2
- 53 X1
- 52 GND
- 51 GND
- 50 NC
- 49 NC
- 48 VTH

Bottom pins (24–47):
- 24 IC
- 25 P23/DMARQ1
- 26 P24/DMAAK1
- 27 P25/TC1
- 28 P26/HLDAK
- 29 P27/HLDRQ
- 30 P10/NMI
- 31 P11/INTP0
- 32 P12/INTP1
- 33 P13/INTP2/INTAK
- 34 P14/INT/POLL
- 35 P15/TOUT
- 36 P16/SCK0
- 37 P17/READY
- 38 PT0
- 39 PT1
- 40 PT2
- 41 PT3
- 42 PT4
- 43 PT5
- 44 NC
- 45 PT6
- 46 PT7
- 47 IC

Remarks: IC: Internally Connected
NC: Non-Connection

Notes:
* Fix each IC pin to 'H' level via a resistor from outside, except pin 9 to be fixed to 'L' level
* EA pin should be fixed to low for µPD70330 and µPD70335
* EA pin should be fixed to high for µPD70337 and µPD79021
* Only for µPD70337GJ: pin no.24 has N/S function

INTERNAL BLOCK DIAGRAM (µPD70320, µPD70322, µPD70325, µPD70327, µPD79011)
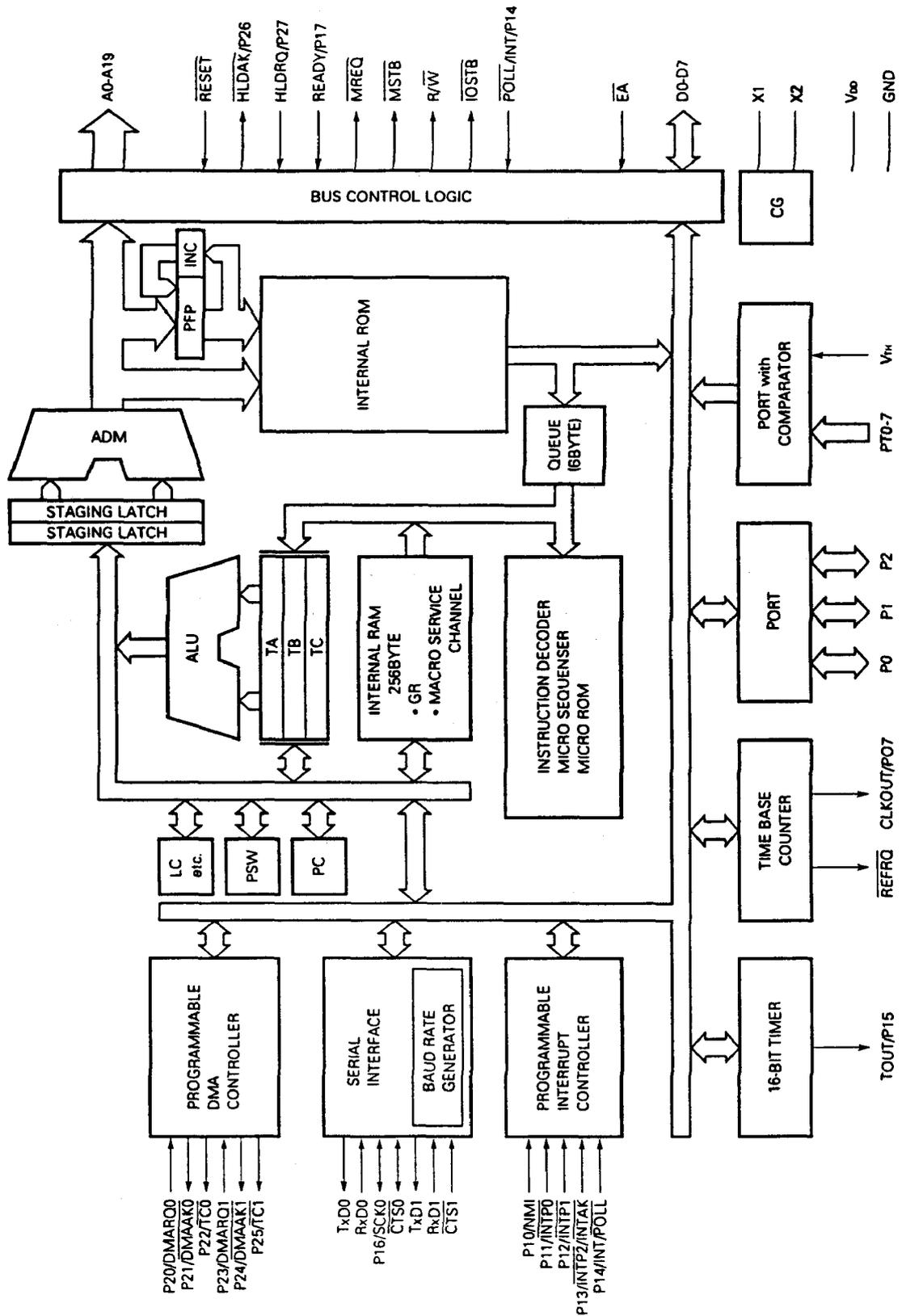
INTERNAL BLOCK DIAGRAM (µPD70330, µPD70332, µPD70335, µPD70337, µPD79021)

1. PIN FUNCTIONS

PORT PINS

Pin Name	I/O	Port Function	Control Function
P00–P06	I/O	Eight-bit bidirectional input/output port for which input or output mode can be specified bitwise.	—
P07/CLKOUT	I/O/O		System clock output
P10/NMI	I	Nonmaskable interrupt request input (input port)	—
P11/INTP0		External interrupt request input and input port	
P12/INTP1			
P13/INTP2/INTAK	I/I/O		INT acknowledge signal output
P14/POLL/INT	I/O/I/I	Bidirectional input/output port and POLL input	External interrupt request input
P15/TOUT	I/O/I	Bidirectional input/output port; input or output mode can be specified bitwise	Timer output
P16/SCK0			Serial clock output
P17/READY	I/O/I		READY input
P20/DMARQ0	I/O/I	Eight-bit bidirectional input/output port; input or output mode can be specified bitwise	DMA request input (CH0)
P21/DMAAK0	I/O/O		DMA acknowledge output (CH0)
P22/TC0			DMA termination output (CH0)
P23/DMARQ1	I/O/I		DMA request input (CH1)
P24/DMAAK1	I/O/O		DMA acknowledge output (CH1)
P25/TC1			DMA termination output (CH1)
P16/HLDAK	I/O/O		HOLD acknowledge output
P27/HLDRQ	I/O/I		HOLD input
PT0–PT7	I	Input port with 8-bit comparator	—

Remark All port pins become input ports after RESET returns high.

When using P13/INTP2/INTAK as an INTAK pin, be sure to pull up the pin to avoid a malfunction of external-interrupt controller after RESET returns high.

PINS OTHER THAN PORTS (μPD70320, μPD70322, μPD70325, μPD70327, μPD79011)

Pin Name	Input/Output	Function
TXD0	Output	Serial data output
TXD1		
RXD0	Input	Serial data input
RXD1		
$\overline{\text{CTS0}}$	Input & output	CTS input in asynchronous mode, receive clock input/output in I/O interface mode
$\overline{\text{CTS1}}$	Input	CTS input
$\overline{\text{REFRQ}}$	Output	DRAM refresh pulse output
V$_{TH}$	Input	Comparator reference voltage input
$\overline{\text{RESET}}$		RESET signal input
$\overline{\text{EA}}$		Input used to set ROM-less Mode
X1		Used to connect crystal for oscillating system clock. External clock is entered by
X2		entering reverse phase clock to both X1 and X2 pins.
D0 to D7	Input & output	8-bit data bus
A0 to A19	Output	20-bit address output
$\overline{\text{MREQ}}$		Output used to indicate that memory bus cycle has been started
$\overline{\text{MSTB}}$		Memory read/memory write strobe output
R/$\overline{\text{W}}$		Read cycle/write cycle ID signal output
$\overline{\text{IOSTB}}$		I/O read/I/O write strobe output
V$_{DD}$		Positive power supply pins. Both pins should be connected.
GND		GND pins. Both pins should be connected.
IC		Internal connect. This pin should be connected at "H" level via a pull-up resistor from outside.

PINS OTHER THAN PORTS (μPD70330, μPD70332, μPD70335, μPD70337, μPD79021)

Pin Name	I/O	Function
TxD0	O	Serial data output
TxD1		
RxD0	I	Serial data input
RxD1		
$\overline{\text{CTS0}}$	I/O	CTS input in asynchronous mode. Receive clock input/output in I/O interface mode.
$\overline{\text{CTS1}}$	I	CTS input
$\overline{\text{REFRQ}}$	O	DRAM refresh pulse output
VTH		Comparator reference voltage input
$\overline{\text{RESET}}$	I	Reset signal input
$\overline{\text{EA}}$		Input to set ROM less mode
X1		Crystal connection pins for system clock oscillator.
X2		External clock is input with opposing phases to the X1 and X2 pins.
D0–D15	I/O	8-bit data bus
A0	O	Select low-order memory bank.
$\overline{\text{UBE}}$		Select high-order memory bank.
A1–A19		Output 19-bit address
$\overline{\text{MREQ}}$		Output indicating that memory bus cycle is started.
$\overline{\text{MSTB}}$		Memory read or memory write strobe output.
R/$\overline{\text{W}}$		Read or write cycle identification signal output.
$\overline{\text{IOSTB}}$		I/O read or I/O write strobe output.
VDD		Positive power supply pin. Connect both the VDD pins.
GND		GND pin. Connect both the GND pins.
IC		Internal connect. Fix to the high level via pull-up resistor from external.

2. INSTRUCTION SET

2.1 ADDITIONAL INSTRUCTIONS TO THE μPD70108/μPD70116

(1) Conditional branch instruction

- BTCLR: Special function register bit test instruction

    When BTCLR is executed, the target special function register bit is cleared if the bit is set to 1, and a branch is made to short-label described in the operand. If the bit is set to 0, the next instruction is executed. PSW does not change.

(Description format)

Mnemonic	Operand		
	Special function register address	Special function register bit	Branch destination
BTCLR	sfr	imm3	short-label

(2) Interrupt instructions

- RETRBI: Register bank return instruction

    The RETRBI instruction is used to return from the interrupt service routine using the register bank switching function. It cannot be used to return from a vectored interrupt.

(Description format)

Mnemonic	Operand
RETRBI	None

- FINT: Instruction to inform the interrupt controller that interrupt service terminates

    If an interrupt other than NMI, INT, or software interrupt is used, execute the FINT instruction before a return instruction from the interrupt. Do not use the FINT instruction in NMI, INT, or software interrupts.

(Description format)

Mnemonic	Operand
FINT	None

(3) CPU instruction
- STOP: Transition instruction to the STOP state

(Description format)

Mnemonic	Operand
STOP	None

(4) Register bank change instruction

BRKCS: Register bank change instruction
The current register bank is changed to the register bank indicated by the contents of the low-order three bits of the 16-bit register described in the operand. A branch is taken to the address obtained from PS prestored in the new register bank and vector PC. To return from the new register bank, use the RETRBI instruction.

(Description format)

Mnemonic	Operand
BRKCS	reg16

TSKSW: Register bank change instruction
The current register bank is changed to the register bank indicated by the contents of the three bits of the 16-bit register described in the operand. A branch is taken to the address obtained from PS prestored in the new register bank and the PC save area.

(Description format)

Mnemonic	Operand
TSKSW	reg16

(5) Data transfer instructions

MOVSPA: SS and SP transfer instruction
The SS and SP values before register banks are changed are transferred to SS and SP in the new register bank indicated.

(Description format)

Mnemonic	Operand
MOVSPA	None

MOVSPB: SS and SP transfer instruction
The SS and SP values in the current register bank are transferred to SS and SP in the new register bank indicated by the contents of the low-order three bits of the 16-bit register described in the operand.

(Description format)

Mnemonic	Operand
MOVSPB	reg16

(6) Mode change instructions

o BRKS ...... Change to S mode   instruction
(only for μPD70327, 70337)

Switches the operation mode to S mode and generates a vectored interrupt.

The RETI instruction is used to return from the instruction (returns to operating mode prior to execution of the BRKS instruction).

(Descriptive format)

Mnemonic	Operand
BRKS	imm8 (≠ 3)

o BRKN ...... Change to N mode   instruction
(only for μPD70327, 70337)

Switches the operating mode to N mode and generates a vectored interrupt.

The RETI instruction is used to return from the instruction (returns to operating mode prior to execution of the BRKN instruction).

(Descriptive format)

Mnemonic	Operand
BRKN	imm8 (≠ 3)

When the following instructions of the μPD70108/μPD70116 instruction set are used note the following:

* { Input/output:
  instruction
  primitive
  input/output
  instruction

If the PSW $\overline{IBRK}$ flag is reset to 0, the instruction is not executed and an interrupt occurs. To use the input/output instruction, set the $\overline{IBRK}$ flag to 1.

* FPO instruction: The instruction is not executed and an interrupt occurs.

2.2 INSTRUCTION SET OPERATION

Table 2-1 Operand Identifier

Identifier	Description
reg	8/16-bit general-purpose register
reg8	8-bit general-purpose register
reg16	16-bit general-purpose register
dmem	8/16-bit memory location
mem	8/16-bit memory location
mem8	8-bit memory location
mem16	16-bit memory location
mem32	32-bit memory location
sfr	8-bit special function register location
imm	Constant in the range of 0-FFFFH
imm3	Constant in the range of 0-7
imm4	Constant in the range of 0-FH
imm8	Constant in the range of 0-FFH
imm16	Constant in the range of 0-FFFFH
acc	Register AW or AL
sreg	Segment register
src-table	256-byte translation table name
src-block	Name of block addressed in register IX
dst-block	Name of block addressed in register IY
near-proc	Procedure in the current program segment
far-proc	Procedure in another program segment
near-label	Label in the current program segment
short-label	Label in the range of –128 to +127 bytes from the instruction end
far-label	Label in another program segment
memptr16	Work containing location offset in the current program segment to which control is to be transferred
memptr32	Double-word containing the segment base address and location offset in another program segment to which control is to be transferred
regptr16	16-bit general-purpose register containing location offset in another program segment to which control is to be transferred
pop-value	Number of bytes discarded from stack (0 to 64K, normally even-number)
fp-op	Immediate value to determine the instruction code of an external floating-point operation chip
R	Register set

Table 2-2 Operand Code Identifier

Identifier	Description
W	Word/byte field (0–1)
reg	Register field (000–111)
mem	Memory field (000–111)
mod	Mode field (00–10)
S:W	When S:W=01, data=16 bits; when S:W≠01, data 8 bits When S:W=11, the byte data sign is extended and a 16-bit operand is made
X,XXX,YYY, ZZZ	Data to determine the instruction code of an external floating-point operation chip

Table 2-3 Operation Identifier

Identifier	Description
AW	Accumulator (16 bits)
AH	Accumulator (upper byte)
AL	Accumulator (lower byte)
BW	Register BW (16 bits)
CW	Register CW (16 bits)
CL	Register CW (lower byte)
DW	Register DW (16 bits)
SP	Stack pointer (16 bits)
PC	Program counter (16 bits)
PSW	Program status word (16 bits)
IX	Index register (source) (16 bits)
IY	Index register (destination) (16 bits)
PS	*Program segement register (16 bits)*
DS1	Data segment 1 register (16 bits)
DS0	Data segment 0 register (16 bits)
SS	Stack segement register (16 bits)
AC	Auxiliary carry flag
CY	Carry flag
P	Parity flag
S	Sign flag
Z	Zero flag
DIR	Direction flag
IE	Interrupt enable flag

Identifier	Description
V	Overflow flag
BRK	Break flag
MD	Mode flag
(...)	Contents of memory indicated in ( )
disp	Displacement (8 or 16 bits)
ext-disp8	16 bits of 8-bit displacement with extended sign
temp	Temporary register (8, 16, or 32 bits)
tmpcy	Temporary carry flag (one bit)
seg	Immediate segment data (16 bits)
offset	Immediate offset data (16 bits)
←	Transfer direction
+	Addition
−	Subtraction
×	Multiplication
÷	Division
%	Modulo
∧	AND
∨	OR
∀	Exclusive OR
xxH	2-digit hexadecimal number
xxxxH	4-digit hexadecimal number

Table 2-4 Flag Operation Identifier

Identifier	Description
(blank)	No change
0	Cleared to 0
1	Set to 1
×	Set to 1 or cleared according to the result
U	Undefined
R	The previously saved value is restored

**Table 2-5 Selection of 8- or 16-Bit General
Purpose Register**

reg	W = 0	W = 1
000	AL	AW
001	CL	CW
010	DL	DW
011	BL	BW
100	AH	SP
101	CH	BP
110	DH	IX
111	BH	IY

Table 2-6 Segment Register Selection

sreg	
00	DS1
01	PS
10	SS
11	DS0

Table 2-7 Number of Clocks for Each Memory Addressing

mod mem	00	Clocks	01	Clocks	10	Clocks
000	BW + IX	3	BW + IX + disp8	3	BW + IX + disp16	4
001	BW + IY	3	BW + IY + disp8	3	BW + IY + disp16	4
010	BP + IX	3	BP + IX + disp8	3	BP + IX + disp16	4
011	BP + IY	3	BP + IY + disp8	3	BP + IY + disp16	4
100	IX	3	IX + disp8	3	IX + disp16	4
101	IY	3	IY + disp8	3	IY + disp16	4
110	Direct address	3	BP + disp8	3	BP + disp16	4
111	BW	3	BW + disp8	3	BW + disp16	4

In memory operand, the number of clocks varies depending on the addressing mode. Apply the numeric values listed in Table 2-8 to those written as "EA" in the list of the number of clocks.

"T" denotes the number of wait states. Apply any number of wait states from 0 (no wait).

The instruction fetch cycle is not counted as the number of clocks.

There are some branch instructions for which such description as the example below is provided. The description indicates as follows:

Example 15/8 .... 15: the number of clock cycles when branched
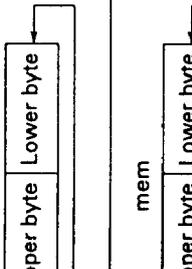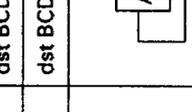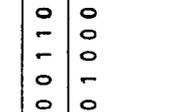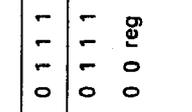8: the number of clock cycles when not branched

2.8 INSTRUCTION SET TABLE

Group	Mnemonic	Operand	Operation Code (7 6 5 4 3 2 1 0 / 7 6 5 4 3 2 1 0)	Number of bytes	Operation	Flags AC	CY	V	P	S	Z
Data transfer	MOV	reg, reg	1 0 0 0 1 0 1 W / 1 1 reg reg	2	reg ← reg						
		mem, reg	1 0 0 0 1 0 0 W / mod reg mem	2 – 4	(mem) ← reg						
		reg, mem	1 0 0 0 1 0 1 W / mod reg mem	2 – 4	reg ← (mem)						
		mem, imm	1 1 0 0 0 1 1 W / mod 0 0 0 mem	3 – 6	(mem) ← imm						
		reg, imm	1 0 1 1 W reg	2 – 3	reg ← imm						
		acc, dmem	1 0 1 0 0 0 0 W	3	When W=0, AL ← (dmem) / When W=1, AH ← (dmem+1), AL ← (dmem)						
		dmem, acc	1 0 1 0 0 0 1 W	3	When W=0, (dmem) ← AL / When W=1, (dmem+1) ← AH, (dem) ← AL						
		sreg, reg16	1 0 0 0 1 1 1 0 / 1 1 0 sreg reg	2	sreg ← reg16 sreg: SS, DS0, DS1						
		sreg, mem16	1 0 0 0 1 1 1 0 / mod 0 sreg mem	2 – 4	sreg ← (mem16) sreg: SS, DS0, DS1						
		reg16, sreg	1 0 0 0 1 1 0 0 / 1 1 0 sreg reg	2	reg16 ← sreg						
		mem16, sreg	1 0 0 0 1 1 0 0 / mod 0 sreg mem	2 – 4	(mem16) ← sreg						
		DS0, reg16, mem32	1 1 0 0 0 1 0 1 / mod reg mem	2 – 4	reg16 ← (mem32) / DS0 ← (mem32-2)						
		DS1, reg16, mem32	1 1 0 0 0 1 0 0 / mod reg mem	2 – 4	reg16 ← (mem32) / DS1 ← (mem32-2)						
		AH, PSW	1 0 0 1 1 1 1 1	1	AH ← S, Z, F1, AC, F0, P, IBRK, CY						
		PSW, AH	1 0 0 1 1 1 1 0	1	S, Z, F1, AC, F0, P, IBRK, CY ← AH	×	×	×	×	×	×
	LDEA	reg16, mem16	1 0 0 0 1 1 0 1 / mod reg mem	2 – 4	reg16 ← mem16						
	TRANS	src-table	1 1 0 1 0 1 1 1	1	AL ← (BW+AL)						
	XCH	reg, 'reg	1 0 0 0 0 1 1 W / 1 1 reg reg	2	reg ↔ reg						
		mem, reg / reg, mem	1 0 0 0 0 1 1 W / mod reg mem	2 – 4	(mem) ↔ reg						
		AW, reg16 / reg16, AW	1 0 0 1 0 reg	1	AW ↔ reg16						
	MOVSPA [Note]		0 0 0 0 1 1 1 1 / 0 0 1 0 0 1 0 1	2	SS and SP of the new register bank ← SS and SP of the old register bank						
	MOVSPB [Note]	reg16	0 0 0 0 1 1 1 1 / 1 0 0 1 0 1 0 1 / 1 1 1 1 1 reg	3	SS and SP of the new register bank by reg16 ← SS and SP of the old register						

Note New added instruction from the µPD70108/70116

Group	Mnemonic	Operand	Operation Code	Number of bytes	Operation	AC	CY	V	P	S	Z
Repeat prefix	REPC		0 1 1 0 0 1 0 1	1	While CW≠0, primitive block transfer instruction of the subsequent byte is executed and CW is decremented by one. If an interrupt is held, it is processed. When CY≠1, loop is terminated						
	REPNC		0 1 1 0 0 1 0 0	1	Same as above When CY≠0, loop is terminated.						
	REP REPE REPZ		1 1 1 1 0 0 1 1	1	While CW≠0, primitive block transfer instruction of the subsequent byte is executed and CW is decremented by one. If an interrupt is held, it is processed. When the primitive block transfer instruction is CMPBK or CMPM and Z≠1, loop is terminated.						
	REPNE REPNZ		1 1 1 1 0 0 1 0	1	Same as above When Z≠0, loop is terminated.						
Primitive block transfer	MOVBK	dst-block, src-block	1 0 1 0 0 1 0 W	1	When W=0, (IY) ← (IX) DIR=0: IX←IX+1, IY←IY+1 DIR=1: IX←IX-1, IY←IY-1 When W=1, (IY+1, IY)←(IX+1, IX) DIR=0: IX←IX+2, IY←IY+2 DIR=1: IX←IX-2, IY←IY-2						
	CMPBK	src-block, dst-block	1 0 1 0 0 1 1 W	1	When W=0, (IX) – (IY) DIR=0: IX←IX+1, IY←IY+1 DIR=1: IX←IX-1, IY←IY-1 When W=1, (IX+1, IX) – (IY+1, IY) DIR=0: IX←IX+2, IY←IY+2 DIR=1: IX←IX-2, IY←IY-2	x	x	x	x	x	x
	CMPM	dst-block	1 0 1 0 1 1 1 W	1	When W=0, AL – (IY) DIR=0: IY←IY+1; DIR=1: IY←IY-1 When W=1 AW – (IY+1,IY) DIR=0: IY←IY+2; DIR=1: IY←IY-2	x	x	x	x	x	x
	LDM	src-block	1 0 1 0 1 1 0 W	1	WHen W=0, AL ← (IX) DIR=0: IX←IX+1; DIR=1: IX←IX-1 When W=1, AW ← (IX+1, IX) DIR=0: IX←IX+2; DIR=1: IX←IX-2						

Group	Mnemonic	Operand	Operation Code 7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	Number of bytes	Operation	AC	CY	V	P	S	Z
Primitive block transfer	STM	dst-block	1 0 1 0 1 0 1 W		1	When W=0, (IY) ← AL DIR=0: IY ← IY+1; DIR=1: IY ← IY−1 When W=1 (IY+1, IY) ← AW DIR=0: IY ← IY+2; DIR=1: IY ← IY−2						
Bit field operation	INS	reg8, reg8	0 0 0 0 1 1 1 1 1 1 reg reg	0 0 1 1 0 0 0 1	3	16-bit field ← AW						
		reg8, imm4	0 0 0 0 1 1 1 1 1 1 0 0 0 reg	0 0 1 1 1 0 0 1	4	16-bit field ← AW						
	EXT	reg8, reg8	0 0 0 0 1 1 1 1 1 1 reg reg	0 0 1 1 0 0 1 1	3	AW ← 16-bit field						
		reg8, imm4	0 0 0 0 1 1 1 1 1 1 0 0 0 reg	0 0 1 1 1 0 1 1	4	AW ← 16-bit field						
Input/output	IN Note	acc, imm8	1 1 1 0 0 1 0 W		2	When W=0, AL ← (imm8) When W=1, AH ← (imm8+1), AL ← (imm8)						
		acc, DW	1 1 1 0 1 1 0 W		1	When W=0, AL ← (DW) When W=1, AH ← (DW+1), AL ← (DW)						
	OUT Note	imm8, acc	1 1 1 0 0 1 1 W		2	When W=0, (imm8) ← AL When W=1, (imm8+1) ← AH, (imm8) ← AL						
		DW, acc	1 1 1 0 1 1 1 W		1	When W=0, (DW) ← AL When W=1, (DW+1) ← AH, (DW) ← AL						
Primitive input/output	INM Note	dst-block, DW	0 1 1 0 1 1 0 W		1	When W=0, (IY) ← (DW) DIR=0: IY ← IY+1; DIR=1: IY ← IY−1 When W=1, (IY+1, IY) ← (DW+1, DW) DIR=0: IY ← IY+2; DIR=1: IY ← IY−2						
	OUTM Note	DW, src-block	0 1 1 0 1 1 1 W		1	When W=0, (DW) ← (IX) DIR=0: IX ← IX+1; DIR=1: IX ← IX−1 When W=1, (DW+1, DW) ← (IX+1, IX) DIR=0: IX ← IX+2; DIR=1: IX ← IX−2						

Note When $\overline{\text{IBRK}}$=0, a software interrupt automatically occurs, and the instruction is not executed.

Group	Mnemonic	Operand	Operation Code (7 6 5 4 3 2 1 0 / 7 6 5 4 3 2 1 0)		Number of bytes	Operation	Flags AC	CY	V	P	S	Z
Addition and subtraction	ADD	reg, reg	0 0 0 0 0 0 1 W	1 1 reg reg	2	reg ← reg+reg	x	x	x	x	x	x
		mem, reg	0 0 0 0 0 0 0 W	mod reg mem	2 – 4	(mem) ← (mem)+reg	x	x	x	x	x	x
		reg, mem	0 0 0 0 0 0 1 W	mod reg mem	2 – 4	reg ← reg+(mem)	x	x	x	x	x	x
		reg, imm	1 0 0 0 0 0 1 W	1 1 0 0 0 reg	3 – 4	reg ← reg+imm	x	x	x	x	x	x
		mem, imm	1 0 0 0 0 0 S W	mod 0 0 0 mem	3 – 6	(mem) ← (mem)+imm	x	x	x	x	x	x
		acc, imm	0 0 0 0 0 0 1 0 W		2 – 3	When W=0, AL ← AL+imm / When W=1, AW ← AW+imm	x	x	x	x	x	x
	ADDC	reg, reg	0 0 0 1 0 0 1 W	1 1 reg reg	2	reg ← reg+reg+CY	x	x	x	x	x	x
		mem, reg	0 0 0 1 0 0 0 W	mod reg mem	2 – 4	(mem) ← (mem)+reg+CY	x	x	x	x	x	x
		reg, mem	0 0 0 1 0 0 1 W	mod reg mem	2 – 4	reg ← reg+(mem)+CY	x	x	x	x	x	x
		reg, imm	1 0 0 0 0 0 S W	1 1 0 1 0 reg	3 – 4	reg ← reg+imm+CY	x	x	x	x	x	x
		mem, imm	1 0 0 0 0 0 S W	mod 0 1 0 mem	3 – 6	(mem) ← (mem)+imm+CY	x	x	x	x	x	x
		acc, imm	0 0 0 1 0 0 1 0 W		2 – 3	When W=0, AL ← AL+imm+CY / When W=1, AW ← AW+imm+CY	x	x	x	x	x	x
	SUB	reg, reg	0 0 1 0 1 0 1 W	1 1 reg reg	2	reg ← reg-reg	x	x	x	x	x	x
		mem, reg	0 0 1 0 1 0 0 W	mod reg mem	2 – 4	(mem) ← (mem)-reg	x	x	x	x	x	x
		reg, mem	0 0 1 0 1 0 1 W	mod reg mem	2 – 4	reg ← reg-(mem)	x	x	x	x	x	x
		reg, imm	1 0 0 0 0 0 S W	1 1 1 0 1 reg	3 – 4	reg ← reg-imm	x	x	x	x	x	x
		mem, imm	1 0 0 0 0 0 S W	mod 1 0 1 mem	3 – 6	(mem) ← (mem)-imm	x	x	x	x	x	x
		acc, imm	0 0 1 0 1 0 1 0 W		2 – 3	When W=0, AL ← AL-imm / When W=1, AW ← AW-imm	x	x	x	x	x	x
	SUBC	reg, reg	0 0 0 1 1 0 1 W	1 1 reg reg	2	reg ← reg-reg-CY	x	x	x	x	x	x
		mem, reg	0 0 0 1 1 0 0 W	mod reg mem	2 – 4	(mem) ← (mem)-reg-CY	x	x	x	x	x	x
		reg, mem	0 0 0 1 1 0 1 W	mod reg mem	2 – 4	reg ← reg-(mem)-CY	x	x	x	x	x	x
		reg, imm	1 0 0 0 0 0 S W	1 1 0 1 1 reg	3 – 4	reg ← reg-imm-CY	x	x	x	x	x	x
		mem, imm	1 0 0 0 0 0 S W	mod 0 1 1 mem	3 – 6	(mem) ← (mem)-imm-CY	x	x	x	x	x	x
		acc, imm	0 0 0 1 1 1 0 W		2 – 3	When W=0, AL ← AL-imm-CY / When W=1, AW ← AW-imm-CY	x	x	x	x	x	x

Group	Mnemonic	Operand	Operation Code		Number of bytes	Operation	AC	CY	V	P	S	Z
BCD operation	ADD4S		`0000 1111`	`0010 0000`	2	dst BCD string ← dst BCD string + src BCD string (Note)	U	x	U	U	U	x
	SUB4S		`0000 1111`	`0010 0010`	2	dst BCD string ← dst BCD string − src BCD string (Note)	U	x	U	U	U	x
	CMP4S		`0000 1111`	`0010 0110`	2	dst BCD string − src BCD string (Note)	U	x	U	U	U	x
	ROL4	reg8	`0000 1111` `0010 1000`	`1100 0 reg`	3	ALₗ ↔ reg (Upper byte / Lower byte)						
		mem8	`0000 1111` `0010 1000`	`mod 0 0 0 mem`	3 – 5	ALₗ ↔ mem (Upper byte / Lower byte)						
	ROR4	reg8	`0000 1111` `0010 1010`	`1100 0 reg`	3	ALₗ ↔ reg (Upper byte / Lower byte)						
		mem8	`0000 1111` `0010 1010`	`mod 0 0 0 mem`	3 – 5	ALₗ ↔ mem (Upper byte / Lower byte)						
Increment and decrement	INC	reg8	`1111 1110`	`1100 0 reg`	2	reg8 ← reg8+1	x		x	x	x	x
		mem	`1111 111 W`	`mod 0 0 0 mem`	2 – 4	(mem) ← (mem)+1	x		x	x	x	x
		reg16	`0100 0 reg`		1	reg16 ← reg16+1	x		x	x	x	x
	DEC	reg8	`1111 1110`	`1100 1 reg`	2	reg8 ← reg8−1	x		x	x	x	x
		mem	`1111 111 W`	`mod 0 0 1 mem`	2 – 4	(mem) ← (mem)−1	x		x	x	x	x
		reg16	`0100 1 reg`		1	reg16 ← reg16−1	x		x	x	x	x

n: Half of the number of BCD digits

Note: The number of BCD digits is specified in the CL register. CL can be set in the range of 1 to 254.

Group	Mnemonic	Operand	Operation Code 7 6 5 4 3 2 1 0	Operation Code 7 6 5 4 3 2 1 0	Number of bytes	Operation	AC	CY	V	P	S	Z
Multiplication	MULU	reg8	1 1 1 1 0 1 1 0	1 1 1 1 1 0 0 reg	2	AW ← AL × reg8 AH=0 CY←0, V←0 AH≠0: CY←1, V←1	U	x	x	U	U	U
		mem8	1 1 1 1 0 1 1 0	mod 1 0 0 mem	2 – 4	AW ← AL × (mem8) AH=0 CY←0, V←0 AH≠0: CY←1, V←1	U	x	x	U	U	U
		reg16	1 1 1 1 0 1 1 1	1 1 1 1 1 0 0 reg	2	DW, AW ← AW × reg16 DW=0 CY←0, V←0 DW=1: CY←1, V←1	U	x	x	U	U	U
		mem16	1 1 1 1 0 1 1 1	mod 1 0 0 mem	2 – 4	DW, AW ← AW × (mem16) DW=0 CY←0, V←0 DW=1: CY←1, V←1	U	x	x	U	U	U
	MUL	reg8	1 1 1 1 0 1 1 0	1 1 1 1 1 0 1 reg	2	AW ← AL × reg8 AH=AL sign extension: CY←0, V←0 AH≠AL sign extension: CY←1, V←1	U	x	x	U	U	U
		mem8	1 1 1 1 0 1 1 0	mod 1 0 1 mem	2 – 4	AW ← AL × (mem8) AH=AL sign extension: CY←0, V←0 AH≠AL sign extension: CY←1, V←1	U	x	x	U	U	U
		reg16	1 1 1 1 0 1 1 1	1 1 1 1 1 0 1 reg	2	DW, AW ← AW × reg16 DW=AW sign extension: CY←0, V←0 DW≠AW sign extension: CY←1, V←1	U	x	x	U	U	U
		mem16	1 1 1 1 0 1 1 1	mod 1 0 1 mem	2 – 4	DW, AW ← AW × (mem16) DW=AW sign extension: CY←0, V←0 DW≠AW sign extension: CY←1, V←1	U	x	x	U	U	U
		reg16, (reg16)Note, imm8	0 1 1 0 1 0 1 1	1 1 reg reg	3	reg16 ← reg16 × imm8 Product ≤ 16 bits: CY←0, V←0 Product > 16 bits: CY←1, V←1	U	x	x	U	U	U
		reg16, mem16, imm8	0 1 1 0 1 0 1 1	mod reg mem	3 – 5	reg16 ← (mem16) × imm8 Product ≤ 16 bits: CY←0, V←0 Product > 16 bits: CY←1, V←1	U	x	x	U	U	U
		reg16, (reg16)Note, imm8	0 1 1 0 1 0 0 1	1 1 reg reg	4	reg16 ← reg16 × imm16 Product ≤ 16 bits: CY←0, V←0 Product > 16 bits: CY←1, V←1	U	x	x	U	U	U
		reg16, mem16, imm8	0 1 1 0 1 0 0 1	mod reg mem	4 – 6	reg16 ← (mem16) × imm16 Product ≤ 16 bits: CY←0, V←0 Product > 16 bits: CY←1, V←1	U	x	x	U	U	U

Note The second operand may be omitted. If it is omitted, the same register as the first operand is assumed to be specified.

Group	Mnemonic	Operand	Operation Code (7 6 5 4 3 2 1 0 / 7 6 5 4 3 2 1 0)		Number of bytes	Operation	Flags					
							AC	CY	V	P	S	Z
Unsigned division	DIVU	reg8	1 1 1 1 0 1 1 0	1 1 1 1 0 reg	2	temp ← AW When temp + reg8 ≤ FFH, AH ← temp%reg8, AL ← temp + reg8 When temp + reg8 > FFH, (SP-1, SP-2) ← PSW, (SP-3, SP-4) ← PS (SP-5, SP-6) ← PC, SP ← SP-6 IE ← 0, BRK ← 0, PS ← (3, 2), PC ← (1, 0)	U	U	U	U	U	U
		mem8	1 1 1 1 0 1 1 0	mod 1 1 0 mem	2 – 4	temp ← AW When temp + (mem8) ≤ FFH, AH ← temp%(mem8), AL ← temp + (mem8) When temp + (mem8) > FFH, (SP-1, SP-2) ← PSW, (SP-3, SP-4) ← PS (SP-5, SP-6) ← PC, SP ← SP-6 IE ← 0, BRK ← 0, PS ← (3, 2), PC ← (1, 0)	U	U	U	U	U	U
		reg16	1 1 1 1 0 1 1 1	1 1 1 1 0 reg	2	temp ← DW, AW When temp + reg16 ≤ FFFFH, DW ← temp%reg16, AW ← temp + reg16 When temp + reg16 > FFFFH, (SP-1, SP-2) ← PSW, (SP-3, SP-4) ← PS (SP-5, SP-6) ← PC, SP ← SP-6 IE ← 0, BRK ← 0, PS ← (3, 2), PC ← (1, 0)	U	U	U	U	U	U
		mem16	1 1 1 1 0 1 1 1	mod 1 1 0 mem	2 – 4	temp ← DW, AW When temp + (mem16) ≤ FFFFH, DW ← temp%(mem16), AW ← temp + (mem16) When temp + (mem16) > FFFFH, (SP-1, SP-2) ← PSW, (SP-3, SP-4) ← PS (SP-5, SP-6) ← PC, SP ← SP-6 IE ← 0, BRK ← 0, PS ← (3, 2), PC ← (1, 0)	U	U	U	U	U	U

Group	Mnemonic	Operand	Operation Code (7 6 5 4 3 2 1 0)	Number of bytes	Operation	AC	CY	V	P	S	Z
BCD adjustment	ADJBA		0 0 1 1 0 1 1 1	1	When AL∧0FH>9 or AC=1, AL←AL+6 AH←AH+1, AC←1, CY←AC, AL←AL∧0FH	x	x	U	U	U	U
	ADJ4A		0 0 1 0 0 1 1 1	1	When AL∧0FH>9 or AC=1, AL←AL+6 AC←1 When AL>9FH or CY=1 AL←AL+60H, CY←1	x	x	U	x	x	x
	ADJBS		0 0 1 1 1 1 1 1	1	When AL∧0FH>9 or AC=1, AL←AL-6, AH←AH-1, AC←1 CY←AC, AL←AL∧0FH	x		U	U	U	U
	ADJ4S		0 0 1 0 1 1 1 1	1	When AL∧0FH>9 or AC=1, AL←AL-6, AC←1 When AL>9FH or CY=1 AL←AL-60H, CY←1	x	x	U	x	x	x
Data conversion	CVTBD		1 1 0 1 0 1 0 0 / 0 0 0 0 1 0 1 0	2	AH←AL÷0AH, AL←AL%0AH	U	U	U	x	x	x
	CVTDB		1 1 0 1 0 1 0 1 / 0 0 0 0 1 0 1 0	2	AL←AH×0AH+AL, AH←0	U	U	U	x	x	x
	CVTBW		1 0 0 1 1 0 0 0	1	When AL<80H, AH←0; otherwise, AH←FFH						
	CVTWL		1 0 0 1 1 0 0 1	1	When AW<8000H, DW←0; otherwise, DW←FFFFH						
Comparison	CMP	reg, reg	0 0 1 1 1 0 1 W / 1 1 reg reg	2	reg - reg	x	x	x	x	x	x
		mem, reg	0 0 1 1 1 0 0 W / mod reg mem	2 - 4	(mem) - reg	x	x	x	x	x	x
		reg, mem	0 0 1 1 1 0 1 W / mod reg mem	2 - 4	reg - (mem)	x	x	x	x	x	x
		reg, imm	1 0 0 0 0 0 S W / 1 1 1 1 1 reg	3 - 4	reg - imm	x	x	x	x	x	x
		mem, imm	1 0 0 0 0 0 S W / mod 1 1 1 mem	3 - 6	(mem) - imm	x	x	x	x	x	x
		acc, imm	0 0 1 1 1 1 0 W	2 - 3	When W=0, AL - imm When W=1, AW - imm	x	x	x	x	x	x
Complement operation	NOT	reg	1 1 1 1 0 1 1 W / 1 1 0 1 0 reg	2	reg ← $\overline{reg}$						
		mem	1 1 1 1 0 1 1 W / mod 0 1 0 mem	2 - 4	(mem) ← $\overline{(mem)}$						
	NEG	reg	1 1 1 1 0 1 1 W / 1 1 0 1 0 reg	2	reg ← $\overline{reg}$ + 1	x	x	x	x	x	x
		mem	1 1 1 1 0 1 1 W / mod 0 1 0 mem	2 - 4	(mem) ← $\overline{(mem)}$ + 1	x	x	x	x	x	x

Group	Mnemonic	Operand	Operation Code (7 6 5 4 3 2 1 0 / 7 6 5 4 3 2 1 0)		Number of bytes	Operation	Flags AC	CY	V	P	S	Z
Signed division	DIV	reg8	1 1 1 1 0 1 1 0	1 1 1 1 1 reg	2	temp ← AW When temp + reg8 > 0 and temp + reg8 ≤ 7FH or temp + reg8 < 0 and temp + reg8 > 0–7FH–1, AH ← temp%reg8, AL ← temp + reg8 When temp + reg8 > 0 and temp + reg8 > 7FH or temp + reg8 > 0 and temp + reg8 < 0–7FH–1, (SP–1, SP–2) ← PSW, (SP–3, SP–4) ← PS (SP–5, SP–6) ← PC, SP ← SP–6 IE ← 0, BRK ← 0, PS ← (3, 2), PC ← (1, 0)	U	U	U	U	U	U
		mem8	1 1 1 1 0 1 1 0	mod 1 1 0 mem	2 – 4	temp ← AW When temp + (mem8) > 0 and temp + (mem8) ≤ 7FH or temp + (mem8) < 0 and temp + (mem8) > 0–7FH–1, AH ← temp%(mem8), AL ← temp + (mem8) When temp + (mem8) > 0 and temp + (mem8) > 7FH or temp + (mem8) > 0 and temp + (mem8) < 0–7FH–1, (SP–1, SP–2) ← PSW, (SP–3,SP–4) ← PS (SP–5, SP–6) ← PC, SP ← SP–6 IE ← 0, BRK ← 0, PS ← (3, 2), PC ← (1, 0)	U	U	U	U	U	U
		reg16	1 1 1 1 0 1 1 1	1 1 1 1 1 reg	2	temp ← DW, AW When temp + reg16 > 0 and temp + reg16 ≤ 7FFFH or temp + reg16 < 0 and temp + reg16 > 0–7FFFH–1, DW ← temp%reg16, AW ← temp + reg16 When temp + reg16 > 0 and temp + reg16 > 7FFFH or temp + reg16 > 0 and temp + reg16 < 0–7FFFH–1, (SP–1, SP–2)← PSW, (SP–3, SP–4)←PS (SP–5, SP–6)← PC, SP ← SP–6 IE ← 0, BRK ← 0, PS ← (3, 2), PC ← (1, 0)	U	U	U	U	U	U
		mem16	1 1 1 1 0 1 1 1	mod 1 1 1 mem	2 – 4	temp ← DW, AW When temp + (mem16) > 0 and temp + (mem16) ≤ 7FFFH or temp + (mem16) < 0 and temp + (mem16) > 0–7FFFH–1, DW ← temp%(mem16), AW ← temp + (mem16) When temp + (mem16) > 0 and temp + (mem16) > 7FFFH or temp + (mem16) > 0 and temp + (mem16) < 0–7FFFH–1, (SP–1, SP–2)← PSW, (SP–3, SP–4)←PS (SP–5, SP–6)← PC, SP ← SP–6 IE ← 0, BRK ← 0, PS ← (3, 2), PC ← (1, 0)	U	U	U	U	U	U

Group	Mnemonic	Operand	Operation Code (byte 1)	Operation Code (byte 2)	Number of bytes	Operation	AC	CY	V	P	S	Z
Logical operation	TEST	reg, reg	1 0 0 0 0 1 0 W	1 1 reg reg	2	reg ∧ reg	U	0	0	x	x	x
		mem, reg / reg, mem	1 0 0 0 0 1 0 W	mod reg mem	2 – 4	(mem)∧reg	U	0	0	x	x	x
		reg, imm	1 1 1 1 0 1 1 W	1 1 0 0 0 reg	3 – 4	reg∧imm	U	0	0	x	x	x
		mem, imm	1 1 1 1 0 1 1 W	mod 0 0 0 mem	3 – 6	(mem)∧imm	U	0	0	x	x	x
		acc, imm	1 0 1 0 1 0 0 W		2 – 3	When W=0, AL←AL∧imm8; When W=1, AW←AW∧imm16	U	0	0	x	x	x
	AND	reg, reg	0 0 1 0 0 0 1 W	1 1 reg reg	2	reg ← reg ∧ reg	U	0	0	x	x	x
		mem, reg	0 0 1 0 0 0 0 W	mod reg mem	2 – 4	(mem)←(mem)∧reg	U	0	0	x	x	x
		reg, mem	0 0 1 0 0 0 1 W	mod reg mem	2 – 4	reg←reg∧(mem)	U	0	0	x	x	x
		reg, imm	1 0 0 0 0 0 0 W	1 1 1 0 0 reg	3 – 4	reg←reg∧imm	U	0	0	x	x	x
		mem, imm	1 0 0 0 0 0 0 W	mod 1 0 0 mem	3 – 6	(mem)←(mem)∧imm	U	0	0	x	x	x
		acc, imm	0 0 1 0 0 1 0 W		2 – 3	When W=0, AL←AL∧imm8; When W=1, AW←AW∧imm16	U	0	0	x	x	x
	OR	reg, reg	0 0 0 0 1 0 1 W	1 1 reg reg	2	reg←reg∨reg	U	0	0	x	x	x
		mem, reg	0 0 0 0 1 0 0 W	mod reg mem	2 – 4	(mem)←(mem)∨reg	U	0	0	x	x	x
		reg, mem	0 0 0 0 1 0 1 W	mod reg mem	2 – 4	reg←rev∨(mem)	U	0	0	x	x	x
		reg, imm	1 0 0 0 0 0 0 W	1 1 0 0 1 reg	3 – 4	reg←reg∨imm	U	0	0	x	x	x
		mem, imm	1 0 0 0 0 0 0 W	mod 0 0 1 mem	3 – 6	(mem)←(mem)∨imm	U	0	0	x	x	x
		acc, imm	0 0 0 0 1 1 0 W		2 – 3	When W=0, AL←AL∨imm8; When W=1, AW←AW∨imm16	U	0	0	x	x	x
	XOR	reg, reg	0 0 1 1 0 0 1 W	1 1 reg reg	2	reg←reg⊻reg	U	0	0	x	x	x
		mem, reg	0 0 1 1 0 0 0 W	mod reg mem	2 – 4	(mem)←(mem)⊻reg	U	0	0	x	x	x
		reg, mem	0 0 1 1 0 0 1 W	mod reg mem	2 – 4	reg←reg⊻(mem)	U	0	0	x	x	x
		reg, imm	1 0 0 0 0 0 0 W	1 1 1 1 0 reg	3 – 4	reg←reg⊻imm	U	0	0	x	x	x
		mem, imm	1 0 0 0 0 0 0 W	mod 1 1 0 mem	3 – 6	(mem)←(mem)⊻imm	U	0	0	x	x	x
		acc, imm	0 0 1 1 0 1 0 W		2 – 3	When W=0, AL←AL⊻imm8; When W=1, AW←AW⊻imm16	U	0	0	x	x	x

Group	Mnemonic	Operand	Operation Code (Second byte[Note])	Operation Code (Third byte[Note])	Number of bytes	Operation	AC	CY	V	P	S	Z
Bit operation	TEST1	reg8, CL	0001000 0	1 1 0 0 0 reg	3	reg8 bit NO. CL=0: Z←1 / reg8 bit NO. CL=1: Z←0	U	0	0	U	U	×
		mem8, CL	0 0 0 0	mod 0 0 0 mem	3 – 5	(mem8) bit NO. CL=0: Z←1 / (mem8) bit NO. CL=1: Z←0	U	0	0	U	U	×
		reg16, CL	0 0 0 1	1 1 0 0 0 reg	3	reg16 bit NO. CL=0: Z←1 / reg16 bit NO. CL=1: Z←0	U	0	0	U	U	×
		mem16, CL	0 0 0 1	mod 0 0 0 mem	3 – 5	(mem16) bit NO. CL=0: Z←1 / (mem16) bit NO. CL=1: Z←0	U	0	0	U	U	×
		reg8, imm3	1 0 0 0	1 1 0 0 0 reg	4	reg8 bit NO. imm3=0: Z←1 / reg8 bit NO. imm3=1: Z←0	U	0	0	U	U	×
		mem8, imm3	1 0 0 0	mod 0 0 0 mem	4 – 6	(mem8) bit NO. imm3=0: Z←1 / (mem8) bit NO. imm3=1: Z←0	U	0	0	U	U	×
		reg16, imm4	1 0 0 1	1 1 0 0 0 reg	4	reg16 bit NO. imm4=0: Z←1 / reg16 bit NO. imm4=1: Z←0	U	0	0	U	U	×
		mem16, imm4	1 0 0 1	mod 0 0 0 mem	4 – 6	(mem16) bit NO. imm4=0: Z←1 / (mem16) bit NO. imm4=1: Z←0	U	0	0	U	U	×
	NOT1	reg8, CL	0 1 1 0	1 1 0 0 0 reg	3	reg 8 bit NO. CL ← reg8 bit NO. CL						
		mem8, CL	0 1 1 0	mod 0 0 0 mem	3 – 5	(mem8) bit NO. CL ← $\overline{\text{(mem8) bit NO. CL}}$						
		reg16, CL	0 1 1 1	1 1 0 0 0 reg	3	reg 16 bit NO. CL ← $\overline{\text{reg16 bit NO. CL}}$						
		mem16, CL	0 1 1 1	mod 0 0 0 mem	3 – 5	(mem16) bit NO. CL ← $\overline{\text{(mem16) bit NO. CL}}$						
		reg8, imm3	1 1 1 0	1 1 0 0 0 reg	4	reg 8 bit NO. imm3 ← $\overline{\text{reg8 bit NO. imm3}}$						
		mem8, imm3	1 1 1 0	mod 0 0 0 mem	4 – 6	(mem8) bit NO. imm3 ← $\overline{\text{(mem8) bit NO. imm3}}$						
		reg16, imm4	1 1 1 1	1 1 0 0 0 reg	4	reg 16 bit NO. imm4 ← $\overline{\text{reg16 bit NO. imm4}}$						
		mem16, imm4	1 1 1 1	mod 0 0 0 mem	4 – 6	(mem16) bit NO. imm4 ← $\overline{\text{(mem16) bit NO. imm4}}$						

Note First byte = 0FH

NOT1	CY	1 1 1 1 0 1 0 1	1	CY ← $\overline{\text{CY}}$	×

Bit operation

Note: First byte = 0FH

Group	Mnemonic	Operand	Second byte [Note] (7 6 5 4 3 2 1 0)	Third byte [Note] (7 6 5 4 3 2 1 0)	Number of bytes	Operation	AC	CY	V	P	S	Z
Bit operation	CLR1	reg8, CL	0 0 0 1 0 0 1 0	1 1 0 0 0 reg	3	reg8 bit NO. CL ← 0						
		mem8, CL	0 0 0 1 0 0 1 0	mod 0 0 0 mem	3 – 5	(mem8) bit NO. CL ← 0						
		reg16, CL	0 0 0 1 0 0 1 1	1 1 0 0 0 reg	3	reg16 bit NO. CL ← 0						
		mem16, CL	0 0 0 1 0 0 1 1	mod 0 0 0 mem	3 – 5	(mem16) bit NO. CL ← 0						
		reg8, imm3	0 0 0 1 1 0 1 0	1 1 0 0 0 reg	4	reg8 bit NO. imm3 ← 0						
		mem8, imm3	0 0 0 1 1 0 1 0	mod 0 0 0 mem	4 – 6	(mem8) bit NO. imm3 ← 0						
		reg16, imm4	0 0 0 1 1 0 1 1	1 1 0 0 0 reg	4	reg16 bit NO. imm4 ← 0						
		mem16, imm4	0 0 0 1 1 0 1 1	mod 0 0 0 mem	4 – 6	(mem16) bit NO. imm4 ← 0						
	SET1	reg8, CL	0 0 0 1 0 1 0 0	1 1 0 0 0 reg	3	reg 8 bit NO. CL ← 1						
		mem8, CL	0 0 0 1 0 1 0 0	mod 0 0 0 mem	3 – 5	(mem8) bit NO. CL ← 1						
		reg16, CL	0 0 0 1 0 1 0 1	1 1 0 0 0 reg	3	reg 16 bit NO. CL ← 1						
		mem16, CL	0 0 0 1 0 1 0 1	mod 0 0 0 mem	3 – 5	(mem16) bit NO. CL ← 1						
		reg8, imm3	0 0 0 1 1 1 0 0	1 1 0 0 0 reg	4	reg 8 bit NO. imm3 ← 1						
		mem8, imm3	0 0 0 1 1 1 0 0	mod 0 0 0 mem	4 – 6	(mem8) bit NO. imm3 ← 1						
		reg16, imm4	0 0 0 1 1 1 0 1	1 1 0 0 0 reg	4	reg 16 bit NO. imm4 ← 1						
		mem16, imm4	0 0 0 1 1 1 0 1	mod 0 0 0 mem	4 – 6	(mem16) bit NO. imm4 ← 1						

Mnemonic	Operand	Operation Code (7 6 5 4 3 2 1 0)	Number of bytes	Operation	AC	CY	V	P	S	Z
CLR1	CY	1 1 1 1 1 0 0 0	1	CY ← 0		0				
	DIR	1 1 1 1 1 1 0 0	1	DIR ← 0						
SET1	CY	1 1 1 1 1 0 0 1	1	CY ← 1		1			–	
	DIR	1 1 1 1 1 1 0 1	1	DIR ← 1						

Group	Mnemonic	Operand	Operation Code 7 6 5 4 3 2 1 0	Operation Code 7 6 5 4 3 2 1 0	Number of bytes	Operation	Flags AC	CY	V	P	S	Z
Shift	SHL	reg, 1	1 1 0 1 0 0 0 W	1 1 1 0 0 reg	2	CY ← reg MSB, reg ← reg × reg2 When reg MSB≠CY, V←1 When reg MSB=CY, V←0	U	×	×	×	×	×
		mem, 1	1 1 0 1 0 0 0 W	mod 1 0 0 mem	2 – 4	CY ← (mem) MSB, (mem) ← (mem) × 2 When (mem) MSB≠CY, V←1 When (mem) MSB=CY, V←0	U	×	×	×	×	×
		reg, CL	1 1 0 1 0 0 1 W	1 1 1 0 0 reg	2	While temp ← CL and temp≠0, the following operation is repeated: CY ← reg MSB, reg ← reg × 2 temp ← temp–1	U	×	U	×	×	×
		mem, CL	1 1 0 1 0 0 1 W	mod 1 0 0 mem	2 – 4	While temp ← CL and temp≠0, the following operation is repeated: CY ← (mem) MSB, (mem) ← (mem) × 2 temp ← temp–1	U	×	U	×	×	×
		reg, imm8	1 1 0 0 0 0 0 W	1 1 1 0 0 reg	3	While temp ← imm8, temp≠0, the following operation is repeated: CY ← reg MSB and reg ← reg × 2 temp ← temp–1	U	×	U	×	×	×
		mem, imm8	1 1 0 0 0 0 0 W	mod 1 0 0 mem	3 – 5	While temp ← imm8 and temp≠0, the following operation is repeated: CY ← (mem) MSB, (mem) ← (mem) × 2 temp ← temp–1	U	×	U	×	×	×

n: Shift count

Group	Mnemonic	Operand	Operation Code (7-0)	Operation Code (7-0)	Number of bytes	Operation	AC	CY	V	P	S	Z
Shift	SHR	reg, 1	1 1 0 1 0 0 0 W	1 1 1 0 1 reg	2	CY ← reg LSB, reg ← reg + 2 / reg MSB≠second MSB of reg: V ← 1 / reg MSB=second MSB of reg: V ← 0	U	×	×	×	×	×
		mem, 1	1 1 0 1 0 0 0 W	mod 1 0 1 mem	2 – 4	CY ← (mem) MSB, (mem) ← (mem) + 2 / (mem) MSB≠second MSB of reg: V ← 1 / (mem) MSB=second MSB of reg: V ← 0	U	×	×	×	×	×
		reg, CL	1 1 0 1 0 0 1 W	1 1 1 0 1 reg	2	While temp ← CL and temp≠0, the following operation is repeated: CY ← reg LSB, reg ← reg + 2 temp ← temp−1	U	×	U	×	×	×
		mem, CL	1 1 0 1 0 0 1 W	mod 1 0 1 mem	2 – 4	While temp ← CL and temp≠0, the following operation is repeated: CY ← (mem) LSB, (mem) ← (mem) + 2 temp ← temp−1	U	×	U	×	×	×
		reg, imm8	1 1 0 0 0 0 0 W	1 1 1 0 1 reg	3	While temp ← imm8 and temp≠0, the following operation is repeated: CY ← reg LSB, reg ← reg + 2 temp ← temp−1	U	×	U	×	×	×
		mem, imm8	1 1 0 0 0 0 0 W	mod 1 0 1 mem	3 – 5	While temp ← imm8 and temp≠0, the following operation is repeated: CY ← (mem) LSB, (mem) ← (mem) + 2 temp ← temp−1	U	×	U	×	×	×
	SHRA	reg, 1	1 1 0 1 0 0 0 W	1 1 1 1 1 reg	2	CY ← reg LSB, reg ← reg + 2, V ← 0 / Operand MSB does not change.	U	×	0	×	×	×
		mem, 1	1 1 0 1 0 0 0 W	mod 1 1 1 mem	2 – 4	CY ← (mem) LSB, (mem) ← (mem) + 2, V ← 0 / Operand MSB does not change.	U	×	0	×	×	×
		reg, CL	1 1 0 1 0 0 1 W	1 1 1 1 1 reg	2	While temp ← CL and temp≠0, the following operation is repeated: CY ← reg LSB, reg ← reg + 2 temp ← temp−1, operand MSB does not change.	U	×	U	×	×	×
		mem, CL	1 1 0 1 0 0 1 W	mod 1 1 1 mem	2 – 4	While temp ← CL and temp≠0, the following operation is repeated: CY ← (mem) LSB, (mem) ← (mem) + 2 temp ← temp−1, operand MSB does not change.	U	×	U	×	×	×
		reg, imm8	1 1 0 0 0 0 0 W	1 1 1 1 1 reg	3	While temp ← imm8, temp≠0, the following operation is repeated: CY ← reg LSB, reg ← reg + 2 temp ← temp−1, operand MSB does not change.	U	×	U	×	×	×
		mem, imm8	1 1 0 0 0 0 0 W	mod 1 1 1 mem	3 – 5	While temp ← imm8 and temp≠0, the following operation is repeated: CY ← (mem) LSB, (mem) ← (mem) + 2 temp ← temp−1, operand MSB does not change.	U	×	U	×	×	×

n: Shift count

Group	Mnemonic	Operand	Operation Code (byte 1)	Operation Code (byte 2)	Number of bytes	Operation	AC	CY	V	P	S	Z
Rotate	ROL	reg, 1	1 1 0 1 0 0 0 W	1 1 0 0 0 reg	2	CY ← reg MSB, reg ← reg × reg2+CY reg MSB≠CY: V ← 1 reg MSB=CY: V ← 0		×	×			
		mem, 1	1 1 0 1 0 0 0 W	mod 0 0 0 mem	2 – 4	CY ← (mem) MSB, (mem) ← (mem) × 2+CY (mem) MSB≠CY: V ← 1 (mem) MSB=CY: V ← 0		×	×			
		reg, CL	1 1 0 1 0 0 1 W	1 1 0 0 0 reg	2	While temp ← CL and temp≠0, the following operation is repeated: CY ← reg MSB, reg ← reg × 2+CY temp ← temp–1		×	U			
		mem, CL	1 1 0 1 0 0 1 W	mod 0 0 0 mem	2 – 4	While temp ← CL and temp≠0, the following operation is repeated: CY ← (mem) MSB, (mem) ← (mem) × 2+CY temp ← temp–1		×	U			
		reg, imm8	1 1 0 0 0 0 0 W	1 1 0 0 0 reg	3	While temp ← imm8, temp≠0, the following operation is repeated: CY ← reg MSB, reg ← reg × 2 +CY temp ← temp–1		×	U			
		mem, imm8	1 1 0 0 0 0 0 W	mod 0 0 0 mem	3 – 5	While temp ← imm8, temp≠0, the following operation is repeated: CY ← (mem) MSB, (mem) ← (mem) × 2+CY temp ← temp–1		×	U			
	ROR	reg, 1	1 1 0 1 0 0 0 W	1 1 0 0 1 reg	2	CY ← reg LSB, reg ← reg + 2 reg MSB ← CY reg MSB≠second MSB of reg: V ← 1 reg MSB=second MSB of reg: V ← 0		×	×			
		mem, 1	1 1 0 1 0 0 0 W	mod 0 0 1 mem	2 – 4	CY ← (mem) LSB, (mem) ← (mem) + 2 (mem) MSB ← CY (mem) MSB≠second MSB of (mem) (mem) MSB=second MSB of (mem)		×	×			
		reg, CL	1 1 0 1 0 0 1 W	1 1 0 0 1 reg	2	While temp ← CL, CL≠0, the following operation is repeated: CY ← reg LSB, reg ← reg + 2 reg MSB ← CY temp ← temp–1		×	U			
		mem, CL	1 1 0 1 0 0 1 W	mod 0 0 1 mem	2 – 4	While temp ← CL, CL≠0, the following operation is repeated: CY ← (mem) LSB, (mem) ← (mem) + 2 (mem) MSB ← CY temp ← temp–1		×	U			

n: Shift count

Group	Mnemonic	Operand	Operation Code	Number of bytes	Operation	AC	CY	V	P	S	Z
Rotate	ROR	reg, imm8	1 1 0 0 0 0 0 W | 1 1 0 0 1 reg	3	While temp ← imm8, CL≠0, the following operation is repeated: CY ← reg LSB, reg ← reg + 2 reg MSB ← CY temp ← temp-1		×	U			
		mem, imm8	1 1 0 0 0 0 0 W | mod 0 0 1 mem	3 – 5	While temp ← imm8, CL≠0, the following operation is repeated: CY ← (mem) LSB, (mem) ← (mem) + 2 (mem) MSB ← CY temp ← temp-1		×	U			
	ROLC	reg, 1	1 1 0 1 0 0 0 W | 1 1 0 1 0 reg	2	tmpcy ← CY, CY ← reg MSB reg ← reg × 2+tmpcy reg MSB≠CY: V ← 1 reg MSB=CY: V ← 0		×	×			
		mem, 1	1 1 0 1 0 0 0 W | mod 0 1 0 mem	2 – 4	tmpcy ← CY, CY ← (mem) MSB (mem) ← (mem) × 2+tmpcy (mem) MSB≠CY: V ← 1 (mem) MSB=CY: V ← 0		×	×			
		reg, CL	1 1 0 1 0 0 1 W | 1 1 0 1 0 reg	2	While temp ← CL, CL≠0, the following operation is repeated: tmpcy ← CY, CY ← reg MSB reg ← reg × 2+tmpcy temp ← temp-1		×	U			
		mem, CL	1 1 0 0 0 0 0 1 W | mod 0 1 0 mem	2 – 4	While temp ← CL, CL≠0, the following operation is repeated: tmpcy ← CY, CY ← (mem) MSB (mem) ← (mem) × 2+tmpcy temp ← temp-1		×	U			
		reg, imm8	1 1 0 0 0 0 0 W | 1 1 0 1 0 reg	3	While temp ← imm8, CL≠0, the following operation is repeated: tmpcy ← CY, CY ← reg MSB reg ← reg × 2+tmpcy temp ← temp-1		×	U			
		mem, imm8	1 1 0 0 0 0 0 W | mod 0 1 0 mem	3 – 5	While temp ← imm8, CL≠0, the following operation is repeated: tmpcy ← CY, CY ← (mem) MSB (mem) ← (mem) × 2+tmpcy temp ← temp-1		×	U			

n: Shift count

Group	Mnemonic	Operand	Operation Code		Number of bytes	Operation	Flags AC	CY	V	P	S	Z
Rotate	RORC	reg, 1	1 1 0 1 0 0 0 W	1 1 0 1 1 reg	2	tmpcy ← CY, CY ← reg LSB reg ← reg + 2 reg MSB ← tmpcy reg MSB≠second MSB of reg: V ← 1 reg MSB=second MSB of reg: V ← 0		×	×			
		mem, 1	1 1 0 1 0 0 0 W	mod 0 1 1 mem	2 – 4	tmpcy ← CY, CY ← (mem) LSB (mem) ← (mem) + 2 (mem) MSB ← tmpcy (mem) MSB≠second MSB of (mem): V ← 1 (mem) MSB=second MSB of (mem): V ← 0		×	×			
		reg, CL	1 1 0 1 0 0 1 W	1 1 0 1 1 reg	2	While temp ← CL, CL≠0, the following operation is repeated: tmpcy ← CY, CY ← reg LSB reg ← reg + 2 reg MSB ← tmpcy temp ← temp–1		×	U			
		mem, CL	1 1 0 1 0 0 1 W	mod 0 1 1 mem	2 – 4	While temp ← CL, CL≠0, the following operation is repeated: tmpcy ← CY, CY ← (mem) LSB (mem) ← (mem) + 2 (mem) MSB ← tmpcy temp ← temp–1		×	U			
		reg, imm8	1 1 0 0 0 0 0 W	1 1 0 1 1 reg	3	While temp ← imm8, CL≠0, the following operation is repeated: tmpcy ← CY, CY ← reg LSB reg ← reg + 2 reg MSB ← tmpcy temp ← temp–1		×	U			
		mem, imm8	1 1 0 0 0 0 0 W	mod 0 1 1 mem	3 – 5	While temp ← imm8, CL≠0, the following operation is repeated: tmpcy ← CY, CY ← (mem) LSB (mem) ← (mem) + 2 (mem) MSB ← tmpcy temp ← temp–1		×	U			

n: Shift count

Group	Mnemonic	Operand	Operation Code (7 6 5 4 3 2 1 0)	Number of bytes	Operation	AC	CY	V	P	S	Z
Subroutine control	CALL	near-proc	1 1 1 0 1 0 0 0	3	(SP-1, SP-2)←PC, SP←SP-2 / PC←PC+disp						
		regptr16	1 1 1 1 1 1 1 1 / 1 1 0 1 0 reg	2	(SP-1, SP-2)←PC, PC←regptr16 / SP←SP-2						
		memptr16	1 1 1 1 1 1 1 1 / mod 0 1 0 mem	2 – 4	(SP-1, SP-2)←PC, SP←SP-2 / PC←(memptr16)						
		far-proc	1 0 0 1 1 0 1 0	5	(SP-1, SP-2)←PS, (SP-3, SP-4)←PC / SP←SP-4 / PS←seg, PC←offset						
		memptr32	1 1 1 1 1 1 1 1 / mod 0 1 1 mem	2 – 4	(SP-1, SP-2)←PS, (SP-3, SP-4)←PC / SP←SP-4 / PS←(memptr32+2), PC←(memptr32)						
	RET		1 1 0 0 0 0 1 1	1	PC←(SP+1, SP) / SP←SP+2						
		pop-value	1 1 0 0 0 0 1 0	3	PC←(SP+1, SP) / SP←SP+2, SP←SP+pop-value						
			1 1 0 0 1 0 1 1	1	PC←(SP+1, SP) / PS←(SP+3, SP+2) / SP←SP+4						
		pop-value	1 1 0 0 1 0 1 0	3	PC←(SP+1, SP) / PS←(SP+3, SP+2) / SP←SP+4, SP←SP+pop-value						
Stack operation	PUSH	mem16	1 1 1 1 1 1 1 1 / mod 1 1 0 mem	2 – 4	(SP-1, SP-2)←(mem16) / SP←SP-2						
		reg16	0 1 0 1 0 reg	1	(SP-1, SP-2)←reg16 / SP←SP-2						
		sreg	0 0 0 sreg 1 1 0	1	(SP-1, SP-2)←sreg / SP←SP-2						
		PSW	1 0 0 1 1 1 0 0	1	(SP-1, SP-2)←PSW / SP←SP-2						
		R	0 1 1 0 0 0 0 0	1	Push registers on the stack						
		imm	0 1 1 0 1 0 S 0	2 – 3	(SP-1, SP-2)←imm / SP←SP-2, when S=1, sign extension						

Group	Mnemonic	Operand	Operation Code 7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	Number of bytes	Operation	AC	CY	V	P	S	Z
Stack operation	POP	mem16	1 0 0 0 1 1 1 1	mod 0 0 0 mem	2-4	(mem16) ← (SP+1, SP); SP ← SP+2						
		reg16	0 1 0 1 1 reg		1	reg16 ← (SP+1, SP); SP ← SP+2						
		sreg	0 0 0 sreg 1 1 1		1	sreg ← (SP+1, SP); SP ← SP+2 sreg: SS, DS0, DS1						
		PSW	1 0 0 1 1 1 0 1		1	PSW ← (SP+1, SP); SP ← SP+2	R	R	R	R	R	R
		R	0 1 1 0 0 0 0 1		1	Pop registers from the stack						
	PREPARE	imm16, imm8	1 1 0 0 1 0 0 0		4	Prepare New Stack Frame						
	DISPOSE		1 1 0 0 1 0 0 1		1	Dispose of Stack Frame						
Branch	BR	near-label	1 1 1 0 1 0 0 1		3	PC ← PC+disp						
		short-label	1 1 1 0 1 0 1 1		2	PC ← PC+ext-disp8						
		regptr16	1 1 1 1 1 1 1 1	1 1 1 0 0 reg	2	PC ← regptr16						
		memptr16	1 1 1 1 1 1 1 1	mod 1 0 0 mem	2 - 4	PC ← (memptr16)						
		far-label	1 1 1 0 1 0 1 0		5	PS ← set; PC ← offset						
		memptr32	1 1 1 1 1 1 1 1	mod 1 0 1 mem	2 - 4	PS ← (memptr32+2); PC ← (memptr32)						

Group	Mnemonic	Operand	Operation Code 7654 3210	Number of bytes	Operation		AC	CY	V	P	S	Z
Conditional branch	BV	short-label	0111 0000	2	PC ← PC+ext-disp8	if V=1						
	BNV	short-label	0111 0001	2	PC ← PC+ext-disp8	if V=0						
	BC BL	short-label	0111 0010	2	PC ← PC+ext-disp8	if CY=1						
	BNC BNL	short-label	0111 0011	2	PC ← PC+ext-disp8	if CY=0						
	BE BZ	short-label	0111 0100	2	PC ← PC+ext-disp8	if Z=1						
	BNE BNZ	short-label	0111 0101	2	PC ← PC+ext-disp8	if Z=0						
	BNH	short-label	0111 0110	2	PC ← PC+ext-disp8	if CY ∨ Z=1						
	BH	short-label	0111 0111	2	PC ← PC+ext-disp8	if CY ∨ Z=0						
	BN	short-label	0111 1000	2	PC ← PC+ext-disp8	if S=1						
	BP	short-label	0111 1001	2	PC ← PC+ext-disp8	if S=0						
	BPE	short-label	0111 1010	2	PC ← PC+ext-disp8	if P=1						
	BPO	short-label	0111 1011	2	PC ← PC+ext-disp8	if P=0						
	BLT	short-label	0111 1100	2	PC ← PC+ext-disp8	if S ⊻ V=1						
	BGE	short-label	0111 1101	2	PC ← PC+ext-disp8	if S ⊻ V=0						
	BLE	short-label	0111 1110	2	PC ← PC+ext-disp8	if (S ⊻ V) ∨ Z=1						
	BGT	short-label	0111 1111	2	PC ← PC+ext-disp8	if (S ⊻ V) ∨ Z=0						
	DBNZNE	short-label	1110 0000	2	PC ← PC+ext-disp8	CW=CW-1 if Z=0 and CW=0						
	DBNZE	short-label	1110 0001	2	PC ← PC+ext-disp8	CW=CW-1 if Z=1 and CW=0						
	DBNZ	short-label	1110 0010	2	PC ← PC+ext-disp8	CW=CW-1 if CW≠0						
	BCWZ	short-label	1110 0011	2	PC ← PC+ext-disp8	if CW=0						
	BTCLR[Note]	sfr, imm3, short-label	0000 1111 1001 1100	5	When (sfr) bit No. imm3=1, PC ← PC+ext-disp8, (sfr) bit No. imm3 ← 0							

Note New added instruction from the µPD70108/µPD70116

Group	Mnemonic	Operand	Operation Code	Number of bytes	Operation	AC	CY	V	P	S	Z
Interrupt	BRK	3	11001100	1	(SP-1, SP-2) ← PSW, (SP-3, SP-4) ← PS, (SP-5, SP-6) ← PC, SP ← SP-6, IE ← 0, BRK ← 0 PS ← (15, 14), PC ← (13, 12)						
		imm8 (*3)	11001101	2	(SP-1, SP-2) ← PSW, (SP-3, SP-4) ← PS, (SP-5, SP-6) ← PC, SP ← SP-6, IE ← 0, BRK ← 0 PS ← (n×4+3, n×4+2), PC ← (n×4+1, n×4) n=imm8						
	BRKV		11001110	1	When V=1, (SP-1, SP-2) ← PSW, (SP-3, SP-4) ← PS, (SP-5, SP-6) ← PC, SP ← SP-6 IE ← 0, BRK ← 0 PS ← (19, 18), PC ← (17, 16)						
	RETI		11001111	1	PC ← (SP+1, SP), PS ← (SP+3, SP+2), PSW ← (SP+5, SP+4), SP ← SP+6	R	R	R	R	R	R
	RETRBI Note		00001111 10010001	2	PC ← Save PC, PSW ← Save PSW	R	R	R	R	R	R
	FINT Note		00001111 10010010	2	Inform the internal interrupt controller in CPU that the interrupt service routine terminates.						
	CHIKIND	reg16, mem32	01100010 mod reg mem	2 – 4	When (mem32) > reg16 or (mem32+2) < reg16, (SP-1, SP-2) ← PSW, (SP-3, SP-4) ← PS, (SP-5, SP-6) ← PC, SP ← SP-6 IE ← 0, BRK ← 0 PS ← (23, 22), PC ← (21, 20)						
Register bank switch	BRKCS Note	reg16	00001111 00101101 / 11000 reg	3	RB2-0 ← reg16 lower 3 bits, IE ← 0, BRK ← 0, Save PSW ← PSW, Save PC ← PC, PC ← Vector PC	x	x	x	x	x	x
	TSKSW Note	reg16	00001111 00101100 / 11111 reg	3	RB2-0 ← reg16 lower 3 bits, Old register bank Save PSW ← PSW, Save PC ← PC, PC, PSW, PC ← New register bank Save PSW, Save PC	x	x	x	x	x	x

Note New added instruction from the µPD70108/µPD70116

Group	Mnemonic	Operand	Operation Code 7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	Number of bytes	Operation	Flags AC	CY	V	P	S	Z
CPU control	HALT		1 1 1 1 0 1 0 0		1	CPU Halt						
	STOP Note 2		0 0 0 0 1 1 1 1	1 0 0 1 1 1 1 0	2	CPU Stop						
	POLL		1 0 0 1 1 0 1 1		1	Poll and wait						
	DI		1 1 1 1 1 0 1 0		1	IE ← 0						
	EI		1 1 1 1 1 0 1 1		1	IE ← 1						
	BUSLOCK		1 1 1 1 0 0 0 0		1	Bus Lock Prefix						
	FPO1 Note 3	fp-op	1 1 0 1 1 X X X	1 1 Y Y Y Z Z Z	2	No Operation						
		fp-op, mem	1 1 0 1 1 X X X	mod Y Y Y mem	2 – 4	data bus ← (mem)						
	FPO2 Note 3	fp-op	0 1 1 0 0 1 1 X	1 1 Y Y Y Z Z Z	2	No Operation						
		fp-op, mem	0 1 1 0 0 1 1 X	mod Y Y Y mem	2 – 4	data bus ← (mem)						
	NOP		1 0 0 1 0 0 0 0		1	No Operation						
	Note 1		0 0 1 sreg 1 1 0		1	Segment override prefix						

Note 1. DS0:, DS1:, PS:, SS:
2. New added instruction from the µPD70108/µPD70116
3. In the µPD70332 and µPD70330, the instruction is not executed and an interrupt occurs.

2.9 NUMBER OF CLOCKS (µPD70320, µPD70322, µPD70325, µPD70327, µPD79011)

In-struc-tion group	Mnemonic	Operand	Clock Count			
			Byte Processing		Word Processing	
			Internal RAM Access Enable	Internal RAM Access Disable	Internal RAM Access Enable	Internal RAM Access Disable
Data transfer instructions	MOV	reg, reg'	2	2	2	2
		mem, reg	EA+4+T	EA+2	EA+6+2·T	EA+2
		reg, mem	EA+6+T	EA+6+T	EA+8+2·T	EA+8+2·T
		mem, imm	EA+5+T	EA+5+T	EA+5+2·T	EA+5+T
		reg, imm	5	5	6	6
		acc, dmem	9+T	9+T	11+2·T	11+2·T
		dmem, acc	7+T	5	9+2·T	5
		sreg, reg16	—	—	4	4
		sreg, mem16	—	—	EA+10+2·T	EA+10+2·T
		reg16, sreg	—	—	3	3
		mem16, sreg	—	—	EA+7+2·T	EA+3
		DS0, reg16, mem32	—	—	EA+19+4·T	EA+19+4·T
		DS1, reg16, mem32	—	—	EA+19+4·T	EA+19+4·T
		AH, PSW	2	2	—	—
		PSW, AH	3	3	—	—
	LDEA	reg16, mem16	—	—	EA+2	EA+2
	TRANS	src-table	10+T	10+T	—	—
	XCH	reg, reg'	3	3	3	3
		mem, reg/ reg, mem	EA+10+2·T	EA+8+2·T	EA+14+2·T	EA+10+2·T
		AW, reg16/ reg16, AW	—	—	4	4
	MOVSPA		—	—	16	16
	MOVSPB	reg16	—	—	11	11
Repeat prefix	REPC		2	2	2	2
	REPNC		2	2	2	2
	REP/ REPE/ REPZ		2	2	2	2
	REPNE/ REPNZ		2	2	2	2
Primitive block transfer instructions	MOVKB (Note 1)	dst-block, src-block	20+2·T	16+T	24+4·T	20+2·T
	(Note 2)		16+(16+2·T)·n	16+(12+T)·n	16+(20+4·T)·n	16+(12+2·T)·n
	CMPKB (Note 1)	dst-block, src-block	23+2·T	19+T	27+4·T	21+4·T
	(Note 2)		16+(21+2·T)·n	16+(21+2·T)·n	16+(25+4·T)·n	16+(25+2·T)·n

Note 1:   No repeat
     2:   Repeat, n: Transfer rate (n ≧ 1)

In-struc-tion group	Mnemonic		Operand	Clock Count			
				Byte Processing		Word Processing	
				Internal RAM Access Enable	Internal RAM Access Disable	Internal RAM Access Enable	Internal RAM Access Disable
primi-tive block trans-fer in-struc-tions	CMPM	(Note 1)	dst-block, src-block	17+T	17+T	19+2·T	19+2·T
		(Note 2)		16+(15+T)·n	16+(15+T)·n	16+(17+2·T)·n	16+(17+2·T)·n
	LDM	(Note 1)	src-block	12+T	12+T	14+2·T	14+2·T
		(Note 2)		16+(10+T)·n	16+(10+T)·n	16+(12+2·T)·n	16+(12+2·T)·n
	STM	(Note 1)	dst-block	12+T	10	14+2·T	10
		(Note 2)		16+(8+T)·n	16+(6+T)·n	16+(10+2·T)·n	16+(6+2·T)·n
Bit field mani-pula-tion in-struc-tions	INS		reg8, reg8'	63-155 (The processing differs among bit length)			
			reg8, imm4	64-156 (The processing differs among bit length)			
	EXT		reg8, reg8'	41-121 (The processing differs among bit length)			
			reg, imm4	41-122 (The processing differs among bit length)			
I/O in-struc-tions	IN		acc, imm8	14+T	14+T	16+2·T	16+2·T
		(Note 3)	acc, DW	13+T	13+T	15+2·T	15+2·T
	OUT		imm8, acc	10+T	10+T	10+2·T	10+2·T
		(Note 3)	DW, acc	9+T	9+T	9+2·T	9+2·T
Primi-tive I/O in-struc-tions	INM		dst-block, DW	19+2·T	17+2·T	21+4·T	17+4·T
		(Note 3)		18+(13+2·T)·n	18+(11+2·T)·n	18+(15+4·T)·n	18+(11+4·T)·n
	OUTM		DW, src-block	19+2·T	17+2·T	21+4·T	17+4·T
		(Note 3)		18+(13+2·T)·n	18+(11+2·T)·n	18+(15+4·T)·n	18+(11+4·T)·n
Addi-tion/ sub-trac-tion in-struc-tions	ADD		reg, reg'	2	2	2	2
			mem, reg	EA+8+2·T	EA+6+T	EA+12+4·T	EA+8+2·T
			reg, mem	EA+6+T	EA+6+T	EA+8+2·T	EA+8+2·T
			reg, imm	5	5	6	6
			mem, imm	EA+9+2·T	EA+7+2·T	EA+14+4·T	EA+10+4·T
			acc, imm	5	5	6	6
	ADDC		reg, reg'	2	2	2	2
			mem, reg	EA+8+2·T	EA+6+T	EA+12+4·T	EA+8+2·T
			reg, mem	EA+6+T	EA+6+T	EA+8+2·T	EA+8+2·T
			reg, imm	5	5	6	6
			mem, imm	EA+9+2·T	EA+7+2·T	EA+14+4·T	EA+10+4·T
			acc, imm	5	5	6	6

Note 1: No repeat

2: Repeat, n: Transfer rate (n ≥ 1)

3: When $\overline{IBRK}$=1

In-struc-tion group	Mnemonic	Operand	Clock Count			
			Byte Processing		Word Processing	
			Internal RAM Access Enable	Internal RAM Access Disable	Internal RAM Access Enable	Internal RAM Access Disable
Addition/subtraction instructions	SUB	reg, reg'	2	2	2	2
		mem, reg	EA+8+2·T	EA+6+T	EA+12+4·T	EA+8+2·T
		reg, mem	EA+6+T	EA+6+T	EA+8+2·T	EA+8+2·T
		reg, imm	5	5	6	6
		mem, imm	EA+9+2·T	EA+7+2·T	EA+14+4·T	EA+10+4·T
		acc, imm	5	5	6	6
	SUBC	reg, reg'	2	2	2	2
		mem, reg	EA+8+2·T	EA+6+T	EA+12+4·T	EA+8+2·T
		reg, mem	EA+6+T	EA+6+T	EA+8+2·T	EA+8+2·T
		reg, imm	5	5	6	6
		mem, imm	EA+9+2·T	EA+7+2·T	EA+14+4·T	EA+10+4·T
		acc, imm	5	5	6	6
BCD operation instruction	ADD4S (Note)		22+(27+3·T)·n	22+(25+3·T)·n	—	—
	SUB4S (Note)		22+(27+3·T)·n	22+(25+3·T)·n	—	—
	CMP4S (Note)		22+(23+3·T)·n	22+(23+3·T)·n	—	—
	ROL4	reg8	17	17	—	—
		mem8	EA+18+2·T	EA+16+2·T	—	—
	ROR4	reg8	21	21	—	—
		mem8	EA+24+2·T	EA+22+2·T	—	—
Increment/decrement instruction	INC	reg8	5	5	—	—
		mem8	EA+11+2·T	EA+9+2·T	EA+15+4·T	EA+11+4·T
		reg16	—	—	2	2
	DEC	reg8	5	5	—	—
		mem8	EA+11+2·T	EA+9+2·T	EA+15+4·T	EA+11+4·T
		reg16	—	—	2	2
Multiplication instruction	MULU	reg8	24	24	—	—
		mem8	EA+26+T	EA+26+T	—	—
		reg16	—	—	32	32
		mem16	—	—	EA+34+2·T	EA+34+2·T

Note: n: 1/2 of the number of BCD digits

In-struc-tion group	Mnemonic	Operand	Clock Count			
			Byte Processing		Word Processing	
			Internal RAM Access Enable	Internal RAM Access Disable	Internal RAM Access Enable	Internal RAM Access Disable
Multi-plica-tion in-struc-tions	MUL	reg8	31 to 40	31 to 40	—	—
		mem8	EA+33+T to EA+42+T	EA+33+T to EA+42+T	—	—
		reg16	—	—	39 to 48	39 to 48
		mem16	—	—	EA+43+2·T to EA+52+2·T	EA+43+2·T to EA+52+2·T
		reg16,(reg16',) imm8	—	—	39 to 49	39 to 49
		reg16, mem16, imm8	—	—	EA+43+2·T to EA+53+2·T	EA+43+2·T to EA+53+2·T
		reg16,(reg16',) imm16	—	—	40 to 50	40 to 50
		reg16, mem16, imm16	—	—	EA+44+2·T to EA+54+2·T	EA+44+2·T to EA+54+2·T
Un-signed divi-sion in-struc-tions	DIVU	reg8	31	31	—	—
		mem8	EA+33+T	EA+33+T	—	—
		reg16	—	—	39	39
		mem16	—	—	EA+43+2·T	EA+43+2·T
Signed divi-sion in-struc-tions	DIV	reg8	46 to 56	46 to 56	—	—
		mem8	EA+48+T to EA+58+T	EA+48+T to EA+58+T	—	—
		reg16	—	—	54 to 64	54 to 64
		mem16	—	—	EA+58+2·T to EA+68+2·T	EA+58+2·T to EA+68+2·T
BCD cor-rection in-struc-tions	ADJBA		17	17	—	—
	ADJ4A		9	9	—	—
	ADJBS		17	17	—	—
	ADJ4S		9	9	—	—
Data conver-sion in-struc-tions	CVTBD		19	19	—	—
	CVTDB		20	20	—	—
	CVTBW		3	3	—	—
	CVTWL		—	—	8	8
Com-parison in-struc-tions	CMP	reg, reg'	2	2	2	2
		mem, reg	EA+6+T	EA+6+T	EA+8+2·T	EA+8+2·T
		reg, mem	EA+6+T	EA+6+T	EA+8+2·T	EA+8+2·T
		reg, imm	5	5	6	6
		mem, imm	EA+7+T	EA+7+T	EA+10+2·T	EA+10+2·T
		acc, imm	5	5	6	6
Com-plement opera-tion in-struc-tions	NOT	reg	5	5	5	5
		mem	EA+11+2·T	EA+9+T	EA+15+4·T	EA+11+2·T
	NEG	reg	5	5	5	5
		mem	EA+11+2·T	EA+9+T	EA+15+4·T	EA+11+2·T

Instruction group	Mnemonic	Operand	Clock Count			
			Byte Processing		Word Processing	
			Internal RAM Access Enable	Internal RAM Access Disable	Internal RAM Access Enable	Internal RAM Access Disable
Logical instructions	TEST	reg, reg'	4	4	4	4
		mem, reg/ reg, mem	EA+8+T	EA+8+T	EA+10+2·T	EA+10+2·T
		reg, imm	7	7	8	8
		mem, imm	EA+11+T	EA+11+T	EA+11+2·T	EA+11+2·T
		acc, imm	5	5	6	6
	AND	reg, reg'	2	2	2	2
		mem, reg	EA+8+2·T	EA+6+T	EA+12+4·T	EA+8+2·T
		reg, mem	EA+6+T	EA+6+T	EA+8+2·T	EA+8+2·T
		reg, imm	5	5	6	6
		mem, imm	EA+9+T	EA+7+T	EA+14+4·T	EA+10+4·T
		acc, imm	5	5	6	6
	OR	reg, reg'	2	2	2	2
		mem, reg	EA+8+2·T	EA+6+T	EA+12+4·T	EA+8+2·T
		reg, mem	EA+6+T	EA+6+T	EA+8+2·T	EA+8+2·T
		reg, imm	5	5	6	6
		mem, imm	EA+9+T	EA+7+T	EA+14+4·T	EA+10+4·T
		acc, imm	5	5	6	6
	XOR	reg, reg'	2	2	2	2
		mem, reg	EA+8+2·T	EA+6+T	EA+12+4·T	EA+8+2·T
		reg, mem	EA+6+T	EA+6+T	EA+8+2·T	EA+8+2·T
		reg, imm	5	5	6	6
		mem, imm	EA+9+T	EA+7+T	EA+14+4·T	EA+10+4·T
		acc, imm	5	5	6	6
Bit manipulation instructions	TEST1	reg8, CL	7	7	—	—
		mem8, CL	EA+11+T	EA+11+T	—	—
		reg16, CL	—	—	7	7
		mem16, CL	—	—	EA+13+2·T	EA+13+2·T
		reg8, imm3	6	6	—	—
		mem8, imm3	EA+8+T	EA+8+T	—	—
		reg16, imm4	—	—	6	6
		mem16, imm4	—	—	EA+10+2·T	EA+10+2·T
	NOT1	reg8, CL	7	7	—	—
		mem8, CL	EA+13+2·T	EA+11+T	—	—
		reg16, CL	—	—	7	7

Instruction group	Mnemonic	Operand	Clock Count			
			Byte Processing		Word Processing	
			Internal RAM Access Enable	Internal RAM Access Disable	Internal RAM Access Enable	Internal RAM Access Disable
Bit manipulation instructions	NOT1	mem16, CL	—	—	EA+17+4·T	EA+13+2·T
		reg8, imm3	6	6	—	—
		mem8, imm3	EA+10+2·T	EA+8+T	—	—
		reg16, imm4	—	—	6	6
		mem16, imm4	—	—	EA+14+4·T	EA+10+2·T
		CY	2	2	2	2
	CLR1	reg8, CL	8	8	—	—
		mem8, CL	EA+14+2·T	EA+12+T	—	—
		reg16, CL	—	—	8	8
		mem16, CL	—	—	EA+18+4·T	EA+14+2·T
		reg8, imm3	7	7	—	—
		mem8, imm3	EA+11+2·T	EA+9+T	—	—
		reg16, imm4	—	—	7	7
		mem16, imm4	—	—	EA+15+4·T	EA+10+2·T
	SET1	reg8, CL	7	7	—	—
		mem8, CL	EA+13+2·T	EA+11+T	—	—
		reg16, CL	—	—	7	7
		mem16, CL	—	—	EA+17+4·T	EA+13+2·T
		reg8, imm3	6	6	—	—
		mem8, imm3	EA+10+2·T	EA+8+T	—	—
		reg16, imm4	—	—	6	6
		mem16, imm4	—	—	EA+14+4·T	EA+10+2·T
	CLR1	CY	2	2	2	2
		DIR	2	2	2	2
	SET1	CY	2	2	2	2
		DIR	2	2	2	2
Shift instructions	SHL	reg, 1	8	8	8	8
		mem, 1	EA+14+2·T	EA+12+T	EA+18+4·T	EA+14+2·T
	(Note)	reg, CL	11+2·n	11+2·n	11+2·n	11+2·n
		mem, CL	EA+17+2·T+2·n	EA+15+T+2·n	EA+21+4·T+2·n	EA+17+2·T+2·n
		reg, imm8	9+2·n	9+2·n	9+2·n	9+2·n
		mem, imm8	EA+13+2·T+2·n	EA+11+T+2·n	EA+17+4·T+2·n	EA+13+2·T+2·n
	SHR	reg, 1	8	8	8	8
		mem, 1	EA+14+2·T	EA+12+T	EA+18+4·T	EA+14+2·T

Note: n: Shift count

Instruction group	Mnemonic	Operand	Clock Count			
			Byte Processing		Word Processing	
			Internal RAM Access Enable	Internal RAM Access Disable	Internal RAM Access Enable	Internal RAM Access Disable
Shift instructions	SHR (Note)	reg, CL	$11+2 \cdot n$	$11+2 \cdot n$	$11+2 \cdot n$	$11+2 \cdot n$
		mem, CL	$EA+17+2 \cdot T+2 \cdot n$	$EA+15+T+2 \cdot n$	$EA+21+4 \cdot T+2 \cdot n$	$EA+17+2 \cdot T+2 \cdot n$
		reg, imm8	$9+2 \cdot n$	$9+2 \cdot n$	$9+2 \cdot n$	$9+2 \cdot n$
		mem, imm8	$EA+13+2 \cdot T+2 \cdot n$	$EA+11+T+2 \cdot n$	$EA+17+4 \cdot T+2 \cdot n$	$EA+13+2 \cdot T+2 \cdot n$
	SHRA	reg, 1	8	8	8	8
		mem, 1	$EA+14+2 \cdot T$	$EA+12+T$	$EA+18+4 \cdot T$	$EA+14+2 \cdot T$
	(Note)	reg, CL	$11+2 \cdot n$	$11+2 \cdot n$	$11+2 \cdot n$	$11+2 \cdot n$
		mem, CL	$EA+17+2 \cdot T+2 \cdot n$	$EA+15+T+2 \cdot n$	$EA+21+4 \cdot T+2 \cdot n$	$EA+17+2 \cdot T+2 \cdot n$
		reg, imm8	$9+2 \cdot n$	$9+2 \cdot n$	$9+2 \cdot n$	$9+2 \cdot n$
		mem, imm8	$EA+13+2 \cdot T+2 \cdot n$	$EA+11+T+2 \cdot n$	$EA+17+4 \cdot T+2 \cdot n$	$EA+13+2 \cdot T+2 \cdot n$
Rotate instructions	ROL	reg, 1	8	8	8	8
		mem, 1	$EA+14+2 \cdot T$	$EA+12+T$	$EA+18+4 \cdot T$	$EA+14+2 \cdot T$
	(Note)	reg, CL	$11+2 \cdot n$	$11+2 \cdot n$	$11+2 \cdot n$	$11+2 \cdot n$
		mem, CL	$EA+17+2 \cdot T+2 \cdot n$	$EA+15+T+2 \cdot n$	$EA+21+4 \cdot T+2 \cdot n$	$EA+17+2 \cdot T+2 \cdot n$
		reg, imm8	$9+2 \cdot n$	$9+2 \cdot n$	$9+2 \cdot n$	$9+2 \cdot n$
		mem, imm8	$EA+13+2 \cdot T+2 \cdot n$	$EA+11+T+2 \cdot n$	$EA+17+4 \cdot T+2 \cdot n$	$EA+13+2 \cdot T+2 \cdot n$
	ROR	reg, 1	8	8	8	8
		mem, 1	$EA+14+2 \cdot T$	$EA+12+T$	$EA+18+4 \cdot T$	$EA+14+2 \cdot T$
	(Note)	reg, CL	$11+2 \cdot n$	$11+2 \cdot n$	$11+2 \cdot n$	$11+2 \cdot n$
		mem, CL	$EA+17+2 \cdot T+2 \cdot n$	$EA+15+T+2 \cdot n$	$EA+21+4 \cdot T+2 \cdot n$	$EA+17+2 \cdot T+2 \cdot n$
		reg, imm8	$9+2 \cdot n$	$9+2 \cdot n$	$9+2 \cdot n$	$9+2 \cdot n$
		mem, imm8	$EA+13+2 \cdot T+2 \cdot n$	$EA+11+T+2 \cdot n$	$EA+17+4 \cdot T+2 \cdot n$	$EA+13+2 \cdot T+2 \cdot n$
	ROLC	reg, 1	8	8	8	8
		mem, 1	$EA+14+2 \cdot T$	$EA+12+T$	$EA+18+4 \cdot T$	$EA+14+2 \cdot T$
	(Note)	reg, CL	$11+2 \cdot n$	$11+2 \cdot n$	$11+2 \cdot n$	$11+2 \cdot n$
		mem, CL	$EA+17+2 \cdot T+2 \cdot n$	$EA+15+T+2 \cdot n$	$EA+21+4 \cdot T+2 \cdot n$	$EA+17+2 \cdot T+2 \cdot n$
		reg, imm8	$9+2 \cdot n$	$9+2 \cdot n$	$9+2 \cdot n$	$9+2 \cdot n$
		mem, imm8	$EA+13+2 \cdot T+2 \cdot n$	$EA+11+T+2 \cdot n$	$EA+17+4 \cdot T+2 \cdot n$	$EA+13+2 \cdot T+2 \cdot n$
	RORC	reg, 1	8	8	8	8
		mem, 1	$EA+14+2 \cdot T$	$EA+12+T$	$EA+18+4 \cdot T$	$EA+14+2 \cdot T$

Note: n: Shift count

In-struc-tion group	Mnemonic	Operand		Clock Count			
				Byte Processing		Word Processing	
				Internal RAM Access Enable	Internal RAM Access Disable	Internal RAM Access Enable	Internal RAM Access Disable
Rotate in-struc-tions	RORC (Note)	reg, CL		11+2·n	11+2·n	11+2·n	11+2·n
		mem, CL		EA+17+2·T+2·n	EA+15+T+2·n	EA+21+4·T+2·n	EA+13+2·T+2·n
		reg, imm8		9+2·n	9+2·n	9+2·n	9+2·n
		mem, imm8		EA+13+2·T+2·n	EA+11+T+2·n	EA+17+4·T+2·n	EA+13+2·T+2·n
Sub-routine control in-struc-tions	CALL	near-proc		—	—	22+2·T	18+2·T
		regptr16		—	—	22+2·T	18+2·T
		memptr16		—	—	EA+26+4·T	EA+24+4·T
		far-proc		—	—	38+4·T	34+4·T
		memptr32		—	—	EA+36+8·T	EA+24+8·T
	RET			—	—	20+2·T	20+2·T
		pop-value		—	—	20+2·T	20+2·T
				—	—	29+4·T	29+4·T
		pop-value		—	—	30+4·T	30+4·T
Stack mani-pula-tion in-struc-tions	PUSH	mem16		—	—	EA+18+4·T	EA+14+4·T
		reg16		—	—	10+2·T	6
		sreg		—	—	11+2·T	7
		PSW		—	—	10+2·T	6
		R		—	—	82+16·T	50
		imm8		—	—	13+2·T	9
		imm16		—	—	14+2·T	10
	POP	mem16		—	—	EA+16+4·T	EA+12+2·T
		reg16		—	—	12+2·T	12+2·T
		sreg		—	—	13+2·T	13+2·T
		PSW		—	—	14+2·T	14+2·T
		R		—	—	82+16·T	58
	PREPARE (Note 2)	imm16, imm8	When imm8=0, 27+2·T When imm8=1, 39+4·T When imm8=n and n>1, 46+19(n-1)+4·T				
	DISPOSE			—	—	12+2·T	12+2·T

Note 1: n: Shift count
    2: n: Procedure block depth (Lexical level)

In-struc-tion group	Mnemonic	Operand	Clock Count			
			Byte Processing		Word Processing	
			Internal RAM Access Enable	Internal RAM Access Disable	Internal RAM Access Enable	Internal RAM Access Disable
Branch in-struc-tion	BR	near-label	—	—	12	12
		short-label	—	—	12	12
		regptr16	—	—	13	13
		memptr16	—	—	EA+17+2·T	EA+17+2·T
		far-label	—	—	15	15
		memptr32	—	—	EA+25+4·T	EA+25+4·T
(Note) Condi-tional branch in-struc-tions	BV	short-label	—	—	15/8	15/8
	BNV	short-label	—	—	15/8	15/8
	BC/BL	short-label	—	—	15/8	15/8
	BNC/BNL	short-label	—	—	15/8	15/8
	BE/BZ	short-label	—	—	15/8	15/8
	BNE/BNZ	short-label	—	—	15/8	15/8
	BNH	short-label	—	—	15/8	15/8
	BH	short-label	—	—	15/8	15/8
	BN	short-label	—	—	15/8	15/8
	BP	short-label	—	—	15/8	15/8
	BPE	short-label	—	—	15/8	15/8
	BPO	short-label	—	—	15/8	15/8
	BLT	short-label	—	—	15/8	15/8
	BGE	short-label	—	—	15/8	15/8
	BLE	short-label	—	—	15/8	15/8
	BGT	short-label	—	—	15/8	15/8
	DBNZNE	short-label	—	—	17/8	17/8
	DBNZE	short-label	—	—	17/8	17/8
	DBNZ	short-label	—	—	17/8	17/8
	BCWZ	short-label	—	—	15/8	15/8
	BTCLR	sfr, imm3, short-label	29/21	29/21	—	—

Note: Clock count: Left side value is truth, and right side value is false

In-struc-tion group	Mnemonic	Operand	Clock Count			
			Byte Processing		Word Processing	
			Internal RAM Access Enable	Internal RAM Access Disable	Internal RAM Access Enable	Internal RAM Access Disable
Inter-rupt in-struc-tions	BRK	3	—	—	$55+10 \cdot T$	$43+10 \cdot T$
		imm8($\neq$3)	—	—	$56+10 \cdot T$	$44+10 \cdot T$
	BRKV		—	—	$55+10 \cdot T$	$43+10 \cdot T$
	RETI		—	—	$45+6 \cdot T$	$37+2 \cdot T$
	RETRBI		—	—	12	12
	FINT		2	2	2	2
	CHKIND	reg16, mem32	—	—	$EA+26+4 \cdot T$	$EA+26+4 \cdot T$
Reg-ister bank switch in-struc-tions	BRKCS	reg16	—	—	15	15
	TSKSW	reg16	—	—	20	20
CPU control in-struc-tions	HALT		—	—	—	—
	STOP		—	—	—	—
	POLL		—	—	—	—
	DI		4	4	4	4
	EI		12	12	12	12
	BUSLOCK		2	2	2	2
	FPO1	fp-op	—	—	$60+10 \cdot T$	$48+10 \cdot T$
		fp-op, mem	—	—	$60+10 \cdot T$	$48+10 \cdot T$
	FPO2	fp-op	—	—	$60+10 \cdot T$	$48+10 \cdot T$
		fp-op, mem	—	—	$60+10 \cdot T$	$48+10 \cdot T$
	NOP		4	4	4	4
(Note)			2	2	2	2

Note: Segment override prefix (DS0:, DS1:, PS: and SS:)

2.10 NUMBER OF CLOCKS (µPD70330, µPD70332, µPD70335, µPD70337, µPD79021)

In-struc-tion group	Mnemonic	Operand	No. of clocks			
			Byte operation		Word operation	
			On-chip RAM access enable	On-chip RAM access disable	On-chip RAM access enable	On-chip RAM access disable
Data transfer	MOV	reg, reg'	2	2	2	2
		mem, reg	EA+5+T	EA+2	EA+5+T	EA+2
		reg, mem	EA+7+T	EA+7+T	EA+7+T	EA+7+T
		mem, imm	EA+6+T	EA+6+T	EA+6+T	EA+6+T
		reg, imm	5	5	6	6
		acc, dmem	10+T	10+T	10+T	10+T
		dmem, acc	8+T	5	8+T	5
		sreg, reg16	—	—	4	4
		sreg, mem16	—	—	EA+9+T	EA+9+T
		reg16, sreg	—	—	3	3
		mem16, sreg	—	—	EA+6+T	EA+3
		DS0, reg16, mem32	—	—	EA+17+2·T	EA+17+2·T
		DS1, reg16, mem32	—	—	EA+17+2·T	EA+17+2·T
		AH, PSW	2	2	—	—
		PSW, AH	3	3	—	—
	LDEA	reg16, mem16	—	—	EA+2	EA+2
	TRANS	src-table	11+T	11+T	—	—
	XCH	reg, reg'	3	3	3	3
		mem, reg/ reg, mem	EA+12+2·T	EA+9+T	EA+12+2·T	EA+9+T
		AW, reg16/ reg16, AW	—	—	4	4
	MOVSPA		—	—	16	16
	MOVSPB	reg16	—	—	11	11
Repeat prefix	REPC		2	2	2	2
	REPNC		2	2	2	2
	REP/ REPE/ REPZ		2	2	2	2
	REPNE/ REPNZ		2	2	2	2
Primitive block transfer	MOVBK (Note 1)	dst-block, src-block	22+2·T	17+T	22+2·T	19+T
	(Note 2)		16+(18+2·T)·n	16+(13+T)·n	16+(18+2·T)·n	16+(10+T)·n
	CMPBK (Note 1)	dst-block, src-block	25+2·T	21+2·T	25+2·T	19+2·T
	(Note 2)		16+(23+2·T)·n	16+(23+T)·n	16+(23+2·T)·n	16+(23+T)·n

Note 1: No repetition
2: Repetition. n: Transfer count (n ≥ 1)

In-struc-tion group	Mnemonic	Operand	No. of clocks			
			Byte operation		Word operation	
			On-chip RAM access enable	On-chip RAM access disable	On-chip RAM access enable	On-chip RAM access disable
Primitive block transfer	CMPM (Note 1)	dst-block, src-block	$18+T$	$18+T$	$19+2 \cdot T$	$19+2 \cdot T$
	(Note 2)		$16+(16+T) \cdot n$	$16+(16+T) \cdot n$	$16+(16+T) \cdot n$	$16+(16+T) \cdot n$
	LDM (Note 1)	dst-block, src-block	$13+T$	$13+T$	$13+T$	$13+T$
	(Note 2)		$16+(11+T) \cdot n$	$16+(11+T) \cdot n$	$16+(11+T) \cdot n$	$16+(11+T) \cdot n$
	STM (Note 1)	dst-block, src-block	$13+T$	10	$13+T$	10
	(Note 2)		$16+(9+T) \cdot n$	$16+(7+T) \cdot n$	$16+(9+T) \cdot n$	$16+(5+T) \cdot n$
Bit field handling	INS	reg8, reg8'	—	—	63 to 155	63 to 155
		reg8, imm4	—	—	64 to 156	64 to 156
	EXT	reg8, reg8'	—	—	41 to 121	41 to 121
		reg, imm8	—	—	42 to 122	42 to 122
Input/ output	IN	acc, imm8	$15+T$	$15+T$	$15+T$	$15+T$
	(Note 3)	acc, DW	$14+T$	$14+T$	$14+T$	$14+T$
	OUT	imm8, acc	$11+T$	$11+T$	$9+T$	$9+T$
	(Note 3)	DW, acc	$10+T$	$10+T$	$8+T$	$8+T$
Primitive input/ output	INM	dst-block, DW	$21+2 \cdot T$	$19+2 \cdot T$	$19+2 \cdot T$	$15+2 \cdot T$
	(Note 3)		$18+(15+2 \cdot T) \cdot n$	$18+(13+2 \cdot T) \cdot n$	$18+(13+2 \cdot T) \cdot n$	$18+(9+2 \cdot T) \cdot n$
	OUTM	DW, dst-block	$21+2 \cdot T$	$19+2 \cdot T$	$19+2 \cdot T$	$15+2 \cdot T$
	(Note 3)		$18+(15+2 \cdot T) \cdot n$	$18+(13+2 \cdot T) \cdot n$	$18+(13+2 \cdot T) \cdot n$	$18+(9+2 \cdot T) \cdot n$
Addition and sub-trac-tion	ADD	reg, reg'	2	2	2	2
		mem, reg	$EA+10+2 \cdot T$	$EA+7+T$	$EA+10+2 \cdot T$	$EA+7+T$
		reg, mem	$EA+7+T$	$EA+7+T$	$EA+7+T$	$EA+7+T$
		reg, imm	5	5	6	6
		mem, imm	$EA+11+2 \cdot T$	$EA+9+2 \cdot T$	$EA+12+2 \cdot T$	$EA+8+2 \cdot T$
		acc, imm	5	5	6	6
	ADDC	reg, reg'	2	2	2	2
		mem, reg	$EA+10+2 \cdot T$	$EA+7+T$	$EA+10+2 \cdot T$	$EA+7+T$
		reg, mem	$EA+7+T$	$EA+7+T$	$EA+7+T$	$EA+7+T$
		reg, imm	5	5	6	6
		mem, imm	$EA+11+2 \cdot T$	$EA+9+2 \cdot T$	$EA+12+2 \cdot T$	$EA+8+2 \cdot T$
		acc, imm	5	5	6	6

Note 1: No repetition

2: Repetition. n: Transfer count ($n \geq 1$)

3: When $\overline{IBRK}=1$

In-struc-tion group	Mnemonic	Operand	No. of clocks			
			Byte operation		Word operation	
			On-chip RAM access enable	On-chip RAM access disable	On-chip RAM access enable	On-chip RAM access disable
Addi-tion and sub-trac-tion	SUB	reg, reg'	2	2	2	2
		mem, reg	$EA+10+2 \cdot T$	$EA+7+T$	$EA+10+2 \cdot T$	$EA+7+T$
		reg, mem	$EA+7+T$	$EA+7+T$	$EA+7+T$	$EA+7+T$
		reg, imm	5	5	6	6
		mem, imm	$EA+11+2 \cdot T$	$EA+9+2 \cdot T$	$EA+12+2 \cdot T$	$EA+8+2 \cdot T$
		acc, imm	5	5	6	6
	SUBC	reg, reg'	2	2	2	2
		mem, reg	$EA+10+2 \cdot T$	$EA+7+T$	$EA+10+2 \cdot T$	$EA+7+T$
		reg, mem	$EA+7+T$	$EA+7+T$	$EA+7+T$	$EA+7+T$
		reg, imm	5	5	6	6
		mem, imm	$EA+11+2 \cdot T$	$EA+9+2 \cdot T$	$EA+12+2 \cdot T$	$EA+8+2 \cdot T$
		acc, imm	5	5	6	6
BCD opera-tion	ADD4S (Note)		$22+(30+3 \cdot T) \cdot n$	$22+(28+3 \cdot T) \cdot n$	—	—
	SUB4S (Note)		$22+(30+3 \cdot T) \cdot n$	$22+(28+3 \cdot T) \cdot n$	—	—
	CMP4S (Note)		$22+(25+2 \cdot T) \cdot n$	$22+(25+2 \cdot T) \cdot n$	—	—
	ROL4	reg8	17	17	—	—
		mem8	$EA+20+2 \cdot T$	$EA+18+2 \cdot T$	—	—
	ROR4	reg8	21	21	—	—
		mem8	$EA+26+2 \cdot T$	$EA+24+2 \cdot T$	—	—
Incre-ment and decre-ment	INC	reg8	5	5	—	—
		mem8	$EA+13+2 \cdot T$	$EA+11+2 \cdot T$	$EA+13+2 \cdot T$	$EA+9+2 \cdot T$
		reg16	—	—	2	2
	DEC	reg8	5	5	—	—
		mem8	$EA+13+2 \cdot T$	$EA+11+2 \cdot T$	$EA+13+2 \cdot T$	$EA+9+2 \cdot T$
		reg16	—	—	2	2
Multi-plica-tion	MULU	reg8	24	24	—	—
		mem8	$EA+27+T$	$EA+27+T$	—	—
		reg16	—	—	32	32
		mem16	—	—	$EA+33+T$	$EA+33+T$

Note: n: Half of the number of BCD digits

In-struc-tion group	Mnemonic	Operand	No. of clocks			
			Byte operation		Word operation	
			On-chip RAM access enable	On-chip RAM access disable	On-chip RAM access enable	On-chip RAM access disable
Multi-plica-tion	MUL	reg8	31 to 40	31 to 40	—	—
		mem8	EA+34+T to EA+43+T	EA+34+T to EA+43+T	—	—
		reg16	—	—	39 to 48	39 to 48
		mem16	—	—	EA+42+T to EA+51+T	EA+42+T to EA+51+T
		reg16,(reg16',) imm8	—	—	39 to 49	39 to 49
		reg16, mem16, imm8	—	—	EA+42+T to EA+52+T	EA+42+T to EA+52+T
		reg16,(reg16',) imm16	—	—	40 to 50	40 to 50
		reg16, mem16, imm16	—	—	EA+43+T to EA+53+T	EA+43+T to EA+53+T
Un-signed divi-sion	DIVU	reg8	31	31	—	—
		mem8	EA+34+T	EA+34+T	—	—
		reg16	—	—	39	39
		mem16	—	—	EA+43+2·T	EA+43+2·T
Signed divi-sion	DIV	reg8	46 to 56	46 to 56	—	—
		mem8	EA+49+T to EA+59+T	EA+49+T to EA+59+T	—	—
		reg16	—	—	54 to 64	54 to 64
		mem16	—	—	EA+57+T to EA+67+T	EA+57+T to EA+67+T
BCD adjust-ment	ADJBA		17	17	—	—
	ADJ4A		9	9	—	—
	ADJBS		17	17	—	—
	ADJ4S		9	9	—	—
Data conver-sion	CVTBD		19	19	—	—
	CVTDB		20	20	—	—
	CVTBW		3	3	—	—
	CVTWL		—	—	8	8
Com-parison	CMP	reg, reg'	2	2	2	2
		mem, reg	EA+7+T	EA+7+T	EA+7+T	EA+7+T
		reg, mem	EA+7+T	EA+7+T	EA+7+T	EA+7+T
		reg, imm	5	5	6	6
		mem, imm	EA+8+T	EA+8+T	EA+9+T	EA+9+T
		acc, imm	5	5	6	6
Com-plement ope-ration	NOT	reg	5	5	5	5
		mem	EA+13+2·T	EA+10+T	EA+13+2·T	EA+10+T
	NEG	reg	5	5	5	5
		mem	EA+13+2·T	EA+10+T	EA+13+2·T	EA+10+T

In-struc-tion group	Mnemonic	Operand	No. of clocks			
			Byte operation		Word operation	
			On-chip RAM access enable	On-chip RAM access disable	On-chip RAM access enable	On-chip RAM access disable
Logical operation	TEST	reg, reg'	4	4	4	4
		mem, reg/ reg, mem	EA+12+T	EA+12+T	EA+11+2·T	EA+11+2·T
		reg, imm	7	7	8	8
		mem, imm	EA+9+T	EA+9+T	EA+10+T	EA+10+T
		acc, imm	5	5	6	6
	AND	reg, reg'	2	2	2	2
		mem, reg	EA+10+2·T	EA+7+T	EA+10+2·T	EA+7+T
		reg, mem	EA+7+T	EA+7+T	EA+7+T	EA+7+T
		reg, imm	5	5	6	6
		mem, imm	EA+11+2·T	EA+9+2·T	EA+12+2·T	EA+8+2·T
		acc, imm	5	5	6	6
	OR	reg, reg'	2	2	2	2
		mem, reg	EA+10+2·T	EA+7+T	EA+10+2·T	EA+7+T
		reg, mem	EA+7+T	EA+7+T	EA+7+T	EA+7+T
		reg, imm	5	5	6	6
		mem, imm	EA+11+2·T	EA+9+2·T	EA+12+2·T	EA+8+2·T
		acc, imm	5	5	6	6
	XOR	reg, reg'	2	2	2	2
		mem, reg	EA+10+2·T	EA+7+T	EA+10+2·T	EA+7+T
		reg, mem	EA+7+T	EA+7+T	EA+7+T	EA+7+T
		reg, imm	5	5	6	6
		mem, imm	EA+11+2·T	EA+9+2·T	EA+12+2·T	EA+8+2·T
		acc, imm	5	5	6	6
Bit manipulation	TEST1	reg8, CL	7	7	—	—
		mem8, CL	EA+12+T	EA+12+T	—	—
		reg16, CL	—	—	7	7
		mem16, CL	—	—	EA+12+T	EA+12+T
		reg8, imm3	6	6	—	—
		mem8, imm3	EA+9+T	EA+9+T	—	—
		reg16, imm4	—	—	6	6
		mem16, imm4	—	—	EA+9+T	EA+9+T
	NOT1	reg8, CL	7	7	—	—
		mem8, CL	EA+15+2·T	EA+12+T	—	—
		reg16, CL	—	—	7	7

In-struc-tion group	Mnemonic	Operand	No. of clocks			
			Byte operation		Word operation	
			On-chip RAM access enable	On-chip RAM access disable	On-chip RAM access enable	On-chip RAM access disable
Bit manipu-lation	NOT1	mem16, CL	—	—	EA+15+2·T	EA+12+T
		reg8, imm3	6	6	—	—
		mem8, imm3	EA+12+2·T	EA+9+T	—	—
		reg16, imm4	—	—	6	6
		mem16, imm4	—	—	EA+12+2·T	EA+9+T
		CY	2	2	2	2
	CLR1	reg8, CL	8	8	—	—
		mem8, CL	EA+16+2·T	EA+13+T	—	—
		reg16, CL	—	—	8	8
		mem16, CL	—	—	EA+16+2·T	EA+13+T
		reg8, imm3	7	7	—	—
		mem8, imm3	EA+13+2·T	EA+10+T	—	—
		reg16, imm4	—	—	7	7
		mem16, imm4	—	—	EA+13+2·T	EA+9+T
	SET1	reg8, CL	7	7	—	—
		mem8, CL	EA+15+2·T	EA+12+T	—	—
		reg16, CL	—	—	7	7
		mem16, CL	—	—	EA+15+2·T	EA+12+T
		reg8, imm3	6	6	—	—
		mem8, imm3	EA+12+2·T	EA+9+T	—	—
		reg16, imm4	—	—	6	6
		mem16, imm4	—	—	EA+12+2·T	EA+9+T
	CLR1	CY	2	2	2	2
		DIR	2	2	2	2
	SET1	CY	2	2	2	2
		DIR	2	2	2	2
Shift	SHL	reg, 1	8	8	8	8
		mem, 1	EA+16+2·T	EA+13+T	EA+16+2·T	EA+13+T
	(Note)	reg, CL	11+2·n	11+2·n	11+2·n	11+2·n
		mem, CL	EA+19+2·T+2·n	EA+16+T+2·n	EA+19+2·T+2·n	EA+16+T+2·n
		reg, imm8	9+2·n	9+2·n	9+2·n	9+2·n
		mem, imm8	EA+15+2·T+2·n	EA+12+T+2·n	EA+15+2·T+2·n	EA+12+T+2·n
	SHR	reg, 1	8	8	8	8
		mem, 1	EA+16+2·T	EA+13+T	EA+16+2·T	EA+13+T

Note: n: Shift count

In-struction group	Mnemonic	Operand	No. of clocks			
			Byte operation		Word operation	
			On-chip RAM access enable	On-chip RAM access disable	On-chip RAM access enable	On-chip RAM access disable
Shift	SHR (Note)	reg, CL	11+2·n	11+2·n	11+2·n	11+2·n
		mem, CL	EA+19+2·T+2·n	EA+16+T+2·n	EA+19+2·T+2·n	EA+16+T+2·n
		reg, imm8	9+2·n	9+2·n	9+2·n	9+2·n
		mem, imm8	EA+15+2·T+2·n	EA+12+T+2·n	EA+15+2·T+2·n	EA+12+T+2·n
	SHRA	reg, 1	8	8	8	8
		mem, 1	EA+16+2·T	EA+13+T	EA+16+2·T	EA+13+T
	(Note)	reg, CL	11+2·n	11+2·n	11+2·n	11+2·n
		mem, CL	EA+19+2·T+2·n	EA+16+T+2·n	EA+19+2·T+2·n	EA+16+T+2·n
		reg, imm8	9+2·n	9+2·n	9+2·n	9+2·n
		mem, imm8	EA+15+2·T+2·n	EA+12+T+2·n	EA+15+2·T+2·n	EA+12+T+2·n
Rotate	ROL	reg, 1	8	8	8	8
		mem, 1	EA+16+2·T	EA+13+T	EA+16+2·T	EA+13+T
	(Note)	reg, CL	11+2·n	11+2·n	11+2·n	11+2·n
		mem, CL	EA+19+2·T+2·n	EA+16+T+2·n	EA+19+2·T+2·n	EA+16+T+2·n
		reg, imm8	9+2·n	9+2·n	9+2·n	9+2·n
		mem, imm8	EA+15+2·T+2·n	EA+12+T+2·n	EA+15+2·T+2·n	EA+12+T+2·n
	ROR	reg, 1	8	8	8	8
		mem, 1	EA+16+2·T	EA+13+T	EA+16+2·T	EA+13+T
	(Note)	reg, CL	11+2·n	11+2·n	11+2·n	11+2·n
		mem, CL	EA+19+2·T+2·n	EA+16+T+2·n	EA+19+2·T+2·n	EA+16+T+2·n
		reg, imm8	9+2·n	9+2·n	9+2·n	9+2·n
		mem, imm8	EA+15+2·T+2·n	EA+12+T+2·n	EA+15+2·T+2·n	EA+12+T+2·n
	ROLC	reg, 1	8	8	8	8
		mem, 1	EA+16+2·T	EA+13+T	EA+16+2·T	EA+13+T
	(Note)	reg, CL	11+2·n	11+2·n	11+2·n	11+2·n
		mem, CL	EA+19+2·T+2·n	EA+16+T+2·n	EA+19+2·T+2·n	EA+16+T+2·n
		reg, imm8	9+2·n	9+2·n	9+2·n	9+2·n
		mem, imm8	EA+15+2·T+2·n	EA+12+T+2·n	EA+15+2·T+2·n	EA+12+T+2·n
	RORC (Note)	reg, 1	8	8	8	8
		mem, 1	EA+16+2·T	EA+13+T	EA+16+2·T	EA+13+T

Note: n: Shift count

In-struc-tion group	Mnemonic	Operand	No. of clocks			
			Byte operation		Word operation	
			On-chip RAM access enable	On-chip RAM access disable	On-chip RAM access enable	On-chip RAM access disable
Rotate	RORC (Note)	reg, CL	$11+2\cdot n$	$11+2\cdot n$	$11+2\cdot n$	$11+2\cdot n$
		mem, CL	$EA+19+2\cdot T+2\cdot n$	$EA+16+T+2\cdot n$	$EA+19+2\cdot T+2\cdot n$	$EA+16+T+2\cdot n$
		reg, imm8	$9+2\cdot n$	$9+2\cdot n$	$9+2\cdot n$	$9+2\cdot n$
		mem, imm8	$EA+15+2\cdot T+2\cdot n$	$EA+12+T+2\cdot n$	$EA+15+2\cdot T+2\cdot n$	$EA+12+T+2\cdot n$
Sub-routine control	CALL	near-proc	—	—	$21+T$	$17+T$
		regptr16	—	—	$21+T$	$17+T$
		memptr16	—	—	$EA+24+2\cdot T$	$EA+22+2\cdot T$
		far-proc	—	—	$36+2\cdot T$	$32+2\cdot T$
		memptr32	—	—	$EA+32+4\cdot T$	$EA+20+4\cdot T$
	RET		—	—	$19+T$	$19+T$
		pop-value	—	—	$19+T$	$19+T$
			—	—	$27+2\cdot T$	$27+2\cdot T$
		pop-value	—	—	$28+2\cdot T$	$28+2\cdot T$
Stack handl-ing	PUSH	mem16	—	—	$EA+16+2\cdot T$	$EA+12+2\cdot T$
		reg16	—	—	$13+T$	$9+T$
		sreg	—	—	$10+T$	7
		PSW	—	—	$9+T$	6
		R	—	—	$74+8\cdot T$	50
		imm8	—	—	$12+T$	9
		imm16	—	—	$13+T$	10
	POP	mem16	—	—	$EA+14+2\cdot T$	$EA+11+T$
		reg16	—	—	$11+T$	$11+T$
		sreg	—	—	$12+T$	$12+T$
		PSW	—	—	$13+T$	$13+T$
		R	—	—	$74+8\cdot T$	58
	PREPARE (Note 2)	imm16, imm8	When imm8=0 $26+T$ When imm8=1 $37+2\cdot T$ When imm8=n where n>1, $44+19(n-1)2\cdot n\cdot T$			
	DISPOSE		—	—	$11+T$	$11+T$

Note 1: n: Shift count

Note 2: n: Procedure block depth (lexical level)

In-struc-tion group	Mnemonic	Operand	No. of clocks			
			Byte operation		Word operation	
			On-chip RAM access enable	On-chip RAM access disable	On-chip RAM access enable	On-chip RAM access disable
Branch	BR	near-label	—	—	12	12
		short-label	—	—	12	12
		regptr16	—	—	13	13
		memptr16	—	—	EA+16+T	EA+16+T
		far-label	—	—	15	15
		memptr32	—	—	EA+23+2·T	EA+23+2·T
(Note) Conditional branch	BV	short-label	—	—	15/8	15/8
	BVN	short-label	—	—	15/8	15/8
	BC/BL	short-label	—	—	15/8	15/8
	BNC/BNL	short-label	—	—	15/8	15/8
	BE/BZ	short-label	—	—	15/8	15/8
	BNE/BNZ	short-label	—	—	15/8	15/8
	BNH	short-label	—	—	15/8	15/8
	BH	short-label	—	—	15/8	15/8
	BN	short-label	—	—	15/8	15/8
	BP	short-label	—	—	15/8	15/8
	BPE	short-label	—	—	15/8	15/8
	BPO	short-label	—	—	15/8	15/8
	BLT	short-label	—	—	15/8	15/8
	BGE	short-label	—	—	15/8	15/8
	BLE	short-label	—	—	15/8	15/8
	BGT	short-label	—	—	15/8	15/8
	DBNZNE	short-label	—	—	17/8	17/8
	DBNZE	short-label	—	—	17/8	17/8
	BCWZ	short-label	—	—	15/8	15/8
	BTCLR	sfr, imm3 short-label	29	29	—	—
Interrupt	BRK	3	—	—	50+5·T	38+5·T
		imm8(≠3)	—	—	51+5·T	39+5·T
	BRKV		—	—	50+5·T	38+5·T
	RETI		—	—	42+3·T	36+T
	RETRBI		—	—	12	12
	FINT		2	2	2	2
	CHKIND	reg16, mem32	—	—	EA+24+2·T	EA+24+2·T

Note: The numeric value to the left of / under No. of clocks applies when the condition is true; the numeric value to the right of / applies when the condition is false.

In-struc-tion group	Mnemonic	Operand	No. of clocks			
			Byte operation		Word operation	
			On-chip RAM access enable	On-chip RAM access disable	On-chip RAM access enable	On-chip RAM access disable
Inter-rupt	BRKCS	reg16	—	—	15	15
	TSKSW	REG16	—	—	20	20
CPU control	HALT		—	—	—	—
	STOP		—	—	—	—
	POLL		—	—	—	—
	DI		4	4	4	4
	EI		12	12	12	12
	BUSLOCK		2	2	2	2
	FPO1	fp-op	—	—	$55+5 \cdot T$	$43+5 \cdot T$
		fp-op, mem	—	—	$55+5 \cdot T$	$43+5 \cdot T$
	FPO2	fp-op	—	—	$55+5 \cdot T$	$43+5 \cdot T$
		fp-op, mem	—	—	$55+5 \cdot T$	$43+5 \cdot T$
	NOP		4	4	4	4
(Note)			2	2	2	2

Note: Segment override prefix (DS0:, DS1:, PS:, SS:)

3.0 ELECTRICAL SPECIFICATION

3.1 FOR µPD70320, µPD70320(A), µPD70322, µPD70322(A), µPD70327, µPD79011

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply Voltage	V_{DD}		−0.5 to +7.0	V
Input Voltage	V_{TH}		−0.5 to V_{DD} +0.5	V
	V_I		−0.5 to V_{DD} +0.5	V
Output Voltage	V_O		−0.5 to V_{DD} +0.5	V
Output Current Low	I_{OL}	Each output pin	4.0	mA
		Total	50	mA
Output Current High	I_{OH}	Each output pin	−2.0	mA
		Total	−20	mA
Operating Ambient Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OSCILLATOR CHARACTERISTICS
(T_a = −40 to +85 °C, V_{DD} = +5.0 V ±10 %, V_{SS} = 0 V, 0 V ≤ V_{TH} ≤ V_{DD} + 0.1 V)

CONFIGU-RATION	RECOMMENDED CIRCUIT	PARAMETER	70322, 70320, 70322(A), 70320(A)		70322-8, 70320-8, 70322(A)-8, 70320(A)-8		UNIT
			MIN.	MAX.	MIN.	MAX.	
Internal Oscillator (Ceramic or Crystal Resonator)		Oscillator frequency (f_{XX})	4	10	4	16	MHz
External Clock		X1 input frequency (f_X)	4	10	4	16	MHz
		X1 rise/fall time (t_{XR}, t_{XF})	0	20	0	20	ns
		X1 input high-/low-level width (t_{WXH}, t_{WXL})	35	250	20	250	ns
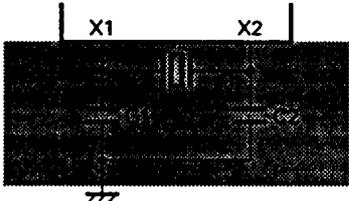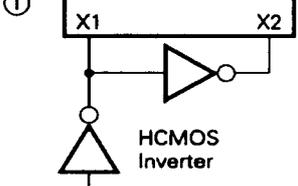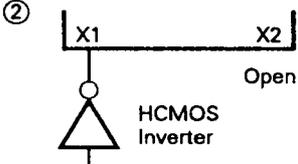
Cautions 1. Mount the capacitors and crystal or ceramic resonator as close to pins X1 and X2 as possible.
2. Do not route other signal lines through the ▓▓▓ area.

RECOMMENDED OSCILLATOR CONSTANT

Ceramic resonator

MANUFACTURER	PRODUCT NUMBER	RECOMMENDED CONSTANTS	
		C1 [pF]	C2 [pF]
Kyocera Corp.	KBR-10.0M Note 1	33	33
Murata Mfg. Co., Ltd.	CSA7.37MT040 Note 2	100	100
	CSA10.0MT Note 1	47	47
	CSA11.0MT Note 2		
	CSA16.0MX040 Note 1	30	30
TDK	FCR10.0M2S Note 2	30	30
	FCR16.0M2S Note 2	15	6
	FCR16.0M2G Note 2	22	10

Notes 1. The operating temperature for the ceramic resonators ranges from –10 °C to +70 °C.
2. The operating temperature for the ceramic resonators ranges from –20 °C to +80 °C.

Crystal resonator

MANUFACTURER	PRODUCT NUMBER	RECOMMENDED CONSTANTS	
		C1 [pF]	C2 [pF]
Kinseki Co., Ltd.	HC-49/U(KR-100)	22	22
	HC-49/U(KR-160)	22	22

Remark For more details on the characteristics of the resonators, please contact the manufacturer.

CAPACITANCE (T$_a$ = 25 °C, V$_{DD}$ = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C$_I$	fc = 1 MHz			10	pF
Output Capacitance	C$_O$	Unmeasured pins returned to 0 V.			20	pF
Input/output Capacitance	C$_{IO}$				20	pF

DC CHARACTERISTICS (T$_a$ = –40 °C to +85 °C, V$_{DD}$ = +5.0 V ±10 %)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Voltage Low	V$_{IL}$			0		0.8	V
Input Voltage High	V$_{IH1}$	Except RESET, P10/NMI, X1, X2		2.2		V$_{DD}$	V
	V$_{IH2}$	RESET, P10/NMI, X1, X2		0.8V$_{DD}$		V$_{DD}$	V
Output Voltage Low	V$_{OL}$	I$_{OL}$ = 1.6 mA				0.45	V
Output Voltage High	V$_{OH}$	I$_{OH}$ = –0.4 mA		V$_{DD}$–1.0			V
Input Current	I$_I$	EA, P10/NMI; 0 ≤ V$_I$ ≤ V$_{DD}$				±20	μA
Input Leakage Current	I$_{LI}$	Except EA, P10/NMI; 0 ≤ V$_I$ ≤ V$_{DD}$				±10	μA
Output Leakage Current	I$_{LO}$	0 ≤ V$_O$ ≤ V$_{DD}$				±10	μA
V$_{TH}$ Current	I$_{TH}$	0 V ≤ V$_{TH}$ ≤ V$_{DD}$			0.5	1.0	mA
V$_{DD}$ Supply Current	I$_{DD1}$	Operating mode	70322, 70320		50	100	mA
			70322-8, 70320-8		65	120	mA
	I$_{DD2}$	HALT mode	70322, 70320		20	40	mA
			70322-8, 70320-8		25	50	mA
	I$_{DD3}$	STOP mode			10	30	μA

AC CHARACTERISTICS (T$_a$ = –40 to +85 °C, V$_{DD}$ = +5.0 V ±10 %)

PARAMETER	SYMBOL	TEST CONDITION	70322, 70320, 70322(A), 70320(A)		70322-8, 70320-8, 70322(A)-8, 70320(A)-8		UNIT
			MIN.	MAX.	MIN.	MAX.	
X1 Input Cycle Time	t$_{CYX}$		98	250	62	250	ns
X1 Input High-/Low-Level Width	t$_{WXH}$, t$_{WXL}$		35		20		ns
X1 Input Rise/Fall Time	t$_{XR}$, t$_{XF}$			20		20	ns
CLKOUT Output Cycle Time	t$_{CYK}$	fx/2, T = t$_{CYK}$	200	2000	125	2000	ns
CLKOUT Output High-/Low-Level Width	t$_{WKH}$, t$_{WKL}$		0.5T–15		0.5T–15		ns
CLKOUT Output Rise/Fall Time	t$_{KR}$, t$_{KF}$			15		15	ns
Input Rise/Fall Time	t$_{IR}$, t$_{IF}$	Except RESET, NMI, X1 and X2		20		20	ns
	t$_{IRS}$, t$_{IFS}$	RESET, NMI		30		30	ns
Output Rise/Fall Time	t$_{OR}$, t$_{OF}$	Except CLKOUT		20		20	ns

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Address Delay Time from CLKOUT	t_{DKA}			90	ns
Data Input Delay Time from Address	t_{DADR}			$(n + 1.5)T - 90$	ns
Data Delay Time from $\overline{MREQ}$ ↓	t_{DMRD}			$(n + 1)T - 75$	ns
Data Delay Time from $\overline{MSTB}$ ↓	t_{DMSD}			$(n + 0.5)T - 75$	ns
$\overline{MSTB}$ ↓ Delay Time from $\overline{MREQ}$ ↓	t_{DMRMS}		$0.5T - 35$	$0.5T + 35$	ns
$\overline{MREQ}$ Low-Level Width	t_{WMRL}		$(n + 1)T - 30$	$(n + 1)T + 30$	ns
Address Hold Time (from $\overline{MREQ}$ ↑)	t_{HMA}		$0.5T - 30$		ns
Data Input Hold Time (from $\overline{MREQ}$ ↑)	t_{HMDR}		0		ns
Control Signal Recovery Time	t_{RVC}		$T - 25$		ns
Data Output Delay Time from Address	t_{DADW}			$0.5T + 50$	ns
Address Setup Time (to $\overline{MREQ}$ ↓)	t_{DAMR}		$0.5T - 30$		ns
Address Setup Time (to $\overline{MSTB}$ ↓)	t_{DAMS}		$T - 30$		ns
$\overline{MSTB}$ Low-Level Width	t_{WMSL}		$(n + 0.5)T - 30$	$(n + 0.5)T + 30$	ns
Data Output Setup Time (to $\overline{MSTB}$ ↑)	t_{SDM}		$(n + 1)T - 50$		ns
Data Output Hold Time (from $\overline{MSTB}$ ↑)	t_{HMDW}		$0.5T - 30$		ns
Address Setup Time (to $\overline{IOSTB}$ ↓)	t_{DAIS}		$0.5T - 30$		ns
Data Delay Time from $\overline{IOSTB}$ ↓	t_{DISD}			$(n + 1)T - 90$	ns
$\overline{IOSTB}$ Low-Level Width	t_{WISL}		$(n + 1)T - 30$		ns
Address Hold Time (from $\overline{IOSTB}$ ↑)	t_{HISA}		$0.5T - 30$		ns
Data Input Hold Time (from $\overline{IOREQ}$ ↑)	t_{HISDR}		0		ns
Data Output Setup Time (to $\overline{IOSTB}$ ↑)	t_{SDIS}		$(n + 1)T - 50$		ns
Data Output Hold Time (from $\overline{IOSTB}$ ↑)	t_{HISDW}		$0.5T - 30$		ns
$\overline{DMARQ}$ Setup Time (to $\overline{MREQ}$ ↓)	t_{SDADQ}	Demand release mode		1T	ns
$\overline{DMARQ}$ Hold Time (from $\overline{DMAAK}$ ↓)	t_{HDADQ}	Demand release mode	0		ns
$\overline{DMAAK}$ Output Low-Level Width	t_{WDMRL}	Read mode	$(n + 1.5)T - 30$		ns
$\overline{TC}$ ↓ Delay Time from $\overline{DMAAK}$ ↓	T_{DDATC}			$0.5T + 50$	ns
$\overline{TC}$ Low-Level Width	T_{WTCL}		$2T - 30$		ns
$\overline{DMAAK}$ Output Low-Level Width	t_{WDMWL}	Write mode	$(n + 1)T - 30$		ns
Address Setup Time (to $\overline{REFRQ}$ ↓)	t_{DARF}		$0.5T - 30$		ns
$\overline{REFRQ}$ Low-Level Width	t_{WRFL}		$(n + 1)T - 30$		ns
Address Hold Time (from $\overline{REFRQ}$ ↑)	t_{HRFA}		$0.5T - 30$		ns
RESET Low-Level Width	t_{WRSL1}	STOP mode release/ power-ON reset	30		ms
	t_{WRSL2}	System rest	5		μs
READY Setup Time (to $\overline{MREQ}$ ↓, $\overline{IOSTB}$ ↓)	t_{SCRY0}	$n \geq 2$		$T - 100$	ns
	t_{SCRY}	$n \geq 3$		$(n - 1)T - 100$	ns

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
READY Hold Time (from $\overline{\text{MREQ}}$ ↓, $\overline{\text{IOSTB}}$ ↓)	t_{HCRY0}	n = 2	1T		ns
	t_{HCRY}	n ≥ 3	(n − 1)T		ns
	t_{HCRY1}	n ≥ 3	(n − 2)T		ns
HLDRQ Setup Time (to CLKOUT ↑)	t_{SHQK}		30		ns
HLDAK ↓ Delay Time from CLKOUT ↑	t_{DKHA}			80	ns
HLDAK ↓ Delay Time from Bus Float	t_{CFHA}		1T − 50		ns
Bus Output Delay Time from $\overline{\text{HLDAK}}$ ↑	t_{DHAC}		1T − 50		ns
HLDAK ↑ Delay Time from HLDRQ ↓	t_{DHQHA}			3T + 160	ns
Bus Output Delay Time from HLDRQ ↓	t_{DHQC}		3T + 30		ns
HLDRQ Low-Level Width	t_{WHQL}		1.5T		ns
$\overline{\text{HLDAK}}$ Low-Level Width	t_{WHAL}		1T		ns
INT, DMARQ Setup Time (to CLKOUT ↑)	t_{SIQK}		30		ns
INT, DMARQ High-/Low-Level Width	t_{WIQH}, t_{WIQL}		8T		ns
$\overline{\text{POLL}}$ Setup Time (to CLKOUT ↑)	t_{SPLK}		30		ns
NMI High-/Low-Level Width	t_{WNIH}, t_{WNIL}		5		μs
$\overline{\text{CTS}}$ Low-Level Width	t_{WCTL}		2T		ns
INT Setup Time (to CLKOUT ↑)	t_{SIRK}		30		ns
$\overline{\text{INTAK}}$ ↓ Delay Time from CLKOUT ↓	t_{DKIA}			80	ns
INT Hold Time (from $\overline{\text{INTAK}}$ ↓)	t_{HIAIQ}		0		ns
$\overline{\text{INTAK}}$ Low-Level Width	t_{WIAL}		2T − 30		ns
$\overline{\text{INTAK}}$ High-Level Width	t_{WIAH}		1T − 30		ns
Data Delay Time from $\overline{\text{INTAK}}$ ↓	t_{DIAD}			2T − 130	ns
Data Hold Time (from $\overline{\text{INTAK}}$ ↑)	t_{HIAD}		0	0.5T	ns
$\overline{\text{SCK0}}$ Cycle Time	t_{CYTK}		1000		ns
$\overline{\text{SCK0}}$ High-/Low-Level Width	t_{WSTH}, t_{WSTL}		450		ns
TxD Delay Time from $\overline{\text{SCK0}}$ ↓	t_{DTKD}			210	ns
TxD Hold Time (from $\overline{\text{SCK0}}$ ↓)	t_{HTKD}		20		ns
$\overline{\text{CTS0}}$ Cycle Time	t_{CYRK}		1000		ns
$\overline{\text{CTS0}}$ High-/Low-Level Width	t_{WSRH}, t_{WSRL}		420		ns
RxD Setup/Hold Time (to/from $\overline{\text{CTS0}}$ ↑)	t_{SRDK}, t_{HKRD}		80		ns

Remark n indicates the number of wait states. No wait is "n = 0".

COMPARATOR CHARACTERISTICS (T_a = –40 °C to +85 °C, V_{DD} = +5.0 V ±10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Comparator Accuracy	V_{ACOMP}				±100	mV
Threshold Voltage	V_{TH}		0		V_{DD}+0.1	V
Compare Time	t_{COMP}		64		65	t_{CYK}
PT Input Voltage	V_{IPT}		9		V_{DD}	V

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA HOLDING CHARACTERISTICS
(T_a = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Data Hold Supply Voltage	V_{DDDR}		2.5	5.5	V
V_{DD} Rise/Fall Time	t_{RVD}, t_{FVD}		200		μs

3.2 FOR µPD70325-8, µPD70325-10

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Test conditions	Rating	Unit
Supply voltage	V_{DD}		-0.5 to +7.0	V
	V_{TH}		-0.5 to V_{DD}+0.5	V
Input voltage	V_I		-0.5 to V_{DD}+0.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Low level output current	I_{OL}	Per pin	4.0	mA
		Total, all output	50	mA
High level output current	I_{OH}	Per pin	-2.0	mA
		Total, all output	-20	mA
Operating temperature	T_{opt}		-10 to +70	°C
Storage temperature	T_{stg}		-65 to +150	°C

Caution 1: Do not directly connect output (or input/output) pins of IC products to each other or to V_{DD} or V_{CC} or GND. However, open drain pins and open collector pins can be connected to each other.
Direct connection can be made at an external circuit where timing design is made to avoid output collision with pins which become high impedance.

Caution 2: If one of the parameters exceeds the absolute maximum ratings even instantaneously, the product quality may be damaged. This means that the absolute maximum ratings are rated values which may physically damage the products Preferably, use the products at values less than the absolute maximum ratings.
The specifications and test conditions listed under the DC and AC characteristics are the range in which the normal operation and quality of the product are guaranteed.

Oscillator characteristics

uPD70325-8 (Ta = -10 to +70°C, V_{DD} = +5.0V±10%, V_{SS} = 0V,
OV ≤ V_{TH} ≤ V_{DD}+0.1V)

uPD70325-10 (Ta = -10 to +70°C, V_{DD} = +5.0V±5%, V_{SS} = 0V,
OV ≤ V_{TH} ≤ V_{DD}+0.1V)

Oscillator	Recommended circuit	Parameter	uPD70325-8		uPD70325-10		Unit
			MIN.	MAX.	MIN.	MAX.	
Ceramic oscillator or crystal resonator		Oscillation frequency (f_{XX})	4	16	4	20	MHz
External clock	① X1 X2 HCMOS inverter Or ② X1 X2 open HCMOS inverter	X1 input frequency (f_X)	4	16	4	20	MHz
		X1 input rising, falling time (t_{XR}, t_{XF})	0	20	0	15	ns
		X1 input high, low level width (t_{WXH}, t_{WXL})	20		16		ns

Remarks 1: Place the oscillation circuit as near the X1 and X2 pins as possible.

2: Do not pass other signal lines through the shaded area.

Recommended oscillation circuit constant

(1) The following are recommended for ceramic resonators and external capacitance.

Manufacturer	Product Name	Recommended Constant	
		C1 [pF]	C2 [pF]
Murata Mfg.	CSA16.00MX040	30	30
	CSA20.00MX040	10	10
TDK	FCR16.0M2G	30	30

(2) The following are recommended for crystal resonators and external capacitance.

Manufacturer	Product Name	Recommended Constant	
		C1[pF]	C2[pF]
Kinseki	HC-49/U (KR-100)	22	22
	HC-49/U (KR-160)	22	22
	HC-49/U (KR-200)	22	22

Remarks: For such as characteristics of each oscillator, confirm to the each maker.

Capacitance (Ta = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C=1 MHz Pins other than the measured pin: 0V			10	pF
Output capacitance	C_O				20	pF
Input/output capacitance	C_{IO}				20	pF

DC characteristics

uPD70325-8 (Ta=-10 to +70°C, V_{DD}=+5.0V±10%)
uPD70325-10 (Ta=-10 to +70°C, V_{DD}=+5.0V±5%)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Input voltage low	V_{IL}			0		0.8	V
Input voltage high	V_{IH1}	Other than $\overline{RESET}$, P10/NMI, X1, X2		2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P10/NMI, X1, X2		0.8 V_{DD}		V_{DD}	V
Output voltage low	V_{OL}	I_{OL}=1.6 mA				0.45	V
Output voltage high	V_{OH}	I_{OH}=-0.4 mA		V_{DD}-1.0			V
Input current	I_I	$\overline{EA}$, P10/NMI; 0 ≤ V_I ≤ V_{DD}				±20	uA
Input leakage current	I_{LI}	Other than $\overline{EA}$ and P10/NMI; 0 ≤ V_I ≤ V_{DD}				±10	uA
Output leakage current	I_{LO}	0 ≤ V_O ≤ V_{DD}				±10	uA
V_{TH} current	I_{TH}	0 V ≤ V_{TH} ≤ V_{DD}			0.5	1.0	mA
V_{DD} supply	I_{DD1}	Operating model	uPD70325-8		65	120	mA
			uPD70325-10		95	130	mA
	I_{DD2}	HALT mode	uPD70325-8		25	50	mA
			uPD70325-10		30	55	mA
	I_{DD3}	STOP mode			10	30	uA

AC characteristics

(1) uPD70325-8 (Ta=-10 to +70°C, V_{DD}=+5.0V±10%)

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
X1 input cycle time	t_{CYX}		62	250	ns
X1 input high/low level width	t_{WXH}, t_{WXL}		20		ns
X1 input rising/falling time	t_{XR}, t_{XF}			20	ns
CLKOUT output cycle time	t_{CYK}	$f_X/2$, T=t_{CYK}	125	2000	ns
CLKOUT output high/low level width	t_{WKH}, t_{WKL}		0.5T-15		ns
CLKOUT output rising/falling time	t_{KR}, t_{KF}			15	ns
Input rising/falling time	t_{IR}, t_{IF}	Other than $\overline{RESET}$, NMI, X1 and X2		20	ns
	t_{IRS}, t_{IFS}	$\overline{RESET}$, NMI		30	ns
Output rising/falling time	t_{OR}, t_{OF}	Other than CLKOUT		20	ns
Address delay time from CLKOUT	t_{DKA}		15	90	ns
Data input delay time from address	t_{DADR}			(n+1.5)T-70	ns
Data delay time from $\overline{MREQ}$↓	t_{DMRD}			(n+1)T-60	ns
Data delay time from $\overline{MSTB}$↓	t_{DMSD}			(n+0.5)T-60	ns
$\overline{MSTB}$↓ delay time from $\overline{MREQ}$↓	t_{DMRMS}		0.5T-35	0.5T+35	ns
$\overline{MREQ}$ low level width	t_{WMRL}		(n+1)T-30	(n+1)T+30	ns
Address hold time (from $\overline{MREQ}$↓)	t_{HMA}		0.5T-30		ns

(to be continued)

(cont'd)

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
Data input hold time (from $\overline{MREQ}\uparrow$)	t_{HMDR}		0		ns
Control signal recovery time	t_{RVC}		T-25		ns
Data output delay time from address	t_{DADW}		0.5T-35	0.5T+50	ns
Address setup time (to $\overline{MREQ}\downarrow$)	t_{DAMR}		0.5T-30		ns
Address setup time (to $\overline{MSTB}\downarrow$)	t_{DAMS}		T-30		ns
$\overline{MSTB}$ low level width	t_{WMSL}		(n+0.5)T-30	(n+0.5)T+30	ns
Data output setup time (to $\overline{MSTB}\uparrow$)	t_{SDM}		(n+1)T-50		ns
Data output hold time (to $\overline{MSTB}\uparrow$)	t_{HMDW}		0.5T-30		ns
$\overline{IOSTB}$ Address setup time (to $\overline{IOSTB}\downarrow$)	t_{DAIS}		0.5T-30		ns
Data delay time from $\overline{IOSTB}\downarrow$	t_{DISD}			(n+1)T-60	ns
$\overline{IOSTB}$ low level width	t_{WISL}		(n+1)T-30		ns
Address hold time (from $\overline{IOSTB}\downarrow$)	t_{HISA}		0.5T-30		ns
Data input hold time (from $\overline{IOREQ}\downarrow$)	t_{HISDR}		0		ns
Data output setup time (to $\overline{IOSTB}\uparrow$)	t_{SDIS}		(n+1)T-50		ns
Data output hold time (from $\overline{IOSTB}\uparrow$)	t_{HISDW}		0.5T-30		ns
$\overline{DMARQ}$ setup time (to $\overline{MREQ}\downarrow$)	t_{SDADQ}	Demand release mode, n ≥ 2		(n-1)T-50	ns
$\overline{DMARQ}$ hold time (from $\overline{DMAAK}\downarrow$)	t_{HDADQ}	Demand release mode	0		ns
$\overline{DMAAK}$ output low level width	t_{WDMRL}	Read operation	(n+1.5)T-30		ns
$\overline{TC}\downarrow$ delay time from $\overline{DMAAK}\downarrow$	t_{DDATC}			0.5T+50	ns
$\overline{TC}$ low level width	t_{WTCL}		(n+2)T-30		ns
$\overline{DMAAK}$ output low level width	t_{WDMWL}	Write operation	(n+1)T-30		ns

(to be continued)

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
Address setup time (to REFRQ↓)	t_{DARF}		0.5T-30		ns
REFRQ low level width	t_{WRFL}		(n+1)T-30		ns
Address hold time (from REFRQ↑)	t_{HRFA}		0.5T-30		ns
RESET low level width	t_{WRSL1}	STOP mode release/power ON reset	30		ms
	t_{WRSL2}	System reset	5		us
READY setup time (to MREQ↓, IOSTB↓)	t_{SCRYO}	n ≥ 2		T-100	ns
	t_{SCRY}	n ≥ 3		(n-1)T-100	ns
READY hold time (from MREQ↓, IOSTB↓)	t_{HCRYO}	n = 2	T		ns
	t_{HCRY}	n ≥ 3	(n-1)T		ns
	t_{HCRY1}	n ≥ 3	(n-2)T		ns
HLDRQ setup time (to CLKOUT↓)	t_{SHQK}		30		ns
HLDAK↓delay time from CLKOUT↓	t_{DKHA}		15	80	ns
HLDAK↓delay time from bus float	t_{CFHA}		T-50		ns
Bus output delay time from HLDAK↑	t_{DHAC}		T-50		ns
HLDAK↑ delay time from HLDRQ↓	t_{DHQHA}			3T+160	ns
Bus output delay time from HLDRQ↓	t_{DHQC}		3T+30		ns
HLDRQ low level width	t_{WHQL}		1.5T		ns
HLDAK low level width	t_{WHAL}		T		ns
INT, DMARQ setup time (to CLKOUT↓)	t_{SIQK}		30		ns
INT, DMARQ high/ low level width	t_{WIQH}, t_{WIQL}		8T		ns
POLL setup time (to CLKOUT↓)	t_{SPLK}		2T		ns
NMI high/low level width	t_{WNIH}, t_{WNIL}		5		us

(to be continued)

(cont'd)

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
CTS low level width	t_{WCTL}		2T		ns
INT setup time (to CLKOUT↓)	t_{SIRK}		30		ns
INTAK↓ delay time from CLKOUT↓	t_{DKIA}		15	80	ns
INT hold time (from INTAK)	t_{HIAIQ}		0		ns
INTAK low level width	t_{WIAL}		2T-30		ns
INTAK high level width	t_{WIAH}		T-30		ns
Data delay time from INTAK↓	t_{DIAD}			2T-130	ns
Data hold time (from INTAK↑)	t_{HIAD}		0	0.5T	ns
SCKO cycle time	t_{CYTK}		1000		ns
SCKO high/low level width	t_{WSTH}, t_{WSTL}		450		ns
TxD delay time from SCKO↑	t_{DTKD}			210	ns
TxD hold time (from SCKO↑)	t_{HTKD}		20		ns
CTSO cycle time	t_{CYRK}		1000		ns
CTSO high/low level width	t_{WSRH}, t_{WSRL}		420		ns
RxD setup/hold time (to/from CTSO↑)	t_{SRDK}, t_{HKRD}		80		ns

Remarks: n indicates the number of wait states. No wait is "n = 0".

(2) uPD70325-10 (Ta = -10 to +70°C, V_{DD} = +5.0 V±5%)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
X1 input cycle time	t_{CYX}		49	250	ns
X1 input high/low level width	t_{WXH}, t_{WXL}		16		ns
X1 input rising/falling time	t_{XR}, t_{XF}			15	ns
CLKOUT output cycle time	t_{CYK}	$f_X/2$, $T=t_{CYK}$	100	2000	ns
CLKOUT output high/low level width	t_{WKH}, t_{WKL}		0.5T-12		ns
CLKOUT output rising/falling time	t_{KR}, t_{KF}			12	ns
Input rising/falling time	t_{IR}, t_{IF}	Other than RESET, NMI, X1 and X2		20	ns
	t_{IRS}, t_{IFS}	RESET, NMI		30	ns
Output rising/falling time	t_{OR}, t_{OF}	Other than CLKOUT		15	ns
Address delay time from CLKOUT	t_{DKA}		15	75	ns
Data input delay time from address	t_{DADR}			(n+1.5)T-60	ns
Data delay time from MREQ↓	t_{DMRD}			(n+1T)-50	ns
Data delay time from MSTB↓	t_{DMSD}			(n+0.5)T-50	ns
MSTB↓ delay time from MREQ↓	t_{DMRMS}		0.5T-20	0.5T+30	ns
MREQ low level width	t_{WMRL}		(n+1)T-25	(n+1)T+25	ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Address hold time (from $\overline{MREQ}\downarrow$)	t_{HMA}		0.5T-30		ns
Data input hold time (from $\overline{MREQ}\downarrow$)	t_{HMDR}		0		ns
Control signal recovery time	t_{RVC}		T-25		ns
Data output delay time from address	t_{DADW}		0.5T-30	0.5T+50	ns
Address setup time (to $\overline{MREQ}\downarrow$)	t_{DAMR}		0.5T-30		ns
Address setup time (to $\overline{MSTB}\downarrow$)	t_{DAMS}		T-30		ns
$\overline{MSTB}$ low level width	t_{WMSL}		(n+0.5)T-25	(n+0.5)T+25	ns
Data output setup time (to $\overline{MSTB}\downarrow$)	t_{SDM}		(n+1)T-50		ns
Data output hold time (from $\overline{MSTB}\downarrow$)	t_{HMDW}		0.5T-30		ns
Address setup time (to $\overline{IOSTB}\downarrow$)	t_{DAIS}		0.5T-30		ns
Data delay time from $\overline{IOSTB}\downarrow$	t_{DISD}			(n+1)T-50	ns
$\overline{IOSTB}$ low level width	t_{WISL}		(n+1)T-25		ns
Address hold time (from $\overline{IOSTB}\downarrow$)	t_{HISA}		0.5T-30		ns
Data input hold time (from $\overline{IOREQ}\downarrow$)	t_{HISDR}		0		ns
Data output setup time (to $\overline{IOSTB}\downarrow$)	t_{SDIS}		(n+1)T-50		ns
Data output hold time (from $\overline{IOSTB}\downarrow$)	t_{HISDW}		0.5T-30		ns
$\overline{DMARQ}$ setup time (to $\overline{MREQ}\downarrow$)	t_{SDADQ}	Demand release mode, n ≥ 2		(n-1)T-50	ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{DMARQ}$ hold time (from $\overline{DMAAK}\uparrow$)	t_{HDADQ}	Demand release mode	0		ns
$\overline{DMAAK}$ output low level width	t_{WDMRL}	Read operation	$(n+1.5)T-25$		ns
$\overline{TC}\downarrow$ delay time from $\overline{DMAAK}\uparrow$	t_{DDATC}			$0.5T+35$	ns
$\overline{TC}$ low level width	t_{WTCL}		$(n+2)T-25$		ns
$\overline{DMAAK}$ output low level width	t_{WDMWL}	Write operation	$(n+1)T-25$		ns
Address setup time (to $\overline{REFRQ}\downarrow$)	t_{DARF}		$0.5T-30$		ns
$\overline{REFRQ}$ low level width	t_{WRFL}		$(n+1)T-25$		ns
Address hold time (from $\overline{REFRQ}\downarrow$)	t_{HRFA}		$0.5T-30$		ns
$\overline{RESET}$ low level width	t_{WRSL1}	STOP mode release/power ON reset	30		ms
	t_{WRSL2}	System reset	5		us
READY setup time (to $\overline{MREQ}\downarrow$, $\overline{IOSTB}\downarrow$)	t_{SCRY0}	$n \geq 2$		$T-80$	ns
	t_{SCRY}	$n \geq 3$		$(n-1)T-80$	ns
READY hold time (from $\overline{MREQ}\downarrow$, $\overline{IOSTB}\downarrow$)	t_{HCRY0}	$n = 2$	T		ns
	t_{HCRY}	$n \geq 3$	$(n-1)T$		ns
	t_{HCRY1}	$n \geq 3$	$(n-2)T$		ns
HLDRQ setup time (to $CLKOUT\uparrow$)	t_{SHQK}		25		ns
$\overline{HLDAK}\downarrow$ delay time from $CLKOUT\downarrow$	t_{DKHA}		15	70	ns
$\overline{HLDAK}\downarrow$ delay time from bus float	t_{CFHA}		$T-35$		ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Bus output delay time from $\overline{HLDAK}$ ↑	t_{DHAC}		T-35		ns
$\overline{HLDAK}$ ↑ delay time from HLDRQ ↑	t_{DHQHA}			3T+160	ns
Bus output delay time from HLKRQ ↓	t_{DHQC}		3T+30		ns
HLDRQ low level width	t_{WHQL}		1.5T		ns
$\overline{HLDAK}$ low level width	t_{WHAL}		T		ns
INT, DMARQ setup time (to CLKOUT↑)	t_{SIQK}		25		ns
INT, DMARQ high/ low level width	t_{WIQH}, t_{WIQL}		8T		ns
$\overline{POLL}$ setup time (to CLKOUT↑)	t_{SPLK}		25		ns
NMI high/low level width	t_{WNIH}, t_{WNIL}		5		us
$\overline{CTS}$ low level width	t_{WCTL}		2T		ns
INT setup time (to CLKOUT↑)	t_{SIRK}		25		ns
$\overline{INTAK}$ ↓ delay time from CLKOUT ↓	t_{DKIA}		15	70	ns
INT hold time (from $\overline{INTAK}$ ↓)	t_{HIAIQ}		0		ns
$\overline{INTAK}$ low level width	t_{WIAL}		2T-2!		ns
$\overline{INTAK}$ high level width	t_{WIAH}		T-25		ns
Data delay time from $\overline{INTAK}$ ↓	t_{DIAD}			2T-100	ns
Data hold time (from $\overline{INTAK}$ ↓)	t_{HIAD}		0	0.5T	ns
$\overline{SCKO}$ cycle time	t_{CYTK}		1000		ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{SCKO}$ high/low level width	t_{WSTH}, t_{WSTL}		450		ns
TxD delay time from $\overline{SCKO}$↓	t_{DTKD}			210	ns
TxD hold time (from $\overline{SCKO}$↓)	t_{HTKD}		20		ns
$\overline{CTSO}$ cycle time	t_{CYRK}		1000		ns
$\overline{CTSO}$ high/low level width	t_{WSRH}, t_{WSRL}		420		ns
RxD setup/hold time (to/from $\overline{CTSO}$↓)	t_{SRDK}, t_{HKRD}		80		ns

Remarks: n indicates the number of wait states. No wait is "n = 0".

Comparator characteristics

uPD70325-8   (Ta=-10 to +70°C, V_{DD}=+5.0V±10%)
uPD70325-10 (Ta=-10 to +70°C, V_{DD}=+5.0V±5%)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Comparison accuracy	V_{ACOMP}				±100	mV
Threshold voltage	V_{TH}		0		V_{DD}+0.1	V
Comparison time	t_{COMP}		64		65	t_{CYK}
PT input voltage	V_{IPT}		0		V_{DD}	V

Data Memory STOP Mode Low Supply Voltage Data Holding Characteristics (Ta=-10 to +70°C)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Data hold supply voltage	V_{DDDR}		2.5	5.5	V
V_{DD} rising/falling time	t_{RVD}, t_{FVD}		200		us

3.3 FOR μPD70325(A)-9

Absolute maximum Ratings (Ta = 25°C)

Parameter	Symbol	Test condition	Rating	Unit
Power supply voltage	V_{DD}		-0.5 to +7.0	V
	V_{TH}		-0.5 to V_{DD}+0.5	V
Input voltage	V_I		-0.5 to V_{DD}+0.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Output current low	I_{OL}	1 pin	4.0	mA
		Total, all pins	50	mA
Output current high	I_{OH}	1 pin	-2.0	mA
		Total, all pins	-20	mA
Oprating temperature	T_{opt}		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Caution 1: Do not directly connect output (or input/output) pins of IC products to each other or to V_{DD} or V_{CC} or GND. However, open drain pins and open collector pins can be connected to each other.
Direct connection can be made at an external circuit where timing design is made to avoid output collision with pins which become high impedance.

Caution 2: If one of the parameters exceeds the absolute maximum ratings even instantaneously, the product quality may be damaged. This means that the absolute maximum ratings are rated values which may physically damage the products. Preferably, use the products at values less than the absolute maximum ratings.
The specifications and test conditions listed under the DC and AC characteristics are the range in which the normal operation and quality of the product are guaranteed.

NEC

Oscillator Characteristics

uPD70325(A)-9 (Ta = -40 to +85°C, V_{DD} = +5.0 V ±5%, V_{SS} = 0 V, 0 V $\leq$ V_{TH} $\leq$ V_{DD}+0.1 V)

Resonator	Recommended circuit	Parameter	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator	X1 X2 C1 C2	Oscillation frequency (f_{XX})	4	18	MHz
External clock	① X1 X2 HCMOS inverter Or ② X1 X2 open HCMOS inverter	X1 input frequency (f_X)	4	18	MHz
		X1 input rising, falling time (t_{XR}, t_{XF})	0	15	ns
		X1 high, low level width (t_{WXH}, t_{WXL})	17		ns

Remarks 1: Place the oscillation circuit as near the X1 and X2 pins as possible.

2: Do not pass other signal lines through the shaded area.

Capacitance (Ta = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			10	p_F
Output capacitance	C_O				20	p_F
I/O capacitance	C_{IO}				20	p_F

DC Characteristics

uPD70325(A)-9 (Ta = -40 ro +85°C, V_{DD} = +5.0 V±5%)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input voltage low	V_{IL}		0		0.8	V
Input voltage high	V_{IH1}	Other than RESET, P10/ NMI, X1, X2	2.2		V_{DD}	V
	V_{IH2}	RESET, P10/NMI, X1, X2	0.8 V_{DD}		V_{DD}	V
Output voltage low	V_{OL}	I_{OL} = 1.6 mA			0.45	V
Output voltage high	V_{OH}	I_{OH} = -0.4 mA	V_{DD} -1.0			V
Input current	I_I	EA, P10/NMI; $0 \le V_I \le V_{DD}$			±20	uA
Input leakage current	I_{LI}	Other than EA, P10/NMI; $0 \le V_I \le V_{DD}$			±10	uA
Output leakage current	I_{LO}	$0 \le V_O \le V_{DD}$			±10	uA
V_{TH} current	I_{TH}	$0 V \le V_{TH} \le V_{DD}$		0.5	1.0	mA
V_{DD} supply current	I_{DD1}	Operating mode		95	130	mA
	I_{DD2}	HALT mode		30	55	mA
	I_{DD3}	STOP mode		15	35	uA

AC Characteristics

uPD70325(A)-9 (Ta = -40 to +85°C, V_{DD} = +5.0 V ±5%)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
X1 input cycle time	t_{CYX}		55	250	ns
X1 input high/low level width	t_{WXH}, t_{WXL}		17		ns
X1 input rising/falling time	t_{XR}, t_{XF}			15	ns
CLKOUT output cycle time	t_{CYK}	$f_X/2$, T = t_{CYK}	111	2000	ns
CLKOUT output high/low level width	t_{WKH}, t_{WKL}		0.5T-12		ns
CLKOUT output rising/falling time	t_{KR}, t_{KF}			12	ns
Input rising/falling time	t_{IR}, t_{IF}	Other than RESET, NMI, X1 and X2		20	ns
	t_{IRS}, t_{IFS}	RESET, NMI		30	ns
Output rising/falling time	t_{OR}, t_{OF}	Other than CLKOUT		15	ns
Address delay time from CLKOUT	t_{DKA}		15	80	ns
Data input delay time from address	t_{DADR}			(n+1.5)T-60	ns
Data delay time from MREQ↓	t_{DMRD}			(n+1)T-50	ns
Data delay time from RSTB↓	t_{DMSD}			(n+0.5)T-50	ns

<div align="right">(to be continued)</div>

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{\text{MSTB}}$ ↑ delay time from $\overline{\text{MREQ}}$ ↓	t_{DMRMS}		0.5T-30	0.5T+30	ns
$\overline{\text{MREQ}}$ low level width	t_{WMRL}		(n+1)T-25	(n+1)T+25	ns
Address hold time (from $\overline{\text{MREQ}}$↑)	t_{HMA}		0.5T-35		ns
Data input hold time (from $\overline{\text{MREQ}}$↑)	t_{HMDR}		0		ns
Control signal recovery time	t_{RVC}		T-25		ns
Data output delay time from address	t_{DADW}			0.5T+50	ns
Address setup time (to $\overline{\text{MREQ}}$↓)	t_{DAMR}		0.5T-35		ns
Address setup time (to $\overline{\text{MSTB}}$↓)	t_{DAMS}		T-30		ns
$\overline{\text{MSTB}}$ low level width	t_{WMSL}		(n+0.5)T-25	(n+0.5)T+25	ns
Data output setup time (to $\overline{\text{MSTB}}$↑)	t_{SDM}		(n+1)T-50		ns
Data output hold time (from $\overline{\text{MSTB}}$↑)	t_{HMDW}		0.5T-35		ns
Address setup time (to $\overline{\text{IOSTB}}$↓)	t_{DAIS}		0.5T-35		ns
Data delay time from $\overline{\text{IOSTB}}$↓	t_{DISD}			(n+1)T-50	ns
$\overline{\text{IOSTB}}$ low level width	t_{WISL}		(n+1)T-25		ns
Address hold time (from $\overline{\text{IOSTB}}$↑)	t_{HISA}		0.5T-30		ns
Data input hold time (from $\overline{\text{IOREQ}}$↑)	t_{HISDR}		0		ns
Data output setup time (to $\overline{\text{IOSTB}}$↑)	t_{SDIS}		(n+1)T-50		ns
Data output hold time (from $\overline{\text{IOSTB}}$↑)	t_{HISDW}		0.5T-35		ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{DMARQ}$ setup time (to $\overline{MREQ}\downarrow$)	t_{SDADQ}	Demand release mode, n ≥ 2		(n-1)T-50	ns
$\overline{DMARQ}$ hold time (from $\overline{DMAAK}\downarrow$)	t_{HDADQ}	Demand release mode	0		ns
$\overline{DMAAK}$ output low level width	t_{WDMRL}	Read operation	(n+1.5)T-25		ns
$\overline{TC}\downarrow$ delay time from $\overline{DMAAK}\downarrow$	t_{DDATC}			0.5T+35	ns
$\overline{TC}$ low level width	t_{WTCL}		(n+2)T-25		ns
$\overline{DMAAK}$ output low level width	t_{WDMWL}	Write operation	(n+1)T-25		ns
Address setup time (to $\overline{REFRQ}\downarrow$)	t_{DARF}		0.5T-35		ns
$\overline{REFRQ}$ low level width	t_{WRFL}		(n+1)T-25		ns
Address hold time (from $\overline{REFRQ}\uparrow$)	t_{HRFA}		0.5T-35		ns
$\overline{RESET}$ low level width	t_{WRSL1}	STOP mode release/power ON reset	30		ns
	t_{WRSL2}	System reset	5		us
READY setup time (to $\overline{MREQ}\downarrow$, $\overline{IOSTB}\downarrow$)	t_{SCRYO}	n ≥ 2		T-80	ns
	t_{SCRY}	n ≥ 3		(n-1)T-80	ns
READY hold time (from $\overline{MREQ}\downarrow$, $\overline{IOSTB}\downarrow$)	t_{HCRYO}	n = 2	T		ns
	t_{HCRY}	n ≥ 3	(n-1)T		ns
	t_{HCRY1}	n ≥ 3	(n-2)T		ns
HLDRQ setup time (to CLKOUT↓)	t_{SHQK}		25		ns
$\overline{HLDAK}\downarrow$ delay time from CLKOUT↓	t_{DKHA}		15	75	ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{\text{HLDAK}}$ delay time from bus float	t_{CFHA}		T-35		ns
Bus output delay time from $\overline{\text{HLDAK}}$	t_{DHAC}		T-35		ns
$\overline{\text{HLDAK}}$ delay time from HLDRQ	t_{DHQHA}			3T+160	ns
Bus output delay time from HLDRQ	t_{DHQC}		3T+30		ns
HLDRQ low level width	t_{WHQL}		1.5T		ns
$\overline{\text{HLDAK}}$ low level width	t_{WHAL}		T		ns
INT, DMARQ setup time (to CLKOUT)	t_{SIQK}		25		ns
INT, DMARQ high/ low level width	t_{WIQH}, t_{WIQL}		8T		ns
$\overline{\text{POLL}}$ setup time (to CLKOUT)	t_{SPLK}		25		ns
NMI high/low level width	t_{WNIH}, t_{WNIL}		5		us
$\overline{\text{CTS}}$ low level width	t_{WCTL}		2T		ns
INT setup time (to CLKOUT)	t_{SIRK}		25		ns
$\overline{\text{INTAK}}$ delay time from CLKOUT	t_{DKIA}		15	75	ns
INT hold time (from $\overline{\text{INTAK}}$)	t_{HAIQ}		0		ns
$\overline{\text{INTAK}}$ low level width	t_{WIAL}		2T-25		ns
$\overline{\text{INTAK}}$ high level width	t_{WIAH}		T-25		ns
Data delay time from $\overline{\text{INTAK}}$	t_{DIAD}			2T-100	ns
Data hold time (from $\overline{\text{INTAK}}$)	t_{HIAD}		0	0.5T	ns
$\overline{\text{SCKO}}$ cycle time	t_{CYTK}		1000		ns
$\overline{\text{SCKO}}$ high/low level width	t_{WSTH}, t_{WSTL}		450		ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
TxD delay time from $\overline{SCKO}$ ↓	t_{DTKD}			210	ns
TxD hold time (from $\overline{SCKO}$ ↓)	t_{HTKD}		20		ns
$\overline{CTSO}$ cycle time	t_{CYRK}		1000		ns
$\overline{CTSO}$ high/low level width	t_{WSRH}, t_{WSRL}		420		ns
RxD setup/hold time (to/from $\overline{CTSO}$ ↓)	t_{SRDK}, t_{HKRD}		80		ns

Remarks: n indicates the number of wait states. No wait is "n = 0".

Comparator Characteristics

uPD70325(A)-9 (Ta = -40 to +85°C, V_{DD} = +5.0 V ±5%)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Comparator accuracy	V_{ACOMP}				±100	mV
Threshold voltage	V_{TH}		0		V_{DD} +0.1	V
Compare time	t_{COMP}		64		65	t_{CYK}
PT input voltage	V_{IPT}		0		V_{DD}	V

Data Memory STOP Mode Low Supply Voltage Data Holding
Characteristics (Ta = -40 to +85°C)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Data hold supply voltage	V_{DDDR}		2.5	5.5	V
V_{DD} rising/falling time	t_{RVD}, t_{FVD}		200		us

3.4 V25 Family Timing Wafeforms

DATA HOLDING TIMING
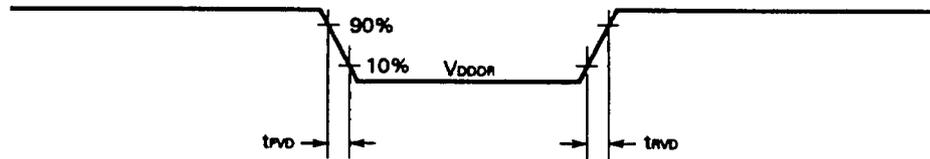
AC TEST INPUT WAVEFORM (EXCEPT RESET, NMI, X1 AND X2)
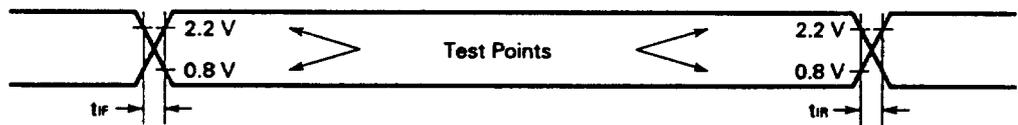
AC TEST INPUT WAVEFORM (RESET, NMI, X1 AND X2)
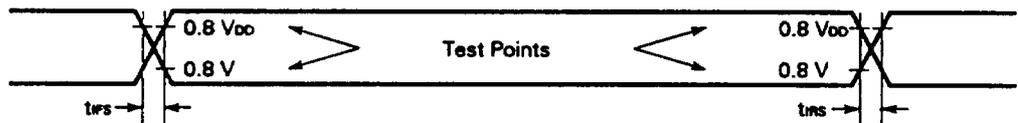
AC TEST OUTPUT TEST POINTS

Output and condition: 100 pF
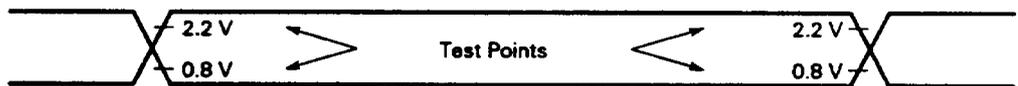
CLOCK TIMING
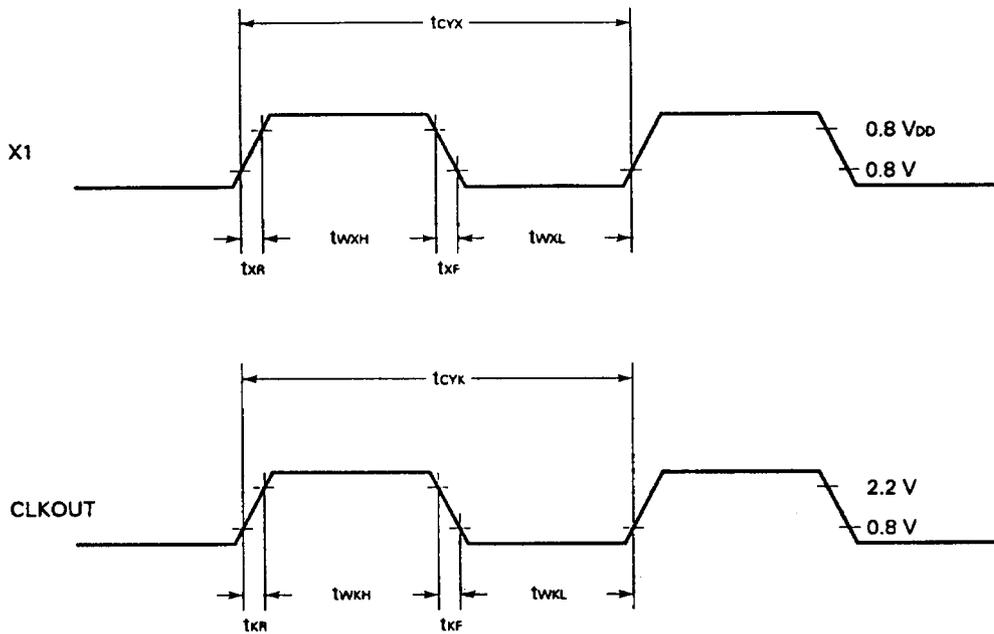
POLL INPUT TIMING
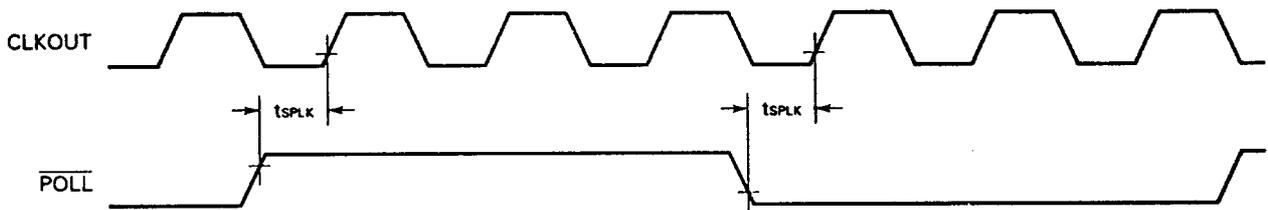
CTS0 AND CTS1 INPUT TIMING

INTERRUPT INPUT/DMA INPUT TIMING
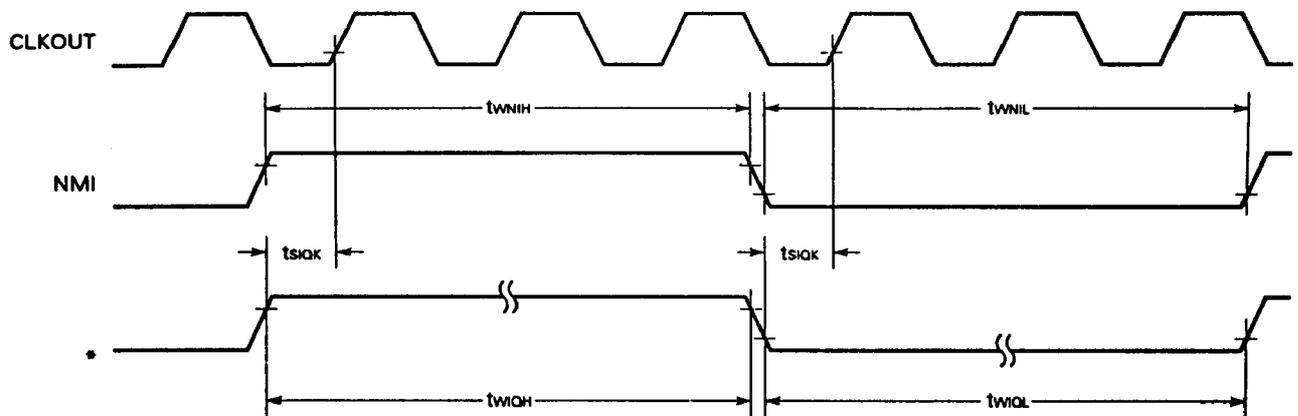
* $\overline{\text{INTP0}}$-$\overline{\text{INTP2}}$, DMARQ0-DMARQ1

$\overline{\text{RESET}}$ INPUT TIMING

When STOP mode is released/at power-on reset:
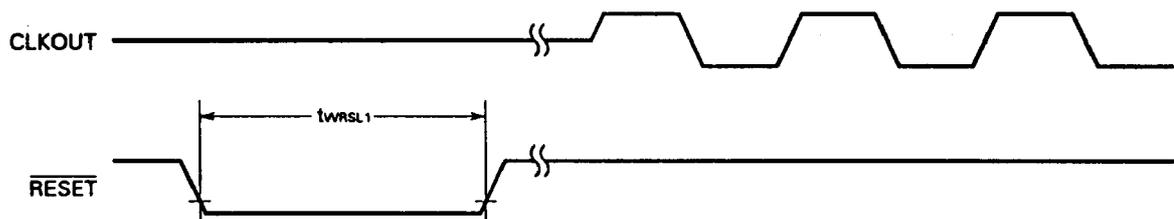
When system is reset:
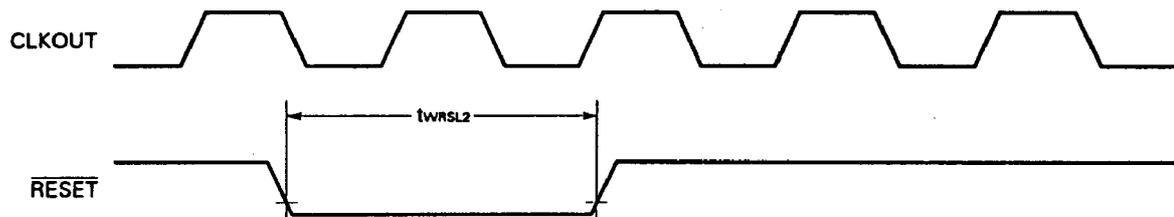
READY TIMING

When 2 wait states are inserted:
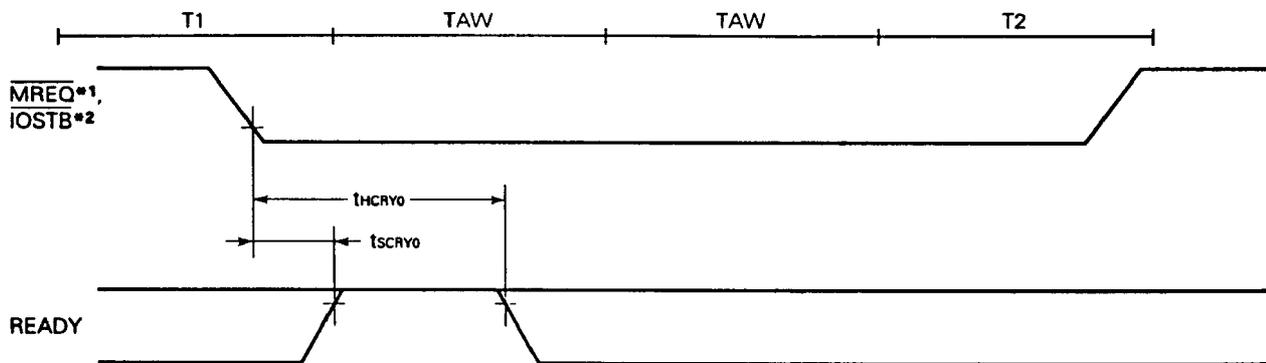
When (n − 2) extra wait states are inserted [n ≥ 3]:
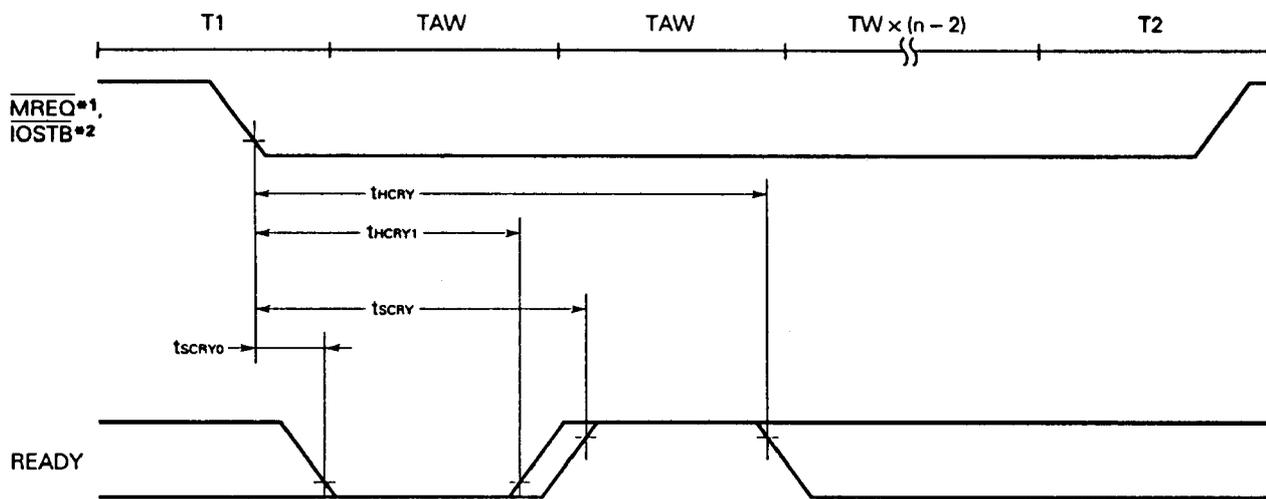
*1. In case of memory cycle
2. In case of I/O cycle

SERIAL OPERATION

When transmitting data in I/O interface mode
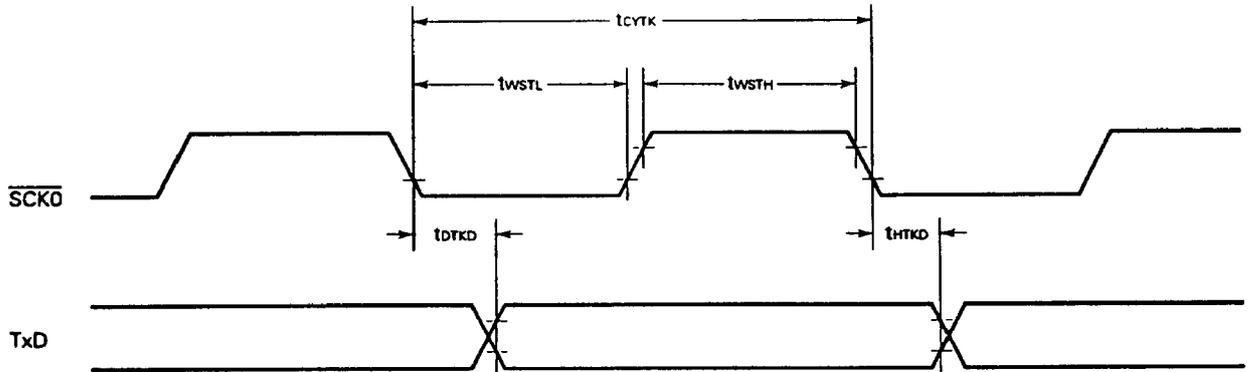
When receiving data in I/O interface mode
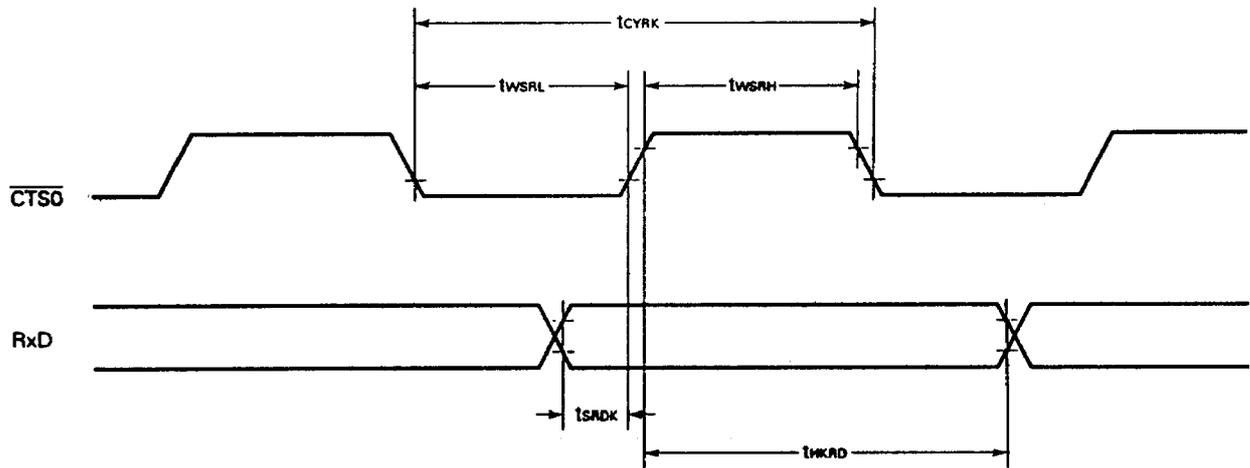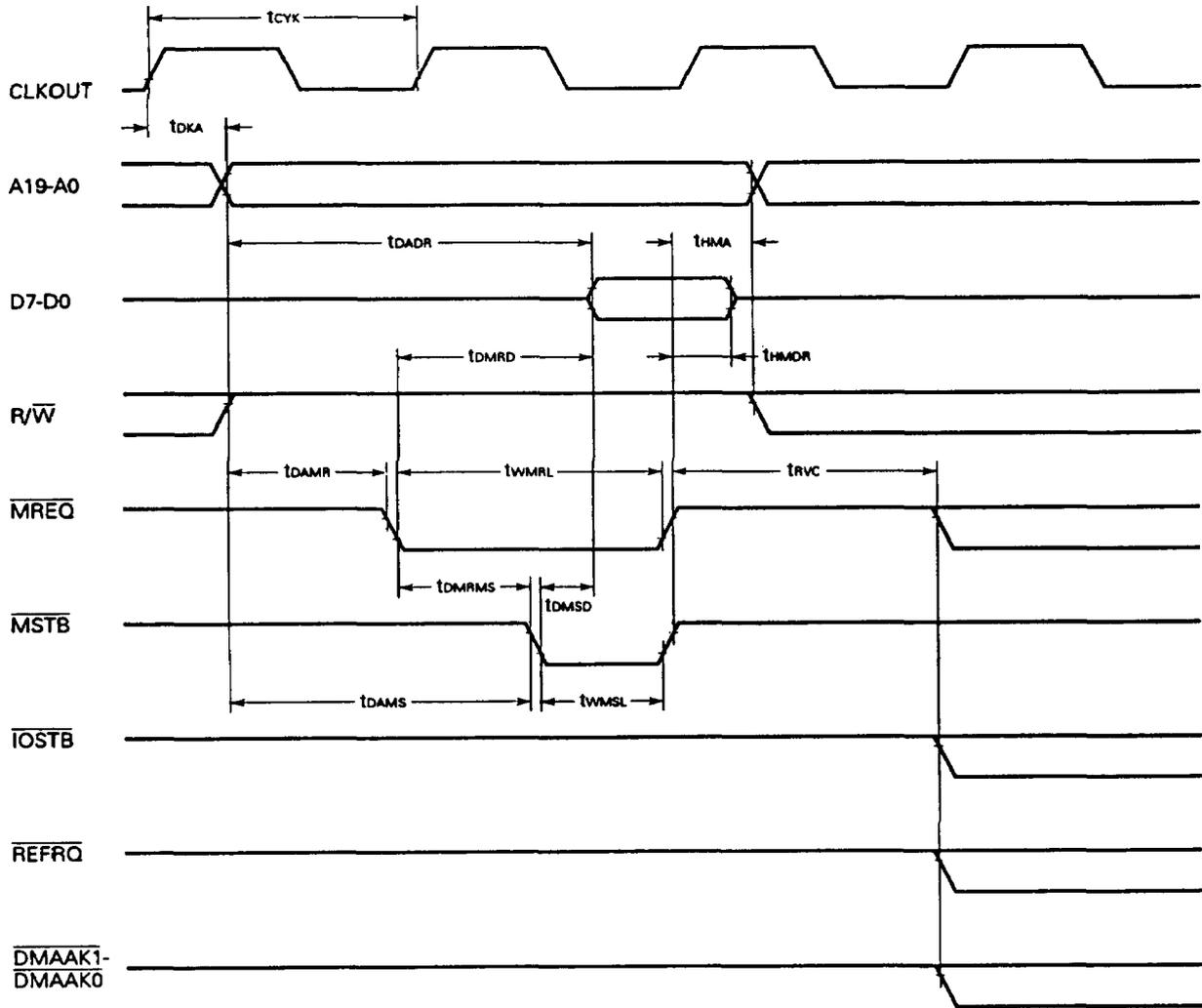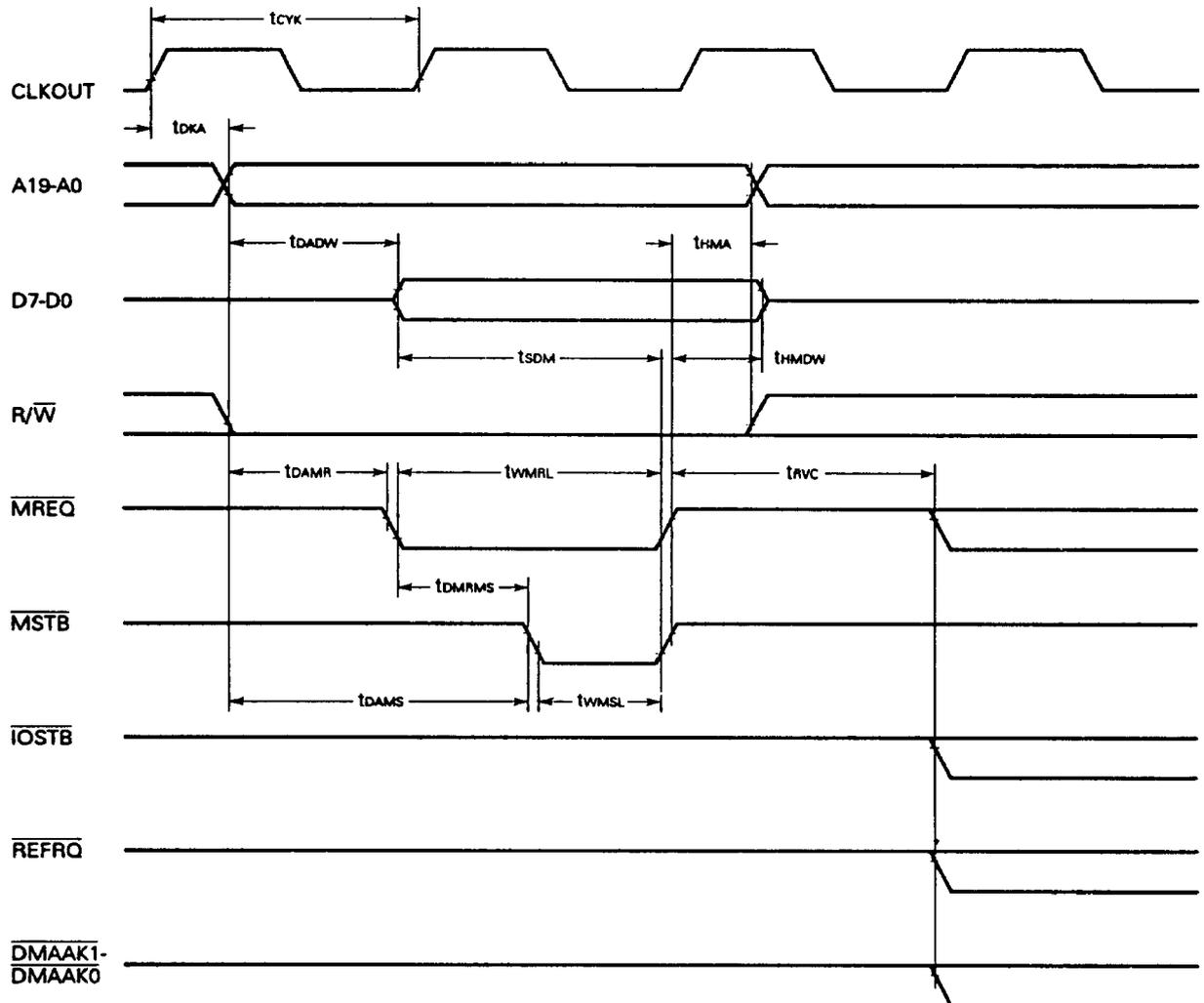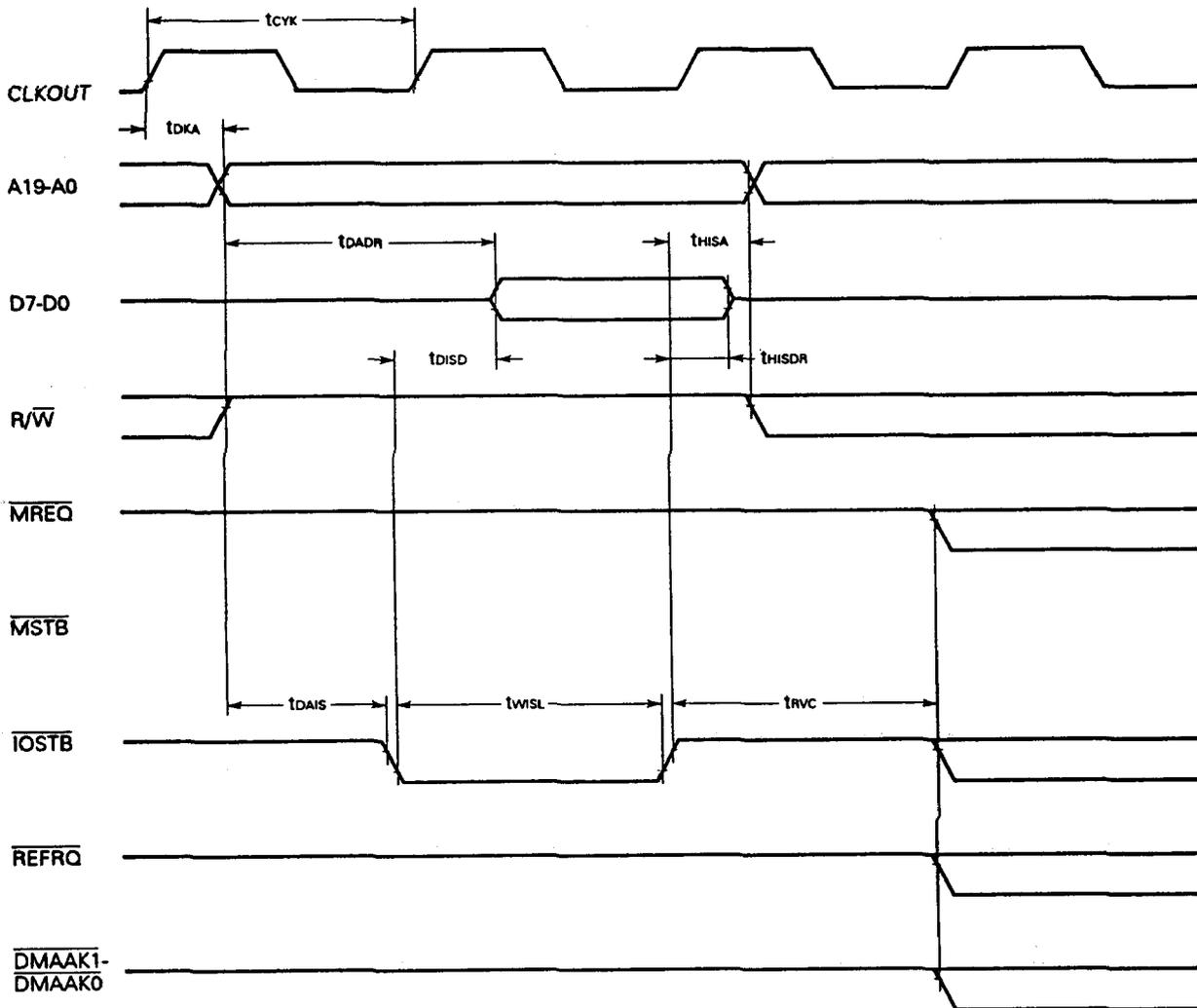
READ OPERATION

WRITE OPERATION

I/O READ TIMING

I/O WRITE TIMING
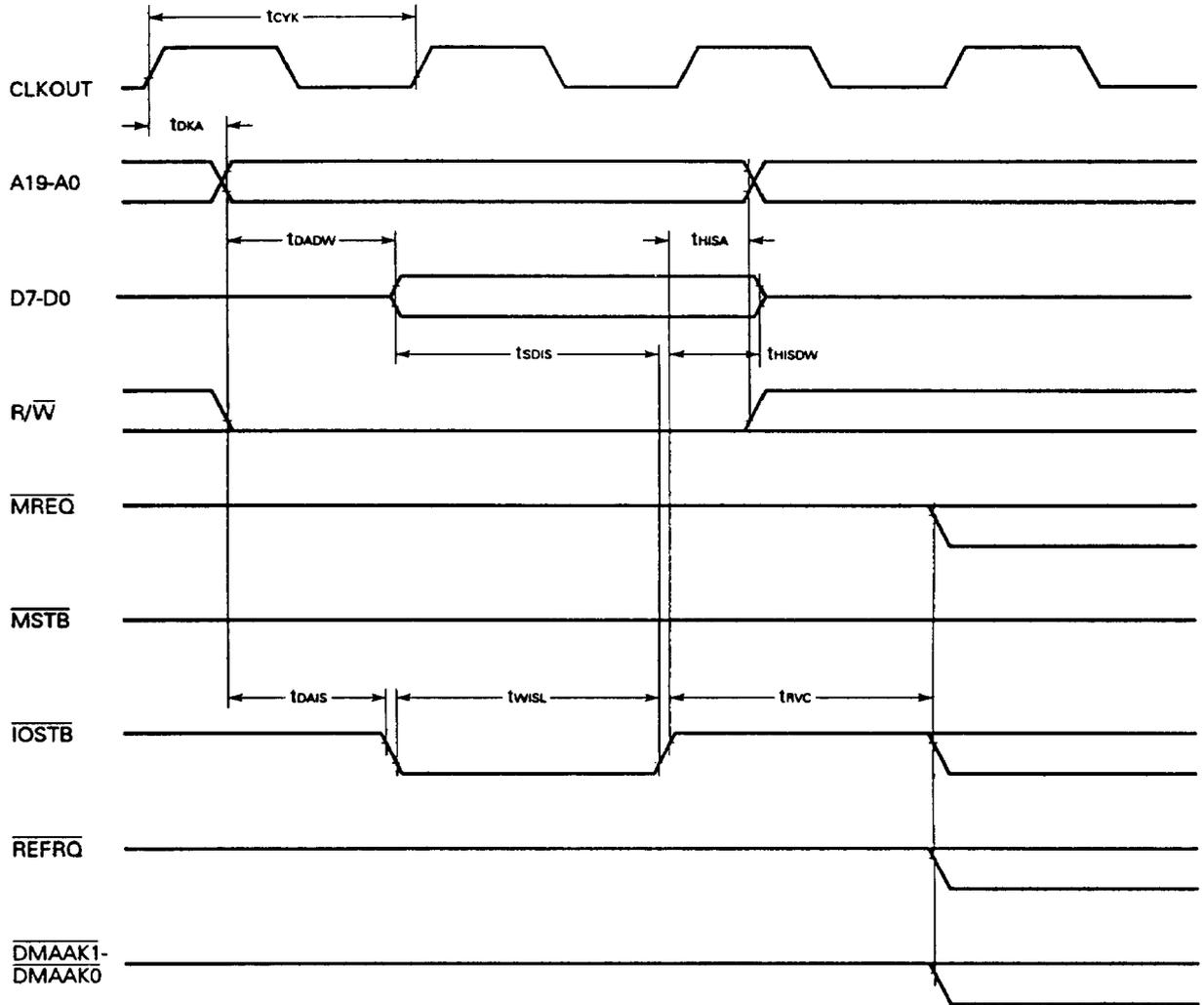
DMA (I/O → MEMORY) TIMING
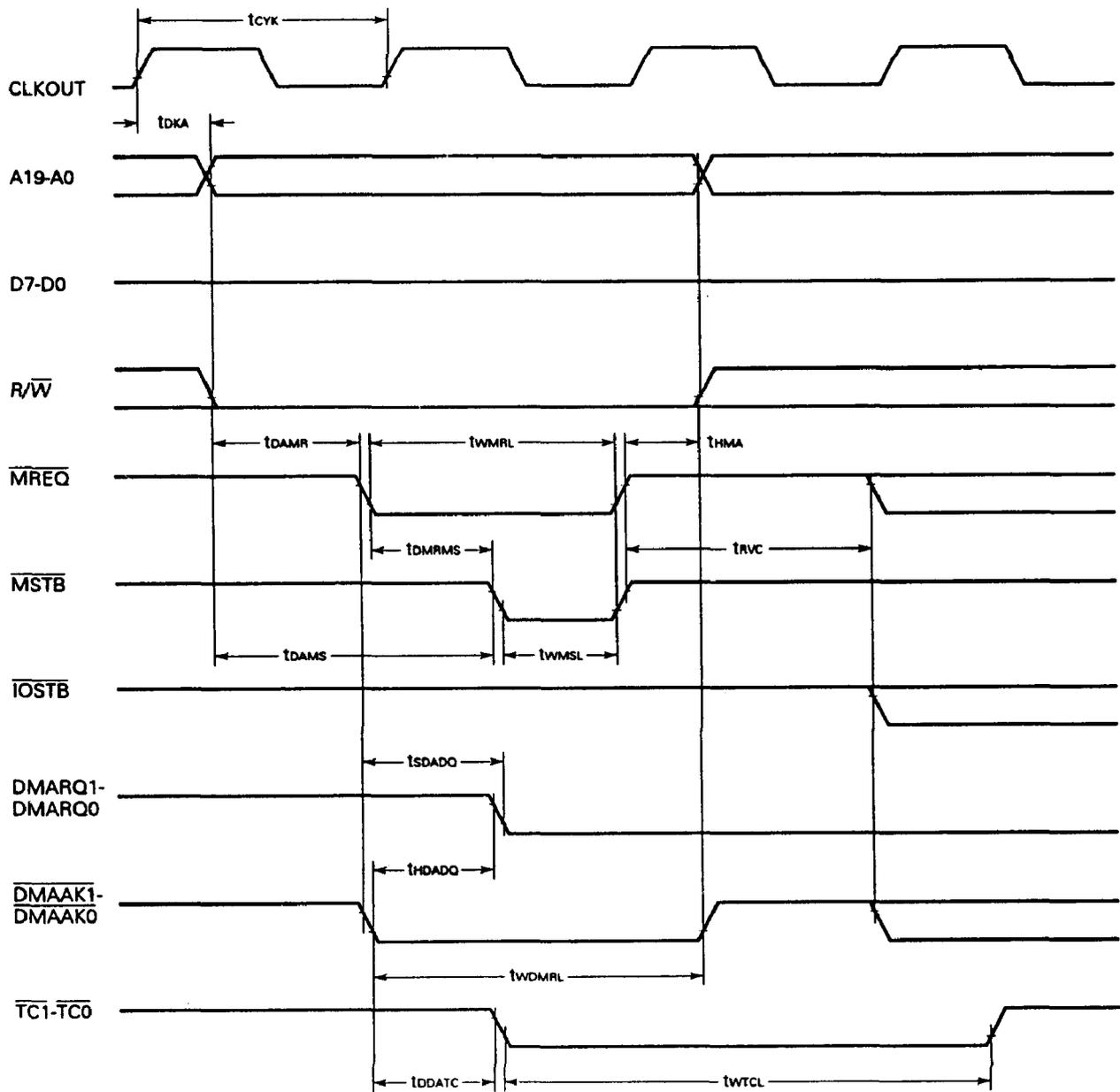
DMA (MEMORY → I/O) TIMING
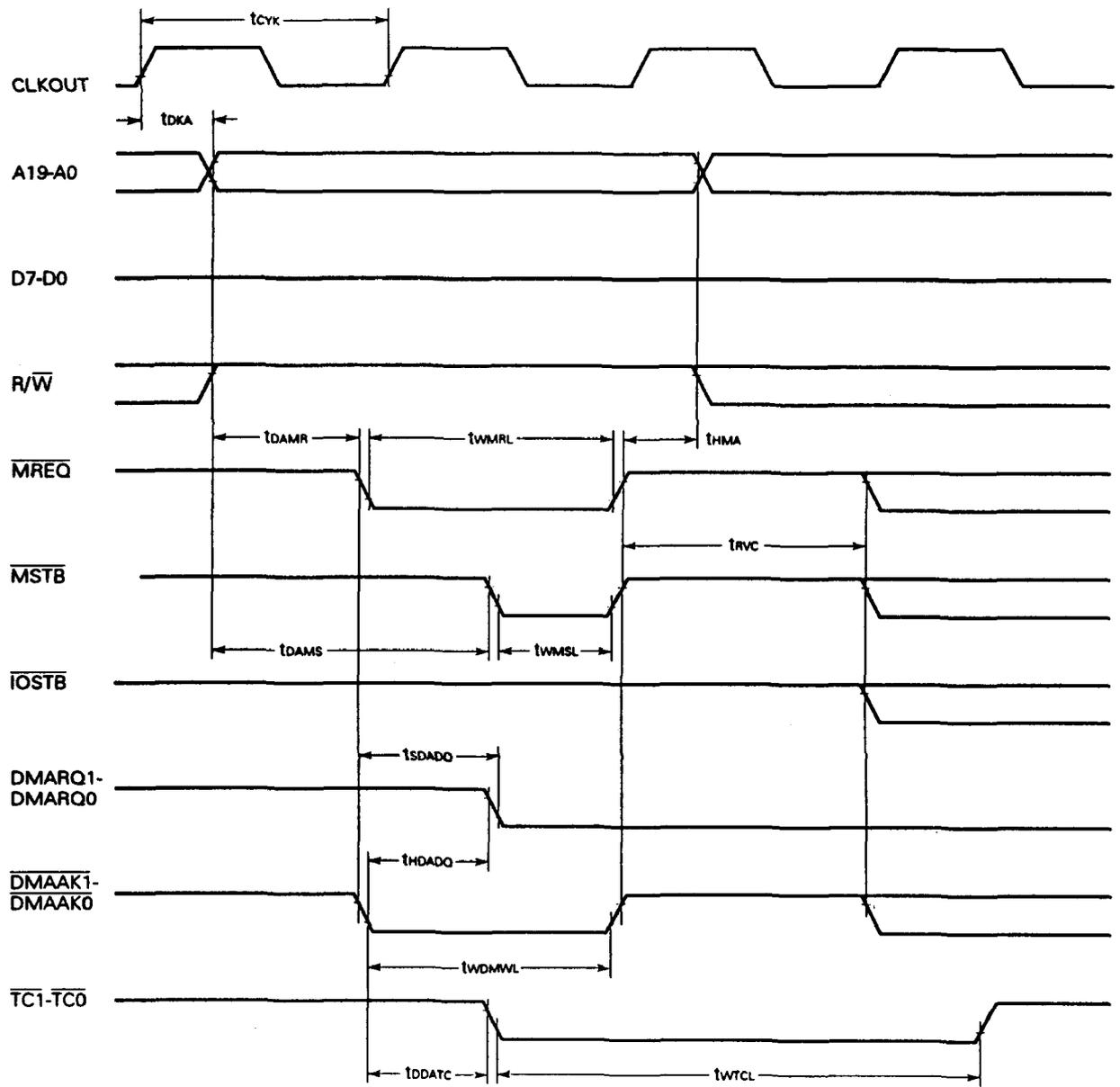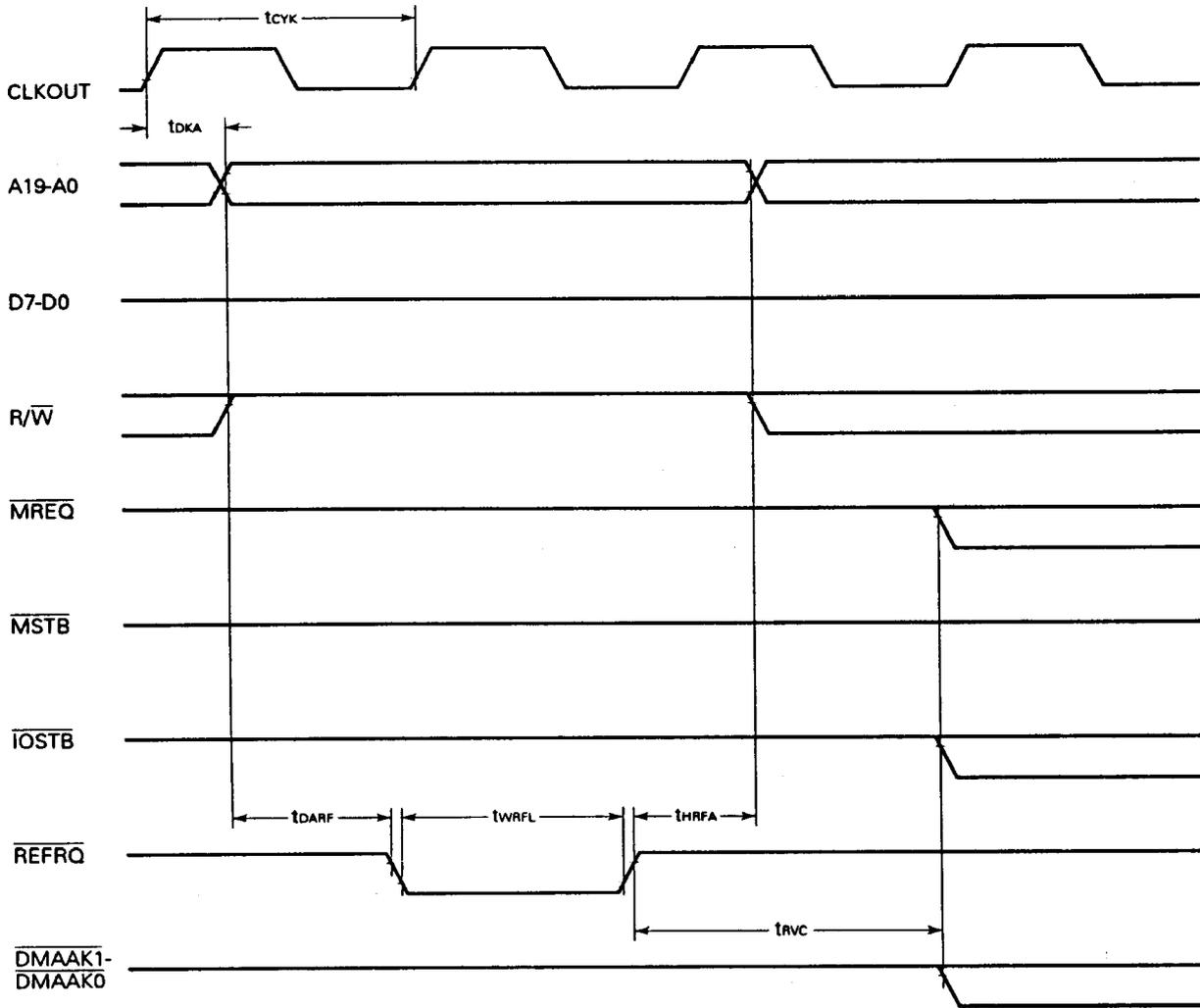
REFRESH TIMING

HOLD REQUEST/ACKNOWLEDGE TIMING

Normal mode
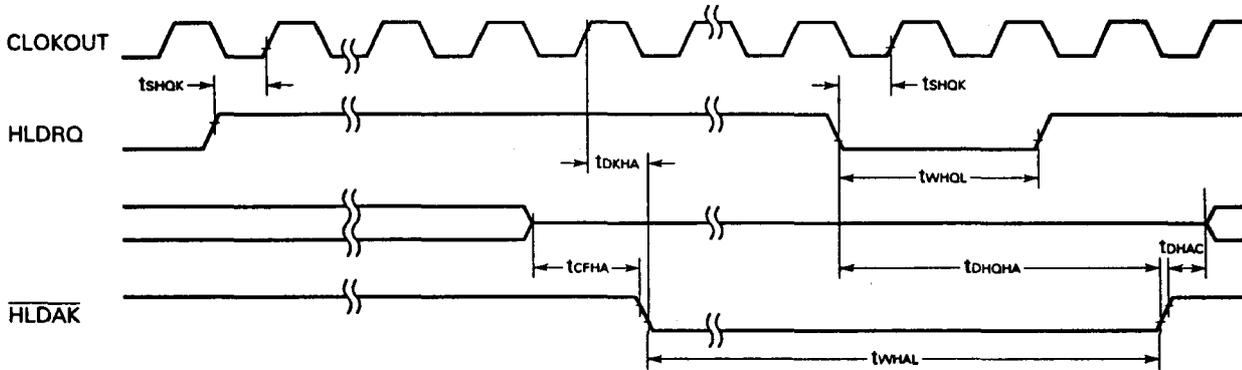
Releasing HOLD mode at refreshing time
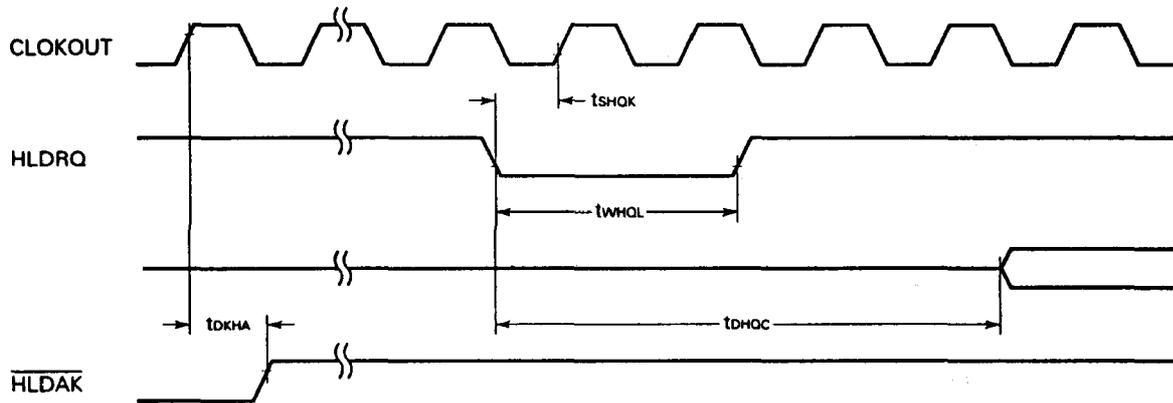
* A19 to A0, D7 to D0, $\overline{MREQ}$, $\overline{MSTB}$, $\overline{IOSTB}$, R/$\overline{W}$

EXTERNAL INTERRUPT REQUEST/ACKNOWLEDGE TIMING
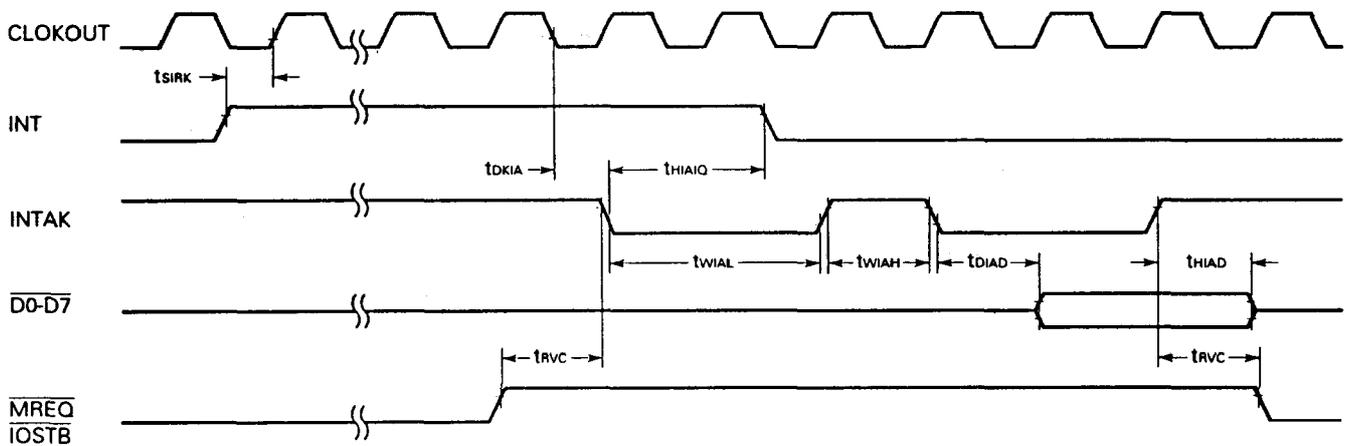
3.5 FOR μPD70330, μPD70330(A), μPD70332, μPD70332(A), μPD70337, μPD79021

ABSOLUTE MAXIMUM RATINGS (T$_a$ = 25 °C)

PARAMETER	SYMBOL	TEST CONDITION	RATINGS	UNIT
Supply Voltage	V$_{DD}$		−0.5 to +7.0	V
Input Voltage	V$_{TH}$		−0.5 to V$_{DD}$ + 0.5	V
	V$_I$		−0.5 to V$_{DD}$ +0.5	V
Output Voltage	V$_O$		−0.5 to V$_{DD}$ +0.5	V
Output Low Current	I$_{OL}$	Each output pin	4.0	mA
		Total	50	mA
Output High Current	I$_{OH}$	Each output pin	−2.0	mA
		Total	−20	mA
Operation Temperature	T$_{opt}$		−40 to +85	°C
Storage Temperature	T$_{stg}$		−65 to +150	°C

OSCILLATOR CHARACTERISTICS

(T$_a$ = −40 °C to +85 °C, V$_{DD}$ = +5.0 V ± 10%, V$_{SS}$ = 0 V, 0 V ≤ V$_{TH}$ ≤ V$_{DD}$ + 0.1 V)

CONFIGURATION	RECOMMENDED CIRCUIT	PARAMETER	MIN.	MAX.	UNIT
Internal Oscillator (Ceramic[Note 1] or Crystal Resonator[Note 2])		Oscillation frequency (f$_{XX}$)	4	16	MHz
External Clock		X1 input frequency (f$_X$)	4	16	MHz
		X1 rise, fall time (t$_{XR}$, t$_{XF}$)	0	20	ns
		X1 input high, low level width (t$_{WXH}$, t$_{WXL}$)	20	250	ns

Caution 1. Mount the capacitors and crystal or ceramic resonator as close to pins X1 and X2 as possible.
2. Do not route other signal lines through the ▢ area.

Recommended Oscillator Constants

Ceramic resonator

Manufacturer	Product number	Recommended constants	
		C1 (pF)	C2 (pF)
Kyocera	KBR-10.0M Note 1	33	33
Murata	CSA7.37MT040 Note 2	100	100
	CSA10.0MT Note 1	47	47
	CSA11.0MT Note 2		
	CSA16.0MX040 Note 1	30	30
TDK	FCR10.0M2S Note 2	30	30
	FCR16.0M2S Note 2	15	6
	FCR16.0M2G Note 2	22	10

Note 1. The operation temperature range is −10 to +70 °C if these oscillators are used.

2. The operation temperature range is −20 to +80 °C if these oscillators are used.

Crystal resonator

Manufacturer	Product number	Recommended constants	
		C1 (pF)	C2 (pF)
Kinseki	HC-49/U(KR-100)	22	22
	HC-49/U(KR-160)	22	22

Remark For such as characteristics of each resonator, confirm to the each manufacturer.

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_I	f_c = 1 MHz Unmeasured pins returned to 0 V			10	pF
Output Capacitance	C_O				20	pF
Input/output Capacitance	C_{IO}				20	pF

DC CHARACTERISTICS (T_a = −40 °C to +85 °C, V_{DD} = +5.0 V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	Except $\overline{RESET}$, P10/NMI, X1, or X2	2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P10/NMI, X1, X2	0.8 V_{DD}		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −0.4 mA	V_{DD} −1.0			V
Input Current	I_I	EA, P10/NMI; 0 ≤ V_I ≤ V_{DD}			±20	µA
Input Leakage Current	I_{LI}	Except $\overline{EA}$, P10/NM; 0 ≤ V_I ≤ V_{DD}			±10	µA
Output Leakage Current	I_{LO}	0 ≤ V_O ≤ V_{DD}			±10	µA
V_{TH} Current	I_{TH}	0 V ≤ V_{TH} ≤ V_{DD}		0.5	1.0	mA
V_{DD} Supply Current	I_{DD1}	Operation mode		65	120	mA
	I_{DD2}	HALT mode		25	50	mA
	I_{DD3}	STOP mode		10	30	µA

AC CHARACTERISTICS (T$_a$ = −40 °C to +85 °C, V$_{DD}$ = +5.0 V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
X1 Input Cycle Time	tCYX		62	250	ns
X1 Input High Low Level Width	tWXH, tWXL		20		ns
X1 Input Rise, Fall Time	tXR, tXF			20	ns
CLKOUT Output Cycle Time	tCYK	fx/2, T = tCYK	125	2000	ns
CLKOUT Output High, Low Level Width	tWKH, tWKL		0.5T−15		ns
CLKOUT Output Rise, Fall Time	tKR, tKF			15	ns
Input Rise, Fall Time	tIR, tIF	Except $\overline{RESET}$, MNI, X1, X2		20	ns
	tIRS, tIFS	$\overline{RESET}$, NMI		30	ns
Output Rise, Fall Time	tOR, tOF	Except CLKOUT		2	ns
CLKOUT → Address Delay Time	tDKA			90	ns
Address → Data Input Delay Time	tDADR			(n+1.5)T−90	ns
$\overline{MREQ}$ ↓ → Data Delay Time	tDMRD			(n+2)T−75	ns
$\overline{MSTB}$ ↓ → Data Delay Time	tDMSD			(n+1)T−75	ns
$\overline{MREQ}$ ↓ → $\overline{MSTB}$ ↓ Data Delay Time	tDMRMS1	Read operation	T−35	T+35	ns
	tDMRMS2	Write operation	(n+1)T−35	(n+1)T+35	ns
$\overline{MREQ}$ Low Level Width	tWMRL		(n+2)T−30	(n+2)T+30	ns
$\overline{MREQ}$ ↓ → Address Hold Time	tHMRA		0.5T−30		ns
Address Hold Time from $\overline{MREQ}$ ↑	tHMA		0.5T−30		ns
Data Input Hold Time from $\overline{MREQ}$ ↑	tHMDR		0		ns
Control Signal Recovery Time	tRVC		T−25		ns
Address → Data Output Delay Time	tDADW			0.5T+50	ns

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Address Setting Time from MREQ ↓	tDAMR		0.5T–30		ns
R/W → MSTB ↓ Delay Time	tDRMS		0.5T–30		ns
	tDWMS		(n+0.5)T–30		ns
MSTB Low Level Width	tWMSL1	Read operation	(n+1)T–30		ns
	tWMSL2	Write operation	1T–30	1T+30	ns
Data Output Set Up Time to MSTB ↑	tSDM		(n+2)T–50		ns
Address Setting Time from IOSTB ↓	tDAIS		0.5T–30		ns
IOSTB ↓ → Data Delay Time	tDISD			(n+1)T–90	ns
MREQ ↓ → IOSTB ↓ Delay Time	tDMRIS		1T–35		ns
IOSTB Low Level Width	tWISL		(n+1)T–30		ns
Address Hold Time from IOSTB ↑	tHISA		0.5T–30		ns
Data Input Hold Time from IOSTB ↑	tHISDR		0		ns
Data Output Setup Time from IOSTB ↑	tSDIS		(n+2)T–50		ns
DMARQ Setup Time from MREQ ↓	tSDADQ	Demand release mode		1T	ns
DMARQ Hold Time from DMAAK ↓	tHDADQ	Demand release mode	0		ns
DMAAK Output Low Level Width	tWDMRL	Read operation	(n+2.5)T–30		ns
DMAAK ↓ → TC ↓ Delay Time	tDDATC			0.5T+50	ns
TC Low Level Width	tWTCL		2T–30		ns
DMAAK Output Low Level Width	tWDMWL	Write operation	(n+2)T–30		ns
Address Setting Time from REFRQ ↓	tDARF		0.5T–30		ns
REFRQ Low Level Width	tWRFL		(n+2)T–30		ns
Address Hold Time from REFRQ ↑	tHRFA		0.5T–30		ns

PARAMETER	SYMBOL	TEST CONDITION	MAX.	MAX.	UNIT
RESET Low Level Width	t_{WRSL1}	STOP mode release/ power-on reset	30		ms
	t_{WRSL2}	System reset	5		μs
READY Setup Time (MREQ ↓)	t_{SCRY0}	n ≥ 2		2T–100	ns
	t_{SCRY}	n ≥ 3		nT–100	ns
READY Hold Time (MREQ ↓)	t_{HCRY0}	n = 2	2T		ns
	t_{HCRY}	n ≥ 3	nT		ns
	t_{HCRY1}	n ≥ 3	(n–1)T		ns
READY Setup Time (IOSTB ↓)	t_{SSRY0}	n ≥ 2		T–100	ns
	t_{SSRY}	n ≥ 3		(n–1)T–100	ns
READY Hold Time (IOSTB ↓)	t_{HSRY0}	n = 2	1T		ns
	t_{HSRY}	n ≥ 3	(n–1)T		ns
	t_{HSRY1}	n ≥ 3	(n–2)T		ns
HLDRQ Setup Time to CLKOUT ↑	t_{SHQK}		30		ns
CLKOUT ↑ → HLDAK , Delay Time	t_{DKHA}			80	ns
Bus Float → HLDAK ↓ Delay Time	t_{CFHA}		1T–50		ns
HLDAK ↑ → Bus Output Delay Time	t_{DHAC}		1T–50		ns
HLDRQ ↓ → HLDAK ↑ Delay Time	t_{DHQHA}			3T+160	ns
HLDRQ ↓ → Bus Output Delay Time	t_{DHQC}		3T+30		ns
HLDRQ Low Level Width	t_{WHQL}		1.5T		ns
HLDAK Low Level Width	t_{WHAL}		1T		ns
INTDMARQ Setup Time to CLKOUT ↑	t_{SIQK}		30		ns
INTDMARQ High, Low Level Width	t_{WIQH}, t_{WIQL}		8T		ns

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
POLL Setup Time to CLKOUT ↑	tSPLK		30		ns
NMI High, Low Level Width	tWNIH, tWNIL		5		μs
CTS Low Level Width	tWCTL		2T		ns
INT Setup Time to CLKOUT ↑	tSIRK		30		ns
CLKOUT ↓ → INTAK ↓ Delay Time	tDKIA			80	ns
INT Hold Time to INTAK ↓	tHIAIQ		0		ns
INTAK Low Level Width	tWIAL		2T−30		ns
INTAK High Level Width	tWIAH		1T−30		ns
INTAK ↓ → Data Delay Time	tDIAD			2T−130	ns
Data Hold Time from INTAK ↑	tHIAD		0	0.5T	ns
SCK0 Cycle Time	tCYTK		1000		ns
SCK0 High, Low Level Width	tWSTH, tWSTL		450		ns
SCK0 ↓ → TxD Delay Time	tDTKD			210	ns
SCK0 ↓ → TxD Hold Time	tHTKD		20		ns
CTS0 Cycle Time	tCYRK		1000		ns
CTS0 High Low Level Width	tWSRH, tWSRL		420		ns
RxD Setup Hold Time (CTS0 ↑)	tSRDK, tHKRD		80		ns

Remark n denotes the number of wait states. n = 0 denotes no wait.

COMPARATOR CHARACTERISTICS (Ta = −40 °C to +85 °C, VDD = +5.0 V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Comparison Accuracy	VACOMP				±100	mV
Threshold Voltage	VTH		0		VDD+0.1	V
Comparison time	tCOMP		64		65	tCYK
PT Input Voltage	VIPT		0		VDD	V

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION
(Ta = −40 °C to +85 °C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Data Retention Supply Voltage	VDDDR		2.5	5.5	V
VDD Rise, Fall Time	tRVD, tFVD		200		μs

3.6 FOR μPD70335-8, μPD70335-10

Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Test condition	Ratings	Unit
Power supply voltage	V_{DD}		-0.5 to +7.0	V
	V_{TH}		-0.5 to V_{DD}+0.5	V
Input voltage	V_I		-0.5 to V_{DD}+0.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Output low current	I_{OL}	Per pin	4.0	mA
		Total, all output	50	mA
Output high current	I_{OH}	Per pin	-2.0	mA
		Total, all output	-20	mA
Operation temperature	T_{opt}		-10 to +70	°C
Storage temperature	T_{stg}		-65 to +150	°C

Oscillator characteristics

uPD70335-8 (Ta=-10 to +70°C, V_{DD}=+5.0V$\pm$10%, V_{SS}=0V,
$0V \leq V_{TH} \leq V_{DD}$+0.1V)

uPD70335-10 (Ta=-10 to +70°C, V_{DD}=+5.0V$\pm$5%, V_{SS}=0V,
$0V \leq V_{TH} \leq V_{DD}$+0.1V)

Resonator	Recommended circuit	Parameter	uPD70335-8		uPD70335-10		Unit
			MIN.	MAX.	MIN.	MAX.	
Ceramic resonator or crystal resonator		Oscillation frequency (f_{XX})	4	16	4	20	MHz
External clock		X1 input frequency (f_X)	4	16	4	20	MHz
		X1 input rising, falling time (t_{XR}, t_{XF})	0	20	0	15	ns
		X1 input high, low level width (t_{WXH}, t_{WXL})	20		16		ns

Remarks 1: Put the oscillator near to the X1 and X2 pins as much as possible.

2: Do not pass any other signal line through the shaded area.

Recommended oscillator constant

(1)   The following ceramic resonators and external capacitors are recommended:

Manufacturer	Part number	Recommended constant	
		C1[pF]	C2[pF]
MURATA	CSA16.00MX040	30	30
	CSA20.00MX040	10	10
TDK	FCR16.0M2G	30	30

(2)   The following crystal resonators and external capacitors are recommended:

Manufacturer	Part number	Recommended constant	
		C1[pF]	C2[pF]
KINSEKI	HC-49/U (KR-100)	22	22
	HC-49/U (KR-160)	22	22
	HC-49/U (KR-200)	22	22

Remarks: For such as characteristics of each oscillator, confirm to the each maker.

Capacitance (Ta=25°C, V_{DD}=0 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C=1 MHz Unmeasured pins returned to 0 V			10	pF
Output capacitance	C_O				20	pF
Input/output capacitance	C_{IO}				20	pF

DC characteristics

uPD70335-8   (Ta=-10 to +70°C, V_{DD}=+5.0V±10%)

uPD70335-10 (Ta=-10 to +70°C, V_{DD}=+5.0V±5%)

Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}			0		0.8	V
Input high voltage	V_{IH1}	Except for $\overline{RESET}$, P10/NMI, X1, or X2		2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P10/NMI, X1, X2		$0.8V_{DD}$		V_{DD}	V
Output low voltage	V_{OL}	I_{OL}=1.6 mA				0.45	V
Output high voltage	V_{OH}	I_{OH}=-0.4 mA		V_{DD}-1.0			V
Input current	I_I	EA, P10/NMI;0 ≤ V_I ≤ V_{DD}				±20	uA
Input leakage current	I_{LI}	Except for EA or P10/NMI; 0 ≤ V_I ≤ V_{DD}				±10	uA
Output leakage current	I_{LO}	0 ≤ V_O ≤ V_{DD}				±10	uA
V_{TH} current	I_{TH}	0 V ≤ V_{TH} ≤ V_{DD}			0.5	1.0	mA
V_{DD} power supply current	I_{DD1}	Operation mode	uPD70335-8		65	120	mA
			uPD70335-10		95	130	
	I_{DD2}	HALT mode	uPD70335-8		25	50	mA
			uPD70335-10		30	55	
	I_{DD3}	STOP mode			10	30	uA

AC characteristics

(1) uPD70335-8 (Ta=-10 to +70°C, V_{DD}=+5.0V±10%)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
X1 input cycle time	t_{CYX}		62	250	ns
X1 input high, low level width	t_{WXH}, t_{WXL}		20		ns
X1 input rising, falling time	t_{XR}, t_{XF}			20	ns
CLKOUT output cycle time	t_{CYK}	$f_X/2$, T=t_{CYK}	125	200	ns
CLKOUT output high, low level width	t_{WKH}, t_{WKL}		0.5T-15		ns
CLKOUT output rising, falling time	t_{KR}, t_{KF}			15	ns
Input rising, falling time	t_{IR}, t_{IF}	Except for $\overline{RESET}$, NMI, X1 or X2		20	ns
	t_{IRS}, t_{IFS}	$\overline{RESET}$, NMI		30	ns
Output rising, falling time	t_{OR}, t_{OF}	Except for CLKOUT		20	ns

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
CLKOUT → address delay time	t_{DKA}		15	90	ns
Address → data input delay time	t_{DADR}			$(n+1.5)T-70$	ns
$\overline{MREQ}$ ↓ → data delay time	t_{DMRD}			$(n+2)T-60$	ns
$\overline{MSTB}$ ↓ → data delay time	t_{DMSD}			$(n+1)T-60$	ns
$\overline{MREQ}$ ↓ → $\overline{MSTB}$ ↓ delay time	t_{DMRMS1}	Read operation	$T-35$	$T+35$	ns
	t_{DMRMS2}	Write operation	$(n+1)T-35$	$(n+1)T+35$	ns
$\overline{MREQ}$ low level width	t_{WMRL}		$(n+2)T-30$	$(n+2)T+30$	ns
$\overline{MREQ}$ ↓ → Address hold time	t_{HMRA}		$0.5T-30$		ns
Address hold time from $\overline{MREQ}$ ↑	t_{HMA}		$0.5T-30$		ns
Data input hold time from $\overline{MREQ}$ ↑	t_{HMDR}		0		ns
Control signal recovery time	t_{RVC}		$T-25$		ns
Address → data output delay time	t_{DADW}		$0.5T-35$	$0.5T+50$	ns
Address setup time to $\overline{MREQ}$ ↓	t_{DAMR}		$0.5T-30$		ns
Second address setup time to $\overline{MSTB}$ ↓	t_{DRMS}	Read operation	$0.5T-30$		ns
	t_{DWMS}	Write operation	$(n+0.5)T-30$		ns
$\overline{MSTB}$ low level width	t_{WMSL1}	Read operation	$(n+1)T-30$		ns
	t_{WMSL2}	Write operation	$T-30$	$T+30$	ns
Data output setup time to $\overline{MSTB}$ ↑	t_{SDM}		$(n+2)T-50$		ns
Address setup time to $\overline{IOSTB}$ ↓	t_{DAIS}		$0.5T-30$		ns
$\overline{IOSTB}$ ↓ → data delay time	t_{DISD}			$(n+1)T-60$	ns
$\overline{MREQ}$ ↓ → $\overline{IOSTB}$ ↓ delay time	t_{DMRIS}		$T-35$		ns
$\overline{IOSTB}$ low level width	t_{WISL}		$(n+1)T-30$		ns
Address hold time from $\overline{IOSTB}$ ↑	t_{HISA}		$0.5T-30$		ns
Data input hold time from $\overline{IOSTB}$ ↑	t_{HISDR}		0		ns
Data output setup time to $\overline{IOSTB}$ ↑	t_{SDIS}		$(n+2)T-50$		ns
$\overline{DMARQ}$ setup time to $\overline{MREQ}$ ↓	t_{SDADQ}	Demand release mode, $n \geq 2$		$(n-1)T-50$	ns
$\overline{DMARQ}$ hold time from $\overline{DMAAK}$ ↓	t_{HDADQ}	Demand release mode	0		ns
$\overline{DMAAK}$ output low level width	t_{WDMRL}		$(n+2.5)T-30$		ns
$\overline{DMAAK}$ ↓ → $\overline{TC}$ ↓ delay time	t_{DDATC}			$0.5T+50$	ns
$\overline{TC}$ low level width	t_{WTCL}		$(n+3)T-30$		ns
$\overline{DMAAK}$ output low level width	t_{WDMWL}		$(n+2)T-30$		ns
Address setup time to $\overline{REFRQ}$ ↓	t_{DARF}		$0.5T-30$		ns
$\overline{REFRQ}$ low level width	t_{WRFL}		$(n+2)T-30$		ns
Address hold time from $\overline{REFRQ}$ ↑	t_{HRFA}		$0.5T-30$		ns

Remarks: n denotes the number of wait states. When no wait states are inserted, n is 0.

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low level width	t_{WRSL1}	STOP mode release or power on reset	30		ms
	t_{WRSL2}	System reset	5		us
READY setup time to $\overline{\text{MREQ}}$ ↓	t_{SCRY0}	n≦2		2T-100	ns
	t_{SCRY}	n≧3		nT-100	ns
READY hold time from $\overline{\text{MREQ}}$ ↓	t_{HCRY0}	n=2	2T		ns
	t_{HCRY}	n≧3	nT		ns
	t_{HCRY1}	n≧3	(n-1)T		ns
READY setup time to $\overline{\text{IOSTB}}$ ↓	t_{SSRY0}	n≧2		T-100	ns
	t_{SSRY}	n≧3		(n-1)T-100	ns
READY hold time from $\overline{\text{IOSTB}}$ ↓	t_{HSRY0}	n=2	T		ns
	t_{HSRY}	n≧3	(n-1)T		ns
	t_{HSRY1}	n≧3	(n-2)T		ns
HLDRQ setup time from CLKOUT ↓	t_{SHQK}		30		ns
CLKOUT ↑ → $\overline{\text{HLDAK}}$ ↓ delay time	t_{DKHA}		15	80	ns
Bus float → $\overline{\text{HLDAK}}$ ↓ delay time	t_{CFHA}		T-50		ns
$\overline{\text{HLDAK}}$ ↑ → bus output delay time	t_{DHAC}		T-50		ns
HLDRQ ↓ → $\overline{\text{HLDAK}}$ ↑ delay time	t_{DHQHA}			3T+160	ns
HLDRQ ↓ → bus output delay time	t_{DHQC}		3T+30		ns
HLDRQ low level width	t_{WHQL}		1.5T		ns
$\overline{\text{HLDAK}}$ low level width	t_{WHAL}		T		ns
INT, DMARQ setup time to CLKOUT ↑	t_{SIQK}		30		ns
INT, DMARQ high, low level width	t_{WIQH}, t_{WIQL}		8T		ns
$\overline{\text{POLL}}$ setup time to CLKOUT ↑	t_{SPLK}		30		ns
NMI high, low level width	t_{WNIH}, t_{WNIL}		5		us
$\overline{\text{CTS}}$ low level width	t_{WCTL}		2T		ns
INT setup time to CLKOUT ↑	t_{SIRK}		30		ns
CLKOUT ↓ → $\overline{\text{INTAK}}$ ↓ delay time	t_{DKIA}		15	80	ns
INT hold time from $\overline{\text{INTAK}}$ ↓	t_{HIAIQ}		0		ns
$\overline{\text{INTAK}}$ low level width	t_{WIAL}		2T-30		ns
$\overline{\text{INTAK}}$ high level width	t_{WIAH}		T-30		ns
$\overline{\text{INTAK}}$ ↓ → data delay time	t_{DIAD}			2T-130	ns
Data hold time from $\overline{\text{INTAK}}$ ↑	t_{HIAD}		0	0.5T	ns

Remarks: n denotes the number of wait states. When no wait states are inserted, n is 0.

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{SCKO}$ cycle time	t_{CYTK}		1000		ns
$\overline{SCKO}$ high, low level width	t_{WSTH}, t_{WSTL}		450		ns
$\overline{SCKO}$ ↓ → TxD delay time	t_{DTKD}			210	ns
$\overline{SCKO}$ ↓ → TxD hold time	t_{HTKD}		20		ns
$\overline{CTSO}$ cycle time	t_{CYRK}		1000		ns
$\overline{CTSO}$ high, low level width	t_{WSRH}, t_{WSRL}		420		ns
RxD setup time to, hold time from $\overline{CTSO}$↑	t_{SRDK}, t_{HKRD}		80		ns

(2) uPD70335-10 (Ta=-10 to +70°C, V_{DD}=+5.0V±5%)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
X1 input cycle time	t_{CYX}		49	250	ns
X1 input high, low level width	t_{WXH}, t_{WXL}		16		ns
X1 input rising, falling time	t_{XR}, t_{XF}			15	ns
CLKOUT output cycle time	t_{CYK}	$f_X/2$, T=t_{CYK}	100	2000	ns
CLKOUT output high, low level width	t_{WKH}, t_{WKL}		0.5T-12		ns
CLKOUT output rising, falling time	t_{KR}, t_{KF}			12	ns
Input rising, falling time	t_{IR}, t_{IF}	Except for $\overline{RESET}$, NMI, X1, or X2		20	ns
	t_{IRS}, t_{IFS}	$\overline{RESET}$, NMI		30	ns
Output rising, falling time	t_{OR}, t_{OF}	Except for CLKOUT		15	ns
CLKOUT → address delay time	t_{DKA}		15	75	ns
Address → data input delay time	t_{DADR}			(n+1.5)T-60	ns
$\overline{MREQ}$ ↓ → data delay time	t_{DMRD}			(n+2)T-50	ns
$\overline{MSTB}$ ↓ → data delay time	t_{DMSD}			(n+1)T-50	ns
$\overline{MREQ}$ ↓ → $\overline{MSTB}$ ↓ delay time	t_{DMRMS1}	Read operation	T-30	T+30	ns
	t_{DMRMS2}	Write operation	(n+1)T-30	(n+1)T+30	ns
$\overline{MREQ}$ low level width	t_{WMRL}		(n+2)T-25	(n+2)T+25	ns
Address hold time from $\overline{MREQ}$ ↓	t_{HMRA}		0.5T-25		ns
Data input hold time from $\overline{MREQ}$ ↑	t_{HMA}		0.5T-30		ns
Data input hold time from $\overline{MREQ}$ ↑	t_{HMDR}		0		ns
Control signal recovery time	t_{RVC}		T-25		ns
Address → data output delay time	t_{DADW}		0.5T-30	0.5T+50	ns
Address setup time to $\overline{MREQ}$ ↓	t_{DAMR}		0.5T-30		ns
Second address setup time to $\overline{MSTB}$ ↓	t_{DRMS}	Read operation	0.5T-30		ns
	t_{DWMS}	Write operation	(n+0.5)T-30		ns
$\overline{MSTB}$ low level width	t_{WMSL1}	Read operation	(n+1)T-25		ns
	t_{WMSL2}	Write operation	T-20	T+20	ns
Data output setup time to $\overline{MSTB}$ ↑	t_{SDM}		(n+2)T-50		ns
Address setup time to IOSTB ↓	t_{DAIS}		0.5T-30		ns
$\overline{IOSTB}$ ↓ → data delay time	t_{DISD}			(n+1)T-50	ns
$\overline{MREQ}$ ↓ → IOSTB ↓ delay time	t_{DMRIS}		T-30		ns
$\overline{IOSTB}$ low level width	t_{WISL}		(n+1)T-25		ns
Address hold time from $\overline{IOSTB}$ ↑	t_{HISA}		0.5T-30		ns
Data input hold time from $\overline{IOSTB}$ ↑	t_{HISDR}		0		ns
Data output setup time to $\overline{IOSTB}$ ↑	t_{SDIS}		(n+2)T-50		ns

Remarks: n denotes the number of wait states. When no wait states are inserted, n is 0.

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{\text{DMARQ}}$ setup time to $\overline{\text{MREQ}}$ ↓	t_{SDADQ}	Demand release mode, n≧2		(n-1)T-50	ns
$\overline{\text{DMARQ}}$ hold time from $\overline{\text{DMAAK}}$ ↓	t_{HDADQ}	Demand release mode	0		ns
$\overline{\text{DMAAK}}$ output low level width	t_{WDMRL}		(n+2.5)T-25		ns
$\overline{\text{DMAAK}}$ ↓ → $\overline{\text{TC}}$ ↓ delay time	t_{DDATC}			0.5t+35	ns
$\overline{\text{TC}}$ low level width	t_{WTCL}		(n+3)T-25		ns
$\overline{\text{DMAAK}}$ output low level width	t_{WDMWL}		(n+2)T-25		ns
Address setup time to $\overline{\text{REFRQ}}$ ↓	t_{DARF}		0.5T-30		ns
$\overline{\text{REFRQ}}$ low level width	t_{WRFL}		(n+2)T-25		ns
Address hold time from $\overline{\text{REFRQ}}$ ↑	t_{HRFA}		0.5T-30		ns
$\overline{\text{RESET}}$ low level width	t_{WRSL1}	STOP mode release or power on reset	30		ms
	t_{WRSL2}	System reset	5		us
READY setup time to $\overline{\text{MREQ}}$ ↓	t_{SCRY0}	n≧2		2T-80	ns
	t_{SCRY}	n≧3		nT-80	ns
READY hold time from $\overline{\text{MREQ}}$ ↓	t_{HCRY0}	n=2	2T		ns
	t_{HCRY}	n≧3	nT		ns
	t_{HCRY1}	n≧3	(n-1)T		ns
READY setup time to $\overline{\text{IOSTB}}$ ↓	t_{SSRY0}	n≧2		T-80	ns
	t_{SSRY}	n≧3		(n-1)T-80	ns
READY hold time from $\overline{\text{IOSTB}}$ ↓	t_{HSRY0}	n=2	T		ns
	t_{HSRY}	n≧3	(n-1)T		ns
	t_{HSRY1}	n≧3	(n-2)T		ns
HLDRQ setup time to CLKOUT ↑	t_{SHQK}		25		ns
CLKOUT ↑ → $\overline{\text{HLDAK}}$ ↓ delay time	t_{DKHA}		15	70	ns
Bus float → $\overline{\text{HLDAK}}$ ↓ delay time	t_{CFHA}		T-35		ns
$\overline{\text{HLDAK}}$ ↑ → bus output delay time	t_{DHAC}		T-35		ns
HLDRQ ↓ → $\overline{\text{HLDAK}}$ ↑ delay time	t_{DHQHA}			3T+160	ns
HLDRQ ↓ → bus output delay time	t_{DHQC}		3T+30		ns
HLDRQ low level width	t_{WHQL}		1.5T		ns
$\overline{\text{HLDAK}}$ low level width	t_{WHAL}		T		ns
INTP, DMARQ setup time to CLKOUT ↑	t_{SIQK}		25		ns
INTP, DMARQ high, low level width	t_{WIQH}, t_{WIQL}		8T		ns
POLL setup time to CLKOUT ↑	t_{SPLK}		25		ns
NMI high, low level width	t_{WNIH}, t_{WNIL}		5		us
$\overline{\text{CTS}}$ low level width	t_{WCTL}		2T		ns

Remarks: n denotes the number of wait states. When no wait states are inserted, n is 0.

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
INT setup time to CLKOUT ↑	t_{SIRK}		25		ns
CLKOUT ↓ → $\overline{INTAK}$ ↓ delay time	t_{DKIA}		15	70	ns
INT hold time from $\overline{INTAK}$ ↓	t_{HIAIQ}		0		ns
$\overline{INTAK}$ low level width	t_{WIAL}		2T-25		ns
$\overline{INTAK}$ high level width	t_{WIAH}		T-25		ns
$\overline{INTAK}$ ↑ → data delay time	t_{DIAD}			2T-100	ns
Data hold time from $\overline{INTAK}$ ↑	t_{HIAD}		0	0.5T	ns
$\overline{SCKO}$ cycle time	t_{CYTK}		1000		ns
$\overline{SCKO}$ high, low level width	t_{WSTH}, t_{WSTL}		450		ns
$\overline{SCKO}$ ↓ → TxD delay time	t_{DTKD}			210	ns
$\overline{SCKO}$ ↓ → TxD hold time	t_{HTKD}		20		ns
$\overline{CTSO}$ cycle time	t_{CYRK}		1000		ns
$\overline{CTSO}$ high, low level width	t_{WSRH}, t_{WSRL}		420		ns
RxD setup time to, hold time from $\overline{CTSO}$ ↑	t_{SRDK}, t_{HKRD}		80		ns

Comparator characteristics

uPD70335-8 (Ta=-10 to +70°C, V_{DD}=+5.0V±10%)

uPD70335-10 (Ta=-10 to +70°C, V_{DD}=+5.0V±5%)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Comparison accuracy	V_{ACOMP}				±100	mV
Threshold voltage	V_{TH}		0		V_{DD}+0.1	V
Comparison time	t_{COMP}		64		65	t_{CYK}
PT input voltage	V_{IPT}		0		V_{DD}	V

Data memory STOP mode low supply voltage data retention characteristics (Ta=-10 to +70°C)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.5	5.5	V
V_{DD} rising, falling time	t_{RVD}, t_{FVD}		200		us

3.7 FOR μPD70335(A)-9

Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Test condition	Ratings	Unit
Power supply voltage	V_{DD}		-0.5 to +7.0	V
	V_{TH}		-0.5 to V_{DD}+0.5	V
Input voltage	V_I		-0.5 to V_{DD}+0.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Output low current	I_{OL}	Per pin	4.0	mA
		Total, all output	50	mA
Output high current	I_{OH}	Per pin	-2.0	mA
		Total, all output	-20	mA
Operation temperature	T_{opt}		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Oscillator characteristics

uPD70335(A)-9 (Ta=-40 to +85°C, V_{DD}=+5.0V±5%, V_{SS}=0V, 0V≤V_{TH}≤V_{DD}+0.1V)

Resonator	Recommended circuit	Parameter	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator	X1 X2, C1, C2	Oscillation frequency (f_{XX})	4	18	MHz
External clock	① X1 X2, HCMOS inverter or ② X1 X2 open, HCMOS inverter	X1 input frequency (f_X)	4	18	MHz
		X1 input rising, falling time (t_{XR}, t_{XF})	0	15	ns
		X1 input high, low level width (t_{WXH}, t_{WXL})	17		ns

Remarks 1: Place the oscillator as close as possible to the X1 and X2 pins.

2: Do not pass any other signal line through the shaded portion.

Capacitance (Ta=25°C, V_{DD}=0 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C=1 MHz Unmeasured pins returned to 0 V			10	pF
Output capacitance	C_O				20	pF
Input/output capacitance	C_{IO}				20	pF

DC characteristics

uPD70335(A)-9   (Ta=-40 to +85°C, V_{DD}=+5.0V±5%)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input low voltage	V_{IL}		0		0.8	V
Input high voltage	V_{IH1}	Except for $\overline{RESET}$, P10/NMI, X1, or X2	2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P10/NMI, X1, X2	$0.8V_{DD}$		V_{DD}	V
Output low voltage	V_{OL}	I_{OL}=1.6 mA			0.45	V
Output high voltage	V_{OH}	I_{OH}=-0.4 mA	V_{DD}-1.0			V
Input current	I_I	$\overline{EA}$, P10/NMI; $0 \le V_I \le V_{DD}$			±20	uA
Input leakage current	I_{LI}	Except for $\overline{EA}$ or P10/NMI; $0 \le V_I \le V_{DD}$			±10	uA
Output leakage current	I_{LO}	$0 \le V_O \le V_{DD}$			±10	uA
V_{TH} current	I_{TH}	$0 V \le V_{TH} \le V_{DD}$		0.5	1.0	mA
V_{DD} power supply current	I_{DD1}	Operation mode		95	130	mA
	I_{DD2}	HALT mode		30	55	mA
	I_{DD3}	STOP mode		15	35	uA

AC characteristics

uPD70335(A)-9 (Ta=-40 to +85°C, V_{DD}=+5.0V±5%)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
X1 input cycle time	t_{CYX}		55	250	ns
X1 input high, low level width	t_{WXH}, t_{WXL}		17		ns
X1 input rising, falling time	t_{XR}, t_{XF}			15	ns
CLKOUT output cycle time	t_{CYK}	$f_X/2$, $T-t_{CYK}$	111	2000	ns
CLKOUT output high, low level width	t_{WKH}, t_{WKL}		0.5T-12		ns
CLKOUT output rising, falling time	t_{KR}, t_{KF}			12	ns
Input rising, falling time	t_{IR}, t_{IF}	Except for $\overline{RESET}$, NMI, X1 or X2		20	ns
	t_{IRS}, t_{IFS}	$\overline{RESET}$, NMI		30	ns
Output rising, falling time	t_{OR}, t_{OF}	Except for CLKOUT		15	ns
CLKOUT → address delay time	t_{DKA}		15	80	ns
Address → data input delay time	t_{DADR}			(n+1.5)T-60	ns
$\overline{MREQ}$ ↓ → data delay time	t_{DMRD}			(n+2)T-50	ns
$\overline{MSTB}$ ↓ → data delay time	t_{DMSD}			(n+1)T-50	ns
$\overline{MREQ}$ ↓ → $\overline{MSTB}$ ↓ delay time	t_{DMRMS1}	Read operation	T-30	T+30	ns
	t_{DMRMS2}	Write operation	(n+1)T-30	(n+1)T+30	ns
$\overline{MREQ}$ low level width	t_{WMRL}		(n+2)T-25	(n+2)T+25	ns
$\overline{MREQ}$↓ → address hold time	t_{HMRA}		0.5T-30		ns
Address hold time from $\overline{MREQ}$↑	t_{HMA}		0.5T-35		ns
Data input hold time from $\overline{MREQ}$↑	t_{HMDR}		0		ns
Control signal recovery time	t_{RVC}		T-25		ns
Address → data output delay time	t_{DADW}			0.5T+50	ns
Address setup time to $\overline{MREQ}$↓	t_{DAMR}		0.5T-35		ns
Second address setup time to $\overline{MSTB}$↓	t_{DRMS}	Read operation	0.5T-30		ns
	t_{DWMS}	Write operation	(n+0.5)T-30		ns
$\overline{MSTB}$ low level width	t_{WMSL1}	Read operation	(n+1)T-25		ns
	t_{WMSL2}	Write operation	T-25	T+25	ns
Data output setup time to $\overline{MSTB}$↑	t_{SDM}		(n+2)T-50		ns
Address setup time to $\overline{IOSTB}$↓	t_{DAIS}		0.5T-30		ns
$\overline{IOSTB}$↓ → data delay time	t_{DISD}			(n+1)T-50	ns
$\overline{MREQ}$↓ → $\overline{IOSTB}$↓ delay time	t_{DMRIS}		T-35		ns
$\overline{IOSTB}$ low level width	t_{WISL}		(n+1)T-30		ns
Address hold time from $\overline{IOSTB}$↑	t_{HISA}		0.5T-30		ns
Data input hold time from $\overline{IOSTB}$↑	t_{HISDR}		0		ns
Data output setup time to $\overline{IOSTB}$↑	t_{SDIS}		(n+2)T-50		ns

Remarks: n represents the number of wait states. n=0 means no wait.

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{DMARQ}$ setup time to $\overline{MREQ}$ ↓	t_{SDADQ}	Demand release mode, n≥2		(n-1)T-50	ns
$\overline{DMARQ}$ hold time from $\overline{DMAAK}$ ↓	t_{HDADQ}	Demand release mode	0		ns
$\overline{DMAAK}$ output low level width	t_{WDMRL}		(n+2.5)T-25		ns
$\overline{DMAAK}$ ↓ → TC ↓ delay time	t_{DDATC}			0.5T+35	ns
$\overline{TC}$ low level width	t_{WTCL}		(n+3)T-25		ns
$\overline{DMAAK}$ output low level width	t_{WDMWL}		(n+2)T-25		ns
Address setup time to $\overline{REFRQ}$ ↓	t_{DARF}		0.5T-35		ns
$\overline{REFRQ}$ low level width	t_{WRFL}		(n+2)T-25		ns
Address hold time from $\overline{REFRQ}$ ↑	t_{HRFA}		0.5T-35		ns
$\overline{RESET}$ low level width	t_{WRSL1}	STOP mode release/ power on reset	30		ms
	t_{WRSL2}	System reset	5		us
READY setup time to $\overline{MREQ}$ ↓	t_{SCRY0}	n≥2		2T-80	ns
	t_{SCRY}	n≥3		nT-80	ns
READY hold time from $\overline{MREQ}$ ↓	t_{HCRY0}	n=2	2T		ns
	t_{HCRY}	n≥3	nT		ns
	t_{HCRY1}	n≥3	(n-1)T		ns
READY setup time to $\overline{IOSTB}$ ↓	t_{SSRY0}	n≥2		T-80	ns
	t_{SSRY}	n≥3		(n-1)T-80	ns
READY hold time from $\overline{IOSTB}$ ↓	t_{HSRY0}	n=2	T		ns
	t_{HSRY}	n≥3	(n-1)T		ns
	t_{HSRY1}	n≥3	(n-2)T		ns
HLDRQ setup time to CLKOUT ↑	t_{SHQK}		25		ns
CLKOUT ↑ → $\overline{HLDAK}$ ↓ delay time	t_{DKHA}		15	75	ns
Bus float → $\overline{HLDAK}$ ↓ delay time	t_{CFHA}		T-35		ns
$\overline{HLDAK}$ ↑ → bus output delay time	t_{DHAC}		T-35		ns
HLDRQ ↓ → $\overline{HLDAK}$ ↑ delay time	t_{DHQHA}			3T+160	ns
HLDRQ ↑ → bus output delay time	t_{DHQC}		3T+30		ns
HLDRQ low level width	t_{WHQL}		1.5T		ns
$\overline{HLDAK}$ low level width	t_{WHAL}		T		ns
INT, DMARQ setup time to CLKOUT ↑	t_{SIQK}		25		ns
INT, DMARQ high, low level width	t_{WIQH}, t_{WIQL}		8T		ns
$\overline{POLL}$ setup time to CLKOUT ↓	t_{SPLK}		30		ns
NMI high, low level width	t_{WNIH}, t_{WNIL}		5		us
$\overline{CTS}$ low level width	t_{WCTL}		2T		ns

Remarks: n represents the number of wait states.   n=0 means no wait.

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
INT setup time to CLKOUT ↑	t_{SIRK}		25		ns
CLKOUT ↓ — $\overline{INTAK}$ ↓ delay time	t_{DKIA}		15	75	ns
INT hold time from $\overline{INTAK}$ ↓	t_{HIAIQ}		0		ns
$\overline{INTAK}$ low level width	t_{WIAL}		2T-25		ns
$\overline{INTAK}$ high level width	t_{WIAH}		T-25		ns
$\overline{INTAK}$ ↓ — data delay time	t_{DIAD}			2T-100	ns
Data hold time from $\overline{INTAK}$ ↑	t_{HIAD}		0	0.5T	ns
$\overline{SCKO}$ cycle time	t_{CYTK}		1000		ns
$\overline{SCKO}$ high, low level width	t_{WSTH}, t_{WSTL}		450		ns
$\overline{SCKO}$ ↓ — TxD delay time	t_{DTKD}			210	ns
$\overline{SCKO}$ ↓ — TxD hold time	t_{HTKD}		20		ns
$\overline{CTSO}$ cycle time	t_{CYRK}		1000		ns
$\overline{CTSO}$ high, low level width	t_{WSRH}, t_{WSRL}		420		ns
RxD setup time to CTSO, hold time from $\overline{CTSO}$ ↑	t_{SRDK}, t_{HKRD}		80		ns

Comparator characteristics

uPD70335(A)-9 (Ta=-40 to +85°C, V_{DD}=+5.0V±5%)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Comparison accuracy	V_{ACOMP}				±100	mV
Threshold voltage	V_{TH}		0		V_{DD}+0.1	V
Comparison time	t_{COMP}		64		6.5	t_{CYK}
P7 input voltage	V_{IPT}		0		V_{DD}	V

Data memory STOP mode low supply voltage data retention characteristics (Ta=-40 to +85°C)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.5	5.5	V
V_{DD} rising, falling time	t_{RVD}, t_{FVD}		200		us

3.8 V35 Family Timing Wafeforms

Data Retention Timing
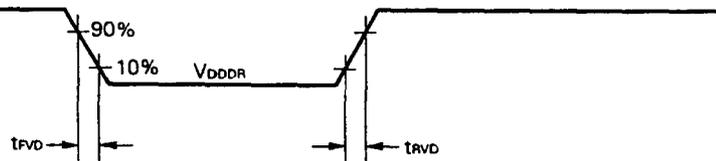
AC Test Input Waveform (Except $\overline{\text{RESET}}$, NMI, X1, or X2)
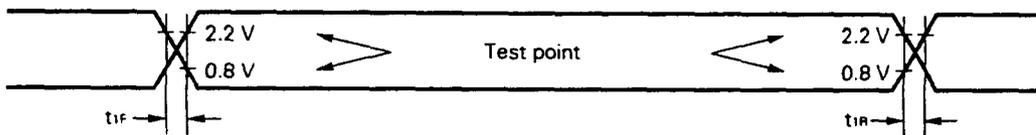
AC Test Output Test Points ($\overline{\text{RESET}}$, NMI, X1, or X2)
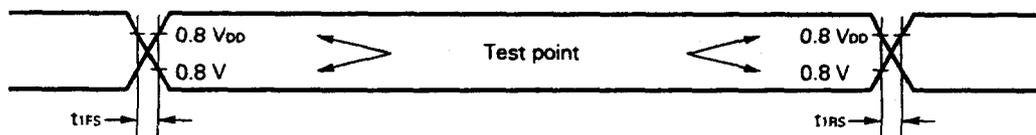
AC Test Output Test Points

Output load condition: 100 pF

Cock Timing

X1

0.8 V_{DD}
0.8 V

t_{CYX} t_{WXH} t_{XR} t_{KF} t_{WXL}

CLKOUT

2.2 V
0.8 V

t_{CYX} t_{WKH} t_{XR} t_{KF} t_{WKL}

$\overline{POLL}$ Input Timing

CLKOUT

t_{SPLK}
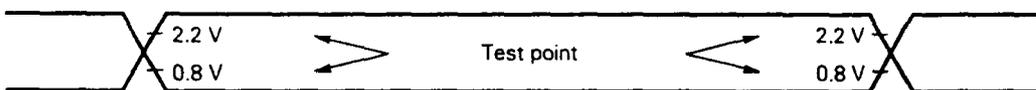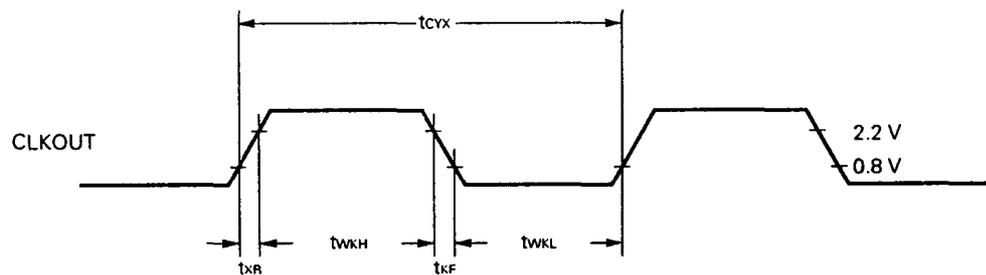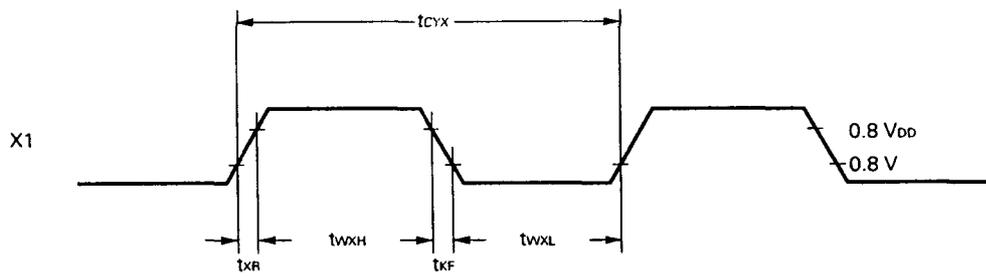
$\overline{POLL}$
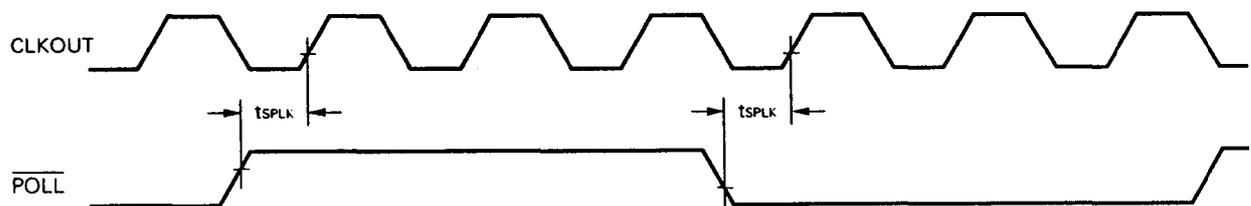
$\overline{CTS0}$-$\overline{CTS1}$ Input Timing

$\overline{CTS0}$-$\overline{CTS1}$

t_{WCTL}

Interrupt Input/DMA Input Timing
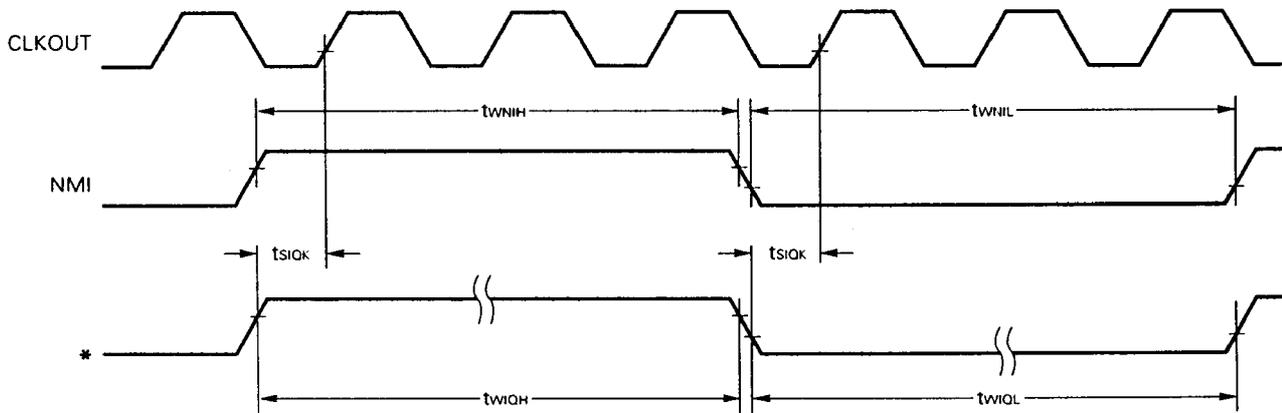
* $\overline{INTP0}$-$\overline{INTP2}$, DMARQ0-DMARQ1

$\overline{RESET}$ Input Timing

At release of STOP mode/Power-on reset:
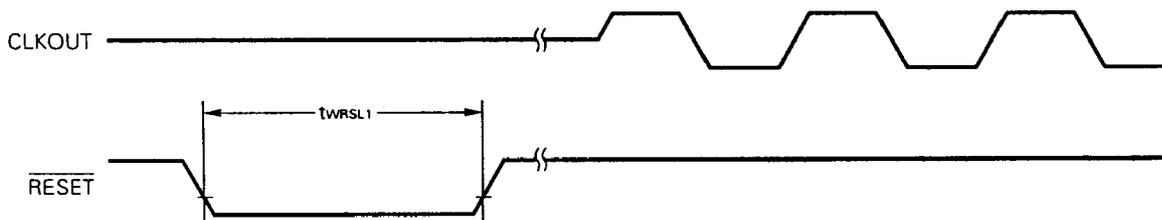
At system reset:
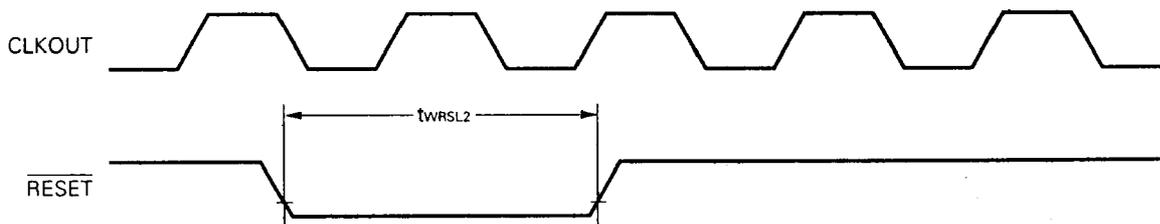
Ready Timing

At insertion of two-wait state:

| T1 | T2 | TAW | TAW | T3 |

$\overline{\text{MREQ}}$

t_{HCRY0}
t_{SCRY0}

$\overline{\text{IOSTB}}$ [NOTE]

t_{HSRY0}
t_{SSRY0}

READY
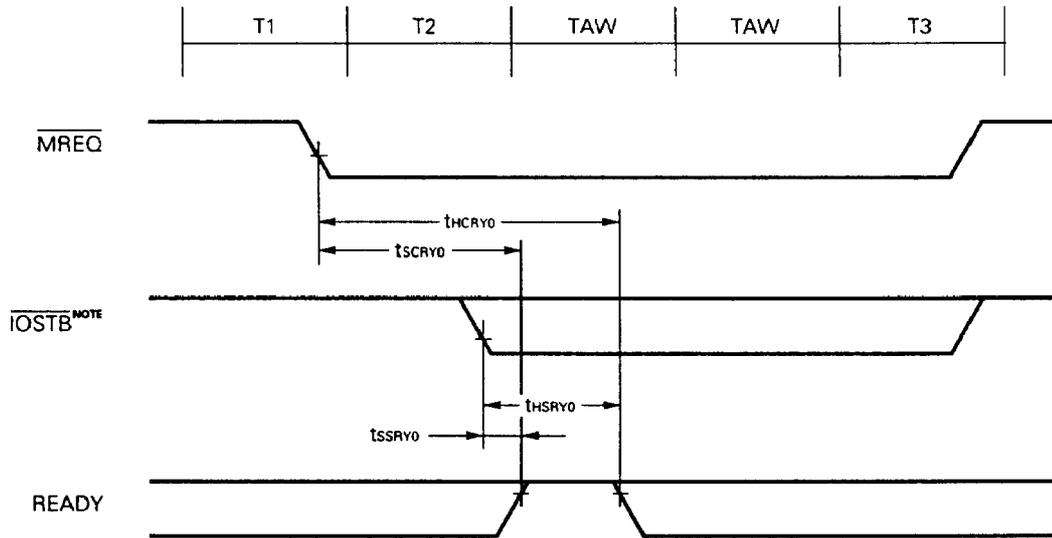
At insertion of additional (n–2) state [n ≥ 3]:

| T1 | T2 | TAW | TAW | TW x (n–2) | T3 |

$\overline{\text{MREQ}}$

t_{HCRY}
t_{HCRY1}

$\overline{\text{IOSTB}}$ [NOTE]

t_{SCRY}
t_{SCRY0}

READY

t_{SSRY0}
t_{HSRY1}
t_{SSRY}
t_{HSRY}
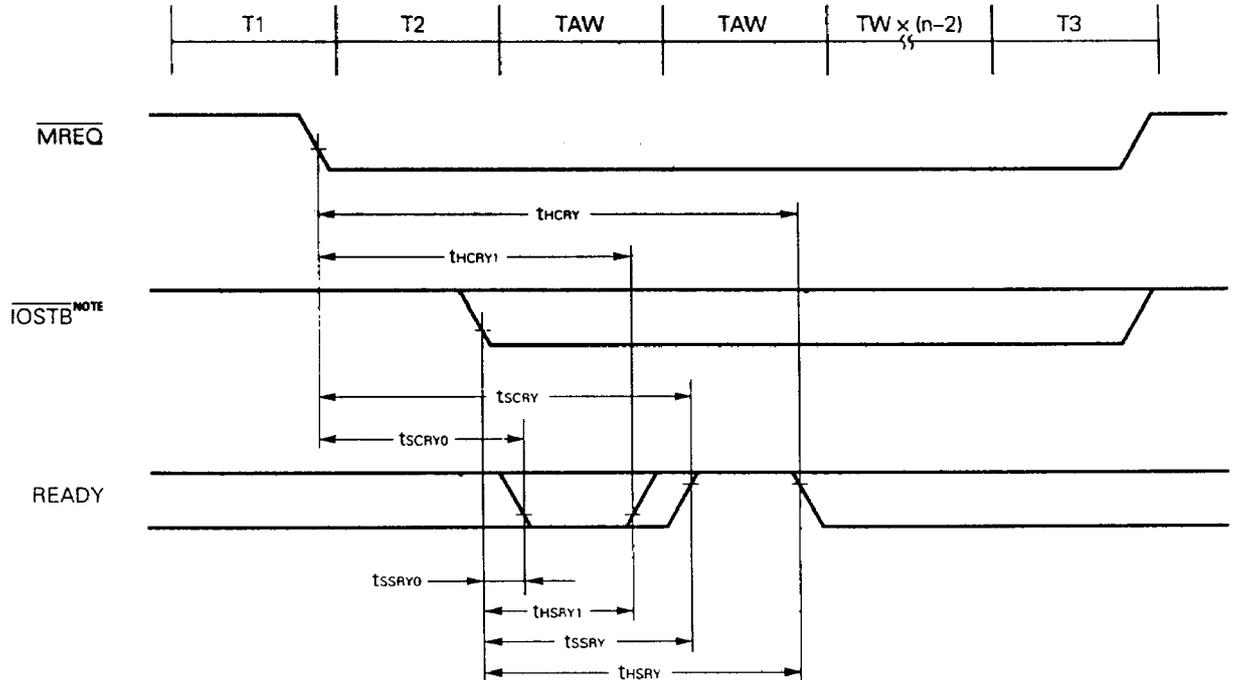
Note Only I/O cycle output

Serial Operation

At transmission of I/O interface mode:
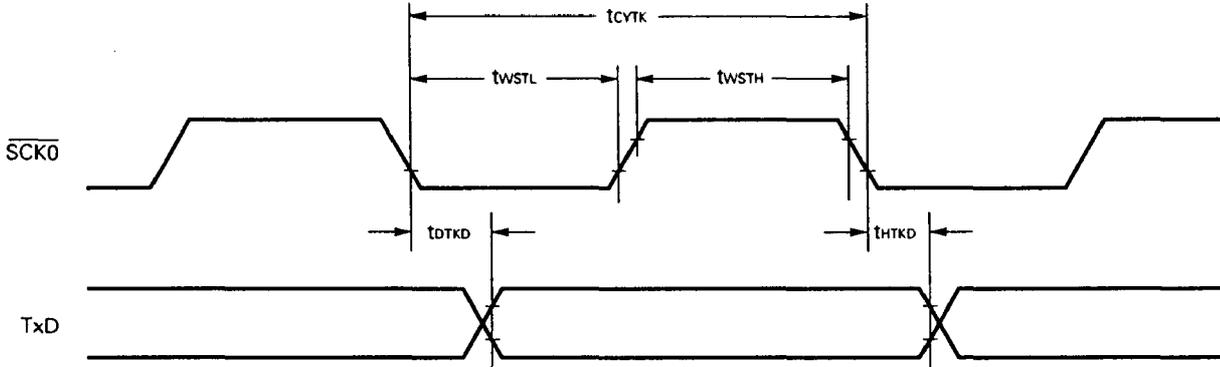
At receiving I/O interface mode:
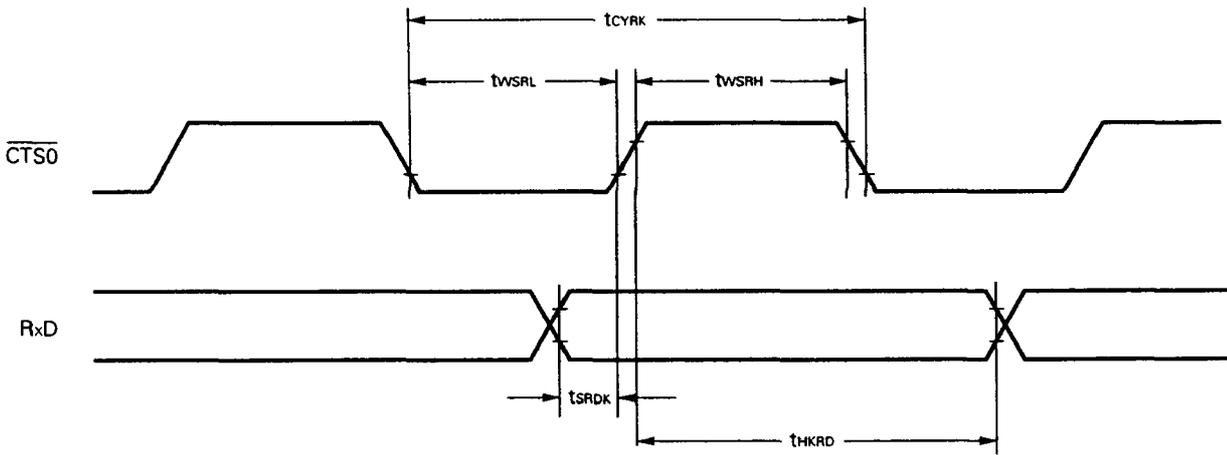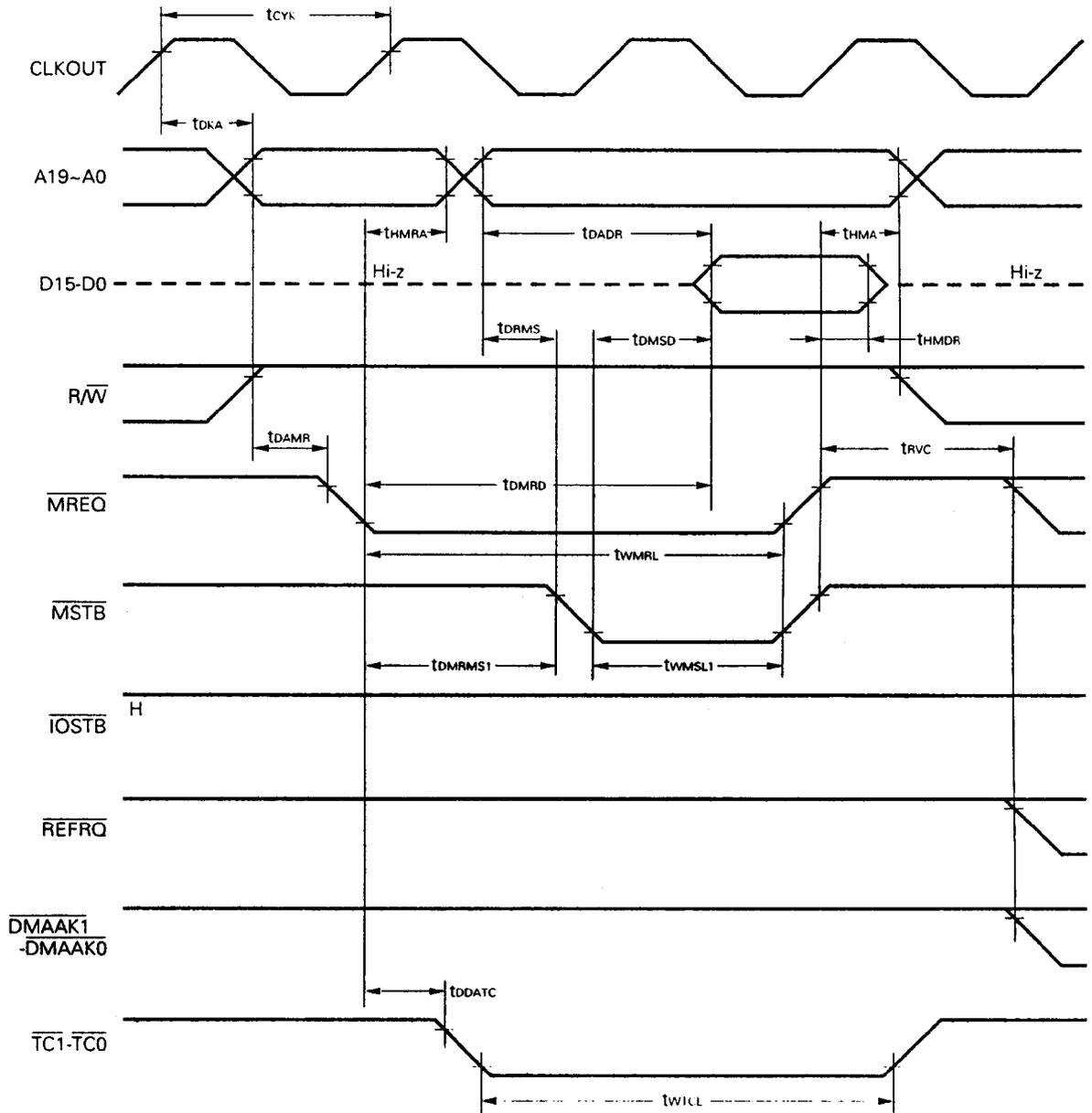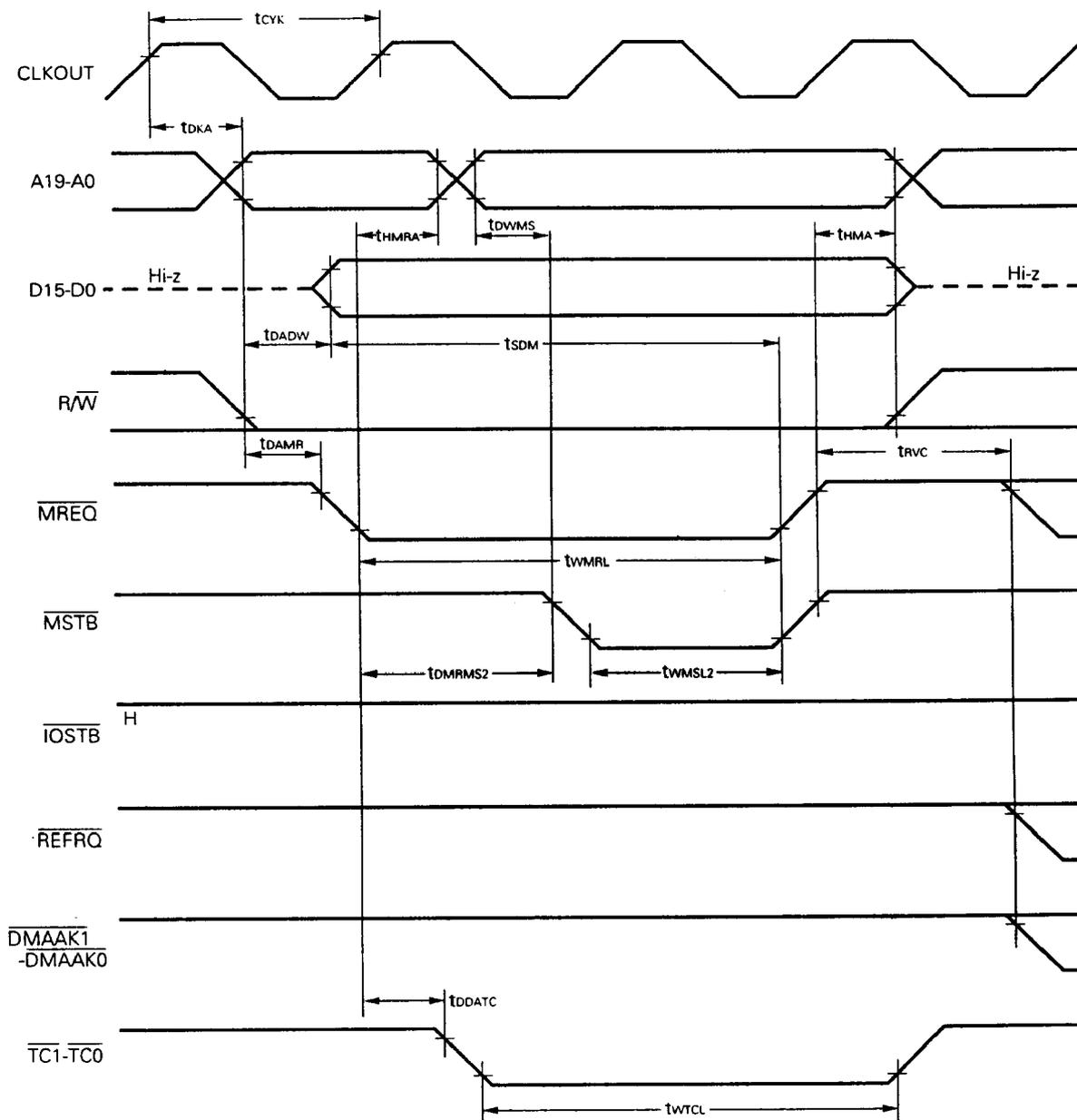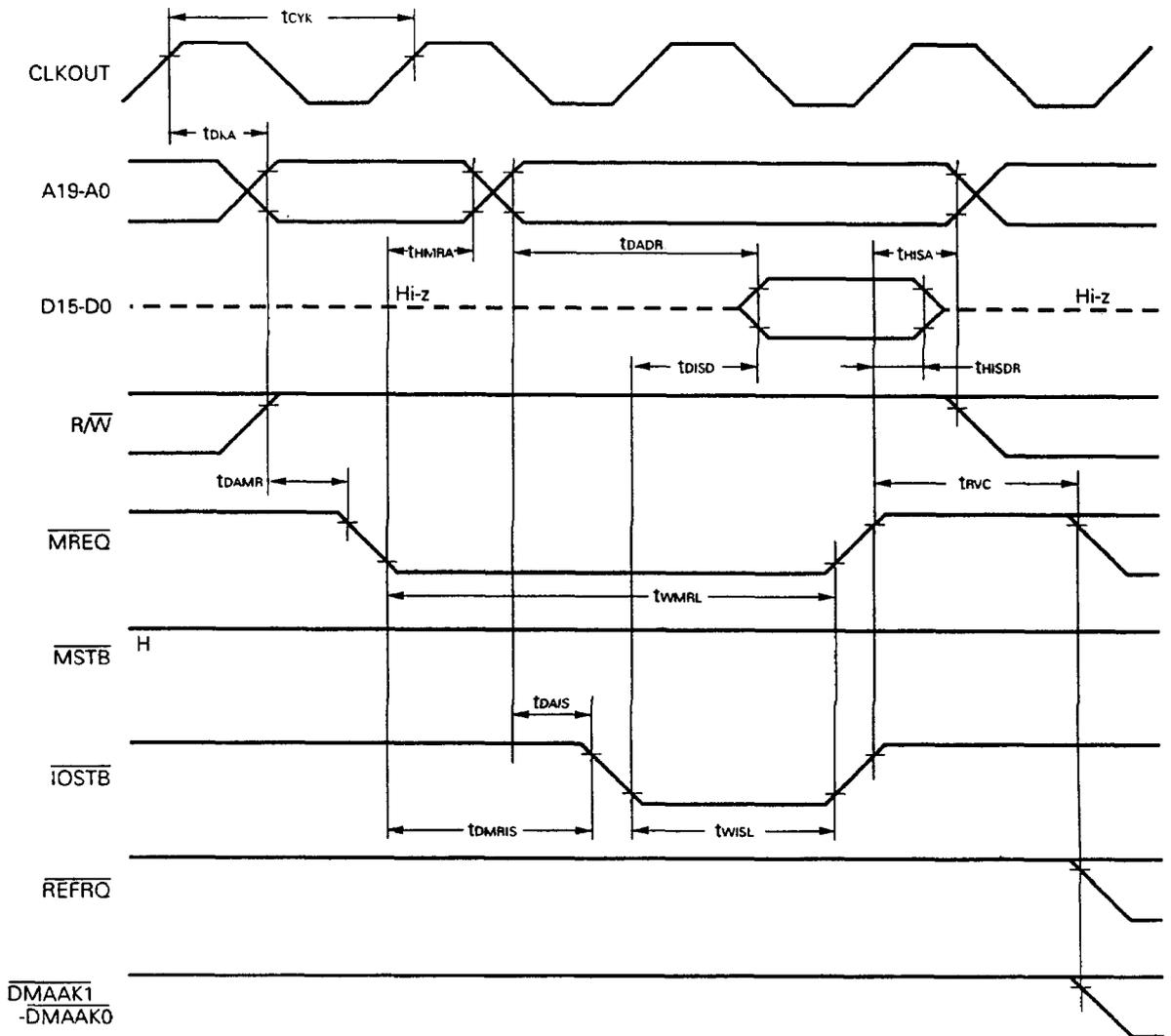
Read Operation

Write Operation

I/O Read Timing

IO Write Timing

DMA (I/O → Memory) Timing

DMA (Memory → I/O) Timing
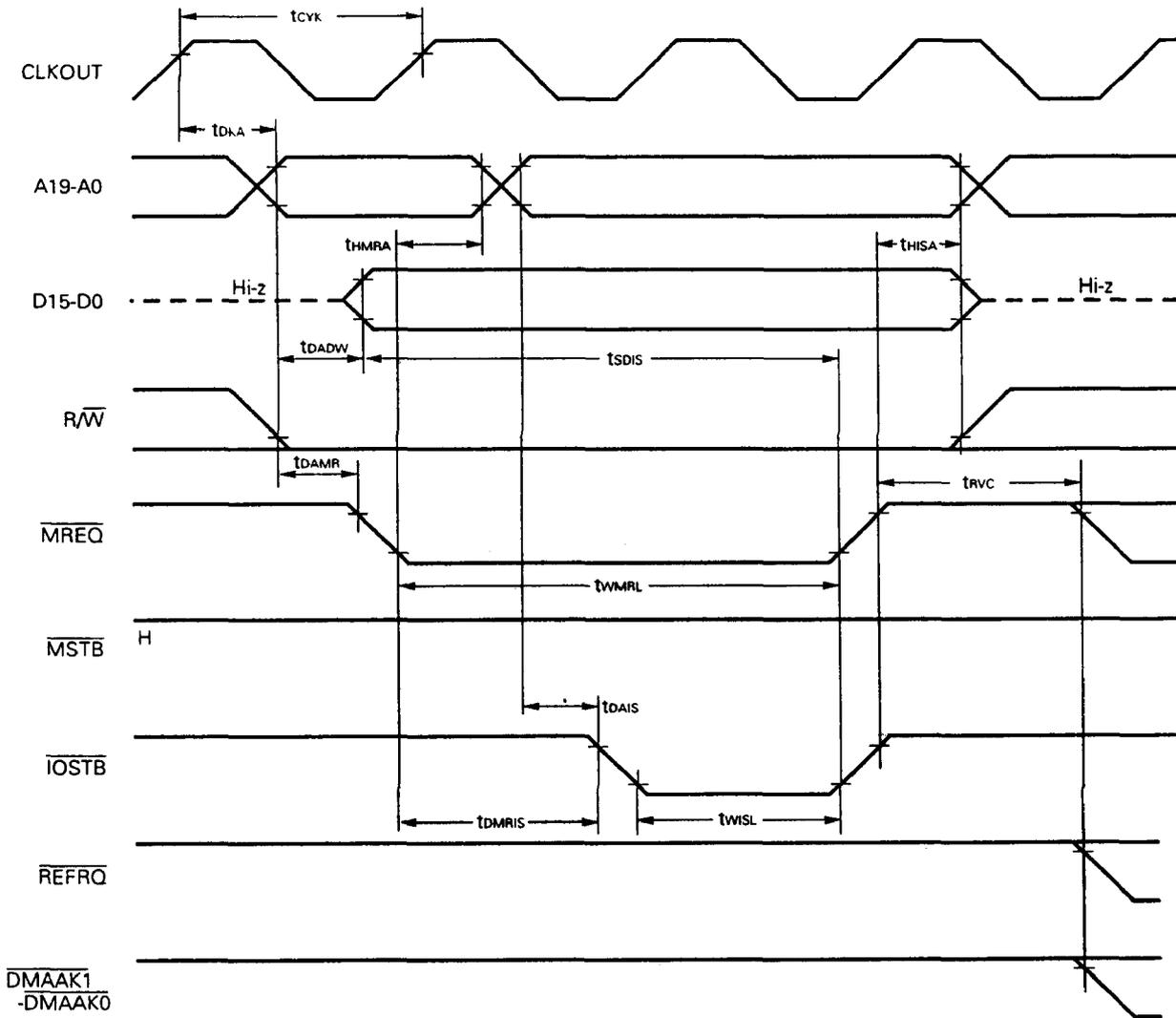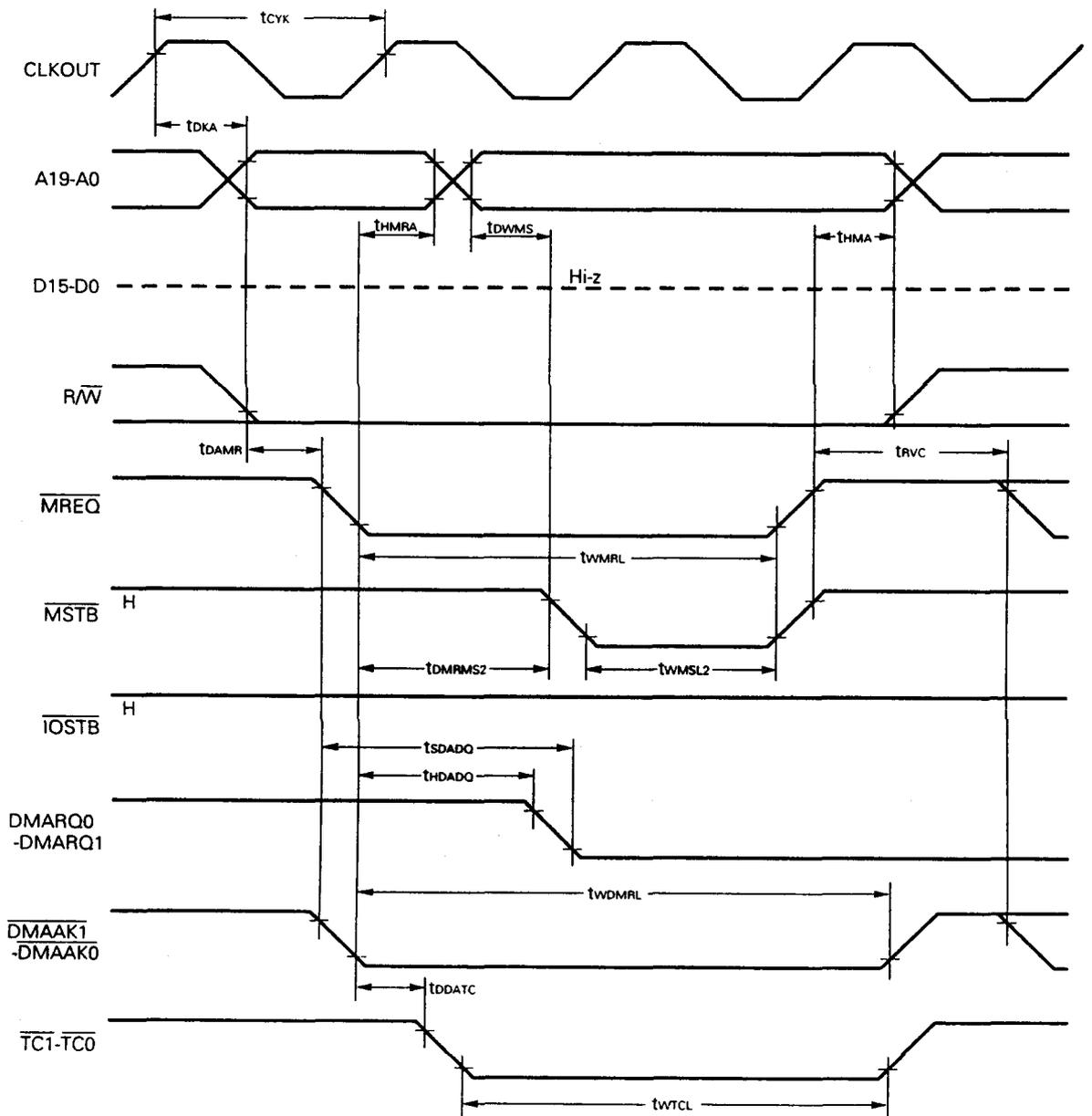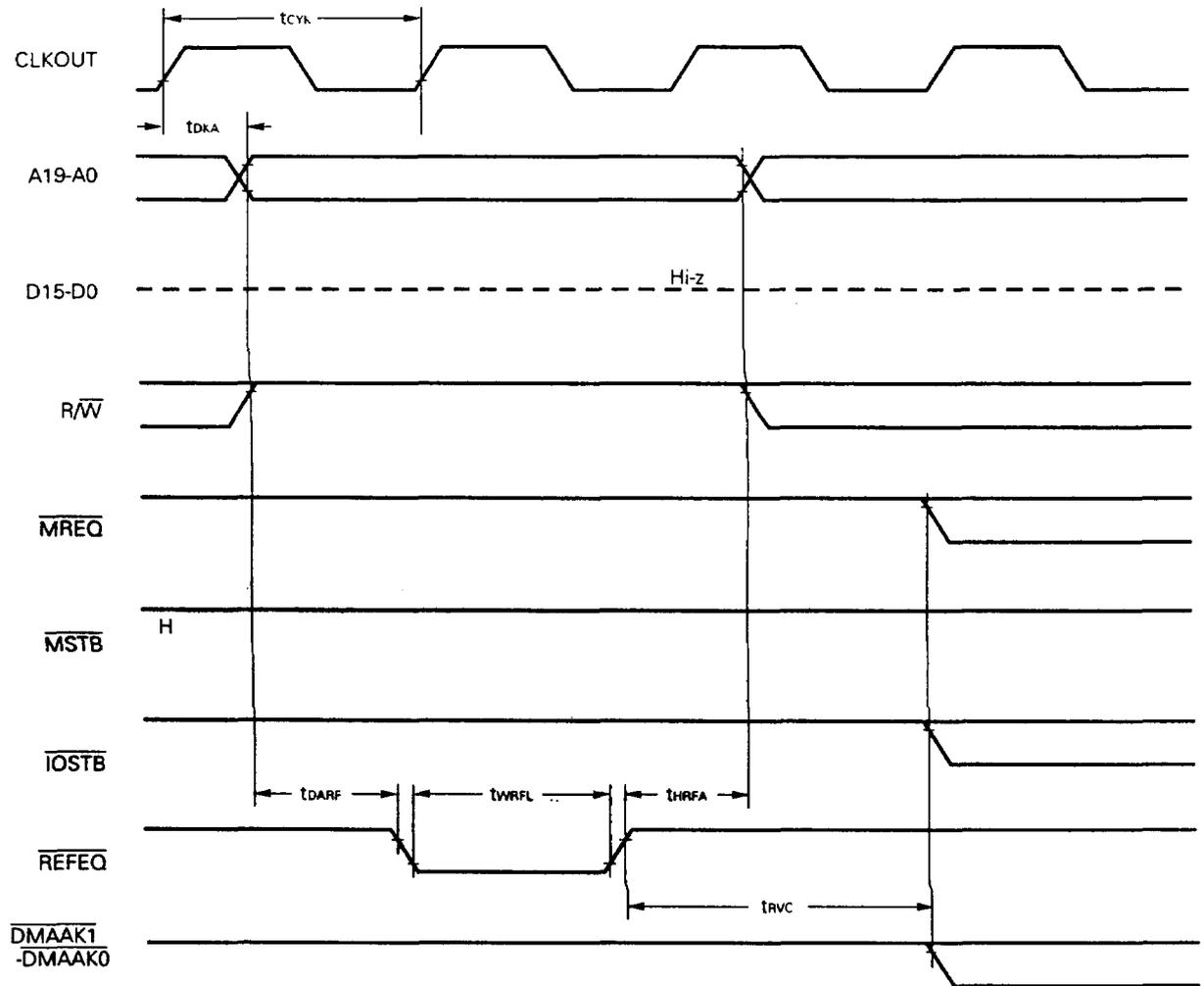
Refresh Timing

Hold Request/Acknowledge Timing

Normal mode:
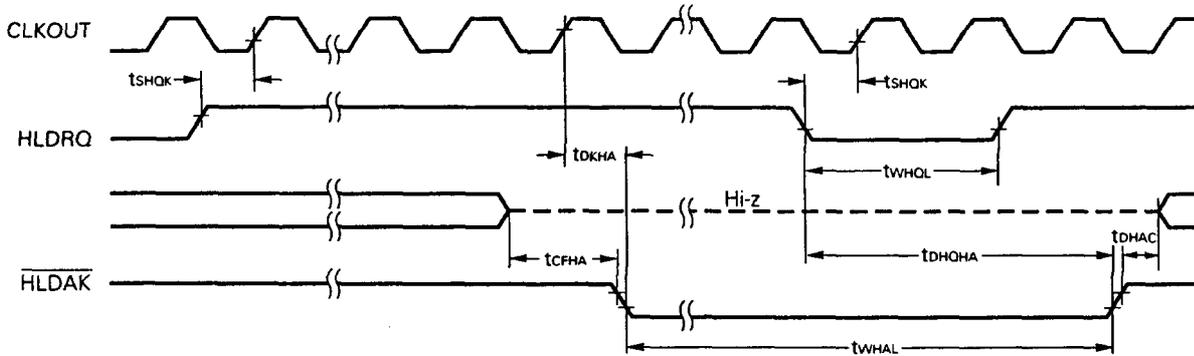
Release of HOLD mode in refresh:
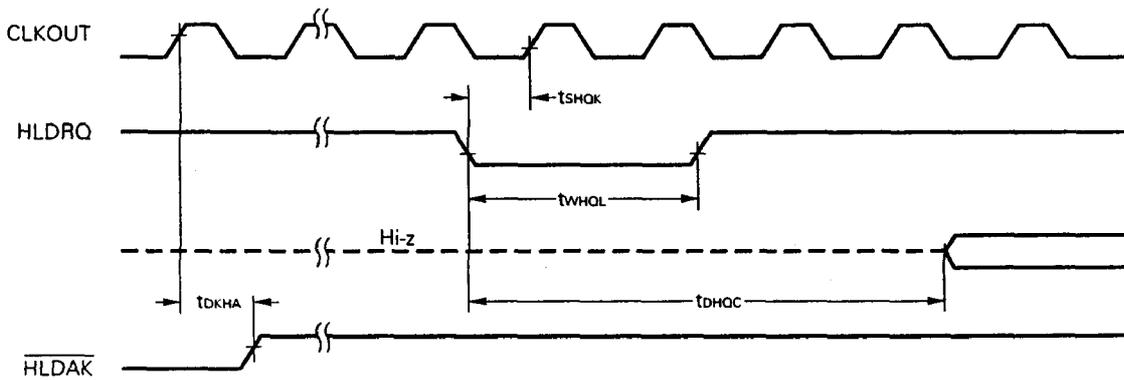
*: A19–A0, D15–D0, $\overline{MREQ}$, $\overline{MSTB}$, $\overline{IOSTB}$, R/$\overline{W}$

External Interrupt Request/Acknowledge Timing
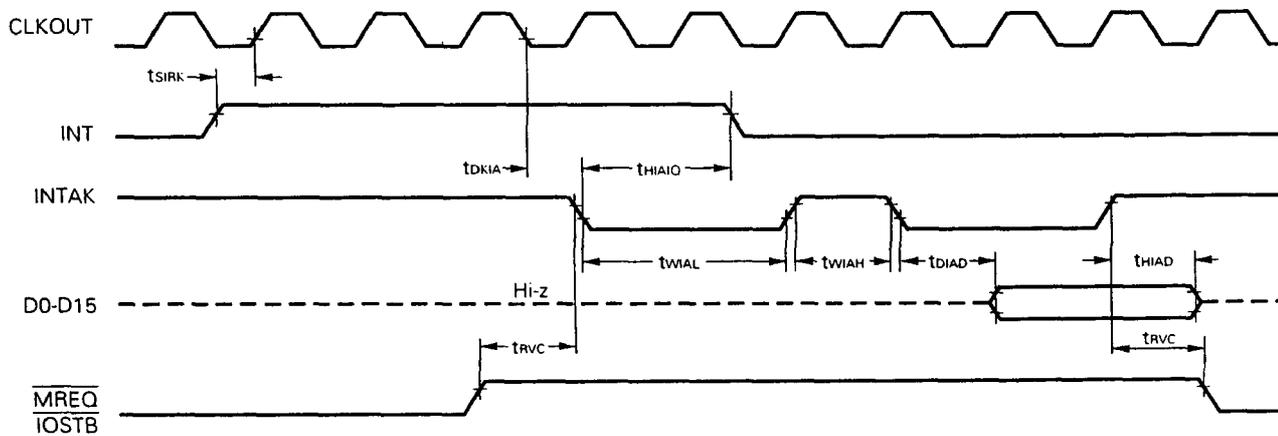
4. PACKAGE INFORMATION

94-pin Plastic QFP (□ 20) (Unit: mm)
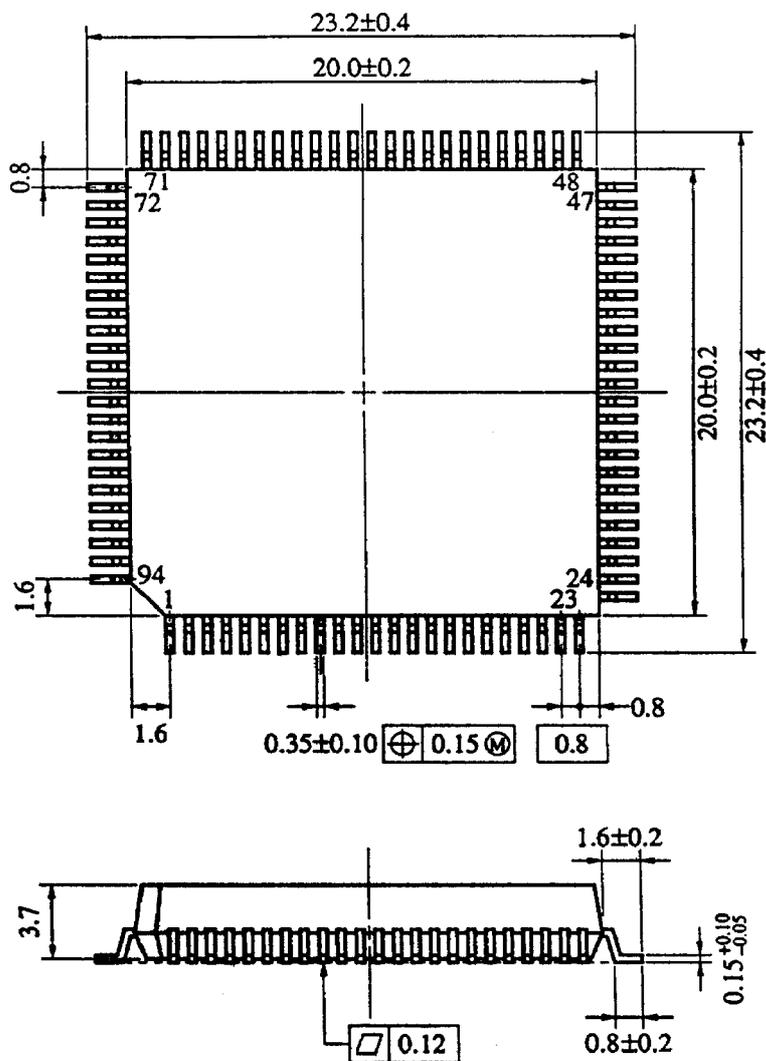
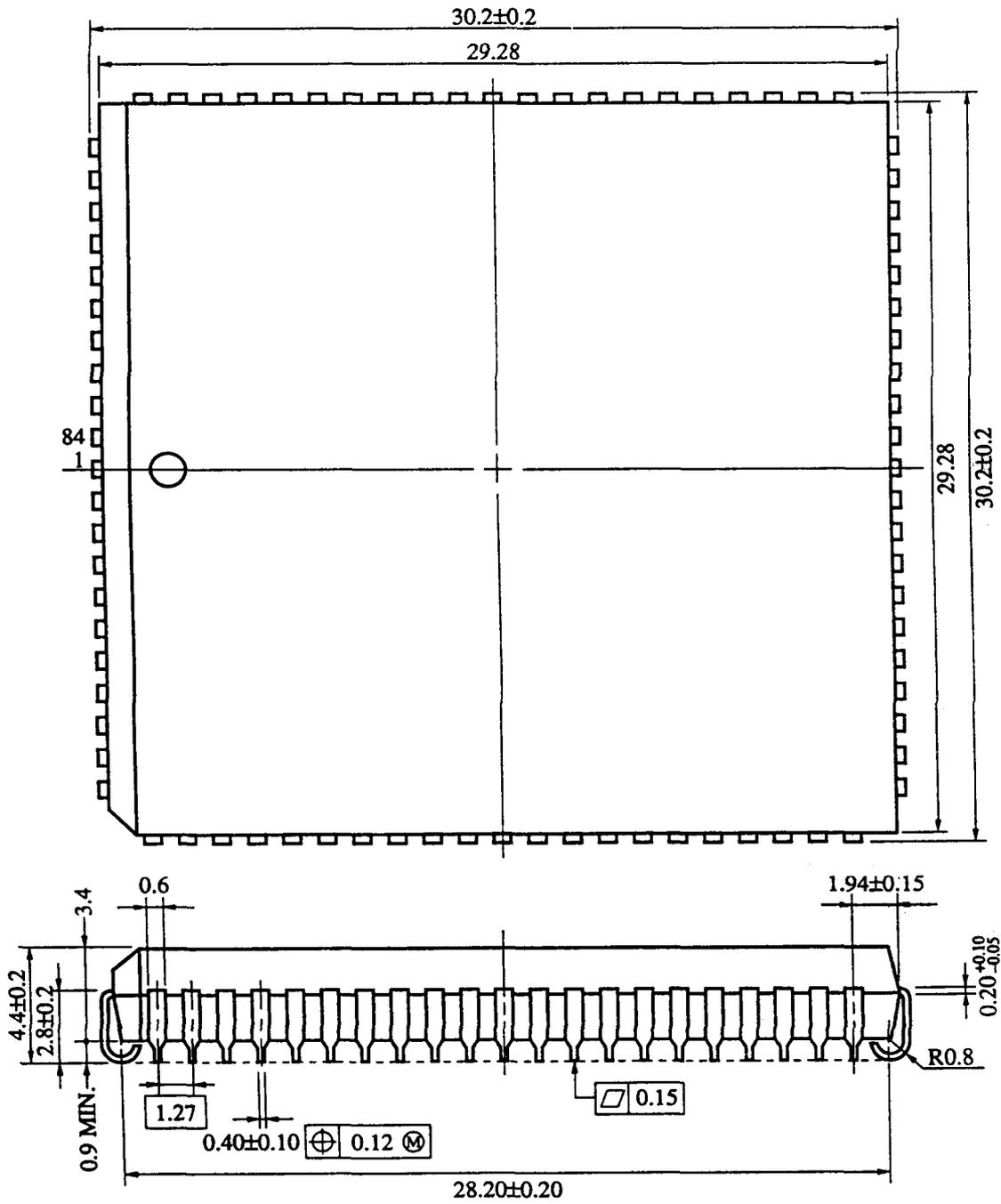Detailed Drawing of
Pin Tip Shape

S94GJ-80-5BG-2

NEC
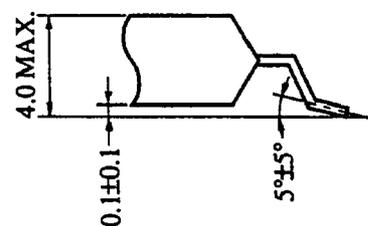
84-Pin Plastic QFJ (□ 1150) (Unit: mm)

P84L-50A3-2