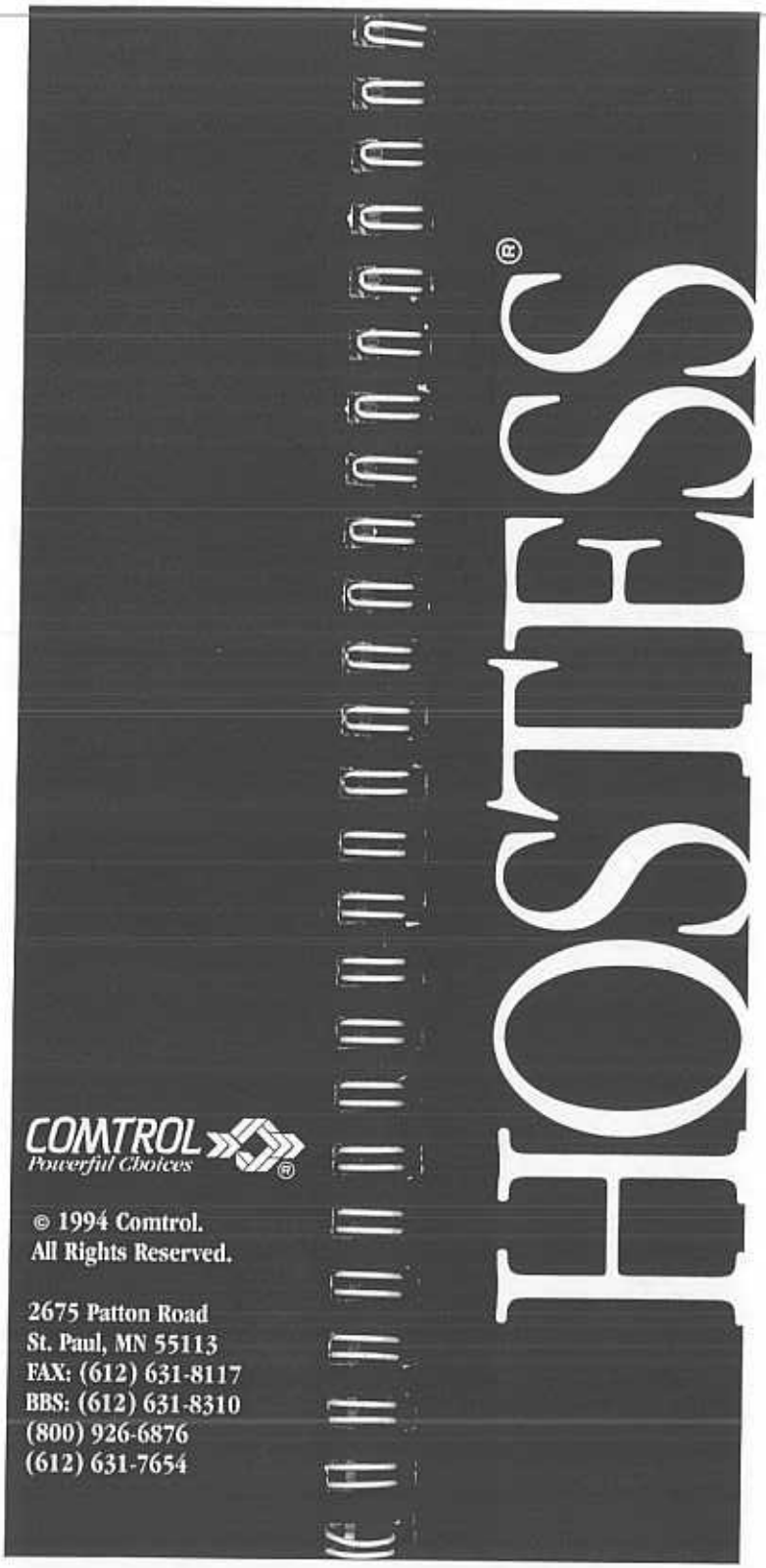

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Smart Hostess™ Series

Product Overview and Programming Guide

COMTROL
Powerful Choices®

Smart Hostess™ Series

Product Overview and Programming Guide

COMTROL
Powerful Choices

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Before You Begin

Scope

This guide provides information to configure, install, and program the *Smart* Hostess controller. (If you requested a Comtrol device driver, refer to the documentation that came with it to install the driver and controller.)

Prerequisites

The following items are required to use this controller:

- An ISA-based machine with at least one high-density diskette drive, 512K bytes of RAM, and an operating system.
- Serial cables to connect the peripheral devices to the interface.

Audience

This guide is primarily for a System Administrator and/or a programmer. The secondary audience includes the system user.

Organization

This guide contains the following information to configure and program the *Smart* Hostess controller:

Section 1. Configuring and Installing the Controller

Shows how to set the EPROM, IRQ, PC/AT, and communication jumpers. It also explains how to install the controller and upgrade a 4-port controller to an 8-port controller.

Section 2. Developing Applications

Describes sample programs that are intended to assist the programmer with writing applications.

Section 3. Programming the Controller

Explains information needed to program the controller.

Section 4. Firmware

Explains the firmware functions.

Section 5. Firmware Debugger

Explains the commands to use with the debugger.

Section 6. Troubleshooting and Technical Support

Contains information that may help you resolve installation or operations problems. In addition, it lists information that you should gather before contacting technical support.

Appendix A. Specifications

Contains the 100-pin pinout information, along with controller specifications.

Appendix B. Warranty

Contains software and hardware warranty information.

Table of Contents

Figures, Flowcharts, and Tables

Figures

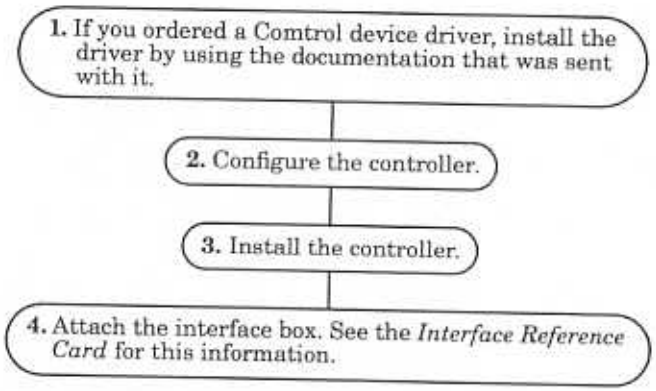
Flowcharts

Tables

Section 1. Configuring and Installing the Controller

1.1. Overview

The following flowchart provides an installation overview for the *Smart* Hostess controller.



Flowchart 1-1. Installation Overview

This section contains detailed information on the following topics:

- Identifying the controller (Page 1-2)
- Selecting the base memory and I/O addresses (Page 1-2)
- Setting the EPROM, if you upgrade the standard EPROM (Page 1-5)
- Selecting the interrupt request (IRQ) (Page 1-5)
- Selecting PC (8 bit) or AT (16 bit) mode (Page 1-6)
- Setting the communications jumpers (Page 1-6)
- Installing the controller (Page 1-10)
- Installing an upgrade kit (Page 1-11)

1.2. Identifying the Controller

To properly configure the controller, you will need to know where some of the basic parts are located. Figure 1-1 shows a 4-port *Smart* Hostess controller.

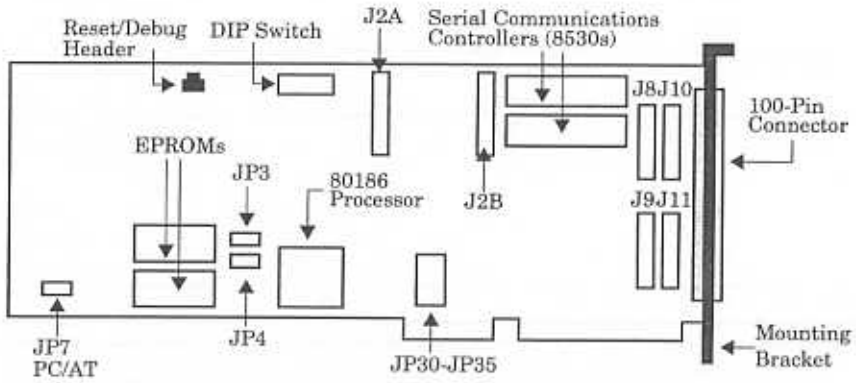


Figure 1-1. 4-Port *Smart* Hostess Controller

Notes: *The* Smart *Hostess 8-port controller is similar, except that it has four 8530 Serial Communications Controllers (SCCs).*

The reset/debug header is only available on controllers set up for development.

1.3. Selecting Addresses

The base memory and base I/O addresses are both set on the DIP switch. The available addresses are divided into two groups:

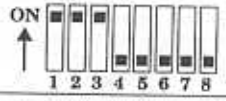
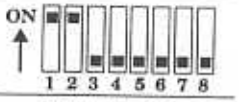
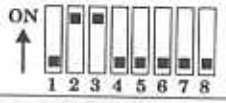
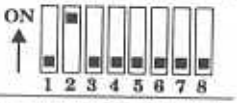
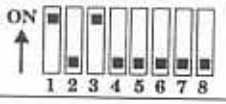
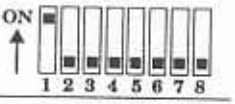
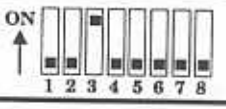
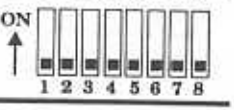
- Addressing below one megabyte of memory
- Addressing above one megabyte of memory

Note: *If you have a device driver from Comtrol, refer to the documentation that came with it for specific addressing information.*

1.3.1. Addressing Below One Megabyte

Table 1-1 shows the available base memory and base I/O addresses below one megabyte.

Table 1-1. Address Settings Under One Megabyte

Base Memory Address Range	Base I/O Address Range 238h-23Bh	Base I/O Address Range 338h-33Bh
80000h-8FFFFh		
90000h-9FFFFh		
A0000h-AFFFFh		
D0000h-DFFFFh		

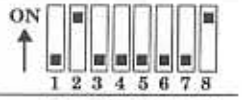
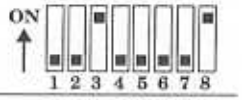
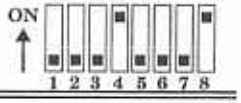
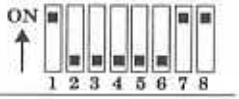
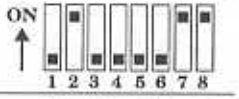
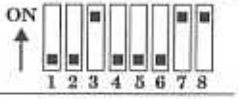
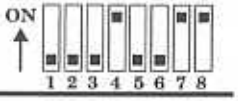
Note: *The base memory address is set with switches 1-2 and 4-8. The base I/O address is set with switch 3.*

1.3.2. Addressing Above One Megabyte

When addressing above one megabyte, both the base memory and base I/O addresses are set with all eight switches. Address settings directly relate to the number of controllers installed in the system.

Table 1-2 shows the available base memory and base I/O addresses above one megabyte.

Table 1-2. Addresses Above One Megabyte

Controller	Base Memory Address	Base I/O Address	DIP Switch Settings
Primary Addresses			
1	F00000 - F1FFFF	218 - 21B	
2	EE0000 - EFFFFF	21C - 21F	
3	EC0000 - EDFFFF	238 - 23B	
4	EA0000 - EBFFFF	23C - 23F	
Secondary Addresses			
1	D00000 - D1FFFF	218 - 21B	
2	D20000 - D3FFFF	21C - 21F	
3	D40000 - D5FFFF	238 - 23B	
4	D60000 - D7FFFF	23C - 23F	

1.4. Selecting the EPROM Size

The default EPROM size is 32K. If you choose a different EPROM size, use Table 1-3 to change the JP3 and JP4 jumper settings accordingly.

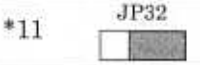
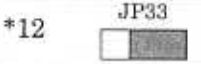
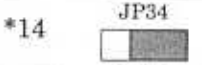
Table 1-3. EPROM Jumper Settings

EPROM Size and Type	JP3 1 2 3	JP4 1 2 3
32K-default (2764/27128)		
64K (27256)		
128K (27512)		

1.5. Selecting the Interrupt Request

The interrupt request (IRQ) is selected by setting one of the six shorting jumpers (JP30 through JP35). Five of the six jumpers will not be used. Table 1-4 shows the jumper settings for all of the available IRQs (the controller is shipped without an IRQ set).

Table 1-4. IRQ Jumper Settings

IRQ	Jumper 1 2 3	IRQ	Jumper 1 2 3
2	JP30 	9	JP30 
3	JP31 	*10	JP31 
4	JP32 	*11	JP32 
5	JP33 	*12	JP33 
6	JP34 	*14	JP34 
7	JP35 	*15	JP35 

Note: ** To use IRQs 10 through 15, the controller must be installed in a 16-bit slot.*

In some instances, a jumper must be set neutrally (disabled). If you have a Comtrol device driver, refer to the documentation that came with it for the IRQs available for your system.

Figure 1-2 shows how to set a jumper neutrally.

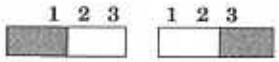


Figure 1-2. Neutral Jumper Settings

1.6. Selecting the PC/AT Mode

The controller operates in either PC (8-bit) or AT (16-bit) mode. When using an 8-bit bus, you must select PC mode. When using a 16-bit bus, select either PC or AT mode.

Figure 1-3 shows the settings for PC/AT mode.

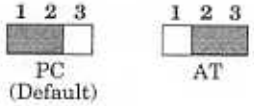


Figure 1-3. Jumper Settings for PC/AT Mode

1.7. Communications Jumpers

The controller is shipped with the communications jumpers set to operate in RS-232 synchronous or asynchronous mode with full modem control (only ports 1 and 5 operate in synchronous mode).

The firmware does not program the 8530 SCCs for synchronous operation. This must be done by the software that is downloaded to the controller.

1.7.1. Synchronous Mode Interfaces

Table 1-5 lists the interfaces that can be used with the *Smart* Hostess in synchronous mode.

Table 1-5. Interfaces Used for Synchronous Mode

Mode	# of Ports	Connector	Part #s
*RS-232/422	4 or 8	Male or Female DB25	INHX0410 INHX0420 INHX0810 INHX0820
**RS-422/485	8	Female DB9	INHX0840

* Use only RS-232 for synchronous mode. Only ports 1 and 5 can operate in synchronous mode.

** Use only RS-422 for synchronous mode.

On the controller, use J8 through J11 to select the communications mode for each port. Each block of ten jumpers configures two particular ports. Each jumper in the block is labeled from A through J. Table 1-6 shows the jumper blocks and the ports they configure.

Table 1-6. Port Communications

Jumper Block	A-E	F-J
J8	Port 1	Port 2
J9	Port 3	Port 4
J10	Port 5	Port 6
J11	Port 7	Port 8

1.7.2. Setting the Communications Mode

Figure 1-4 shows the default communications jumper settings.

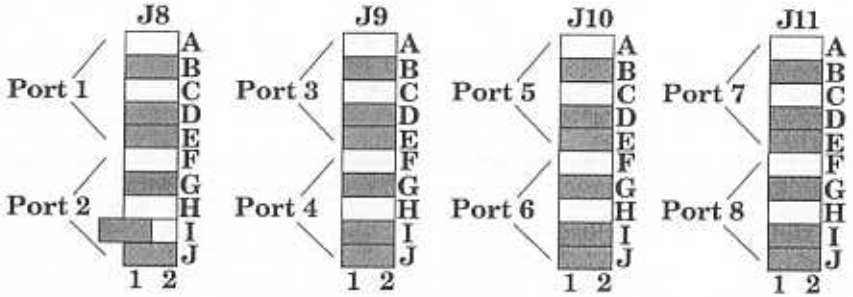


Figure 1-4. Default Jumper Settings

Note: *The transmit clock for port 2 is disabled (J8I).*

Table 1-7 describes the functions of jumpers A through J.

Table 1-7. Communications Jumpers

Jumper	Comments
A Configures Ports 1, 3, 5, 7	When installed, this jumper enables the DTE transmit clock source. This signal outputs on pin 24 when using a DB25 RS-232 connector, and it replaces DTR on ports 3 and 7. *Set A or D, but never both.*
B Configures Ports 1, 3, 5, 7	When installed, this jumper enables the DTR. This signal outputs on pin 20 when using a DB25 RS-232 connector.
C Configures Ports 1, 3, 5, 7	When installed, this jumper enables the DCE receive clock source for RS-422 synchronous mode. *Set C or E, but never both.*
D Configures Ports 1, 3, 5, 7	When installed, this jumper enables the DCE transmit clock source. This signal inputs on pin 15 when using a DB25 RS-232 connector. *Set D or A, but never both.*
E Configures Ports 1, 3, 5, 7	When installed, this jumper enables the DCE receive clock source. This signal inputs on pin 17 when using a DB25 RS-232 connector. *Set E or C, but never both.*
F Configures Ports 2, 4, 6, 8	When installed, this jumper enables the DTE transmit clock source. This signal outputs on pin 24 when using a DB25 RS-232 connector, and it replaces DTR. *Set either F or I, but never both.*
G Configures Ports 2, 4, 6, 8	When installed, this jumper enables DTR. This signal outputs on pin 20 when using a DB25 RS-232 connector.
H Configures Ports 2, 4, 6, 8	When installed, this jumper enables the DCE receive clock source for RS-422 synchronous mode. *Set H or J, but never both.*
I Configures Ports 2, 4, 6, 8	When installed, this jumper enables the DCE transmit clock source. This signal inputs on pin 15 when using a DB25 RS-232 connector. *Set either I or F, but never both.*
J Configures Ports 2, 4, 6, 8	When installed, this jumper enables the DCE receive clock source. This signal inputs on pin 17 when using a DB25 RS-232 connector. *Set J or H, but never both.*

1.7.3. DB25 Synchronous Clock Signals

Table 1-8 defines the clock signals for RS-232 synchronous mode with a DB25 connector.

Table 1-8. RS-232 Synchronous Clock Signals

Location	Receive Clock (Input)	DCE Transmit Clock (Input)	DTE Transmit Clock (Output)
RS-232 Pin	17	15	24
8530 Pin	RTxC	TRxC	TRxC

Note: *It is unnecessary to disable these signals when they are not in use.*

The DCE transmit clock signal is used when the clock is supplied from the remote device (synchronous modem). The DTE transmit clock signal is used when the clock is supplied to the remote device, along with the transmitted data.

1.8. Installing the Controller

After the controller is configured, use the following installation steps.

Warning: *Static electricity may damage the controller. When touching the controller, wear a grounding strap. Hold the controller only by its edges or the mounting bracket.*

1. Turn the power switch for the system unit to the OFF position.
2. Remove the system unit cover.
3. Select a slot to install the controller.
4. Remove the expansion slot cover.
5. Insert the controller in the expansion slot, making sure that it is properly seated.
6. Attach the controller to the chassis with the expansion slot screw. Repeat steps 3 through 5 for each controller.
7. Replace the cover on the system unit.

Once the controller is installed, refer to your *Interface Reference Card* to attach the interface.

1.9. Upgrading the Controller

Use the following steps to upgrade your *Smart* Hostess from a 4-port to an 8-port controller.

1. Purchase an upgrade kit and an 8-port interface box.
2. Remove the 4-port controller from your system.
3. Align the J2A and J2B connectors on the upgrade module to the J2A and J2B connectors on the controller.
4. Snap the module into place, by putting pressure directly over the connectors.
5. Place the controller back into your system.
6. Attach the interface cable.
7. Reinstall the device driver.

Section 2. Developing Applications

The *Smart* Hostess was designed not only for the end-user, but also for software developers. Developers can request one or both of the following sample diskettes:

- Sample Programs (part number 6021)
- Mini-Toolbox and Demo for MS-DOS (part number 6020)

The following subsections provide information about the sample programs, detail files, and routines that are available for developers.

2.1. Sample Programs

The following is a list of sample program files intended to help developers write their own applications with the *Smart* Hostess:

- **SAMPLE.DOC**

  Describes the software tools used during the development of the sample programs.
- **SAMPLE.BAT**

  This batch file contains the commands used to generate the loader and control program executable files.
- **SAMPLE.EQU**

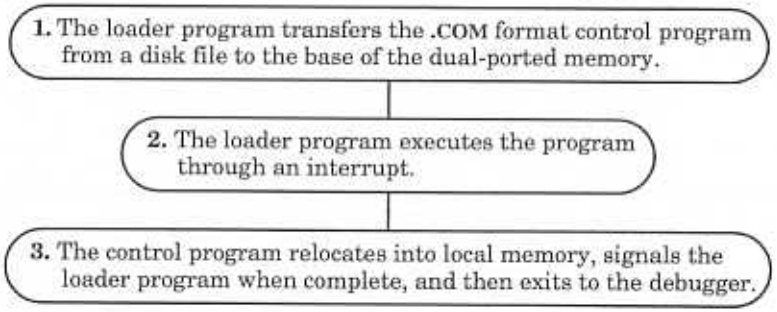
  This equate file defines dual-ported memory.
- **LOADER.ASM, LOADER.LST,** and **LOADER.EXE**

  Contains the source, listing, and executable files for the loader program.
- **CTRLPGM.ASM, CTRLPGM.LST, RELOCATE.ASM, RELOCATE.LST,** and **CTRLPGM.BIN**

  Contains the source, listing and executable files for the control program.

2.1.1. Loader Program

Flowchart 2-1 provides an overview for the loader program.



Flowchart 2-1. Loader Program Overview

The loader program expects dual-ported memory to be located at segment 9000h and the base I/O address to be located at 238h. These values can be altered through equates in the **LOADER.ASM** file.

Initiate the loader program as follows:

A > loader

If the load process is successful, the loader program displays the following:

Sample SMART HOSTESS loader program
Copyright (C) 1987 Comtrol Corporation. All rights reserved.
Loading the SMART HOSTESS control program...load complete

If the load process is unsuccessful, the loader program displays one of the following messages:

timeout error: SMART HOSTESS adapter failed to respond

This message indicates that the loader program did not receive a signal from the *Smart* Hostess. The dual-ported memory or I/O address for the controller may not be at the location expected by the loader program.

open error: ctrlpgm.bin

This message indicates that an error occurred when opening the **CTRLPGM.BIN** control program file.

read error: ctrlpgm.bin

This message indicates that an error occurred when reading the **CTRLPGM.BIN** control program file.

close error: ctrlpgm.bin

This message indicates that an error occurred when closing the **CTRLPGM.BIN** control program file.

2.2. Mini-Toolbox and Demo for the MS-DOS Operating System

The diskette that contains the *Smart* Hostess Mini-Toolbox and Demo for the MS-DOS operating system has a library of routines to assist programmers with writing their own application software programs.

The diskette contains the following files:

- **DEMO.DOC**
  Contains a copy of this subsection.
- **DPRAM.DOC**
  Contains a map of dual-ported memory.
- **DPRAM.EQU**
  Includes the program definitions for dual-ported memory.
- **SCC.EQU**
  Includes the program definitions for the 8530 chip.
- **CTRLPGM.BIN**
  Contains the executable communications program that runs on the *Smart* Hostess.
- **LDLINK.BAT**
  Contains the batch file to assemble and link **LOADER.EXE**. **LOADER.ASM** is the assembler source for **LOADER.EXE**.
- **LOADX.ASM**
  Contains the assembler source for **LOADER.EXE**.
- **LOADER.EXE**
  This file is a program that downloads **CTRLPGM.BIN** to the *Smart* Hostess.
- **SHLIB.ASM**
  Includes toolbox routines to open, close, read to, and write from a *Smart* Hostess port.
- **SHLINK.BAT**
  This is a batch file that compiles and links **SHTERM.EXE**.
- **SHTERM.C**
  Contains the C source for the **SHTERM.EXE** demo program.
- **SHTERM.EXE**
  This is a demo program to transmit to and receive from a *Smart* Hostess port.

2.2.1. SHTERM.EXE

SHTERM.EXE is a demonstration program that transmits and receives characters typed from a keyboard. The following steps describe how to use this program:

1. Configure the controller with the following settings:
   - Set the controller's memory address to D000h and the I/O address to 238h.
   - Set the controller to AT mode.
   - Do not set any hardware interrupts.
2. Install the controller in the system.
3. Hook up a dumb ASCII terminal to the port of the controller that you want to test. The terminal should be set at 9600 baud, 8 data bits, 1 stop bit, no parity, and no flow control.
4. Boot the system.
5. Execute the **LOADER.EXE** program.
6. Execute the **SHTERM.EXE** program, which sends and receives any characters typed into the appropriate keyboard until the **<F10>** key is pressed.

2.2.2. SHLIB.ASM

SHLIB.ASM is the assembler source for the **shopen()**, **shclose()**, **shread()**, and **shwrite()** routines.

This file can be assembled and linked to an application program that allows access to the controller's ports. The following list describes the four routines in C syntax:

- **shopen()**

  ```
  int shopen(portnum)
  int portnum;      /* number (0-7) of SMART HOSTESS port */
  ```

  This routine opens the requested port, and initializes it to 9600 baud, 8 data bits, 1 stop bit, and no parity. A 1 is returned if successful, a 0 is returned if unsuccessful.

- **shclose()**

  ```
  int shclose(portnum)
  int portnum;      /* number (0-7) of SMART HOSTESS port */
  ```

  This routine closes the requested port and returns a 1 if successful, or a 0 if unsuccessful.

- **shread()**

  ```
  shread(buffer,cnt,portnum)
  char *buffer;     /* local receive buffer */
  int cnt;          /* number of bytes to read */
  int portnum;      /* number (0-7) of SMART HOSTESS port */
  ```

  This routine reads a maximum of **cnt** bytes into the receive buffer and does not wait for bytes to read. It also returns the number of bytes read (0 - **cnt**).

- **shwrite()**

  ```
  shwrite(buffer,cnt,portnum)
  char *buffer;     /* local transmit buffer */
  int cnt;          /* number of bytes to write */
  int portnum;      /* number (0-7) of SMART HOSTESS port */
  ```

  This routine writes a maximum of **cnt** bytes from the transmit buffer into dual-ported memory and does not wait for enough room to become available if the **cnt** request is too large. It also returns the number of bytes written (0 - **cnt**).

Section 3. Programming the Controller

3.1. Overview

A significant part of programming the *Smart* Hostess controller involves the 80186 Communications Processor and the 8530 Serial Communications Controllers (SCCs).

This section discusses the following topics:

3.2. Communications Processor Restrictions

The following restrictions apply to the communications processor:

- Software released by Comtrol assumes that the 80186 Peripheral Control Block will be located at the very top (FF00h to FFFFh) of the I/O space. This is the default location.
- DMA channel 1 and timer channel 2 are reserved for memory refresh functions.

Comtrol supplies the software to initialize the communications processor, initiate memory refresh, and perform diagnostics on the system components.

3.3. Communications Processor Overview

Standard configuration for the communications processor consists of 32K of EPROM and 256K of RAM. The amount of EPROM can be expanded to 64K or 128K. The amount of RAM can be expanded to 384K or 512K.

The upper memory Chip Select Line selects the EPROM. The upper address of the EPROM is fixed at FFFFFh. The lower limit varies depending on the amount of EPROM installed (see Figure 3-1).

The processor has four mid-range memory Chip Select Lines that select the RAM. The lower memory Chip Select Line is not used. Software released by Comtrol sets the base address of RAM at 00000h.

The RAM located between 00000h and 3FFFFh is local memory (128K) and can only be accessed by the communications processor. The RAM located between 40000h and 7FFFFh is dual-ported memory (128K) and can be accessed by both the system processor and the communications processor.

Another 128K of memory can be added to either or both of the local and dual-ported areas. This increases the amount of RAM to 384K or 512K.

Peripheral Chip Select Lines control the selection of the I/O ports. Each Chip Select Line selects a contiguous block of 128 bytes. The base address of this block is programmable and can be located in either I/O or memory space. Software released by Comtrol sets the base address of the peripheral chip select block at 0000h, within the I/O address space.

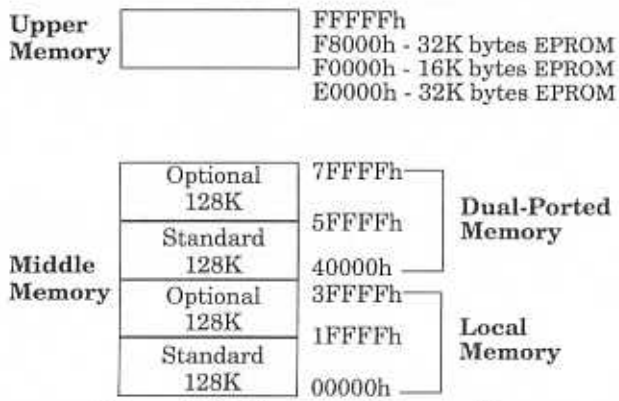


Figure 3-1. Memory Address Map

Note: *The information in Figure 3-1 and Table 3-1 applies only to a specifically programmed configuration of the Chip Select Unit. Software released by Comtrol adheres to this configuration.*

3.4. I/O Address Map

Table 3-1 shows sixteen I/O ports and their address registers on the Serial Communications Controllers (SCCs).

Table 3-1. Address Registers

I/O Port	Address Register Description
0000h	Port 2 command register (SCC #1, Channel B)
0002h	Port 2 data register
0004h	Port 1 command register (SCC #1, Channel A)
0006h	Port 1 data register
0080h	Port 4 command register (SCC #2, Channel B)
0082h	Port 4 data register
0084h	Port 3 command register (SCC #2, Channel A)
0086h	Port 3 data register
0100h	Port 6 command register (SCC#3, Channel B)*
0102h	Port 6 data register
0104h	Port 5 command register (SCC#3, Channel A)*
0106h	Port 5 data register
0180h	Port 8 command register (SCC#4, Channel B)*
0182h	Port 8 data register
0184h	Port 7 command register (SCC#4, Channel A)*
0186h	Port 7 data register

* These I/O ports are only valid on the 8-port controller.

Table 3-2 shows four different I/O ports that address the miscellaneous registers on the communications processor.

Table 3-2. Miscellaneous Address Register Description

I/O Port	Type	Description
0200h	Read	**Modem Status Register (16 bit)** The bits of this register indicate the state of the Data Set Ready and Ring Indicator signals for each communications line (see Table 3-3).
0200h	Write	**Output Register (8 bit)** The contents of this register can be read by the system processor. Usage of this register is defined by the software.
0202h	Read	**Input Register (8 bit)** The contents of this register can be written by the system processor. Usage of this register is defined by the software.
0202h	Write	**Control Register #1 (16 bit)** The bits of this register are defined in Table 3-4.
0204h	Read	**Configuration Switch (8 bit)** Reading this input port yields the state of the eight position configuration (DIP) switch. Usage of the configuration switch is defined by the software. Switch positions 1 through 8 correspond to bits 0 through 7 respectively. A switch in the ON position is read as 0.
0204h	Write	**Control Register #2 (16 bit)** The bits of this register are defined in Table 3-5.
0206h	Write	**Clear System Interrupt** Writing to this port clears any pending interrupt from the system processor to the communications processor.

Tables 3-3 through 3-5 describe some of the address registers listed in Table 3-2.

Table 3-3. Modem Status Register Bit Description

Bit #	Description	Bit #	Description
15	Port 8 RI*	7	Port 8 DSR*
14	Port 7 RI*	6	Port 7 DSR*
13	Port 6 RI*	5	Port 6 DSR*
12	Port 5 RI*	5	Port 6 DSR*
11	Port 4 RI	4	Port 5 DSR*
10	Port 3 RI	3	Port 4 DSR
9	Port 2 RI	2	Port 3 DSR
8	Port 1 RI	1	Port 2 DSR
7	Port 8 DSR*	0	Port 1 DSR

* These bits are only valid on an 8-port controller.

Table 3-4. Control Register #1 Bit Description

Bit#	Description
15	Enables the system processor to interrupt the communications processor. This bit value should be 1.
14	Interrupts the system processor on the selected interrupt request line. This bit must be reset to clear the interrupt request. This bit value should be 1.
13–10	Defines the offset into dual-ported memory of the system processor's window (see Table 3-7).
9	Enables the system processor to access the dual-ported memory on the communications processor. This bit value should be 1.
8-6	Defines the size of the system processor's window into dual-ported memory: Bits 8 7 6 - Window Size 0 0 0 - 128K 1 0 0 - 64K 1 1 0 - 32K 1 1 1 - 16K 64K, 32K, and 16K are not valid in AT mode.

(Continued)

Table 3-4. Control Register #1 Bit Description (Continued)

Bit#	Description
5-0	Defines the base location of dual-ported memory in the system processor's memory space. The bits correspond to the system processor's memory address bits (see Table 3-6).

Table 3-5. Control Register #2 Bit Description

Bit#	Description
15	Enables the system processor to access the I/O ports on the communications processor. This bit value should be 1.
14-8	Defines the base location of the I/O ports in the system processor's I/O space. They correspond to the system processor's 11, 10, 8-5, and 2 I/O address bits. The system processor's 9, 4, and 3 I/O address bits must be set to one (1) (see Table 3-8).
7-5	Not used.
4	Resets the Non-Maskable Interrupt (NMI) logic. Following an NMI and during initialization, this bit must be toggled to zero (0) and then back to one (1). This allows further interrupts to occur.
3-0	Together with bits 5-0 of Control Register #1, these bits define the base location of dual-ported memory in the system processor's memory space. The bits are only effective if AT mode is used, otherwise they are ignored. They correspond to the system processor's 23-20 memory address bits.

3.5. System Processor Memory and I/O Port Locations

Table 3-6 defines the possible base locations of dual-ported memory, which is in the system processor's memory space. Either PC or AT mode can be used:

- When using PC mode, bits 5-0 of Control Register #1 define the one megabyte page of the system processor's memory space.
- When using AT mode, bits 3-0 of Control Register #2 define the one megabyte page of the system processor's memory space.

The base location of dual-ported memory must be a multiple of the system processor's window size. The third column in the following table specifies the valid window sizes for each base address.

Note: *When using AT mode, the only valid window size is 128K.*

Table 3-6. Dual-Ported Memory Base Locations

Bits 5-0	Base Location	Window Sizes	Bits 5-0	Base Location	Window Sizes
0000h	00000h	16K, 32K 64K, 128K	0017h	5C000h	16K
0001h	04000h	16K	0018h	60000h	16K, 32K, 64K, 128K
0002h	08000h	16K, 32K	0019h	64000h	16K
0003h	0C000h	16K	001Ah	68000h	16K, 32K
0004h	10000h	16K, 32K, 64K	001Bh	6C000h	16K
0005h	14000h	16K	001Ch	70000h	16K, 32K, 64K
0006h	18000h	16K, 32K	001Dh	74000h	16K
0007h	1C000h	16K	001Eh	78000h	16K, 32K
0008h	20000h	16K, 32K, 64K, 128K	001Fh	7C000h	16K
0009h	24000h	16K	0020h	80000h	16K, 32K, 64K, 128K
000Ah	28000h	16K, 32K	0021h	84000h	16K
000Bh	2C000h	16K	0022h	88000h	16K, 32K
000Ch	30000h	16K, 32K, 64K	0023h	8C000h	16K
000Dh	34000h	16K	0024h	90000h	16K, 32K, 64K
000Eh	38000h	16K, 32K	0025h	94000h	16K
000Fh	3C000h	16K	0026h	98000h	16K, 32K
0010h	40000h	16K, 32K, 64K, 128K	0027h	9C000h	16K
0011h	44000h	16K	0028h	A0000h	16K, 32K, 64K, 128K
0012h	48000h	16K, 32K	0029h	A4000h	16K
0013h	4C000h	16K	002Ah	A8000h	16K, 32K
0014h	50000h	16K, 32K, 64K	002Bh	AC000h	16K
0015h	54000h	16K	002Ch	B0000h	16K, 32K, 64K
0016h	58000h	16K, 32K	002Dh	B4000h	16K

(Continued)

Table 3-6. Dual-Ported Memory Base Locations (Continued)

Bits 5-0	Base Location	Window Sizes	Bits 5-0	Base Location	Window Sizes
002Eh	B8000h	16K, 32K	0037h	DC000h	16K
002Fh	BC000h	16K	0038h	E0000h	16K, 32K, 64K, 128K
0030h	C0000h	16K, 32K, 64K, 128K	0039h	E4000h	16K
0031h	C4000h	16K	003Ah	E8000h	16K, 32K
0032h	C8000h	16K, 32K	003Bh	EC000h	16K
0033h	CC000h	16K	003Ch	F0000h	16K, 32K, 64K
0034h	D0000h	16K, 32K, 64K	003Dh	F4000h	16K
0035h	D4000h	16K	003Eh	F8000h	16K, 32K
0036h	D8000h	16K, 32K	003Fh	FC000h	16K

Table 3-7. Offset to Dual-Ported Memory

Control Register #1 Bits 13-10	16K Window Offset	32K Window Offset	64K Window Offset	128K Window Offset
0000h	+0	+0	+0	+0
0400h	+16K	+0	+0	+0
0800h	+32K	+32K	+0	+0
0C00h	+48K	+32K	+0	+0
1000h	+64K	+64K	+64K	+0
1400h	+80K	+64K	+64K	+0
1800h	+96K	+96K	+64K	+0
1C00h	+112K	+96K	+64K	+0
2000h*	+128K	+128K	+128K	+128K
2400h*	+144K	+128K	+128K	+128K
2800h*	+160K	+160K	+128K	+128K
2C00h*	+176K	+160K	+128K	+128K
3000h*	+192K	+192K	+192K	+128K
3400h*	+208K	+192K	+192K	+128K
3800h*	+224K	+224K	+192K	+128K
3C00h*	+240K	+224K	+192K	+128K

* These offsets are only valid if the controller has 256K bytes of dual-ported memory.

Table 3-8 defines all possible base locations of I/O ports in the system processor's I/O space.

Table 3-8. System I/O Ports

Control Register #2 Bits 14–8	Base Location of I/O Ports	Control Register #2 Bits 14–8	Base Location of I/O Ports
0000h	0218h	2300h	063Ch
0100h	021Ch	2400h	0658h
0200h	0238h	2500h	065Ch
0300h	023Ch	2600h	0678h
0400h	0258h	2700h	067Ch
0500h	025Ch	2800h	0698h
0600h	0278h	2900h	069Ch
0700h	027Ch	2A00h	06B8h
0800h	0298h	2B00h	06BCh
0900h	029Ch	2C00h	06D8h
0A00h	02B8h	2D00h	06DCh
0B00h	02BCh	2E00h	06F8h
0C00h	02D8h	2F00h	06FCh
0D00h	02DCh	3000h	0718h
0E00h	02F8h	3100h	071Ch
0F00h	02FCh	3200h	0738h
1000h	0318h	3300h	073Ch
1100h	031Ch	3400h	0758h
1200h	0388h	3500h	075Ch
1300h	033Ch	3600h	0778h
1400h	0358h	3700h	077Ch
1500h	035Ch	3800h	0798h
1600h	0378h	3900h	079Ch
1700h	037Ch	3A00h	07B8h
1800h	0398h	3B00h	07BCh
1900h	039Ch	3C00h	07D8h
1A00h	03B8h	3D00h	07DCh
1B00h	03BCh	3E00h	07F8h
1C00h	03D8h	3F00h	07FCh
1D00h	03DCh	4000h	0A18h
1E00h	03F8h	4100h	0A1Ch
1F00h	03FCh	4200h	0A38h
2000h	0618h	4300h	0A3Ch
2100h	061Ch	4400h	0A58h
2200h	0638h	4500h	0A5Ch

(Continued)

Table 3-8. System I/O Ports (Continued)

Control Register #2 Bits 14–8	Base Location of I/O Ports	Control Register #2 Bits 14–8	Base Location of I/O Ports
4600h	0A78h	6300h	0E3Ch
4700h	0A7Ch	6400h	0E58h
4800h	0A98h	6500h	0E5Ch
4900h	0A9Ch	6600h	0E78h
4A00h	0AB8h	6700h	0E7Ch
4B00h	0ABCh	6800h	0E98h
4C00h	0AD8h	6900h	0E9Ch
4D00h	0ADCh	6A00h	0EB8h
4E00h	0AF8h	6B00h	0EBCh
4F00h	0AFCh	6C00h	0ED8h
5000h	0B18h	6D00h	0EDCh
5100h	0B1Ch	6E00h	0EF8h
5200h	0B38h	6F00h	0EFCh
5300h	0B3Ch	7000h	0F18h
5400h	0B58h	7100h	0F1Ch
5500h	0B5Ch	7200h	0F38h
5600h	0B78h	7300h	0F3Ch
5700h	0B7Ch	7400h	0F58h
5800h	0B98h	7500h	0F5Ch
5900h	0B9Ch	7600h	0F78h
5A00h	0BB8h	7700h	0F7Ch
5B00h	0BBCh	7800h	0F98h
5C00h	0BD8h	7900h	0F9Ch
5D00h	0BDCh	7A00h	0FB8h
5E00h	0BF8h	7B00h	0FBCh
5F00h	0BFCh	7C00h	0FD8h
6000h	0E18h	7D00h	0FDCh
6100h	0E1Ch	7E00h	0FF8h
6200h	0E38h	7F00h	0FFCh

3.6. System Processor Memory and I/O Configuration

The software executed by the communications processor specifies the following:

- The base address of dual-ported memory in the system processor's memory space
- The size of the viewing window
- The offset of the viewing window into dual-ported memory

The system processor's primary interface to the communications processor is through dual-ported memory. The system processor views dual-ported memory through a 16K, 32K, 64K, or 128K window.

If 128K of dual-ported memory is installed, there are either eight 16K windows, four 32K windows, two 64K windows, or one 128K window. The number of windows doubles if the optional 128K of dual-ported memory is also installed.

Another way to interface to the communications processor is through I/O ports. The base address of the I/O ports in the system processor's I/O space is specified by software the communications processor executes.

The system processor can write eight bits of data to a register at the base I/O address. The communications processor can read this same information. Similarly, the system processor can read eight bits of data from a register at the base I/O address, which was previously written to by the communications processor.

Note: *The controller can be reset by performing a write operation of any value to I/O base plus three (+3). A soft boot will not reset the controller. Either the write operation must be performed, or the system must be powered OFF.*

3.7. Interrupts

The communications processor accepts interrupts from two different sources:

- **System Processor**

  The system processor interrupts the communications processor by performing a byte wide write operation to the communications processor's base I/O address plus two (+2).

  Make certain that a byte wide write is performed, rather than a word wide write. The word wide write resets the controller due to the function of I/O base plus three (+3), which is viewed by the communications processor on the INT1 line. Usage of this interrupt is defined by the software.

- **Serial Communications Controllers (SCC)**

  The SCCs interrupt the communications processor on the INT0 line, through the interrupt daisy chain system.

  Figure 3-2 shows the interrupt priority for the SCCs.

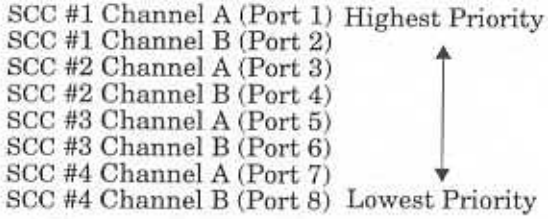


Figure 3-2. SCC Interrupt Priority

The communications processor interrupts the system processor by setting bit 14 of Control Register #1. This interrupt is placed on the IRQ line defined by the IRQ jumpers. To remove the interrupt, clear bit 14. Usage of this interrupt is defined by the software.

3.8. Determining Baud Rate Times

The Baud Rate Time Constant (BRTC) is determined by the following formula:

$$\text{BRTC} = \frac{\text{Serial Clock Frequency}}{2 \times (\text{Baud Rate} \times \text{Baud Rate Factor})} - 2$$

Figure 3-3. Baud Rate Time Constant Formula

Note: *For the communications processor, the Serial Clock Frequency = 4.9152 MHz.*

Table 3-9 shows the BRTCs for the various Baud Rate Factors, along with the standard line speeds for the communications processor.

Table 3-9. Baud Rate Time Constants

Baud Rate	Baud Rate Factor X1*	X16	X32	X64
76800	30	0	*	*
56000	41.886	0.743	*	*
38400	62	2	*	*
19200	126	6	2	0
9600	254	14	6	2
7200	339.333	19.333	8.667	3.333
4800	510	30	14	6
3600	680.667	40.667	19.333	8.667
2400	1022	62	30	14
2000	1226.8	74.8	36.4	17.2
1800	1363.333	83.333	40.667	19.333
1200	2046	126	62	30
600	4094	254	126	62
300	8190	510	254	126
150	16382	1022	510	254
134.5	18270.119	1140.007	569.004	283.502
110	22339.818	1394.364	696.182	347.091
75	32766	2046	1022	510
50	49150	3070	1534	766

Notes: *Using the X1 Baud Rate Factor for asynchronous communications is not reliable.*

A Baud Rate Time Constant value of zero is valid.

3.9. Timer 0 External Clock

The TRxC output from SCC #1 Channel B (Port 2) is supplied to the communications processor's timer 0 external clock input (TMR in 0). This makes the baud rate generator clock available to timer 0 to precisely time serial transmissions.

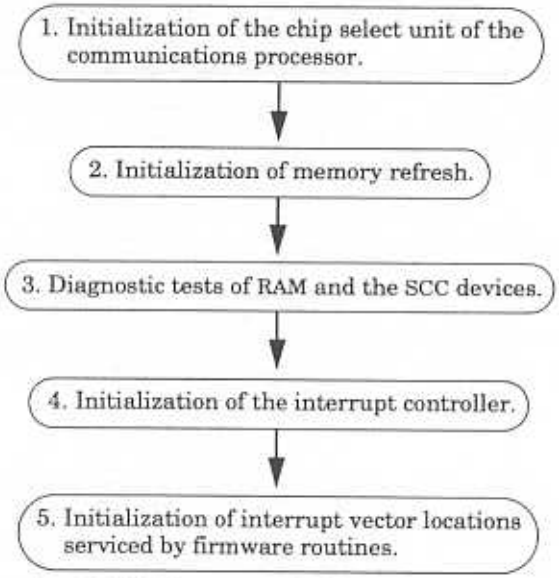
To supply the baud rate generator output to the TRxC output, program the SCC #1 Channel B (Port 2), write register 11, bits 1 and 0 to the binary value of 10. Timer 0 sets the EXT control bit 2 of the timer mode control register. This selects the TRxC output as the timer's clock input.

Section 4. Firmware

This section discusses the controller firmware. The firmware initializes the controller when the system boots. It also provides several other functions invoked by user programs.

4.1. Initializing the Controller

The firmware executes an initialization sequence consisting of the following major steps:



Flowchart 4-1. Firmware Initialization Sequence

- Step 1 determines the location of memory and I/O.
- Timer Channel 2 and DMA Channel 1 are dedicated to Step 2.
- Step 4 determines the interrupt modes for the SCC devices and the system processor.

Following initialization, the firmware halts and waits for an interrupt from the system processor indicating that a user program is loaded. When the interrupt is received, the firmware checks the first two bytes of dual-ported memory for a sequence of 55h, AAh. If this sequence is found, the firmware performs a far call to offset +80h in dual-ported memory and executes the user program.

4.2. Firmware Functions

In addition to system initialization, the firmware provides several functions that are invoked by user programs through the following software interrupts:

- **INT 20h - Debug**

  This interrupt invokes the firmware debugger. During system initialization, the firmware configures the first serial port as the debug console. This is altered by using **INT 22h**. Operation of the firmware debugger is described in Section 5.

- **INT 21h - Firmware RAM Query**

  The firmware uses the memory area immediately above the interrupt vectors (400h) as a work area. A user program determines the segment address of the first paragraph past the end of the firmware work area by executing a software **INT 21h**. The segment address is returned in register AX. Other registers are not altered.

- **INT 22h - Debug Device Initialization**

  This interrupt alters the debug console. Before the interrupt executes, a valid device number (0 through 7) must be loaded into the AL register.

  Device numbers 0 through 7 correspond to I/O ports 1 through 8. The firmware attempts to execute a request specifying a device number in this range. This occurs without regard to the contents of the SCC device configuration map (see **INT 23h**). A request specifying a device number outside the range is ignored. Registers are not altered.

- **INT 23h - Configuration Map Query**

  This interrupt queries the firmware for the system configuration. The firmware returns a copy of the configuration map in the AX register. Other registers are not altered.

  The AH register (the SCC map) contains one bit for each possible SCC channel. A set bit indicates the associated SCC channel is present and has successfully passed the SCC diagnostic test. A bit not set indicates that either the SCC channel does not exist, or that it failed the diagnostic test.

  Table 4-1 shows bit values and the associated SCC channels.

Table 4-1. SCC Channel Bit Values

Bit Value	SCC Channel
Bit 0 (01h)	SCC 1 Channel A
Bit 1 (02h)	SCC 1 Channel B
Bit 2 (04h)	SCC 2 Channel A
Bit 3 (08h)	SCC 2 Channel B
Bit 4 (10h)	SCC 3 Channel A
Bit 5 (20h)	SCC 3 Channel B
Bit 6 (40h)	SCC 4 Channel A
Bit 7 (80h)	SCC 4 Channel B

The AL register (the DRAM map) contains one bit for each possible memory segment. A set bit indicates the associated memory segment is present and has successfully passed the memory diagnostic test. A bit not set indicates that either the memory segment does not exist, or that it failed the diagnostic test.

Table 4-2 shows bit values and the associated memory segments.

Table 4-2. Memory Segment Bit Values

Local		Dual-Ported	
Bit Value	**Memory Segment**	**Bit Value**	**Memory Segment**
Bit 0 (01h)	0 - 0FFFFh	Bit 4 (10h)	40000 - 4FFFFh
Bit 1 (02h)	10000 - 1FFFFh	Bit 5 (20h)	50000 - 5FFFFh
Bit 2 (04h)	20000 - 2FFFFh	Bit 6 (40h)	60000 - 6FFFFh
Bit 3 (08h)	30000 - 3FFFFh	Bit 7 (80h)	70000 - 7FFFFh

- **INT 24h - Get Control Register Values**

  This interrupt returns the values written to Control Register #1 and Control Register #2 either by the initialization process, or by the last invocation of **INT 25h**. The value written to Control Register #1 is returned in the AX register. The value written to Control Register #2 is returned in the DX register. Other registers are not altered.

- **INT 25h - Set Control Register Values**

  This interrupt updates the values of Control Register #1 and Control Register #2. A copy of the control register values is saved in the firmware work area for use by **INT 24h** requests. Control Register #1 is updated with the value in the AX register. Control Register #2 is updated with the value in the DX register. Registers are not altered.

Note: *INT 24h is only useful if INT 25h executes all updates to the control registers. If the user program updates the control registers directly, INT 24h returns invalid values.*

Section 5. Firmware Debugger

5.1. Background

This section explains the commands to use with the firmware debugger. The debugger, which is part of the firmware installed on the controller, provides the following functions:

- Displays memory
- Disassembles instructions
- Sets breakpoints
- Displays registers
- Single steps
- Performs input and output to I/O ports

The debugger console is initially assigned to the first serial port on the controller. The serial communications parameters are defined as follows:

- 9600 bits/second
- No parity
- Eight (8) bits per character
- One (1) stop bit

Because these parameters are fixed, a program cannot alter them.

The controller firmware provides access to debugger functions through the following software interrupts:

- **INT 20h** (see Subsection 4.2)
- **INT 22h** (see Subsection 4.2)

In order to access the firmware debugger, Comtrol recommends that you have the following items:

- A debug/reset switch box or an older interface box with a debug/reset switch
- A debug/reset header on the controller

Contact Comtrol if you are missing any of these items.

A cable attaches the debug/reset switch box to the debug/reset header on the controller. Press the switch on the box, which generates an NMI interrupt, to invoke the firmware debugger.

Note: *If you have an older interface box with a debug/reset switch, press the switch on the interface box to invoke the firmware debugger.*

5.2. Debugger Commands

Table 5-1 lists debugger commands.

Table 5-1. Debugger Commands

Command	Name	Function
B	Byte	Formats all succeeding input or output commands to read or write 8 bit values.
D	Dump	Displays the contents of a specified memory region.
G	Go	Continues execution from the current location with or without breakpoints.
I	Input	Inputs and displays a byte or word from the specified I/O port.
O	Output	Outputs a byte or word to the specified I/O port.
R	Register	Displays the contents of all registers.
T	Trace	Executes the next instruction (single step).
U	Unassemble	Disassembles a specified memory region.
W	Word	Formats all succeeding input or output commands to read or write 16 bit values.

5.3. Debugger Command Definitions

This subsection describes how to use each of the debugger commands listed in Table 5-1. The following is a list of guidelines that apply to the debugger commands:

- Each command consists of a single letter, followed by one or more parameters.
- Optional parameters are displayed inside parenthesis ().
- Enter commands and parameters in uppercase, lowercase, or a combination of both.
- Commands executed after pressing **<Enter>**.

- The debugger prompt is a hyphen (-).
- The location of syntax errors is indicated by the pointer error.

5.3.1. B (Byte Mode)

The byte mode command causes all succeeding input or output commands to read or write 8 bit (byte) values.

Format:

B

Arguments are not required.

5.3.2. D (Dump)

The dump command displays the contents of a specified memory region.

Format:

D (*starting address*) (*ending address*)

or

D (*starting address*) (*l length*)

where:

starting address specifies the first address of a range of addresses to display and takes any of the following forms:

- A segment value, offset value pair separated by a colon (:)
- A segment register mnemonic and an offset value separated by a colon (:)
- An offset value only (a default segment is used)

ending address is an offset value within the segment specified by the ***starting* address**, which specifies the last address of a range of addresses to display.

l length specifies the number of bytes to display.

Note: *If* ***ending address*** *or* ***l length*** *is not specified, the default display length is 128 bytes.*

If arguments are not specified and a **D** command has not been entered, display starts at the current CS:IP location. If a **D** command has been entered, display starts with the byte following the last byte displayed. The default length is 128 bytes.

The following commands display the contents of memory from 0040h:000h through 0040h:00ffh:

D 40:0 FF

or

D 40:0 L 100

The following command displays the contents of memory from the 1000h offset. This is within the segment that the ES register currently points to. The ES register uses the 107Fh offset, which is the default length.

D ES:1000

5.3.3. G (Go)

The go command continues execution from the current location with or without breakpoints.

Format:

G (***breakpoint address***)

where:

breakpoint address specifies an address where program execution is interrupted, and control is returned to the debugger.

If a ***breakpoint address*** is not specified, the program continues normal execution.

The following command allows program execution to continue from the current location (CS:IP), and sets a breakpoint at 4000h:0007h. If the program attempts to execute the instruction at this address, execution is interrupted, and control is returned to the debugger.

G 4000:7

5.3.4. I (Input)

The input command inputs and displays a byte or word from the specified I/O port.

Format:

I ***portaddress***

where:

portaddress specifies a 16 bit I/O address for input data. The size of the input data (byte or word) depends on the current I/O mode (see Subsections 5.3.1 and 5.3.9).

The following command inputs data from the I/O port at 202h:

I 202

5.3.5. O (Output)

The output command outputs a byte or word to the specified I/O port.

Format:

O ***portaddress value***

where:

portaddress specifies a 16 bit I/O address for output data. The size of the output data specified by ***value*** (byte or word) depends on the current I/O mode (see Subsections 5.3.1 and 5.3.9).

The following command outputs 55h to the I/O port at 200h:

O 200 55

5.3.6. R (Register)

The register command displays the contents of all registers.

Format:

R

Arguments are not required.

5.3.7. T (Trace)

The trace command executes the next instruction (single step).

Format:

T

Arguments are not required.

5.3.8. U (Unassemble)

The unassemble command disassembles a specified memory region.

Format:

U (*starting address*) (*count*)

where:

starting address specifies the first address of a range of addresses to disassemble and takes any of the following forms:

- A segment value, offset value pair separated by a colon (:)
- A segment register mnemonic and an offset value separated by a colon (:)
- An offset value only (a default segment is used)

count specifies the number of instructions to disassemble. If *count* is not specified, a default of 16 instructions are disassembled.

If arguments are not specified and a U command has not been entered, disassembly begins at the current CS:IP location. If a U command has been entered, disassembly begins with the instruction following the last instruction previously displayed.

The following command disassembles eight instructions starting at 4000h:0003h:

U 4000:3 8

The following command disassembles 16 instructions (default count). Disassembly begins at the 0003h offset, within the segment that the CS register points to:

U CS:3

5.3.9. W (Word Mode)

The word mode command causes all succeeding input or output commands to read or write 16 bit (word) values.

Format:

W

Arguments are not required.

Section 6. Troubleshooting and Technical Support

6.1. Resolving Installation Problems

If installation fails or you are trying to resolve a problem, you should try the following before calling the Comtrol technical support line:

- Verify that the DIP switch and jumper settings are correct.
- Check the signals between your peripherals and the interface box to verify that they match.
- Check to make sure the cables are connected properly.
- Reseat the controller in the slot.
- Make sure that the expansion slot screw was replaced after inserting the controller.
- Check modem signal settings if the modem cannot send or receive data.

If you have not been able to get the controller operating:

1. Turn off your PC and insert the diagnostic diskette.
2. Boot the PC and follow the instructions provided by the diagnostic diskette.

Table 6-1 defines the 64-byte I/O address blocks from 0 through 3FFh and their known uses.

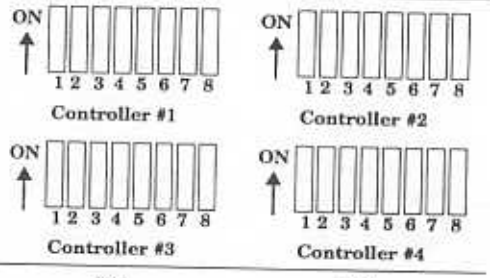
Table 6-1. System I/O Addresses – Up to 3FF

Address Block	Addresses Used	Description
000 – 03F		Reserved for Motherboard
040 – 07F		Reserved for Motherboard
080 – 0BF		Reserved for Motherboard
0C0 – 0FF		Reserved for Motherboard
100 – 13F		
140 – 17F		
180 – 1BF		
1C0 – 1FF	1F0 – 1F8	Fixed Disk
200 – 23F	218 – 21B	
240 – 27F	278 – 27F	LPT2, IDE controllers, and multifunction boards (game ports)
280 – 2BF		
2C0 – 2FF	2E8 – 2EF 2F8 – 2FF	COM4 COM2
300 – 33F	318 – 31B	
340 – 37F	378 – 37F	LPT1
380 – 3BF	3B0 – 3BF	Monochrome Display and LPT3
3C0 – 3FF	3D0 – 3DF 3E8 – 3EF 3F0 – 3F7 3F8 – 3FF	Graphics Monitor Adapter COM3 Floppy Disk Controller COM1

6.2. Placing a Support Call

Before you place a technical support call to Comtrol, please make sure that you have the following information.

Table 6-2. Support Call Information

Item	Your System Information
Controller type	4-port or 8-port
Interface type	RS-232, RS-232/422, RS-422/485, or RS-232/Current Loop
Base memory and Base I/O address (Mark the figures to show your selections)	
EPROM jumper settings (Mark the figures to show which pins you have jumpered)	
IRQ selection	
PC/AT jumper setting	PC Mode - pins 1 and 2 AT Mode - pins 2 and 3
Operating system type and release	
Device driver release number	
PC make, model, and speed	
List of other devices in the PC and their addresses	

After you have gathered this information, contact Comtrol by email, FAX, or phone:

email: **support@Comtrol.com**
FAX: **(612) 631-8117 (US)** or **(44) 869-323-211 (UK)**
Toll free: **(800) 926-6876 (US)**
Phone: **(612) 631-7654 (US)** or **(44) 869-323-220 (UK)**
BBS **(for device driver updates):**
(612) 631-8310 (US)

Appendix A. Specifications

This subsection discusses specifications for the 100-pin connector and for the controller.

A.1. 100-Pin Pinout Information

This subsection contains signal information for the 100-pin connector. Use this information to build your own cables.

Figure A-1 shows the pin locations for the 100-pin connector.

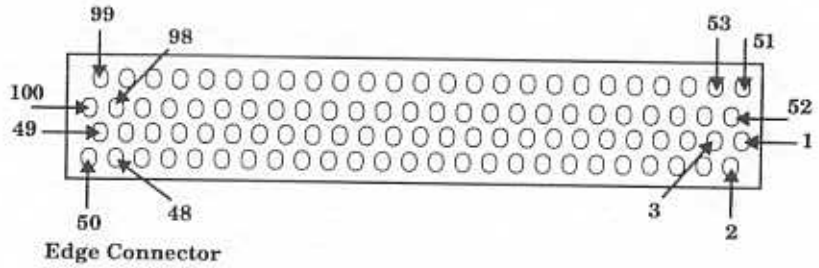


Figure A-1. 100-Pin Connector

Table A-1 lists the signals for the 100-pin connector.

Table A-1. 100-Pin Signal Information

Pin	Signal	Pin	Signal	Pin	Signal
1	RLSD1	35	RTS4	69	DTR6
2	RI1	36	-12VE	70	RC6
3	DSR1	37	DTR4	71	RCV7
4	CTS1	38	CTS4	72	XMIT7
5	XMIT1	39	DSR4	73	RTS7
6	DTR1	40	RLSD4	74	DTR7
7	RTS1	41	VCCE	75	CTS7
8	GNDE	42	VCCE	76	RI7
9	RCV1	43	RI4	77	RLSD7
10	GNDE	44	GNDE	78	TC7
11	RCV2	45	GNDE	79	DSR7
12	XMIT2	46	GNDE	80	RC7
13	RTS2	47	TC1	81	RCV8
14	CTS2	48	RC1	82	+12VE
15	RLSD2	49	RC4	83	XMIT8
16	RI2	50	SCTE1	84	TC8
17	DSR2	51	RLSD5	85	RTS8
18	TC2	52	RI5	86	-12VE
19	DTR2	53	DSR5	87	DTR8
20	RC2	54	CTS5	88	CTS8
21	RCV3	55	XMIT5	89	DSR8
22	XMIT3	56	DTR5	90	RLSD8
23	RTS3	57	RTS5	91	VCCE
24	DTR3	58	GNDE	92	VCCE
25	CTS3	59	RCV5	93	RI8
26	RI3	60	GNDE	94	GNDE
27	RLSD3	61	RCV6	95	GNDE
28	TC3	62	XMIT6	96	GNDE
29	DSR3	63	RTS6	97	TC5
30	RC3	64	CTS6	98	RC5
31	RCV4	65	RLSD6	99	RC8
32	+12VE	66	RI6	100	SCTE5
33	XMIT4	67	DSR6		
34	TC4	68	TC6		

A.2. Controller Specifications

Tables A-2 and A-3 contain specifications for the controller.

Table A-2. Conditions

Condition	Value
Air temperature: System on System off	 0 to 70 degrees C -65 to 125 degrees C
Humidity: System on System off	 8% to 80% 20% to 80%
Altitude	 0 to 10,000 feet 0 to 3,048 meters

Table A-3. Controller Specifications

Topic	Specification	
I/O ports/expansion slot	4 or 8	
Number of controllers/ system	4	
Interfaces available	RS-232, RS-232/422, RS-422/485, or RS-232/Current Loop	
Base memory address	Switch selectable	
Base I/O address	Switch selectable	
Interrupt	Jumper selectable	
Processor	80186	
Serial Communications Controllers	8530	
Control by device driver: Baud rate Data bits Stop bits	 50 through 76.8K bit/sec. 5, 6, 7, or 8 1, 1.5, or 2	
Power requirements: +5 VDC +12 VDC -12 VDC Total	4-Port 07.25 W 00.78 W 00.84 W 08.87 W	8-Port 11.60 W 01.34 W 01.56 W 14.50 W

(Continued)

Table A-3. Controller Specifications (Continued)

Topic	Specification	
Current consumption: +5 VDC +12 VDC -12 VDC	4-Port 1.450 A 0.065 A 0.070 A	8-Port 2.320 A 0.112 A 0.130 A
Heat output:	4-Port 30.2 BTU/HR	8-Port 49.4 BTU/HR
MTBF:	4-Port 11.2 years	8-Port 8.9 years
Modem control	RTS, CTS, DSR, DCD, DTR, RI	
Synchronous Signals *Ports 1 and 5 only	Receive Clock Transmit Clock (DTE/DCE)	
RAM: Dual Port RAM Local RAM Total RAM	 128K or 256K 128K or 256K 256K or 512K	
EPROM	16K (default) through 128K	
Bus interface	ISA	
FCC certification	Yes - Class A	
UL recognition	Yes - Recognized component	
EMC Canadian requirements	Yes - Meets requirements	
Dimensions	13.3" x 3.9" x .4"	

Appendix B. Warranty

Comtrol Corporation provides:

- A 30-day money-back guarantee
- A limited five (5) year warranty* (US and Canada)
- Support for your Comtrol controller for five years from the purchase date.

*Check with your distributor for guarantee conditions in countries other than the U.S.A. and Canada.

B.1. Limited Warranty

Comtrol Corporation, Inc. ("the Company") and its affiliate (Comtrol Europe, Ltd.) make no representations or warranties, expressed or implied including warranties of merchantability, noninfringement, and fitness for a particular purpose except as provided below.

B.2. Hardware

Comtrol warrants to the original purchaser that its controller is free of defect in design, materials and workmanship for five years from the date of delivery of a new controller. Comtrol (or its authorized repair center), at its option, will repair or replace, at the business location of Comtrol each part of the controller which is proven to the satisfaction of Comtrol to have been defective in design, material or workmanship.

This warranty shall not apply to any part of the controller which, in the judgment of Comtrol, has been subjected to misuse, negligence, alteration, accident, improper maintenance, or damage by excessive physical or electrical stress. Adjustment of the controller, where warning labels and operation manuals warn against such adjustments, will void this warranty.

This warranty is void if the serial number of the Comtrol controller has been defaced, altered or removed. This warranty does not apply to expendable components such as fuses or bulbs. Repair and replacement parts will be furnished on an exchange basis and may be either reconditioned or new. All replaced parts or controllers become the property of Comtrol.

The sole remedy for breach of warranty shall be repair, replacement, or refund, at the option of Comtrol, of the defective product provided as follows.

B.3. Software

Comtrol warrants that for a period of ninety (90) days from the date of delivery to you as evidenced by a copy of your receipt, the disks on which the program is furnished will under normal use be free from defects in materials and workmanship and the program under normal use will perform substantially in accordance with the documentation without significant errors that make it unusable.

Comtrol's entire liability and your exclusive remedy under this warranty (which is subject to you returning the program to Comtrol or an authorized dealer with a copy of your receipt) will be, at Comtrol's option, to attempt to correct or help you around errors with efforts that Comtrol believes suitable to the problem, to replace the program or disks with functionally equivalent software or disks, as applicable, or to refund the purchase price and terminate this agreement.

No Comtrol dealer, distributor, agent or employee is authorized to modify this warranty.

Comtrol does not warrant that the functions contained in the programs will meet your requirements or that the operation of the programs will be uninterrupted or error-free. You assume the responsibility for the selection of the programs and hardware to achieve your intended results and for the installation, use and results obtained from the programs.

Some programs contained on disk are specifically for and have been optimized to run with Comtrol products. Therefore, the programs on these disks will not run effectively and will cause errors in data or operation when this software is attempted to be used with non-Comtrol products.

This warranty shall not apply if the serial number has been defaced, altered or removed, or if the software has been altered in any fashion.

B.4. Return Procedures

To qualify for the previously discussed warranty, the original purchaser must follow the procedure outlined below:

1. Comtrol must be notified in writing within thirty (30) days of the date that the defect is discovered. Comtrol will then issue a Return Material Authorization (RMA) Number which the purchaser must include with all correspondence and display on the outside of the shipping container when returning the controller.

2. All Comtrol controllers must be shipped freight and insurance prepaid, in the original shipping container, or in a container providing equal or better protection, with the Return Material Authorization (RMA) Number displayed on the outside of the container in a prominent manner.
3. A written description of the defect together with a copy of your receipt or other proof of purchase, and the name of the dealer which sold you the Comtrol product, must be shipped with the controller. All defects must be reproducible at Comtrol's location to qualify for this limited warranty. Ship the controller to:

   Comtrol Corporation
   2675 Patton Road, Dock D
   Saint Paul, Minnesota 55113

Comtrol will return a controller which qualifies under this warranty freight and insurance prepaid. Comtrol will repair or replace the controllers that do not qualify under the terms of this warranty at the option of the purchaser, in which case the purchaser will pay the cost of repair or replacement, and return freight and insurance.

This limited warranty is in lieu of all other warranties and conditions expressed, implied or statutory including merchantability, fitness for purpose, non-infringement, course of dealing, trade or performance and all other liabilities of Comtrol all of which are hereby disclaimed.

In no event will Comtrol be liable for damages, including lost profits, lost savings or other special, punitive, incidental, or consequential damages arising out of the use of or inability to use the Comtrol controller, even if Comtrol or an authorized dealer has been advised of the possibility of such damages, or for any claim by any other party. This warranty gives you specific legal rights and you may also have other rights that vary from state to state (U.S.) or in your home country.

B.5. Limited Liability

Independent of the warranty or any other agreement between you and Comtrol, regardless of the basis for any claim, neither Comtrol nor anyone else who has been involved in the creation, production, or delivery of this software or hardware shall be liable for any direct, indirect, consequential or incidental damages; Comtrol's maximum liability shall be limited to refund of the purchase price. Some consumer laws may not allow the limitation or exclusion of incidental or consequential damages for consumer products, so the above limitations or exclusions may not apply to you. The price of the materials and programs reflects this allocation of risk.

B.6. Technical Support

If you have questions about your controller, contact Comtrol by email, FAX, or phone:

email: **support@Comtrol.com**
FAX: **(612) 631-8117 (US)** or **(44) 869-323-211 (UK)**
Toll free: **(800) 926-6876 (US)**
Phone: **(612) 631-7654 (US)** or **(44) 869-323-220 (UK)**
BBS: **(for device driver updates)**
(612) 631-8310 (US)

If you are calling for technical support, make sure that you review the *Troubleshooting and Technical Support* section before calling the technical support line.

Comtrol has a staff of hardware and software engineers, and technicians available to help you.

Index

D

E

F

G

H

I

J

L

M

N

O

P