```
MULTIPLE PROTOCOL CONTROLLER / MPC-II          ASSY PA1010407-xx

JUMPER SETTINGS

Device            Description                 Configuration

8530 SCC          Base Address = 380H         E55-E56*
                  Base Address = 280H         E55-E56 OUT

8530 SCC          Interrupt Level IRQ2        E44-E45
                  Interrupt Level IRQ3        E51-E52*
                  Interrupt Level IRQ4        E43-E44
                  Interrupt Level IRQ5        E50-E51

8530 SCC          Optimum Read/Write for PC-AT E53-E54 OUT
                  Optimum Read/Write for PC   E53-E54

8530 SCC          DTE configuration           E1-E17, E2-E18, E3-E19
                                              E4-E20, E5-E21, E6-E22
                                              E8-E24, E11-E12, E13-E29
                                              E14-E30, E15-E31, E16-E32
                                              E33-E34, E36-E38
                  DCE configuration           E1-E2, E3-E4, E5-E6
                                              E7-E8, E9-E25, E10-E26
                                              E13-E14, E17-E18, E21-E22
                                              E23-E24, E29-E30, E35-E37

8253              32-bit counter IRQ2         E40-E41
                  32-bit counter IRQ3         E47-E48
                  32-bit counter IRQ4         E39-E40*
                  32-bit counter IRQ5         E46-E47

8253              16-bit counter IRQ2         E41-E42
                  16-bit counter IRQ3         E48-E49
                  16-bit counter IRQ4         E42-E43
                  16-bit counter IRQ5         E49-E50

* Indicates factory settings.

MPC-II Register Addresses

Hex Address       Hex Address     Device        Description

280               380             74LS74        Interrupt Enable
284               384             8253          Counter 0
285               385             8253          Counter 1
286               386             8253          Counter 2
287               387             8253          Control Word Reg
288               388             8530          Channel B Control
289               389             8530          Channel B Data (Not used)
28A               38A             8530          Channel A Control
28B               38B             8530          Channel A Data
28C               38C             8530          Interrupt Vector
```

PROGRAMMING THE MPC-II CONTROLLER

Interrupts are enabled on the 8530 SCC by writing a 1 to the base address of the
MPC-II controller (280H or 380H). This register is a master interrupt enable for
the MPC-II controller. The 8530 SCC interrupt vector can be read directly from
the MPC-II interrupt vector address (28CH or 38CH). The vector read will be one
of 8 possible vectors presented by the 8530 SCC during an interrupt acknowledge
cycle if the Vector Include Status bit in WR9 is set. Otherwise, the vector
returned is the one written to WR2.