

NI 622x Specifications

Specifications listed below are typical at 25 °C unless otherwise noted. Refer to the *M Series User Manual* for more information about NI 622x devices.

Analog Input

Number of channels

NI 6220/6221	8 differential or 16 single ended
NI 6224/6229	16 differential or 32 single ended
NI 6225	40 differential or 80 single ended

ADC resolution 16 bits

DNL No missing codes
guaranteed

INL Refer to the [AI Absolute Accuracy Table](#)

Sampling rate

Maximum	250 kS/s single channel, 250 kS/s multi-channel (aggregate)
Minimum	No minimum
Timing accuracy	50 ppm of sample rate
Timing resolution	50 ns

Input coupling DC

Input range ± 10 V, ± 5 V,
 ± 1 V, ± 0.2 V

Maximum working voltage for analog inputs
(signal + common mode) ± 11 V of AI GND

CMRR (DC to 60 Hz) 92 dB

Input impedance

Device on

AI+ to AI GND >10 G Ω in parallel
with 100 pF

AI- to AI GND >10 G Ω in parallel
with 100 pF

Device off

AI+ to AI GND 820 Ω

AI- to AI GND 820 Ω

Input bias current ± 100 pA

Crosstalk (at 100 kHz)

Adjacent channels -75 dB

Non-adjacent channels -90 dB

Small signal bandwidth (-3 dB) 700 kHz

Input FIFO size 4,095 samples

Scan list memory 4,095 entries

Data transfers

PCI/PXI devices DMA (scatter-gather),
interrupts,
programmed I/O

USB devices USB Signal Stream,
programmed I/O

Overvoltage protection (AI <0..79>, AI SENSE, AI SENSE 2)

Device on ± 25 V for up to
two AI pins

Device off ± 15 V for up to
two AI pins

Input current during

overvoltage condition ± 20 mA max/AI pin

Settling Time for Multichannel Measurements

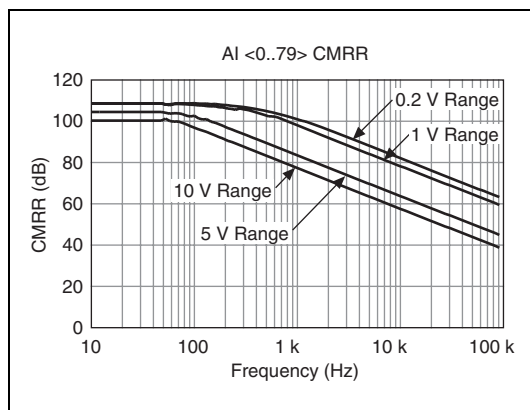
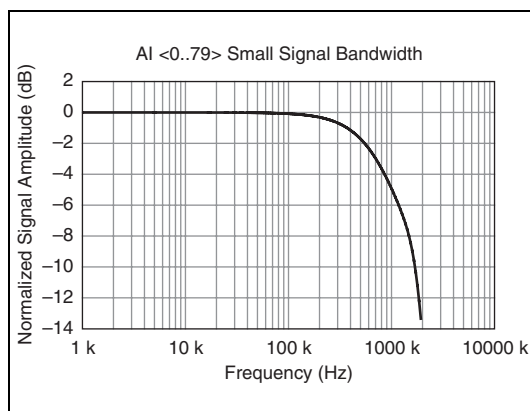
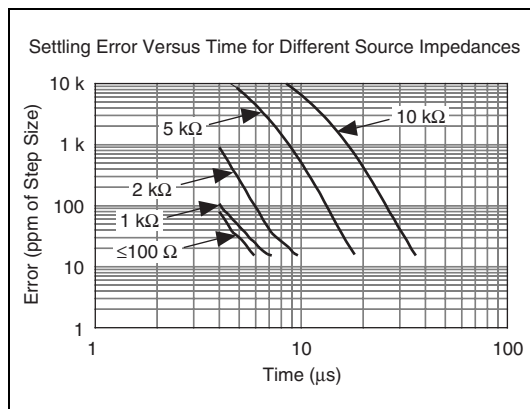
Accuracy, full scale step, all ranges

± 90 ppm of step (± 6 LSB) 4 μ s convert interval

± 30 ppm of step (± 2 LSB) 5 μ s convert interval

± 15 ppm of step (± 1 LSB) 7 μ s convert interval

Typical Performance Graphs



Analog Output

Number of channels

NI 6220/6224	0
NI 6221/6225	2
NI 6229	4

DAC resolution 16 bits

DNL ± 1 LSB

Monotonicity 16 bit guaranteed

Maximum update rate

1 channel	833 kS/s
2 channels	740 kS/s per channel
3 channels	666 kS/s per channel
4 channels	625 kS/s per channel

Timing accuracy 50 ppm of sample rate

Timing resolution 50 ns

Output range ± 10 V

Output coupling DC

Output impedance 0.2Ω

Output current drive ± 5 mA

Overdrive protection ± 25 V

Overdrive current 10 mA

Power-on state ± 20 mV¹

Power-off glitch 400 mV for 200 ms

Output FIFO size 8,191 samples shared among channels used

Data transfers

PCI/PXI devices DMA (scatter-gather), interrupts, programmed I/O

USB devices USB Signal Stream, programmed I/O

AO waveform modes:

- Non-periodic waveform
- Periodic waveform regeneration mode from onboard FIFO
- Periodic waveform regeneration from host buffer including dynamic update

¹ For all USB-6221/6229 devices, when powered on, the analog output signal is not defined until after USB configuration is complete.

Settling time, full scale step
15 ppm (1 LSB) 6 μ s
Slew rate 15 V/ μ s
Glitch energy
 Magnitude..... 100 mV
 Duration..... 2.6 μ s

Calibration (AI and AO)

Recommended warm-up time 15 minutes
Calibration interval 1 year

AI Absolute Accuracy Table

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Random Noise, σ (μ Vrms)	Absolute Accuracy at Full Scale ¹ (μ V)	Sensitivity ² (μ V)
Positive Full Scale	Negative Full Scale									
10	-10	75	25	5	20	57	76	244	3,100	97.6
5	-5	85	25	5	20	60	76	122	1,620	48.8
1	-1	95	25	5	25	79	76	30	360	12.0
0.2	-0.2	135	25	5	80	175	76	13	112	5.2

AbsoluteAccuracy = Reading · (GainError) + Range · (OffsetError) + NoiseUncertainty

GainError = ResidualAGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

OffsetError = ResidualAOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

Uncertainty = $\frac{\text{RandomNoise} \cdot 3}{\sqrt{100}}$ For a coverage factor of 3 σ and averaging 100 points

¹ Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

TempChangeFromLastExternalCal = 10 °C

TempChangeFromLastInternalCal = 1 °C

number_of_readings = 100

CoverageFactor = 3 σ

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

GainError = 75 ppm + 25 ppm · 1 + 5 ppm · 10

GainError = 150 ppm

OffsetError = 20 ppm + 57 ppm · 1 + 76 ppm

OffsetError = 153 ppm

NoiseUncertainty = $\frac{244 \mu\text{V} \cdot 3}{\sqrt{100}}$ NoiseUncertainty = 73 μ

AbsoluteAccuracy = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty AbsoluteAccuracy = 3,100 μ V

² Sensitivity is the smallest voltage change that can be detected. It is a function of noise.

Accuracies listed are valid for up to one year from the device external calibration.

AO Absolute Accuracy Table

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Absolute Accuracy at Full Scale ¹ (µV)
Positive Full Scale	Negative Full Scale							
10	-10	90	10	5	40	5	128	3,230

¹ Absolute Accuracy at full scale numbers is valid immediately following internal calibration and assumes the device is operating within 10 °C of the last external calibration. Accuracies listed are valid for up to one year from the device external calibration.

AbsoluteAccuracy = OutputValue · (GainError) + Range · (OffsetError)

GainError = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

OffsetError = ResidualOffsetError + AOffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

Digital I/O/PFI

Static Characteristics

Number of channels

NI 6220/6221 (68-pin)/6225	24 total
	8 (P0.<0..7>)
	16 (PFI <0..7>/P1, PFI <8..15>/P2)
PCI-6221 (37-pin)	10 total
	2 (P0.<0, 1>)
	8 (PFI <0..7>/P1)
NI 6224/6229	48 total
	32 (P0.<0..31>)
	16 (PFI <0..7>/P1, PFI <8..15>/P2)

Ground reference D GND

Direction control..... Each terminal
individually
programmable
as input or output

Pull-down resistor..... 50 k Ω typical,
20 k Ω minimum

Input voltage protection¹ ± 20 V on up to two pins

Waveform Characteristics (Port 0 Only)

Terminals used

NI 6220/6221 (68-pin)/	
PCI-6221 (37-pin)	Port 0 (P0.<0, 1>)
NI 6224/6229	Port 0 (P0.<0..31>)
NI 6225	Port 0 (P0.<0..7>)

Port/sample size

NI 6220/6221 (68-pin)/6225	Up to 8 bits
PCI-6221 (37-pin)	Up to 2 bits
NI 6224/6229	Up to 32 bits

Waveform generation (DO) FIFO ... 2,047 samples

Waveform acquisition (DI) FIFO 2,047 samples

DO or DI Sample Clock

frequency²..... 0 to 1 MHz

DO or DI Sample Clock source³ Any PFI, RTSI,
AI Sample or
Convert Clock,
AO Sample Clock,
Ctr *n* Internal Output,
and many other signals

PFI/Port 1/Port 2 Functionality⁴

Functionality Static digital input,
static digital output,
timing input,
timing output

Timing output sources Many AI, AO, counter,
DI, DO timing signals

Debounce filter settings 125 ns, 6.425 μ s,
2.54 ms, disable;
high and low transitions;
selectable per input

¹ Stresses beyond those listed under *Input voltage protection* may cause permanent damage to the device.

² Performance can be dependent on bus latency and volume of bus activity.

³ The digital subsystem does not have its own dedicated internal timing engine. Therefore, a sample clock must be provided from another subsystem on the device or an external source.

⁴ Port 2 is not available on PCI-6221 (37-pin) devices.

Recommended Operation Conditions

PCI/PXI devices

Level	Min	Max
Input high voltage (V_{IH})	2.2 V	5.25 V
Input low voltage (V_{IL})	0 V	0.8 V
Output high current (I_{OH})		
P0.<0..31>	—	–24 mA
PFI <0..15>/P1/P2	—	–16 mA
Output low current (I_{OL})		
P0.<0..31>	—	24 mA
PFI <0..15>/P1/P2	—	16 mA

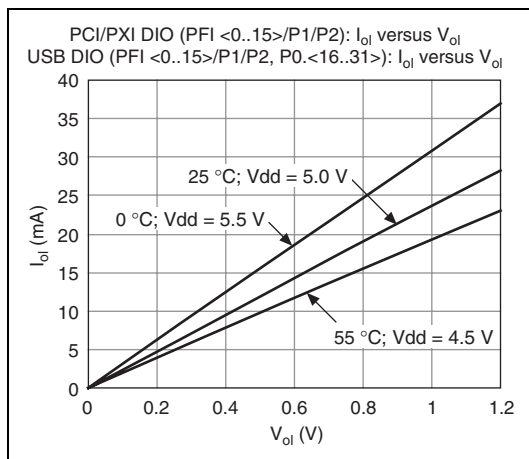
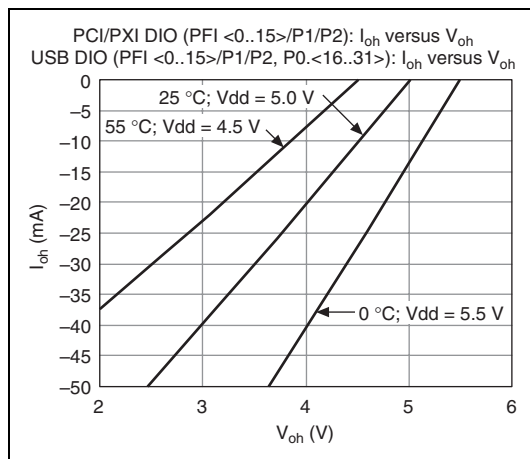
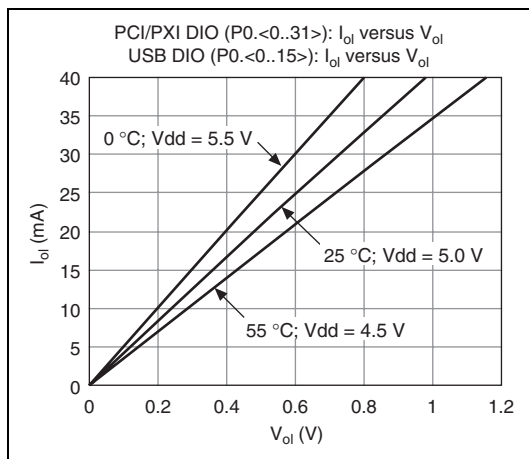
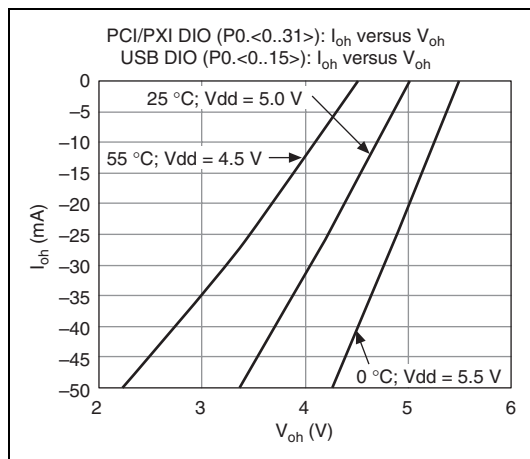
USB devices

Level	Min	Max
Input high voltage (V_{IH})	2.2 V	5.25 V
Input low voltage (V_{IL})	0 V	0.8 V
Output high current (I_{OH})		
P0.<0..15>	—	–24 mA
P0.<16..31>	—	–16 mA
PFI <0..15>/P1/P2	—	–16 mA
Output low current (I_{OL})		
P0.<0..15>	—	24 mA
P0.<16..31>	—	16 mA
PFI <0..15>/P1/P2	—	16 mA

Electrical Characteristics

Level	Min	Max
Positive-going threshold (V_{T+})	—	2.2 V
Negative-going threshold (V_{T-})	0.8 V	—
Delta VT hysteresis ($V_{T+} - V_{T-}$)	0.2 V	—
I_{IL} input low current ($V_{in} = 0$ V)	—	–10 μ A
I_{IH} input high current ($V_{in} = 5$ V)	—	250 μ A

Digital I/O Characteristics



General-Purpose Counter/Timers

Number of counter/timers	2
Resolution	32 bits
Counter measurements	Edge counting, pulse, semi-period, period, two-edge separation
Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding
Output applications	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	80 MHz, 20 MHz, 0.1 MHz
External base clock frequency	0 MHz to 20 MHz
Base clock accuracy	50 ppm
Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down
Routing options for inputs	Any PFI, RTSI, PXI_TRIG, PXI_STAR, analog trigger, many internal signals
FIFO	2 samples
Data transfers	
PCI/PXI devices	Dedicated scatter-gather DMA controller for each counter/timer; interrupts; programmed I/O
USB devices	USB Signal Stream, programmed I/O

Frequency Generator

Number of channels	1
Base clocks	10 MHz, 100 kHz
Divisors	1 to 16
Base clock accuracy	50 ppm
Output can be available on any PFI or RTSI terminal.	

Phase-Locked Loop (PLL)

Number of PLLs	1
Reference signal	PXI_STAR, PXI_CLK10, RTSI <0..7>
Output of PLL	80 MHz Timebase; other signals derived from 80 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source	Any PFI, RTSI, PXI_TRIG, PXI_STAR
Polarity	Software-selectable for most signals
Analog input function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Analog output function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Counter/timer functions	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down,
Digital waveform generation (DO) function	Sample Clock
Digital waveform acquisition (DI) function	Sample Clock

Device-To-Device Trigger Bus

PCI devices	RTSI <0..7> ¹
PXI devices	PXI_TRIG <0..7>, PXI_STAR
USB devices	None
Output selections	10 MHz Clock; frequency generator output; many internal signals
Debounce filter settings	125 ns, 6.425 μ s, 2.54 ms, disabled; high and low transitions; selectable per input

Bus Interface

PCI/PXI devices	3.3 V or 5 V signal environment
USB devices	USB 2.0 Hi-Speed or full-speed ²
DMA channels (PCI/PXI devices)	6, analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1
USB Signal Stream (USB devices)	4, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1

All PXI-622x devices support one of the following features:

- May be installed in PXI Express hybrid slots
- Or, may be used to control SCXI in PXI/SCXI combo chassis

Table 1. PXI and PXI Express Chassis

Device	Part Number	SCXI Control in PXI/SCXI Combo Chassis	PXI Express Hybrid Slot Compatible
PXI-6220	191332B-04	No	Yes
PXI-6221	191332B-03	No	Yes
	191332B-13	Yes	No
PXI-6224	191332B-02	No	Yes
PXI-6225	192227A-01	No	Yes
PXI-6229	191332B-01	No	Yes
	191332B-11	Yes	No
Earlier versions of PXI-6220, PXI-6221, PXI-6224, and PXI-6229	191332A-0x	Yes	No

Power Requirements

Current draw from bus during no-load condition³

+5 V	0.02 A ⁴
+3.3 V	0.25 A ⁴
+12 V	0.15 A

Current draw from bus during AI and AO overvoltage condition³

+5 V	0.02 A ⁴
+3.3 V	0.25 A ⁴
+12 V	0.25 A

¹ In other sections of this document, *RTSI* refers to *RTSI* <0..7> for PCI devices or *PXI_TRIG* <0..7> for PXI devices.

² If you are using a USB M Series device in full-speed mode, device performance will be lower and you will not be able to achieve maximum sampling/update rates.

³ Does not include P0/PFI/P1/P2 and +5 V terminals.

⁴ PXI-6221 (37-pin) devices do not use +3.3 V from the bus. The 3.3 V current draw, shown in the *Power Requirements* section, comes from the +5 V instead.



Caution USB-622x devices must be powered with NI offered AC adapter or a National Electric Code (NEC) Class 2 DC source that meets the power requirements for the device and has appropriate safety certification marks for country of use.

USB power supply requirements 11 to 30 VDC, 20 W

Power Limits



Caution Exceeding the power limits may cause unpredictable behavior by the device and/or PC/chassis.

PCI devices

+5 V terminal (connector 0) 1 A max¹
+5 V terminal (connector 1) 1 A max¹

PXI devices

+5 V terminal (connector 0) 1 A max¹
+5 V terminal (connector 1) 1 A max¹
P0/PFI/P1/P2 and +5 V
terminals combined 2 A max

USB devices

+5 V terminal 1 A max¹
P0/PFI/P1/P2 and +5 V
terminals combined 2 A max
Power supply fuse 2 A, 250 V

Physical Requirements

Printed circuit board dimensions

PCI-6220/6221/6224/
6225/6229 9.7 cm × 15.5 cm
(3.8 in. × 6.1 in.)

PXI-6220/6221/6224/
6225/6229 Standard 3U PXI

Enclosure dimensions (includes connectors)

USB-6221/6229 26.67 × 17.09 × 4.45 cm
(10.5 × 6.73 × 1.75 in.)

Weight

PCI-6220 91 g (3.2 oz)
PCI-6221 (68-pin) 92 g (3.2 oz)
PCI-6221 (37-pin) 95 g (3.3 oz)
PCI-6224 99 g (3.5 oz)
PCI-6225 103 g (3.6 oz)
PCI-6229 101 g (3.5 oz)

PXI-6220 158 g (5.5 oz)
PXI-6221 162 g (5.7 oz)
PXI-6224 170 g (5.9 oz)
PXI-6225 174 g (6.1 oz)
PXI-6229 171 g (6.0 oz)
USB-6221 1.2 kg (2 lb 10 oz)
USB-6229 1.24 kg (2 lb 11 oz)
USB-6221 OEM 86 g (3.0 oz)
USB-6229 OEM 107 g (3.8 oz)

I/O connector

PCI/PXI-6220/6221 (68-pin) 1 68-pin VHDCI
PCI/PXI-6224/6225/6229 2 68-pin VHDCI
PCI-6221 (37-pin) 1 37-pin D-SUB
USB-6221 64 screw terminals
USB-6229 128 screw terminals

Maximum Working Voltage²

NI 6220/6221/6224/6225/6229

Channel to earth 11 V,
Measurement Category I



Caution Do *not* use for measurements within Categories II, III, or IV.

Environmental

Operating temperature

PCI/PXI devices 0 to 55 °C
USB devices 0 to 45 °C

Storage temperature -20 to 70 °C

Humidity 10 to 90% RH,
noncondensing

Maximum altitude 2,000 m

Pollution Degree

(indoor use only) 2

Shock and Vibration (PXI Devices Only)

Operational shock 30 g peak, half-sine,
11 ms pulse
(Tested in accordance
with IEC-60068-2-27.
Test profile developed
in accordance with
MIL-PRF-28800F.)

¹ Has a self-resetting fuse that opens when current exceeds this specification.

² *Maximum working voltage* refers to the signal voltage plus the common-mode voltage.

Random vibration

Operating	5 to 500 Hz, 0.3 g _{rms}
Nonoperating	5 to 500 Hz, 2.4 g _{rms} (Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label or visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 EMC requirements; Minimum Immunity
- EN 55011 Emissions; Group 1, Class A
- CE, C-Tick, ICES, and FCC Part 15 Emissions; Class A



Note For EMC compliance, operate this device according to product documentation.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 73/23/EEC; Low-Voltage Directive (safety)
- 89/336/EEC; Electromagnetic Compatibility Directive (EMC)



Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of their life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit ni.com/environment/weee.htm.

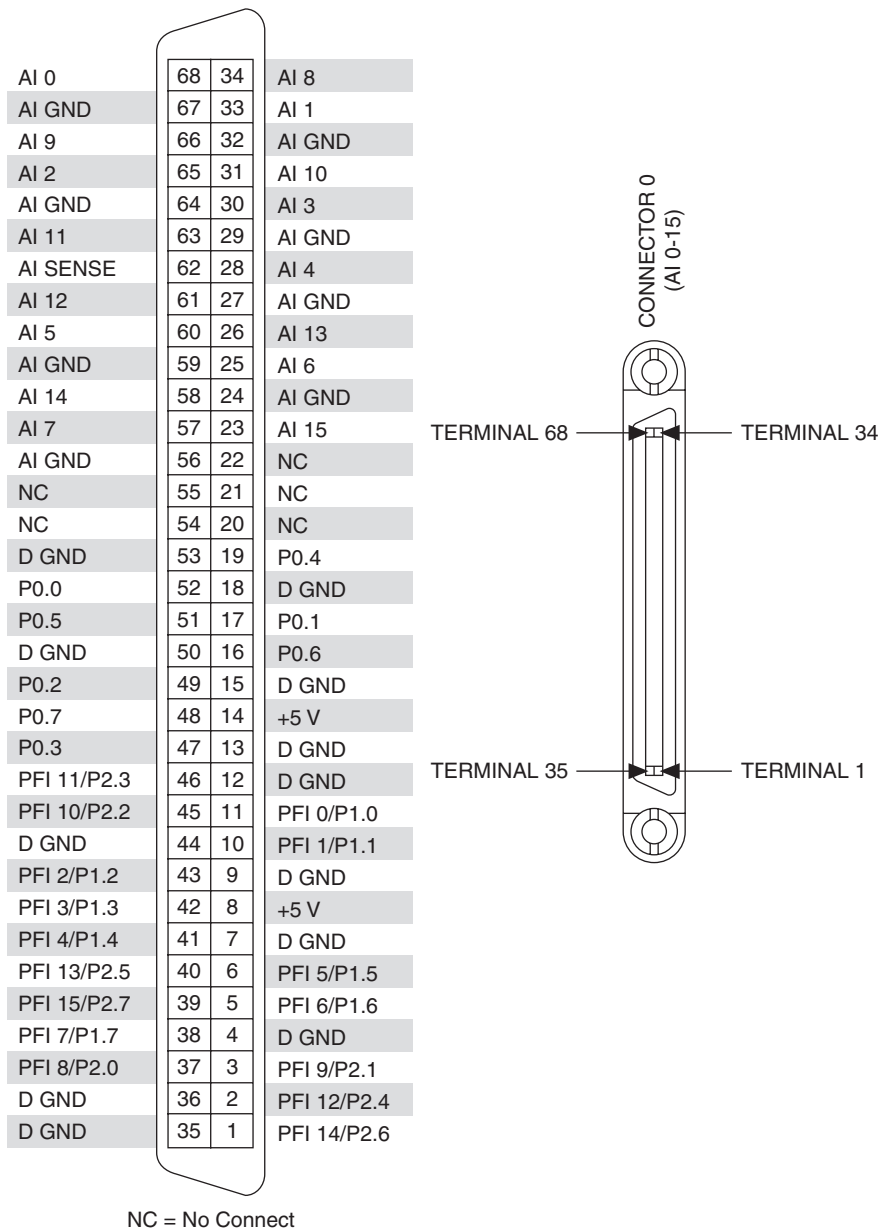


Figure 1. PCI/PXI-6220 Pinout

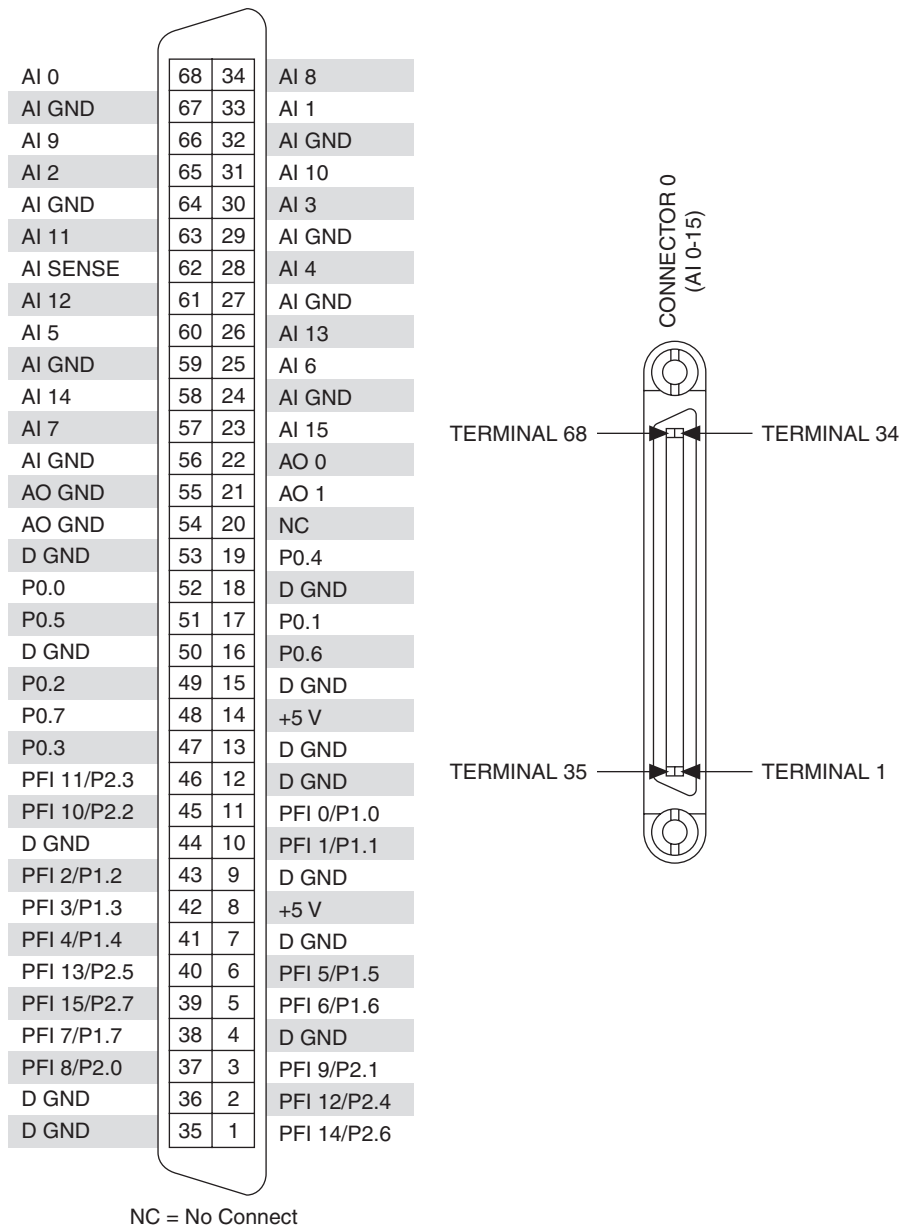


Figure 2. PCI/PXI-6221 (68-Pin) Pinout

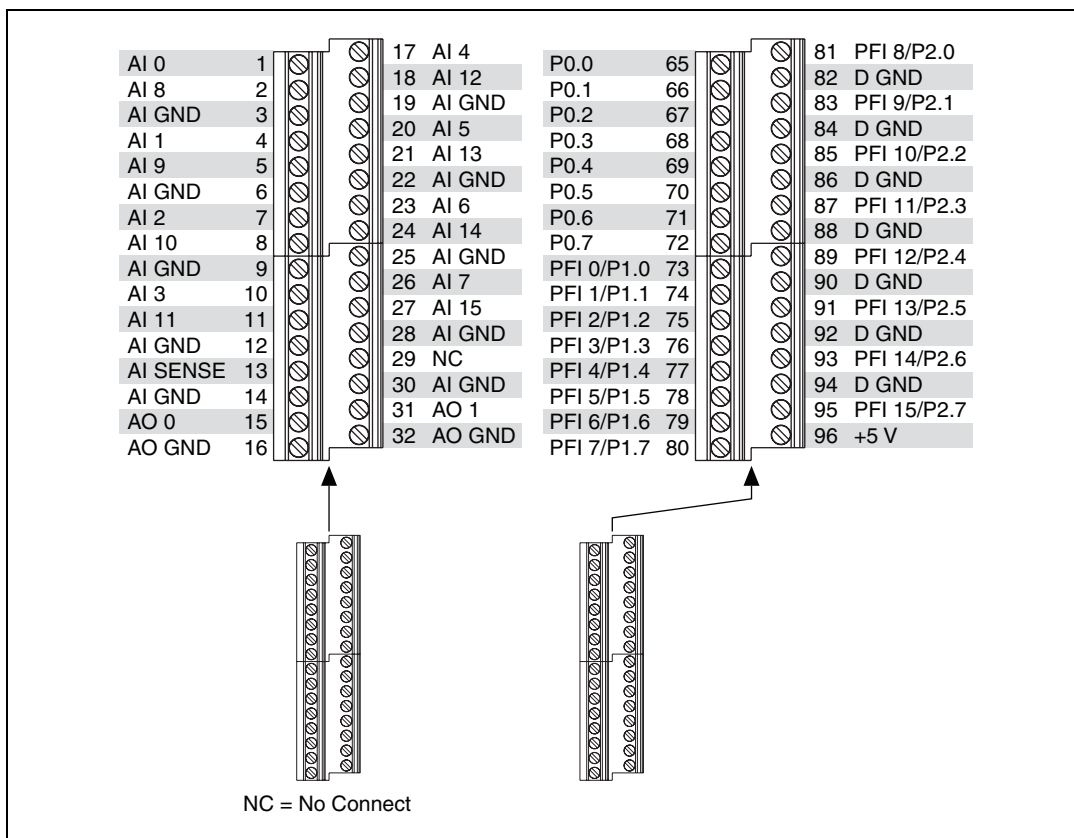
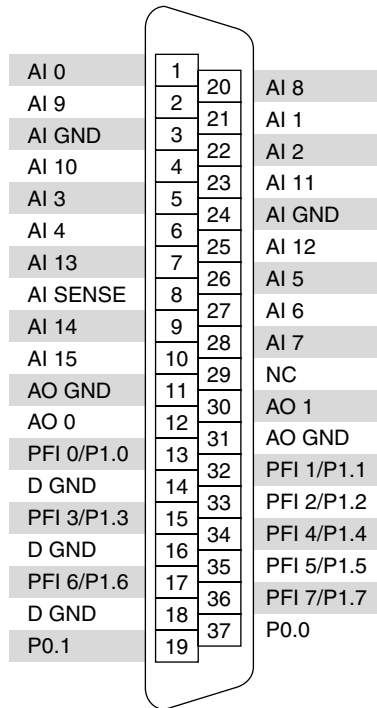


Figure 3. USB-6221 Pinout



NC = No Connect

Figure 4. PCI-6221 (37-Pin) Pinout

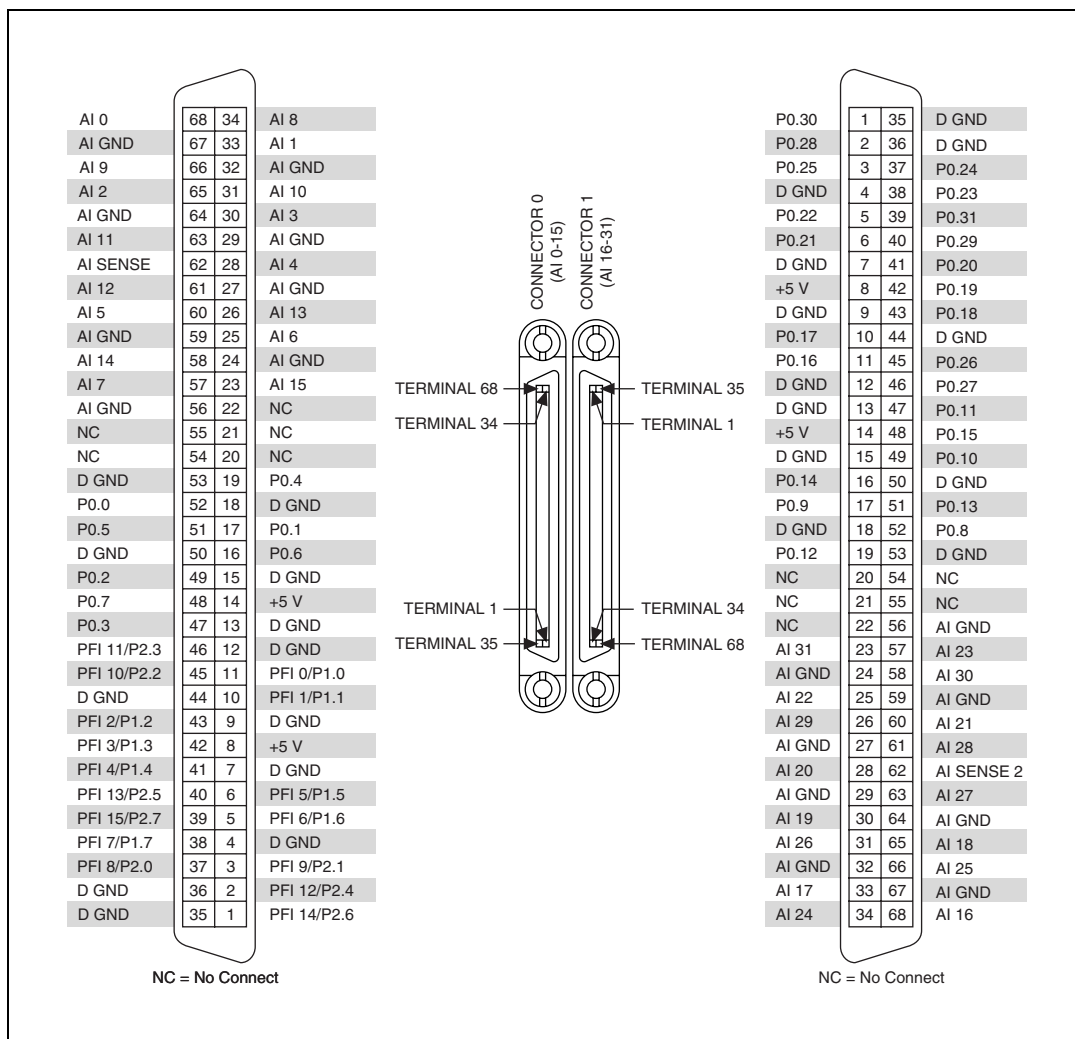


Figure 5. PCI/PXI-6224 Pinout

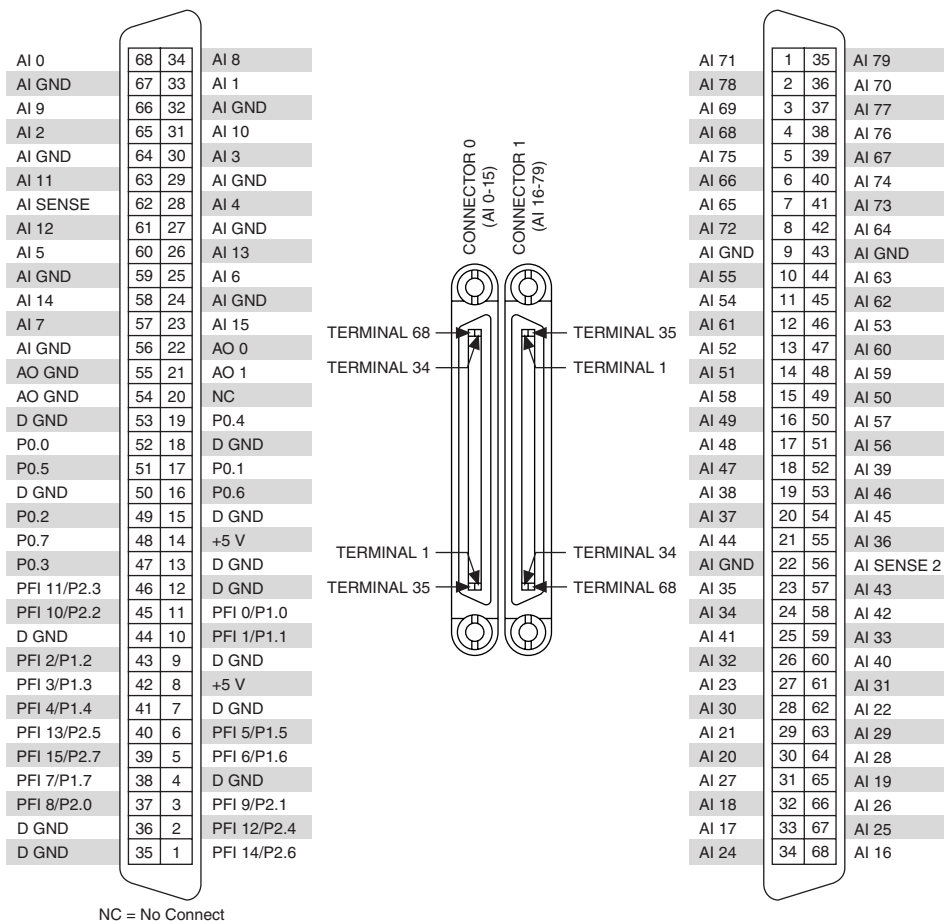


Figure 6. PCI/PXI-6225 Pinout

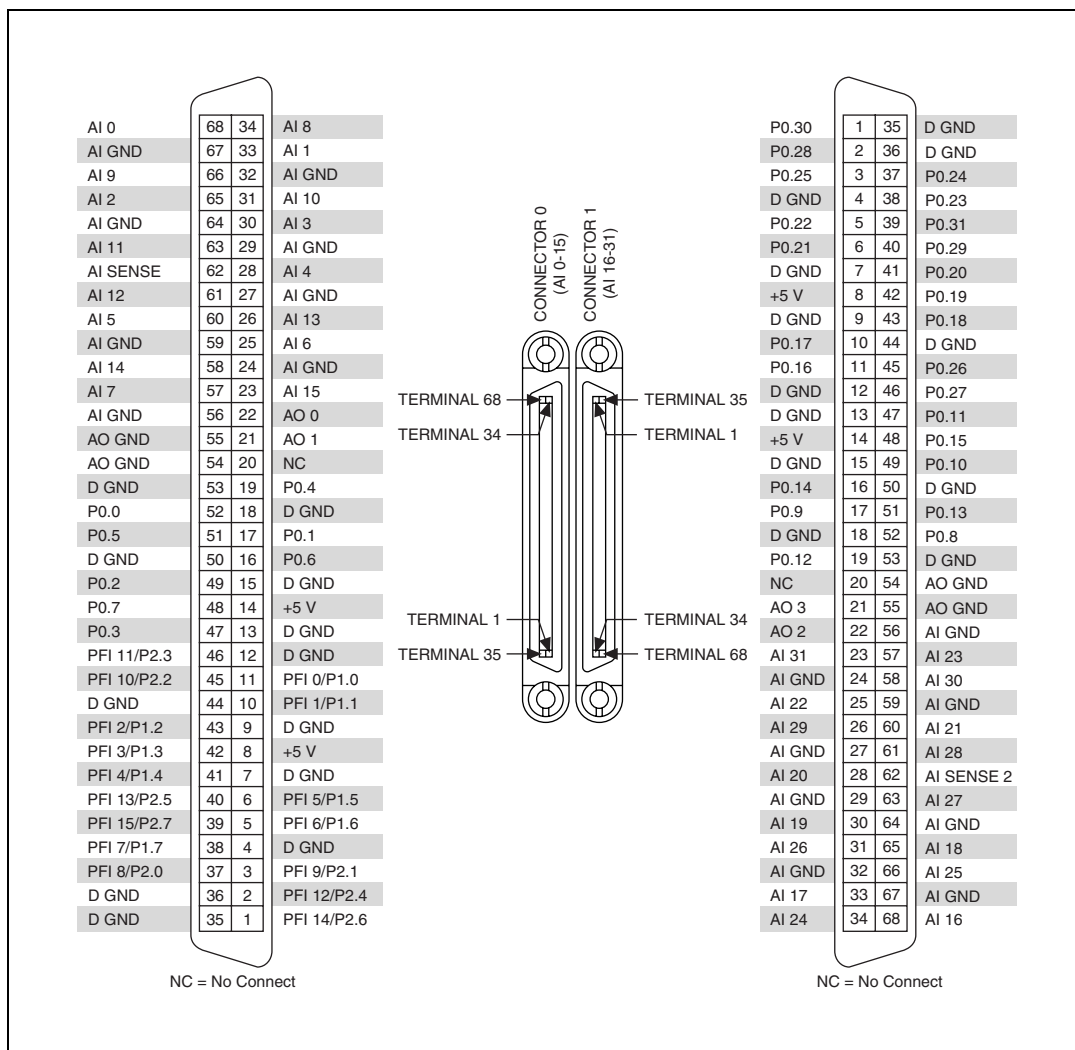


Figure 7. PCI/PXI-6229 Pinout

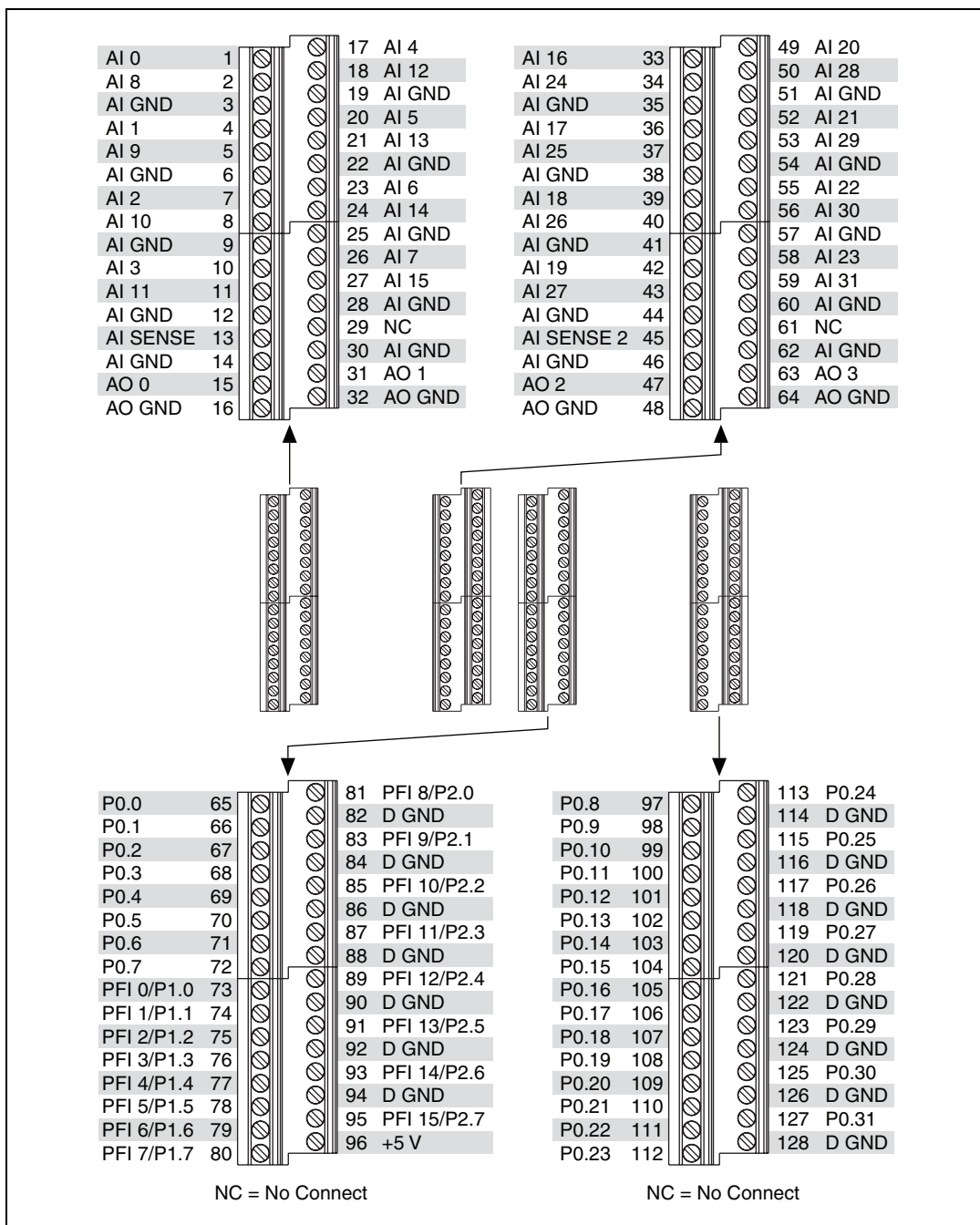


Figure 8. USB-6229 Pinout

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