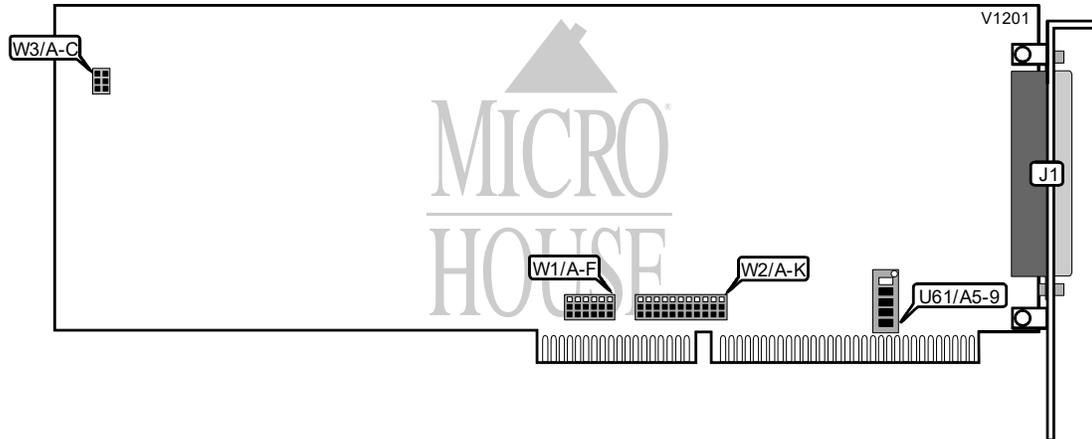


NATIONAL INSTRUMENTS AT-DIO-32F

Card Type Parallel & Digital I/O card
Chipset Controller Unidentified
I/O Options 32 lines of digital I/O (four 8-bit ports)
Maximum DRAM N/A



CONNECTIONS	
Purpose	Location
50-pin I/O interface connector	J1

BASE I/O ADDRESS SELECTION					
Address	U61/A5	U61/A6	U61/A7	U61/A8	U61/A9
240h	On	Off	On	On	Off
000h	On	On	On	On	On
020h	Off	On	On	On	On
040h	On	Off	On	On	On
060h	Off	Off	On	On	On
080h	On	On	Off	On	On
360h	Off	Off	On	Off	Off
380h	On	On	Off	Off	Off
3A0h	Off	On	Off	Off	Off
3C0h	On	Off	Off	Off	Off
3E0h	Off	Off	Off	Off	Off

Note: A total of 255 base address settings are available. The switches are a binary representation of the decimal memory addresses. Switch A9 is the Most Significant Bit and switch A5 is the Least Significant Bit. The switches have the following decimal values: switch A9=512, A8=256, A7=128, A6=64, A5=32. Turn off the switches and add the values of the switches that are off to obtain the correct memory address. (Off=1, On=0)

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NATIONAL INSTRUMENTS

AT-DIO-32F

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DMA CHANNEL SELECTION (GROUP 1)						
DMA	W1/A	W1/B	W1/C	W1/D	W1/E	W1/F
í 5	Pins 1 & 2	Pins 1 & 2	Open	Open	Open	Open
6	Open	Open	Pins 1 & 2	Pins 1 & 2	Open	Open
7	Open	Open	Open	Open	Pins 1 & 2	Pins 1 & 2

Note: Pins designated are in the closed position.

DMA CHANNEL SELECTION (GROUP 2)						
DMA	W1/A	W1/B	W1/C	W1/D	W1/E	W1/F
í 6	Open	Open	Pins 2 & 3	Pins 2 & 3	Open	Open
5	Pins 2 & 3	Pins 2 & 3	Open	Open	Open	Open
7	Open	Open	Open	Open	Pins 2 & 3	Pins 2 & 3

Note: Pins designated are in the closed position.

INTERRUPT SELECTION (INTR 1)											
IRQ	W2/A	W2/B	W2/C	W2/D	W2/E	W2/F	W2/G	W2/H	W2/I	W2/J	W2/K
í 11	Open	Open	Open	Open	Open	Open	Open	1 & 2	Open	Open	Open
2/9	Open	Open	Open	Open	Open	Open	1 & 2	Open	Open	Open	Open
3	1 & 2	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open
4	Open	1 & 2	Open	Open	Open	Open	Open	Open	Open	Open	Open
5	Open	Open	1 & 2	Open	Open	Open	Open	Open	Open	Open	Open
6	Open	Open	Open	1 & 2	Open	Open	Open	Open	Open	Open	Open
7	Open	Open	Open	Open	1 & 2	Open	Open	Open	Open	Open	Open
10	Open	Open	Open	Open	Open	Open	1 & 2	Open	Open	Open	Open
12	Open	Open	Open	Open	Open	Open	Open	Open	1 & 2	Open	Open
14	Open	Open	Open	Open	Open	Open	Open	Open	Open	1 & 2	Open
15	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open	1 & 2

Note: Pins designated are in the closed position.

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NATIONAL INSTRUMENTS

AT-DIO-32F

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INTERRUPT SELECTION (INTR 2)											
IRQ	W2/A	W2/B	W2/C	W2/D	W2/E	W2/F	W2/G	W2/H	W2/I	W2/J	W2/K
12	Open	2 & 3	Open	Open							
2/9	Open	Open	Open	Open	Open	2 & 3	Open	Open	Open	Open	Open
3	2 & 3	Open									
4	Open	2 & 3	Open								
5	Open	Open	2 & 3	Open							
6	Open	Open	Open	2 & 3	Open						
7	Open	Open	Open	Open	2 & 3	Open	Open	Open	Open	Open	Open
10	Open	Open	Open	Open	Open	Open	2 & 3	Open	Open	Open	Open
11	Open	2 & 3	Open	Open	Open						
14	Open	2 & 3	Open								
15	Open	2 & 3									

Note: Pins designated are in the closed position.

RTSI BUS CLOCK CONFIGURATION			
Setting	W3/A	W3/B	W3/C
Use local oscillator board signal	Closed	Closed	Open
Receive the RTSI bus signal	Closed	Open	Closed
Drive RTSI bus & board/OSC	Open	Closed	Closed