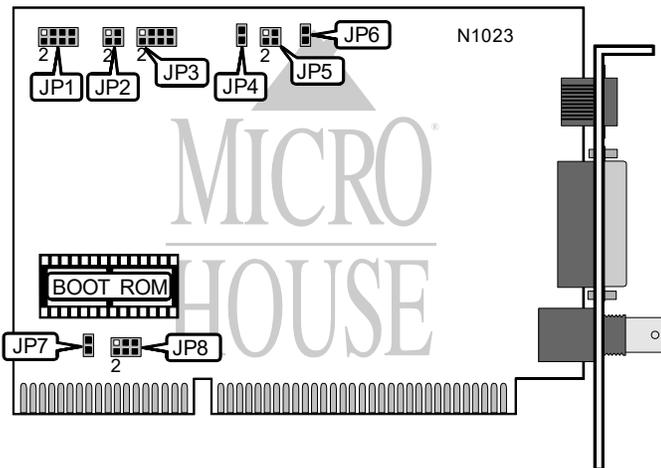


Chapter 5: Jumper Settings
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NIC Type Ethernet
Transfer Rate 10Mbps
Data Bus 16-bit ISA
Topology Linear Bus/Star
Wiring Type Unshielded twisted pair
 AUI Transceiver via DB-15 port
 RG-58A/U 50ohm coaxial
Boot ROM Available



CABLE TYPE SELECTION		
Cable Type	JP2 pins 1 & 2	JP2 pins 3 & 4
Normal unshielded twisted pair	Open	Open
Reduced squelch unshielded twisted pair	Closed	Closed
AUI Transceiver via DB-15 port	Closed	Open
RG-58A/U 50ohm coaxial	Open	Closed

BASE I/O ADDRESS SELECTION			
Address	JP8 pins 1 & 2	JP8 pins 3 & 4	JP8 pins 5 & 6
Software	Open	Open	Open
02C0h	Closed	Open	Open
0240h	Open	Closed	Open
0280h	Open	Closed	Closed
0300h	Open	Open	Open
0320h	Closed	Open	Closed
0340h	Closed	Closed	Open
0360h	Closed	Closed	Closed

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INTERRUPT SELECTION				
IRQ	JP3 pins 1 & 2	JP3 pins 3 & 4	JP3 pins 5 & 6	JP3 pins 7 & 8
IRQ3	Closed	Open	Open	Open
IRQ4	Closed	Open	Open	Closed
IRQ5	Closed	Open	Closed	Open
IRQ9	Closed	Open	Closed	Closed
IRQ10	Closed	Closed	Open	Open
IRQ11	Closed	Closed	Open	Closed
IRQ12	Closed	Closed	Closed	Open
IRQ15	Closed	Closed	Closed	Closed

LINK PULSE CONFIGURATION	
Setting	JP4
Link pulse enabled	Open
Link pulse disabled	Closed

COMPATIBILITY CONFIGURATION		
Setting	JP5 pins 1 & 2	JP5 pins 3 & 4
Channel ready signal generated after command signal	Open	Open
Channel ready signal generated after bus address latch	Closed	Open
I/O 16-bit signal generated after I/O read or I/O write signals	Open	Closed
I/O 16-bit only on address decode	Open	Open

SOFTWARE/HARDWARE CONFIGURATION	
Setting	JP6
Software configured	Closed
Hardware configured	Open

BUFFERING MODE CONFIGURATION	
Setting	JP7
Memory mapped	Open
I/O mapped	Closed

MISCELLANEOUSE TECHNICAL NOTE
Note: The JP1 Boot ROM Base address configuration is not available from the manufacturer.