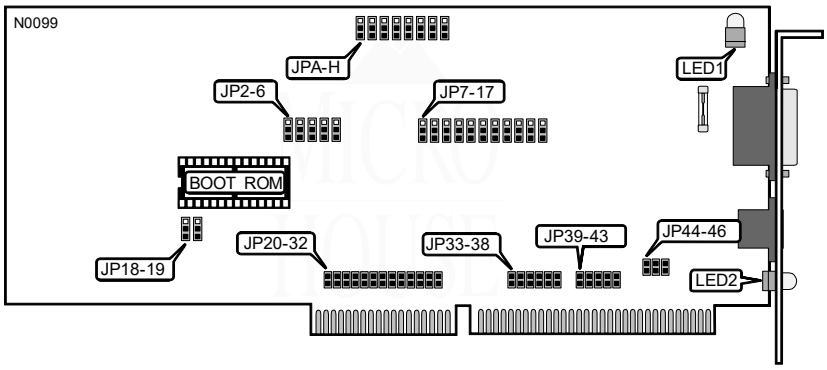
TIARA COMPUTER SYSTEMS, INC.
LanCard/E * AT TP

NIC Type	Ethernet
Transfer Rate	10Mbps
Data Bus	16-bit ISA
Topology	Linear Bus
Wiring Type	Shielded twisted pair Unshielded twisted pair AUI transceiver via DB-15 port
Boot ROM	Available



CABLE TYPE	
Jumper	JPA - JPH
Shielded/Unshielded twisted pair	Pins 1 & 2 closed
AUI transceiver via DB-15 port	Pins 2 & 3 closed

DIAGNOSTIC LED(S)		
LED	Status	Condition
LED1	On	Power on
LED1	Off	Card is not receiving power, the fuse is blown, or cable type is twisted pair.
LED2	On	Twisted pair network connection is good
LED2	Off	Twisted pair network connection is broken
Note: LED2 will only function is the cable type is twisted pair.		

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I/O BASE ADDRESS					
Address	JP2	JP3	JP4	JP5	JP6
300h	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2
000h	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3
020h	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3
040h	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3
060h	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3
080h	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3
0A0h	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3
0C0h	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3
0E0h	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3
100h	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3
120h	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3
140h	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3
160h	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3
180h	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3
1A0h	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3
1C0h	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3
1E0h	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3
200h	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2
220h	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2
240h	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2
260h	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2
280h	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2
2A0h	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2
2C0h	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2
2E0h	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2
320h	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2
340h	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2
360h	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2
380h	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2
3A0h	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2
3C0h	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2
3E0h	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2
Note: Pins designated should be in the closed position.					

BOOT ROM	
Setting	JP7
Disabled	Pins 2 & 3 closed
Enabled	Pins 1 & 2 closed

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BASE MEMORY ADDRESS - FIRST DIGIT				
Address Segment	JP8	JP9	JP10	JP11
0h	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
1h	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 1 & 2 closed
2h	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
3h	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 1 & 2 closed
4h	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
5h	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 1 & 2 closed
6h	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
7h	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 1 & 2 closed
8h	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
9h	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 1 & 2 closed
Ah	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
Bh	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 1 & 2 closed
Ch	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
Dh	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 1 & 2 closed
Eh	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
Fh	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 1 & 2 closed

Note: The Address Segment is the first digit in the Base Memory Address. Refer to the next table for the remaining three digits in the address. Note that not all configurable addresses are valid on all systems.

BASE MEMORY ADDRESS - LAST THREE DIGITS				
Address	ROM Size	JP11	JP12	JP30
x000h	8K x 8	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
x200h	8K x 8	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 1 & 2 closed
x400h	8K x 8	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
x600h	8K x 8	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 1 & 2 closed
x800h	8K x 8	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
xA00h	8K x 8	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 1 & 2 closed
xC00h	8K x 8	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
xE00h	8K x 8	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 1 & 2 closed
x000h	16K x 8	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
x400h	16K x 8	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
x800h	16K x 8	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
xC00h	16K x 8	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
x000h	32K x 8	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
x800h	32K x 8	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
x000h	64K x 8	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed

Note: Place the three digit address given here behind the single digit given in the previous table to get the complete Base Memory Address.

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BOOT ROM SIZE					
Size	JP15	JP16	JP17	JP18	JP19
í2764 (8KB)	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3
27128 (16KB)	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2
27256 (32KB)	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3
27512 (64KB)	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2
Note: Pins designated should be in the closed position.					

DMA REQUEST CHANNEL								
Channel	JP20	JP22	JP24	JP26	JP39	JP41	JP44	JP46
íDisabled	Open	Open	Open	Open	Open	Open	Open	Closed
DRQ0	Open	Open	Open	Closed	Open	Open	Open	Open
DRQ1	Open	Open	Open	Open	Closed	Open	Open	Open
DRQ2	Open	Open	Open	Open	Open	Open	Closed	Open
DRQ3	Open	Open	Open	Open	Open	Closed	Open	Open
DRQ5	Open	Open	Closed	Open	Open	Open	Open	Open
DRQ6	Open	Closed	Open	Open	Open	Open	Open	Open
DRQ7	Closed	Open	Open	Open	Open	Open	Open	Open

DMA ACKNOWLEDGE CHANNEL								
Channel	JP21	JP23	JP25	JP27	JP33	JP40	JP42	JP43
íDisabled	Open	Open	Open	Open	Open	Open	Open	Closed
DACK0	Open	Open	Open	Closed	Open	Open	Open	Open
DACK1	Open	Open	Open	Open	Closed	Open	Open	Open
DACK2	Open	Open	Open	Open	Open	Open	Closed	Open
DACK3	Open	Open	Open	Open	Open	Closed	Open	Open
DACK5	Open	Open	Closed	Open	Open	Open	Open	Open
DACK6	Open	Closed	Open	Open	Open	Open	Open	Open
DACK7	Closed	Open	Open	Open	Open	Open	Open	Open
Note: DMA acknowledge channel must be set to the same number as the DMA request.								

INTERRUPT REQUEST											
IRQ	JP28	JP29	JP30	JP31	JP32	JP34	JP35	JP36	JP37	JP38	JP45
í3	Open	Open	Open	Open	Open	Closed	Open	Open	Open	Open	Open
2	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open	Closed
4	Open	Open	Open	Open	Open	Open	Closed	Open	Open	Open	Open
5	Open	Open	Open	Open	Open	Open	Open	Closed	Open	Open	Open
6	Open	Open	Open	Open	Open	Open	Open	Open	Closed	Open	Open
7	Open	Open	Open	Open	Open	Open	Open	Open	Open	Closed	Open
10	Open	Open	Open	Open	Closed	Open	Open	Open	Open	Open	Open
11	Open	Open	Open	Closed	Open	Open	Open	Open	Open	Open	Open

12	Open	Open	Closed	Open	Open	Open	Open	Open	Open	Open	Open
14	Closed	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open
15	Open	Closed	Open	Open	Open	Open	Open	Open	Open	Open	Open