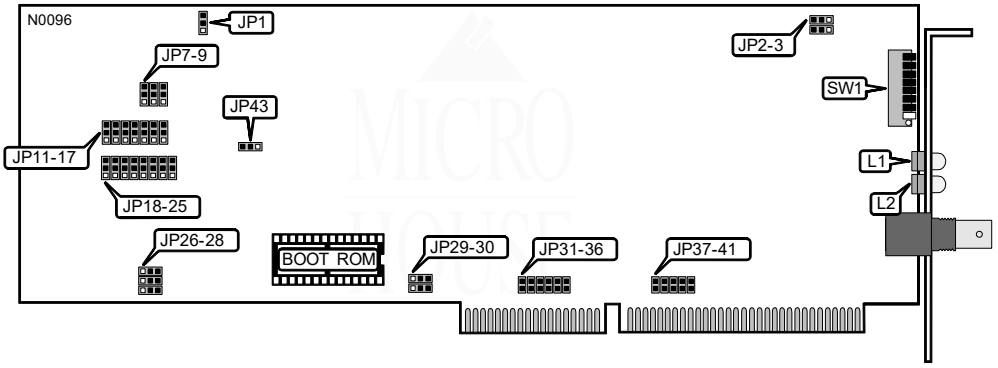
TIARA COMPUTER SYSTEMS, INC.
LanCard/A-PC16 & LanCard/A-PC16 HiZ

NIC Type ARCnet
Transfer Rate 2.5Mbps
Data Bus 16-bit ISA
Topology Star
Wiring Type RG-62A/U 93ohm coaxial (A-PC16 and A-PC16 HiZ)
RG-58A/U 50ohm coaxial (A-PC16 Hiz)
Boot ROM Available



NODE ADDRESS								
Node	SW1/1	SW1/2	SW1/3	SW1/4	SW1/5	SW1/6	SW1/7	SW1/8
0	-	-	-	-	-	-	-	-
1	On	Off	Off	Off	Off	Off	Off	Off
2	Off	On	Off	Off	Off	Off	Off	Off
3	On	On	Off	Off	Off	Off	Off	Off
4	Off	Off	On	Off	Off	Off	Off	Off
251	On	On	Off	On	On	On	On	On
252	Off	Off	On	On	On	On	On	On
253	On	Off	On	On	On	On	On	On
254	Off	On	On	On	On	On	On	On
255	On	On	On	On	On	On	On	On

Note: Node address 0 is used for messaging between nodes and must not be used.
A total of 255 node address settings are available. The switches are a binary representation of the decimal node addresses. Switch 1 is the Least Significant Bit and switch 8 is the Most Significant Bit. The switches have the following decimal values: switch 1=1, 2=2, 3=4, 4=8, 5=16, 6=32 7=64, 8=128. Turn on the switches and add the values of the on switches to obtain the correct node address. (On=1, off=0)

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EXTENDED TIMEOUT CONFIGURATION				
Distance	Response Time	Reconfiguration	JP2	JP3
4.8 miles	74.7µs	840ms	Pins 1 & 2 closed	Pins 1 & 2 closed
21.0 miles	263.4µs	1680ms	Pins 1 & 2 closed	Pins 2 & 3 closed
42.5 miles	561.8µs	1680ms	Pins 2 & 3 closed	Pins 1 & 2 closed
85.6 miles	1118.6µs	1680ms	Pins 2 & 3 closed	Pins 2 & 3 closed
Note: The distance given is the maximum distance between the two furthest nodes on the network.				

RIM BUFFER CONFIGURATION			
Address	JP7	JP8	JP9
íD000-D1FFh	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
COOO-DFFFh	N/A	N/A	Pins 1 & 2 closed
D400-D5FFh	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
D800-D9FF	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
DC00-DEFF	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
Note: When JP9 has pins 1 & 2 closed, the buffer size is 128KB, rather than 8KB. Use this setting when experiencing difficulty with fast AT-class machines.			

I/O BASE ADDRESS					
Address	JP18	JP19	JP20	JP21	JP22
í0280h	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3
02Aoh	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3	Pins 1 & 2	Pins 2 & 3
02E0h	Pins 2 & 3	Pins 1 & 2	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3
0300h	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2
0330h	Pins 1 & 2	Pins 1 & 2	Pins 2 & 3	Pins 2 & 3	Pins 1 & 2
Note: Pins designated should be in the closed position.					

INTERRUPT REQUEST											
IRQ	JP31	JP32	JP33	JP34	JP35	JP36	JP37	JP38	JP39	JP40	JP41
í2	Open	Open	Open	Open	Open	Closed	Open	Open	Open	Open	Open
3	Open	Open	Open	Open	Open	Open	Closed	Open	Open	Open	Open
4	Open	Open	Open	Open	Open	Open	Open	Closed	Open	Open	Open
5	Open	Open	Open	Open	Open	Open	Open	Open	Closed	Open	Open
6	Open	Open	Open	Open	Open	Open	Open	Open	Open	Closed	Open
7	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open	Closed
10	Open	Open	Open	Open	Closed	Open	Open	Open	Open	Open	Open
11	Open	Open	Open	Closed	Open	Open	Open	Open	Open	Open	Open
12	Open	Open	Closed	Open	Open	Open	Open	Open	Open	Open	Open

14	Closed	Open	Open	Open	Open	Open	Open	Open	Open	Open	Open
15	Open	Closed	Open	Open	Open	Open	Open	Open	Open	Open	Open

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BASE MEMORY ADDRESS - LAST THREE DIGITS									
Address	ROM	JP11	JP12	JP13	JP26	JP27	JP28	JP29	JP30
x000h-x1FFh	8K x 8	Pins 2&3	Pins 2&3	Pins 2&3	Pins 1&2	Pins 1&2	Pins 1&2	Pins 2&3	Pins 2&3
x200h-x3FFh	8K x 8	Pins 1&2	Pins 2&3	Pins 2&3	Pins 1&2	Pins 1&2	Pins 1&2	Pins 2&3	Pins 2&3
x400h-x5FFh	8K x 8	Pins 2&3	Pins 1&2	Pins 2&3	Pins 1&2	Pins 1&2	Pins 1&2	Pins 2&3	Pins 2&3
x600h-x7FFh	8K x 8	Pins 1&2	Pins 1&2	Pins 2&3	Pins 1&2	Pins 1&2	Pins 1&2	Pins 2&3	Pins 2&3
x800h-x9FFh	8K x 8	Pins 2&3	Pins 2&3	Pins 1&2	Pins 1&2	Pins 1&2	Pins 1&2	Pins 2&3	Pins 2&3
xA00h-xBFFh	8K x 8	Pins 1&2	Pins 2&3	Pins 1&2	Pins 1&2	Pins 1&2	Pins 1&2	Pins 2&3	Pins 2&3
xC00h-xDFFh	8K x 8	Pins 2&3	Pins 1&2	Pins 1&2	Pins 1&2	Pins 1&2	Pins 1&2	Pins 2&3	Pins 2&3
xE00h-xFFFh	8K x 8	Pins 1&2	Pins 1&2	Pins 1&2	Pins 1&2	Pins 1&2	Pins 1&2	Pins 2&3	Pins 2&3
x000h-x3FFh	16K x 8	Pins 2&3	Pins 2&3	Pins 2&3	Pins 2&3	Pins 1&2	Pins 1&2	Pins 2&3	Pins 1&2
x400h-x7FFh	16K x 8	Pins 2&3	Pins 1&2	Pins 2&3	Pins 2&3	Pins 1&2	Pins 1&2	Pins 2&3	Pins 1&2
x800h-xBFFh	16K x 8	Pins 2&3	Pins 2&3	Pins 1&2	Pins 2&3	Pins 1&2	Pins 1&2	Pins 2&3	Pins 1&2
xC00h-xFFFh	16K x 8	Pins 2&3	Pins 1&2	Pins 1&2	Pins 2&3	Pins 1&2	Pins 1&2	Pins 2&3	Pins 1&2
x000h-x7FFh	32K x 8	Pins 2&3	Pins 2&3	Pins 2&3	Pins 2&3	Pins 2&3	Pins 1&2	Pins 1&2	Pins 2&3
x800h-xFFFh	32K x 8	Pins 2&3	Pins 2&3	Pins 1&2	Pins 2&3	Pins 2&3	Pins 1&2	Pins 1&2	Pins 2&3
x000h-xFFFh	64K x 8	Pins 2&3	Pins 2&3	Pins 2&3	Pins 2&3	Pins 2&3	Pins 2&3	Pins 1&2	Pins 1&2

Note: Pins designated should be in the closed position.

Note: Place the three digit address given here behind the single digit given in the following table to get the complete base memory address.

BASE MEMORY ADDRESS - FIRST DIGIT				
Address Segment	JP14	JP15	JP16	JP17
0h	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
1h	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
2h	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
3h	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed
4h	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
5h	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
6h	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
7h	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 2 & 3 closed
8h	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 1 & 2 closed
9h	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 1 & 2 closed
Ah	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 1 & 2 closed
Bh	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 1 & 2 closed
Ch	Pins 2 & 3 closed	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 1 & 2 closed
Dh	Pins 1 & 2 closed	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 1 & 2 closed
Eh	Pins 2 & 3 closed	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 1 & 2 closed
Fh	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 1 & 2 closed	Pins 1 & 2 closed

Note: The Address Segment is the first digit in the Base Memory Address. Refer to the previous table for the remaining three digits in the address.

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BOOT ROM	
Setting	JP43
íDisabled	Pins 2 & 3 closed
Enabled	Pins 1 & 2 closed

FACTORY CONFIGURED SETTINGS - DO NOT ALTER	
Jumper	Setting
JP1	Pins 2 & 3 closed
JP23	Pins 1 & 2 closed
JP24	Pins 2 & 3 closed
JP25	Pins 2 & 3 closed

DIAGNOSTIC LED(S)			
LED	Color	Status	Condition
L1	Red	On	Data is being received
L1	Red	Off	Data is not being received
L1	Red	Blinking	Card is reconfiguring
L2	Green	On	Data is being transmitted
L2	Green	Off	Data is not being transmitted
L2	Green	Blinking	Card is reconfiguring