MULTIPLE PROTOCOL CONTROLLER MPC ASSY 12-10071-xx

JUMPER SETTINGS

Device	Description	Configuration
8530 SCC	Base Address = 380H	E1-E2*
	Base Address = 280H	E1-E2 OUT
8530 SCC	Interrupt Level IRQ2	E46-E47
	Interrupt Level IRQ3	E56-E57*
	Interrupt Level IRQ4	E45-E46
	Interrupt Level IRQ5	E55-E56
8530 DMA INT	Interrupt Level IRQ1	E48-E49 & E58-E59*
	Interrupt Level IRQ2	E59-E60 & E49-E50
8530 SCC	DTE configuration	E3-E19, E4-E20, E5-E21 E6-E22, E7-E23, E8-E24 E10-E26, E13-E14, E15-E31 E16-E32, E17-E33, E18-E34 E35-E36, E38-E40
	DCE configuration	E3-E4, E5-E6, E7-E8 E9-E10, E11-E27, E12-E28 E15-E16, E19-E20, E23-E24 E25-E26, E31-E32, E37-E39 REMOVED E5-E21, E13-E14 E17-E33, E18-E34, E35-E36
8253	32-bit counter IRQ2	E42-E43
	32-bit counter IRQ3	E52-E53
	32-bit counter IRQ4	E41-E42*
	32-bit counter IRQ5	E51-E52
8253	16-bit counter IRQ2	E43-E44
	16-bit counter IRQ3	E53-E54
	16-bit counter IRQ4	E44-E45
	16-bit counter IRQ5	E54-E55

* Indicates factory settings.

MPC-II Register Addresses

Hex Address	Hex Address	Device	Description
280	380	74LS74	Interrupt Enable
284	384	8253	Counter 0
285	385	8253	Counter 1
286	386	8253	Counter 2
287	387	8253	Control Word Reg
288	388	8530	Channel B Control
289	389	8530	Channel B Data (Not used)
28A	38A	8530	Channel A Control
28B	38B	8530	Channel A Data
28C	38C	8530	Interrupt Vector

PROGRAMMING THE MPC-II CONTROLLER

Interrupts are enabled on the 8530 SCC by writing a 1 to the base address of the MPC-II controller (280H or 380H). This register is a master interrupt enable for the MPC-II controller. The 8530 SCC interrupt vector can be read directly from the MPC-II interrupt vector address (28CH or 38CH). The vector read will be one of 8 possible vectors presented by the 8530 SCC during an interrupt acknowledge cycle if the Vector Include Status bit in WR9 is set. Otherwise, the vector returned is the one written to WR2.