VLSI TECHNOLOGY, INC.

VL82C037

IBM VGA®-COMPATIBLE VIDEO GRAPHICS CONTROLLER

FEATURES

- Single-chip VGA video graphics device that is completely compatible in the following systems:
  - –IBM PC/AT-compatible
  - –IBM PC/XT-compatible
  - –IBM PS/2-compatible
- Fully compatible with IBM VGA in all modes
- Provides 800 x 600 element high-resolution graphics with 16 colors
- Flicker-free operation in all video modes
- Supports 132-column text modes
- Supports both digital and analog monitor

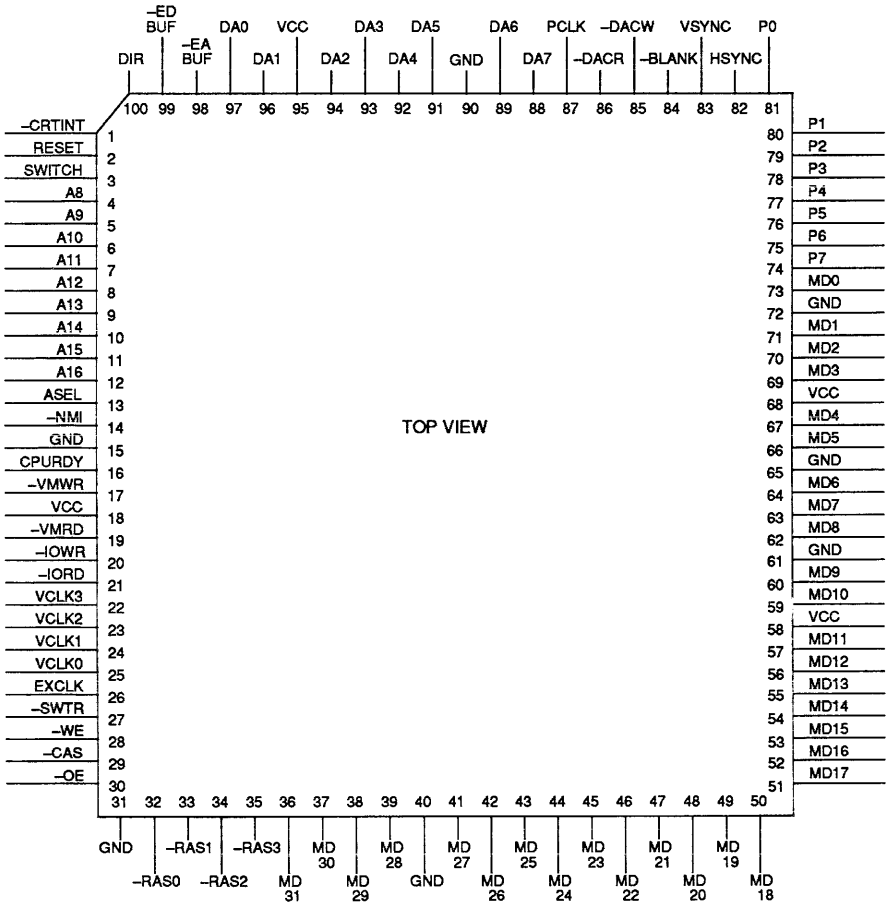
DESCRIPTION

The VL82C037 VGA-compatible Video Graphics Controller is a single-chip, high-integration, high resolution graphics device intended for use in IBM PS/2® Model 30-compatible systems as well PC/AT- and PC/XT-compatible systems. It provides high resolution graphics up to 800 x 600 elements with 16 colors.

The VL82C037 is fully compatible with IBM VGA in all modes, as well as being fully compatible with Hercules graphics. VL82C037 compatibility also extends to IBM EGA BIOS® (basic input/output system), CGA and MDA. It is also flicker-free in all modes. It supports an external digital-to-analog look-up table. The VL82C037 is available from VLSI Technology, Inc. in an industry-standard plastic 100-pin flatpack.

PIN DIAGRAM

VL82C037



ORDER INFORMATION

Part Number	Package
VL82C037-FC	Plastic Flatpack

Notes: Operating temperature range is 0°C to +70°C.

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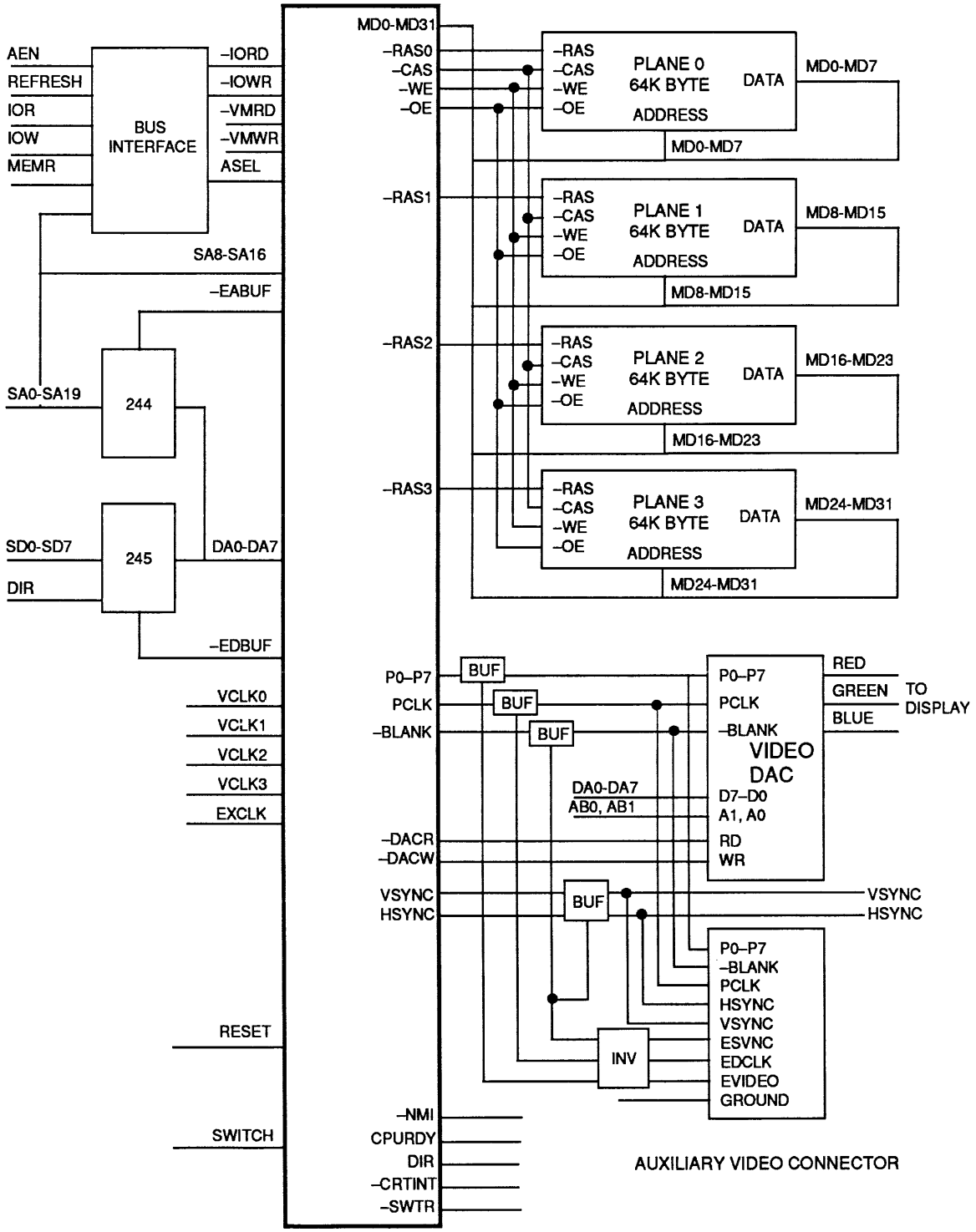
SYSTEM BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
–CRTINT	1	O	Display vertical retrace interrupt. An active low open collector.
RESET	2	I	System reset signal, active high.
SWITCH	3	I	Signal that detects the type of monitor. The state of this input can be read at Input Status Register 0 (Address 03C2) Bit 4.
A8-A16	4-12	I	CPU address bus bits 8 through16.
ASEL	13	I	Active high, to select VGA address to decode.
–NMI	14	O	Non maskable interrupt. An active low open collector.
CPURDY	16	O	An open collector active high output to signal processor that the VGA is ready for access.
–VMWR	17	I	Active low, video memory write signal.
–VMRD	19	I	Active low, video memory read signal.
–IOWR	20	I	Active low, I/O write signal.
–IORD	21	I	Active low, I/O read signal.
VCLK3	22	I	32.514 MHz input clock signal.
VCLK2	23	I	Reserved
VCLK1	24	I	28.322 MHz input clock signal.
VCLK0	25	I	25.175 MHz input clock signal.
EXCLK	26	I	External clock signal.
–SWTR	27	O	Read DIP switch control signal. Active during I/O read from address 03DF (Index = 10).
–WE	28	O	Video memory write enable for bank A (first 256K video memory). An active low signal.
–CAS	29	O	Column address strobe to all planes. An active low signal.
–OE	30	O	Output enable signal to memory bank A (first 256K video memory). It is active low.
–RAS0-RAS3	32-35	O	Row address strobe to planes 0-3. An active low signal.
MD31	36	I/O	Display memory address/data time multiplexed bus line 7, interface to video memory plane 3.
MD30	37	I/O	Display memory address/data time multiplexed bus line 6, interface to video memory plane 3.
MD29	38	I/O	Display memory address/data time multiplexed bus line 5, interface to video memory plane 3.
MD28	39	I/O	Display memory address/data time multiplexed bus line 4, interface to video memory plane 3.
MD27	41	I/O	Display memory address/data time multiplexed bus line 3, interface to video memory plane 3.
MD26	42	I/O	Display memory address/data time multiplexed bus line 2, interface to video memory plane 3.
MD25	43	I/O	Display memory address/data time multiplexed bus line 1, interface to video memory plane 3.
MD24	44	I/O	Display memory address/data time multiplexed bus line 0, interface to video memory plane 3.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MD23	45	I/O	Display memory address/data time multiplexed bus line 7, interface to video memory plane 2.
MD22	46	I/O	Display memory address/data time multiplexed bus line 6, interface to video memory plane 2.
MD21	47	I/O	Display memory address/data time multiplexed bus line 5, interface to video memory plane 2.
MD20	48	I/O	Display memory address/data time multiplexed bus line 4, interface to video memory plane 2.
MD19	49	I/O	Display memory address/data time multiplexed bus line 3, interface to video memory plane 2.
MD18	50	I/O	Display memory address/data time multiplexed bus line 2, interface to video memory plane 2.
MD17	51	I/O	Display memory address/data time multiplexed bus line 1, interface to video memory plane 2.
MD16	52	I/O	Display memory address/data time multiplexed bus line 0, interface to video memory plane 2.
MD15	53	I/O	Display memory address/data time multiplexed bus line 7, interface to video memory plane 1.
MD14	54	I/O	Display memory address/data time multiplexed bus line 6, interface to video memory plane 1.
MD13	55	I/O	Display memory address/data time multiplexed bus line 5, interface to video memory plane 1.
MD12	56	I/O	Display memory address/data time multiplexed bus line 4, interface to video memory plane 1.
MD11	57	I/O	Display memory address/data time multiplexed bus line 3, interface to video memory plane 1.
MD10	59	I/O	Display memory address/data time multiplexed bus line 2, interface to video memory plane 1.
MD9	60	I/O	Display memory address/data time multiplexed bus line 1, interface to video memory plane 1.
MD8	62	I/O	Display memory address/data time multiplexed bus line 0, interface to video memory plane 1.
MD7	63	I/O	Display memory address/data time multiplexed bus line 7, interface to video memory plane 0.
MD6	64	I/O	Display memory address /data time multiplexed bus line 6, interface to video memory plane 0.
MD5	66	I/O	Display memory address/data time multiplexed bus line 5, interface to video memory plane 0.
MD4	67	I/O	Display memory address/data time multiplexed bus line 4, interface to video memory plane 0.
MD3	69	I/O	Display memory address/data time multiplexed bus line 3, interface to video memory plane 0.
MD2	70	I/O	Display memory address/data time multiplexed bus line 2, interface to video memory plane 0.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MD1	71	I/O	Display memory address/data time multiplexed bus line I, interface to video memory plane 0.
MD0	73	I/O	Display memory address/data time multiplexed bus line 0, interface to video memory plane 0.
P7-P0	74-81	O	Video color look up table address bits 7 through 0.
HSYNC	82	O	Horizontal SYNC signal for monitor.
VSYNC	83	O	Vertical SYNC signal for monitor.
–BLANK	84	O	An active low blanking signal to external palette chip.
–DACW	85	O	An active low I/O write signal for external palette chip (256 color look up table).
–DACR	86	O	An active low I/O read signal for external palette chip (256 color look up table).
PCLK	87	O	Pixel clock signal for external palette chip (256 color look up table).
DA7-DA0	88, 89 91-94 96, 97	I/O	Multiplexed address/data bus bits 7 through 0.
–EABUF	98	O	Active low, enable external address buffer.
–EDBUF	99	O	Active low, enable external data buffer.
DIR	100	O	Control signal for bidirectional data bus transceiver.
VCC	18, 58 68, 95		System Power : +5 V
GND	15, 31, 40 61, 65, 72 90		System Ground

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FUNCTIONAL DESCRIPTION

INTRODUCTION

The VGA single chip is a standard video controller for PS/2 line machines including Model 50, 60 and 80. With the same architecture, it can be used on Model 30 and PC/XT/AT systems too. Several new things supported by IBM VGA include higher resolution (640 x 480), new video mode, 256 colors support for 320 x 200 graphics mode, up to 64 shades of grey display for monochrome monitor, and eight fonts loaded into video RAM simultaneously. In the VL82C037 chip, even more functions are added to gain performance.

The host can access both VGA registers and video memory by setting up bus address and read/write commands to read or write 8-bit data. Video RAM and screen refresh activities occur concurrently and independently by assigning appropriate memory access cycles to each of them.

Most registers are readable so that BIOS and driver software can determine the current state of video. In the basic configuration, 256K byte of memory is needed as the display buffer. Four planes of video memory are controlled by four different –RAS (Row Address Strobe) signals, one –CAS (Column Address Strobe), one –WE (Write Enable), and one –OE (Output Enable) signal. The video data bus is time multiplexed with the video address bus in a way that outputs –RAS and –CAS address early in the memory cycle and inputs 8-bit data for read or output for write late in the memory cycle.

NMI (Non-Maskable Interrupt) is generated by trapping accesses to certain I/O ports so that backward compatibility can be achieved through software emulation. The VGA chip provides a 'DIRectional' signal to control data flow to the system data bus for CPU Read or Write.

MAJOR COMPONENTS

There are four major components of VL82C037 contained within a single 100-pin plastic flatpack. They are described below:

CRT CONTROLLER

The VL82C037 CRT Controller provides synchronization control, timing generation and supplies video memory addressing to display memory. Flexible timing configuration options are allowed by accessing I/O registers through software control. During the blanking period, an 8-bit refresh counter is placed on the memory address lines. A split screen feature is also provided to allow two windows. This is done using the Preset Row Scan Register, the Line Compare Register, and the Horizontal Panning Register to pan part of the screen while the rest remains stationary.

SEQUENCER

The VL82C037 Sequencer takes care of basic memory timing for the display memory and the character clock for the control of memory fetches.

The state machine in the sequencer automatically assigns appropriate memory access cycles to the CPU and CRT Controller during active display. The sequencer can also protect the entire memory plane by selectively masking out planes through the Mask register.

GRAPHICS CONTROLLER

The Graphics Controller provides a data path for both CPU Read/Write and CRT Read access to the display memory. For CRT access it directs data to the Attribute Controller while for CPU access it directs data to the system bus. It handles two basic modes which are alphanumeric and graphics. In alphanumeric mode, data is sent in parallel directly to the Attribute Controller. In graphics mode memory data is shifted out serially to the Attribute Controller.

Data formatting and manipulation are implemented for the various modes. A color comparator is provided for fast color comparison in the application of color painting modes. Since the Graphics Controller can process 32-bit data (8-bits from each plane) at a time, a fast color presetting and area fill operations can be achieved.

ATTRIBUTE CONTROLLER

The VL82C037 Attribute Controller provides video shifting, attribute processing and an internal palette of 16 colors selectable from a possible 64 colors. Pixel panning is also provided for both graphics and text modes. Underline, cursor and blinking logic are interpreted and manipulated here. The final output of Attribute Controller is 8-bit wide color data to be sent to the external color look-up table for final color mapping.

MEMORY AND CLOCK CONSIDERATIONS

In basic configuration, eight 64K x 4-bit dynamic RAM's should be used to configure 256K byte of video memory. The supported speed of DRAM and CLOCK are related to the graphics resolution as shown in Table 1.

VGA REGISTERS

All the registers in the VGA can be categorized into six groups for the different function blocks in the hardware. In the VL82C037 VGA chip, the system microprocessor data latches are readable for faster save and restore of the VGA state in the VGA BIOS. The VGA also provides the system microprocessor interface for the video DAC (external color pallete chip). The DAC has one address register which can be accessed through address hex 03C7 for read, and hex 03C8 for write. Table 2 lists the registers and the I/O address where they are located. It also lists whether or not they are read/write, read-only, or write-only.

Note that the PEL Mask Register must not be written to by application code or destruction of the color look-up table data may occur.

GENERAL REGISTERS

This section describes the general registers. The (?) in some of the addresses is controlled by bit 0 of the Miscellaneous Output Register.

TABLE 1. RESOLUTION REQUIREMENTS

DRAM	120 ns	120 ns	100 ns
CLOCK	28 MHz	25 MHz	36 MHz
RESOLUTION	720 x 400	640 x 480	800 x 600
COLORS	16	16	16

TABLE 2. VGA REGISTERS

Register Group	R/W	Mono Emulation	Color Emulation
General Registers			
Miscellaneous	W	03C2	03C2
	R	03CC	03CC
Input Status 0	RO	03C2	03C2
Input Status 1	RO	03BA	03DA
Feature Control	W	03BA	03DA
	R	03CA	03CA
VGA Enable	RW	03C3	03C3
PEL Address (Write)	RW	03C8	03C8
PEL Address (Read)	WO	03C7	03C7
PEL Data Register	RW	03C9	03C9
PEL Mask	RW	03C6	03C6
Sequencer Registers			
Address Register	RW	03C4	03C4
Data Registers	RW	03C5	03C5
CRTC Registers			
Address Register	RW	03B4	03D4
Data Registers	RW	03B5	03D5
Graphics Registers			
Address Register	RW	03CE	03CE
Data Register	RW	03CF	03CF
Attribute Registers			
Address Register	RW	03C0	03C0
Data Registers	W	03C0	03C0
	R	03C1	03C1
Extended Registers			
Address Register	RW	03DE	03DE
Data Registers	RW	03DF	03DF

TABLE 3. GENERAL REGISTERS

Name	Read Port	Write Port
Miscellaneous Output	03CC	03C2
Input Status 0	03C2	—
Input Status 1	03?A	—
Feature Control	03CA	03?A
VGA Enable	03C3	03C3
DAC State	03C7	—

TABLE 4. VERTICAL SIZE REGISTER

Bit 7	Bit 6	Vertical Size
0	0	Reserved
0	1	400 lines
1	0	350 lines
1	1	480 lines

TABLE 5. CLOCK REGISTERS

CSEL2	CSEL1	CSEL0	CLOCK
0	0	0	25.175 MHz
0	0	1	28.322 MHz
0	1	0	External Input Clock
0	1	1	Reserved
1	0	0	14.161 MHz
1	0	1	16.257 MHz
1	1	0	Reserved
1	1	1	32.514 MHz

Miscellaneous Output Register
Read-03CC **Write-03C2**

Bit 7, 6 The Polarity of Vertical/ Horizontal Sync is used to select the vertical size as shown in Table 4.

Bit 5 Selects between two pages of memory when in the Odd/Even modes (mode 0-5, 7). A logical 0 selects the low page of memory; a logical 1 selects the high page of memory. This bit is provided for diagnostic use.

Bit 4 Reserved

Bit 3, 2 These two bits select the clock source. In VL82C037 VGA the third bit is defined in Extended Registers and used with these two bits to select a wider range of clock source for different video modes. See Table 5.

Bit 1 A logical 0 disables Video RAM address decode from the system microprocessor; a logical 1 enables Video RAM to the system microprocessor.

Bit 0 A logical 0 sets CRTC addresses to Hex 03BX and Input Status Register 0's address to 03BA for Monochrome emulation. A logical 1 sets CRTC addresses to Hex 03DX and Input Status Register 0's address to Hex 03DA for color emulation.

Input Status Register 0
Read-Only **Address = 03C2**

Bit 7 A logical 1 indicates a vertical retrace interrupt is pending. A logical 0 indicates the vertical retrace interrupt is cleared.

Bit 6, 5 Reserved

Bit 4 This bit allows the power-on initialization to determine if a monochrome or color monitor

is connected to the system. It reflects the state of the switch input.

Bit 3-0 Reserved

Input Status Register 1
Read-Only **Address = 03?A**

Bits 7, 6 Reserved

Bits 5, 4 These two bits are used for diagnostics. They are connected to two of the eight color outputs of the Attribute Controller. The two bits defined in the Color Plane Enable Register control the multiplexer for the color output wiring and are described in Table 6.

Bit 3 A logical 1 occurs during a vertical retrace interval. A logical 0 shows that video information is being displayed.

Bits 2, 1 Reserved

Bit 0 A logical 1 indicates a horizontal or vertical retrace interval. A logical 0 indicates that the internal Display Enable Signal is active. Some programs use this status bit to restrict screen updates to blanked display intervals. The VL82C037 has been designed to eliminate this software requirement, so display screen updates may be made at any time.

Feature Control Register
Read = 03CA **Write = 03?A**

Bits 7-4 Reserved

Bits 3 This bit should always be set to 0 to enable normal vertical sync output to the monitor; when bit 3 = 1, the "vertical sync" output is the logical OR of "vertical sync" and "vertical display enable". It is normally set to 0.

Bits 2-0 Reserved

Video Subsystem Enable Register
Read-03C3 **Write-03C3**

Bits 7-1 Reserved

Bit 0 A logical 1 enables video I/O and memory address decoding. A 0 disables the video I/O and memory address decoding.

SEQUENCER REGISTERS

This section describes the registers in the Sequencer Control block. See Table 7.

Sequencer Address Register
Read-03C4 **Write-03C4**

Bits 7-3 Reserved

Bits 2-0 A binary value pointing to the register where data is to be written or read.

Reset Register
Port = 03C5 **Index 0**

Bits 7-2 Reserved

Bit 1 A logical 0 directs the sequencer to synchronously clear and halt. Bits 1 and 0 must be 1 to allow the sequencer to operate. This bit must be set to 0 before changing either bit 3 or bit 0 of the Clocking Mode register, or bit 3 or bit 2 of the Miscellaneous Output Register, or bit 5, bit 4 or bit 3 of the Bandwidth Control Register.

Bit 0 A logical 0 directs the sequencer to asychronously clear and halt. Bit 1 and 0 must both be 1 to allow the sequencer to operate. Resetting the sequencer with this bit can cause data loss in the dynamic video RAM.

Clocking Mode Register
Port = 03C5 **Index 1**

Bits 7, 6 Reserved

Bit 5 When set to 1, turns off the video screen and assigns maximum memory bandwidth to the system CPU. A logical 0 puts the screen into normal operation. Synchronization pulses are maintained during blanking. This bit can be used for fast full-screen updates.

Bit 4 When set to 1, the internal shift registers are loaded every fourth character clock. When set to 0, they are loaded every character clock. When 32 bits are fetched each cycle and used together in the shift registers, this mode is useful.

Bit 3 A logical 0 selects normal the dot clock directly from the sequencer master clock input. A logical 1 will select master clock divided by two as dot clock. Normally, dot clock divided by two is used for 320 and 360 horizontal resolution modes.

Bit 2 When set to 1, the internal shift load registers are loaded every other character clock. When set to 0, and bit 4 is set to 0, the internal shift load registers are loaded every character clock. This mode is useful when 16 bits are fetched per cycle and chained together in the shift load registers.

Bit 1 Reserved

Bit 0 A logical 0 directs the sequencer to generate nine dot wide character clocks. A logical 1 generates eight dot wide character clocks from the

TABLE 6. REGISTER BITS

Color Plane Register		Input Status 1 Register	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

TABLE 7. SEQUENCER REGISTERS

Register Name	I/O Port	Index
Sequencer Address	03C4	—
Reset	03C5	00
Clocking Mode	03C5	01
Map Mask	03C5	02
Character Map Select	03C5	03
Memory Mode	03C5	04

TABLE 8. MAP SELECT (1)

Bit 5	Bit 3	Bit 2	Map	Table Location
0	0	0	0	1st 8K of Map 2
0	0	1	1	3rd 8K of Map 2
0	1	0	2	5th 8K of Map 2
0	1	1	3	7th 8K of Map 2
1	0	0	4	2nd 8K of Map 2
1	0	1	5	4th 8K of Map 2
1	1	0	6	6th 8K of Map 2
1	1	1	7	8th 8K of Map 2

TABLE 9. MAP SELECT (2)

Bit 4	Bit 1	Bit 0	Map	Table Location
0	0	0	0	1st 8K of Map 2
0	0	1	1	3rd 8K of Map 2
0	1	0	2	5th 8K of Map 2
0	1	1	3	7th 8K of Map 2
1	0	0	4	2nd 8K of Map 2
1	0	1	5	4th 8K of Map 2
1	1	0	6	6th 8K of Map 2
1	1	1	7	8th 8K of Map 2

sequencer. Select nine dots for alphanumeric modes only. For nine dot modes, the ninth dot equals the eighth dot for ASCII codes C0 through DF hex. Also, see the Line Graphics bit in the Mode Control Register in the Attribute Register section.

Map Mask Register
Port = 03C5 **Index = 02**
Bits 7-4 Reserved
Bits 3-0 A logical 1 enables the CPU to write to the corresponding memory map. These bits are used to write protect any memory map. When all four bits are logical 1, a 32-bit write operation can be performed by the CPU with only one memory cycle. This is useful for intensive screen updates in graphics modes. For odd/even modes, maps 0 and 1, and maps 2 and 3 should have the same map mask value. When chain 4 mode is selected, all maps should be enabled. This is a read-modify-write operation for CPU write.

Character Map Select Register
Port = 03C5 **Index = 03**
Bits 7, 6 Reserved

Bits 5,3,2 Selects font table from map 2 according to Table 8 when attribute bit 3 is a 1.

Bits 4,1,0 Selects font table from map 2 according to Table 9 when attribute bit 3 is a 0.

Note: Bit 3 of the attribute byte normally controls the foreground intensity in text modes. This bit, however, may be redefined as a switch between character sets. For this feature to work, the value of Character Map Select A must not equal the value of Character Map Select B.

Memory Mode Register
Port = 03C5 **Index = 04**
Bits 7-4 Reserved

Bit 3 A logical 0 enables the CPU to access data sequentially within a bit map by use of the Map Mask Register. A logical 1 causes two low-order address bits (A0, A1) to select the map that will be accessed according to Table 10. For read operation by the CPU, these two bits are also used to select the map in the graphics section.

TABLE 10. MAP SELECT (3)

A1	A0	Map Selected
0	0	Map 0
0	1	Map 1
1	0	Map 2
1	1	Map 3

Bit 2 A logical 0 directs even CPU addresses to access maps 0 and 2, while odd CPU addresses access maps 1 and 3. A logical 1 causes access to data within a bit map sequentially.

Bit 1 A logical 1 shows that greater than 64K bytes of video memory is being used. This is set to permit the VGA to use 256K bytes of video memory. This also enables character map selection. (See Character Map Select Register.)

Bit 0 Reserved

CRT CONTROLLER REGISTERS
This section describes the registers in the CRT Controller. See Table 11.

CRT Controller Address Register
Port = 03?4
Bits 7, 6 Reserved

Bit 5 Test bit, must remain 0.

Bit 4-0 Binary value programmed in these bits selects one of the CRT Controller registers where data is to be accessed.

Note: All CRT Controller Registers are read/write registers.

Horizontal Total Register
Port = 03?5 **Index = 0**
In the CRT Controller, there is a horizontal character counter which counts character clock inputs generated by the Sequencer and compares this against the value of the Horizontal Total Register to provide horizontal timings. The horizontal total defines the total number of characters in the horizontal scan interval including the retrace time.

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TABLE 11. CRT CONTROLLER REGISTERS

Register Name	Port	Index
CRT Controller Address Register	03?4	—
Horizontal Total	03?5	00
Horizontal Display Enable End	03?5	01
Start Horizontal Blanking	03?5	02
End Horizontal Blanking	03?5	03
Start Horizontal Retrace	03?5	04
End Horizontal Retrace	03?5	05
Vertical Total	03?5	06
Overflow	03?5	07
Preset Row Scan	03?5	08
Maximum Scan Line	03?5	09
Cursor Start	03?5	0A
Cursor End	03?5	0B
Start Address High	03?5	0C
Start Address Low	03?5	0D
Cursor Location High	03?5	0E
Cursor Location Low	03?5	0F
Start Vertical Retrace	03?5	10
End Vertical Retrace	03?5	11
Vertical Display Enable End	03?5	12
Offset	03?5	13
Underline Location	03?5	14
Start Vertical Blank	03?5	15
End Vertical Blank	03?5	16
CRTC Mode Control	03?5	17
Line Compare	03?5	18

? = B or D in accordance with Bit 0 of Miscellaneous Output register.

TABLE 12. SKEW

Bit 6	Bit 5	Amount of Skew
0	0	Zero Characters
0	1	One Characters
1	0	Two Characters
1	1	Three Characters

Bits 7-0 The total number of characters minus 5.

Horizontal Display Enable End Register
Port = 03?5 **Index = 01**

This register defines the length of the horizontal display enable signal. It determines the number of displayed character positions per horizontal line.

Bits 7-0 Total number of displayed characters minus 1.

Start Horizontal Blanking Register
Port = 03?5 **Index = 02**

Bit 7-0 This 8-bit value determines when to start the internal horizontal blanking output signal. When the internal character counter reaches this value, the horizontal blanking signal becomes active.

End Horizontal Blanking Register
Port = 03?5 **Index = 03**

Bit 7 Test Bit

Bits 6, 5 Bits 6 and 5 indicate the magnitude of display enable skew. Display enable skew control is necessary to give adequate time for the CRT Controller to interrogate the display buffer in order to obtain a character and attribute code. It must also access the character generator font and access the Horizontal PEL Panning register in the Attribute Controller. The display enable signal must be skewed one character clock unit for every access. This allows the video output to be in synchronization with the horizontal and vertical retrace signals. See Table 12.

Bits 4-0 A binary value programmed in these bits is compared to the six least-significant bits of the horizontal character counter to determine the status of the horizontal blanking signal. When the values are equal the horizontal blanking signal becomes inactive. Use the following algorithm to calculate the value of the register:

Value of Start Blanking register + width of blanking signal in character clock units = 6-bit

result to be programmed into these bits. Bit number 5 is located in the End Horizontal Retrace register.

Start Horizontal Retrace Register
Port = 03?5 **Index = 04**

Bits 7-0 This register is used to center the screen horizontally and to specify the character position at which the Horizontal Retrace Pulse becomes active. The value programmed is a binary count of the character position at which the signal becomes active.

End Horizontal Retrace Register
Port = 03?5 **Index = 05**

This register specifies the character position at which the Horizontal Retrace Pulse becomes inactive.

Bit 7 This is bit number 5 of End Horizontal Blanking. The first four bits are located in the End Horizontal Blanking register (index hex 03).

Bits 6, 5 These bits control the skew of the Horizontal Retrace signal. See Table 12.

Bits 4-0 A value programmed here is compared to the five least-significant bits of the horizontal character counter. When they are equal, the horizontal retrace signal becomes inactive. Use the following algorithm to calculate the end of the retrace signal:

Value of Start Horizontal Retrace Register + Width of Horizontal Retrace signal in character clock units = 5-bit result to be programmed into the End Horizontal Retrace Register.

Vertical Total Register
Port = 03?5 **Index = 06**

The 8-bit binary value gives the number of horizontal scan lines on the CRT screen, minus 2, including vertical retrace. This is the low-order 8-bits of a 10-bit value. Bit 8 of this register is located in the CRT Controller Overflow register (index 07, bit 0). Bit 9 of this register is located in the CRT Controller Overflow register (index 07, bit 5).

Bits 7-0 Total number of horizontal scan lines, minus 2.

Overflow Register
Port = 03?5 **Index = 07**

Bit 7 Bit 9 of the Start Vertical Retrace register.

Bit 6 Bit 9 of the Vertical Display Enable End Register.

Bit 5 Bit 9 of the Vertical Total Register.

Bit 4 Bit 8 of the Line Compare Register.

Bit 3 Bit 8 of the Start Vertical Blanking Register.

Bit 2 Bit 8 of the Start Vertical Retrace Register.

Bit 1 Bit 8 of the Vertical Display Enable End Register.

Bit 0 Bit 8 of the Vertical Total Register.

Preset Row Scan Register
Port = 03?5 **Index = 08**

Bit 7 Reserved

Bits 6, 5 Bits 6 and 5 control byte panning when programmed as multiple shift modes. (This is currently not used.) The PEL Panning register in the attribute section allows panning of up to eight single PELs. When in single byte shift modes the CRT Controller start address is increased by one, while attribute panning is reset to 0. This is done to pan the next higher PEL. When used for multiple shift modes, the byte pan bits are extensions to the Horizontal PEL Panning Register in the Attribute Controller. In this manner, panning across the width of the video output shift is achieved. In the 32-bit shift mode, the byte pan and PEL panning bits provide up to 31 bits of panning capability. To pan from position 31 to 32, the CRT Controller start address is incremented and PEL and byte panning is reset to 0. These bits should normally be set to 0.

Bits 4-0 A binary value to specify the starting row scan count after a vertical retrace. The row scan counter increments each horizontal retrace time until a maximum row scan occurs. At maximum row scan compare time, the row scan is cleared (not preset).

Maximum Scan Line Register
Port = 03?5 **Index = 09**

Bit 7 A logical 1 causes the clock to the row scan counter to be divided by 2 and enables 200 to 400 line conversion. This allows the older 200-line modes to be displayed as 400 lines on the display (i.e. each line is displayed twice). When this bit is a 0, the clock to the row scan counter is equal to the horizontal scan rate.

Bit 6 Bit 9 of the Line Compare Register.

Bit 5 Bit 9 of the Start Vertical Blank Register.

Bits 4-0 These bits specify the number of lines per character row. The number to be programmed is the maximum row scan number minus 1.

Cursor Start Register
Port = 03?5 **Index = 0A**

Bits 7, 6 Reserved

Bit 5 A logical 1 turns off the cursor, a logical 0 turns on the cursor.

Bits 4-0 The value of these five bits tells the row scan line of a character where cursor is to begin.

Note that when Cursor Start is programmed with a value greater than the Cursor End, no cursor is generated.

Cursor End Register
Port = 03?5 **Index = 0B**

Bit 7 Reserved

Bits 6, 5 These bits control the skew of the cursor signal. Cursor skew delays the cursor by the selected number of clocks. Each additional skew moves the cursor right one position on the screen. See Table 13.

Bits 4-0 These bits specify the row scan line where the cursor is to end.

TABLE 13. CLOCK SKEW

Bit 6	Bit 5	Function
0	0	Zero-character clock skew
0	1	One-character clock skew
1	0	Two-character clock skew
1	1	Three-character clock skew

Start Address High Register
Port = 03?5 Index = 0C

Bits 7-0 These are the high-order 8 bits of the start address. The 16-bit value from the high-order and low-order Start Address Registers is the first address after the vertical retrace on each screen refresh.

Start Address Low Register
Port = 03?5 Index = 0D

Bits 7-0 These are the low-order 8 bits of the start address.

Cursor Location High Register
Port = 03?5 Index = 0E

Bits 7-0 These are the high-order 8 bits of the cursor location.

Cursor Location Low Register
Port = 03?5 Index = 0F

Bits 7-0 These are the low-order 8 bits of the cursor location.

Start Vertical Retrace Register
Port = 03?5 Index = 10

Bits 7-0 These are the low-order 8 bits of the vertical retrace pulse start position in horizontal scan lines. Bit 8 and 9 are in the CRTC Overflow register.

End Vertical Retrace Register
Port = 03?5 Index 11

Bit 7 A logical 0 enables writing to CRTC registers 0-7. A logical 1 disables writing to these registers. Note that the line compare bit 4 in register 07 is not protected.

Bit 6 A logical 0 selects three refresh DRAM cycles. A logical 1 selects five refresh cycles per horizontal line. Five refresh cycles are used for slow (15.75 KHz) sweep rate displays.

Bit 5 A logical 0 enables a vertical retrace interrupt. This occurs on IRQ2. Since this may be a "shared" interrupt level, the Input Status register 0, bit 7, must be checked to determine if the VGA caused the interrupt to occur.

Bit 4 A logical 0 clears a vertical retrace interrupt. An interrupt handler has to reset an internal flip-flop by writing a 0 to this bit, then setting the bit to 1 so that the flip-flop does not hold interrupts inactive. Note that you should not change the other bits in this register when changing this bit. Read this register first before resetting this flip-flop so that the value of the other bits can be preserved.

Bits 3-0 These bits determine the horizontal scan count value when the vertical retrace output signal becomes inactive. Use the following algorithm to calculate the vertical retrace signal end:

Value of Start Vertical Retrace register + width of vertical retrace signal in horizontal scan line units = 4-bit result to be programmed into the End Vertical Retrace register.

Vertical Display Enable End Register
Port = 03?5 Index = 12

Bits 7-0 These are the low-order 8 bits of a 10-bit register that determines the vertical display enable end position. Bits 8 and 9 of this register are contained in the CRT Controller Overflow register bits 1 and 6 respectively.

Offset Register
Port = 03?5 Index = 13

Bits 7-0 This register defines the logical line width of the screen. Starting memory address for the next character row is larger than the current character row by a factor of 2X or 4X this value. A word or doubleword address may be used to program the Offset Register, depending on the method of clocking the CRT Controller.

Underline Location Register
Port = 03?5 Index = 14

Bit 7 Reserved

Bit 6 A logical 1 enables doubleword mode for memory addresses. Also, see the description of the CRT Controller Mode Control register bit 6.

Bit 5 When this bit is set to 1, the memory address counter is clocked with the character clock divided by 4. This bit is used when doubleword addresses are used.

Bits 4-0 This register determines the horizontal row scan of a character row where an underline occurs. The scan line number desired is one greater than the number programmed.

Start Vertical Blanking Register
Port = 03?5 Index = 15

Bits 7-0 These are the low-order 8 bits of a 10-bit register. The value of this register determines when the vertical blanking signal becomes active. Bit 8 is located in the CRT Controller Overflow register bit 3. Bit 9 is contained in the CRT Controller Maximum Scan Line register bit 5. The horizontal scan line count (at which the vertical blanking signal becomes active) is one greater than the value of these 10 bits.

End Vertical Blanking Register
Port = 03?5 Index = 16

Bits 7-0 This register defines the horizontal scan count value at the time the vertical blank output signal goes inactive. The register must be programmed in whole units of horizontal scan lines. Use the following algorithm to obtain the vertical blank signal end value:

(Value of Start Vertical Blank register - 1) + width of vertical blank signal in horizontal scan unit = 8-bit result to be programmed into the End Vertical Blank register.

CRTC Mode Control Register
Port = 03?5 Index =17

Bit 7 A logical 0 clears horizontal and vertical retrace. A logical 1 enables horizontal and vertical retrace. This bit does not reset any other registers or outputs.

Bit 6 A logical 0 selects word address mode which shifts all memory address counter bits down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output. A logical 1 selects the byte address mode. Note that bit 6 of the Underline Location register also controls the addressing. When it is a 0, bit 6 of this register has control. When it is a 1, the addressing is forced to be shifted by two bits. (See Table 14.)

Bit 5 This bit selects the memory address counter bit MA13 or bit MA15, and it appears on the MA0 output in the word address mode. A logical 1 selects MA15. MA13 is selected for the case where only 64K memory is installed. Since 256K memory is normally installed for VL82C037, MA15 should be selected only in odd/even mode.

Bit 4 Reserved

Bit 3 A logical 0 causes the memory address counter to be clocked with the normal character clock input. A logical 1 clocks the memory address counter with the character clock input divided by 2. This bit is used to create either a byte or word refresh address for the display buffer.

Bit 2 A logical 0 selects normal horizontal retrace. A logical 1 selects horizontal retrace divided by 2 as the clock that controls the vertical timing counter. This bit can be used to effectively double the vertical resolution capability of the CRT Controller. The 10-bit vertical counter has a maximum of 1024 scan lines. If the vertical counter is clocked with the horizontal retrace divided by 2, then the vertical resolution is doubled to 2048 horizontal scan lines.

Bit 1 A logical 0 selects row scan counter bit 1 for CRT memory address bit MA14. A logical 1 selects MA14 counter bit for CRT memory address bit MA14.

Bit 0 When this bit is a logical 0, row scan address bit 0 is substituted for memory address bit 13 during active display time. This allows compatibility with the 6845 CRTC. A logical 1 enables memory address bit 13 to appear on the memory address output bit 13 of the CRT Controller.

Line Compare Register
Port = 03?5 Index = 18

Bits 7-0 This register is the lower byte of the 10-bit line compare target. When the vertical counter matches this value, the internal start of the line counter is reset. This causes an area of the screen not to be affected by scrolling. Bit 9 is in the Maximum Scan Line register. Bit 8 of this register is in the Overflow Register.

TABLE 14. REGISTER MODES

Memory Address	Byte Mode	Word Mode	Doubleword Mode
MA0/RFA0	MA0	MA15/MA13	MA12
MA1/RFA1	MA1	MA0	MA13
MA2/RFA2	MA2	MA1	MA0
MA3/RFA3	MA3	MA2	MA1
MA4/RFA4	MA4	MA3	MA2
MA5/RFA5	MA5	MA4	MA3
MA6/RFA6	MA6	MA5	MA4
MA7/RFA7	MA7	MA6	MA5
MA8/RFA8	MA8	MA7	MA6
MA9	MA9	MA8	MA7
MA10	MA10	MA9	MA8
MA11	MA11	MA10	MA9
MA12	MA12	MA11	MA10
MA13	MA13	MA12	MA11
MA14	MA14	MA13	MA12
MA15	MA15	MA14	MA13

GRAPHICS CONTROLLER REGISTERS

This section describes the registers in the Graphics Controller. See Table 15.

Graphics Address Register
Port = 03CE

Bits 7-4 Reserved

TABLE 15. GRAPHICS CONTROLLER REGISTERS

Register Name	Port	Index
Graphics Address	03CE	–
Set/Reset	03CF	00
Enable Set/Reset	03CF	01
Color Compare	03CF	02
Data Rotate	03CF	03
Read Map Select	03CF	04
Graphics Mode	03CF	05
Miscellaneous	03CF	06
Color Don't Care	03CF	07
Bit Mask	03CF	08

TABLE 16. DATA FUNCTIONS

Bit 4	Bit 3	Function
0	0	Data Unmodified
0	1	Data ANDed with Latched Data
1	0	Data ORed with Latched Data
1	1	Data XORed with Latched Data

TABLE 17. ROTATE FUNCTIONS

Bit 2	Bit 1	Bit 0	Function
0	0	0	No Rotate
0	0	1	Rotate 1 Position
0	1	0	Rotate 2 Positions
0	1	1	Rotate 3 Positions
1	0	0	Rotate 4 Positions
1	0	1	Rotate 5 Positions
1	1	0	Rotate 6 Positions
1	1	1	Rotate 7 Positions

TABLE 18. MAP DATA

MS 1	MS 0	Function
0	0	Read Data from Map 0
0	1	Read Data from Map 1
1	0	Read Data from Map 2
1	1	Read Data from Map 3

Bits 3-0 A binary value in these bits selects the other registers in the Graphics Controller section.

Set/Reset Register
Port = 03CF **Index = 00**

Bits 7-4 Reserved

Bits 3-0 During CPU memory write with write mode 0, the value of these bits will be written to all eight bits of the respective memory map if Set/Reset mode is enabled for the corresponding map.

Enable Set/Reset Register
Port = 03CF Index = 01

Bits 7-4 Reserved

Bits 3-0 A logical 1 enables the Set/Reset function. When enabled, the respective memory map is written with the value of the Set/Reset register if write mode 0 is selected. However, when write mode is 0 and Set/Reset is not enabled on a map, that map is written with the value of the system microprocessor data.

Color Compare Register
Port = 03CF **Index = 02**

Bits 7-4 Reserved

Bits 3-0 These bits represent a 4-bit color value to be compared. If the system microprocessor sets read mode 1 and does a memory read, the data returned from the memory cycle will be a 1 in each bit position where the four maps equal the color compare register.

The color compare bit is the value that all bits of the corresponding map's byte are compared with. Each of the eight bit positions of the selected byte are then compared across the four maps and a 1 is returned in each bit position where the bits of all four maps equal their respective color compare values.

Data Rotate Register
Port = 03CF **Index = 03**

Bits 7-5 Reserved

Bits 4, 3 Data in the system microprocessor latches can operate logically with data written to memory. If rotate function is selected, it is applied before the logical function. See Table 16.

Bits 2-0 These bits specify the number of positions to right-rotate the system microprocessor data bus during system microprocessor memory writes. This operation is done when the write mode is 0. To write non-rotated data, the bits should be set to 0. See Table 17.

Read Map Select Register
Port = 03CF **Index = 04**

Bits 7-2 Reserved

Bits 1, 0 These bits select the memory map number from which the system microprocessor reads data. This register has no effect on the color compare read mode. In odd/even modes the value may be 00 or 01 (10 or 11) for chained maps 0, 1 (2, 3). See Table 18.

Graphics Mode Register
Port = 03CF **Index = 05**

Bit 7 Reserved

Bit 6 A logical 0 permits bit 5 to handle the loading of the Shift Registers. A logical 1 supports the 256 color mode (only for 320 x 200 resolution).

Bit 5 A logical 1 instructs the Shift Registers in the graphic section to format the serial data with odd numbered bits from both of the odd numbered maps and even numbered bits

TABLE 19. FUNCTION DECODE

Bit-1	Bit-0	Function
0	0	The system microprocessor data is rotated by the number or counts in the Rotate Register that each memory map is written with, unless Set/Reset is enabled for the map. When the map Set/Reset is enabled, they are written with 8-bits of the value in the Set/Reset Register for that map.
0	1	The contents of the system microprocessor latches are written to each memory map. A system read operation loads these latches.
1	0	8-bits of the value of data bit n fills memory map n (0-3).
1	1	The maps are written by the 8-bits contained in the Set/Reset Register for that specific map (Enable Set/Reset Register is a "don't care"). Rotated system microprocessor data is logically ANDed with Bit Mask Register data and forms an 8-bit value. This is the function that the Bit Mask Register performs in write modes 0 and 2. (See Bit Mask Register.)

Note that the logic function specified by the Function Select register is applied to data being written to memory following modes 0, 2, and 3 described above.

from both of the even numbered maps. This bit is used in modes 4 and 5.

Bit 4 A logical 1 enables the odd/even addressing mode, which can emulate the IBM CGA. The value which should be programmed is the value of the Memory Mode register bit 2 of the Sequencer.

Bit 3 A logical 0 causes the system microprocessor to read data from the memory map selected by the Read Map Select register, unless chain 4 (bit 3 of the Sequencer Memory Mode Register) is set to 1. In this case the Read Map Select register has no effect. When this bit is a logical 1, the system microprocessor reads the results of the comparison of the four memory maps and the Color Compare register.

Bit 2 Reserved

Bits 1,0 Write Mode (See Table 19.)

Miscellaneous Register
Port = 03CF **Index = 06**
Bits 7-4 Reserved

Bits 3, 2 These bits control the mapping of the regenerative buffer into the CPU address space. The bit functions are defined in Table 20.

Bit 1 When set to a logical 1, this bit instructs the system microprocessor address bit 0 to be replaced by a higher-order bit. The odd/even maps will be selected with odd/even values of the system microprocessor A0 bit, respectively.

Bit 0 This is the text mode addressing control. A logical 1 enables the graphics mode. The character generator address latches are disabled when set to graphics mode.

Color Don't Care Register
Port = 03CF **Index = 07**
Bits 7-4 Reserved

Bit 3 1 - Do the color compare for map 3.
0 - Don't Care for map 3.

Bit 2 1 - Do the color compare for map 2.
0 - Don't Care for map 2.

Bit 1 1 - Do the color compare for map 1.
0 - Don't Care for map 1.

Bit 0 1 - Do the color compare for map 0.
0 - Don't Care for map 0.

Bit Mask Register
Port = 03CF **Index = 08**

Bits 7-0 Bits programmed to a 1 allow writes to the corresponding bits in the maps. A logical 0 permits the corresponding bit n in each map to be locked at its current state, providing the location being written was the last location read by the system's microprocessor.

Note that the bit mask applies to write modes 0 and 2. To preserve bits using the bit mask, data must be latched internally by reading the location. When data is written to preserve the bits, the most current data in the latches is written in those positions. The bit mask applies to all maps simultaneously.

ATTRIBUTE CONTROLLER REGISTERS

This section describes the registers in the Attribute Controller section. See Table 21.

TABLE 20. BYTE SELECT

Bit 3	Bit 2	Function
0	0	Hex A0000 for 128K Bytes
0	1	Hex A0000 for 64K Bytes
1	0	Hex B0000 for 32K Bytes
1	1	Hex B8000 for 32K Bytes

TABLE 21. ATTRIBUTE CONTROLLER REGISTERS

Register Name	Port	Index
Address Register	03C0	–
Palette Registers	03C0	00-0F
Attribute Mode Control Register	03C0	10
Overscan Color Register	03C0	11
Color Plan Enable Register	03C0	12
Horizontal PEL Panning Register	03C0	13
Color Select Register	03C0	14

Attribute Address Register
Port = 03C0

Bits 7, 6 Reserved

Bit 5 Bit 5 must be written to 0 before loading the Color Palette registers. Normal operation of the Attribute Controller requires that bit 5 be set to 1, which allows the video memory data to reach the palette registers.

Bits 4-0 A binary value in these bits points to the Attribute Data register where data is to be written.

The Address and Data registers can not be selected directly. An internal address flip-flop controls this selection. To initialize the flip-flop, an I/O Read instruction must be sent to the Attribute Controller at address 03BA or 03DA. This clears the flip-flop, and then selects the Address register. The Address register is then loaded with an I/O Write to 03C0. The following I/O Write instruction to 03C0 loads the Data register. The flip-flop changes state each time an I/O Write instruction is sent to the Attribute Controller. It does not change when an I/O Read to 03C1 occurs.

Palette Registers
Write-03C0 Read-03C1 Index-00-0F

Bits 7, 6 Reserved

Bits 5-0 The attribute byte of text or graphic color value is indexed to these 16 Color Palette registers. The content of the selected Palette register is then used as a value sent off the chip to the video DAC, where they in turn serve as addresses into the DAC internal registers.

The Palette registers should be modified only during the vertical retrace interval to avoid problems with the displayed image.

Attribute Mode Control
Port = 03C0 (W), 03C1 (R) Index = 10

Bit 7 This bit selects the source for palette bits P4 and P5, which go to the video DAC. A logic 0 selects bits 4 and 5 of the palette registers above. A logic 1 selects bits 0 and 1 of the Color Select Register.

Bit 6 A logical 1 causes the video pipeline to be sampled so that eight bits are available to select a color in the 256 color mode (hex 13). This bit must be a logical 0 in all other modes.

Bit 5 A logical 0 makes line compare have no effect on the output of the PEL Panning register. A logical 1 causes a successful line compare in the CRTC to force the output of the PEL Panning register to 0. When VSYNC occurs, the output reverts to its programmed value. This bit allows part of the screen to be panned while the rest remains stationary.

Bit 4 Reserved

Bit 3 This bit is set to 1 for blinking graphics modes and alphanumeric modes. A logical 0 selects the background intensity of the attribute input.

Bit 2 A logical 1 enables the special line graphics character codes for the monochrome emulation mode. A logical 0 causes the ninth dot to be the same as the background. When this bit is set to 1 it forces the ninth dot of a line graphic character to be the same as the eighth dot. Graphics character codes are hex C0 through hex DF. For character fonts that do not use the line graphics character codes in this range (hex C0 through hex DF) bit 2 should be a 0. If not, unwanted video information will be shown on the CRT screen.

Bit 1 A logical 1 sets monochrome emulation mode. A logical 0 sets color emulation mode.

Bit 0 A logical 0 selects text mode. A logical 1 selects graphics mode.

Overscan Color Register
Port = 03C0 (W), 03C1 (R) Index = 11

Bits 7-0 A binary value in this register determines the border color displayed on the CRT screen. The border color is displayed right after the Display Enable signal goes low and before the start of blanking period. The border is not supported in the 40-column text modes or the 320-PEL graphics modes, except for mode hex 13.

Color Plane Enable
Port = 03C0 (W), 03C1 (R) Index = 12
Bits 7, 6 Reserved

Bits 5, 4 Two of the eight color outputs will be selected, according to these two bits, to be available for reading on bits 4 and 5 of Input Status Register 1. See Table 22.

Bits 3-0 A logical 1 in each bit enables the respective display memory color plane. A logical 0 disables the color plane.

Horizontal PEL Panning
Port = 03C0 (W), 03C1 (R) Index = 13
Bits 7-4 Reserved

Bits 3-0 These four bits select the number of pixels to shift the video data to the left. PEL panning is available in both graphics and text modes. In modes 0+, 1+, 2+, 3+, 7 and 7+, the maximum shift is eight pixels. Mode 13 allows a maximum of three pixels. In the remaining modes, the image can be shifted a maximum of seven pixels. The order for shifting the image is shown in Table 23.

Color Select Register
Port = 03C0 (W), 03C1 (R) Index = 14
Bits 7-4 Reserved

Bits 3, 2 These bits are the two high-order bits of the 8-bit digital color value sent off-chip in all modes except the 256 color graphics. In the 256 color modes, the 8-bit attributes are stored in video memory. This becomes the 8-bit digital color value to be sent off-chip to the video DAC. These bits can be used to switch quickly among sets of colors in the video DAC.

Bits 1, 0 These two bits can be used to replace the P4 and P5 bits from the Attribute Palette registers to form the 8-bit digital color value sent off-chip. This is controlled by bit 7 of Attribute Mode Control register. By using this feature, sets of colors can be rapidly switched in the video DAC.

TABLE 22. COLOR PLANE AND STATUS

Color Plane Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

TABLE 23. PEL REGISTER

PEL Panning Register Value	Number of PELs Shifted to the Left		
	0+, 1+, 2+ 3+, 7, 7+	All Other Modes	Mode 13
0	1	0	0
1	2	1	–
2	3	2	1
3	4	3	–
4	5	4	2
5	6	5	–
6	7	6	3
7	8	7	–
8	0	–	–

TABLE 24. EXTENDED REGISTERS

Port	Index	R/W	Bits	Register
3DE	–	R/W	5	Extension Address Register
3DF	D	R/W	6	Bandwidth Control
3DF	E	R/W	4	I/O Trap Control
3DF	F	R	8	NMI Data Cache (FIFO)
3DF	10	R	8	Read DIP Switch

EXTENDED REGISTERS
A set of new registers have been added into the basic VGA to perform new features and enhancements. They are grouped under I/O port 3DE and 3DF for address and data access respectively. All except the NMI Data Cache register have both read and write access. A summary of these registers is given in Table 24.

03DE - EXTENSION ADDRESS REGISTER

Bit	Description
0-4	5-bit index pointer to the extension data registers.
5-7	Reserved

The contents of this register need to be programmed before the data register is accessed. The I/O address is 3DE for both read and write access.

03DF - BANDWIDTH CONTROL INDEX D

Bit	Description
0-2	Reserved
3-4	Bandwidth Control (See Table 25.)
5	Clock select bit 2 (CSEL2). Used with bit 2 and 3 of Miscellaneous Register. Up to eight different clock inputs can be selected from. (See Table 5.)
6-7	Reserved

03DF - I/O TRAP CONTROL INDEX E

Bit	Description
0	When set to 1, it turns on the trap and generates NMI for downward compatibility emulation. When set to 0, it turns off the NMI logic.
1-2	Backward Compatibility Mode (See Table 26.)
3-6	Reserved = 0
7	Graphics Latch read compatibility.

03DF - NMI DATA CACHE INDEX F

Bit	Description
0-7	First read of this register gets the address of the trapped I/O.

Second read gets the data of the trapped I/O. The size of the cache is two bytes wide and six rows deep. Each read will cause the read pointer to auto-increment and then reset at the end of the information.

Note that only the first 8 bits of the I/O address are saved into the cache. Since bit 7 is always 1 if there is an address saved at this position, the trapped software should check this bit to determine whether this is the last read or not.

Note that this is a read only register.

03DF - READ DIP SWITCH INDEX 10

Bit	Description
7	Reserved
6	DIP Switch 6
5	DIP Switch 5
4	DIP Switch 4
3	DIP Switch 3
2	DIP Switch 2
1	DIP Switch 1
0	DIP Switch 0

These bits can be read by the BIOS to determine the configuration desired.

TABLE 25. BANDWIDTH

Bit 4	Bit 3	Bandwidth
0	0	1-4
1	0	1-7
0	1	1-9
1	1	Reserved

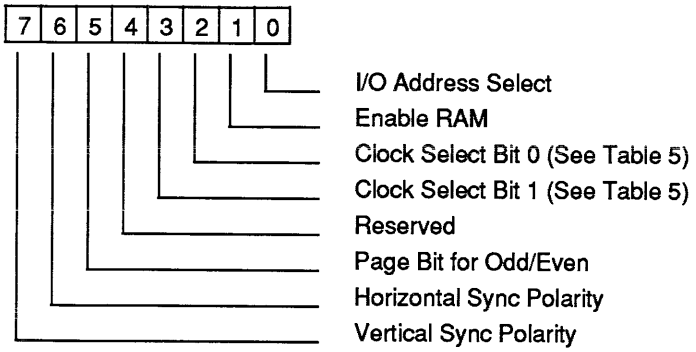
TABLE 26. GRAPHICS MODE

Bit 2	Bit 1	Mode
0	0	VGA
0	1	EGA
1	0	CGA
1	1	MCGA (MDA & HERC)

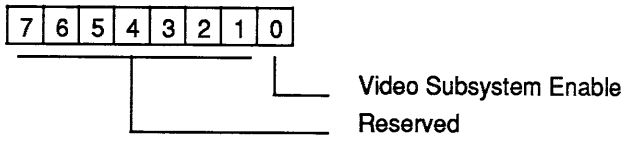
REGISTER SUMMARY

GENERAL REGISTERS

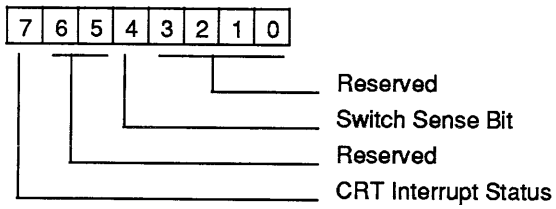
MISCELLANEOUS OUTPUT REGISTER
Address = 03CC (Read), 03C2 (Write)



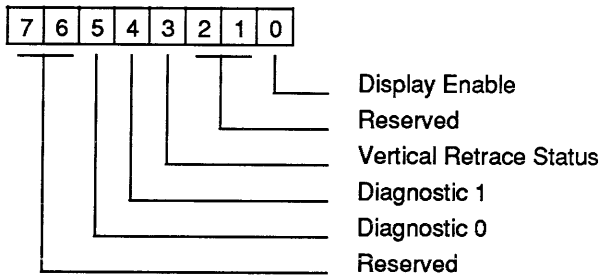
VIDEO SUBSYSTEM ENABLE REGISTER
Address = 03C3 (Read/Write)



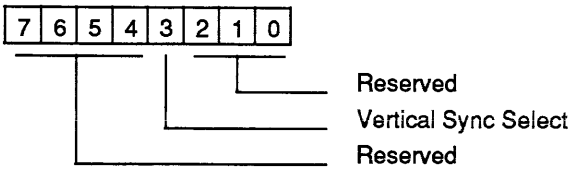
INPUT STATUS REGISTER 0
Address = 03C2 (Read Only)



INPUT STATUS REGISTER 1
Address = 03?A (Read Only)



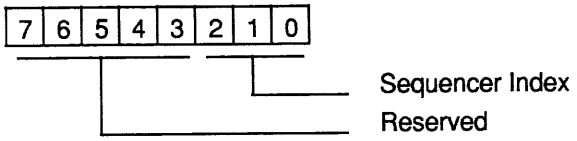
FEATURE CONTROL REGISTER
Address = 03CA (Read), 03?A (Write)



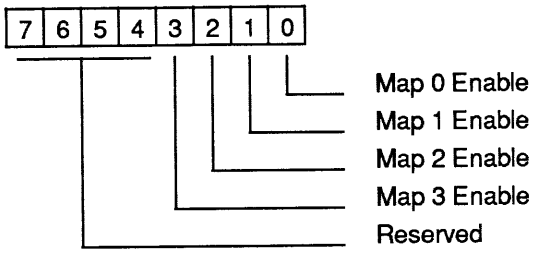
5

SEQUENCER REGISTERS

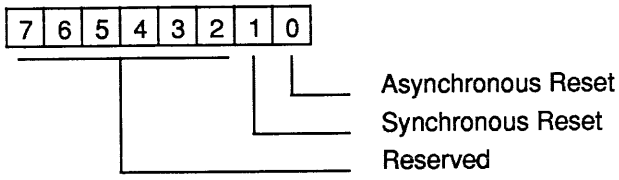
SEQUENCER ADDRESS REGISTER
Address = 03C4 (Read/Write)



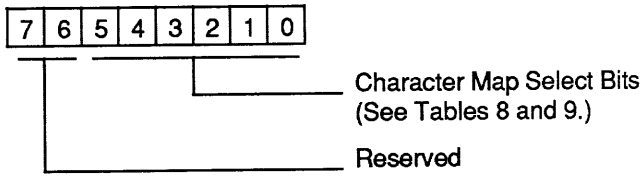
MAP MASK REGISTER
Address = 03C5 Index = 2 (Read/Write)



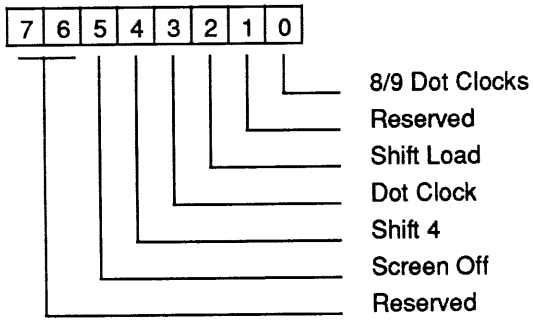
RESET REGISTER
Address = 03C5 Index = 0 (Read/Write)



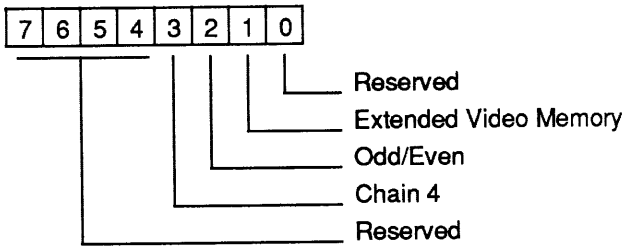
CHARACTER MAP SELECT REGISTER
Address = 03C5 Index = 3 (Read/Write)



CLOCKING MODE REGISTER
Address = 03C5 Index = 1 (Read/Write)

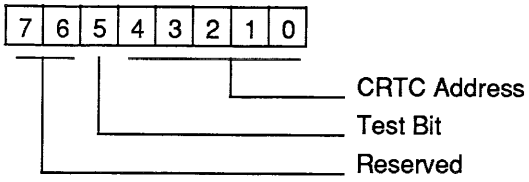


MEMORY MODE REGISTER
Address = 03C5 Index = 4 (Read/Write)

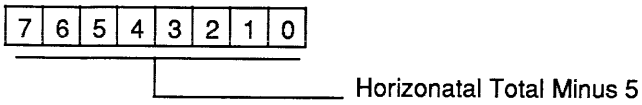


CRT CONTROLLER REGISTERS

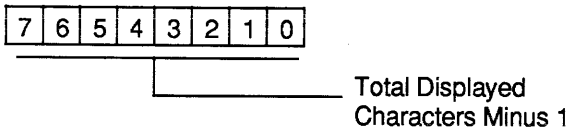
CRT CONTROLLER ADDRESS REGISTER
Address = 03?4 (Read/Write)



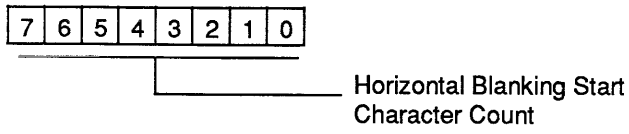
HORIZONTAL TOTAL REGISTER
Address = 03?5 Index 0 (Read/Write)



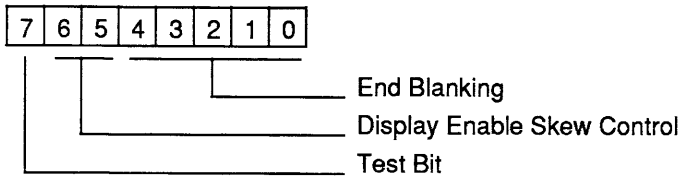
HORIZONTAL DISPLAY ENABLE END REGISTER
Address = 03?5 Index 1 (Read/Write)



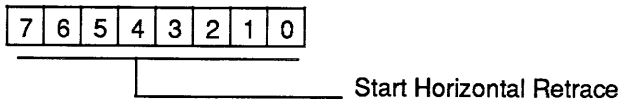
START HORIZONTAL BLANKING REGISTER
Address = 03?5 Index 2 (Read/Write)



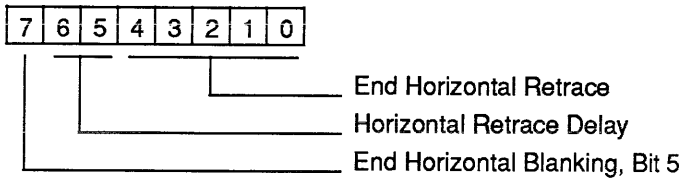
END HORIZONTAL BLANKING REGISTER
Address = 03?5 Index 3 (Read/Write)



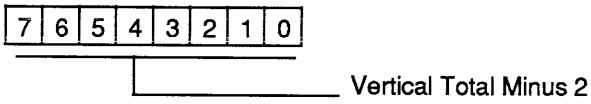
START HORIZONTAL RETRACE REGISTER
Address = 03?5 Index 4 (Read/Write)



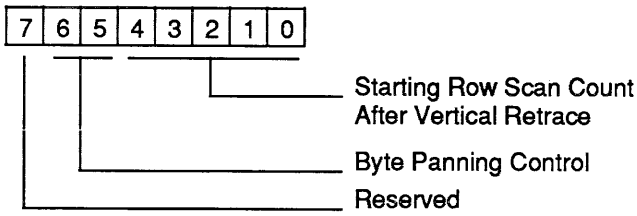
END HORIZONTAL RETRACE REGISTER
Address = 03?5 Index 5 (Read/Write)



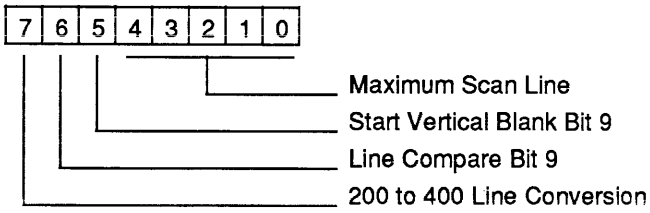
VERTICAL TOTAL REGISTER
Address = 03?5 Index 6 (Read/Write)



PRESET ROW SCAN REGISTER
Address = 03?5 Index 8 (Read/Write)



MAXIMUM SCAN LINE REGISTER
Address = 03?5 Index = 9 (Read/Write)



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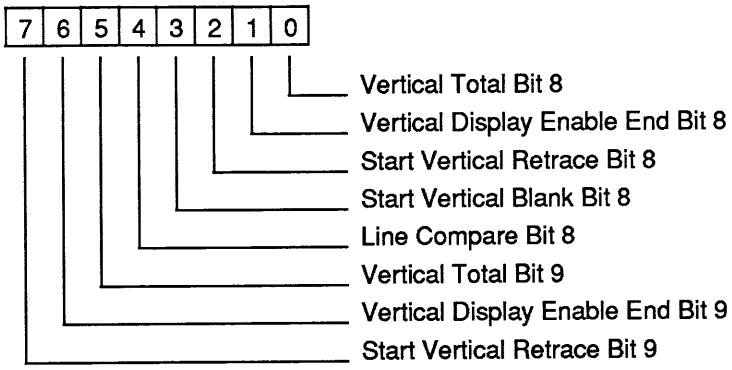
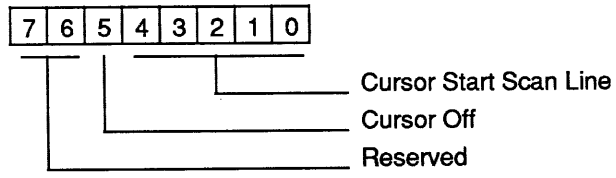
CRT CONTROLLER REGISTERS (Cont.)

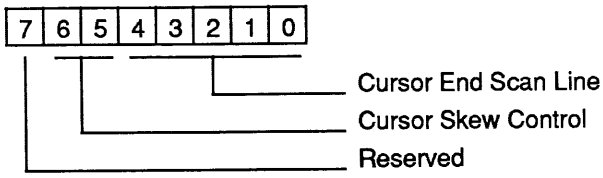
OVERFLOW REGISTER
Address = 03?5 Index 7 (Read/Write)



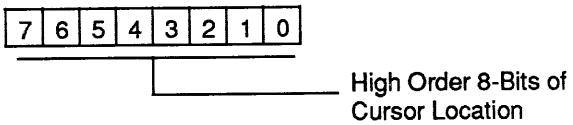
CURSOR START REGISTER
Address = 03?5 Index = A (Read/Write)



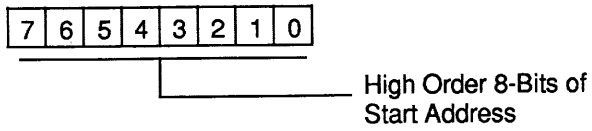
CURSOR END REGISTER
Address = 03?5 Index = B (Read/Write)



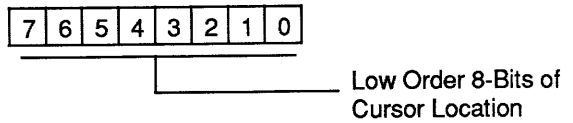
CURSOR LOCATION HIGH REGISTER
Address = 03?5 Index = E (Read/Write)



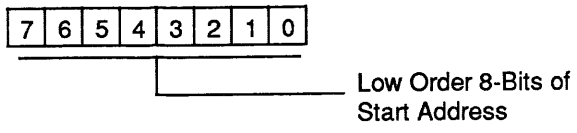
START ADDRESS HIGH REGISTER
Address = 03?5 Index = C (Read/Write)



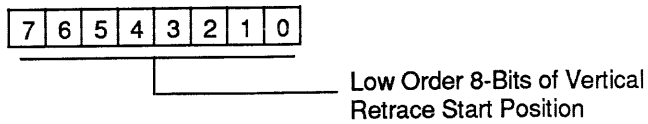
CURSOR LOCATION LOW REGISTER
Address = 03?5 Index = F (Read/Write)



START ADDRESS LOW REGISTER
Address = 03?5 Index = D (Read/Write)

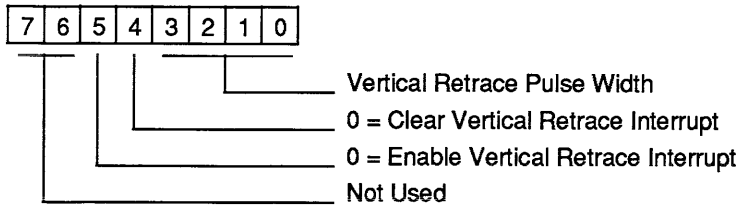


START VERTICAL RETRACE REGISTER
Address = 03?5 Index = 10 (Read/Write)

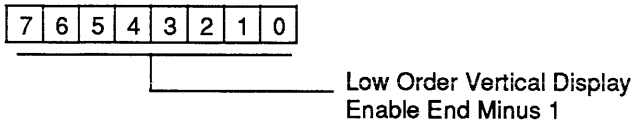


CRT CONTROLLER REGISTERS (Cont.)

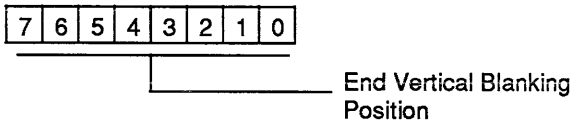
END VERTICAL RETRACE REGISTER
Address = 03?5 Index = 11 (Read/Write)



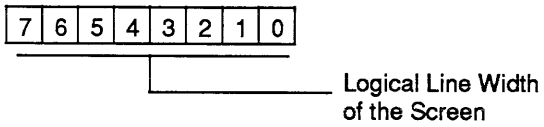
VERTICAL DISPLAY ENABLE END REGISTER
Address = 03?5 Index = 12 (Read/Write)



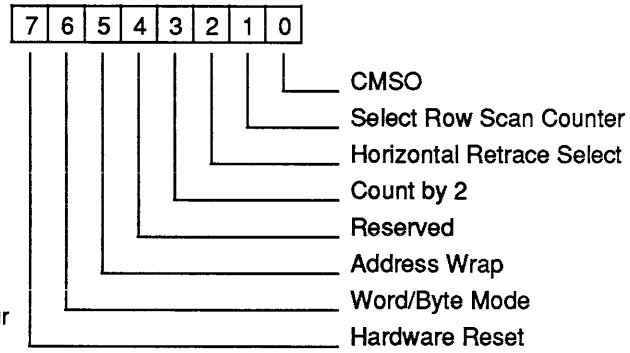
END VERTICAL BLANKING REGISTER
Address = 03?5 Index = 16 (Read/Write)



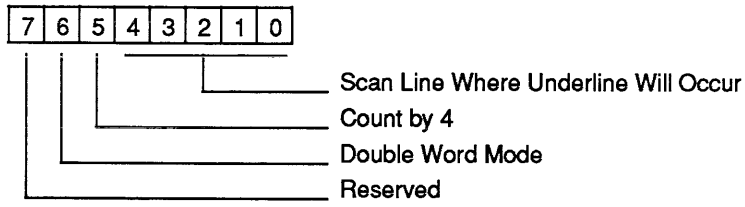
OFFSET REGISTER
Address = 03?5 Index = 13 (Read/Write)



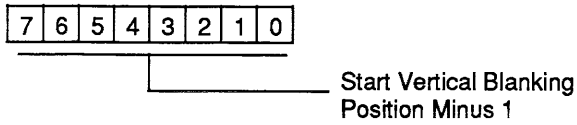
CRTC MODE CONTROL REGISTER
Address = 03?5 Index = 17 (Read/Write)



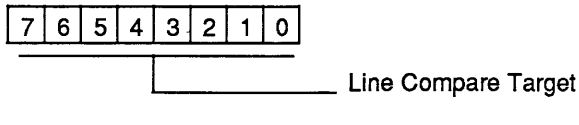
UNDERLINE LOCATION REGISTER
Address = 03?5 Index = 14 (Read/Write)



START VERTICAL BLANKING REGISTER
Address = 03?5 Index = 15 (Read/Write)



LINE COMPARE REGISTER
Address = 03?5 Index = 18 (Read/Write)



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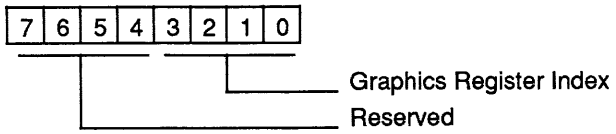
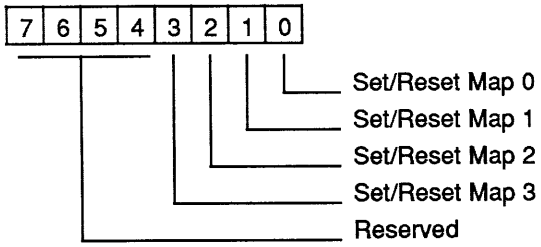
GRAPHICS CONTROLLER REGISTERS

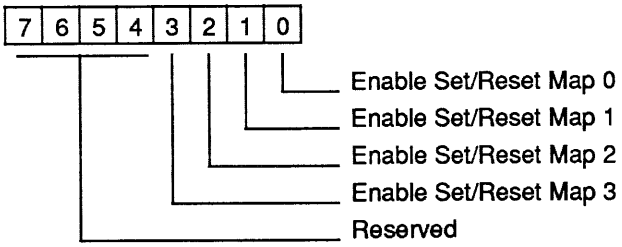
GRAPHICS ADDRESS REGISTER
Address = 03CE (Read/Write)



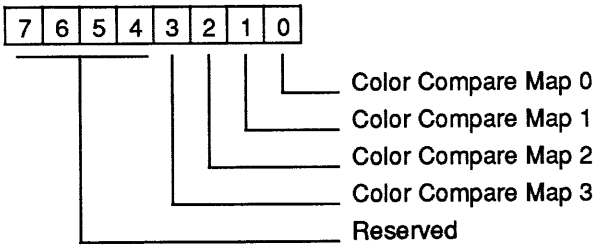
SET/RESET REGISTER
Address = 03CF Index = 0 (Read/Write)



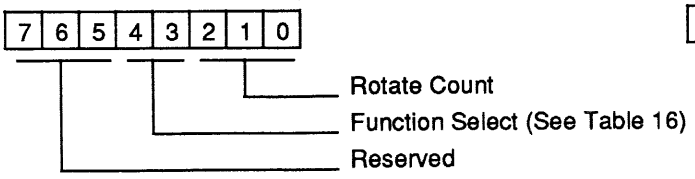
ENABLE SET/RESET REGISTER
Address = 03CF Index = 1 (Read/Write)



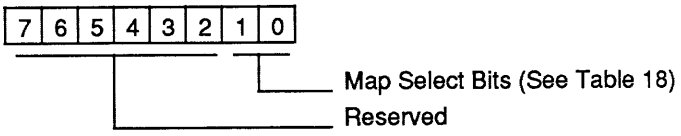
COLOR COMPARE REGISTER
Address = 03CF Index = 2 (Read/Write)



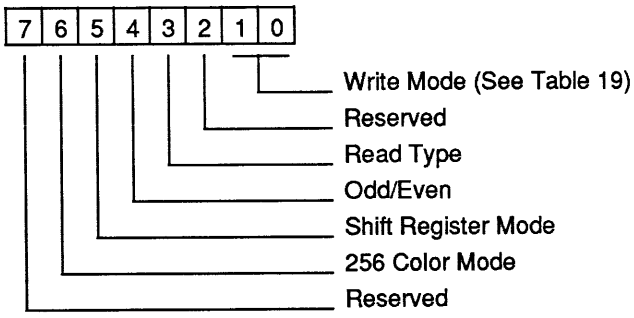
DATA ROTATE REGISTER
Address = 03CF Index = 3 (Read/Write)



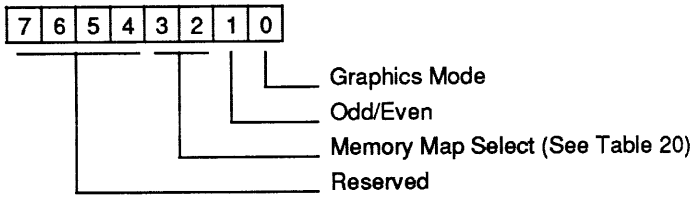
READ MAP SELECT REGISTER
Address = 03CF Index = 4 (Read/Write)



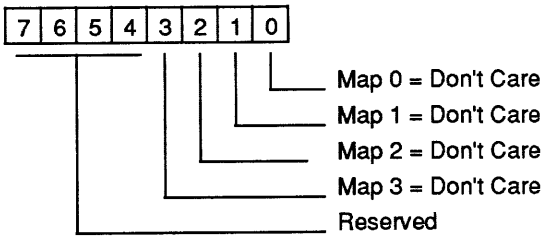
GRAPHICS MODE REGISTER
Address = 03CF Index = 5 (Read/Write)



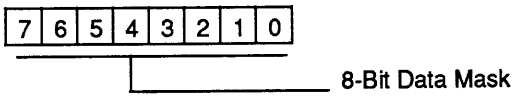
MISCELLANEOUS REGISTER
Address = 03CF Index = 6 (Read/Write)



COLOR DON'T CARE REGISTER
Address = 03CF Index = 7 (Read/Write)

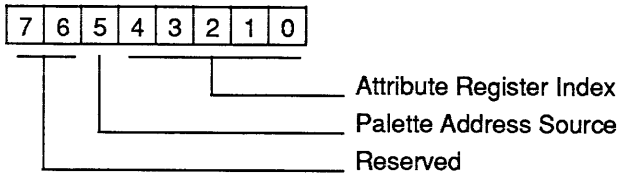


BIT MASK REGISTER
Address = 03CF Index = 8 (Read/Write)

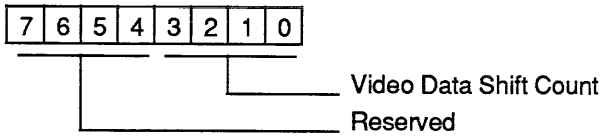


ATTRIBUTE CONTROLLER REGISTERS

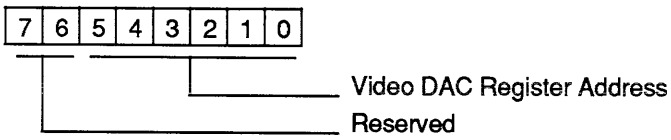
ATTRIBUTE ADDRESS REGISTER
Address = 03C0 (Read/Write)



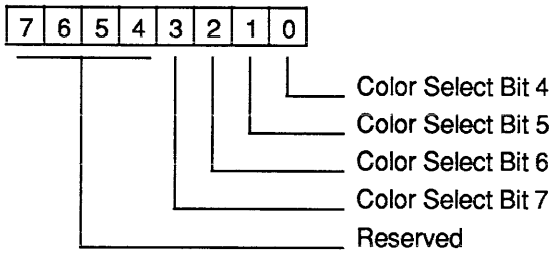
HORIZONTAL PEL PANNING REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 13



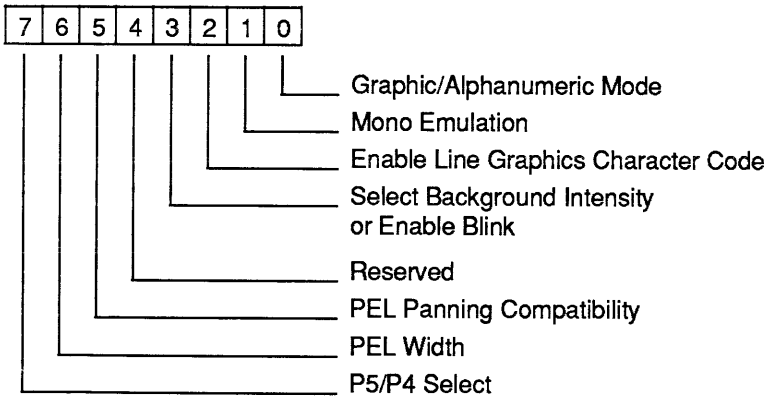
PALETTE REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 0-F



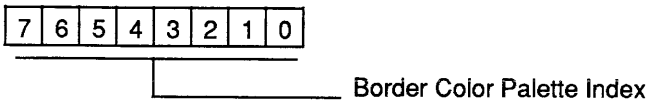
COLOR SELECT REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 14



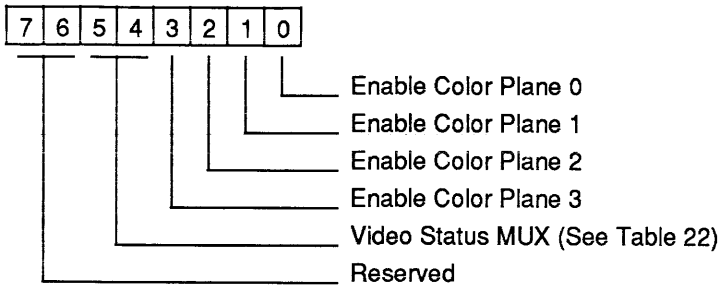
ATTRIBUTE MODE CONTROL REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 10



OVERSCAN COLOR REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 11



COLOR PLANE ENABLE REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 12



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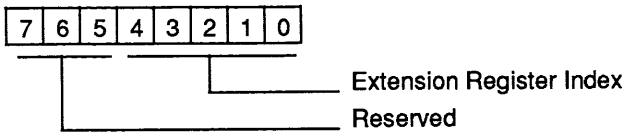
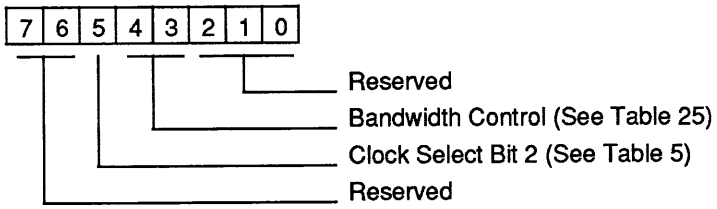
EXTENDED REGISTERS

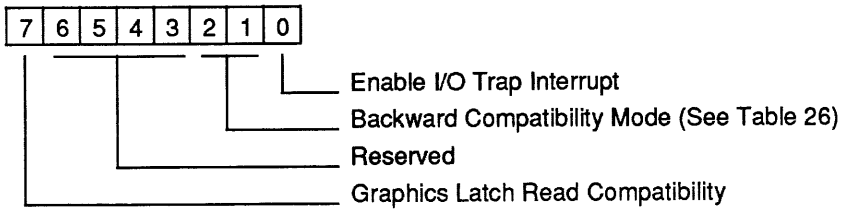
EXTENSION ADDRESS REGISTER
Address = 03DE (Read/Write)



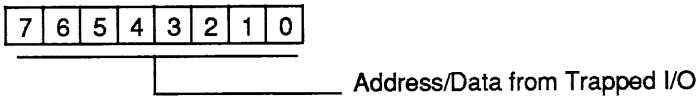
BANDWIDTH CONTROL REGISTER
Address = 03DF Index = D (Read/Write)



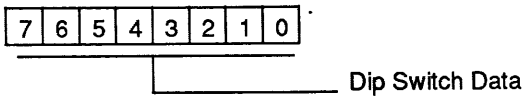
I/O TRAP CONTROL REGISTER
Address = 03DF Index = E (Read/Write)



NMI DATA CACHE REGISTER
Address = 03DF Index = F (Read Only)



DIP SWITCH READ REGISTER
Address = 03DF Index = 10 (Read Only)



AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

I/O READ/WRITE, DAC READ/WRITE, SWITCH READ (See Figures 1, 2, 8, 9 & 10.)

Symbol	Parameter	Min	Max	Units	Conditions
tSU1	Address Setup Time	60	–	ns	
tSU2	ASEL Setup Time	30	–	ns	
tH3	Address Hold Time	0	–	ns	
tH4	ASEL Hold Time	0	–	ns	
t5	Command Pulse Width	200	–	ns	Note
tD6	Write Data Delay	–	80	ns	
tH7	Write Data Hold Time	0	–	ns	
tD8	–EDBUF and –EABUF Delay	–	50	ns	
tD9	Read Data Valid Delay	–	120	ns	
tH10	Read Data Hold Time	10	–	ns	
tD11	Read to DIR Delay	–	45	ns	
tD12	Read to DAC Read Delay	–	50	ns	
tD13	Write to DAC Write Delay	–	50	ns	
tD14	Read to Switch Read Delay	–	40	ns	

Note: 200 ns when VCLK0 = 25 MHz; otherwise, three clocks +80 ns.

5

MEMORY READ/WRITE (See Figures 3 & 4.)

Symbol	Parameter	Min	Max	Units	Conditions
tSU15	Address Setup Time	60	–	ns	
tSU16	ASEL Setup Time	30	–	ns	
tH17	Address Hold Time	0	–	ns	
tH18	ASEL Hold Time	0	–	ns	
tD19	Write Data Delay	–	80	ns	
tH20	Write Data Hold Time	0	–	ns	
tD21	–EDBUF and –EABUF Delay	–	50	ns	
tD22	Read to DIR Delay	–	45	ns	
tD23	Command to CPURDY Low Delay	–	40	ns	
tD24	RD Data from CPURDY High Delay	–	15	ns	
tH25	Valid RD Data Hold Time	–	45	ns	

AC CHARACTERISTICS (Cont.)

DRAM READ/WRITE (See Figures 6 & 7.)

Symbol	Parameter	Min	Max	Units	Conditions
tSU26	Row Address Setup	10	–	ns	
tH27	Row Address Hold Time	.5 tCLK	–	ns	
t28	–RAS Low Time	4 tCLK –10	–	ns	
t29	–RAS High Time	3 tCLK	–	ns	
tSU30	Column Address Setup Time	10	–	ns	
tH31	Column Address Hold Time	tCLK	–	ns	
t32	–CAS Low Time	4.5 tCLK	–	ns	
t33	–CAS High Time	2.5 tCLK –10	–	ns	
tD34	–RAS to –OE Delay	2.5 tCLK –10	–	ns	
tD35	–RAS to –WE Delay	2.5 tCLK –10	–	ns	
tD36	–WE to –RAS High	tCLK	–	ns	
tD37	–RAS to –CAS Reference	1.5 tCLK –10	–	ns	
tSU38	Data to –WE Setup Time	10	–	ns	
tH39	Data to –WE Hold Time	tCLK	–	ns	

CLOCK AND VIDEO (See Figure 5.)

Symbol	Parameter	Min	Max	Units	Conditions
tCLK	CLKIN Cycle	28	–	ns	
tD40	P0-P7 Delay	–	80	ns	
tD41	–BLANK Delay	–	80	ns	
tD42	HSYNC/VSYNC Delay	–	80	ns	
tD43	CLKIN to PCLK Delay	–	60	ns	

TIMING DIAGRAMS

FIGURE 1. I/O READ TIMING

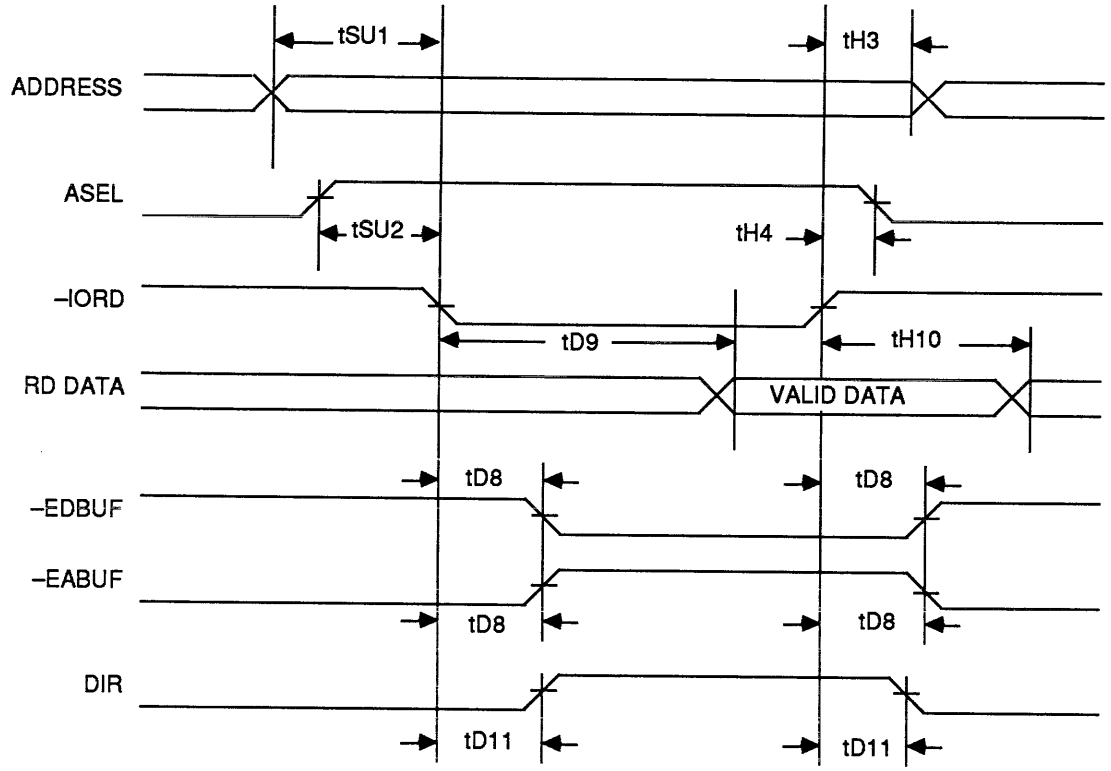


FIGURE 2. I/O WRITE TIMING

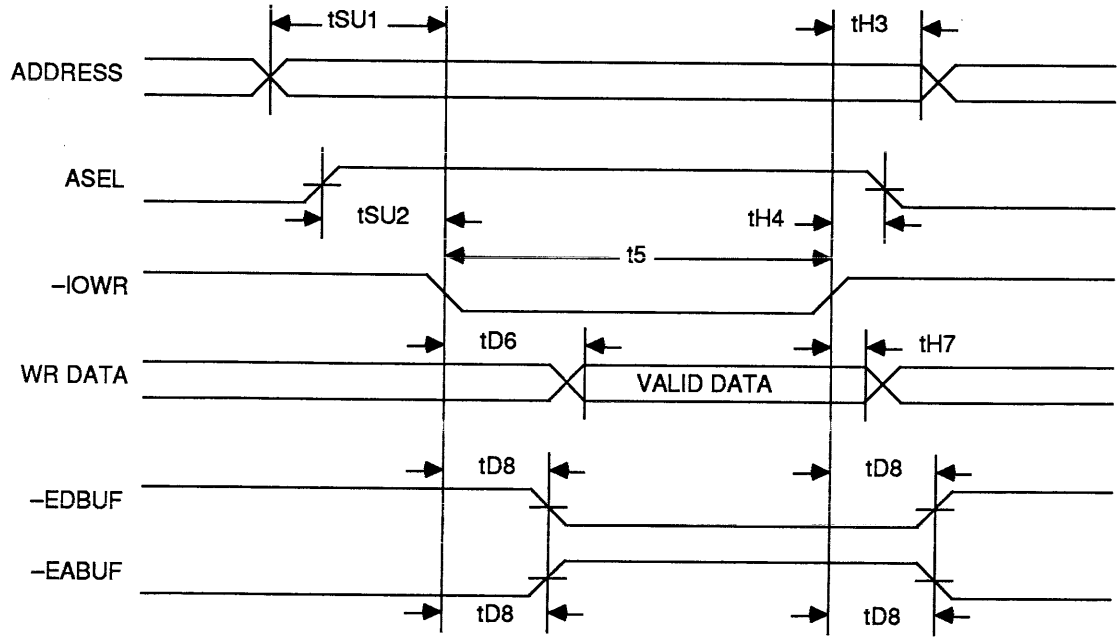


FIGURE 3. MEMORY READ TIMING

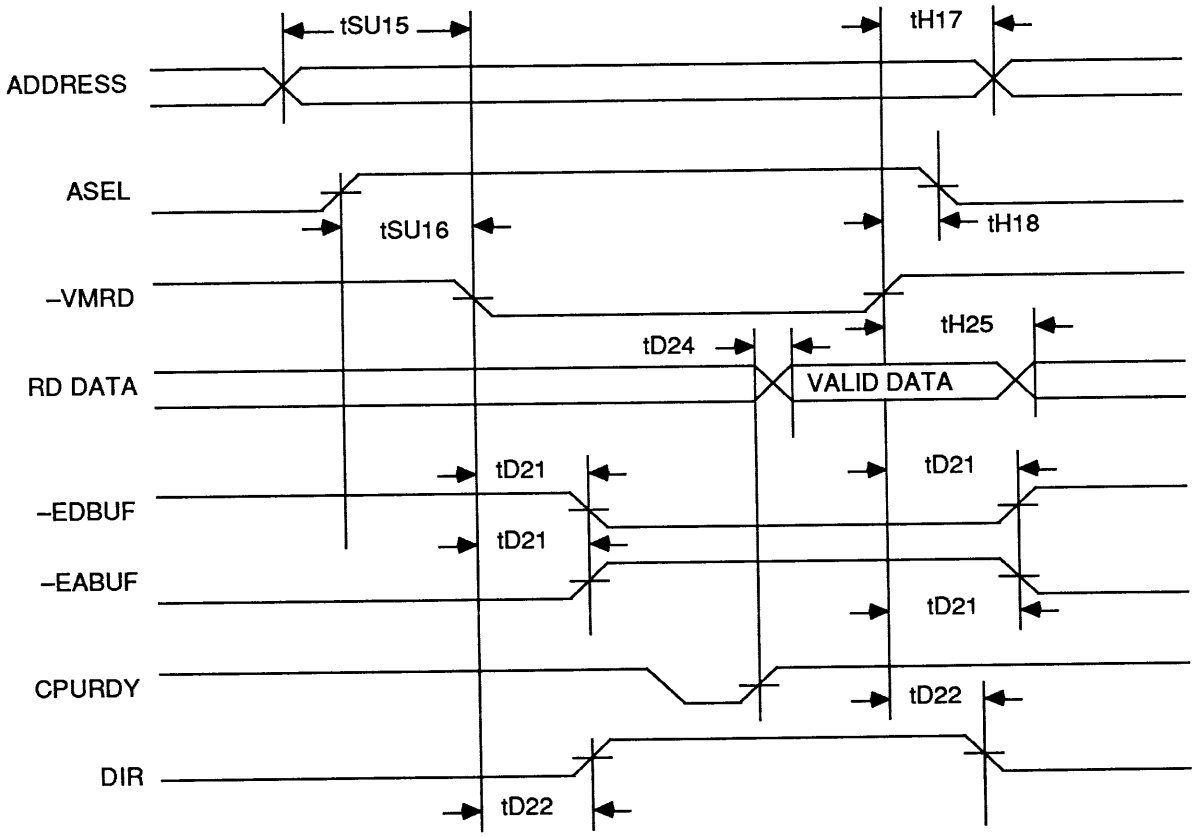


FIGURE 4. MEMORY WRITE TIMING

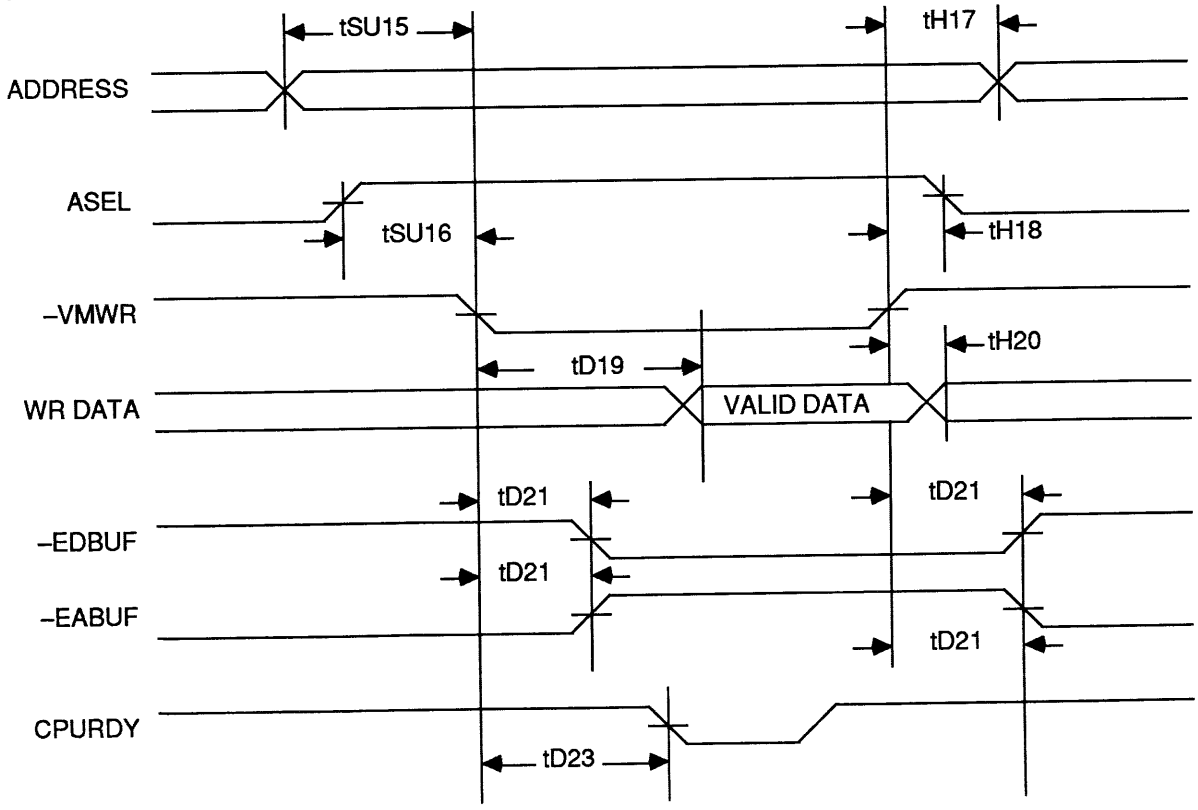


FIGURE 5. CLOCK AND VIDEO TIMING

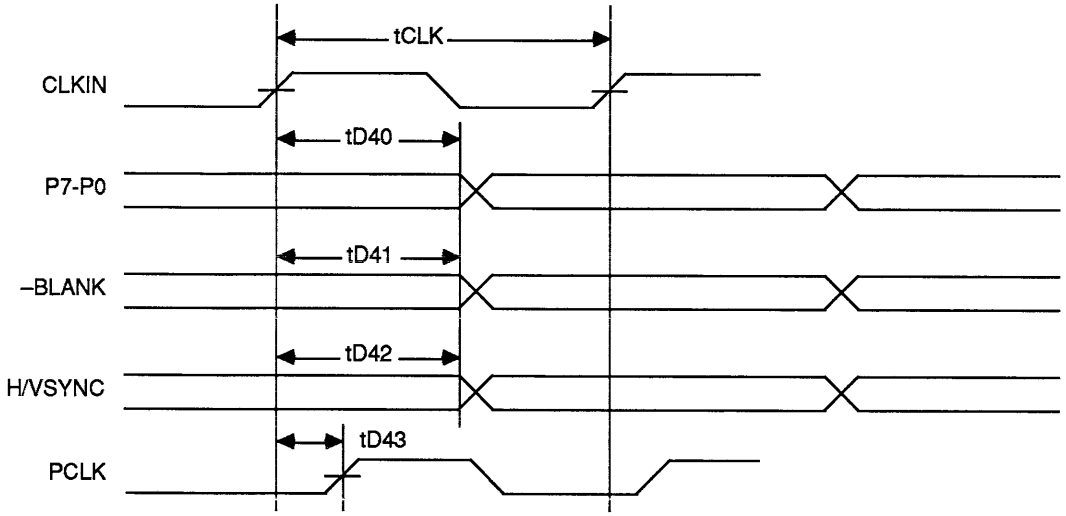


FIGURE 6. DRAM READ TIMING

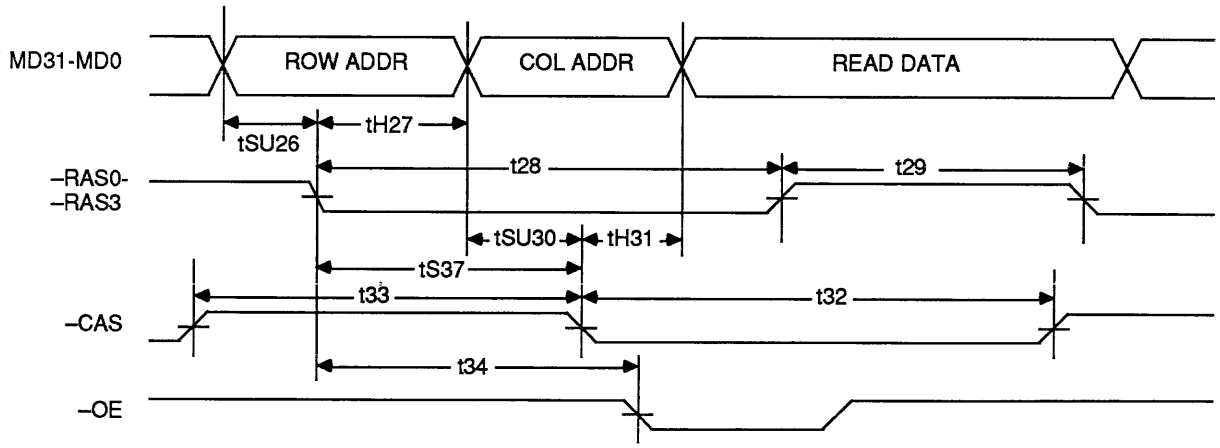


FIGURE 7. DRAM WRITE TIMING

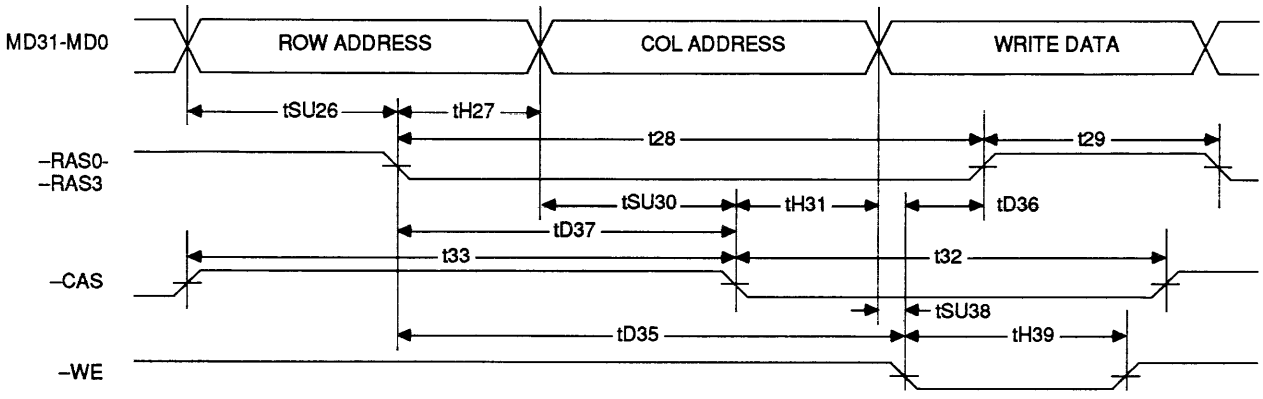


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FIGURE 8. DAC READ TIMING

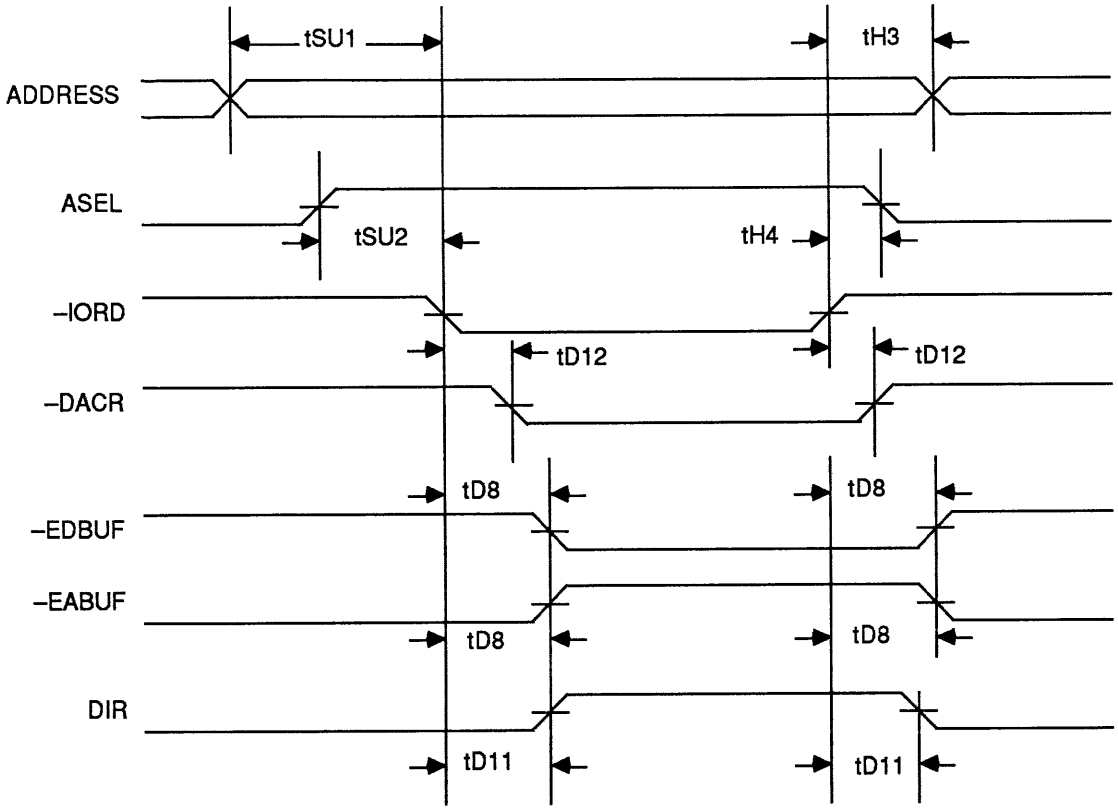


FIGURE 9. DAC WRITE TIMING

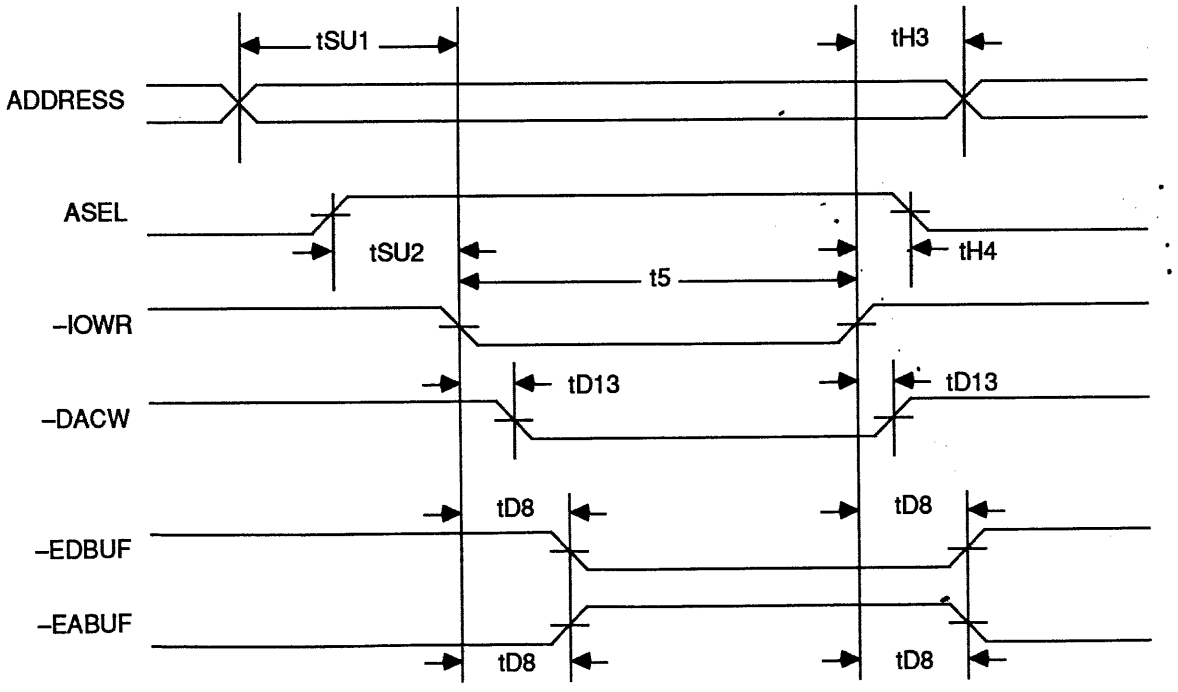
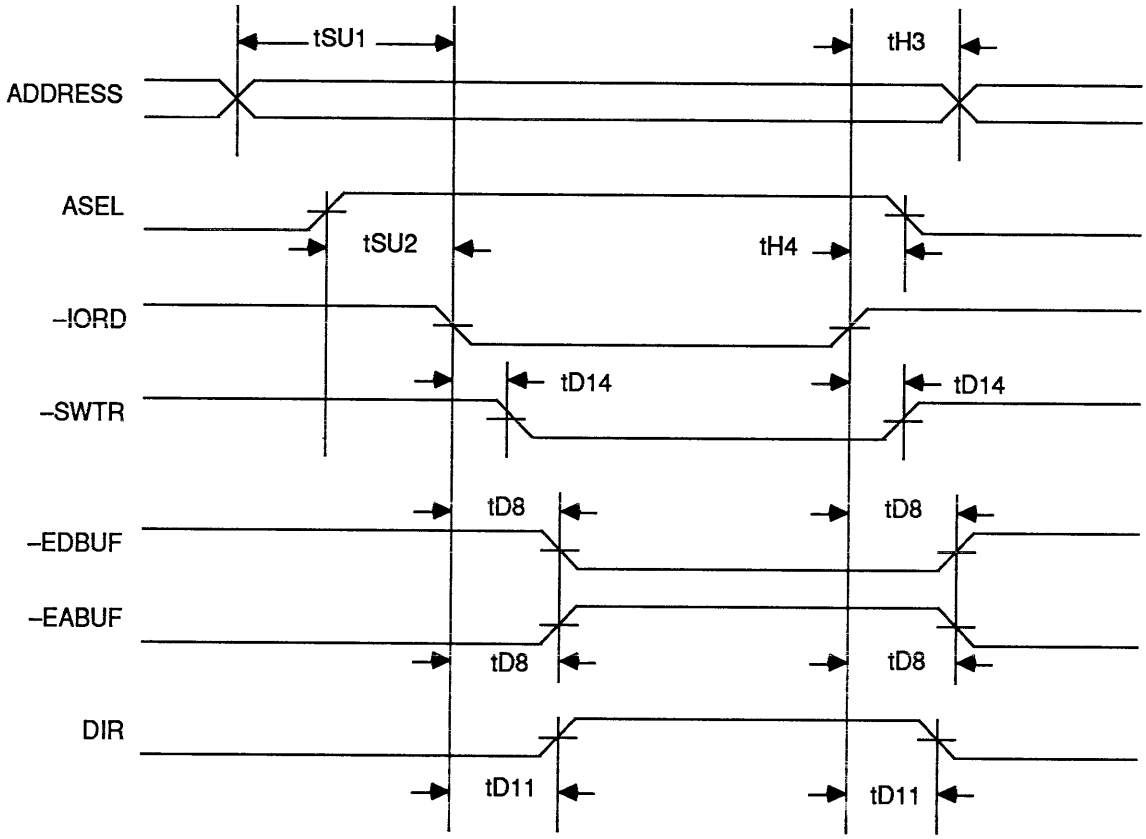


FIGURE 10. SWITCH READ TIMING



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–40°C to +125°C
Supply Voltage to Ground Potential	–0.5 V to VCC +6.0 V
Applied Input Voltage	–0.5 V to VCC +0.5 V
DC Input Current	± 20 mA
Lead Temperature	300°C

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Units	Conditions
VIH	Input High Voltage	2.0	VCC	V	VCC = 5.25 V
VIL	Input Low Voltage	–0.5	0.8	V	VCC = 5.25 V
VOH	Output High Voltage	2.4	–	V	IOH (See Note 2)
VOL	Output Low Voltage	–	0.4	V	IOL (See Note 1)
IIN	Input Leakage Current	–10	10	µA	VIN = VCC/GND
IOZ	3-State Output Leakage Current	–10	10	µA	VOUT = VCC/GND
IDD	IDD Dynamic Current	–	80	mA	VCC = 5.25 V

Note 1: 2 mA Output Pads: –EABUF, –EDBUF, DIR, –CRTINT, –NMI, CPURDY, –SWTR, HSYNC, VSYNC, –BLANK, –DACR, –DACW, PCLK
4 mA Output Pads: P7-P0, DA7-DA0, MD31-MD0.
8 mA Output Pads: –RAS0—RAS3, –WE
12 mA Output Pads: –OE
20 mA Output Pads: –CAS

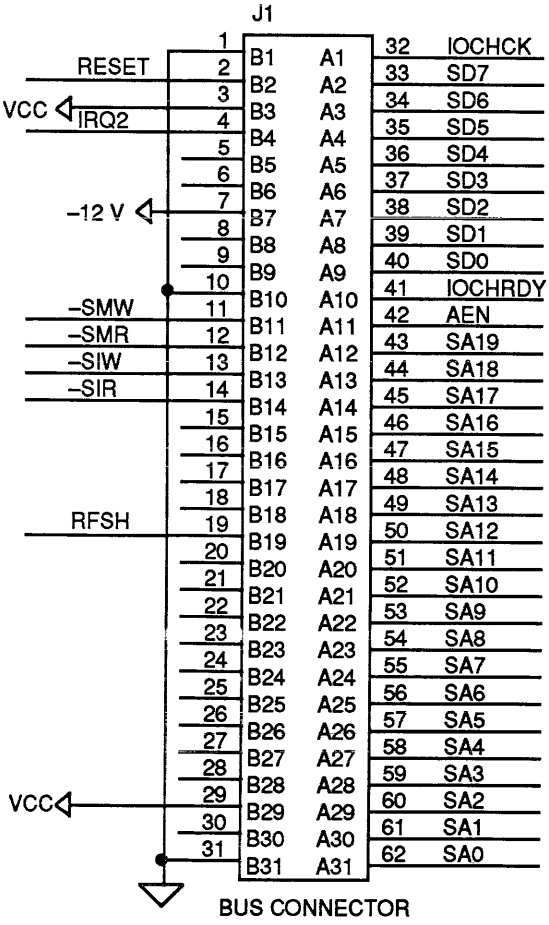
Note 2: –200 µA Output Pads: –EABUF, –EDBUF, DIR, –CRTINT, –NMI, CPURDY, –SWTR, HSYNC, VSYNC, –BLANK, –DACR, –DACW, P7-P0, DA7-DA0, MD31-MD0, PCLK
–1 mA Output Pads: –RAS0, –RAS1, –RAS2, –RAS3, –WE
–3.3 mA Output Pads: –OE, –CAS

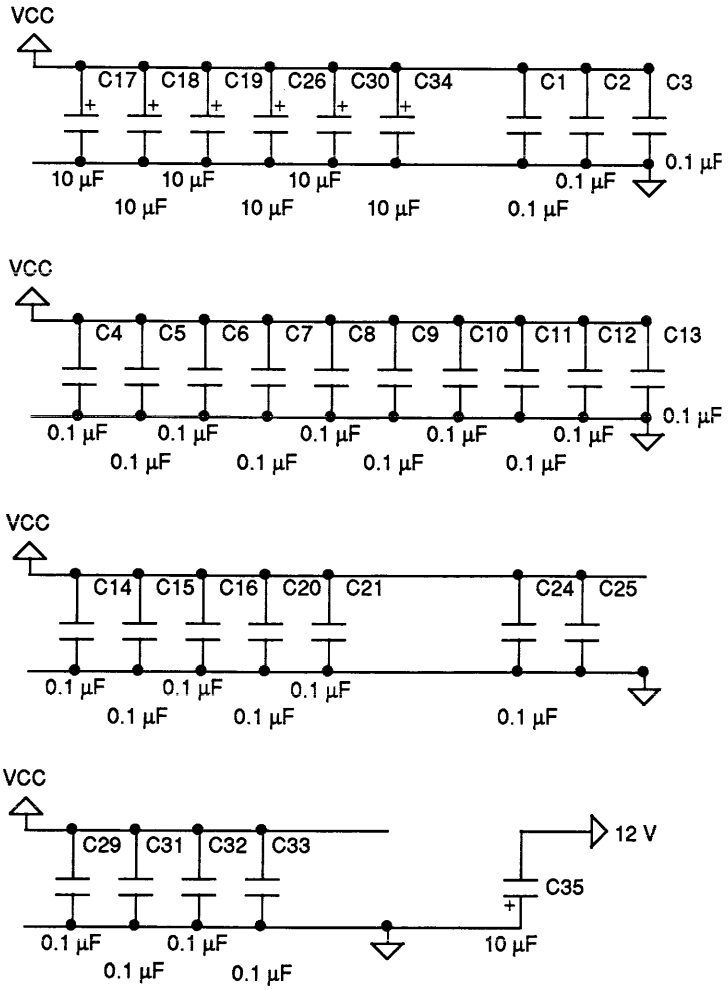
VGA ADD-ON CARD

VLSI Logic Products group has made available an XT-compatible evaluation board for the VL82C037. The board has a 15-pin connector for connecting a stand VGA analog monitor, and a 9-pin connector for connecting older style digital monitors. The DIP switch bank is used to configure the board for the type of monitor being used, according to the following table:

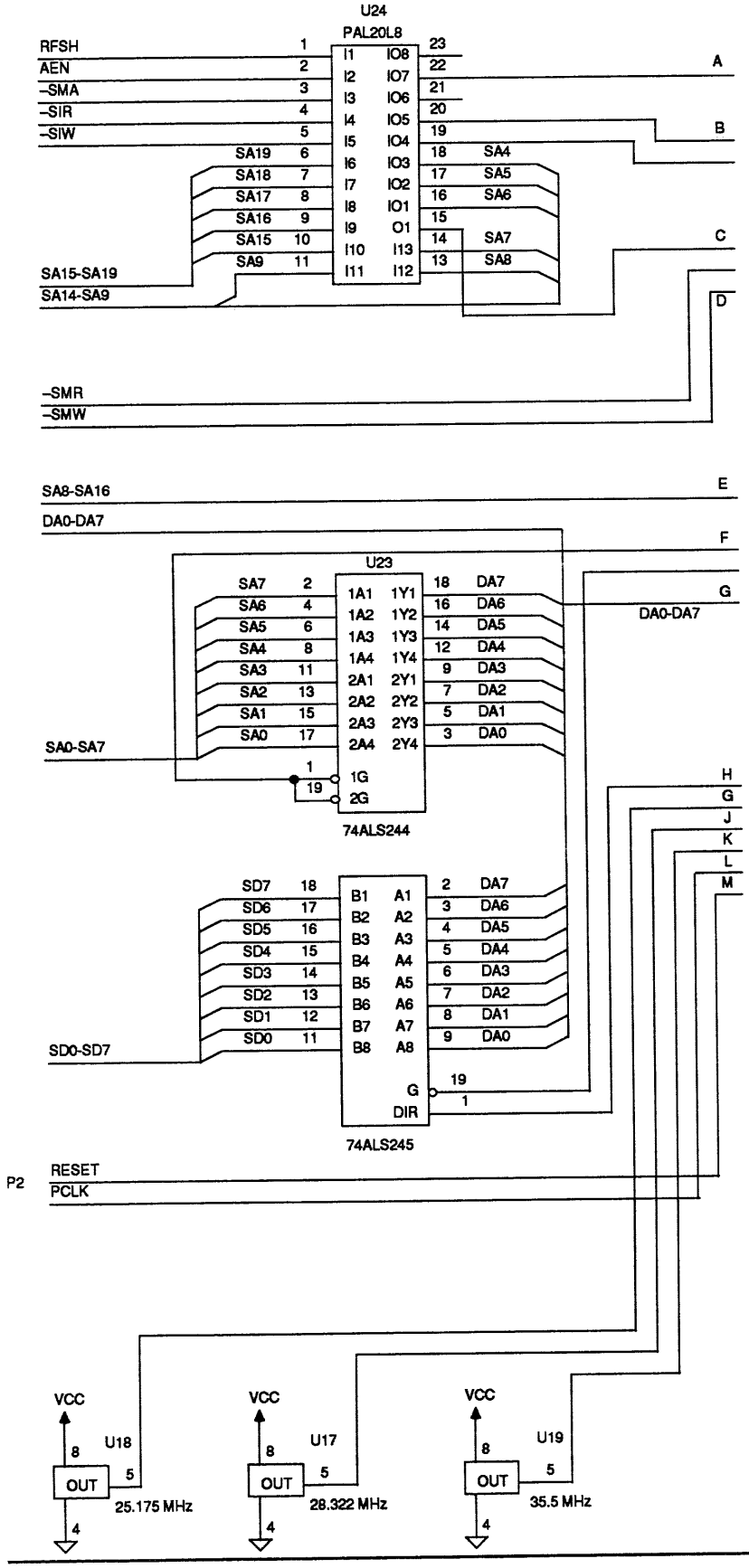
The board is capable of supporting non-standard video modes which can be set using a program called VGAMODE.EXE, which is available on request. The non-standard text modes supported are 132 columns by 25 rows, and 132 columns by 43 rows. The 132 x 43 mode requires a high speed multisync monitor. The 800 x 600 16 color graphics mode requires 100 ns DRAMs and a 36 MHz clock, and is not supported on this board. Other software is available which demonstrates hardware panning and a 160 column by 50 row text display mode.

SW4	SW3	SW2	SW1	MONITOR
off	x	x	x	IBM Analog Monitor (Mono or Color)
on	off	off	off	Digital Monochrome
on	off	off	on	Digital CGA
on	off	on	off	Digital EGA
on	off	on	on	NEC MultiSync or Compatible (Analog)
on	on	off	off	NEC MultiSync Plus (Analog)
on	on	off	on	Reserved
on	on	on	off	Reserved
on	on	on	on	Reserved

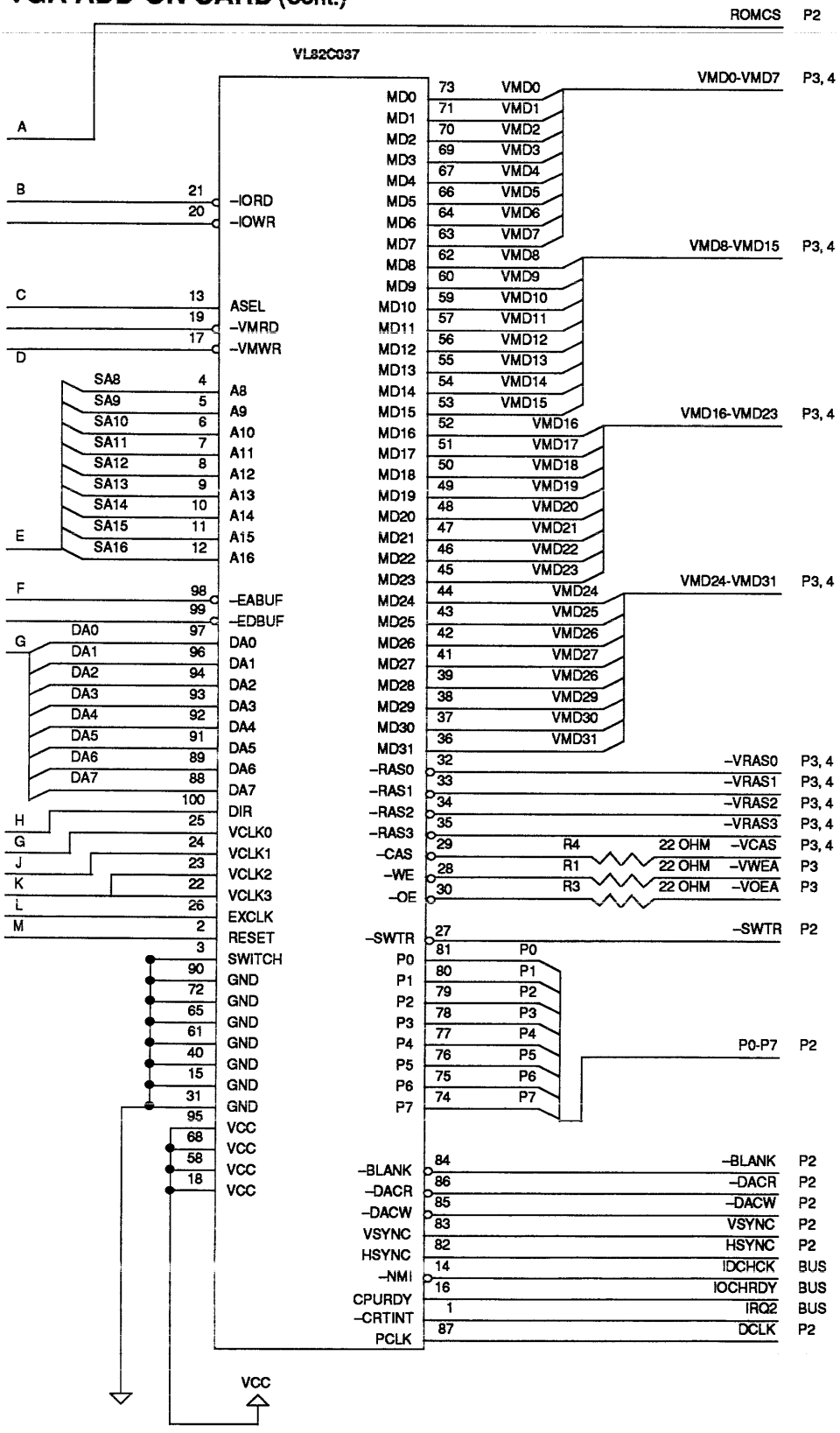




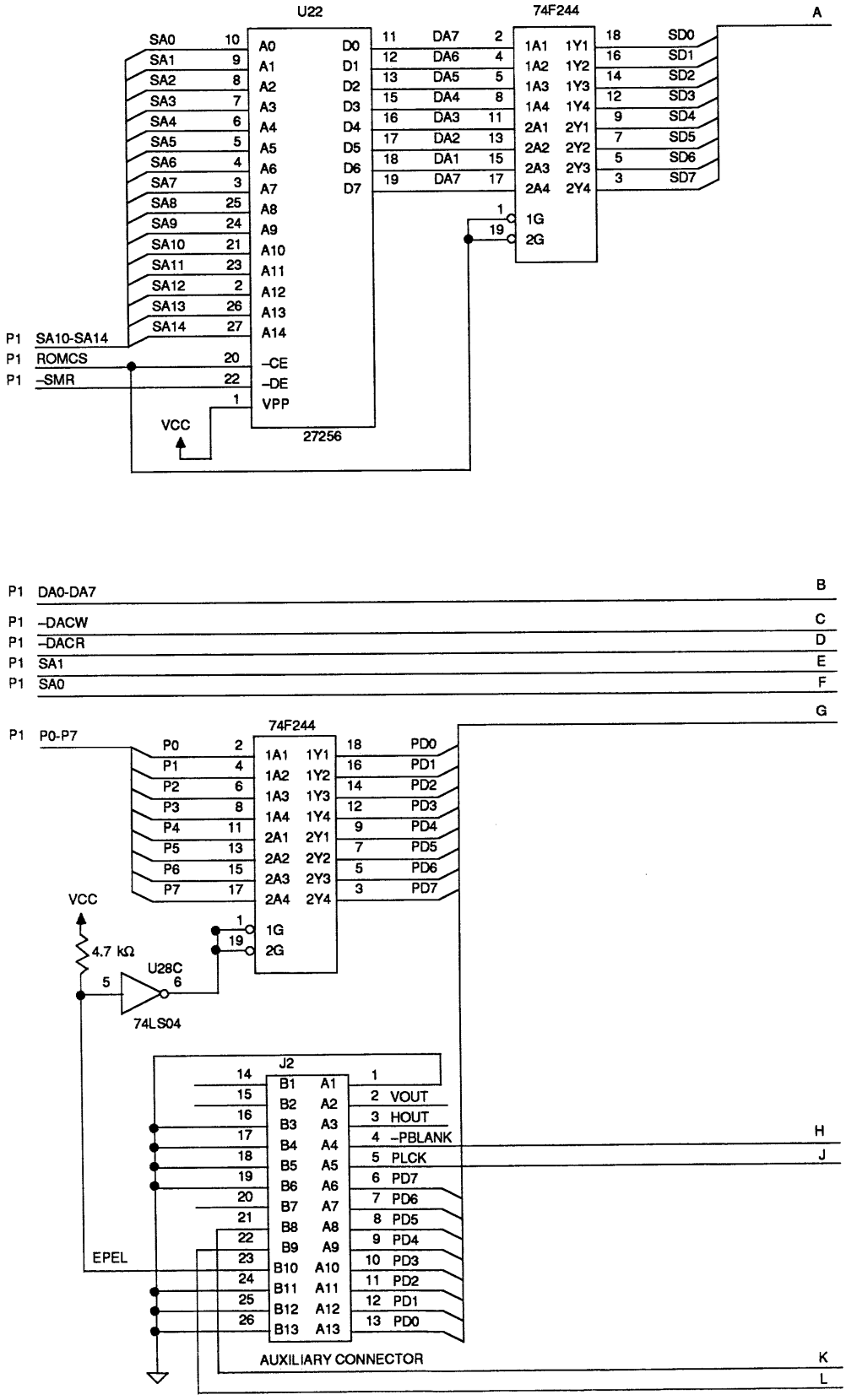
VGA ADD-ON CARD (Cont.)



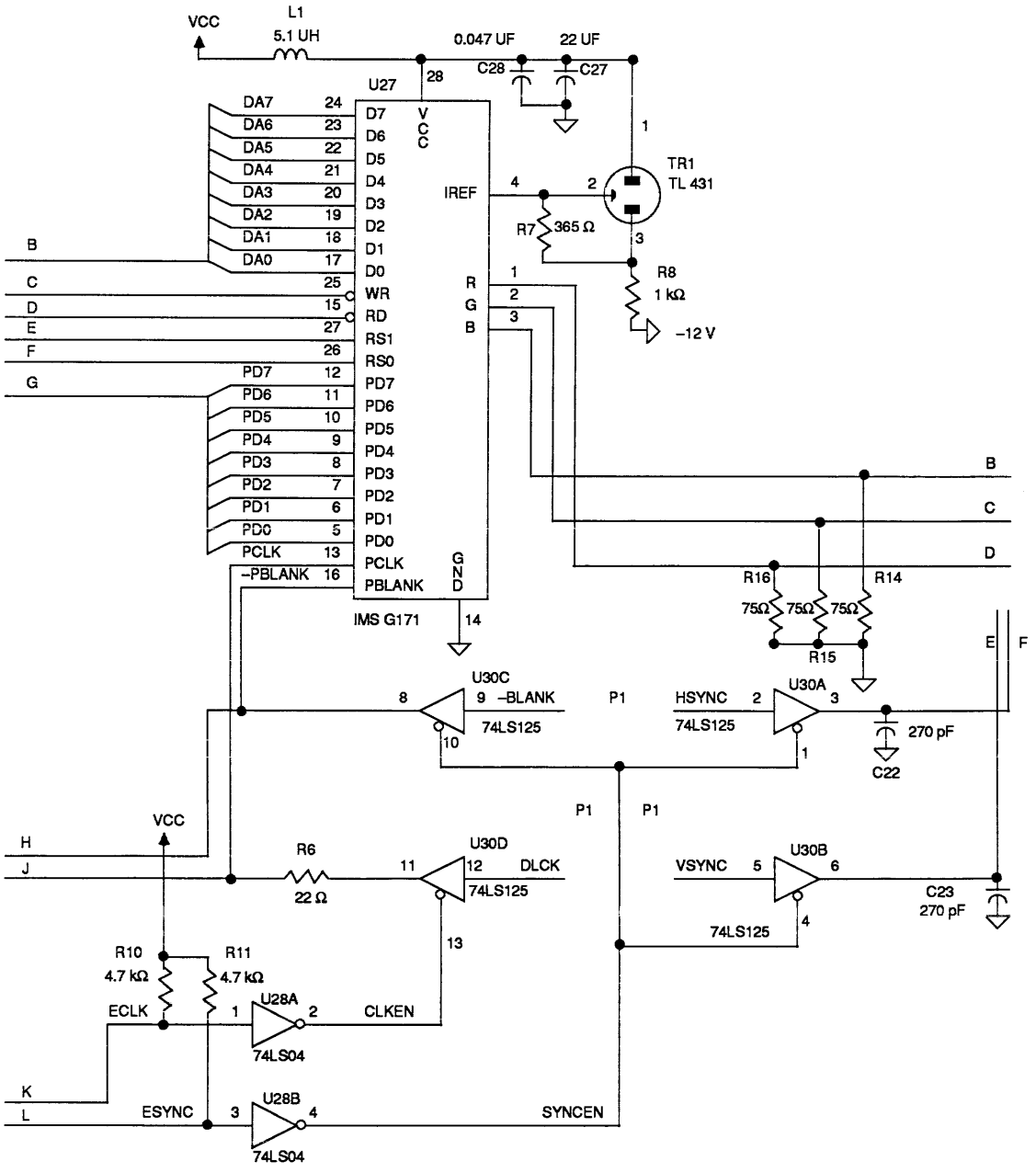
VGA ADD-ON CARD (Cont.)



VGA ADD-ON CARD (Cont.)

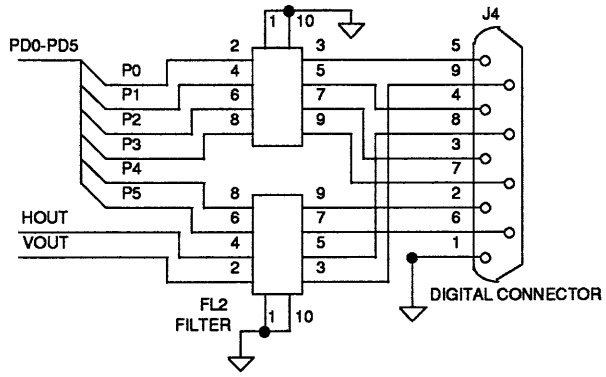


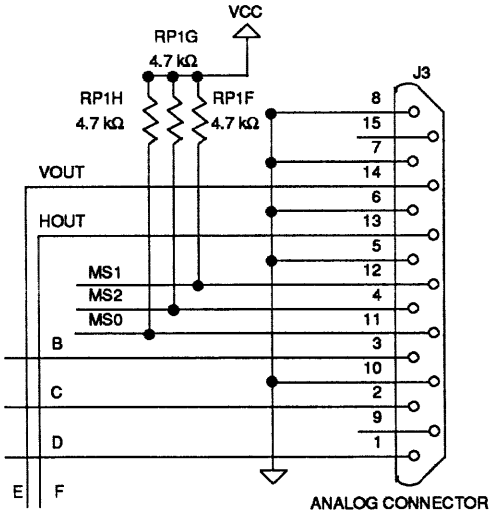
VGA ADD-ON CARD (Cont.)

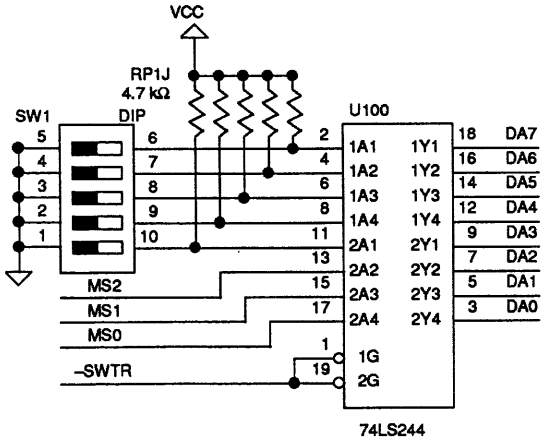


VGA ADD-ON CARD (Cont.)

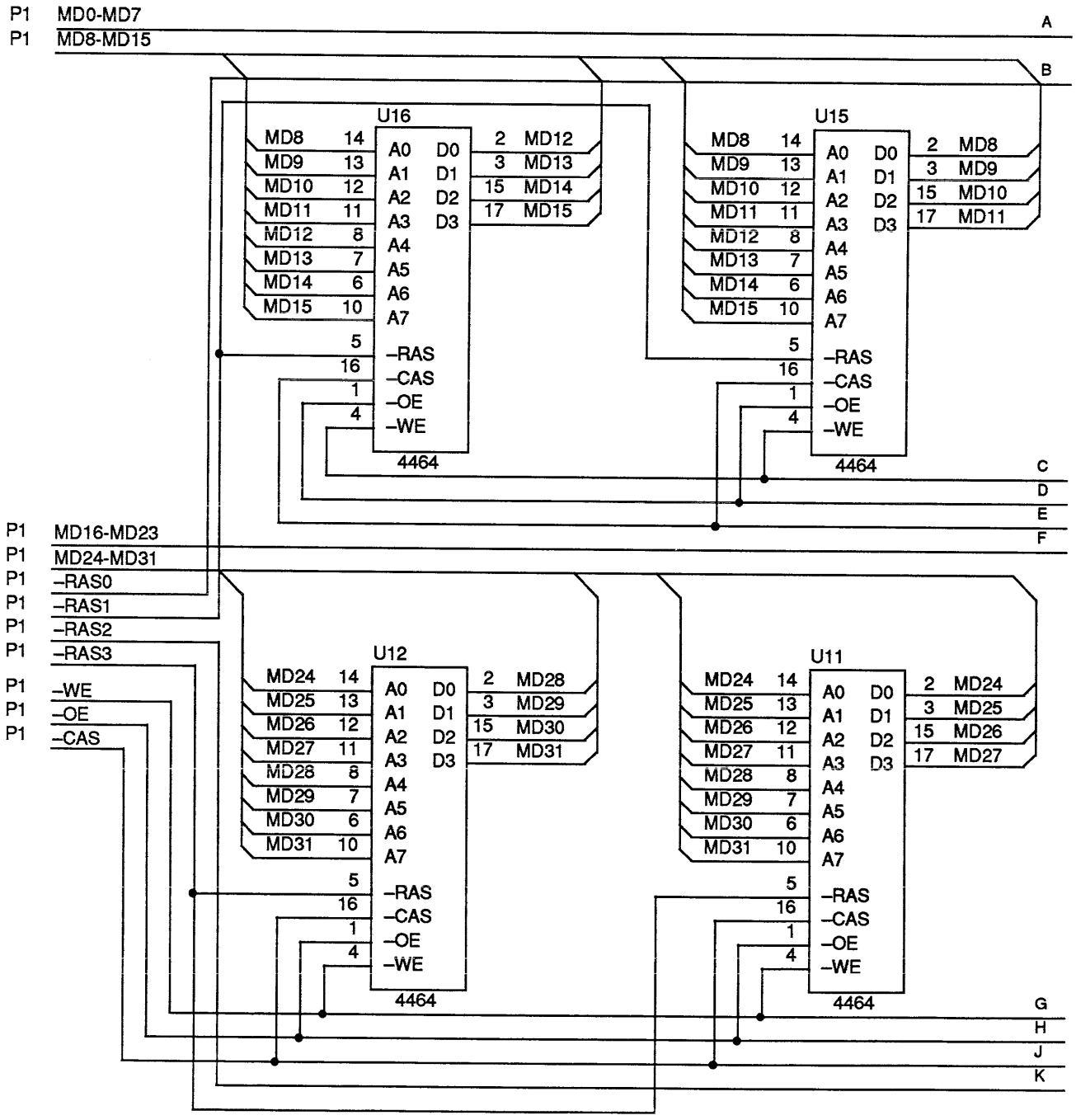
A SD0-SD7 P1



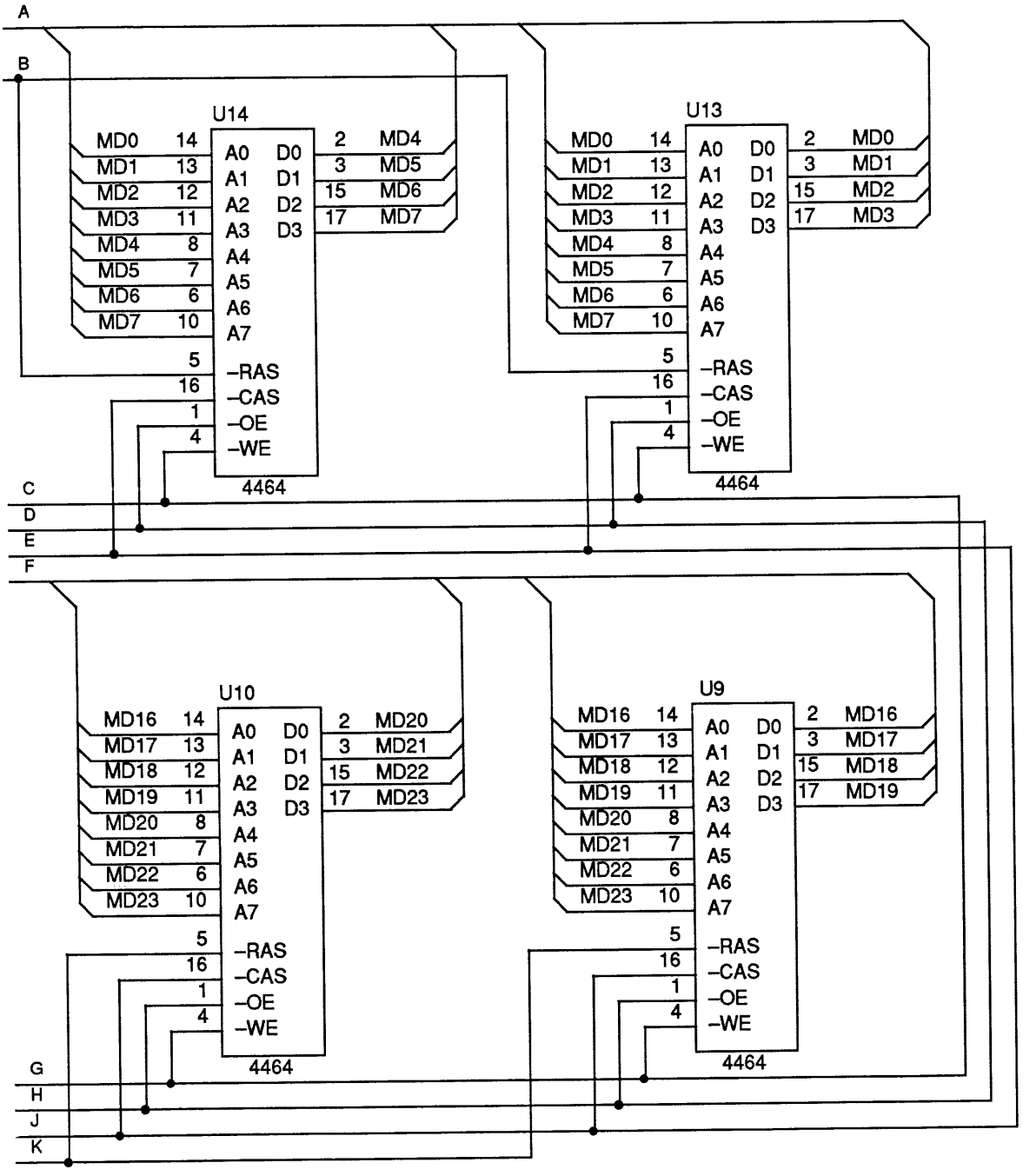




VGA ADD-ON CARD - FIRST BANK OF MEMORY



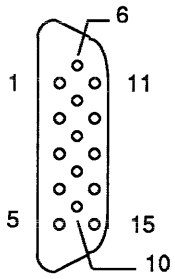
VGA ADD-ON CARD - FIRST BANK OF MEMORY (Cont.)



DISPLAY CONNECTOR

Analog Monitor Connector

—> 15-pin D-shell Display Connector

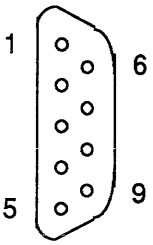


Pin Number	I/O	Output	Monochrome	Color
1	O	Red	No Pin	Red
2	O	Green	Mono	Green
3	O	Blue	No Pin	Blue
4	NA	Reserved	No Pin	No Pin
5	NA	Digital G	Self Test	Self Test
6	NA	Red Rtn	Key Pin	Red Rtn
7	NA	Green Rtn	Mono Rtn	Green Rtn
8	NA	Blue Rtn	No Pin	Blue Rtn
9	NA	Plug	No Pin	No Pin
10	NA	Digital G	Digital G	Digital G
11	NA	Reserved	No Pin	Digital G
12	NA	Reserved	Digital G	No Pin
13	O	HSYNC	HSYNC	HSYNC
14	O	VSYNC	VSYNC	VSYNC
15	NA	Reserved	No Pin	No Pin

Note: Red Rtn, Green Rtn, Blue Rtn = Analog Grounds
Digital G = Digital ground for sync returns and self test

Digital Monitor Connector

—> 9-pin D-shell Display Connector



Pin Number	Signal Description
1	Ground
2	Secondary Red
3	Primary Red
4	Primary Green
5	Primary Blue
6	Secondary Green/Intensity
7	Secondary Blue/Mono Video
8	Horizontal Retrace (Hsync)
9	Vertical Retrace (Vsync)

AUXILIARY VIDEO CONNECTOR

Pin Number	Signal Description
A1	Ground
A2	VSYNC
A3	HSYNC
A4	Blank
A5	PCLK
A6	P7
A7	P6
A8	P5
A9	P4
A10	P3
A11	P4
A12	P1
A13	P0
B1	Reserved
B2	Reserved
B3	Ground
B4	Ground
B5	Ground
B6	Ground
B7	Reserved
B8	ECLK
B9	ESYNC
B10	EPEL
B11	Ground
B12	Ground
B13	Ground

PARTS LIST

Resistors

Description	Quantity	Discrete
22 Ohm	4	R1, R3, R4, R6
75 Ohm	3	R14, R15, R16
365 Ohm	1	R7
1K Ohm	1	R8
4.7K Ohm	3	R10, R11, R12

Resistor Network

Description	Quantity	Discrete
4.7K Ohm 10-Pin	1	RP1

Capacitors

Description	Quantity	Discrete
0.1 µF DCAP	17	C8, C9, C10, C11, C12, C13, C14, C15, C16, C20, C21, C24, C25, C29, C31, C32, C33
10 µF TCAP	7	C17, C18, C19, C26, C30, C34, C35
0.047 µF DCAP	1	C28
270 pF DCAP	2	C22, C23

Semiconductors

Description	Quantity	Discrete
74ALS245	1	U29
74ALS244	1	U23
74LS244	2	U26, U100
74F244	1	U25
4464-10 DRAM	8	U9, U10, U11, U12, U13, U14, U15, U16
OTI-036/ IMS G171 DAC	1	U27
27256-200 EPROM	1	U22
PAL20L8-15	1	U24
VL82C037	1	U21

Crystal Oscillators

Description	Quantity	Discrete
25.175 MHz	1	U18
28.322 MHz	1	U17
35.5 MHz	1	U19

Connectors

Description	Quantity	Discrete
15-Pin D-shell	1	J3
9-Pin D-shell	1	J4

Miscellaneous

Description	Quantity	Discrete
TL431 Volt. Regulator	1	TR1
10-Pin RC Network	2	FL1, FL2
5.1 µH Inductor	1	L1
4-position DIP Switch	1	SW1

PAL EQUATION (FOR THE ADD-ON CARD)

A 15 ns 20L8 PAL is required for interface between bus connector and VGA chip. The equation of the PAL is listed below.

PAL20L8
VGA BOARD

```
/RFSH AEN /SMRN /SIRN /SIWN SA19 SA18 SA17 SA16 SA15 SA9 GND
SA8 SA7 /ASEL SA6 SA5 SA4 /IOWR /IORD /SEL0 /ROMCS NC VCC

SEL0 = SA19 * /SA18 * SA17 * /RFSH +
       SA9 * SA8 * SA7 * SA6 * /SA5 * /RFSH * /AEN * SIWN +
       SA9 * SA8 * SA7 * SA6 * /SA5 * /RFSH * /AEN * SIRN +
       SA9 * SA8 * SA7 * /SA6 * SA5 * SA4 * /RFSH * /AEN * SIWN +
       SA9 * SA8 * SA7 * /SA6 * SA5 * SA4 * /RFSH * /AEN * SIRN
ASEL = /SEL0
ROMCS = SA19 * SA18 * /SA17 * /SA16 * /SA15 * /RFSH * SMRN
IORD = SIRN * /AEN
IOWR = SIWN * /AEN
```