Data Sheet

NVIDIA nForce4 Ultra
Media and Communications Processor

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PLATFORM PROCESSORS

Document Change History

Version	Date	Responsible	Reason for Change
01	8/04	DV, JK, SR, GM, RC, JM, AK, MH	• Initial release
01.1	08/04	DV, JK	• Updated DC Current Characteristics
02	09/04	DV, JK, JM, SR, TT	• Minor edits • Removed PCI_GMT0# as a strapping pin
02.1	11/04	JK, DV	• through ±0.6V • Table 39: Changed Absolute Ratings maximum power dissipation from TBD to 13 W.
02.2	11/04	JK, DV	• TRST# must be pulled down to GND for normal operation.
02.3	11/18/04	MS	• AC'97 Interface: updated 20-bit 48 kHz input streams to 16 bit
02.4	12/09/04	JK, DV	• TCO timer is disabled in SAFE mode
02.5	02/28/05	JK, DV	• Updated PCI Express features list to include PCI Express Specification 1.0a compliance

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About this Document

This document is targeted towards motherboard designers and is intended to provide them with the information necessary to design an NVIDIA® nForce™ motherboard. It contains a detailed features list, signal description, power and system management description, signal states, GPIO signals, power sequencing and RESET information, package information, AC/DC specifications, and the ball map. Please note that the information contained in this document is under NDA and is preliminary and subject to change.

Chapter 1. Introduction

The NVIDIA® nForce™4 Ultra media and communications processor (MCP) is a single-chip, highly integrated, high-performance HyperTransport peripheral controller. It has a ×16, two ×1 and one ×2 or ×1 PCI Express interfaces. It has a 16 × 16 HyperTransport interface to an AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs processor, four Serial-ATA 2 (SATA 2) interfaces, NVIDIA MAC with either RGMII or MII, dual ATA-133 interfaces, ten USB2.0 ports, audio/modem, and support for five PCI slots. These interfaces support the NVIDIA processor bridge functionality for next-generation PCs using the AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPUs. The level of integration and functionality offered by the NVIDIA nForce4 Ultra media and communications processor is unmatched by any other single chip-device controller.

Product Overview

The NVIDIA nForce4 Ultra integrates the following features:

- HyperTransport ×16 up and down links at up to 1.0 GHz to the AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU
- Four separate and independent PCI Express controllers with a total of 20 lanes
  - Configured as either
    - One ×16, two ×1, and one ×2 PCI Express lanes
    - One ×16 and three ×1 PCI Express lanes
- PCI 2.3 interface
  - Supports up to five PCI slots with dedicated REQ/GNT pairs
- Two separate SATA 2 (Gen 1 and Gen 2) controllers with integrated PHYs, each supporting two drives in master mode
- IEEE 802.3 NVIDIA MAC for 1000BASE-T/100BASE-T/10BASE-T Gigabit/Fast Ethernet/Ethernet
  - RGMII for Gigabit/Fast Ethernet/Ethernet
    OR
  - MII for Fast Ethernet/Ethernet
- USB 2.0 EHCI and USB 1.1 OHCI
  - Supports up to ten ports

- Fast ATA-133 IDE controller
  - Primary and secondary interfaces each supporting master and slave configuration
- Dual SMBus 2.0 interfaces
- AC '97 2.3 interface
  - Supports standard and enhanced audio functionality
  - Supports S/PDIF pass-through function
- LPC bus 1.0 compatible interface
- Integrated AT legacy controllers
- Integrated clock synthesizer with spread spectrum capability
- System and power management
- AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU power sequencing protection logic
- 31 mm × 31 mm, 1 mm ball pitch PBGA

System and Block Diagram

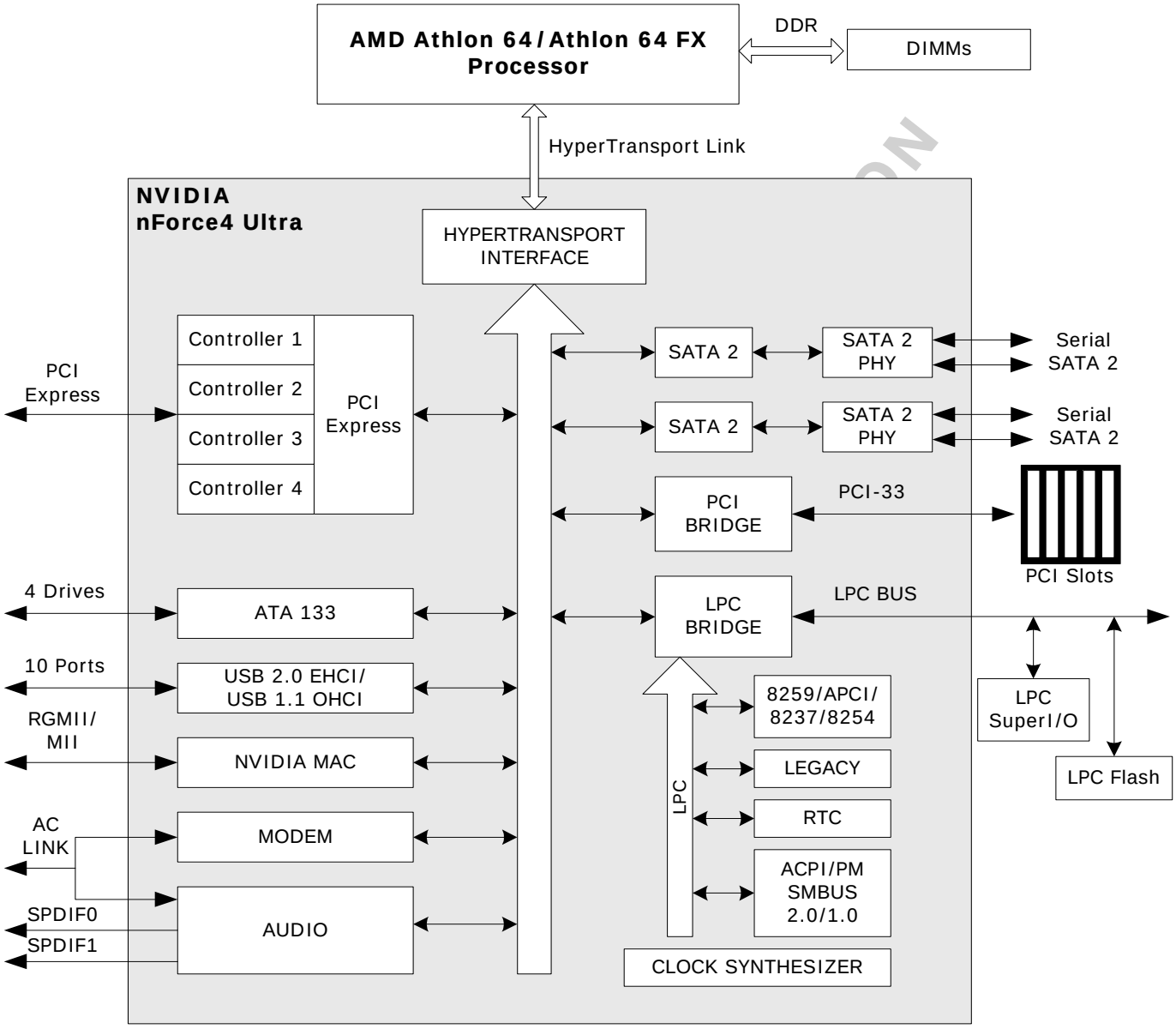

Figure 1. System and Block Diagram

Features and Functions

HyperTransport Link to AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU

- High-speed, differential, low voltage interface
- Communication with the AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU
- ×16 up and ×16 down links
- Up to 1.0 GHz for a total bandwidth of 8.0 GT/s
- Supports coherent and non-coherent data types
- Supports isochronous and non-isochronous data channels
- Supports real-time link reconnect/disconnect
- Clock spread spectrum capability

PCI Express Interface

- Four separate PCI Express controllers with 20 total lanes that can be configured as either
  - One ×16, one ×2, and two ×1 PCI Express lanes
  - One ×16 and three ×1 PCI Express lanes
- ×16 controller supports isochronous data
- WAKE# function is supported for power management
- 2.5 GHz support for a total bandwidth of 2.5 Gb/s per direction per lane
- Clock spread spectrum capability
- PCI Express Specification 1.0a compliant

PCI Interface

- PCI 2.3 compliant
- 5 V tolerant
- Supports five external PCI slots at 33 MHz
  - Supports five PCI REQ/GNT pairs
  - Supports five bus master arbitrations
- PCI master and slave interfaces
- Supports both master-initiated and slave-initiated terminations
- Bidirectional write posting support for concurrency
- Flexible routing of all PCI interrupts
- Supports read ahead—memory read line (MRL) and memory read multiple (MRM)
- Supports **PCI_CLKRUN#** functionality

- Clock spread spectrum capability

Fast ATA 133 IDE Controller

- 5V-tolerant primary and secondary interfaces
  - Each interface supports two devices (master and slave) for a total of four devices
- Industry-standard PCI bus master IDE (BM-IDE) register set
  - Compliant with Microsoft BM-IDE drivers
- Supports UltraDMA modes 6–0 (UltraDMA-133/100/66/33)
- Supports standard PIO modes 4-0
- Supports standard DMA modes 2-0
- Supports scatter-gather function

Integrated Serial ATA 2 (SATA 2) Gen 1 and Gen 2 Interface

- Two separate SATA 2 compliant controllers with PHYs
  - Each controller supports two drives in master mode for a total of four
  - PHYs are compliant with Gen1i (1.5 Gb/s) and Gen2i (3.0 Gb/s) electrical requirements defined in the SATA 2 specification
- Achieves higher performance at lower CPU utilization
- Compliant with ATA/ATAPI-7 Volume 3 Serial ATA standards
- High speed, low voltage, low pin count
- Each channel can operate at 1.5 Gb/s or 3.0 Gb/s independently from the other channels
- Supports full Tag and Native Command Queuing
- Supports power-down capabilities
- Supports SATA ATAPI devices
- Clock spread spectrum capability

USB 2.0 EHCI and USB 1.1 OHCI

- USB 2.0 Enhanced Host Controller Interface (EHCI) and USB 1.1 Open Host Controller Interface (OHCI) controllers
- Supports transfer rates at high speed (480 Mb/s), full speed (12 Mb/s), and low speed (1.2 Mb/s)
- Dynamically configures slower devices for best utilization of bandwidth
- High-speed devices default to EHCI
- Full speed and low speed devices automatically delegated to OHCI
- Allows USB concurrency
- Five over-current protection
  - Can be configured in any grouping

IEEE 802.3 NVIDIA MAC

- Ethernet Carrier Sense Multiple Access/Collision Detect (CSMA/CD)
- Compliant with IEEE 802.3-2002 (RGMII for connectivity to Gigabit Ethernet PHYs or MII for connectivity to Fast Ethernet/Ethernet PHYs)
  - Configured through a strapping option
- Hardware-based support for unicast, multicast, and broadcast address
- Individual transmit and receive FIFOs support efficient scatter-gather dual channel DMA operations with unlimited burst read/write operations for reduced latency
  - Reduces number of indications on receive
- Accepts multiple frames on transmit
- Supports auto-negotiation of link speed and duplex setting through the external RGMII or MII PHY
- Supports WoL and Preboot Execution Environment (PXE)
- Supports 1000BASE-T/100BASE-T/10BASE-T Gigabit/Fast Ethernet/Ethernet PHYs through RGMII or 100BASE-T/10BASE-T Fast Ethernet/Ethernet PHYs through MII
- Support for Ethernet jumbo frames (up to 9018 bytes)
- Supports 100/10 Mb/s Fast Ethernet/Ethernet full duplex and half duplex operation
- Supports 1000 Mb/s Gigabit Ethernet full duplex operations
- Support for IP, TCP, and UDP checksum offloads
- Support for TCP segmentation offload (also known as large send offloads)
  - TCP segmentation offload up to 64 KB of packet size
  - Supports TCP segmentation over IPv4 or IPv6
  - Supports TCP segmentation over Gigabit Ethernet jumbo frames
  - Supports Tx and Rx checksum offload over IPv4
- Supports IEEE802.1p traffic prioritization specification
- Supports IEEE802.1Q specification to enable VLAN
- Microsoft TCP Chimney compliant
- Supports ACPI 2.0 and PCI PMI 1.1
  - Supports all wake-up events for OnNow! (WoL) – link status, pattern matching, and magic packet

NVIDIA Firewall

- ICSA certified
- Desktop stateful and stateless firewall including support for IPv4 and IPv6
- Prevents outgoing packets with spoofed IP source addresses
- Prevents ARP spoofing attacks
- Ability to restrict MAC from going into promiscuous mode
- Ability to prevent from acting as a DHCP server
- Ability to drop UDP-over-IPv4 packets that either have invalid or null checksums
- Automatically maps application to port, for ease of use and better support for games
- Stateful firewall capabilities in hardware for improved performance
- Deep PPPOE parsing for better support of some DSL modems
- Logging/configuration capabilities

Network Management (NetMgmt)

- CLI command line configuration tool (useful for automated batch file tasks)
- Web-based configuration/monitoring (available locally or remotely through the use of the integrated web server)
- WMI (Windows Management Instrumentation) support. Users can write scripts to configure any parameters
- Secure remote management through Web-based interfaces

Dual SMBus 2.0 Interface

- Supports System Management Bus (SMBus) host and slave
- Supports Address Resolution Protocol (ARP)
- Supports embedded controller (EC)

AC '97 Interface

- AC '97 2.3 compliant
  - Supports analog audio codecs for eight, six, four, and two channels.
  - Supports 20-bit 48 kHz fixed and variable rate audio analog codecs
  - Accepts independent 16-bit 48 kHz input streams from primary and secondary codecs
  - Accepts independent MIC_IN and primary LINE_IN streams from two separate codecs
- Enhanced AC '97 2.3 mode (AC '97+)
  - Supports enhanced eight-channel audio by means of a secondary S/PDIF output (SPDIF1) to a secondary two-channel analog audio codec

- Two front channels are driven by a 24-bit 96 kHz codec connected to SPDIF1
- Remaining six channels are driven by a standard AC '97 20-bit 48 kHz primary analog audio codec

- Supports S/PDIF out (SPDIF0) pass-through function without an external analog audio codec
  - SPDIF0 provides 24-bit output data at 48 kHz or 96 kHz
  - Provides either compressed data or PCM (pulse code modulation) data
- Supports S/PDIF over AC '97
- AC-link supports two simultaneous codecs, audio (AC) and modem (MC)
  - AC/AC '97 codec (primary/secondary)
  - AC/MC '97 codec (primary)
  - MC/AC '97 codec (secondary)
- Supports input, output, and GPIO channels for host-based modems
- Separate independent functions for audio and modem
- Independent DMA controllers for primary audio-in, secondary audio-in, audio-out, SPDIF0-out, SPDIF1-out, primary MIC-in, secondary MIC-in, modem-in, and modem-out
  - The DMA controllers supports 32-bit addressing and scatter-gather functionality
- Supports double rate audio (DRA) for high-end audio up to 96 kHz audio stereo implementation with no modem present
  - Support provided for front left, front right, and center signals only
  - All other signals remain at 48 kHz
- Compliant with *PCI PMI Revision 1.1*

LPC 1.0-Compatible Interface

- Low Pin Count 1.0-compatible interface
- Integrated LPC bridge
- Subtractive decode
- LPC DMA mastering
  - Supports two LPC DMA masters
- Serial interrupt protocol support

Integrated AT Legacy Controllers

- Legacy AT support including all AT-compatible registers
- Interrupt control
  - Dual 8259 Programmable Interrupt Controllers (PICs) supports 15 interrupts
  - 82093-compatible I/O Advanced Programmable Interrupt Controller (APIC) supports 24 interrupts

- PCI interrupt routing and masking
- Independent edge/level triggered interrupts
- Interrupt sharing for all internal devices

- DMA control
  - Dual 8237 supports seven independently programmable channels
  - Standard page registers allow 24-bit addressing
- 8254 programmable interval timer counter based on 14.31818 MHz clock
- MC146818A/DS12887-compatible RTC with 256 byte battery backed-up RAM

Integrated Clock Synthesizer

- Generates all necessary internal and external clock frequencies
  - Based on a single 25 MHz crystal
  - Generates clocks for HyperTransport link, PCI Express, AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU, PCI, LPC, IDE, AC '97, SuperI/O, SATA 2, MAC, and USB 2.0
- Spread spectrum capable on the following clocks: CPU, HyperTransport link, PCI Express, PCI, and Serial ATA 2 clocks
- Simplifies system design and motherboard layout

System and Power Management

System Management

- Wired for Management (WfM) and Wake on LAN (WoL) support
- Total Cost of Ownership (TCO) features
  - TCO timer, processor presence detection, and intruder detection
  - CPU clock frequency control, function disable, and legacy disable

Power Management

- Supports instantly available PC (IAPC), ACPI 2.0, and PCI PM 1.1
- PME# detection
- SMI# generation
- Clock generator control
- CPU power state control
- Multiplexed and individually configurable GPIO pins
- Thermal event detection (alarm)
- Power On Suspend (POS) or ACPI S1 support
- Suspend to RAM (STR) or ACPI S3 support
- Suspend to Disk (STD) or ACPI S4/S5 support
- Supports C0, C1, C2, and C3 states

High Precision Event Timer

This is a Microsoft-mandated timer to enable accurate timing of multimedia streams. High Precision Event Timer (HPET) was formerly known as the multimedia timer.

- Three comparator design
- 32-bit precision counter
- One periodic and two one-shot interrupt sources

Watchdog Timer

Required for Microsoft .NET server operating system.

Chapter 2.
Signal Descriptions

This chapter contains the signal descriptions for the NVIDIA nForce4 Ultra. See Appendix A for signal listings by ball location and signal name and Appendix B for the ballout.

This chapter contains the following information:

- Signal Descriptions
  - Conventions
  - HyperTransport 16 × 16 interface to AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU
  - CPU interface
  - PCI Express ×16 interface
  - PCI Express interface
  - PCI Express shared interface
  - PCI 2.3 interface
  - Integrated SATA 2 interface
  - NVIDIA MAC interface
    - RGMII interface for Gigabit/Fast Ethernet/Ethernet
    - MII interface for Fast Ethernet/Ethernet
  - USB 2.0/1.1 interface
  - Dual SMBus interfaces
  - Dual ATA-133 IDE interfaces
    - Shared interface
    - Primary IDE interface
    - Secondary IDE interface
  - AC '97 interface
  - LPC interface
  - Clock interface
  - System and power interfaces
  - Power supply interface
  - Miscellaneous interface
  - GPIO interface

- AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU power sequencing balls
- Mobile function interface
- Transmeta interface
- JTAG interface
- Strapping/Test balls

Signal Descriptions

Conventions

Following are the conventions used in describing the signals for the NVIDIA nForce4 Ultra:

- Signal Names
  Signal names use a mnemonic to represent the function of the signal. Active low signals are identified by a pound sign (#) after the signal name. Active high signals do not have the pound sign (#) after the signal names.
- I/O Type
  The signal I/O type is represented as a code to indicate the operational characteristics of the signal. Table 1 lists the I/O codes used in the signal description tables.

Table 1. Signal Type Codes

Item	Description
A	Analog
DIFF I/O	Differential input/output
DIFF IN	Differential input
DIFF OUT	Differential output
I	Input
I/O	Bidirectional input/output
O	Output
OC	Open collector output
OD	Open drain output
P	Power

Note: Signals can appear in more than one interface.

HyperTransport x16 Interface to AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU

Table 2. HyperTransport x16 Interface Signals to AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs

Signal	I/O	Definition
HT_REQ#	I	**HyperTransport Link Request** This asynchronous input low signal indicates that an external master wishes to send a transaction upstream and the HyperTransport link should be reconnected. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
	I/O	**GPIO_10** When **HT_REQ#** is not selected, it becomes **GPIO_10.**
HT_RXCLK[1:0] **HT_RXCLK[1:0]#**	DIFF IN	**HyperTransport Link Differential Receive Clocks** These signals are the differential pairs used as the timing reference for **HT_RXD[15:0]** and **HT_RXCTL**. **HT_RXCLK1/HT_RXCLK1#** is used for **HT_RXD[15:8]** and **HT_RXCLK0/HT_RXCLK0#** is used for **HT_RXD[7:0]** and **HT_RXCTL**.
HT_RXCTL **HT_RXCTL#**	DIFF IN	**HyperTransport Link Differential Receive Control** Receive link control signal.
HT_RXD[15:0] **HT_RXD[15:0]#**	DIFF IN	**HyperTransport Link Differential Receive Data** These signals are the differential pairs used to receive the high-speed 16 bits of information from the AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU.
HT_STOP#	OD	**HyperTransport Link Disconnect** This signal enables and disables the HyperTransport link during system state transitions. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
HT_TXCLK[1:0] **HT_TXCLK[1:0]#**	DIFF OUT	**HyperTransport Link Differential Transmit Clocks** These signals are the differential pairs used as the timing reference for **HT_TXD[15:0]** and **HT_TXCTL**. **HT_TXCLK1/HT_TXCLK1#** is used for **HT_TXD[15:8]** and **HT_TXCLK0/HT_TXCLK0#** is used for **HT_TXD[7:0]** and **HT_TXCTL**. These clock pairs are spread spectrum capable for EMI reduction.
HT_TXCTL **HT_TXCTL#**	DIFF OUT	**HyperTransport Link Differential Transmit Control** Transmit link control signal.
HT_TXD[15:0] **HT_TXD[15:0]#**	DIFF OUT	**HyperTransport Link Differential Transmit Data** These signals are the differential pairs used to transmit the high-speed 16 bits of information to the AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU.
HT_CAL_GND1	A	**HyperTransport Calibration 1** Used for HyperTransport Link interface pads calibration. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
HT_CAL_GND2	A	**HyperTransport Calibration 2** Used for HyperTransport Link interface pads calibration. Please refer to the *nForce4 (CrushK8-04) Design Guide*.

CPU Interface

Table 3. CPU Interface Signals

Signal	I/O	Definition
A20GATE	I	**A20 Gate** This signal is an input from the keyboard controller (SuperI/O). This signal is not +5V tolerant.
	I/O	**GPIO_40** When **A20GATE** is not selected, it becomes **GPIO_40**.
CPU_COMP	A	**CPU Interface Compensation** Used for CPU interface pads calibration. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
CPU_PWROK	OD	**CPU Power OK** This signal is the Power Good/Cold Reset control for the AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
CPU_RST#	OD	**CPU Reset** This signal is the warm reset signal control for the AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
THERMTRIP#	I	**CPU Thermal Trip Point Exceeded** This signal is generated from the AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU indicating that it is shutting down to avoid damaging itself. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
	I/O	**GPIO_26** When **THERMTRIP#** is not selected, it becomes **GPIO_26**.

PCI Express x16 Interface

Table 4. PCI Express x16 Interface Signals

Signal	I/O	Definition
PE0_PRSNT#	I	**PCI Express x 16 Presence Detect** This signal is the hot plug presence detect of a device on the ×16 PCI Express link.
PE0_REFCLK **PE0_REFCLK#**	DIFF OUT	**PCI Express x16 Reference Clock** These signals are the 100 MHz differential reference clock pair for the ×16 PCI Express link.
PE0_RX[15:0] **PE0_RX[15:0]#**	DIFF IN	**PCI Express x16 Receive Data** These signals are the ×16 differential receive data pairs of the PCI Express link.
PE0_TX[15:0] **PE0_TX[15:0]#**	DIFF OUT	**PCI Express x16 Transmit Data** These signals are the ×16 differential transmit data pairs of the PCI Express link.

PCI Express Interface

Table 5. PCI Express1 x1 Interface Signals

Signal	I/O	Definition
PE1_PRSNT#	I	**PCI Express x1 Presence Detect** This signal is the hot plug presence detect of a device on a ×1 PCI Express link.
PE1_REFCLK **PE1_REFCLK#**	DIFF OUT	**PCI Express x1 Reference Clock** These signals are the 100 MHz differential reference clock pair for the first ×1 PCI Express link.
PE1_RX **PE1_RX#**	DIFF IN	**PCI Express x1 Receive Data** These signals are the ×1 differential receive data pair of the first ×1 PCI Express link.
PE1_TX **PE1_TX#**	DIFF OUT	**PCI Express x1 Transmit Data** These signals are the ×1 differential transmit data pair of the first ×1 PCI Express link.

Table 6. PCI Express2 x1 Interface Signals

Signal	I/O	Definition
PE2_PRSNT#	I	**PCI Express x1 Presence Detect** This signal is the hot plug presence detect of a device on a ×1 PCI Express link.
PE2_REFCLK **PE2_REFCLK#**	DIFF OUT	**PCI Express x1 Reference Clock** These signals are the 100 MHz differential reference clock pair for the second ×1 PCI Express link.
PE2_RX **PE2_RX#**	DIFF IN	**PCI Express x1 Receive Data** These signals are the ×1 differential receive data pair of the second ×1 PCI Express link.
PE2_TX **PE2_TX#**	DIFF OUT	**PCI Express x1 Transmit Data** These signals are the ×1 differential transmit data pair of the second ×1 PCI Express link.

Table 7. PCI Express3 x 2 Interface Signals

Signal	I/O	Definition
PE3_PRSNT#	I	**PCI Express x2 Presence Detect** This signal is the hot plug presence detect of a device on a ×2 PCI Express link. **Note**: This signal is also the hot plug presence detect of a device on a ×1 PCI Express link in a ×1 configuration.
PE3_REFCLK **PE3_REFCLK#**	DIFF OUT	**PCI Express x2 Reference Clock** These signals are the 100 MHz differential reference clock pair of the ×2 PCI Express link. **Note**: These signals are also the 100 MHz differential reference clock pair of the third ×1 PCI Express link in a ×1 configuration.
PE3_RX **PE3_RX#**	DIFF IN	**PCI Express First of Two of the x2 Receive Data** These signals are the first of two differential receive data pairs of the ×2 PCI Express link. **Note**: These signals are also the third x1 differential receive data pair of the x1 PCI Express link in a x1 configuration.
PE3_TX **PE3_TX#**	DIFF OUT	**PCI Express First of Two of the x2 Transmit Data** These signals are the first of two differential transmit data pairs of the ×2 PCI Express link. **Note**: These signals are also the third x1 differential transmit data pair of the ×1 PCI Express link in a ×1 configuration.
PE4_RX **PE4_RX#**	DIFF IN	**PCI Express Second of Two of the x2 Receive Data** These signals are the second of two differential receive data pairs of the ×2 PCI Express link. **Note**: When a ×1 configuration is used, then these signals are not used and can be left unconnected.
PE4_TX **PE4_TX#**	DIFF OUT	**PCI Express Second of Two of the x2 Transmit Data** These signals are the second of two differential transmit data pairs of the ×2 PCI Express link. **Note**: When a ×1 configuration is used, then these signals are not used and can be left unconnected.

PCI Express Shared Interface

Table 8. PCI Express Shared Interface Signals

Signal	I/O	Definition
PECLK_COMP_GND	A	**PCI Express Clock Bias Control** Used to provide the current reference for the PCI Express clock driver. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
PE_REFCLK_IN **PE_REFCLK_IN#**	DIFF IN	**PCI Express Reference Clock** This differential reference clock pair can be use for all the 100 MHz PCI Express reference clocks.
PE_RST#	O	**PCI Express RESET** This signal provides a reset signal to the PCI Express bus. It must be asserted 100 ms after the power to the PCI Express slots have stabilized. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
PE_WAKE#	I	**PCI Express Wake** This signal is used as the PCI Express Wake Event interrupt signal.

PCI Interface

Table 9. PCI Bus Interface Signals

Signal	I/O	Definition
PCI_AD[31:0]	I/O	**PCI Address/Data Bus** A bus transaction consists of an address phase followed by one or more data phases. When **PCI_FRAME#** is asserted (first clock of a PCI transaction), the physical address (32 bits) is driven. During subsequent clocks, data is driven or received.
PCI_C/BE#[3:0]	I/O	**PCI Command/Byte Enables** During the address phase of a transaction, these signals define the PCI bus command. During the data phase, these signals are used as the byte enables corresponding to the supplied/requested data. The byte enables are valid for the entire data phase and determine which byte lanes contain valid data.
PCI_CLK[5:0]	O	**PCI Output Clocks** These signals are the six in-phase 33 MHz PCI bus clock outputs. Five of these signals (**PCI_CLK[4:0]**) are intended for the five external PCI slots and one (**PCI_CLK5**) for the loop-back to the NVIDIA nForce4 Ultra. They provide the timing reference for all transactions on the PCI bus. **PCI_CLK5** is used as the feedback clock back into the NVIDIA nForce4 Ultra. These clocks are spread spectrum capable to reduce EMI. All **PCI_CLKn** are spread together. They are not independently controlled.
PCI_CLKFB	I	**PCI Clock Feedback In** This signal is **PCI_CLK5** that is looped back into the NVIDIA nForce4 Ultra to be used internally. The trace length of this signal must match the other **PCI_CLKn** signals. Please refer to the *nForce4 (CrushK8-04) Design Guide.*

Signal	I/O	Definition
PCI_CLKRUN#	I/O	**PCI Clock Run** This signal is used in conjunction with the logic that stops the external **PCI_CLKn** signals. It is compliant with the PCI Mobile Design Guide Specification for **PCI CLK** management. It is mainly used in mobile applications. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
	I/O	**GPIO_9** This is the secondary function of this pin and must be configured as a GPIO on power up for desktop applications. When **PCI_CLKRUN#** is not selected, it becomes **GPIO_9**.
PCI_DEVSEL#	I/O	**PCI Device Select** When acting as an output, this signal indicates that the NVIDIA nForce4 Ultra has decoded the PCI address and is claiming the current access as the target. As an input, it indicates whether any other device on the bus has accepted the current transaction that was initiated by the NVIDIA nForce4 Ultra.
PCI_FRAME#	I/O	**PCI Frame** This signal is driven by the current master to indicate the beginning and duration of an access. It is asserted to indicate that a bus transaction is beginning and that it is in the address phase. Data transfers can continue while it is asserted (bursting). When it is de-asserted, the transaction is in the final data phase.
PCI_GNT[4:0]#	O	**PCI Bus Grants** These signals are asserted by the NVIDIA nForce4 Ultra to grant the PCI bus to a requesting PCI bus master device. Each external device has a dedicated grant line. Only one of these signals may be active at any given time. **PCI_GNT0#** must always be paired with **PCI_REQ0#**, **PCI_GNT1#** must always be paired with **PCI_REQ1#**, and so on.
	I/O	**GPIO_[46,17,8]** When **PCI_GNT[4:2]#** is not selected, it becomes **GPIO_[46,17,8].**
PCI_INT[Z:W]#	I	**PCI Bus Interrupts** These signals are generated by a PCI device in any of the five external PCI slots to indicate that it needs service.
PCI_IRDY#	I/O	**PCI Initiator Ready** This signal indicates the initiator's ability to complete the current data phase of the transaction. It is asserted from the first clock cycle after **PCI_FRAME#** is asserted to the last clock cycle of the PCI transaction. It is used in conjunction with **PCI_TRDY#**. Data is transferred on each **PCI_CLK[5:0]** in which both **PCI_IRDY#** and **PCI_TRDY#** are sampled asserted. Wait states are inserted until both **PCI_IRDY#** and **PCI_TRDY#** are asserted together. During a write cycle**, PCI_IRDY#** indicates the NVIDIA nForce4 Ultra has valid data on **PCI_AD[31:0]**. During a read cycle, it indicates the NVIDIA nForce4 Ultra is ready to latch data.
PCI_PAR	I/O	**PCI Parity** This signal is the even-parity bit generated across **PCI_AD[31:0]** and **PCI_C/BE#[3:0]**. It is stable and valid one clock after the address phase. It is stable and valid one clock after each write data phase. It is stable and valid one clock after each read phase is completed.
PCI_PERR#	I/O	**PCI Parity Error** This signal is driven by an external PCI device when it receives data that has parity error. The NVIDIA nForce4 Ultra drives this signal when it detects a parity error.
	I/O	**GPIO_38** When **PCI_PERR#** is not selected, it becomes **GPIO_38**.
PCI_PME#	I	**PCI Power Management Interrupt** This signal is asserted by an external PCI device to signal a power management wake event.

Signal	I/O	Definition
	I/O	**GPIO_37** When **PCI_PME#** is not selected, it becomes **GPIO_37.**
PCI_REQ[4:0]#	I	**PCI Bus Requests** These signals are generated by an external PCI device on any of the five external PCI slots to request bus ownership from the NVIDIA nForce4 Ultra. Each external PCI slot or device has a dedicated request line. **PCI_REQ0#** must always be paired with **PCI_GNT0#**, **PCI_REQ1#** must always be paired with **PCI_GNT1#**, and so on.
	I/O	**GPIO_[45,16,6]** When **PCI_REQ[4:2]#** is not selected, it becomes **GPIO_[45,16,6]**.
PCI_RESET[3:0]#	O	**PCI Reset** These signals are asserted by the NVIDIA nForce4 Ultra to reset devices that reside on the PCI bus, as well as other devices, such as IDE. The NVIDIA nForce4 Ultra asserts these signals during power up and when software initiates a hard reset sequence.
PCI_SERR#	I	**PCI System Error** This signal can be asserted active for one clock cycle by any PCI device that detects a system error condition. A system error condition can be an address or data parity error on a special cycle command. It has no timing relationship to a PCI transaction. It is a synchronous signal.
PCI_STOP#	I/O	**PCI Stop** This signal indicates that the current target is requesting the initiator to stop the current PCI transaction. It is an output when the NVIDIA nForce4 Ultra is the target and an input when the NVIDIA nForce4 Ultra is the initiator.
PCI_TRDY#	I/O	**PCI Target Ready** This signal indicates the target's ability to complete the current data phase of the transaction. It is used in conjunction with **PCI_IRDY#.** A data phase is completed when both **PCI_TRDY#** and **PCI_IRDY#** are sampled asserted. Wait states are inserted until both **PCI_IRDY#** and **PCI_TRDY#** are asserted together. During a read cycle, it indicates that the target has placed valid data on **PCI_AD[31:0]**. During a write cycle, it indicates the target has latched the data. **PCI_TRDY#** is an input to the NVIDIA nForce4 Ultra when the NVIDIA nForce4 Ultra is the initiator and an output from the NVIDIA nForce4 Ultra when the NVIDIA nForce4 Ultra is the target.

Integrated Serial ATA 2 Interface

Table 10. Integrated SATA 2 Interface Signals

Signal	I/O	Definition
SP_RXP[1:0] **SP_RXN[1:0]**	DIFF IN	**Integrated SATA 2 Controller A Differential Receive Signals** These are the high speed differential receive signals of integrated SATA 2 controller A for channel 1 and channel 0. The SATA 2 signals require AC coupling capacitors near the connector. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
SP_TXP[1:0] **SP_TXN[1:0]**	DIFF OUT	**Integrated SATA 2 Controller A Differential Transmit Signals** These are the high speed differential transmit signals of integrated SATA 2 controller A for channel 1 and channel 0. The SATA 2 signals require AC coupling capacitors near the connector. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
SP_RXP[3:2] **SP_RXN[3:2]**	DIFF IN	**Integrated SATA 2 Controller B Differential Receive Signals** These are the high speed differential receive signals of integrated SATA 2 controller B for channel 1 and channel 0. The SATA 2 signals require AC coupling capacitors near the connector. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
SP_TXP[3:2] **SP_TXN[3:2]**	DIFF OUT	**Integrated SATA 2 Controller B Differential Transmit Signals** These are the high speed differential transmit signals of integrated SATA 2 controller B for channel 1 and channel 0. The SATA 2 signals require AC coupling capacitors near the connector. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
SP_REFCLKP **SP_REFCLKN**	DIFF IN	**Integrated SATA 2 Reference Clock** These pins are for the optional external reference clock for the internal SATA 2 PHY. The PLL can accept a 200 MHz, 150 MHz, or 100 MHz external reference clock. The default reference clock for the SATA 2 PHY is generated internally by the NVIDIA nForce4 Ultra. If the internal clock is used as the reference clock for the PLL, then these pins should be left floating. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
SP_TERMP	A	**Integrated SATA 2 Positive Termination** This pin is used in conjunction with **SP_TERMN** to calibrate the integrated termination resistors on the SATA 2 transmit and receive pins. A resistor should be connected between **SP_TERMP** and **SP_TERMN**. Special care must be taken to isolate the **SP_TERMP** pin from any unwanted noise sources. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
SP_TERMN	A	**Integrated SATA 2 Negative Termination** This pin is used in conjunction with **SP_TERMP** to calibrate the integrated termination resistors on the SATA 2 transmit and receive pins. A resistor should be connected between **SP_TERMP** and **SP_TERMN**. Special care must be taken to isolate the **SP_TERMN** pin from any unwanted noise sources. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
SP_LED#	OD	**Integrated SATA 2 PHY Activity LED** This signal is asserted whenever there is activity on any of the integrated SATA 2 PHYs. It can be used to drive an LED in the front panel to indicate SATA 2 activity.
	I/O	**GPIO_19** When **SP_LED#** is not selected, it becomes **GPIO_19**

IEEE 802.3 NVIDIA MAC Interface

RGMII Interface for Gigabit/Fast Ethernet/Ethernet

This section contains the signals associated with the RGMII interfaces. This interface is selected through an external strapping pin. Only one interface, either RGMII or MII, can be selected at a time.

Table 11. RGMII Signals

Signal	I/O	Definition
RGMII_INTR	I	**RGMII Interrupt** This signal is used as the interrupt between the PHY and the MAC.
	I/O	**GPIO_11** When **RGMII_INTR** function is not selected, it becomes **GPIO_11**.
RGMII_MDC	O	**RGMII Management Data Clock** This signal is used as the timing reference for transfer of information on the **RGMII_MDIO** signal.
RGMII_MDIO	I/O	**RGMII Management Data I/O** This signal is a bidirectional signal between the PHY and the NVIDIA nForce4 Ultra. It is used to transfer control information and status. Control information is driven by the NVIDIA nForce4 Ultra synchronously with respect to **RGMII_MDC** and is sampled by the PHY. Status information is driven by the PHY synchronously with respect to **RGMII_MDC** and is sampled by the NVIDIA nForce4 Ultra.
RGMII_PWRDWN	O	**RGMII PHY Power Down** This signal is used to power down the external PHY. This signal can be programmed as active high or active low.
	I/O	**GPIO_20** When **RGMII_PWRDWN** function is not selected, it becomes **GPIO_20**.
RGMII_RXCLK	I	**RGMII Receive Clock** This signal is the continuous receive reference clock that is derived from the received data.
RGMII_RXCTL	I	**RGMII Receive Control** This signal has **RXDV** on the rising edge of **RGMII_RXCLK** and a derivative of **RXDV** and **RXERR** on the falling edge of **RGMII_RXCLK**.
RGMII_RXD[3:0]	I	**RGMII Receive Data** These signals contain data bits [3:0] on the rising edge of **RGMII_RXCLK** and bits [7:4] on the falling edge of **RGMII_RXCLK**.
RGMII_TXCLK	O	**RGMII Transmit Clock** This signal is the transmit reference clock.
RGMII_TXCTL	O	**RGMII Transmit Control** This signal contains **TXEN** on the rising edge of **RGMII_TXCLK** and a derivative of **TXEN** and **TXERR** on the falling edge **of RGMII_TXCLK**.
RGMII_TXD[3:0]	O	**RGMII Transmit Data** These signals contain data bits [3:0] on the rising edge of **RGMII_TXCLK** and bits [7:4] on the falling edge of **RGMII_TXCLK**.
RGMII_VREF	A	**RGMII Voltage Reference** This is the reference voltage for the RGMII interface. Please refer to the *nForce4 (CrushK8-04) Design Guide*.

MII Interface for Fast Ethernet/Ethernet

This section contains the signals associated with the MII interfaces. This interface is selected through an external strapping pin. Only one interface, RGMII or MII, can be selected at a time.

Table 12. MII Signals

Signal	I/O	Definition
MII_COL	I	**MII Collision** This signal is asserted by the PHY upon detection of a collision condition on the medium. It remains asserted while the collision condition persists. It is not required to transition synchronously with respect to either the **MII_TXCLK** or the **MII_RXCLK**.
MII_CRS	I	**MII Carrier Sense** This signal is asserted by the PHY when either the transmit or receive medium is non-idle. It is de-asserted by the PHY when both transmit and receive media are idle. It remains asserted throughout the duration of a collision condition. It is not required to transition synchronously with respect to either the **MII_TXCLK** or the **MII_RXCLK**.
MII_INTR	I	**MII Interrupt** This signal is used as the interrupt between the PHY and the MAC.
	I/O	**GPIO_11** When **MII_INTR** function is not selected, it becomes **GPIO_11.**
MII_MDC	O	**MII Management Data Clock** This signal is used as the timing reference for transfer of information on the **MII_MDIO** signal. This signal is a periodic signal that has no maximum high or low times. The minimum high and low time is 160 ns each, and the minimum period is 400 ns, regardless of the nominal period of **MII_TXCLK** and **MII_RXCLK**.
MII_MDIO	I/O	**MII Management Data I/O** This signal is a bidirectional signal between the PHY and the NVIDIA nForce4 Ultra. It is used to transfer control information and status.
MII_PWRDWN	O	**MII PHY Power Down** This signal is used to power down the external 100BASE-T/10BASE-T PHY. This signal can be programmed as active high or active low.
	I/O	**GPIO_20** When **MII_PWRDWN** function is not selected, it becomes **GPIO_20**.
MII_RXCLK	I	**MII Received Clock** This signal is a continuous clock that provides the timing reference for the transfer of the **MII_RXDV**, **MII_RXD[3:0]**, and **MII_RXER** signals.
MII_RXD[3:0]	I	**MII Received Data** These signals transfer four bits of recovered data for each **MII_RXCLK** period when **MII_RXDV** is asserted. **MII_RXD[0]** is the least significant bit. While **MII_RXDV** is de-asserted, these signals will have no effect on the MAC. It transitions synchronously with respect to **MII_RXCLK**.

Signal	I/O	Definition
MII_RXDV	I	**MII Received Data Valid** This signal is driven by the PHY to indicate that it is presenting recovered and decoded data on the **MII_RXD[3:0]** lines and that the data is synchronous to **MII_RXCLK**. This signal transitions synchronously with respect to **MII_RXCLK**. This signal remains asserted continuously from the first recovered **MII_RXD[3:0]** of the frame through the final recovered **MII_RXD[3:0]**. It is negated prior to the first **MII_RXCLK** that follows the final **MII_RXD[3:0]**. In order for a received frame to be correctly interpreted by the MAC, **MII_RXDV** must encompass the frame, starting no later than the start-of-frame delimiter (SFD) and excluding an end-of-frame delimiter.
MII_RXER	I	**MII Receive Error** This signal is asserted for one or more **MII_RXCLK** periods to indicate to the MAC that an error was detected somewhere in the frame presently being transferred from the PHY. This signal transitions synchronously with respect to **MII_RXCLK**. While **MII_RXDV** is de-asserted, the PHY may provide a False Carrier indication by asserting this signal for at least one cycle of **MII_RXCLK** while driving the appropriate value onto **MII_RXD[3:0]**.
	I/O	**GPIO_21** When **MII_RXER** function is not selected, it becomes **GPIO_21**.
MII_TXCLK	I	**MII Transmit Clock** This signal is a continuous clock that provides the timing reference for the transfer of the **MII_TXEN** and **MII_TXD[3:0]** signals.
MII_TXD[3:0]	O	**MII Transmit Data** These signals transfer four bits of data to the PHY for each **MII_TXCLK** period when **MII_TXEN** is asserted. **MII_TXD[0]** is the least significant bit. While **MII_TXEN** is de-asserted, these signals have no effect upon the PHY. These signals transition synchronously with respect to **MII_TXCLK**.
MII_TXEN	O	**MII Transmit Data Enable** This signal indicates that the MAC is presenting valid data on **MII_TXD[3:0]** on the MII channel for transmission. This signal is asserted by the MAC synchronously with the first **MII_TXD[3:0]** for the preamble and will remain asserted while all **MII_TXD[3:0]** to be transmitted are presented on the MII channel. This signal is negated prior to the first **MII_TXCLK** following the final **MII_TXD[3:0]** of a frame.
MII_VREF	A	**MII Voltage Reference** This is the voltage reference for the MII interface. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.

Table 13. RGMII and MII Signal Multiplexing

RGMII	MII
RGMII_MDC	MII_MDC
RGMII_MDIO	MII_MDIO
RGMII_PWRDWN	MII_PWRDWN
RGMII_RXCLK	MII_RXCLK
RGMII_RXCTL	MII_RXDV
RGMII_RXD[3:0]	MII_RXD[3:0]
RGMII_TXCLK	MII_TXCLK
RGMII_TXCTL	MII_TXEN
RGMII_TXD[3:0]	MII_TXD[3:0]
	MII_COL
	MII_CRS
	MII_RXER

Dual USB Interface

Table 14. USB Interface Signals

Signal	I/O	Definition
USB_[9:0] **USB_[9:0]#**	DIFF I/O	**USB Differential Signals** These signals are the differential I/O pairs of the USB port [9:0] data signals. They support high-speed (480 Mb/s), full-speed (12 Mb/s), and low-speed (1.5 Mb/s) data rates. These signals should be pulled down to GND through a resistor to prevent them from floating when not used. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
USB_OC[4:0]#	I	**USB Over-Current Indicators** These signals set corresponding bits in the USB controller to indicate that an over-current condition has occurred when this function is selected. These signals are not +5V tolerant. Each **USB_OC[4:0]#** can be used to group USB ports. That is, **USB_OC0#** and **USB_OC1#** could be used for all the front panel USB ports, while **USB_OC2#** and **USB_OC3#** could be used for all the rear panel USB ports, and so forth. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
	I/O	**GPIO_[25:22]** When **USB_OC[4:1]#** are not selected, they become **GPIO_[25:22]**.
USB_RBIAS	A	**USB Reference Bias** This signal is a reference current setting bias resistor for all ten USB pads. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.

Dual SMBus Interface

Table 15. Dual SMBus Signals

Signal	I/O	Definition
SMB_CLK[1:0]	OD	**SMBus Clocks** These signals are the two System Management Bus clocks when SMBus is selected. Clocks [1:0] control the second and first SMBus interface, respectively.
	I/O	**GPIO_[43,41]** When **SMB_CLK[1:0]** are not selected, they become **GPIO_[43,41]**.
SMB_DATA[1:0]	OD	**SMBus Data** These signals are the two System Management Bus lines when SMBus is selected. Bits [1:0] correspond to the second and first SMBus interface, respectively.
	I/O	**GPIO_[44,42]** When **SMB_DATA[1:0]** are not selected, they become **GPIO_[44,42]**.

Dual ATA-133 IDE Interfaces

This section contains the signals associated with the following IDE interfaces:

- Shared Table 16
- Primary Table 17
- Secondary Table 18

Shared Signals

Table 16. Shared IDE Interface Signals

Signal	I/O	Definition
IDE_COMP_GND	A	**IDE Interface Compensation** This pin is used for the IDE Interface pads calibration. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
IDE_COMP_3P3V	A	**IDE Interface Compensation** This pin is used for the IDE Interface pads calibration. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
CABLE_DET_P	I	**Primary Cable Type Detect** This input is used to determine if an 80-pin or 40-pin cable is connected to the primary IDE interface.
CABLE_DET_S	I	**Secondary Cable Type Detect** This input is used to determine if an 80-pin or 40-pin cable is connected to the secondary IDE interface.

Primary IDE Interface

Table 17. Primary IDE Interface Signals

Signal	I/O	Definition
IDE_ADDR_P[2:0]	O	**Primary IDE Address** These signals are the IDE controller's primary port address. It indicates which byte in either the ATA command block or control register is being addressed.
IDE_CS1_P#	O	**Primary IDE Port Chip Select 1xx** This signal is the primary port chip select for the 1F7h-1F0h range. It is used for the AT command register block.
IDE_CS3_P#	O	**Primary IDE Port Chip Select 3xx** This signal is the primary port chip select for the 3F7h-3F4h range. It is used for the AT control register block.
IDE_DACK_P#	O	**Primary IDE DMA Acknowledge** This signal is the DMA acknowledge of the primary IDE channel. The NVIDIA nForce4 Ultra responds to the **IDE_DREQ_P** signal from a primary IDE device either to acknowledge that the DMA data has been accepted or to inform that DMA data is available.
IDE_DATA_P[15:0]	I/O	**Primary IDE Data Bus** These signals are the bidirectional data bus used to transfer data to or from the primary IDE device. When the NVIDIA nForce4 Ultra is writing to a primary IDE device, they are driven valid before the negation of the **IDE_IOW_P#** signal. When the NVIDIA nForce4 Ultra is reading from a primary IDE device, they are sampled at the rising edge of **IDE_IOR_P#** signal. They are tri-stated when no read or write is in progress. These signals have internal series resistors per the ATA specification.
IDE_DREQ_P	I	**Primary IDE DMA Request** This signal is the DMA request signal from the primary IDE channel. A primary IDE device will assert this signal when ready to read or write DMA data.
IDE_INTR_P	I	**Primary IDE Interrupt** This signal is the interrupt signal from the primary IDE device to request service.
IDE_IOR_P#	O	**Primary IDE I/O Read** This signal is the primary IDE channel read strobe for PIO and DMA modes. The falling edge of this signal enables the transfer of data from a register or data port of the device onto **IDE_DATA_P[15:0]**. **Primary IDE UltraDMA Host Ready** This signal is the primary channel flow control for UltraDMA input data bursts. When the primary IDE host is ready to receive DMA data, it asserts this signal. The primary IDE host may stop toggling this signal to pause an UltraDMA input data transfer. **Primary IDE UltraDMA Host Strobe** This signal is the primary channel strobe signal from the host for an UltraDMA output data transfer. Both edges of this signal latch data from **IDE_DATA_P[15:0]** into the device. The host may stop toggling this signal to pause an UltraDMA output data transfer.
IDE_IOW_P#	O	**Primary IDE I/O Write** This signal is the primary IDE channel write strobe for PIO and DMA modes. The rising edge of this signal latches **IDE_DATA_P[15:0]** into either a register or data port of the device. **IDE Primary Stop** This signal is the primary IDE channel stop for UltraDMA modes. It halts the data transfer of the primary IDE channel.

Signal	I/O	Definition
IDE_RDY_P	I	**Primary IDE Device Ready** This signal is the primary IDE device-ready indicator for PIO modes. If a device is not ready to respond to a data transfer request, the device negates this signal to extend the read or write cycle. When negated, this signal is in a high impedance state. **Primary IDE UltraDMA Device Ready** This signal is the primary channel flow control signal for UltraDMA output data bursts. When the host is ready to receive DMA data, the primary IDE device asserts this signal. The primary IDE device negates this signal to pause an UltraDMA output data transfer. **Primary IDE UltraDMA Device Strobe** This signal is the primary channel input data strobe signal from the primary IDE device for an UltraDMA input data transfer. Both edges of this signal latch data from **IDE_DATA_P[15:0]** into the host. The primary IDE device may stop toggling this signal to pause an UltraDMA data in transfer.

Secondary IDE Interface

Table 18. Secondary IDE Interface Signals

Signal	I/O	Definition
IDE_ADDR_S[2:0]	O	**Secondary IDE Address** These signals are the IDE controller's secondary port address. It indicates which byte in either the ATA command block or control register is being addressed.
IDE_CS1_S#	O	**Secondary IDE Port Chip Select 1xx** This signal is the secondary port chip select for the 1F7h–1F0h range. It is used for the AT command register block.
IDE_CS3_S#	O	**Secondary IDE Port Chip Select 3xx** This signal is the secondary port chip select for the 3F7h–3F4h range. It is used for the AT control register block.
IDE_DACK_S#	O	**Secondary IDE DMA Acknowledge** This signal is the DMA acknowledge of the secondary IDE channel. The NVIDIA nForce4 Ultra responds to the **IDE_DREQ_S** signal from a secondary IDE device either to acknowledge that the DMA data has been accepted or to inform that DMA data is available.
IDE_DATA_S[15:0]	I/O	**Secondary IDE Data Bus** These signals are the bidirectional data bus used to transfer data to or from the secondary IDE device. When the NVIDIA nForce4 Ultra is writing to a secondary IDE device, they are driven valid before the negation of the **IDE_IOW_S#** signal. When the NVIDIA nForce4 Ultra is reading from a secondary IDE device, they are sampled at the rising edge of **IDE_IOR_S#** signal. They are tri-stated when no read or write is in process. These signals have internal series resistors per the ATA specification.
IDE_DREQ_S	I	**Secondary IDE DMA Request** This signal is the DMA request signal from the secondary IDE channel. A secondary IDE device will assert this signal when it is ready to read or write DMA data.
IDE_INTR_S	I	**Secondary IDE Interrupt** This signal is the interrupt signal from the secondary IDE device to request service.

Signal	I/O	Definition
IDE_IOR_S#	O	**Secondary IDE I/O Read** This signal is the secondary IDE channel read strobe for PIO and DMA modes. The falling edge of this signal enables the transfer of data from a register or data port of the device onto **IDE_DATA_S[15:0]**. **Secondary IDE UltraDMA Host Ready** This signal is the secondary channel flow control for UltraDMA input data bursts. When a secondary IDE host is ready to receive DMA data, it asserts this signal. The secondary IDE host may stop toggling this signal to pause an UltraDMA input data transfer. **Secondary IDE UltraDMA Host Strobe** This signal is the secondary channel strobe signal from the host for an UltraDMA output data transfer. Both edges of this signal latch data from **IDE_DATA_S[15:0]** into the device. The host may stop toggling this signal to pause an UltraDMA output data transfer.
IDE_IOW_S#	O	**Secondary IDE I/O Write** This signal is the secondary IDE channel write strobe for PIO and DMA modes. The rising edge of this signal latches **IDE_DATA_S[15:0]** into either a register or data port of the device. **Secondary IDE Stop** This signal is the secondary IDE channel stop for UltraDMA modes. It halts the data transfer of the secondary IDE channel.
IDE_RDY_S	I	**Secondary IDE Device Ready** This signal is the secondary IDE device ready indicator for PIO modes. If a device is not ready to respond to a data transfer request, the device negates this signal to extend the read or write cycle. When negated, this signal is in a high impedance state. **Secondary IDE UltraDMA Device Ready** This signal is the secondary channel flow control signal for UltraDMA output data bursts. When the host is ready to receive DMA data, the secondary IDE device asserts this signal. The secondary IDE device negates this signal to pause an UltraDMA output data transfer. **Secondary IDE UltraDMA Device Strobe** This signal is the secondary channel input data strobe signal from the secondary IDE device for an UltraDMA input data transfer. Both edges of this signal latch data from **IDE_DATA_S[15:0]** into the host. The secondary IDE device may stop toggling this signal to pause an UltraDMA data in transfer.

Audio/Modem Interface (AC' 97 Link)

Table 19. Audio/Modem Interface Signals

Signal	I/O	Definition
AC_BITCLK	I	**AC-Link Clock** This signal is the AC '97 12.288 MHz clock used for serial data transfer between the codec and NVIDIA nForce4 Ultra. This clock is also used for S/PDIF out.
AC_RESET#	O	**AC-Link Reset** This signal is the active low AC '97 reset signal. This pin is also used as a strap pin. Refer to Table 30 for a detailed explanation of the strap function.
AC_SDATA_IN0	I	**AC-Link Serial Primary Data In** This signal is the serial time division multiplexed AC '97 input data stream from the primary codec.
	I/O	**GPIO_14** When **AC_SDATA_IN0** is not selected, it becomes **GPIO_14**.
AC_SDATA_IN1	I	**AC-Link Serial Secondary Data In** This signal is the serial time division multiplexed AC '97 input data stream from the secondary codec when AC-link is selected.
	I/O	**GPIO_27** When **AC_SDATA_IN1** is not selected, it becomes **GPIO_27**.
AC_SDATA_OUT	O	**AC-Link Serial Primary Data Out** This signal is the serial time division multiplexed AC '97 output data stream to the primary codec. This pin is also used as a strap pin. Refer to Table 30 for a detailed explanation of the strap function.
	I/O	**GPIO_13** When **AC_SDATA_OUT** is not selected, it becomes **GPIO_13**.
AC_SYNC	O	**AC Link Synchronization** This signal is the fixed AC '97 48 kHz synchronization signal between the NVIDIA nForce4 Ultra and the codec. This pin is also used as a strap pin. Refer to Table 30 for a detailed explanation of the strap function.
	I/O	**GPIO_12** When **AC_SYNC** is not selected, it becomes **GPIO_12**.
AC97_CLK	O	**AC '97 Clock** This signal is the AC '97 24.576 MHz master clock to be used by the AC '97 codec.

LPC Interface

Table 20. LPC Interface Signals

Signal	I/O	Definition
LPC_AD[3:0]	I/O	**LPC Multiplexed Command, Address, Data** These signals are used to communicate information such as start, stop (abort a cycle), transfer type (memory, I/O, DMA), transfer direction (read/write), address, data, wait states, DMA channel, and bus master grant. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
LPC_CLK[1:0]	O	**LPC Clock[1:0]** These signals are the 33 MHz clocks that are in phase with the **PCI_CLKn** clocks. They provide the timing reference for all transactions on the LPC bus. **LPC_CLK1** can be used as a spare LPC or PCI bus clock.
LPC_DRQ0#	I	**LPC Serial DMA/Master Request0** This signal is used by an external device to request DMA or bus master accesses when this function is selected. **LPC_DRQ0#** is typically connected to an external SuperI/O device. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
LPC_CS# / LPC_DRQ1#	O	**LPC Chip Select** This signal is used as a chip select on the LPC bus when this function is selected.
	I	**LPC Serial DMA/Master Request1** This signal is used by an external device to request DMA or bus master accesses when this function is selected. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.
LPC_FRAME#	O	**LPC Frame** This signal indicates the start of an LPC cycle or termination of a LPC cycle due to an abort or timeout. This pin is also used as a strap pin. Refer to Table 30 for a detailed explanation of the strap function.
LPC_PWRDWN#	O	**LPC Power Down** This signal is used to power down the LPC bus, which complies to the *LPC 1.1 Specification.*
	I/O	**GPIO_39** When **LPC_PWRDWN#** is not selected, it becomes **GPIO_39**.
LPC_RESET#	O	**LPC Reset** This signal is used to reset the LPC bus.
SERIRQ	I/O	**LPC Serial Interrupt** This signal is the serial interrupt signal from the external LPC bus. It is used to transmit interrupt information to the internal interrupt controller. It is usually connected to the SuperI/O device. Please refer to the *nForce4* (*CrushK8-04) Design Guide*.

Clock Interface

Table 21. Clock Interface Signals

Signal	I/O	Definition
BUF_25MHZ	O	**Buffered 25 MHz** This signal is the 25 MHz clock for the external 1000BASE-T/100BASE-T/10BASE-T PHY.
BUF_SIO_CLK	O	**Buffered SuperI/O Clock** This signal is the buffered clock to the SuperI/O. A frequency of either 24 MHz or 14.31818 MHz is selected through a strap resistor.
CPU_CLK **CPU_CLK#**	DIFF OUT	**CPU Clock** This is the differential 200 MHz CPU clock. This clock is spread spectrum capable for EMI reduction.
CPU_CLK_66	O	**66 MHz CPU Clock** This is a 66 MHz CPU clock that is spread spectrum capable with a gate. It is controlled by **CPU_CLKRUN#**.
SUSCLK	O	**32.768 kHz SUSCLK Output Clock** This clock is active in S0-S5 states (when VAUX is on).
	I/O	**GPIO_31** When **SUSCLK** is not selected, it becomes **GPIO_31**.
XTAL_IN	I	**25 MHz Crystal Input** This signal is used by the internal clock synthesizer to generate all internal clocks. It is connected to a 25 MHz crystal. This signal is a no-connect when **XTAL_OUT** is driven by a CMOS clock driver.
XTAL_OUT	O	**25 MHz Crystal Output** This signal is connected to a 25 MHz crystal. It can also be driven by a 3.3 V CMOS clock driver with a 25 MHz frequency.
XTALIN_RTC	I	**RTC Crystal Input 0** This signal is connected to a 32.768 kHz crystal. It can also be driven by a CMOS clock driver with a 32.768 kHz frequency.
XTALOUT_RTC	O	**RTC Crystal Input 1** This signal is connected to the 32.768 kHz crystal. This signal is a no-connect when **XTALIN_RTC** is driven by a CMOS clock driver.

System and Power Management Interface

Table 22. System and Power Management Interface Signals

Signal	I/O	Definition
EXT_SMI#	I	**External SMI** This signal can be used to generate SMI or SCI interrupts and resume events. This signal can be wired as a logical OR.
	I/O	**GPIO_29** When **EXT_SMI#** is not selected, it becomes **GPIO_29**.
FANCTL[1:0]	O	**Fan Control** This signal can be used to control the rate of system fans.
	I/O	**GPIO_[36,35]** When **FANCTL[1:0]** are not selected, they become **GPIO_[36,35]**.
FANRPM	I	**Fan RPM** This signal can be used to track the RPM of the fan.
	I/O	**GPIO_34** When **FANRPM** is not selected, it becomes **GPIO_34**.
INTRUDER#	I	**Intruder** This signal is an input that can be connected to a switch that is activated by opening the system chassis. When this input is asserted for more than 60 µs, it can be enabled to cause an SCI or SMI interrupt.
KBRDRSTIN#	I	**Keyboard Reset In** This signal functions as a reset input from the external keyboard controller that is used to generate a pulse on the **CPU_RST#** line or an **INIT#** message. This signal is not +5V tolerant.
	I/O	**GPIO_18** When **KBRDRSTIN#** is not selected, it becomes **GPIO_18**.
PWRBTN#	I	**Power Button** When the system is in the soft off (G2) state, this signal controls the automatic transition to full on (G0). It can be programmed to generate SCI or SMI interrupts from any state other than soft off (G2). If asserted for four seconds from any state other than soft off (G2), a power button override event is generated.
PWRGD	I	**Power Good** When this signal is asserted, it is an indication to the NVIDIA nForce4 Ultra that its core power and all other power have been stable for at least 10 ms. This signal can be driven asynchronously. When this signal is negated, the NVIDIA nForce4 Ultra shuts down to S5, as required by the AMD Design Guide. This input is a Schmitt trigger input.
PWRGD_SB	I	**Power Good Standby** This signal is connected to an external signal that goes active when the standby power supply is stable. It must be held low for a minimum of 10 ms after the resume power plane is stable. It is used to reset the logic on the standby power plane. This input is a Schmitt trigger input.
RI#	I	**Ring Indicator** This signal can be connected to an external modem circuitry to allow the system to be reactivated by a phone call. It causes the system to resume the full on (G0) state and generates SCI or SMI interrupts.
	I/O	**GPIO_30** When **RI#** is not selected, it becomes **GPIO_30**.

Signal	I/O	Definition
RSTBTN#	I	**Reset Button** The assertion of this signal will initiate a warm reset to the system. When this signal is asserted for 32 ms, the NVIDIA nForce4 Ultra will assert **PCI_RESET[x]#** for 1 ms. **CPU_RST#** will also be asserted and released soon after (refer to the Power Sequencing section). All Power Good signals (**PWRGD**, **PWRGD_SB**, and **CPU_PWROK**) will remain high through out this process. This signal will only be valid after **PWRGD** has been asserted. This signal should be connected to the front panel. This signal is edge sensitive and will generate one warm reset sequence regardless of how long this signal is pressed.
RTC_RST#	I	**RTC Reset** When this signal is asserted low, it clears all the CMOS contents, except time-of-day, for the subsequent boot.
SIO_PME#	I	**SuperI/O Power Management Event Indicator** This signal is asserted by the SuperI/O device to indicate a power management event.
	I/O	**GPIO_28** When **SIO_PME#** is not selected, it becomes **GPIO_28**.
SLP_S3#	O	**Sleep State S3** This signal is asserted when the power state machine is in the S3 low power state. This can be used to control all power planes, except the system memory power plane.
SLP_S5#	O	**Sleep State S5** This signal is asserted when the power state machine is in the S4 or S5 state. This can be used to control system memory power planes.
THERM#	I	**Thermal** This signal can be enabled to automatically result in CPU throttling when a thermal event has occurred.
	I/O	**GPIO_32** When **THERM#** is not selected, it becomes **GPIO_32**.

Power Supply Interface

Table 23. Power Supply Interface Signals

Signal	I/O	Power	Definition
+1.2V_HT	P	1.2 V	**1.2 V HyperTransport Power** This voltage powers the HyperTransport interface.
+1.5V	P	1.5 V	**1.5 V Core Power** This voltage powers the NVIDIA nForce4 Ultra core.
+1.5V_DUAL	P	1.5 V	**1.5 V Sleep Mode Core Power** This voltage powers the internal power management circuitry and devices that remain active while in S3-S5.
+1.5V_PE_A	P	1.5 V	**1.5 V PCI Express Analog Power** This voltage powers the analog section of the PCI Express interface.
+1.5V_PE_D	P	1.5 V	**1.5 V PCI Express Digital Power** This voltage powers the digital section of the PCI Express interface.
+1.5V_PLL_HT	P	1.5 V	**1.5 V HyperTransport PLL Power** This voltage powers the HyperTransport PLL clock drivers.
+1.5V_PLL_PE_AVDD	P	1.5 V	**1.5 V PCI Express Analog PLL Power** This voltage powers the analog section of the PCI Express PLL driver.
+1.5V_PLL_PE_CORE	P	1.5 V	**1.5 V PCI Express Core PLL Power** This voltage powers the integrated PCI Express PLL core.
+1.5V_PLL_PE_DVDD	P	1.5 V	**1.5 V PCI Express Digital PLL Power** This voltage powers the digital section of the PCI Express PLL driver.
+1.5V_PLL_SP_AVDD	P	1.5 V	**1.5 V SATA 2 Analog PLL Power** This voltage powers the analog section of the integrated SATA 2 PLL driver.
+1.5V_PLL_SP_CORE	P	1.5 V	**1.5 V Integrated SATA 2 Core PLL power** This voltage powers the integrated SATA 2 PLL core.
+1.5V_PLL_SP_DVDD	P	1.5 V	**1.5 V SATA 2 Digital PLL Power** This voltage powers the digital section of the integrated SATA 2 PLL driver.
+1.5V_SP_A	P	1.5 V	**1.5 V SATA 2 Analog Power** This voltage powers the analog section of the integrated SATA 2.
+1.5V_SP_D	P	1.5 V	**1.5 V SATA 2 Digital Power** This voltage powers the digital section of the integrated SATA 2.
+3.3V	P	3.3 V	**3.3 V Power** This voltage powers the 3.3 V interface to 3.3 V peripherals.
+3.3V_DUAL	P	3.3 V	**3.3 V Sleep Mode Power** This voltage powers the power management interface to 3.3 V peripherals.
+3.3V_PLL_CPU	P	3.3 V	**3.3 V CPU Interface PLL Power** This voltage powers the CPU interface PLL.

Signal	I/O	Power	Definition
+3.3V_PLL_DUAL	P	3.3 V	**3.3 V Standby PLL Power** This voltage powers the integrated core PLL during power management states.
+3.3V_PLL_HT	P	3.3 V	**3.3 V HyperTransport PLL Power** This voltage powers the HyperTransport PLL.
+3.3V_PLL_PE_CORE	P	3.3 V	**3.3 V Core PLL Power** This voltage powers the core PLL.
+3.3V_PLL_SP_CORE	P	3.3 V	**3.3 V SATA 2 Core PLL Power** This voltage powers the integrated SATA 2 PLL core.
+3.3V_PLL_USB	P	3.3 V	**3.3V USB PLL Power** This voltage powers the USB PLL.
+3.3V_USB_DUAL	P	3.3 V	**3.3 V USB Power** This voltage powers the two integrated USB controllers. It is connected directly to the **+3.3 V_DUAL** power plane.
+3.3V_VBAT	P	3.3 V	**3.3 V Battery Voltage** This voltage powers the RTC.
+5V	P	5 V	**5 V Power** This voltage is used as the reference voltage for the 5 V tolerant I/O.
V3P3_DEEP	P	3.3 V	**Power Button and Deep Sleep Logic Power** This voltage powers the power button and deep sleep logic. It MUST always be tied to **+3.3V_DUAL**.
GND	P		**Ground**
GND_PLL_PE	P		**PCI Express PLL Ground**
GND_PLL_SP	P		**SATA 2 PLL Ground**
PE_AGND	P		**PCI Express Analog Ground**
PE_DGND	P		**PCI Express Digital Ground**
SP_AGND	P		**SATA 2 Analog Ground**
SP_DGND	P		**SATA 2 Digital Ground**

Miscellaneous Interface

Table 24. Miscellaneous Interface Signals

Signal	I/O	Definition
SPDIF0	O	**SPDIF Output 0** This signal is used to transmit 24 bit, 48 kHz, or 96 kHz compressed or PCM data to an external SPDIF receiver when this function is selected. This pin should always be used to provide the SPDIF OUT functionality. This pin is also used as a strap pin. See Table 30 for a detailed explanation of the strap function.
	I/O	**GPIO_33** When **SPDIF0** is not selected, it becomes **GPIO_33**.
SPDIF1	O	**SPDIF Output 1** In the AC '97+ mode, this signal is used to transmit 24 bit, 96 kHz stereo data to a two-channel codec on the motherboard. In the standard AC '97 mode, this signal may be used in conjunction with **AC_SDATA_OUT** to provide 7.1 speaker support. In this case, this pin should be connected to a standard AC '97 two-channel codec for best results. This pin is also used as a strap pin. See Table 30 for a detailed explanation of the strap function.
	I/O	**GPIO_15** When **SPDIF1** is not selected, it becomes **GPIO_15**.
SPKR	O	**Speaker** This signal is the output of counter 2. This signal drives an external speaker driver, which in turn drives the system speaker. This pin is also used as a strap input. See Table 30 for a detailed explanation of the strap function.
SP_ATEST	I	**SP Test** This signal should be left as a no-connect.
TEST	I	**Test** This signal is sampled on the rising edge of **PWRGD_SB** and is used to place the device into a test mode. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
PE_CLK_TEST **PE_CLK_TEST#**	DIFF OUT	**PCI Express Differential Test Signals** These differential signals should be left as no-connect.
SP_TESTP **SP_TESTN**	DIFF OUT	**SATA 2 Differential Test Signals** These differential signals should be left as no-connect.

GPIO Signals

Table 25. GPIO Interface Signals

Signal	I/O	Definition
GPIO_1	I/O	**GPIO 1** This is the **GPIO_1** signal.
GPIO_2	I/O	**GPIO 2** This is the primary signal.
	O	**CPU_SLP#** This is the secondary signal. Please refer to Table 29, Transmeta Interface Signals.
GPIO_3	I/O	**GPIO 3** This is the primary signal.
	I	**CPU_CLKRUN#** This is the secondary signal. Please refer to Table 29, Transmeta Interface Signals.
GPIO_4	I/O	**GPIO 4** This is the primary signal.
	O	**SUS_STAT#** This is the secondary signal. Please refer to Table 29, Transmeta Interface Signals.
GPIO_5	I/O	**GPIO 5** This is the **GPIO_5** signal.

AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU Power Sequencing

Table 26. AMD Athlon 64/Athlon 64 FX and Sempron 939/754 pin CPUs CPU Power Sequencing Signals

Signal	I/O	Definition
CPU_VLD	I	**CPU VDD Power Valid** This signal indicates that the CPU VDD power plane is valid. This input is a Schmitt trigger input.
CPUVDD_EN	O	**CPU VDD Enable** This signal should be used to control the voltage regulator that powers the **CPU_VDD** power plane.
HT_VLD	I	**HyperTransport Link +1.2 V Power Valid** This signal indicates that the **+1.2V_HT** power plane is valid. This input is a Schmitt trigger input.
HTVDD_EN	O	**HyperTransport Link +1.2V_HT Enable** This signal should be used to control the voltage regulator that powers the **+1.2V_HT** power plane.
MEM_VLD	I	**Memory +2.5 V Power Valid** This signal indicates that the DDR DRAM **+2.5 V** power plane is valid. This input is a Schmitt trigger input.

Mobile Function Signals

Table 27. Mobile Function Signals

Signal	I/O	Definition
LID#	I	**Laptop Lid Switch** This signal is used to indicate to the operating system that the laptop lid has been closed or opened while the power is on. It will generate a SCI/Wake event on the rising or falling edge of **LID#**. It is debounced for 31 ms. This is the primary function of this pin and is only used for mobile applications.
	I/O	**GPIO_7** This is the secondary function of this pin and must be configured as a **GPIO** on power up for desktop applications. When **LID#** is not selected, then it becomes **GPIO_7**.
LLB#	I	**Very Low Battery Indicator** This signal is used to indicate to the operating system that the battery power is very low. It will generate an SCI event to alert the operating system that a shutdown operation should occur. Also, when asserted, resumes from S5 are prevented. This is the primary function of this pin and is only used for mobile applications. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
SLP_DEEP#	O	**Very Deep Sleep** This signal is used to enter a very deep sleep state. The system will only respond to **PWRBTN#** for wake events. The system will appear to have been woken from the G3 state. Almost no internal logic is powered in this mode except for the deep sleep wake logic and the battery backup logic. This signal is only used for mobile applications. This signal becomes a no-connect for desktop applications.
V3P3_DEEP	P	**Deep Sleep 3.3V Power** This **+3.3V** voltage powers the deep sleep wake logic. This signal is only used for mobile applications. This signal must be connected to **+3.3V_DUAL**.

Transmeta Interface

Table 28. Transmeta Interface Signals

Signal	I/O	Definition
CPU_CLKRUN#	I	**CPU_CLK_66 Control** This signal permits external control (enable/disable) of the **CPU_CLK_66** output. This signal is the secondary signal that is multiplexed with the primary **GPIO_3** signal.
CPU_SLP#	O	**CPU Sleep Control** This signal is used to place the CPU in a lower power state than C2. It is optionally used to stop the CPU clock in Transmeta processor systems. This signal is the secondary signal that is multiplexed with the primary **GPIO_2** signal.
SUS_STAT#	O	**CPU Power Management State** This signal is a sideband power management signal to indicate that the CPU is in a non-C0 state. This signal is the secondary signal that is multiplexed with the primary **GPIO_4** signal.

JTAG Interface

Table 29. JTAG Interface Signals

Signal	I/O	Definition
TCK	I	**JTAG Clock** This signal must be pulled down to **GND** through a resistor for normal operation. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
TDI	I	**JTAG Serial Data Input** This signal must be pulled up to **+3.3 V** through a resistor for normal operation. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
TDO	O	**JTAG Serial Data Output** This signal must be left as a no-connect for normal operation. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
TMS	I	**JTAG Mode Select** This signal must be pulled up to **+3.3 V** through a resistor for normal operation. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
TRST#	I	**JTAG Reset** This signal must be pulled down to GND through a resistor for normal operation. Please refer to the *nForce4 (CrushK8-04) Design Guide*.

Strapping/Test Balls

The NVIDIA nForce4 Ultra strapping and test balls are listed in Table 30 and 31. When **PWRGD** is asserted low, these outputs will become inputs. When **PWRGD** goes high, their value is latched internally and used to configure the device.

Table 30. Strapping Signals

Signal	Strap Name	Strapped Value	Description
AC_RESET#	Networking interface select	0 = MII 1 = RGMII	Selects the networking interface.
AC_SDATA_OUT	PE_REFCLK_IN/ PE_REFCLK_IN# Termination enable	0 = Termination disabled 1 = Termination enabled	Enable internal 100 Ω differential termination for PCI Express reference clock input pins, **PE_REFCLK_IN/ PE_REFCLK_IN#.**
AC_SYNC	Reserved	0 = Normal operation 1 = Reserved	**Reserved Function**
LPC_FRAME#	PE_REFCLK_IN/ PE_REFCLK_IN# Common mode level select	0: Common mode below VDD/2 1: Common mode above VDD/2	Select common-mode level range for PCI Express external reference clock input pins, **PE_REFCLK_IN/PE_REFCLK_IN#.**
SPDIF0	BUF_SIO_CLK select	0 = 14.31818 MHz 1 = 24 MHz	Selects the SuperI/O clock to be either 14.31818 MHz or 24 MHz.
SPDIF1	PE_REFCLK select	0 = Internal clock reference 1 = External clock reference	Selects the source for the PCI Express PLL reference clock.
SPKR	Boot mode select	0 = User Mode Boot Init table (TCO timer enabled) 1 = Safe Mode Boot Init table (TCO timer disabled	Selects between a USER table and a SAFE table for boot initialization parameters. **Note**: When booting the SAFE table, it is assumed that the boot values are valid, so the automatic recovery logic is disabled (TCO timer will not reboot the system).

Note: Use a 4.7 kΩ – 10 kΩ resistor for the pull-up or pull-down function.

Table 31. Test Balls

Signal	Description
SP_ATEST	This signal can be left as a no-connect for normal operation.
TEST	This signal must be tied to **GND** through a resistor for normal operation. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
PE_CLK_TEST **PE_CLK_TEST#**	These signals can be left as no-connect for normal operation.
SP_TESTP **SP_TESTN**	These signals can be left as no-connect for normal operation.

Chapter 3.
Clock Domains

Clocking

The following clocks are used or generated by the NVIDIA nForce4 Ultra to and from the various peripherals. Figure 2 shows the NVIDIA nForce4 Ultra clocking block diagram and Table 32 lists the signals associated with clocking.

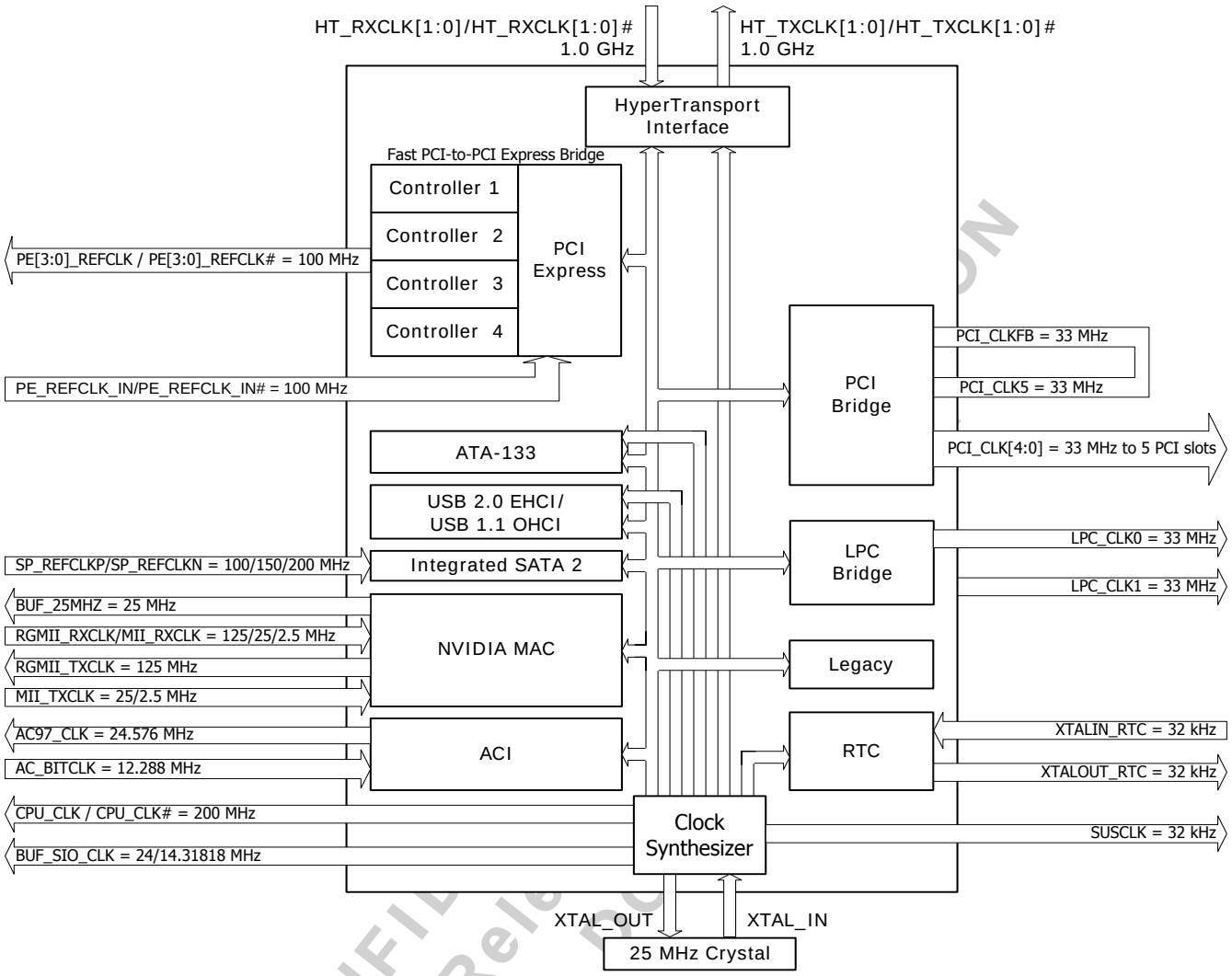

Figure 2. Clock Block Diagram

Table 32. Clock Signals

Clock Signal	Frequency (in MHz unless noted)	I/O	Description
AC97_CLK	24.576	O	**AC '97 Clock** This signal is the AC '97 24.576 MHz master clock used by the AC '97 codec.
AC_BITCLK	12.288	I	**AC-Link Clock** This signal is the AC '97 12.288 MHz clock used for serial data transfer between the codecs and NVIDIA nForce4 Ultra. This clock is also used for **S/PDIF** out.
BUF_25MHZ	25	O	**Buffered 25 MHz Clock** This signal is the 25 MHz clock for the external RGMII/MII PHY.
BUF_SIO_CLK	24/14.31818	O	**Buffered SuperIO Clock** This signal is the 24 MHz /14.31818 MHz clock for the FDC (floppy disk controller) of the SuperI/O.
CPU_CLK **CPU_CLK#**	200	DIFF OUT	**CPU Clock** This is the differential 200 MHz CPU clock. This clock is spread spectrum capable.
CPU_CLK_66	66	O	**66 MHz CPU Clock** This is a single-ended 66 MHz CPU clock that is spread spectrum capable and can be dynamically gated off.
HT_RXCLK[1:0] **HT_RXCLK[1:0]#**	Variable	DIFF IN	**HyperTransport Link Differential Receive Clock** These signals are the differential pairs used as the timing reference for **HT_RXD[15:0]** and **HT_RXCTL.** These default to 200 MHz on cold reset.
HT_TXCLK[1:0] **HT_TXCLK[1:0]#**	Variable	DIFF OUT	**HyperTransport Link Differential Transmit Clock** These signals are the differential pairs used as the timing reference for **HT_TXD[15:0]** and **HT_TXCTL**. These default to 200 MHz on cold reset. These are spread spectrum capable.
LPC_CLK[1:0]	33	O	**LPC Clock [1:0]** These clocks are in-phase with the **PCI_CLKn** 33 MHz clock output. They provide the timing reference for all transactions on the LPC bus. These clocks are spread spectrum capable with the **PCI_CLKn** clocks. **LPC_CLK1** can be used as a second LPC or extra PCI clock.
PCI_CLK[5:0]	33	O	**PCI Output Clocks** These are the six in-phase 33 MHz PCI bus clock outputs. These clocks are intended for the five external PCI devices or slots [4:0] and one loop back [5] for the NVIDIA nForce4 Ultra. They provide the timing reference for all transactions on the PCI bus. Together, these clocks are spread spectrum capable.
PCI_CLKFB **(PCI_CLK5)**	33	I	**PCI Clock In** This is the looped-back PCI clock signal that is used internally.
PE_REFCLK_IN **PE_REFCLK_IN#**	100	I	**PCI Express Reference Clock Input** This differential reference clock can be used for the 100 MHz PCI Express reference clocks.
PE[3:0]_REFCLK **PE[3:0]_REFCLK#**	100	O	**PCI Express Reference Clock Output** These signals are the PCI Express reference clock outputs for the PCI Express slots.

Clock Signal	Frequency (in MHz unless noted)	I/O	Description
RGMII_RXCLK/ MII_RXCLK	125/25/2.5	I	**RGMII/MII Received Clock** This is the continuous clock that provides the timing reference for the transfer of the **RGMII_RXCTL** and **RGMII_RXD[3:0]** signals in RGMII mode. In MII mode, it provides the timing reference for the transfer of the **MII_RXDV**, **MII_RXER**, and **MII_RXD[3:0]** signals.
RGMII_TXCLK/ MII_TXCLK	125 25/2.5	O I	**RGMII Transmit Clock** This is the continuous clock that provides the timing reference for the transfer of the **RGMII_TXCTL** and **RGMII_TXD[3:0]** signals in RGMII mode. In MII mode, it provides the timing reference for the transfer of the **MII_TXEN** and **MII_TXD[3:0]** signals. This clock is an output in RGMII and an input in MII mode.
SP_REFCLKP **SP_REFCLKN**	200/150/100	I	**SATA 2 Reference Clock** These pins are for the optional external reference clock for the internal SATA 2 PHY. The PLL can accept a 200 MHz, 150 MHz, or 100 MHz external reference clock. The default reference clock for the SATA 2 PLL is generated internally by the NVIDIA nForce4 Ultra. If the internal clock is used as the reference clock for the PLL, then these pins should be left floating. Please refer to the *nForce4 (CrushK8-04) Design Guide*.
SUSCLK	32.768 kHz	O	**SUSCLK Output** This signal is active in S0-S5 states (when VAUX is on) and is used by external devices.
XTAL_IN	25	I	**25 MHz Crystal Input** This is used by the internal clock synthesizer to generate all internal clocks. It is connected to a 25 MHz crystal. This signal is a no-connect when **XTAL_OUT** is driven by a CMOS clock driver.
XTAL_OUT	25	O	**25 MHz Crystal Output** This is connected to a 25 MHz crystal. It can also be driven by a CMOS clock driver with a 25 MHz frequency.
XTALIN_RTC	32.768 kHz	I	**RTC Crystal Input** This is connected to a 32.768 kHz crystal. It can also be driven by a CMOS clock driver with a 32.768 kHz frequency.
XTALOUT_RTC	32.768 kHz	O	**RTC Crystal Output** This is connected to a 32.768 kHz crystal. This signal is a no-connect when **XTALIN_RTC** is driven by a CMOS clock driver.

Chapter 4.
Power and System Management

Power and System Management

System Power State Controller

The NVIDIA nForce4 Ultra system power state controller supports the states listed in Table 33. The state names generally match the corresponding ACPI states.

Table 33. Power Management States

Global State	Sleep/CPU State	VDD	VAUX	VRTC	Notes
G0	C0	On	On	On	Full On (FON)
G0	C1	On	On	On	CPU Halt
G0	C2	On	On	On	CPU Stop Grant (CPU cache may be snooped)
G0	C3	On	On	On	CPU Stop Grant (CPU cache may not be snooped)
G1	S1	On	On	On	Power On Suspend (POS)
G1	S3	Off	On	On	Suspend to RAM (STR)
G1	S4	Off	On	On	Suspend to Disk (STD)
G2	S5	Off	On	On	Soft Off (SOFF)
G3		Off	Off	On	Mechanical Off (MOFF)

VDD +5 V (IO 5 V), +3.3 V (IO 3.3 V), +1.5 V (Core 1.5 V), +1.2V_HT (HyperTransport 1.2 V)
VAUX +3.3V_DUAL (IO 3.3V), +1.5V_DUAL (Core 1.5 V)
VRTC +3.3V_VBAT (RTC Battery 3.3 V)

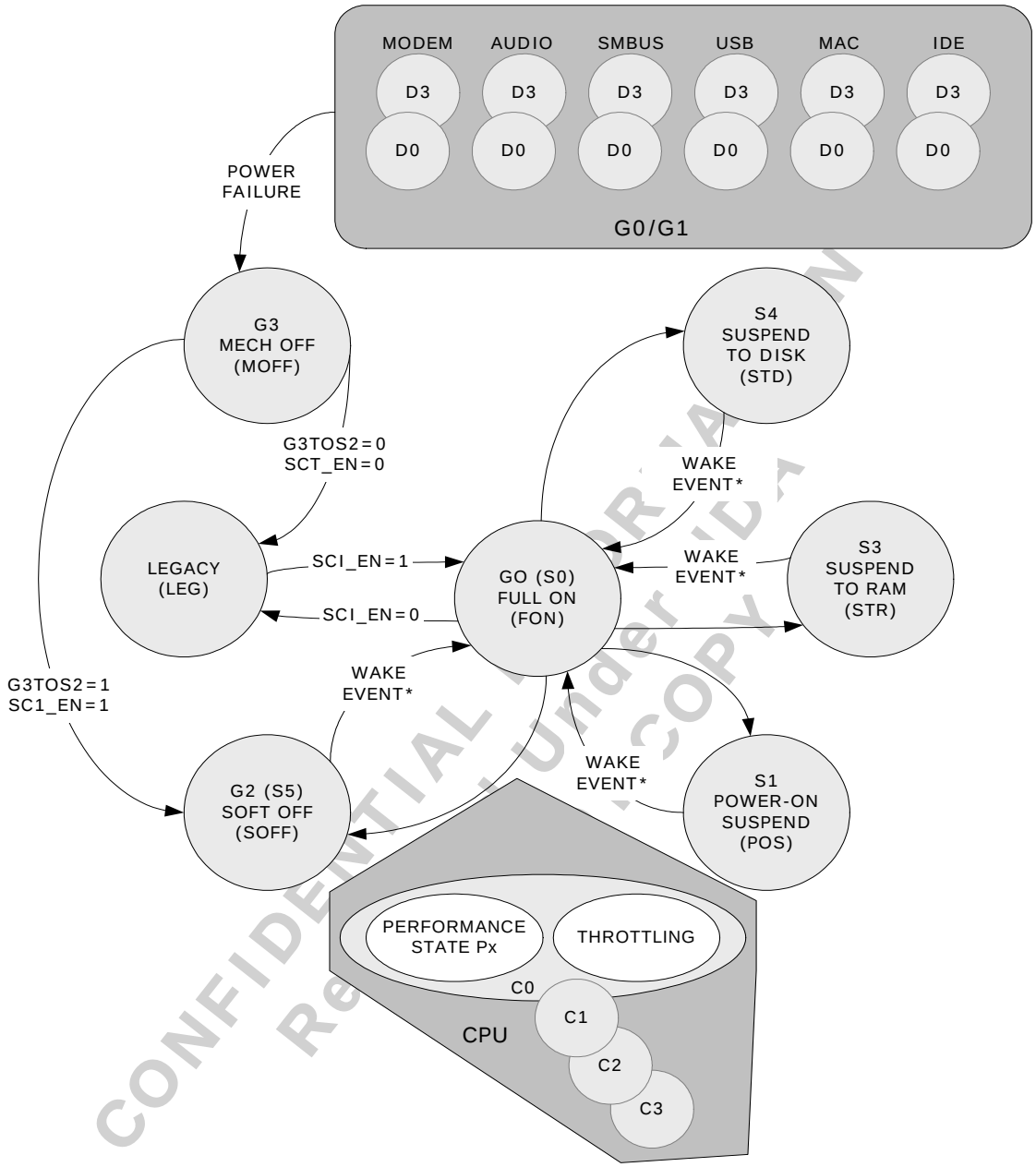

Figure 3. Power Management State Diagram

If software enabled the transition from S0 -> S5, then a software enabled event or a power button push is allowed to cause the wake event.

If a power button override (holding power button for four seconds) caused the transition into S5, then only a power button push can cause the wake event.

Figure 4 displays a block diagram of power management states and Table 35 describes each state control signal.

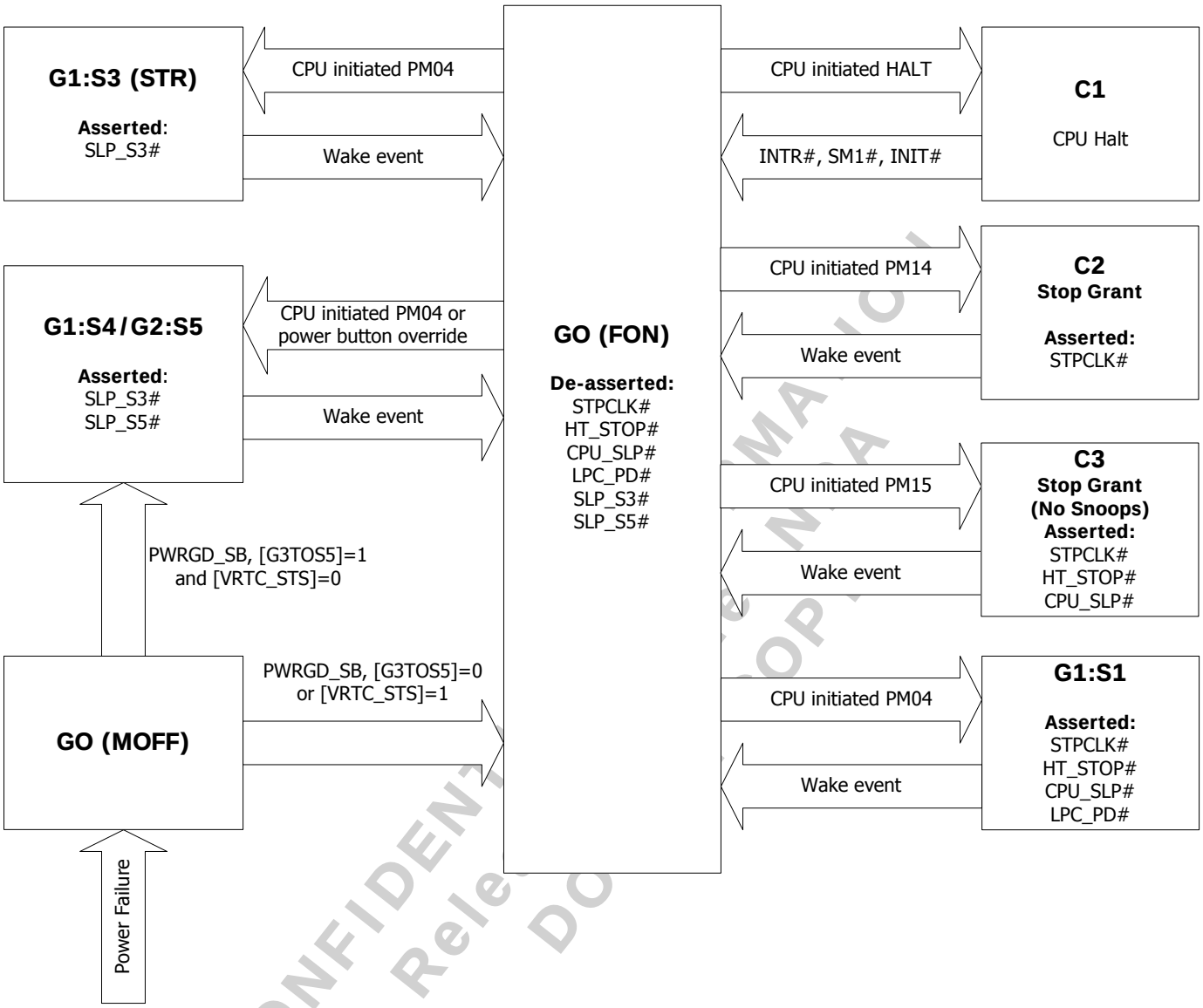

Figure 4. Power Management State Block Diagram

Table 34. Power Management State Control Signals

Signal	Description
PWRGD_SB	**Standby Power Stable** This signal will go high 1 ms (min) after the standby voltage (VAUX) is stable. This is used as a reset signal for the logic powered in the VAUX plane.
PWRGD	**Power Rail Stable** This signal is from the ATX power supply and is used to signal that the standard VDD power supply rails are stable.
SLP_S3#	**Sleep State 3** This signal is used to denote that the system is in an S3 sleep state. It is used to power off many of the standard power planes after they have been properly shut down.
SLP_S5#	**Sleep State 4/5** This signal is used to denote that the system is in an S4 or S5 sleep state. Since the two states are the same for the hardware, no differentiation is made. This signal will be used to remove power from system memory.

G0/S0/C0: Full On

Full on (FON) is the state in which all power planes are powered and the CPU is not in the stop-grant state.

G0/S0/C1: CPU Halt

The CPU can place itself in this state by issuing a halt command. Any Interrupt, NMI, or SMI will cause the CPU to wake up. No NVIDIA nForce4 Ultra support is needed to invoke this mode.

G0/S0/C2: CPU Stop Grant

In C2, the NVIDIA nForce4 Ultra places the CPU into the stop-grant state through the appropriate HyperTransport protocol system management message. The CPU's cache may be snooped while in this state. Any Interrupt, NMI, or SMI will cause the NVIDIA nForce4 Ultra to take the CPU out of the stop-grant state and exit C2.

G0/S0/C3: CPU Stop Grant

In C3, the NVIDIA nForce4 Ultra places the CPU into the stop-grant state through the appropriate HyperTransport protocol system management message. The CPU's cache may not be snooped while in this state. The HyperTransport link between the NVIDIA nForce4 Ultra and CPU will be disconnected. Any Interrupt, NMI or SMI will cause the NVIDIA nForce4 Ultra to reconnect the HyperTransport link, take the CPU out of the stop-grant state, and exit C3. Also, any bus master activity will require the NVIDIA nForce4 Ultra to take the system out of the C3 state so the CPU can snoop the request.

G1/S1: Power on Suspend

All power planes are fully powered in G1:S1 (POS). The CPU is in the stop-grant state.

G1/S3: Suspend to RAM (STR)

The system context is maintained in system memory and the main VDD outputs of the power supply are shut off. The NVIDIA nForce4 Ultra treats S3 similarly to S4 and S5. The main difference is that the NVIDIA nForce4 Ultra keeps **SLP_S5#** de-asserted when in S3. The **SLP_S5#** signal should be used to control the power of the memory.

G1/S4: Suspend to Disk (STD)

The system context is maintained on the disk. This state is functionally equivalent to G2:S5 (SOFF). The difference lies in which wake events are enabled and in the resume path. The system context will be loaded from the disk directly into memory, bypassing much of the normal boot process.

G2/S5: Soft Off (SOFF)

The VAUX planes are powered, but VDD planes are not. System context is not maintained because the VDD power planes are not being powered. **SLP_S3#** and **SLP_S5#** are both asserted, turning off all major power planes. The system normally uses **PWRBTN#** to transition from G2 to G0. However, the NVIDIA nForce4 Ultra may also use other wake events, including SMBus activity, USB resume events, the Real Time Clock alarm, the **EXT_SMI#** signal, the **SIO_PME#** signal, other internal PME events such as the modem wake-on ring, and other GPIO events.

G3: Mechanical OFF (MOFF)

G3 is the state when there is no VDD or VAUX power, just VRTC power. This can happen at any time, from any state, due to the loss of power to the VAUX planes—for example, during a power outage, if the power supply cable is unplugged, or if the power supply's mechanical switch fails. System context is not maintained due to power not being available. When power is applied to VAUX, the system transitions to either S0 or SOFF, depending on settings within the VRTC registers.

CPU Control Logic

CPU control logic refers to the use of clock throttling. Clock throttling is the act of placing the CPU into a stop-grant mode for a specified percentage of time in order to reduce the power being consumed by the CPU. Once throttling is started, the CPU is placed into stop-grant and taken out of stop-grant within a period of 244 µs and a duty cycle, as specified by the control registers.

Two types of throttling are possible, normal and thermal. Normal throttling is controlled by software. Thermal throttling is controlled by the **THERM#** signal. If both are enabled to occur at the same time, the duty cycle specified for thermal throttling is used. Throttling is ignored in the S1, S3, and S5 (POS, STR, SOFF) system power states and the C2/C3 CPU power states. If throttling is enabled when entering these states, it will stop once the state is entered; after exiting the state, throttling will continue.

Total Cost of Ownership

NVIDIA nForce4 Ultra includes simple total cost of ownership (TCO) functions:

- **INTRUDER#** support
- **EXT SMI#** generation

Custom TCO features are used in conjunction with the ACPI BIOS.

System Management Bus

The SMBus is ACPI-EC compatible.

The SMBus unit can generate interrupts and wake events. Interrupts are generated when the device is operational. The SMBus can generate wake events while in D3. General events are used for enumeration and other motherboard-related events.

The host-as-slave controller operates in all power states except G3 (MOFF). This can be used to generate interrupts that wake the system and bring it back to G0 (FON).

Chapter 5. Pin States

Signal Connections

Table 35 lists the signal connections and Table 36 list the signal states.

Table 35. Signal Connections

Notes: I/O = Bidirectional OD = Open Drain I = Input O = Output OC = Open Collector

Signal				
Primary	**Secondary**	**I/O**	**Voltage Tolerance Rail**	**Voltage Drive Rail**
HT_REQ#	GPIO_10	I/O	+3.3V	+3.3V
HT_STOP#		OD	+3.3V	
HT_RXCLK[1:0] **HT_RXCLK[1:0]#**		DIFF IN	+1.2V_HT	
HT_RXCTL **HT_RXCTL#**		DIFF IN	+1.2V_HT	
HT_RXD[15:0] **HT_RXD[15:0]#**		DIFF IN	+1.2V_HT	
HT_TXCLK[1:0] **HT_TXCLK[1:0]#**		DIFF OUT	+1.2V_HT	+1.2V_HT
HT_TXCTL **HT_TXCTL#**		DIFF OUT	+1.2V_HT	+1.2V_HT
HT_TXD[15:0] **HT_TXD[15:0]#**		DIFF OUT	+1.2V_HT	+1.2V_HT
A20GATE	GPIO_40	I/O	+3.3V	+3.3V
CPU_PWROK		OD	+3.3V	
CPU_RST#		OD	+3.3V_DUAL	
THERMTRIP#	GPIO_26	I/O	+3.3V	+3.3V
PE0_PRSNT#		I	+3.3V	
PE0_REFCLK **PE0_REFCLK#**		DIFF OUT	+3.3V	+3.3V
PE0_RX[15:0] **PE0_RX[15:0]#**		DIFF IN	+1.5V_PE_A	

Notes: I/O = Bidirectional OD = Open Drain I = Input O = Output OC = Open Collector				
Signal				
Primary	**Secondary**	**I/O**	**Voltage Tolerance Rail**	**Voltage Drive Rail**
PE0_TX[15:0] **PE0_TX[15:0]#**		DIFF OUT	+1.5V_PE_A	+1.5V_PE_A
PE1_PRSNT#		I	+3.3V	
PE1_REFCLK **PE1_REFCLK#**		DIFF OUT	+3.3V	+3.3V
PE1_RX **PE1_RX#**		DIFF IN	+1.5V_PE_A	
PE1_TX **PE1_TX#**		DIFF OUT	+1.5V_PE_A	+1.5V_PE_A
PE2_PRSNT#		I	+3.3V	
PE2_REFCLK **PE2_REFCLK#**		DIFF OUT	+3.3V	+3.3V
PE2_RX **PE2_RX#**		DIFF IN	+1.5V_PE_A	
PE2_TX **PE2_TX#**		DIFF OUT	+1.5V_PE_A	+1.5V_PE_A
PE3_PRSNT#		I	+3.3V	
PE3_REFCLK **PE3_REFCLK#**		DIFF OUT	+3.3V	+3.3V
PE3_RX **PE3_RX#**		DIFF IN	+1.5V_PE_A	
PE3_TX **PE3_TX#**		DIFF OUT	+1.5V_PE_A	+1.5V_PE_A
PE4_RX **PE4_RX#**		DIFF IN	+1.5V_PE_A	
PE4_TX **PE4_TX#**		DIFF OUT	+1.5V_PE_A	+1.5V_PE_A
PE_REFCLK_IN **PE_REFCLK_IN#**		DIFF IN	+1.5V_PE_A	
PE_RST#		O	+3.3V	+3.3V
PE_WAKE#		I	+3.3V_DUAL	
PCI_AD[31:0]		I/O	+5V	+3.3V
PCI_C/BE#[3:0]		I/O	+5V	+3.3V
PCI_CLK[5:0]		O	+5V	+3.3V
PCI_CLKFB		I	+5V	
PCI_CLKRUN#	GPIO_9	I/O	+3.3V	+3.3V
PCI_DEVSEL#		I/O	+5V	+3.3V
PCI_FRAME#		I/O	+5V	+3.3V
PCI_GNT[1:0]#		O	+5V	+3.3V
PCI_GNT[4:2]#	GPIO_[46,17,8]	I/O	+5V	+3.3V

Notes: I/O = Bidirectional OD = Open Drain I = Input O = Output OC = Open Collector				
Signal				
Primary	Secondary	I/O	Voltage Tolerance Rail	Voltage Drive Rail
PCI_INT[Z:W]#		I	+5V	
PCI_IRDY#		I/O	+5V	+3.3V
PCI_PAR		I/O	+5V	+3.3V
PCI_PERR#	GPIO_38	I/O	+5V	+3.3V
PCI_PME#	GPIO_37	I/O	+3.3V_DUAL	+3.3V_DUAL
PCI_REQ[1:0]#		I	+5V	
PCI_REQ[4:2]#	GPIO_[45,16,6]	I/O	+5V	+3.3V
PCI_RESET[3:0]#		O	+3.3V_DUAL	+3.3V_DUAL
PCI_SERR#		I	+5V	
PCI_STOP#		I/O	+5V	+3.3V
PCI_TRDY#		I/O	+5V	+3.3V
SP_TXP[1:0] SP_TXN[1:0]		DIFF OUT	SP_1.5V_A	SP_1.5V_A
SP_RXP[1:0] SP_RXN[1:0]		DIFF IN	SP_1.5V_A	
SP_TXP[3:2] SP_TXN[3:2]		DIFF OUT	SP_1.5V_A	SP_1.5V_A
SP_RXP[3:2] SP_RXN[3:2]		DIFF IN	SP_1.5V_A	
SP_LED#	GPIO_19	I/O	+3.3V	+3.3V
RGMII_INTR/ MII_INTR	GPIO_11	I/O	+3.3V_DUAL	+3.3V_DUAL
RGMII_MDC MII_MDC		O	+3.3V_DUAL	+3.3V_DUAL
RGMII_MDIO/ MII_MDIO		I/O	+3.3V_DUAL	+3.3V_DUAL
RGMII_PWRDWN/ MII_PWRDWN	GPIO_20	I/O	+3.3V_DUAL	+3.3V_DUAL
RGMII_RXCLK/ MII_RXCLK		I	+3.3V_DUAL	
RGMII_RXCTL/ MII_RXDV		I	+3.3V_DUAL	
RGMII_RXD[3:0]/ MII_RXD[3:0]		I	+3.3V_DUAL	
RGMII_TXCLK/ MII_TXCLK		O/I	+3.3V_DUAL	+3.3V_DUAL
RGMII_TXCTL/ MII_TXEN		O	+3.3V_DUAL	+3.3V_DUAL
RGMII_TXD[3:0]/ MII_TXD[3:0]		O	+3.3V_DUAL	+3.3V_DUAL
MII_COL		I	+3.3V_DUAL	
MII_CRS		I	+3.3V_DUAL	

Notes: I/O = Bidirectional OD = Open Drain I = Input O = Output OC = Open Collector				
Signal				
Primary	Secondary	I/O	Voltage Tolerance Rail	Voltage Drive Rail
MII_RXER	GPIO_21	I/O	+3.3V_DUAL	+3.3V_DUAL
USB_[9:0] USB_[9:0]#		DIFF I/O	+3.3V_USB_DUAL	+3.3V_USB_DUAL
USB_OC0#		I	+3.3V_DUAL	
USB_OC[4:1]#	GPIO_[25:22]	I/O	+3.3V_DUAL	+3.3V_DUAL
IDE_ADDR_P[2:0]		O	+5V	+3.3V
IDE_CS1_P#		O	+5V	+3.3V
IDE_CS3_P#		O	+5V	+3.3V
IDE_DACK_P#		O	+5V	+3.3V
IDE_DATA_P[15:0]		I/O	+5V	+3.3V
IDE_DREQ_P		I	+5V	
IDE_INTR_P		I	+5V	
IDE_IOR_P#		O	+5V	+3.3V
IDE_IOW_P#		O	+5V	+3.3V
IDE_RDY_P		I	+5V	
CABLE_DET_P		I	+5V	
IDE_ADDR_S[2:0]		O	+5V	+3.3V
IDE_CS1_S#		O	+5V	+3.3V
IDE_CS3_S#		O	+5V	+3.3V
IDE_DACK_S#		O	+5V	+3.3V
IDE_DATA_S[15:0]		I/O	+5V	+3.3V
IDE_DREQ_S		I	+5V	
IDE_INTR_S		I	+5V	
IDE_IOR_S#		O	+5V	+3.3V
IDE_IOW_S#		O	+5V	+3.3V
IDE_RDY_S		I	+5V	
CABLE_DET_S		I	+5V	
SMB_CLK0	GPIO_41	I/O	+3.3V_DUAL	+3.3V_DUAL
SMB_CLK1	GPIO_43	I/O	+3.3V_DUAL	+3.3V_DUAL
SMB_DATA0	GPIO_42	I/O	+3.3V_DUAL	+3.3V_DUAL
SMB_DATA1	GPIO_44	I/O	+3.3V_DUAL	+3.3V_DUAL
AC97_CLK		O	+3.3V	+3.3V
AC_BITCLK		I	+3.3V	
AC_RESET#	STRAP	O	+3.3V_DUAL	+3.3V_DUAL
AC_SDATA_IN0	GPIO_14	I/O	+3.3V_DUAL	+3.3V_DUAL
AC_SDATA_IN1	GPIO_27	I/O	+3.3V_DUAL	+3.3V_DUAL
AC_SDATA_OUT	GPIO_13/ STRAP	I/O	+3.3V	+3.3V

Notes: I/O = Bidirectional OD = Open Drain I = Input O = Output OC = Open Collector				
Signal				
Primary	Secondary	I/O	Voltage Tolerance Rail	Voltage Drive Rail
AC_SYNC	GPIO_12/ STRAP	I/O	+3.3V	+3.3V
LPC_AD[3:0]		I/O	+3.3V	+3.3V
LPC_CLK[1:0]		O	+3.3V	+3.3V
LPC_CS#	LPC_DRQ1#	I/O	+3.3V	+3.3V
LPC_DRQ0#		I	+3.3V	
LPC_FRAME#	STRAP	I/O	+3.3V	+3.3V
LPC_PWRDWN#	GPIO_39	I/O	+3.3V	+3.3V
LPC_RESET#		O	+3.3V_DUAL	+3.3V_DUAL
SERIRQ		I/O	+3.3V	+3.3V
BUF_25MHZ		O	+3.3V_DUAL	+3.3V_DUAL
BUF_SIO_CLK		O	+3.3V	+3.3V
CPU_CLK CPU_CLK#		DIFF OUT	+3.3V	+3.3V
SUSCLK	GPIO_31	I/O	+3.3V_DUAL	+3.3V_DUAL
XTAL_IN		I	+3.3V_DUAL	
XTAL_OUT		O	+3.3V_DUAL	+3.3V_DUAL
XTALIN_RTC		I	+3.3V_VBAT	
XTALOUT_RTC		O	+3.3V_VBAT	+3.3V_VBAT
EXT_SMI#	GPIO_29	I/O	+3.3V_DUAL	+3.3V_DUAL
FANCTL[1:0]	GPIO_[36,35]	I/O	+3.3V	+3.3V
FANRPM	GPIO_34	I/O	+3.3V	+3.3V
INTRUDER#		I	+3.3V_VBAT	
KBDRSTIN#	GPIO_18	I/O	+3.3V	+3.3V
PWRBTN#		I	V3P3_DEEP	
PWRGD		I	+3.3V_DUAL	
PWRGD_SB		I	+3.3V_DUAL	
RSTBTN#		I	+3.3V_DUAL	
RI#	GPIO_30	I/O	+3.3V_DUAL	+3.3V_DUAL
RTC_RST#		I	+3.3V_VBAT	
SLP_S3#		O	+3.3V_DUAL	+3.3V_DUAL
SLP_S5#		O	+3.3V_DUAL	+3.3V_DUAL
SIO_PME#	GPIO_28	I/O	+3.3V_DUAL	+3.3V_DUAL
THERM#	GPIO_32	I/O	+3.3V	+3.3V
SP_ATEST		I	SP_1.5V_A	
SPDIF0	GPIO_33/ STRAP	I/O	+3.3V	+3.3V
SPDIF1	GPIO_15/ STRAP	I/O	+3.3V	+3.3V

Notes: I/O = Bidirectional OD = Open Drain I = Input O = Output OC = Open Collector				
Signal				
Primary	Secondary	I/O	Voltage Tolerance Rail	Voltage Drive Rail
SPKR	STRAP	I/O	+3.3V	+3.3V
TEST		I	+3.3V	
PE_CLK_TEST PE_CLK_TEST#		DIFF OUT	+1.5V_PE_A	+1.5V_PE_A
SP_TESTP SP_TESTN		DIFF OUT	SP_1.5V_A	SP_1.5V_A
MEM_VLD		I	+3.3V_DUAL	
HT_VLD		I	+3.3V_DUAL	
CPU_VLD		I	+3.3V_DUAL	
HTVDD_EN		O	+3.3V_DUAL	+3.3V_DUAL
CPUVDD_EN		O	+3.3V_DUAL	+3.3V_DUAL
LID#	GPIO_7	I/O	+3.3V_DUAL	+3.3V_DUAL
LLB#		I	+3.3V_DUAL	
SLP_DEEP#		O	V3P3_DEEP	V3P3_DEEP
GPIO_5		I/O	+3.3V_DUAL	+3.3V_DUAL
GPIO_4	SUS_STAT#	I/O	+3.3V_DUAL	+3.3V_DUAL
GPIO_3	CPU_CLKRUN#	I/O	+3.3V	+3.3V
GPIO_2	CPU_SLP#	I/O	+3.3V	+3.3V
GPIO_1		I/O	+3.3V	+3.3V

Signal States

Table 36. Signal States

Notes: Z = Tri-state I/O = Bidirectional I = Input O = Output
OC = Open Collector OD = Open Drain U = Unpowered L = Low H=High

Signal		Primary					Secondary				
Primary	**Secondary**	**During Reset**	**After RST (SO)**	**S1 (POS)**	**S3 (STR)**	**S4/S5 (SOFF)**	**During Reset**	**After ST (S0)**	**S1 (POS)**	**S3 (STR)**	**S4/S5 (SOFF)**
HT_REQ#	GPIO_10	I	I	I	U	U	I/O	I/O	I/O	U	U
HT_STOP#		O	O	L	U	U					
HT_RXCLK[1:0] **HT_RXCLK[1:0]#**		I	I	I	U	U					
HT_RXCTL **HT_RXCTL#**		I	I	I	U	U					
HT_RXD[15:0] **HT_RXD[15:0]#**		I	I	I	U	U					
HT_TXCLK[1:0] **HT_TXCLK[1:0]#**		O	O	O	U	U					
HT_TXCTL **HT_TXCTL#**		Z	O	O	U	U					
HT_TXD[15:0] **HT_TXD[15:0]#**		Z	O	O	U	U					
PE0_PRSNT#		I	I	I	U	U					
PE0_REFCLK **PE0_REFCLK#**		O	O	O	U	U					
PE0_RX[15:0] **PE0_RX[15:0]#**		I	I	I	U	U					
PE0_TX[15:0] **PE0_TX[15:0]#**		Z	O	O	U	U					
PE1_PRSNT#		I	I	I	U	U					
PE1_REFCLK **PE1_REFCLK#**		O	O	O	U	U					
PE1_RX **PE1_RX#**		I	I	I	U	U					
PE1_TX **PE1_TX#**		Z	O	O	U	U					
PE2_PRSNT#		I	I	I	U	U					
PE2_REFCLK **PE2_REFCLK#**		O	O	O	U	U					
PE2_RX **PE2_RX#**		I	I	I	U	U					
PE2_TX **PE2_TX#**		Z	O	O	U	U					

Notes: Z = Tri-state I/O = Bidirectional I = Input O = Output
OC = Open Collector OD = Open Drain U = Unpowered L = Low H=High

Signal		Primary					Secondary				
Primary	Secondary	During Reset	After RST (SO)	S1 (POS)	S3 (STR)	S4/S5 (SOFF)	During Reset	After ST (S0)	S1 (POS)	S3 (STR)	S4/S5 (SOFF)
PE3_PRSNT#		I	I	I	U	U					
PE3_REFCLK **PE3_REFCLK#**		O	O	O	U	U					
PE3_RX **PE3_RX#**		I	I	I	U	U					
PE3_TX **PE3_TX#**		Z	O	O	U	U					
PE4_RX **PE4_RX#**		I	I	I	U	U					
PE4_TX **PE4_TX#**		Z	O	O	U	U					
PE_REFCLK_IN **PE_REFCLK_IN#**		I	I	I	U	U					
PE_RST#		O	O	O	U	U					
PE_WAKE#		I	I	I	I	I					
PCI_AD[31:0]		Z	I/O	I/O	U	U					
PCI_C/BE#[3:0]		Z	I/O	I/O	U	U					
PCI_CLK[5:0]		O	O	O	U	U					
PCI_CLKFB		I	I	I	U	U					
PCI_CLKRUN#	GPIO_9	Z	I/O	I	U	U	I/O	I/O	I/O	I/O	I/O
PCI_DEVSEL#		Z	I/O	I/O	U	U					
PCI_FRAME#		Z	I/O	I/O	U	U					
PCI_GNT[1:0]#		H	O	H	U	U					
PCI_GNT[4:2]#	GPIO_[46,17,8]	H	O	H	U	U	I/O	I/O	I/O	U	U
PCI_INT[Z:W]#		I	I	I	U	U					
PCI_IRDY#		Z	I/O	I/O	U	U					
PCI_PAR		Z	I/O	I/O	U	U					
PCI_PERR#	GPIO_38	I	I	I	U	U	I/O	I/O	I/O	U	U
PCI_PME#	GPIO_37	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O
PCI_REQ[1:0]#		I	I	I	U	U					
PCI_REQ[4:2]#	GPIO_[45,16,6]	I	I	I	U	U	I/O	I/O	I/O	U	U
PCI_RESET [3:0]#		O	O	O	O	O					
PCI_SERR#		I	I	I	U	U					
PCI_STOP#		Z	I/O	I/O	U	U					
PCI_TRDY#		Z	I/O	I/O	U	U					
SMB_CLK0	GPIO_41	OD	OD	OD	OD	OD	I/O	I/O	I/O	I/O	I/O
SMB_CLK1	GPIO_43	OD	OD	OD	OD	OD	I/O	I/O	I/O	I/O	I/O
SMB_DATA0	GPIO_42	OD	OD	OD	OD	OD	I/O	I/O	I/O	I/O	I/O

Notes: Z = Tri-state I/O = Bidirectional I = Input O = Output
OC = Open Collector OD = Open Drain U = Unpowered L = Low H=High

Signal		Primary					Secondary				
Primary	**Secondary**	**During Reset**	**After RST (SO)**	**S1 (POS)**	**S3 (STR)**	**S4/S5 (SOFF)**	**During Reset**	**After ST (S0)**	**S1 (POS)**	**S3 (STR)**	**S4/S5 (SOFF)**
SMB_DATA1	GPIO_44	OD	OD	OD	OD	OD	I/O	I/O	I/O	I/O	I/O
IDE_ADDR_P[2:0]		L	O	O	U	U					
IDE_CS1_P#		H	O	O	U	U					
IDE_CS3_P#		H	O	O	U	U					
IDE_DACK_P#		H	O	O	U	U					
IDE_DATA_P[15:0]		Z	I/O	I/O	U	U					
IDE_DREQ_P		I	I	I	U	U					
IDE_INTR_P		I	I	I	U	U					
IDE_IOR_P#		H	O	O	U	U					
IDE_IOW_P#		H	O	O	U	U					
IDE_RDY_P		I	I	I	U	U					
CABLE_DET_P		I	I	I	U	U					
IDE_ADDR_S[2:0]		L	O	O	U	U					
IDE_CS1_S#		H	O	O	U	U					
IDE_CS3_S#		H	O	O	U	U					
IDE_DACK_S#		H	O	O	U	U					
IDE_DATA_S[15:0]		Z	I/O	I/O	U	U					
IDE_DREQ_S		I	I	I	U	U					
IDE_INTR_S		I	I	I	U	U					
IDE_IOR_S#		H	O	O	U	U					
IDE_IOW_S#		H	O	O	U	U					
IDE_RDY_S		I	I	I	U	U					
CABLE_DET_S		I	I	I	U	U					
SP_TXP[1:0] **SP_TXN[1:0]**		Z	O	O	U	U					
SP_RXP[1:0] **SP_RXN[1:0]**		I	I	I	U	U					
SP_TXP[1:0] **SP_TXN[1:0]**		Z	O	O	U	U					
SP_RXP[1:0] **SP_RXN[1:0]**		I	I	I	U	U					
SP_LED#	GPIO_19	Z	OD	OD	U	U	I/O	I/O	I/O	I/O	I/O
SP_REFCLKP **SP_REFCLKN**		I	I	I	U	U					
RGMII_INTR/ **MII_INTR**	GPIO_11	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O
RGMII_MDC **MII_MDC**		O	O	O	O	O					

Notes: Z = Tri-state I/O = Bidirectional I = Input O = Output
OC = Open Collector OD = Open Drain U = Unpowered L = Low H=High

Signal		Primary					Secondary				
Primary	**Secondary**	**During Reset**	**After RST (SO)**	**S1 (POS)**	**S3 (STR)**	**S4/S5 (SOFF)**	**During Reset**	**After ST (S0)**	**S1 (POS)**	**S3 (STR)**	**S4/S5 (SOFF)**
RGMII_MDIO/ MII_MDIO		I/O	I/O	I/O	I/O	I/O					
RGMII_PWRDWN/ MII_PWRDWN	GPIO_20	O	O	O	O	O	I/O	I/O	I/O	I/O	I/O
RGMII_RXCLK/ MII_RXCLK		I	I	I	I	I					
RGMII_RXD[3:0]/ MII_RXD[3:0]		I	I	I	I	I					
RGMII_RXCTL/ MII_RXDV		I	I	I	I	I					
RGMII_TXCLK/ MII_TXCLK		O/I	O/I	O/I	O/I	O/I					
RGMII_TXCTL/ MII_TXEN		O	O	O	O	O					
RGMII_TXD[3:0]/ MII_TXD[3:0]		O	O	O	O	O					
MII_CRS		I	I	I	I	I					
MII_COL		I	I	I	I	I					
MII_RXER	GPIO_21	O	O	O	O	O	I/O	I/O	I/O	I/O	I/O
LPC_AD[3:0]		Z	I/O	I/O	U	U					
LPC_CLK[1:0]		O	O	O	U	U					
LPC_CS#	LPC_DRQ1#	H	O	O	U	U	H	I	I	U	U
LPC_DRQ0#		I	I	I	U	U					
LPC_FRAME#	STRAP	Z	O	O	U	U					
LPC_PWRDWN#	GPIO_39	O	O	O	U	U	I/O	I/O	I/O	U	U
LPC_RESET#		L	H	H	L	L					
SERIRQ		Z	I	I	Z	Z					
USB_[9:0] USB_[9:0]#		Z	I/O	Z	Z	Z					
USB_OC0#		I	I	I	I	I					
USB_OC[4:1]#	GPIO_[25:22]	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O
AC97_CLK		O	O	O	O	L					
AC_BITCLK		I	I	I	Z	Z					
AC_RESET#	STRAP	L	O	O	Z	Z					
AC_SDATA_IN0	GPIO_14	I	I	I	Z	Z	I/ O	I/O	I/O	I/O	I/O
AC_SDATA_IN1	GPIO_27	I	I	I	Z	Z	I/O	I/O	I/O	I/O	I/O
AC_SDATA_OUT	GPIO_13/ STRAP	L	O	O	Z	Z	I/O	I/O	I/O	I/O	i/o
AC_SYNC	GPIO_12/ STRAP	L	O	O	Z	Z	I/O	I/O	I/O	I/O	I/ O

Notes: Z = Tri-state I/O = Bidirectional I = Input O = Output
OC = Open Collector OD = Open Drain U = Unpowered L = Low H=High

Signal		Primary					Secondary				
Primary	Secondary	During Reset	After RST (SO)	S1 (POS)	S3 (STR)	S4/S5 (SOFF)	During Reset	After ST (S0)	S1 (POS)	S3 (STR)	S4/S5 (SOFF)
BUF_25MHZ		O	O	O	O	O					
BUF_SIO_CLK		O	O	O	U	U					
CPU_CLK **CPU_CLK#**		O	O	O	U	U					
SUSCLK	GPIO_31	O	O	O	O	O	I/O	I/O	I/O	I/O	I/O
XTAL_IN		Z	Z	Z	Z	Z					
XTAL_OUT		O	O	O	O	O					
XTALIN_RTC		Z	Z	Z	Z	Z					
XTALOUT_RTC		O	O	O	O	O					
EXT_SMI#	GPIO_29	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O
FANCTL[1:0]	GPIO_[36,35]	L	O	O	U	U	I/O	I/O	I/O	U	U
FANRPM	GPIO_34	I	I	I	U	U	I/O	I/O	I/O	U	U
INTRUDER#		I	I	I	I	I					
KBDRSTIN#	GPIO_18	I	I	I	U	U	I/O	I/O	I/O	U	U
PWRBTN#		I	I	I	I	I					
PWRGD		I	I	I	I	I					
PWRGD_SB		I	I	I	I	I					
RTC_RST#		I	I	I	I	I					
RSTBTN#		I	I	I	I	I					
RI#	GPIO_30	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O
SLP_S3#		O	H	H	L	L					
SLP_S5#		O	H	H	H	L					
SIO_PME#	GPIO_28	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O
THERM#	GPIO_32	I	I	I	U	U	I/O	I/O	I/O	U	U
A20GATE	GPIO_40	I	I	I	U	U	I/O	I/O	I/O	U	U
CPU_PWROK		L	H	H	U	U					
CPU_RST#		L	H	H	L	L					
THERMTRIP#	GPIO_26	I	I	I	U	U	I/O	I/O	I/O	U	U
SP_ATEST		I	I	I	U	U					
SPDIF0	GPIO_33/ STRAP	Z	I/O	I/O	U	U	I/O	I/O	I/O	U	U
SPDIF1	GPIO_15/ STRAP	Z	I/O	I/O	U	U	I/O	I/O	I/O	U	U
SPKR	STRAP	Z	O	O	U	U					
TEST		I	I	I	U	U					
PE_CLK_TEST **PE_CLK_TEST#**		Z	O	O	U	U					

Notes: Z = Tri-state I/O = Bidirectional I = Input O = Output
OC = Open Collector OD = Open Drain U = Unpowered L = Low H=High

Signal		Primary					Secondary				
Primary	**Secondary**	**During Reset**	**After RST (SO)**	**S1 (POS)**	**S3 (STR)**	**S4/S5 (SOFF)**	**During Reset**	**After ST (S0)**	**S1 (POS)**	**S3 (STR)**	**S4/S5 (SOFF)**
SP_TESTP **SP_TESTN**		Z	I/O	I/O	U	U					
MEM_VLD		I	I	I	I	I					
HT_VLD		I	I	I	I	I					
CPU_VLD		I	I	I	I	I					
HTVDD_EN		O	O	O	O	O					
CPUVDD_EN		O	O	O	O	O					
LID#	GPIO_7	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O
LLB#		I	I	I	I	I					
SLP_DEEP#		O	O	O	O	O					
GPIO_5		I/O	I/O	I/O	I/O	I/O					
GPIO_4	SUS_STAT#	I/O	I/O	I/O	I/O	I/O	O	O	O	O	O
GPIO_3	CPU_CLKRUN#	I/O	I/O	I/O	I/O	I/O	I	I	I	U	U
GPIO_2	CPU_SLP#	I/O	I/O	I/O	I/O	I/O	O	O	O	U	U
GPIO_1		I/O	I/O	I/O	I/O	I/O					

Chapter 6. GPIO Information

GPIO Signals

The GPIO signals, shown in the following table, provide configurable settings for custom implementations. Other functionality of GPIO signals is ignored when these signals are enabled for GPIO.

Table 37. GPIO Signals

Control Register	Signal Name	Alternate Function	Default	Voltage Drive Rail	Voltage Tolerance Rail
C0h	**GPIO1**	GPIO_1	GPIO Input	+3.3V	+3.3V
C1h	**GPIO2**	CPU_SLP#	GPIO Input	+3.3V	+3.3V
C2h	**GPIO3**	CPU_CLKRUN#	GPIO Input	+3.3V	+3.3V
C3h	**GPIO4**	SUS_STAT#	GPIO Input	+3.3V_DUAL	+3.3V_DUAL
C4h	**GPIO5**	GPIO_5	GPIO Input	+3.3V_DUAL	+3.3V_DUAL
C5h	**PCI_REQ2#**	GPIO6	PCI_REQ2#	+3.3V	+5.0V
C6h	**LID#**	GPIO7	LID#	+3.3V_DUAL	+3.3V_DUAL
C7h	**PCI_GNT2#**	GPIO8	PCI_GNT2#	+3.3V	+5.0V
C8h	**PCI_CLKRUN#**	GPIO9	PCI_CLKRUN#	+3.3V	+3.3V
C9h	**HT_REQ#**	GPIO_10	HT_REQ#	+3.3V	+3.3V
CAh	**RGMII_INTR/ MII_INTR**	GPIO_11	RGMII_INTR/ MII_INTR	+3.3V_DUAL	+3.3V_DUAL
CBh	**AC_SYNC**	GPIO_12/ STRAP	AC_SYNC	+3.3V	+3.3V
CCh	**AC_SDATA_OUT**	GPIO_13/ STRAP	AC_SDATA_OUT	+3.3V	+3.3V
CDh	**AC_SDATA_IN0**	GPIO_14	GPIO Output Low	+3.3V_DUAL	+3.3V_DUAL
CEh	**SPDIF1**	GPIO_15/ STRAP	GPIO Input	+3.3V	+3.3V
CFh	**PCI_REQ3#**	GPIO_16	PCI_REQ3#	+3.3V	+5.0V
D0h	**PCI_GNT3#**	GPIO_17	PCI_GNT3#	+3.3V	+5.0V
D1h	**KBRDRSTIN#**	GPIO_18	KBRDRSTIN#	+3.3V	+3.3V

Control Register	Signal Name	Alternate Function	Default	Voltage Drive Rail	Voltage Tolerance Rail
D2h	**SP_LED#**	GPIO_19	SP_LED#	+3.3V	+3.3V
D3h	**RGMII_PWRDWN/ MII_PWRDWN**	GPIO_20	RGMII_PWRDWN/ MII_PWRDWN	+3.3V_DUAL	+3.3V_DUAL
D4h	**MII_RXER**	GPIO_21	MII_RXER	+3.3V_DUAL	+3.3V_DUAL
D5h	**USB_OC1#**	GPIO_22	USB_OC1#	+3.3V_DUAL	+3.3V_DUAL
D6h	**USB_OC2#**	GPIO_23	USB_OC2#	+3.3V_DUAL	+3.3V_DUAL
D7h	**USB_OC3#**	GPIO_24	USB_OC3#	+3.3V_DUAL	+3.3V_DUAL
D8h	**USB_OC4#**	GPIO_25	USB_OC4#	+3.3V_DUAL	+3.3V_DUAL
D9h	**THERMTRIP#**	GPIO_26	THERMTRIP#	+3.3V	+5.0V
DAh	**AC_SDATA_IN1**	GPIO_27	GPIO Output Low	+3.3V_DUAL	+3.3V_DUAL
DBh	**SIO_PME#**	GPIO_28	SIO_PME#	+3.3V_DUAL	+3.3V_DUAL
DCh	**EXT_SMI#**	GPIO_29	EXT_SMI#	+3.3V_DUAL	+3.3V_DUAL
DDh	**RI#**	GPIO_30	GPIO Input	+3.3V_DUAL	+3.3V_DUAL
DEh	**SUSCLK**	GPIO_31	SUSCLK	+3.3V_DUAL	+3.3V_DUAL
DFh	**THERM#**	GPIO_32	GPIO Input	+3.3V	+3.3V
E0h	**SPDIF0**	GPIO_33/ STRAP	GPIO Input	+3.3V	+3.3V
E1h	**FANRPM**	GPIO_34	FANRPM	+3.3V	+3.3V
E2h	**FANCTL0**	GPIO_35	FANCTL0	+3.3V	+3.3V
E3h	**FANCTL1**	GPIO_36	FANCTL1	+3.3V	+3.3V
E4h	**PCI_PME#**	GPIO_37	PCI_PME#	+3.3V_DUAL	+3.3V_DUAL
E5h	**PCI_PERR#**	GPIO_38	PCI_PERR#	+3.3V	+5.0V
E6h	**LPC_PWRDWN#**	GPIO_39/ STRAP	GPIO Input	+3.3V	+3.3V
E7h	**A20GATE**	GPIO_40	A20GATE	+3.3V_DUAL	+3.3V_DUAL
E8h	**SMB_CLK0**	GPIO_41	SMB_CLK0	+3.3V_DUAL	+3.3V_DUAL
E9h	**SMB_DATA0**	GPIO_42	SMB_DATA0	+3.3V_DUAL	+3.3V_DUAL
EAh	**SMB_CLK1**	GPIO_43	SMB_CLK1	+3.3V_DUAL	+3.3V_DUAL
EBh	**SMB_DATA1**	GPIO_44	SMB_DATA1	+3.3V_DUAL	+3.3V_DUAL
ECh	**PCI_REQ4#**	GPIO_45	PCI_REQ4#	+3.3V	+5.0V
EDh	**PCI_GNT4#**	GPIO_46	PCI_GNT4#	+3.3V	+5.0V

Chapter 7.
Power Sequencing and Reset

Power Sequencing and Reset Information

Please refer to the *nForce4 (CrushK8-04) Design Guide* as a lot of information pertaining to the Power Sequencing and RESET are dependent upon motherboard design implementations.

Chapter 8.
Mechanical Specifications

This chapter contains the package information for the NVIDIA nForce4 Ultra.

Table 38. PBGA Package Dimensions

Ref	Dimensions in Millimeter			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.25	2.50	2.65	0.089	0.098	0.104
A1	0.43	0.52	0.60	0.017	0.020	0.024
A2	0.82	0.87	0.95	0.032	0.034	0.037
A5	0.46	0.53	0.58	0.018	0.021	0.023
D/E	30.80	31.00	31.20	1.213	1.220	1.228
D1/E1	29.00 Basic			1.142 Basic		
Wx1	3.0 Typical			0.118 Typical		
Wx2	3.0 Typical			0.118 Typical		
Wy1	3.0 Typical			0.118 Typical		
Wy2	5.0 Typical			0.197 Typical		
e	1.00 Basic			0.038 Basic		
b	0.51	0.60	0.74	0.020	0.024	0.029
aaa	0.20			0.008		
ccc	0.35			0.014		
ddd	0.20			0.008		
eee	0.30			0.012		
fff	0.10			0.004		
Total Number of Balls: 740						
Package Size: 31 mm × 31 mm						

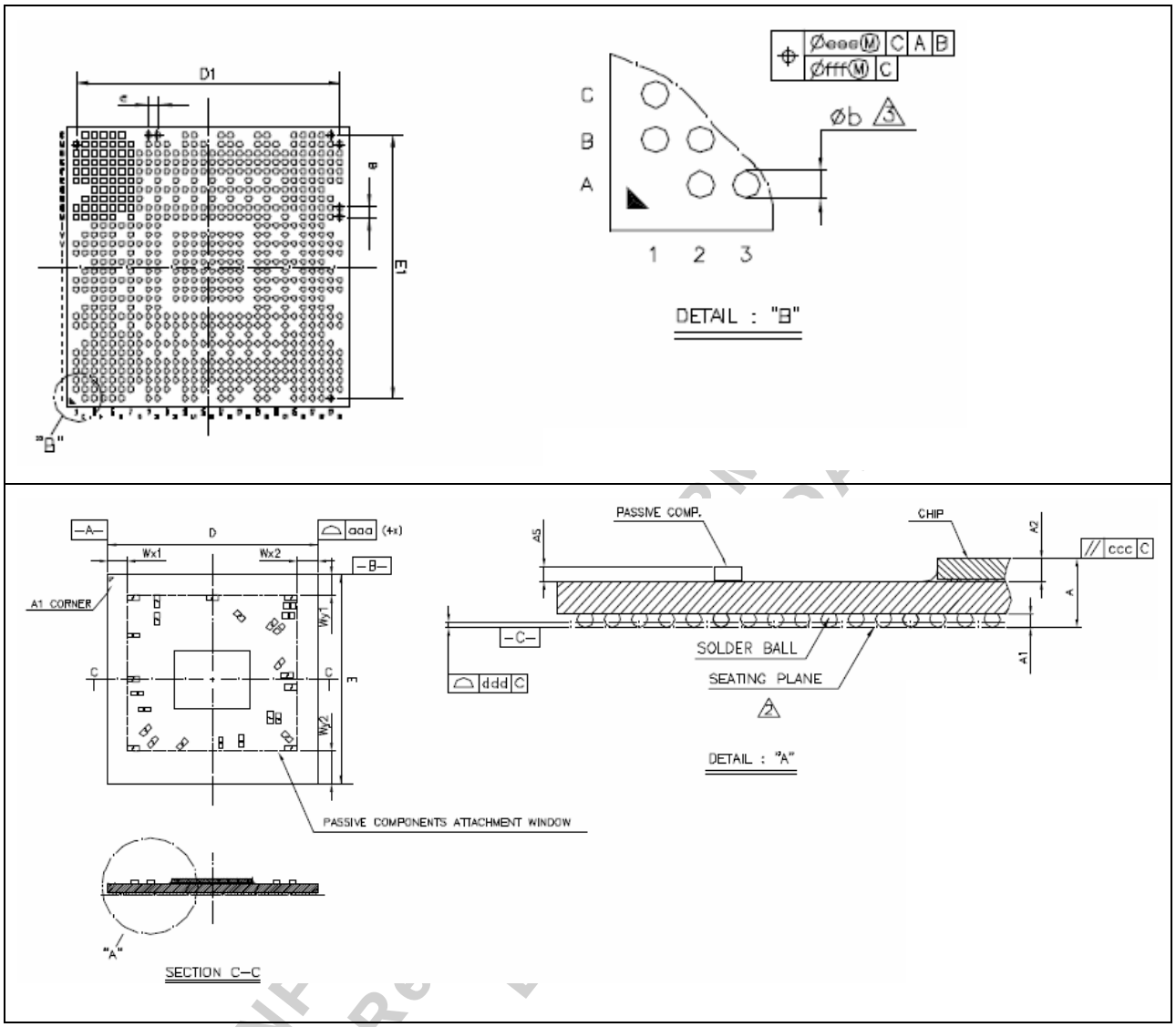

Figure 5. PBGA Package Description

1. Controlling dimension: Millimeter
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. There must be a minimum clearance of 0.38 mm (0.015 in.) between the edge of the solder ball and the body edge.

Chapter 9.
AC/DC Specifications

Absolute Ratings

The NVIDIA nForce4 Ultra should not be subjected to conditions exceeding the absolute maximum ratings listed in Table 39. Exceeding the conditions listed can damage the functionality and affect the long-term reliability of the part.

Table 39. Absolute Ratings

Parameter	Min	Max
Case temperature under bias	0 °C	103 °C
Storage temperature	-50 °C	150 °C
Voltage on any integrated SATA 2 pin with respect to ground	-0.5 V	1.0 V
Voltage on any 1.2 V pin with respect to ground	-0.5 V	1.3 V
Voltage on any 1.5 V pin with respect to ground	-0.5 V	1.65 V
Voltage on any 3.3 V pin with respect to ground	-0.5 V	3.465 V
Voltage on any 5.0 V pin with respect to ground	-0.5 V	5.5 V
1.2 V supply	-0.5 V	1.3 V
1.5V supply	-0.5 V	1.65 V
3.3 V supply	-0.5 V	3.465 V
5.0 V supply	-0.5 V	5.5 V
Maximum power dissipation	13.5 W	

Thermal Operations

The thermal operating temperature range is given in Table 40.

Table 40. Thermal Operating Temperature

Characteristic	Range
Thermal operating temperature (T_{CASE})	0° C to 90° C

DC Characteristics

This section contains the following DC specifications:

- Voltage characteristics
- Current characteristics
- Industry standard characteristics
- Other signal characteristics

DC Voltage Characteristics

Table 41 lists the power characteristics for NVIDIA nForce4 Ultra.

Table 41. Voltage Characteristics

Signal	Min	Max	Range
+1.2V_HT	1.14 V	1.26 V	± 0.6 V
+1.5V	1.4 V	1.6 V	± 0.1 V
+1.5V_DUAL	1.4 V	1.6V	± 0.1 V
+1.5V_PE_A	1.4 V	1.6 V	± 0.1 V
+1.5V_PE_D	1.4 V	1.6 V	± 0.1 V
+1.5V_PLL_HT	1.4 V	1.6 V	± 0.1 V
+1.5V_PLL_PE_AVDD	1.4 V	1.6 V	± 0.1 V
+1.5V_PLL_PE_CORE	1.4 V	1.6 V	± 0.1 V
+1.5V_PLL_PE_DVDD	1.4 V	1.6 V	± 0.1 V
+1.5V_PLL_SP_AVDD	1.4 V	1.6 V	± 0.1 V
+1.5V_PLL_SP_CORE	1.4 V	1.6 V	± 0.1 V
+1.5V_PLL_SP_DVDD	1.4 V	1.6 V	± 0.1 V
+1.5V_SP_A	1.4 V	1.6 V	± 0.1 V
+1.5V_SP_D	1.4 V	1.6 V	± 0.1 V
+3.3V	3.135 V	3.465 V	± 5%
+3.3V_DUAL	3.135 V	3.465 V	± 5%
+3.3V_PLL_CPU	3.135 V	3.465 V	± 5%
+3.3V_PLL_DUAL	3.135 V	3.465 V	± 5%
+3.3V_PLL_HT	3.135 V	3.465 V	± 5%
+3.3V_PLL_PE_CORE	3.135 V	3.465 V	± 5%
+3.3V_PLL_SP_CORE	3.135 V	3.465 V	± 5%
+3.3V_PLL_USB	3.135 V	3.465 V	± 5%
+3.3V_USB_DUAL	3.135 V	3.465 V	± 5%
+3.3V_VBAT	2.0 V	3.45 V	
+5V[1]	4.5 V	5.5 V	± 0.5 V
V3P3_DEEP	3.135 V	3.465 V	± 5%

Note: These rails are used for clamp protection on 5 V tolerant inputs and do not draw any current.

DC Current Characteristics

Table 42 lists the DC current characteristics measured under the following test conditions:

- Temperature = 25° C
- Voltage = Maximum
- Silicon = Fast

Table 42. DC Current Characteristics

Type	S0 Busy	S0 Idle	S1	S3	S5	G3
+1.2V_HT	300 mA	200 mA	200 mA	0	0	0
+1.5V	4500 mA	3200 mA	3200 mA	0	0	0
+1.5V_DUAL	120 mA	100 mA	100 mA	60 mA	60 mA	0
+1.5V_PE_A	2200 mA	2200 mA	1100 mA	0	0	0
+1.5V_PE_D	600 mA	600 mA	200 mA	0	0	0
+1.5V_PLL_HT	140 mA	140 mA	140 mA	0	0	0
+1.5V_PLL_PE_AVDD **+1.5V_PLL_PE_DVDD**	150 mA	150 mA	150 mA	0	0	0
+1.5V_PLL_PE_CORE	80 mA	80 mA	80 mA	0	0	0
+1.5V_PLL_SP_AVDD **+1.5V_PLL_SP_DVDD**	140 mA	140 mA	140 mA	0	0	0
+1.5V_PLL_SP_CORE	10 mA	10 mA	10 mA	0	0	0
+1.5V_SP_A	420 mA	420 mA	420 mA	0	0	0
+1.5V_SP_D	70 mA	70 mA	70 mA	0	0	0
+3.3V	150 mA	150 mA	150 mA	0	0	0
+3.3V_DUAL	55 mA	30 mA	30 mA	30 mA	30 mA	0
+3.3V_PLL_CPU	10 mA	10 mA	10 mA	0	0	0
+3.3V_PLL_DUAL	4 mA	4 mA	4 mA	4 mA	4 mA	0
+3.3V_PLL_HT	7 mA	7 mA	7 mA	0	0	0
+3.3V_PLL_PE_CORE	18 mA	18 mA	18 mA	0	0	0
+3.3V_PLL_SP_CORE	9 mA	9 mA	9 mA	0	0	0
+3.3V_PLL_USB	18 mA	18 mA	18 mA	0	0	0
+3.3V_USB_DUAL	100 mA	100 mA	100 mA	100 mA	100 mA	0
+3.3V_VBAT	5 mA	5 mA	5 mA	0.2 mA	0.2 mA	0.01 mA
+5V	50 mA	50 mA	50 mA	0	0	0
V3P3_DEEP	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0

Industry Standard DC Characteristics

Table 43 lists the industry-standard DC characteristics.

Table 43. Industry Standard DC Characteristics

Interface	Vcc		Vil		Vih		Vol	Voh
	Min	Max	Min	Max	Min	Max	Max	Min
PCI 5 V	4.75 V	5.25 V	-0.5 V	0.8 V	2.0 V	Vcc+0.5V	0.55 V	2.4 V
LPC PCI 3.3V	3.135 V	3.465 V	-0.5 V	0.3*Vcc	0.5*Vcc	Vcc+0.5V	0.1*Vcc	0.9*Vcc
AC'97	3.135 V	3.465 V	-0.3 V	0.35*Vcc	0.65*Vcc	Vcc+0.3V	0.1*Vcc	0.9*Vcc
IDE <UDMA4				0.8 V	2.0 V	5.5 V	0.5 V	2.4 V
IDE UDMA4+	3.135 V	3.465 V		0.8 V	2.0 V	5.5 V	0.51 V	Vcc-0.51V
RGMII				0.7 V	1.7 V		0.4 V	2.0 V
SMBus	2.7 V	3.465 V		0.8 V	2.1 V	Vcc	0.4 V	
USB 1.0				0.8 V	2.0 V	3.6 V	0.3 V	2.8 V

Notes:

1. Vcc values are from the corresponding specification and are used for defining signal levels only in this context.
2. USB 2.0, integrated SATA 2, Athlon64/Athlon64 FX CPU clock, and HyperTransport inputs and outputs are differential and not defined in this format. Please refer to the specification.

Other Signal DC Characteristics

Table 44 provides the DC input characteristics for the inputs and outputs not covered by industry standards.

Table 44. DC Characteristics

Signals	Vil		Vih		Vol	Voh
	Min	Max	Min	Max	Max	Min
INTRUDER#	-0.5 V	0.5 V	2.0 V	3.6 V		
A20GATE, EXT_SMI#, KBRDRSTIN#, SIO_PME#, PWRBTN#, PWRGD, PWRGD_SB, RI#, THERM#, TEST, PCI_CLKFB, FANRPM	-0.5 V	0.8 V	2.0 V	3.6 V		
RSTBTN#	-0.5 V	0.8 V	2.0 V	3.6 V		
USB_OC[4:0]#	-0.5 V	0.8 V	2.0 V	3.6 V	0.4 V	2.4 V
GPIO_[5:1]	-0.5 V	0.8 V	2.0 V	3.6 V	0.4 V	2.4 V
HT_STOP#					0.4 V	
PCI_RESET[4:0]#, BUF_SIO_CLK, BUF_25MHZ, SUSCLK, SPKR, SPDIF0, FANCTL[1:0]					0.4 V	2.4 V

AC Characteristics

This section contains the following AC specifications:

- Input clock characteristics
- Output clock characteristics
- Interface characteristics
  - HyperTransport Bus
  - PCI Express Bus
  - PCI Bus
  - SMBus Interface
  - AC '97 Interface
  - Integrated SATA 2 PHY Interface
  - USB Interface
  - IDE Interface
  - RGMII Interface
  - LPC Interface

Input Clock Characteristics

Table 45 provides the input clock characteristics.

Table 45. AC Input Clock Characteristics

Clock	Characteristic	Min	Typical	Max	Comments
32kHz Crystal	XTALIN_RTC frequency		32.00 kHz		
	XTALIN_RTC period		31.25 µs		
	XTALIN_RTC high time	14.06 µs		17.19 µs	55/45 duty cycle
	XTALIN_RTC low time	14.06 µs		17.19 µs	55/45 duty cycle
	XTALIN_RTC rise time	1 ns		20 ns	
	XTALIN_RTC fall time	1 ns		20 ns	
25MHz Crystal	XTAL_IN frequency		25 MHz		
	XTAL_IN period		40 ns		
	XTAL_IN high time	18 ns		22 ns	55/45 duty cycle
	XTAL_IN low time	18 ns		22 ns	55/45 duty cycle
	XTAL_IN rise time	1 ns		4 ns	
	XTAL_IN fall time	1 ns		4 ns	
AC'97 Clock	AC_BITCLK frequency		12.288 MHz		
	AC_BITCLK period		81.38 ns		
	AC_BITCLK high time	36.0 ns	40.7 ns	45.0 ns	55/45 duty cycle
	AC_BITCLK low time	36.0 ns	40.7 ns	45.0 ns	55/45 duty cycle

Clock	Characteristic	Min	Typical	Max	Comments
	AC_BITCLK rise time	2 ns		6 ns	
	AC_BITCLK fall time	2 ns		6 ns	
MII Transmit Clock	RGMII_TXCLK frequency		2.5/25 MHz		
	RGMII_TXCLK period		400/40 ns		
	RGMII_TXCLK high time	160/16 ns		240/24 ns	60/40 duty cycle
	RGMII_TXCLK low time	160/16 ns		240/24 ns	60/40 duty cycle
	RGMII_TXCLK rise time			0.75 ns	
	RGMII_TXCLK fall time			0.75 ns	
MII Receive Clock	RGMII_RXCLK frequency		2.5/25 MHz		
	RGMII_RXCLK period		400/40 ns		
	RGMII_RXCLK high time	160/16 ns		240/24 ns	60/40 duty cycle
	RGMII_RXCLK low time	160/16 ns		240/24 ns	60/40 duty cycle
	RGMII_RXCLK rise time			0.75 ns	
	RGMII_RXCLK fall time			0.75 ns	
RGMII Transmit Clock	RGMII_TXCLK frequency		125.0 MHz		
	RGMII_TXCLK period		8.0 ns		
	RGMII_TXCLK high time	3.6 ns		4.4 ns	55/45 duty cycle
	RGMII_TXCLK low time	3.6 ns		4.4 ns	55/45 duty cycle
	RGMII_TXCLK rise time			0.75 ns	
	RGMII_TXCLK fall time			0.75 ns	
RGMII Receive Clock	RGMII_RXCLK frequency		125.0 MHz		
	RGMII_RXCLK period		8.0 ns		
	RGMII_RXCLK high time	3.6 ns		4.4 ns	55/45 duty cycle
	RGMII_RXCLK low time	3.6 ns		4.4 ns	55/45 duty cycle
	RGMII_RXCLK rise time			0.75 ns	
	RGMII_RXCLK fall time			0.75 ns	
RGMII MDC Clock	RGMII_MDC frequency	0 Hz	2.39 MHz	2.5 MHz	14.318 MHz/6
	RGMII_MDC period	400 ns			
	RGMII_MDC high time	160 ns			
	RGMII_MDC low time	160 ns			
	RGMII_MDC rise time	1 ns		4 ns	
	RGMII_MDC fall time	1 ns		4 ns	
SMBus Clock	SMB_CLK frequency	0 Hz		100 kHz	See SMBus Spec.
	SMB_CLK period	10 µs			See SMBus Spec.
	SMB_CLK high time	4.0 µs		50 µs	See SMBus Spec.
	SMB_CLK low time	4.7 µs		25 ms	See SMBus Spec.
	SMB_CLK rise time	1 ns		1000 ns	See SMBus Spec.
	SMB_CLK fall time	1 ns		300 ns	See SMBus Spec.

Output Clock Characteristics

Table 46 lists the AC output clock characteristics and Figure 6 shows clock timing.

Table 46. AC Output Clock Characteristics

Clock	Characteristic	Min	Typical	Max	Comments
BUF_SIO_CLK 24.0MHz mode	BUF_SIO_CLK frequency		24.0 MHz		Driven to SuperI/O
	BUF_SIO_CLK period		41.67 ns		
	BUF_SIO_CLK high time	18.75 ns		22.92 ns	55/45 duty cycle
	BUF_SIO_CLK low time	18.75 ns		22.92 ns	55/45 duty cycle
	BUF_SIO_CLK rise time	1 ns		4 ns	
	BUF_SIO_CLK fall time	1 ns		4 ns	
BUF_SIO_CLK 14.318MHz mode	BUF_SIO_CLK frequency		14.318 MHz		
	BUF_SIO_CLK period		69.84 ns		
	BUF_SIO_CLK high time	31.43 ns		38.41 ns	55/45 duty cycle
	BUF_SIO_CLK low time	31.43 ns		38.41 ns	55/45 duty cycle
	BUF_SIO_CLK rise time	1 ns		4 ns	
	BUF_SIO_CLK fall time	1 ns		4 ns	
BUF_25MHZ	BUF_25MHZ frequency		25 MHz		
	BUF_25MHZ period		40 ns		
	BUF_25MHZ high time	16 ns		24 ns	60/40 duty cycle
	BUF_25MHZ low time	16 ns		24 ns	60/40 duty cycle
	BUF_25MHZ rise time			0.75 ns	
	BUF_25MHZ fall time			0.75 ns	
AC97_CLK	AC97_CLK frequency		24.576 MHz		
	AC97_CLK period		40.69 ns		
	AC97_CLK high time	18.31 ns		22.38 ns	55/45 duty cycle
	AC97_CLK low time	18.31 ns		22.38 ns	55/45 duty cycle
	AC97_CLK rise time	1 ns		4 ns	
	AC97_CLK fall time	1 ns		4 ns	
33.33MHz PCI / LPC Clocks	PCI_CLK frequency		33.33 MHz		Driven to PCI/LPC
	PCI_CLK period		30 ns		
	PCI_CLK high time	13.50 ns		16.50 ns	55/45 duty cycle
	PCI_CLK low time	13.50 ns		16.50 ns	55/45 duty cycle
	PCI_CLK rise time	1 ns		4 ns	
	PCI_CLK fall time	1 ns		4 ns	

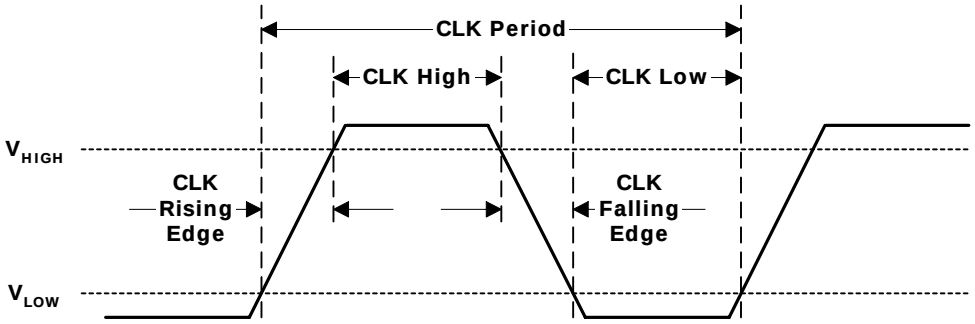

Figure 6. Clock Timing Diagram

Interface Characteristics

The AC interface characteristics are explained in the following tables and diagrams.

HyperTransport Interface

The HyperTransport interface is compliant with the *HyperTransport I/O Link Specification* published by the HyperTransport Technology Consortium. Refer to that document for full details of the interface timing.

NVIDIA nForce4 Ultra meets the timing requirements for transmit and receive up to a link speed of 4000 MT/s.

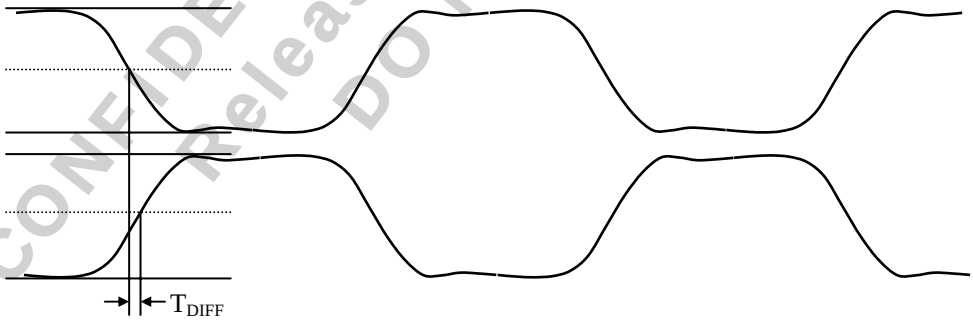

Figure 7. HyperTransport Bus T_{DIFF}

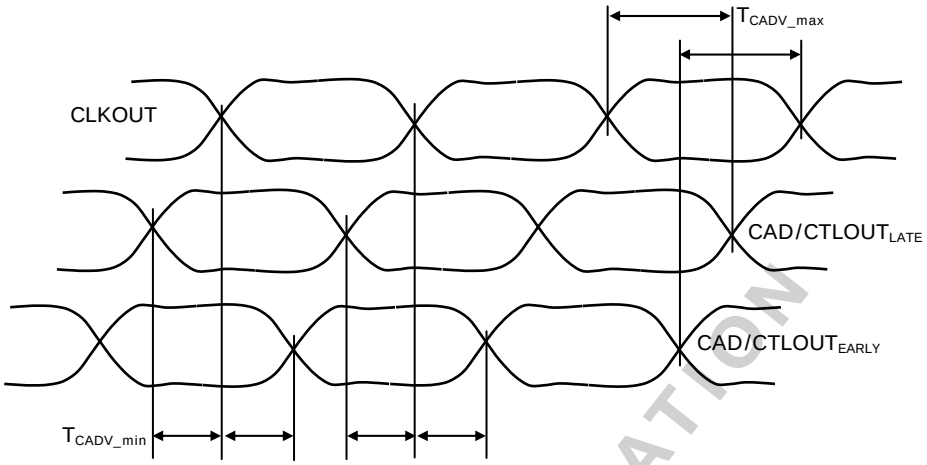

Figure 8. HyperTransport Bus T_{CAD}

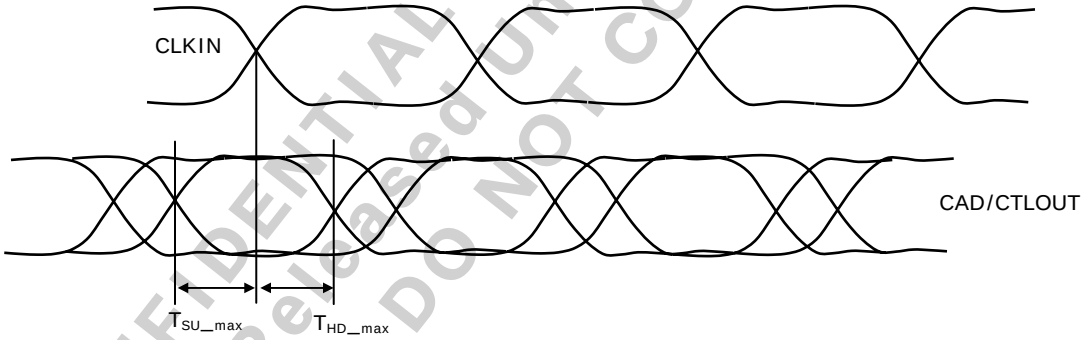

Figure 9. HyperTransport Bus T_{SU} and T_{HD}

Table 47. HyperTransport Bus

Symbol	Characteristic	Link Speed	Min	Max	Comments
T_{ODIFF}	Output differential skew	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s		70 ps 70 ps 70 ps 60 ps 60 ps 60 ps	
T_{IDIFF}	Input differential skew	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s		90 ps 90 ps 90 ps 65 ps 65 ps 65 ps	
T_{CADV}	Transmitter output CAD/CTLOUT valid relative to CLKOUT	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s 4000 MT/s	695 ps 467 ps 345 ps 280 ps 213 ps 166 ps 140 ps	1805 ps 1200 ps 905 ps 720 ps 620 ps 459 ps	
T_{CADVRS}	Receiver input CADIN valid time to CLKIN	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s	460 ps 312 ps 225 ps 194 ps 166 ps 116 ps		
T_{CADVRH}	Receiver input CADIN valid time from CLKIN	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s	460 ps 312 ps 225 ps 194 ps 166 ps 116 ps		
T_{SU}	Receiver input setup time	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s 4000 MT/s		250 ps 215 ps 175 ps 153 ps 138 ps 110 ps 70 ps	
T_{HD}	Receiver input hold time	800 MT/s 1200 MT/s 1600 MT/s 2000 MT/s 2400 MT/s 3200 MT/s 4000 MT/s		250 ps 215 ps 175 ps 153 ps 138 ps 110 ps 70 ps	

PCI Express Interface

The PCI Express interface is compliant with the *PCI Express Base Specification* published by the PCI SIG. Refer to that document for full details of the interface timing.

The NVIDIA nForce4 Ultra meets the timing requirements for transmit and receive at a link speed of 2.5 Gb/s.

Table 48. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400ps +/-300ppm. UI does not account for SSC (spread spectrum clock) dictated variations. See Note 1.
$V_{TX\text{-}DIFFp\text{-}p}$	Differential peak-to-peak output voltage	0.800		1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\|V_{TX\text{-}D+} - V_{TX\text{-}D-}\|$. See Note 2.
$V_{TX\text{-}DE\text{-}RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	This is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 2.
$V_{TX\text{-}EYE}$	Minimum TX eye width	0.70			UI	The maximum transmitter jitter can be derived as $T_{TX\text{-}MAX\ JITTER} = 1 - T_{TX\text{-}EYE} = 0.3$ UI. See Notes 2 and 3.
$V_{TX\text{-}EYE\text{-}MEDIAN\text{-}TO\text{-}MAX\text{-}JITTER}$	Maximum time between jitter median and maximum deviation from the median			0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p} = 0$ V) in relation to an appropriate average TX UI. See Notes 2 and 3.
$V_{TX\text{-}RISE}$, $V_{TX\text{-}FALL}$	D+/D- TX output rise/fall time	0.125			UI	See Notes 2 and 5.
$V_{TX\text{-}CM\text{-}ACp}$	AC peak common mode output voltage			20	mV	$V_{TX\text{-}CM\text{-}ACp} = \|V_{TX\text{-}D+} + V_{TX\text{-}D-}\|/2 - V_{TX\text{-}CM\text{-}DC}$ $V_{TX\text{-}CM\text{-}DC}$ = DC(avg) of $\|V_{TX\text{-}D+} + V_{TX\text{-}D-}\|/2$ during L0. See Note 2.
$V_{TX\text{-}CM\text{-}DC\text{-}ACIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0		100	mV	$\|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}IDLE\text{-}DC[during\ Electrical\ Idle]}\| <= 100$ mV $V_{TX\text{-}CM\text{-}DC}$ = DC(avg) of $\|V_{TX\text{-}D+} + V_{TX\text{-}D-}\|/2$ [L0] $V_{TX\text{-}CM\text{-}IDLE\text{-}DC}$ = DC(avg) of $\|V_{TX\text{-}D+} + V_{TX\text{-}D-}\|/2$ [Electrical Idle]. See Note 2.
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common mode voltage between D+ and D-	0		25	mV	$\|V_{TX\text{-}CM\text{-}DC\text{-}D+\ [during\ L0]} - V_{TX\text{-}CM\text{-}IDLE\text{-}DC\text{-}D\text{-}[during\ L0]}\| <= 25$ mV $V_{TX\text{-}CM\text{-}DC\text{-}D+}$ = DC(avg) of $\|V_{TX\text{-}D+}\|$ [during L0] $V_{TX\text{-}CM\text{-}DC\text{-}D-}$ = DC(avg) of $\|V_{TX\text{-}D-}\|$ [during L0]. See Note 2.
$V_{TX\text{-}IDLE\text{-}DIFFp}$	Electrical idle differential peak output voltage	0		20	mV	$V_{TX\text{-}IDLE\text{-}DIFFp} = \|V_{TX\text{-}IDLE\text{-}D+} - V_{TX\text{-}IDLE\text{-}D-}\| <= 20$ mV See Note 2.

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Figure 8.
$V_{TX-IDLE-MIN}$	Minimum time spec in electrical idle	50			UI	Minimum time a transmitter must be electrical idle.
$V_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			20	UI	After sending an electrical idle ordered-set, the transmitter must meet all electrical idle specifications within this time.
$V_{TX-IDLE-RCVDETECT-MAX}$	Maximum time spent in electrical idle before initiating a receiver detect sequence			100	ms	Maximum time spent in electrical idle before initiating a receiver detect sequence. See Figure 8.
$RL_{TX-DIFF}$	Differential return loss	12			dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
RL_{TX-CM}	Common mode return loss	6			dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$Z_{TX-DIFF-DC}$	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance.
$Z_{TX-COM-High-IMP-DC}$	Transmitter common mode high impedance state (DC)	5		20	KΩ	TX DC high impedance.
$L_{TX-SKEW}$	Lane-to-lane skew			500	ps	Between any two lanes within a single transmitter.
C_{TX}	AC coupling capacitor	75		200	pF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-31 of the PCI Express Base Specification Revision 1.0 and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter Compliance Eye Diagram shown in Figure 4-30 of the PCI Express Base Specification Revision 1.0.)
3. A TTX-EYE = 0.70 UI provides for a total sum of deterministic and random jitter budget of TTX-JITTER-MAX =0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The TTX-EYE-MEDIAN-TO-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the average time value.
4. The transmitter output impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 ohms to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50 ohm probes – see Figure 4-31 of the PCI Express Base Specification Revision 1.0). Note that the series capacitor CTX is optional for the return loss measurement.
5. Measured between 20%-80% at transmitter package pins into a test load as shown in Figure 4-31 for both VTX-D+ and VTX-D-.

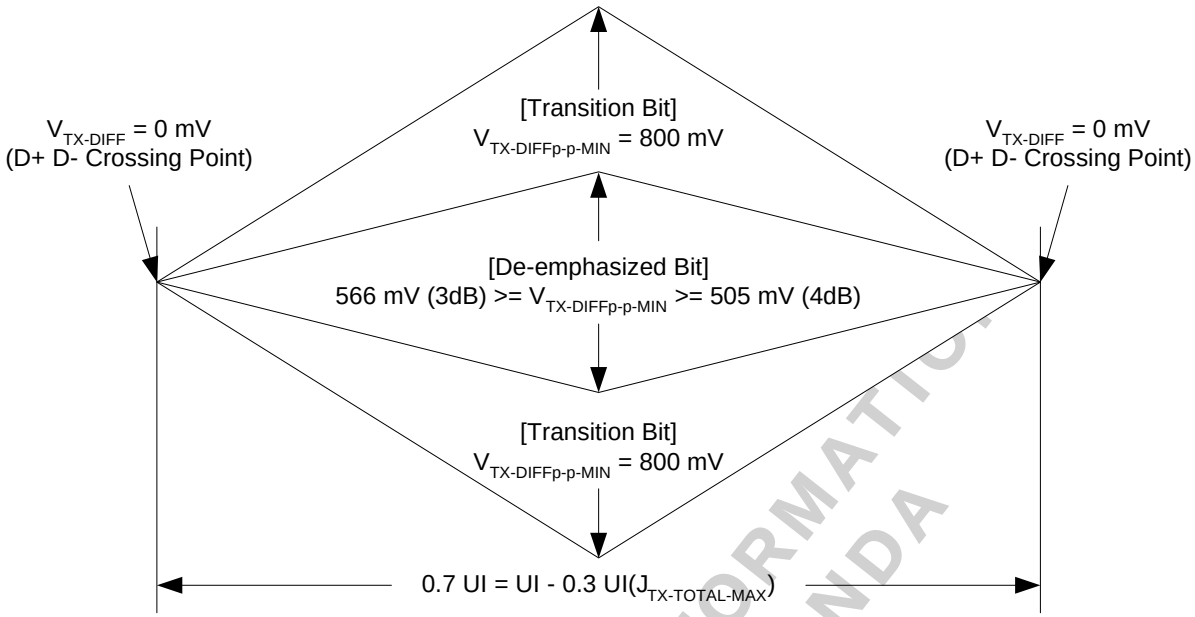

Figure 10. Minimum TX Eye Timing and Voltage Compliance

Table 49. Differential Receiver (RX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400ps +/-300 ppm. UI does not account for SSC dictated variations. See Note 6.
$V_{RX-DIFFp-p}$	Differential input peak-to-peak voltage	0.175		1.2	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$. See Note 7.
V_{RX-EYE}	Minimum RX eye width	0.40			UI	The maximum interconnect media and transmitter jitter can be tolerated by the receiver can be derived as $T_{RX-MAX\ JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 7 and 8.
$V_{TX-EYE-MEDIAN-TO-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to an appropriate average TX UI. See Notes 7 and 8.
$V_{RX-CM-ACp}$	AC peak common mode input voltage			150	mV	$V_{RX-CM-ACp} = \|V_{RX-D+} + V_{RX-D-}\|/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC}$ = DC(avg) of $\|V_{RX-D+} + V_{RX-D-}\|/2$ during L0. See Note 7.
$RL_{RX-DIFF}$	Differential return loss	15			dB	Measured over 50 MHz to 1.25 GHz. See Note 9.
R_{RX-CM}	Common mode return loss	6			dB	Measured over 50 MHz to 1.25 GHz. See Note 9.
$Z_{RX-DIFF-DC}$	DC differential RX impedance	80	100	120	Ω	RX DC differential mode low impedance. See Note 10.
$Z_{RX-COM-DC}$	DC input common mode input impedance	40	50	60	Ω	RX DC common mode impedance 50 ohms +/-20% tolerance. See Note 7 and 10.
$Z_{RX-COM-INITIAL-DC}$	Initial DC input common mode input impedance	5	50	60	Ω	RX DC common mode impedance allowed when the receiver terminations are first powered on. See Note 11
$Z_{RX-COM-HIGH-IMP-DC}$	Powered down DC input common mode input impedance	200			KΩ	RX DC common mode impedance when the receiver terminations are not powered (i.e., no power). See Note 12
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the receiver.
$T_{RX-IDLE-DET-OFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time			10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $V_{RX-IDLE-DET-OFF-ENTERTIME}$ to signal an unexpected idle condition.

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Lane-to-lane skew			20	ns	Across all lanes on a port. This includes variation in the length of a skip ordered-set (e.g., COM and 1 to 5 SKP symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

6. No test load is necessarily associated with this value.
7. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-31 of the PCI Express Base Specification Revision 1.0 should be used as the RX device when taking measurements (Also refer to the Receiver Compliance Eye Diagram shown in Figure 4-32 of the PCI Express Base Specification Revision 1.0). If the clocks to the RX and TX are not derived from the same clock chip the TX UI must be used as a reference for the eye diagram.
8. A TRX-EYE = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget of the TX and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-TO-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.60 UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the average time value. If the clocks to the RX and TX are not derived from the same clock chip, the appropriate average TX UI must be used as the reference for the eye diagram.
9. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 ohms to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50 ohm probes – see Figure 4-31 of the PCI Express Base Specification Revision 1.0). Note that the series capacitor CTX is optional for the return loss measurement.
10. Impedance during all operating conditions.
11. The RX DC common mode impedance that must be present when the receiver terminations are first enabled to ensure that the receiver-detect occurs properly. Compensation of this impedance can start immediately and the (ZRX-COM-DC) RX DC common mode impedance must be within the specified range by the time Detect is entered.
12. The RX DC common mode impedance that exists when the receiver terminations are disabled or when no power is present. This helps ensure that the receiver-detect circuit will not falsely assume a receiver is powered on when it is not.

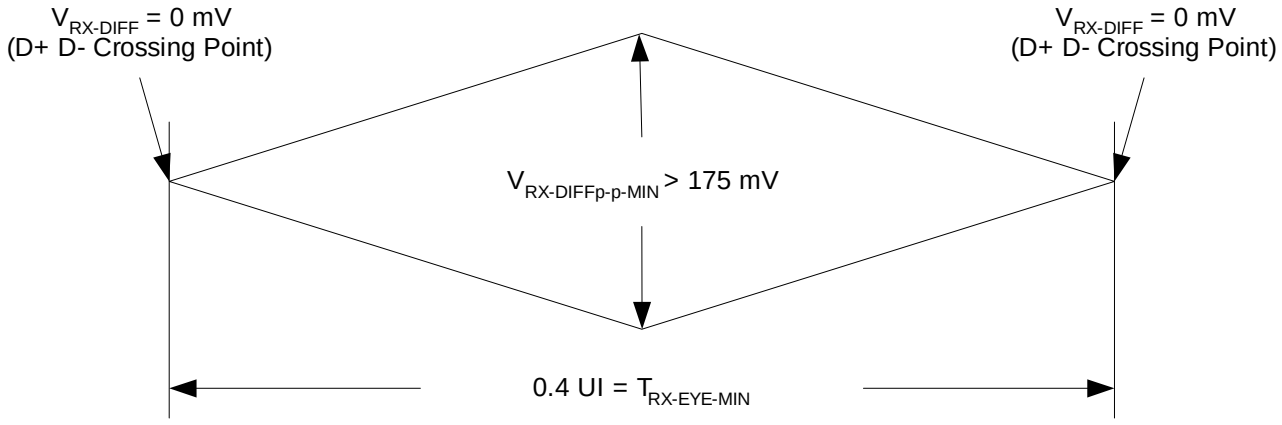

Figure 11. Minimum RX Eye Timing and Voltage Compliance

PCI Bus

Table 50. PCI Bus

Symbol	Characteristics	Min	Max	Comments
$T_{valid:bus}$	Valid delay – bussed	2 ns	11 ns	
$T_{valid:ptp}$	Valid delay – point-to-point	2 ns	11 ns	
$T_{setup:bus}$	Setup delay – bussed	7 ns		
$T_{setup:ptp}$	Setup delay – point-to-point	7 ns		
$T_{hold:bus}$	Hold delay – bussed	0 ns		
$T_{hold:ptp}$	Hold delay – point-to-point	0 ns		
T_{active}	Active delay from float	2 ns		
T_{float}	Float delay from active		28 ns	

Bussed Signals:
PCI_AD[31:0], PCI_CBE[3:0]#, PCI_DEVSEL#, PCI_FRAME#, PCI_IRDY#, PCI_TRDY#, PCI_STOP#, PCI_PAR, PCI_PERR#, PCI_SERR#, LPC_AD[3:0], LPC_FRAME#, SERIRQ

Point-to-Point Signals (ptp):
PCI_REQ[4:0]#, PCI_GNT[4:0]#, LPC_DRQ[1:0]#

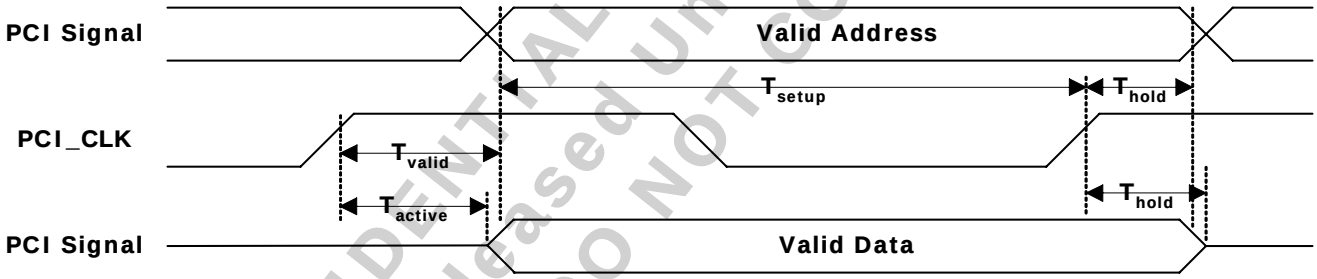

Figure 12. PCI Bus Timing Diagram

SMBus Interface

Table 51. SMBus Interface

Symbol	Characteristic	Min	Max	Comments
T_{lo}	Clock low period	4.7 µs		
T_{hi}	Clock high period	4.0 µs	50 µs	See Note 4
T_{buf}	Bus idle time between stop and start conditions	4.7 µs		
$T_{hd:sta}$	Hold time after (repeated) start condition. After this period, the first clock is generated	4.0 µs		
$T_{su:sta}$	Repeated start condition setup time	4.7 µs		
$T_{su:sto}$	Stop condition setup time	4.0 µs		
$T_{hd:dat}$	Data hold time	300 ns		
$T_{su:dat}$	Data setup time	250 ns		
$T_{timeout}$	Clock low time-out	25 ms	35 ms	Note 1
$T_{low:sext}$	Cumulative clock low extend time (slave device)		25 ms	Note 2
$T_{low:mext}$	Cumulative clock low extend time (master device)		10 ms	Note 3

Notes:

1. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of Ttimeout-Min. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than Ttimeout-Max. This parameter sets a common point at which a master or slave is allowed to conclude that a defective device is holding the clock low indefinitely.
2. Tlow:sext is the cumulative time a given slave device is allowed to extend the clock cycles in one message from the initial START to the STOP. It is possible that another slave device or the master will also extend the clock, causing the combined clock low extend time to be greater than Tlow:sext. Therefore, this parameter is measured with the slave device as the sole target of a full-speed master.
3. Tlow:mext is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message, as defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. It is possible that a slave device or another master will also extend the clock, causing the combined clock low time to be greater than Tlow:mext on a given byte. Therefore, this parameter is measured with a full speed slave
4. Thigh:max provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock has been high for greater than Thigh:max.

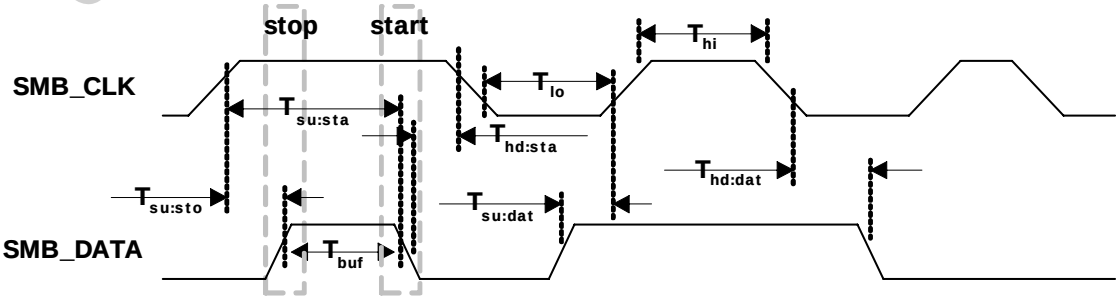

Figure 13. SMBus Timing Diagram

AC '97 Interface

Table 52. AC '97 Interface

Symbol	Characteristic	Min	Max	Comments
T_{vd}	Output valid delay from rising edge of AC_BITCLK		15 ns	
T_{su}	Input setup to falling edge of AC_BITCLK	10 ns		
T_{hd}	Input hold from falling edge of AC_BITCLK	10 ns		

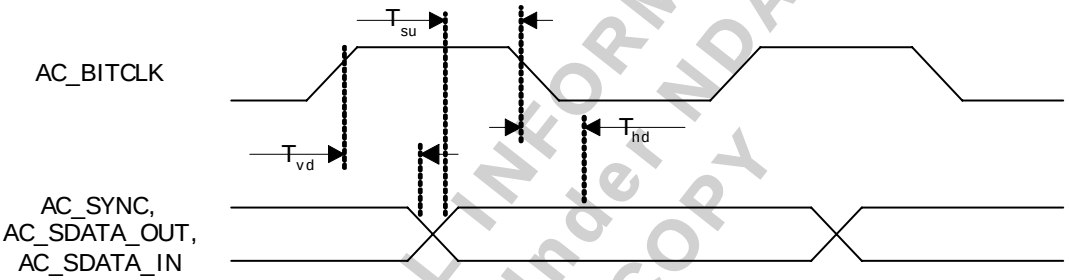

Figure 14. AC-Link Timing Diagram

Integrated SATA 2 Interface

Table 53. Integrated SATA 2 Input Timing/Electrical Characteristics (Gen 1i, 1.5 Gb mode)

Parameter	Symbol	Min	Max	Units	Comments
Rise time	T_{rise}	67	271	ps	20% to 80%
Fall time	T_{fall}	67	271	ps	80% to 20%
Squelch detection level (differential signal amplitude)		50	200	mV p-p	Minimum differential signal amplitude
Output differential amplitude	V_{diff}, Tx	400	600	mV p-p	Measured at SATA 2 connector on Tx side
Input differential amplitude	V_{diff}, Rx	325	600	mV p-p	Measured at SATA 2 connector on Rx side

Table 54. Integrated SATA 2 Input Timing/Electrical Characteristics (Gen 2i, 3.0 Gb mode)

Parameter	Symbol	Min	Max	Units	Comments
Rise time	T_{rise}	67	136	ps	20% to 80%
Fall time	T_{fall}	67	136	ps	80% to 20%
Squelch detection level (differential signal amplitude)		50	200	mV p-p	Minimum differential signal amplitude
Output differential amplitude	V_{diff}, Tx	500	700	mV p-p	Measured at SATA 2 connector on Tx side
Input differential amplitude	V_{diff}, Rx	240	700	mV p-p	Measured at SATA 2 connector on Rx side

USB Interface

The following tables were taken from the *Universal Serial Bus Specification, Revision 2.0*. Refer to Chapter 7 for additional information. All references under the Condition column refer to tables and figures in the specification and sections within Chapter 7.

Table 55. USB Bus Timing/Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Units
Input Levels for Low/Full-Speed (USB1)					
High (driven)	V_{1H}	Note 4, Section 7.1.4	2.0		V
High (floating)	V_{1HZ}		2.7	3.6	V
Low	V_{1L}			0.8	V
Differential input sensitivity	V_{D1}	|(D+)-(D-)|, Note 4	0.2		V
Differential common mode range	V_{CM}	Includes V_{D1} range, Note 4	0.8	2.5	V
Input Levels for High-Speed (USB2)					
High-speed squelch detection threshold (differential signal amplitude)	V_{HSSQ}	Specification refers to differential signal amplitude (Section 7.1.7.2)	100	150	mV
High-speed disconnect detection threshold (differential signal aptitude)	V_{HSDSC}		525	625	mV
High-speed differential input signaling levels		Specified by eye pattern templates			
High-speed data signaling common mode voltage range (guidelines for receiver)	V_{HSCM}	Section 7.1.4.2	-50	500	mV
Output Levels for Low/Full-Speed (USB1)					
Low	V_{OL}	Note 4, 5 (Sec 7.1.1)	0.0	0.3	V
High (driven)	V_{OH}	Note 4, 6 (Sec 7.1.1)	2.8	3.6	V
SE1	V_{OSE1}	(Sec 7.1.1)	0.8		V
Output signal crossover voltage	V_{CRS}	Measured as in Fig 7-8, Note 10	1.3	2.0	V

Parameter	Symbol	Condition	Min	Max	Units
Output Levels for High-Speed (USB2)					
High-speed idle level	V_{HSOI}	Section 7.1.7.2	-10.0	10.0	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		-10.0	10.0	mV
Chirp J level (differential voltage)	V_{CHIRPJ}		700	1100	mV
Chirp K level (differential voltage)	V_{CHIRPK}		-900	-500	mV
Decoupling Capacitance					
Downstream facing port bypass capacitance (per hub)	C_{HPB}	VBUS to GND, Section 7.2.4.1	120		µF
Input Capacitance for Low/Full-speed (USB1)					
Downstream facing port	C_{IND}	Note 2, Section 7.1.6.1		150	pF
Transceiver edge rate control capacitance	C_{EDGE}	Section 7.1.6.1		75	pF
Input Impedance for High-speed (USB2)					
TDR spec for high-speed termination		Section 7.1.6.2			
Terminations (USB1)					
Bus pull-up resistor on downstream facing port	R_{PD}	15 kΩ ±5% Section 7.1.5	14.25	15.75	kΩ
Input impedance exclusive of pull-up/pull-down (for low/full speed – USB1)	Z_{INP}	Section 7.1.6	300		kΩ

Notes:

2. Measured at A receptacle.
4. Measured at A or B connector.
5. Measured with RL of 1.425 kΩ to 3.6 V
6. Measured with RL of 14.25 kΩ to GND.
10. Excluding the first transition from the idle state.

Table 56. High-Speed Source Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Units
Driver Characteristics					
Rise time (10% - 90%)	T_{HSR}	Section 7.1.2	500		ps
Fall time (10% - 90%)	T_{HSF}	Section 7.1.2	500		ps
Driver waveform requirements		Specified by eye pattern templates, Section 7.1.2			
Driver output resistance (also serves as high-speed termination)	Z_{HSDRV}	Section 7.1.1.1	40.5	49.5	Ω

Table 57. Full-Speed Source Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Units
Driver Characteristics					
Rise time	T_{FR}	Figures 7-8, 7-9	4	20	ns
Fall time	T_{FF}		4	20	ns
Differential rise and fall time matching	T_{FRFM}	T_{FR} and T_{FF} (Note 10) Section 7.1.2	90	111.11	%
Driver output resistance for driver not high-speed capable	Z_{DRV}	Section 7.1.1.1	28	44	Ω

Note:
10. Excluding the first transition from the idle state.

Table 58. Low-Speed Source Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Units
Driver Characteristics					
Transition Time: Rise time Fall time	 T_{LR} T_{LF}	Measured as in Figure 7-8	 75 75	 300 300	ns
Rise and fall time matching	T_{LRFM}	T_{LR} and T_{LF} (Note 10)	80	125	%

Note:
10. Excluding the first transition from the idle state.

IDE Interface

Table 59. PIO

Symbol	Characteristic	(ns)	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
$T_{cyc:iox}$	Cycle time (IDE_IOx# to IDE_IOx#)	min	600	383	330	180	120
$T_{su:addr}$	IDE_ADDR setup to IDE_IOx#	min	70	50	30	30	25
$T_{hi:iox}$	IDE_IOx# recovery time	min				70	25
$T_{su:data}$	IDE_DATA write setup to IDE_IOW#	min	60	45	30	30	20
$T_{hd:data}$	IDE_DATA write hold from IDE_IOW#	min	30	20	15	10	10
$T_{su:data}$	IDE_DATA read setup to IDE_IOR#	min	50	35	20	20	20
$T_{hd:data}$	IDE_DATA read hold from IDE_IOR#	min	5	5	5	5	5
$T_{hd:addr}$	IDE_ADDR hold from IDE_IOx#	min	20	15	10	10	10
$T_{su:rdy}$	IDE_RDY setup to IDE_IOx#	min	35	35	35	35	35
$T_{lo:rdy}$	IDE_RDY pulse width	max	1250	1250	1250	1250	1250
$T_{rl:rdy}$	IDE_RDY assertion release	max	5	5	5	5	5
$T_{lo:iox}$	IDE_IOx# pulse width 8-bit (register)	min	290	290	290	80	70
$T_{lo:iox}$	IDE_IOx# pulse width 16-bit (data)	min	165	125	100	80	70

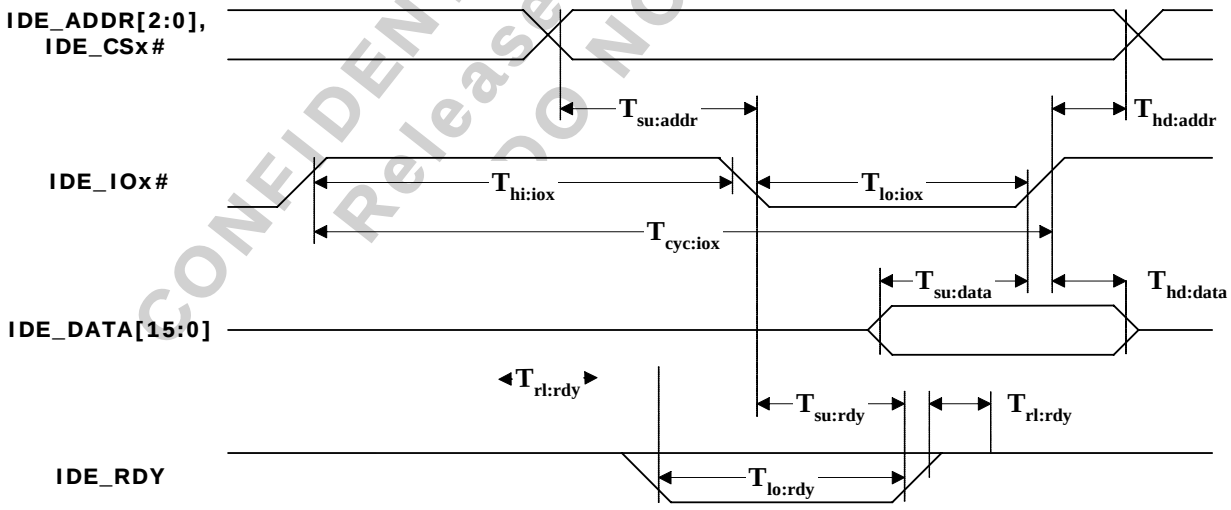

Figure 15. IDE PIO Timing Diagram

Table 60. Multiword DMA

Symbol	Characteristic	(ns)	Mode 0	Mode 1	Mode 2
$T_{cyc:iox}$	Cycle time (IDE_IOx# to IDE_IOx#)	min	480	250	120
$T_{lo:iox}$	IDE_IOx# pulse width	min	215	80	70
$T_{vd:data}$	IDE_IOR# data access	max	150	60	50
$T_{hd:data}$	IDE_IOR# data hold	min	5	5	5
$T_{su:data}$	IDE_IOx# data setup	min	100	30	20
$T_{hd:data}$	IDE_IOW# data hold	min	20	15	10
$T_{su:dack}$	IDE_DACK# to IDE_IOx# setup	min	0	0	0
$T_{hd:dack}$	IDE_IOx# to IDE_DACK# hold	min	20	5	5
$T_{lo:iox}$	IDE_IOR# negative pulse width	min	50	50	25
$T_{lo:iox}$	IDE_IOW# negative pulse width	min	215	50	25
$T_{dl:drq}$	IDE_IOR# to IDE_DRQ delay	max	120	40	35
$T_{dl:drq}$	IDE_IOW# to IDE_DRQ delay	max	40	40	35
$T_{su:cs}$	IDE_CSx# valid to IDE_IOx#	min	50	30	25
$T_{hd:cs}$	IDE_CSx# hold	min	15	10	10
$T_{rl:dack}$	IDE_DACK# to read data released	max	20	25	25
$T_{su:drq}$	IDE_DRQ setup		undefined		

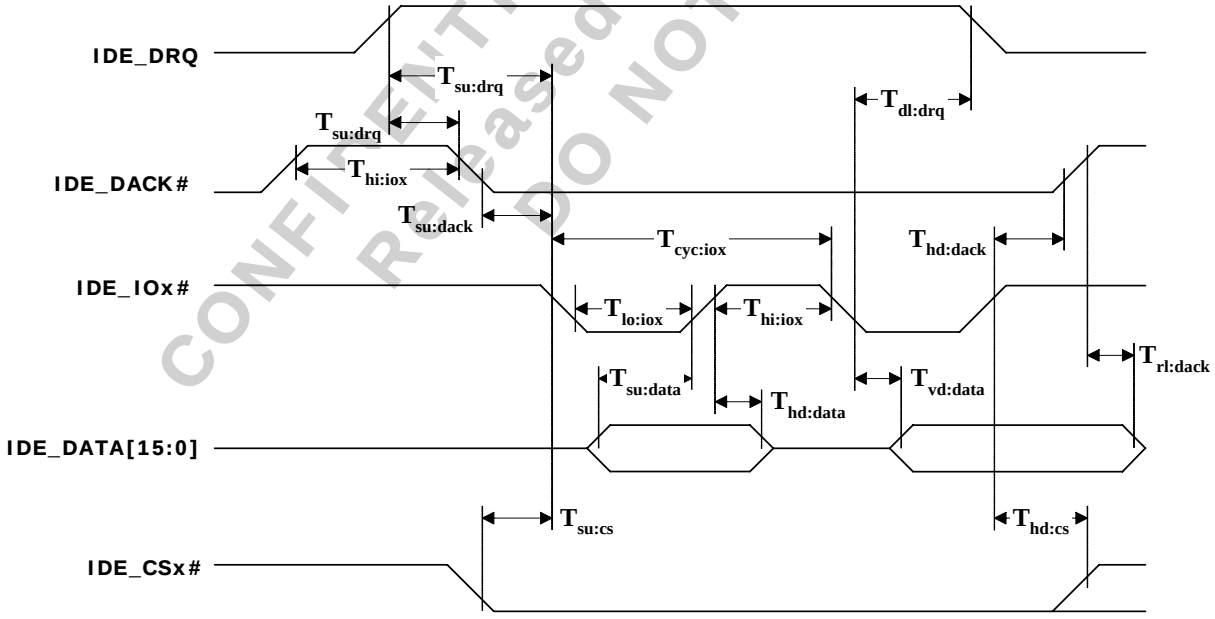

Figure 16. IDE Multiword DMA Timing Diagram

Table 61. UltraDMA

Characteristics	(ns)	Mode 0	1	2	3	4	5	6
Typical sustained average two-cycle time	min	240	160	120	90	60	40	30
Cycle time allowing for asymmetry and clock variations	min	112	73	54	39	25	16.8	13.0
Two cycle time allowing for clock variations	min	230	154	115	86	57	38	29.0
Data setup time at recipient	min	15	10	7	7	5	4	2.6
Data hold time at recipient	min	5	5	5	5	5	4.6	3.5
Data valid setup time at sender	min	70	48	30	20	6	3.3	4.0
Data valid hold time at sender	min	6	6	6	6	6	3.3	4.0
First STROBE time	min	0	0	0	0	0	0	25
First STROBE time	max	230	200	170	130	120	90	80
Limited interlock time	min	0	0	0	0	0	0	0
Limited interlock time	max	150	150	150	100	100	75	60
Interlock time with minimum	min	20	20	20	20	20	20	20
Unlimited interlock time	min	0	0	0	0	0	0	0
Maximum time allowed from output drivers to release	max	10	10	10	10	10	10	10
Minimum delay time required for output driver to assert or negate	min	20	20	20	20	20	20	20
Minimum delay time required for output driver to assert or negate	min	0	0	0	0	0	0	0
Envelope time	min	20	20	20	20	20	20	20
Envelope time	max	70	70	70	55	55	50	50
Ready to final Strobe time	max	75	70	60	60	60	50	50
Minimum time to assert STOP or negate **IDE_DACK#**	min	160	125	100	100	100	85	85
Maximum time before releasing **IDE_RDY#**	max	20	20	20	20	20	20	20
Maximum time before releasing STROBE	min	0	0	0	0	0	0	0
Setup and hold times for **IDE_DACK#**	min	20	20	20	20	20	20	20
Time from STROBE edge to negation of **IDE_REQ#** or assertion of STOP	min	50	50	50	50	50	50	50

Note:
Refer to the ATA 133 Specification for details.

RGMII Interface

The following information for the RGMII interface is from the *RGMII Version 1.3 Specification*. Refer to this and *EIA/JEDEC EIA/JESD8-5* for more detailed information.

Electrical Characteristics

The electrical characteristics for all RGMII signals (including MDIO/MDC) are based on *EIA/JEDEC EIA/JESD8-5*.

Table 62. DC Characteristics for RGMII Interface

Parameter	Min	Max
V_{DD} (supply voltage)	3.15 V	3.45 V
V_{OH}	2.0 V	VDD + 0.3 V
V_{OL}	GND – 0.3 V	0.40 V
V_{IH}	1.7 V	
V_{IL}		0.70 V
I_{IH}		15 uA
I_{IL}	-15 uA	

RGMII Timing

Since the clock and data are generated simultaneously by their source, the skew between these signals is critical for proper operation.

Table 63. Timing Specifics for RGMII Interface

Parameter	Description	Min	Typical	Max
T_{skewT}	Data to clock output skew (at transmitter)	-500 ps	0 ps	500 ps
T_{skewR}	Data to clock input skew (at receiver)[1]	1 ns		2.6 ns
T_{cyc}	Clock cycle duration[2]	7.2 ns	8 ns	8.8 ns
Duty_G	Duty cycle for gigabit[3]	45%	50%	55%
Duty_T	Duty cycle for 10/100T[3]	40%	50%	60%
T_r/T_f	Rise/fall time (20%-80%)			0.75 ns

Notes:

1. This implies that PC board designs will require clocks to be routed such that additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100 Mbps, the Max value is unspecified. (**Note**: The NVIDIA nForce4 Ultra internally skews the receive clock with respect to the received data lines so that there is no need to skew these signals on the PCB.)
2. 10 Mbps = 400 ns ± 40 ns and 100 Mbps = 40 ± 4 ns
3. During speed changes or transitioning to a received packets clock domain, the duty cycle may be stretched or shrunk as long as:
   a. The minimum duty cycle is not violated.
   b. Stretching does not occur for more than three Tcyc of the lowest speed transitioned between.

MDIO Timing Relationship to MDC

MDIO (Management Data Input/Output) is a bidirectional signal that can be sourced by the Station Management entity (STA) or the PHY. When the STA sources the MDIO signal, the STA will provide a minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in Figure 17, measured at the RGMII connector.

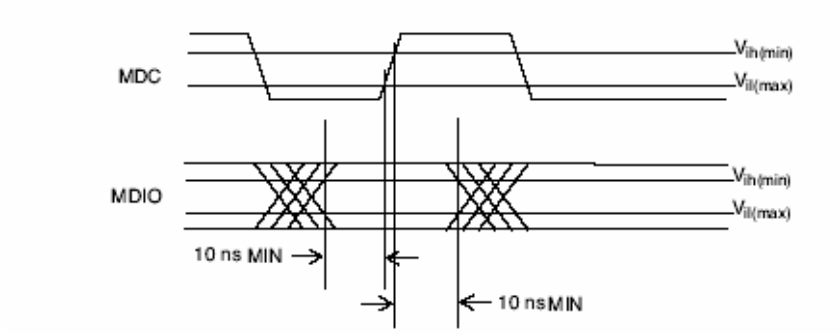

Figure 17. MDIO Sourced by the NVIDIA nForce4 Ultra

When the MDIO signal is sourced by the PHY, it is sampled by the NVIDIA nForce4 Ultra synchronously with respect to the rising edge of MDC. The clock to output delay from the PHY, as measured at the RGMII connector, must be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 22.

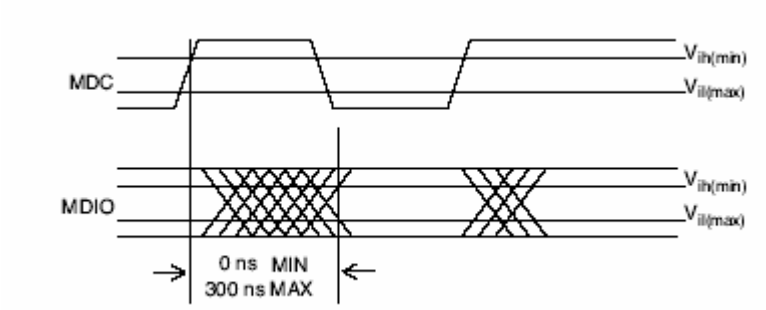

Figure 18. MDIO Sourced by PHY

MDC (Management Data Clock)

MDC is sourced by the Station Management entity to the PHY as the timing reference for transfer of information on the **MDIO** signal. **MDC** is an aperiodic signal that has no maximum high or low times. The minimum high and low times for MDC will be 160 ns each, and the minimum period for MDC will be 400 ns, regardless of the nominal period of **TX_CLK** and **RX_CLK**.

LPC Interface

The AC specification for these signals is the same as those in Section 4.2.2 of the *PCI Local Bus Specification, Revision 2.3*. That section contains the specifications for the 3.3V PCI signaling levels.

Industry Standards

The following industry standard documents are referenced in this document. You should reference these as well as this document.

- *HyperTransport I/O Link Specification*
  Revision 1.03, HyperTransport Technology Consortium
- *PCI Local Bus Specification*
  Revision 2.3, PCI Special Interest Group
- *Low Pin Count (LPC) Interface Specification*
  Revision 1.0, Intel Corporation
- *Audio Codec '97*
  Revision 2.3, Intel Corporation
- *AT Attachment with Packet Interface – 7 (ATA/ATAPI-7)*
  ANSI
- *IEEE Std 802.3*
  2002 Edition
- *System Management Bus (SMBus) Specification*
  Version 2.0, SBS Implementers Forum
- *Universal Serial Bus Specification*
  Revision 2.0, Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC, Philips
- *Reduced Gigabit Media Independent Interface (RGMII)*
  Version 1.3
- *EIA/JEDEC Standard EIA/JESD8-5*
  October 1995

Appendix A. Ball Listings

Table 64 provides the ball listing by package ball and Table 65 provides the ball listing by the signal name.

Table 64. Ball Listing by Package Ball

Ball	Signal Name
A2	GND
A3	PCI_AD25
A4	PCI_AD26
A5	PCI_AD30
A6	+5V
A9	PE0_TX12#
A10	PE0_TX11#
A13	PE0_TX6#
A14	PE0_TX6
A17	PE0_TX1
A18	PE0_TX0
A21	PE4_TX#
A22	PE4_TX
A25	PE_REFCLK_IN
A26	GND_PLL_PE
A27	+1.5V_PLL_PE_AVDD
A28	+1.5V_PLL_PE_DVDD
A29	+3.3V_PLL_DUAL
B1	GND
B2	PCI_AD20
B3	PCI_AD27
B4	PCI_AD24
B5	PCI_INTW#
B6	PE_AGND
B7	PE0_TX15#
B9	PE0_TX12

Ball	Signal Name
B10	PE0_TX11
B11	PE0_TX10
B13	PE0_TX7
B14	PE0_TX5#
B15	PE0_TX4#
B17	PE0_TX1#
B18	PE0_TX0#
B19	PE0_REFCLK
B21	PE2_TX
B22	PE3_TX#
B23	PE3_REFCLK#
B25	PE_REFCLK_IN#
B26	+3.3V_PLL_PE_CORE
B27	+1.5V_PE_A
B28	+1.5V_PLL_PE_CORE
B29	+1.5V_PE_A
B30	+1.5V
C1	PCI_AD17
C2	PCI_AD16
C3	PCI_AD19
C4	PCI_AD28
C5	PCI_AD29
C6	GND
C7	PE0_TX15
C8	PE0_TX14
C9	PE0_TX13

Ball	Signal Name
C10	PE0_TX10#
C11	PE0_TX9#
C12	PE0_TX8#
C13	PE0_TX7#
C14	PE0_TX5
C15	PE0_TX4
C16	PE0_TX3
C17	PE0_TX2
C18	PE0_REFCLK#
C19	PE1_TX#
C20	PE1_REFCLK#
C21	PE2_TX#
C22	PE3_TX
C23	PE3_REFCLK
C24	PE2_REFCLK
C25	PE_CLK_TEST
C26	+1.5V_PE_A
C27	+1.5V_PE_A
C28	+1.5V_PE_A
C29	+1.5V
C30	+1.5V_PE_D
D1	PCI_IRDY#
D2	PCI_AD18
D3	PCI_AD21
D4	PCI_CBE3#
D5	PCI_AD31

Ball	Signal Name
D6	PCI_INTZ#
D7	PE_AGND
D8	PE0_TX14#
D9	PE0_TX13#
D10	PE0_RX12
D11	PE0_TX9
D12	PE_AGND
D13	PE0_TX8
D14	PE0_RX5
D15	PE0_TX3#
D16	PE_AGND
D17	PE0_TX2#
D18	PE1_RX
D19	PE1_TX
D20	PE_AGND
D21	PE1_REFCLK
D22	PE0_PRSNT#
D23	PE2_REFCLK#
D24	PE_CLK_TEST#
D25	PE_AGND
D26	+1.5V_PE_A
D27	+1.5V
D28	+1.5V
D29	+1.5V_PE_D
D30	+1.5V_PE_D
E1	PCI_DEVSEL#
E2	PCI_TRDY#
E3	PCI_AD22
E4	PCI_AD23
E5	PCI_INTY#
E6	PCI_INTX#
E7	PE_AGND
E8	PE0_RX15
E9	PE0_RX14#
E10	PE0_RX12#
E11	PE_AGND
E12	PE0_RX10
E13	PE0_RX8
E14	PE0_RX5#
E15	PE_AGND
E16	PE0_RX4

Ball	Signal Name
E17	PE0_RX1#
E18	PE1_RX#
E19	PE_AGND
E20	PE2_RX#
E21	PE3_PRSNT#
E22	PE_RST#
E23	PE_WAKE#
E24	PECLK_COMP_GND
E25	+1.5V_PE_A
E26	+1.5V
E27	+1.5V_PE_D
E28	+1.5V_PE_D
E29	RGMII_VREF/ MII_VREF
E30	RGMII_RXD1/ MII_RXD1
F1	GND
F2	PCI_STOP#
F3	PCI_CBE2#
F4	PCI_FRAME#
F5	PCI_PERR#/ GPIO_38
F6	PCI_SERR#
F7	GND
F8	PE0_RX15#
F10	PE0_RX14
F12	PE0_RX10#
F14	PE0_RX8#
F16	PE0_RX4#
F18	PE0_RX1
F20	PE2_RX
F22	PE2_PRSNT#
F24	+1.5V_PE_A
F25	+1.5V
F26	+1.5V_PE_D
F27	+1.5V_PE_D
F28	RGMII_RXD3/ MII_RXD3
F29	RGMII_RXD2/ MII_RXD2
F30	GND
G2	PCI_CBE1#
G3	PCI_AD15

Ball	Signal Name
G4	PCI_PAR
G5	PCI_AD11
G6	PCI_AD12
G7	PCI_AD13
G8	PE_AGND
G9	PE_AGND
G10	PE0_RX13#
G11	PE_AGND
G12	PE0_RX9#
G13	PE_AGND
G14	PE0_RX7#
G15	PE_AGND
G16	PE0_RX3#
G17	PE_AGND
G18	PE0_RX0#
G19	PE_AGND
G20	PE3_RX#
G21	PE_AGND
G22	PE1_PRSNT#
G23	+1.5V_PE_A
G24	+1.5V
G25	+1.5V_PE_D
G26	+1.5V_PE_D
G27	GND
G28	RGMII_RXCTL/ MII_RXDV
G29	RGMII_RXD0/ MII_RXD0
H3	PCI_AD10
H4	PCI_AD14
H5	GND
H6	PCI_AD7
H7	PCI_AD0
H8	PCI_AD6
H10	PE0_RX13
H12	PE0_RX9
H14	PE0_RX7
H16	PE0_RX3
H18	PE0_RX0
H20	PE3_RX
H22	+1.5V_PE_A
H24	+1.5V_PE_D

Ball	Signal Name
H25	GND
H26	RGMII_TXCLK/ MII_TXCLK
H27	RGMII_RXCLK/ MII_RXCLK
H28	RGMII_TXD0/ MII_TXD0
J1	PCI_CBE0#
J2	PCI_AD2
J3	PCI_AD4
J4	PCI_AD9
J5	PCI_AD5
J7	GND
J9	+3.3V
J10	PE0_RX11#
J11	PE0_RX11
J12	PE_AGND
J13	PE_AGND
J14	PE_AGND
J15	PE0_RX6#
J16	PE0_RX6
J17	PE0_RX2#
J18	PE0_RX2
J19	PE4_RX#
J20	PE_AGND
J21	+1.5V
J22	+1.5V_PE_D
J24	+1.5V_PE_D
J26	RGMII_TXCTL/ MII_TXEN
J27	RGMII_TXD1/ MII_TXD1
J28	RGMII_TXD2/ MII_TXD2
J29	RGMII_TXD3/ MII_TXD3
J30	RGMII_MDIO/ MII_MDIO
K1	GND
K2	PCI_CLK2
K3	PCI_CLK0
K4	PCI_GNT3#/ GPIO_17
K5	PCI_CLK3

Ball	Signal Name
K6	GND
K7	PCI_AD1
K8	PCI_AD8
K9	GND
K10	PE_DGND
K11	PE_DGND
K12	PE_DGND
K13	PE_DGND
K14	PE_DGND
K15	PE_DGND
K16	PE_DGND
K17	PE_DGND
K18	PE_DGND
K19	PE4_RX
K20	+1.5V
K21	+1.5V_PE_D
K22	+1.5V_PE_D
K23	+1.5V_PE_D
K24	RGMII_MDC/ MII_MDC
K25	RGMII_PWRDWN/ MII_PWRDWN/ GPIO_20
K26	MII_COL
K27	MII_CRS
K28	RGMII_INTR/ MII_INTR/ GPIO_11
K29	MII_RXER/ GPIO_21
K30	GND
L2	PCI_CLK1
L3	PCI_CLK4
L4	PCI_CLK5
L5	GND
L7	GND
L9	PCI_AD3
L10	+3.3V
L21	+1.5V_PE_D
L22	+1.5V_PE_D
L24	GND
L26	GND
L27	CPU_CLK_66

Ball	Signal Name
L28	CPU_CLK
L29	CPU_CLK#
M3	PCI_CLKFB
M4	GND
M5	PCI_GNT2#/ GPIO_8
M6	PCI_GNT1#
M7	PCI_GNT0#
M8	PCI_REQ3#/ GPIO_16
M9	PCI_REQ2#/ GPIO_6
M10	GND
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M17	GND
M18	GND
M19	GND
M21	+3.3V_DUAL
M22	HT_REQ#/GPIO_10
M23	GND
M24	BUF_25MHZ
M25	CPU_COMP
M26	CPU_PWROK
M27	GND
M28	CPU_RST#
N1	PCI_RESET1#
N2	PCI_RESET0#
N3	PCI_RESET2#
N4	PCI_CLKRUN#/ GPIO_9
N5	PCI_REQ0#
N7	GND
N9	PCI_REQ1#
N10	GND
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND

Ball	Signal Name
N17	GND
N18	GND
N19	GND
N21	+1.2V_HT
N22	HT_STOP#
N24	GND
N26	HT_TXD9#
N27	HT_TXD0
N28	HT_TXD0#
N29	HT_TXD1
N30	HT_TXD1#
P1	GND
P2	USB_0
P3	USB_0#
P4	+3.3V_DUAL
P5	PCI_REQ4# / GPIO_45
P6	PCI_PME# / GPIO_37
P7	PCI_GNT4# / GPIO_46
P8	USB_1
P9	USB_1#
P10	GND
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P21	+1.2V_HT
P22	HT_TXD10
P23	HT_TXD10#
P24	HT_TXD8#
P25	HT_TXD8
P26	HT_TXD9
P27	GND
P28	HT_TXD3
P29	HT_TXD2
P30	HT_TXD2#

Ball	Signal Name
R2	USB_2
R3	USB_2#
R4	USB_3#
R5	GND
R7	GND
R9	GND
R10	+3.3V
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R21	GND
R22	GND
R24	GND
R26	GND
R27	HT_TXCLK0#
R28	HT_TXCLK0
R29	HT_TXD3#
T3	USB_3
T4	GND
T5	USB_6
T6	USB_6#
T7	USB_7
T8	USB_7#
T9	+3.3V_USB_DUAL
T10	GND
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	GND
T18	GND
T19	GND
T21	+1.2V_HT
T22	HT_TXD12#
T23	HT_TXCLK1

Ball	Signal Name
T24	HT_TXCLK1#
T25	HT_TXD11
T26	HT_TXD11#
T27	GND
T28	HT_TXD4
U1	USB_5
U2	USB_5#
U3	USB_4
U4	USB_4#
U5	USB_8
U7	GND
U9	GND
U10	+3.3V
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U21	GND
U22	HT_TXD12
U24	GND
U26	HT_TXD13#
U27	HT_TXD4#
U28	HT_TXD5
U29	HT_TXD5#
U30	HT_TXD6
V1	GND
V2	USB_OC3# / GPIO_24
V3	USB_OC2# / GPIO_23
V4	USB_OC0#
V5	USB_OC1# / GPIO_22
V6	USB_8#
V7	USB_9
V8	USB_9#
V9	USB_RBIAS
V10	GND

Ball	Signal Name
V12	GND
V13	GND
V14	GND
V15	GND
V16	GND
V17	GND
V18	GND
V19	GND
V21	+1.2V_HT
V22	HT_TXD15
V23	HT_TXD15#
V24	HT_TXD14
V25	HT_TXD14#
V26	HT_TXD13
V27	GND
V28	HT_TXD7#
V29	HT_TXD7
V30	HT_TXD6#
W2	SMB_CLK1/ GPIO_43
W3	SMB_DATA1/ GPIO_44
W4	SMB_DATA0/ GPIO_42
W5	GND
W7	GND
W9	GND
W10	+3.3V
W12	GND
W13	GND
W14	GND
W15	GND
W16	GND
W17	GND
W18	GND
W19	GND
W21	+1.2V_HT
W22	GND
W24	GND
W26	GND
W27	HT_RXCTL#
W28	HT_TXCTL#

Ball	Signal Name
W29	HT_TXCTL
Y3	SMB_CLK0/ GPIO_41
Y4	GND
Y5	AC_RESET#
Y6	AC97_CLK
Y7	AC_SDATA_IN0/ GPIO_14
Y8	AC_SDATA_OUT/ GPIO_13
Y9	+3.3V_DUAL
Y10	+3.3V
Y21	+1.5V_PLL_HT
Y22	HT_RXD13
Y23	HT_RXD14#
Y24	HT_RXD14
Y25	HT_RXD15#
Y26	HT_RXD15
Y27	GND
Y28	HT_RXCTL
AA1	GND
AA2	FANCTL0/ GPIO_35
AA3	FANRPM/ GPIO_34
AA4	USB_OC4#/ GPIO_25
AA5	AC_BITCLK
AA7	GND
AA9	AC_SYNC/ GPIO_12
AA10	GND
AA11	+3.3V
AA12	+1.5V_SP_D
AA13	SP_AGND
AA14	SP_LED#/ GPIO_19
AA15	+1.5V_SP_A
AA16	GND
AA17	IDE_DATA_P1
AA18	+3.3V
AA19	IDE_IOR_P#
AA20	+3.3V
AA21	GND

Ball	Signal Name
AA22	HT_RXD13#
AA24	GND
AA26	GND
AA27	HT_RXD7#
AA28	HT_RXD7
AA29	HT_RXD6#
AA30	HT_RXD6
AB1	GPIO_5
AB2	GPIO_2/ CPU_SLP#
AB3	GPIO_3/ CPU_CLKRUN#
AB4	FANCTL1/ GPIO_36
AB5	GND
AB6	TDO
AB7	SPDIF0/ GPIO_33
AB8	AC_SDATA_IN1/ GPIO_27
AB9	+3.3V_DUAL
AB10	LPC_CLK0
AB11	LPC_CLK1
AB12	+1.5V_SP_D
AB13	SP_AGND
AB14	SP_TERMN
AB15	+1.5V_SP_A
AB16	GND
AB17	IDE_DATA_P8
AB18	IDE_DATA_P2
AB19	GND
AB20	IDE_IOW_P#
AB21	IDE_DATA_S5
AB22	GND
AB23	HT_RXCLK1#
AB24	HT_RXCLK1
AB25	HT_RXD12#
AB26	HT_RXD12
AB27	GND
AB28	HT_RXD4#
AB29	HT_RXD5#
AB30	HT_RXD5

Ball	Signal Name
AC2	GPIO_4/ SUS_STAT#
AC3	TMS
AC4	PWRGD
AC5	TRST#
AC6	TDI
AC7	SPDIF1/ GPIO_15
AC8	LPC_FRAME#
AC10	LPC_AD3
AC12	SP_DGND
AC14	SP_TERMP
AC16	GND
AC18	IDE_DATA_P12
AC20	IDE_DREQ_P
AC22	IDE_DATA_S11
AC24	HT_RXD10
AC25	HT_RXD11#
AC26	HT_RXD11
AC27	HT_RXCLK0
AC28	HT_RXCLK0#
AC29	HT_RXD4
AD3	CPUVDD_EN
AD4	THERM#/ GPIO_32
AD5	TCK
AD6	V3P3_DEEP
AD7	GND
AD8	SERIRQ
AD9	GND
AD10	LPC_AD2
AD11	GND
AD12	SP_DGND
AD13	+3.3V_PLL_SP_CORE
AD14	SP_REFCLKN
AD15	+1.5V_SP_A
AD16	IDE_COMP_3P3V
AD17	IDE_DATA_P7
AD18	IDE_DATA_P3
AD19	GND
AD20	IDE_DATA_P15
AD21	GND

Ball	Signal Name
AD22	IDE_DATA_S9
AD23	GND
AD24	HT_RXD10#
AD25	HT_RXD9#
AD26	HT_RXD9
AD27	HT_RXD3
AD28	HT_RXD3#
AE1	GND
AE2	RTC_RST#
AE3	HTVDD_EN
AE4	GND
AE5	TEST
AE6	LID#/ GPIO_7
AE7	LPC_RESET#
AE8	LPC_PWRDWN#/ GPIO_39
AE10	LPC_AD1
AE12	+1.5V_PLL_SP_CORE
AE14	SP_REFCLKP
AE16	IDE_COMP_GND
AE18	IDE_DATA_P4
AE20	IDE_DATA_P0
AE22	IDE_DATA_S10
AE24	IDE_IOW_S#
AE25	GND
AE26	HT_RXD8
AE27	GND
AE28	HT_RXD2#
AE29	HT_RXD2
AE30	GND
AF1	BUF_SIO_CLK
AF2	KBRDRSTIN#/ GPIO_18
AF3	SPKR
AF4	+3.3V_USB_DUAL
AF5	XTALIN_RTC
AF6	SLP_DEEP#
AF7	LPC_DRQ0#
AF8	GND
AF9	LPC_AD0
AF10	GND

Ball	Signal Name
AF11	GND_PLL_SP
AF12	+1.5V_PLL_SP_AVDD
AF13	SP_ATEST
AF14	SP_TESTN
AF15	+1.5V_SP_A
AF16	PCI_RESET3#
AF17	GND
AF18	IDE_DATA_P11
AF19	GND
AF20	IDE_DATA_P14
AF21	IDE_DATA_S6
AF22	IDE_DATA_S4
AF23	IDE_DREQ_S
AF24	IDE_DATA_S15
AF25	THERMTRIP#/ GPIO_26
AF26	HT_RXD8#
AF27	HT_CAL_GND1
AF28	HT_CAL_GND2
AF29	HT_RXD1#
AF30	HT_RXD1
AG1	+1.5V_DUAL
AG2	+1.5V_DUAL
AG3	PWRGD_SB
AG4	XTALOUT_RTC
AG5	SUSCLK/ GPIO_31
AG6	GND
AG7	A20GATE/ GPIO_40
AG8	GPIO_1
AG9	GND
AG10	GND
AG11	SP_RXN1
AG12	+1.5V_PLL_SP_DVDD
AG13	SP_TXP2
AG14	SP_TESTP
AG15	SP_AGND
AG16	SP_AGND
AG17	IDE_DATA_P6
AG18	IDE_DATA_P13
AG19	CABLE_DET_P

Ball	Signal Name
AG20	GND
AG21	IDE_ADDR_P2
AG22	IDE_DATA_S8
AG23	IDE_DATA_S1
AG24	IDE_DATA_S0
AG25	GND
AG26	IDE_CS1_S#
AG27	+3.3V_PLL_CPU
AG28	+3.3V_PLL_HT
AG29	HT_RXD0#
AG30	HT_RXD0
AH1	+3.3V_PLL_USB
AH2	GND
AH3	GND
AH4	+3.3V_VBAT
AH5	EXT_SMI# / GPIO_29
AH6	LLB#
AH7	SLP_S3#
AH8	LPC_CS# / LPC_DRQ1#
AH9	GND
AH10	SP_RXP0
AH11	SP_TXN1
AH12	SP_RXP1
AH13	SP_TXN2
AH14	SP_TXN3
AH15	SP_RXP3
AH16	SP_AGND
AH17	IDE_DATA_P9

Ball	Signal Name
AH18	IDE_DACK_P#
AH19	IDE_ADDR_P1
AH20	IDE_ADDR_P0
AH21	IDE_CS1_P#
AH22	IDE_DATA_S12
AH23	IDE_DATA_S13
AH24	IDE_DATA_S14
AH25	IDE_IOR_S#
AH26	IDE_ADDR_S2
AH27	IDE_CS3_S#
AH28	GND
AH29	XTAL_OUT
AH30	+5V
AJ1	GND
AJ2	PWRBTN#
AJ3	RI# / GPIO_30
AJ4	CPU_VLD
AJ5	SIO_PME# / GPIO_28
AJ6	RSTBTN#
AJ7	SLP_S5#
AJ9	SP_TXN0
AJ10	SP_RXN0
AJ11	SP_TXP1
AJ13	SP_RXP2
AJ14	SP_TXP3
AJ15	SP_RXN3
AJ17	IDE_DATA_P5
AJ18	IDE_RDY_P

Ball	Signal Name
AJ19	IDE_INTR_P
AJ21	IDE_CS3_P#
AJ22	IDE_DATA_S3
AJ23	IDE_DATA_S2
AJ25	IDE_RDY_S
AJ26	IDE_INTR_S
AJ27	IDE_ADDR_S1
AJ28	IDE_ADDR_S0
AJ29	XTAL_IN
AJ30	GND
AK2	GND
AK3	INTRUDER#
AK4	MEM_VLD
AK5	HT_VLD
AK6	GND
AK9	SP_TXP0
AK10	GND
AK13	SP_RXN2
AK14	SP_AGND
AK17	IDE_DATA_P10
AK18	GND
AK21	IDE_DATA_S7
AK22	GND
AK25	GND
AK26	IDE_DACK_S#
AK27	GND
AK28	CABLE_DET_S
AK29	GND

Table 65. Ball Listing by Signal Name

Signal Name	Ball
+1.2V_HT	N21
+1.2V_HT	P21
+1.2V_HT	T21
+1.2V_HT	V21
+1.2V_HT	W21
+1.5V	B30
+1.5V	C29
+1.5V	D27
+1.5V	D28
+1.5V	E26
+1.5V	F25
+1.5V	G24
+1.5V	J21
+1.5V	K20
+1.5V_DUAL	AG1
+1.5V_DUAL	AG2
+1.5V_PE_A	B27
+1.5V_PE_A	B29
+1.5V_PE_A	C26
+1.5V_PE_A	C27
+1.5V_PE_A	C28
+1.5V_PE_A	D26
+1.5V_PE_A	E25
+1.5V_PE_A	F24
+1.5V_PE_A	G23
+1.5V_PE_A	H22
+1.5V_PE_D	C30
+1.5V_PE_D	D29
+1.5V_PE_D	D30
+1.5V_PE_D	E27
+1.5V_PE_D	E28
+1.5V_PE_D	F26
+1.5V_PE_D	F27
+1.5V_PE_D	G25
+1.5V_PE_D	G26
+1.5V_PE_D	H24
+1.5V_PE_D	J22
+1.5V_PE_D	J24
+1.5V_PE_D	K21

Signal Name	Ball
+1.5V_PE_D	K22
+1.5V_PE_D	K23
+1.5V_PE_D	L21
+1.5V_PE_D	L22
+1.5V_PLL_HT	Y21
+1.5V_PLL_PE_AVDD	A27
+1.5V_PLL_PE_CORE	B28
+1.5V_PLL_PE_DVDD	A28
+1.5V_PLL_SP_AVDD	AF12
+1.5V_PLL_SP_CORE	AE12
+1.5V_PLL_SP_DVDD	AG12
+1.5V_SP_A	AA15
+1.5V_SP_A	AB15
+1.5V_SP_A	AD15
+1.5V_SP_A	AF15
+1.5V_SP_D	AA12
+1.5V_SP_D	AB12
+3.3V	J9
+3.3V	L10
+3.3V	R10
+3.3V	U10
+3.3V	W10
+3.3V	Y10
+3.3V	AA11
+3.3V	AA18
+3.3V	AA20
+3.3V_DUAL	M21
+3.3V_DUAL	P4
+3.3V_DUAL	Y9
+3.3V_DUAL	AB9
+3.3V_PLL_CPU	AG27
+3.3V_PLL_DUAL	A29
+3.3V_PLL_HT	AG28
+3.3V_PLL_PE_CORE	B26
+3.3V_PLL_SP_CORE	AD13
+3.3V_PLL_USB	AH1
+3.3V_USB_DUAL	T9
+3.3V_USB_DUAL	AF4
+3.3V_VBAT	AH4

Signal Name	Ball
+5V	A6
+5V	AH30
A20GATE/ GPIO_40	AG7
AC_BITCLK	AA5
AC_RESET#	Y5
AC_SDATA_IN0/ GPIO_14	Y7
AC_SDATA_IN1/ GPIO_27	AB8
AC_SDATA_OUT/ GPIO_13	Y8
AC_SYNC/ GPIO_12	AA9
AC97_CLK	Y6
BUF_25MHZ	M24
BUF_SIO_CLK	AF1
CABLE_DET_P	AG19
CABLE_DET_S	AK28
CPU_CLK	L28
CPU_CLK#	L29
CPU_CLK_66	L27
CPU_COMP	M25
CPU_PWROK	M26
CPU_RST#	M28
CPU_VLD	AJ4
CPUVDD_EN	AD3
EXT_SMI#/ GPIO_29	AH5
FANCTL0/ GPIO_35	AA2
FANCTL1/ GPIO_36	AB4
FANRPM/ GPIO_34	AA3
GND	A2
GND	B1
GND	C6
GND	F1
GND	F7
GND	F30
GND	G27

Signal Name	Ball
GND	H5
GND	H25
GND	J7
GND	K1
GND	K6
GND	K9
GND	K30
GND	L5
GND	L7
GND	L24
GND	L26
GND	M4
GND	M10
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	M23
GND	M27
GND	N7
GND	N10
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N24
GND	P1
GND	P10
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16

Signal Name	Ball
GND	P17
GND	P18
GND	P19
GND	P27
GND	R5
GND	R7
GND	R9
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R21
GND	R22
GND	R24
GND	R26
GND	T4
GND	T10
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T27
GND	U7
GND	U9
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	U21

Signal Name	Ball
GND	U24
GND	V1
GND	V10
GND	V12
GND	V13
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V27
GND	W5
GND	W7
GND	W9
GND	W12
GND	W13
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18
GND	W19
GND	W22
GND	W24
GND	W26
GND	Y4
GND	Y27
GND	AA1
GND	AA7
GND	AA10
GND	AA16
GND	AA21
GND	AA24
GND	AA26
GND	AB5
GND	AB16
GND	AB19
GND	AB22
GND	AB27
GND	AC16

Signal Name	Ball
GND	AD7
GND	AD9
GND	AD11
GND	AD19
GND	AD21
GND	AD23
GND	AE1
GND	AE4
GND	AE25
GND	AE27
GND	AE30
GND	AF8
GND	AF10
GND	AF17
GND	AF19
GND	AG6
GND	AG9
GND	AG10
GND	AG20
GND	AG25
GND	AH2
GND	AH3
GND	AH9
GND	AH28
GND	AJ1
GND	AJ30
GND	AK2
GND	AK6
GND	AK10
GND	AK18
GND	AK22
GND	AK25
GND	AK27
GND	AK29
GND_PLL_PE	A26
GND_PLL_SP	AF11
GPIO_1	AG8
GPIO_2/ CPU_SLP#	AB2
GPIO_3/ CPU_CLKRUN#	AB3

Signal Name	Ball
GPIO_4/ SUS_STAT#	AC2
GPIO_5	AB1
HT_CAL_GND1	AF27
HT_CAL_GND2	AF28
HT_REQ#/ GPIO_10	M22
HT_RXCLK0	AC27
HT_RXCLK0#	AC28
HT_RXCLK1	AB24
HT_RXCLK1#	AB23
HT_RXCTL	Y28
HT_RXCTL#	W27
HT_RXD0	AG30
HT_RXD0#	AG29
HT_RXD1	AF30
HT_RXD1#	AF29
HT_RXD2	AE29
HT_RXD2#	AE28
HT_RXD3	AD27
HT_RXD3#	AD28
HT_RXD4	AC29
HT_RXD4#	AB28
HT_RXD5	AB30
HT_RXD5#	AB29
HT_RXD6	AA30
HT_RXD6#	AA29
HT_RXD7	AA28
HT_RXD7#	AA27
HT_RXD8	AE26
HT_RXD8#	AF26
HT_RXD9	AD26
HT_RXD9#	AD25
HT_RXD10	AC24
HT_RXD10#	AD24
HT_RXD11	AC26
HT_RXD11#	AC25
HT_RXD12	AB26
HT_RXD12#	AB25
HT_RXD13	Y22
HT_RXD13#	AA22
HT_RXD14	Y24

Signal Name	Ball
HT_RXD14#	Y23
HT_RXD15	Y26
HT_RXD15#	Y25
HT_STOP#	N22
HT_TXCLK0	R28
HT_TXCLK0#	R27
HT_TXCLK1	T23
HT_TXCLK1#	T24
HT_TXCTL	W29
HT_TXCTL#	W28
HT_TXD0	N27
HT_TXD0#	N28
HT_TXD1	N29
HT_TXD1#	N30
HT_TXD2	P29
HT_TXD2#	P30
HT_TXD3	P28
HT_TXD3#	R29
HT_TXD4	T28
HT_TXD4#	U27
HT_TXD5	U28
HT_TXD5#	U29
HT_TXD6	U30
HT_TXD6#	V30
HT_TXD7	V29
HT_TXD7#	V28
HT_TXD8	P25
HT_TXD8#	P24
HT_TXD9	P26
HT_TXD9#	N26
HT_TXD10	P22
HT_TXD10#	P23
HT_TXD11	T25
HT_TXD11#	T26
HT_TXD12	U22
HT_TXD12#	T22
HT_TXD13	V26
HT_TXD13#	U26
HT_TXD14	V24
HT_TXD14#	V25
HT_TXD15	V22

Signal Name	Ball
HT_TXD15#	V23
HT_VLD	AK5
HTVDD_EN	AE3
IDE_ADDR_P0	AH20
IDE_ADDR_P1	AH19
IDE_ADDR_P2	AG21
IDE_ADDR_S0	AJ28
IDE_ADDR_S1	AJ27
IDE_ADDR_S2	AH26
IDE_COMP_3P3V	AD16
IDE_COMP_GND	AE16
IDE_CS1_P#	AH21
IDE_CS1_S#	AG26
IDE_CS3_P#	AJ21
IDE_CS3_S#	AH27
IDE_DACK_P#	AH18
IDE_DACK_S#	AK26
IDE_DATA_P0	AE20
IDE_DATA_P1	AA17
IDE_DATA_P2	AB18
IDE_DATA_P3	AD18
IDE_DATA_P4	AE18
IDE_DATA_P5	AJ17
IDE_DATA_P6	AG17
IDE_DATA_P7	AD17
IDE_DATA_P8	AB17
IDE_DATA_P9	AH17
IDE_DATA_P10	AK17
IDE_DATA_P11	AF18
IDE_DATA_P12	AC18
IDE_DATA_P13	AG18
IDE_DATA_P14	AF20
IDE_DATA_P15	AD20
IDE_DATA_S0	AG24
IDE_DATA_S1	AG23
IDE_DATA_S2	AJ23
IDE_DATA_S3	AJ22
IDE_DATA_S4	AF22
IDE_DATA_S5	AB21
IDE_DATA_S6	AF21
IDE_DATA_S7	AK21

Signal Name	Ball
IDE_DATA_S8	AG22
IDE_DATA_S9	AD22
IDE_DATA_S10	AE22
IDE_DATA_S11	AC22
IDE_DATA_S12	AH22
IDE_DATA_S13	AH23
IDE_DATA_S14	AH24
IDE_DATA_S15	AF24
IDE_DREQ_P	AC20
IDE_DREQ_S	AF23
IDE_INTR_P	AJ19
IDE_INTR_S	AJ26
IDE_IOR_P#	AA19
IDE_IOR_S#	AH25
IDE_IOW_P#	AB20
IDE_IOW_S#	AE24
IDE_RDY_P	AJ18
IDE_RDY_S	AJ25
INTRUDER#	AK3
KBRDRSTIN# / GPIO_18	AF2
LID# / GPIO_7	AE6
LLB#	AH6
LPC_AD0	AF9
LPC_AD1	AE10
LPC_AD2	AD10
LPC_AD3	AC10
LPC_CLK0	AB10
LPC_CLK1	AB11
LPC_CS# / LPC_DRQ1#	AH8
LPC_DRQ0#	AF7
LPC_FRAME#	AC8
LPC_PWRDWN# / GPIO_39	AE8
LPC_RESET#	AE7
MEM_VLD	AK4
MII_COL	K26
MII_CRS	K27
MII_RXER / GPIO_21	K29
PCI_AD0	H7

Signal Name	Ball
PCI_AD1	K7
PCI_AD2	J2
PCI_AD3	L9
PCI_AD4	J3
PCI_AD5	J5
PCI_AD6	H8
PCI_AD7	H6
PCI_AD8	K8
PCI_AD9	J4
PCI_AD10	H3
PCI_AD11	G5
PCI_AD12	G6
PCI_AD13	G7
PCI_AD14	H4
PCI_AD15	G3
PCI_AD16	C2
PCI_AD17	C1
PCI_AD18	D2
PCI_AD19	C3
PCI_AD20	B2
PCI_AD21	D3
PCI_AD22	E3
PCI_AD23	E4
PCI_AD24	B4
PCI_AD25	A3
PCI_AD26	A4
PCI_AD27	B3
PCI_AD28	C4
PCI_AD29	C5
PCI_AD30	A5
PCI_AD31	D5
PCI_CBE0#	J1
PCI_CBE1#	G2
PCI_CBE2#	F3
PCI_CBE3#	D4
PCI_CLK0	K3
PCI_CLK1	L2
PCI_CLK2	K2
PCI_CLK3	K5
PCI_CLK4	L3
PCI_CLK5	L4

Signal Name	Ball
PCI_CLKFB	M3
PCI_CLKRUN# / GPIO_9	N4
PCI_DEVSEL#	E1
PCI_FRAME#	F4
PCI_GNT0#	M7
PCI_GNT1#	M6
PCI_GNT2# / GPIO_8	M5
PCI_GNT3# / GPIO_17	K4
PCI_GNT4# / GPIO_46	P7
PCI_INTW#	B5
PCI_INTX#	E6
PCI_INTY#	E5
PCI_INTZ#	D6
PCI_IRDY#	D1
PCI_PAR	G4
PCI_PERR# / GPIO_38	F5
PCI_PME# / GPIO_37	P6
PCI_REQ0#	N5
PCI_REQ1#	N9
PCI_REQ2# / GPIO_6	M9
PCI_REQ3# / GPIO_16	M8
PCI_REQ4# / GPIO_45	P5
PCI_RESET0#	N2
PCI_RESET1#	N1
PCI_RESET2#	N3
PCI_RESET3#	AF16
PCI_SERR#	F6
PCI_STOP#	F2
PCI_TRDY#	E2
PE_AGND	B6
PE_AGND	D7
PE_AGND	D12
PE_AGND	D16
PE_AGND	D20
PE_AGND	D25

Signal Name	Ball
PE_AGND	E7
PE_AGND	E11
PE_AGND	E15
PE_AGND	E19
PE_AGND	G8
PE_AGND	G9
PE_AGND	G11
PE_AGND	G13
PE_AGND	G15
PE_AGND	G17
PE_AGND	G19
PE_AGND	G21
PE_AGND	J12
PE_AGND	J13
PE_AGND	J14
PE_AGND	J20
PECLK_COMP_GND	E24
PE_CLK_TEST	C25
PE_CLK_TEST#	D24
PE_DGND	K10
PE_DGND	K11
PE_DGND	K12
PE_DGND	K13
PE_DGND	K14
PE_DGND	K15
PE_DGND	K16
PE_DGND	K17
PE_DGND	K18
PE_REFCLK_IN	A25
PE_REFCLK_IN#	B25
PE_RST#	E22
PE_WAKE#	E23
PE0_PRSNT#	D22
PE0_REFCLK	B19
PE0_REFCLK#	C18
PE0_RX0	H18
PE0_RX0#	G18
PE0_RX1	F18
PE0_RX1#	E17
PE0_RX2	J18
PE0_RX2#	J17

Signal Name	Ball
PE0_RX3	H16
PE0_RX3#	G16
PE0_RX4	E16
PE0_RX4#	F16
PE0_RX5	D14
PE0_RX5#	E14
PE0_RX6	J16
PE0_RX6#	J15
PE0_RX7	H14
PE0_RX7#	G14
PE0_RX8	E13
PE0_RX8#	F14
PE0_RX9	H12
PE0_RX9#	G12
PE0_RX10	E12
PE0_RX10#	F12
PE0_RX11	J11
PE0_RX11#	J10
PE0_RX12	D10
PE0_RX12#	E10
PE0_RX13	H10
PE0_RX13#	G10
PE0_RX14	F10
PE0_RX14#	E9
PE0_RX15	E8
PE0_RX15#	F8
PE0_TX0	A18
PE0_TX0#	B18
PE0_TX1	A17
PE0_TX1#	B17
PE0_TX2	C17
PE0_TX2#	D17
PE0_TX3	C16
PE0_TX3#	D15
PE0_TX4	C15
PE0_TX4#	B15
PE0_TX5	C14
PE0_TX5#	B14
PE0_TX6	A14
PE0_TX6#	A13
PE0_TX7	B13

Signal Name	Ball
PE0_TX7#	C13
PE0_TX8	D13
PE0_TX8#	C12
PE0_TX9	D11
PE0_TX9#	C11
PE0_TX10	B11
PE0_TX10#	C10
PE0_TX11	B10
PE0_TX11#	A10
PE0_TX12	B9
PE0_TX12#	A9
PE0_TX13	C9
PE0_TX13#	D9
PE0_TX14	C8
PE0_TX14#	D8
PE0_TX15	C7
PE0_TX15#	B7
PE1_PRSNT#	G22
PE1_REFCLK	D21
PE1_REFCLK#	C20
PE1_RX	D18
PE1_RX#	E18
PE1_TX	D19
PE1_TX#	C19
PE2_PRSNT#	F22
PE2_REFCLK	C24
PE2_REFCLK#	D23
PE2_RX	F20
PE2_RX#	E20
PE2_TX	B21
PE2_TX#	C21
PE3_PRSNT#	E21
PE3_REFCLK	C23
PE3_REFCLK#	B23
PE3_RX	H20
PE3_RX#	G20
PE3_TX	C22
PE3_TX#	B22
PE4_RX	K19
PE4_RX#	J19
PE4_TX	A22

Signal Name	Ball
PE4_TX#	A21
PWRBTN#	AJ2
PWRGD	AC4
PWRGD_SB	AG3
RGMII_INTR/ MII_INTR/ GPIO_11	K28
RGMII_MDC/ MII_MDC	K24
RGMII_MDIO/ MII_MDIO	J30
RGMII_PWRDWN/ MII_PWRDWN/ GPIO_20	K25
RGMII_RXCLK/ MII_RXCLK	H27
RGMII_RXCTL/ MII_RXDV	G28
RGMII_RXD0/ MII_RXD0	G29
RGMII_RXD1/ MII_RXD1	E30
RGMII_RXD2/ MII_RXD2	F29
RGMII_RXD3/ MII_RXD3	F28
RGMII_TXCLK/ MII_TXCLK	H26
RGMII_TXCTL/ MII_TXEN	J26
RGMII_TXD0/ MII_TXD0	H28
RGMII_TXD1/ MII_TXD1	J27
RGMII_TXD2/ MII_TXD2	J28
RGMII_TXD3/ MII_TXD3	J29
RGMII_VREF/ MII_VREF	E29
RI#/ GPIO_30	AJ3
RSTBTN#	AJ6
RTC_RST#	AE2
SERIRQ	AD8
SIO_PME#/ GPIO_28	AJ5
SLP_DEEP#	AF6

Signal Name	Ball
SLP_S3#	AH7
SLP_S5#	AJ7
SMB_CLK0/ GPIO_41	Y3
SMB_CLK1/ GPIO_43	W2
SMB_DATA0/ GPIO_42	W4
SMB_DATA1/ GPIO_44	W3
SP_AGND	AA13
SP_AGND	AB13
SP_AGND	AG15
SP_AGND	AG16
SP_AGND	AH16
SP_AGND	AK14
SP_ATEST	AF13
SP_DGND	AC12
SP_DGND	AD12
SP_LED#/ GPIO_19	AA14
SP_REFCLKN	AD14
SP_REFCLKP	AE14
SP_RXN0	AJ10
SP_RXN1	AG11
SP_RXN2	AK13
SP_RXN3	AJ15
SP_RXP0	AH10
SP_RXP1	AH12
SP_RXP2	AJ13
SP_RXP3	AH15
SP_TERMN	AB14
SP_TERMP	AC14
SP_TESTN	AF14
SP_TESTP	AG14
SP_TXN0	AJ9
SP_TXN1	AH11
SP_TXN2	AH13
SP_TXN3	AH14
SP_TXP0	AK9
SP_TXP1	AJ11
SP_TXP2	AG13
SP_TXP3	AJ14

Signal Name	Ball
SPDIF0/ GPIO_33	AB7
SPDIF1/ GPIO_15	AC7
SPKR	AF3
SUSCLK/ GPIO_31	AG5
TCK	AD5
TDI	AC6
TDO	AB6
TEST	AE5
THERM#/ GPIO_32	AD4
THERMTRIP#/ GPIO_26	AF25
TMS	AC3
TRST#	AC5
USB_0	P2

Signal Name	Ball
USB_0#	P3
USB_1	P8
USB_1#	P9
USB_2	R2
USB_2#	R3
USB_3	T3
USB_3#	R4
USB_4	U3
USB_4#	U4
USB_5	U1
USB_5#	U2
USB_6	T5
USB_6#	T6
USB_7	T7
USB_7#	T8
USB_8	U5
USB_8#	V6

Signal Name	Ball
USB_9	V7
USB_9#	V8
USB_OC0#	V4
USB_OC1#/ GPIO_22	V5
USB_OC2#/ GPIO_23	V3
USB_OC3#/ GPIO_24	V2
USB_OC4#/ GPIO_25	AA4
USB_RBIAS	V9
V3P3_DEEP	AD6
XTAL_IN	AJ29
XTAL_OUT	AH29
XTALIN_RTC	AF5
XTALOUT_RTC	AG4

Appendix B. Ballout

This appendix contains the ballout for the NVIDIA nForce4 Ultra.

- Ball Locations
  - Ballout (top left view)
  - Ballout (top right view)

Ballout (Top Left View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A		GND	PCI_AD25	PCI_AD26	PCI_AD30	+5V			PE0_TX12#	PE0_TX11#			PE0_TX6#	PE0_TX6	
B	GND	PCI_AD20	PCI_AD27	PCI_AD24	PCI_INTW#	PE_AGND	PE0_TX15#		PE0_TX12	PE0_TX11	PE0_TX10		PE0_TX7	PE0_TX5#	PE0_TX4#
C	PCI_AD17	PCI_AD16	PCI_AD19	PCI_AD28	PCI_AD29	GND	PE0_TX15	PE0_TX14	PE0_TX13	PE0_TX10#	PE0_TX9#	PE0_TX8#	PE0_TX7#	PE0_TX5	PE0_TX4
D	PCI_IRDY#	PCI_AD18	PCI_AD21	PCI_CBE3#	PCI_AD31	PCI_INTZ#	PE_AGND	PE0_TX14#	PE0_TX13#	PE0_RX12	PE0_TX9	PE_AGND	PE0_TX8	PE0_RX5	PE0_TX3#
E	PCI_ DEVSEL#	PCI_TRDY#	PCI_AD22	PCI_AD23	PCI_INTY#	PCI_INTX#	PE_AGND	PE0_RX15	PE0_RX14#	PE0_RX12#	PE_AGND	PE0_RX10	PE0_RX8	PE0_RX5#	PE_AGND
F	GND	PCI_STOP#	PCI_CBE2#	PCI_FRAME#	PCI_PERR#/ GPIO_38	PCI_SERR#	GND	PE0_RX15#		PE0_RX14		PE0_RX10#		PE0_RX8#	
G		PCI_CBE1#	PCI_AD15	PCI_PAR	PCI_AD11	PCI_AD12	PCI_AD13	PE_AGND	PE_AGND	PE0_RX13#	PE_AGND	PE0_RX9#	PE_AGND	PE0_RX7#	PE_AGND
H			PCI_AD10	PCI_AD14	GND	PCI_AD7	PCI_AD0	PCI_AD6		PE0_RX13		PE0_RX9		PE0_RX7	
J	PCI_CBE0#	PCI_AD2	PCI_AD4	PCI_AD9	PCI_AD5		GND		+3.3V	PE0_RX11#	PE0_RX11	PE_AGND	PE_AGND	PE_AGND	PE0_RX6#
K	GND	PCI_CLK2	PCI_CLK0	PCI_GNT3#/ GPIO_17	PCI_CLK3	GND	PCI_AD1	PCI_AD8	GND	PE_DGND	PE_DGND	PE_DGND	PE_DGND	PE_DGND	PE_DGND
L		PCI_CLK1	PCI_CLK4	PCI_CLK5	GND		GND		PCI_AD3	+3.3V					
M			PCI_CLKFB	GND	PCI_GNT2#/ GPIO_8	PCI_GNT1#	PCI_GNT0#	PCI_REQ3#/ GPIO_16	PCI_REQ2#/ GPIO_6	GND		GND	GND	GND	GND
N	PCI_ RESET1#	PCI_ RESET0#	PCI_ RESET2#	PCI_CLKRUN#/ GPIO_9	PCI_REQ0#		GND		PCI_REQ1#	GND		GND	GND	GND	GND
P	GND	USB_0	USB_0#	+3.3V_DUAL	PCI_REQ4#/ GPIO_45	PCI_PME#/ GPIO_37	PCI_GNT4#/ GPIO_46	USB_1	USB_1#	GND		GND	GND	GND	GND
R		USB_2	USB_2#	USB_3#	GND		GND		GND	+3.3V		GND	GND	GND	GND
T			USB_3	GND	USB_6	USB_6#	USB_7	USB_7#	+3.3V_USB_ DUAL	GND		GND	GND	GND	GND
U	USB_5	USB_5#	USB_4	USB_4#	USB_8		GND		GND	+3.3V		GND	GND	GND	GND
V	GND	USB_OC3#/ GPIO_24	USB_OC2#/ GPIO_23	USB_OC0#	USB_OC1#/ GPIO_22	USB_8#	USB_9	USB_9#	USB_RBIAS	GND		GND	GND	GND	GND
W		SMB_CLK1/ GPIO_43	SMB_DATA1/ GPIO_44	SMB_DATA0/ GPIO_42	GND		GND		GND	+3.3V		GND	GND	GND	GND
Y			SMB_CLK0/ GPIO_41	GND	AC_RESET#	AC97_CLK	AC_SDATA_IN0/ GPIO_14	AC_SDATA_OUT/ GPIO_13	+3.3V_DUAL	+3.3V					
AA	GND	FANCTL0/ GPIO_35	FANRPM/ GPIO_34	USB_OC4#/ GPIO_25	AC_BITCLK		GND		AC_SYNC/ GPIO_12	GND	+3.3V	+1.5V_SP_D	SP_AGND	SP_LED#/ GPIO_19	+1.5V_SP_ A
AB	GPIO_5	GPIO_2/ CPU_SLP#	GPIO_3/ CPU_CLKRUN#	FANCTL1/ GPIO_36	GND	TDO	SPDIF0/ GPIO_33	AC_SDATA_IN1/ GPIO_27	+3.3V_DUAL	LPC_CLK0	LPC_CLK1	+1.5V_SP_D	SP_AGND	SP_TERMN	+1.5V_SP_ A
AC		GPIO_4/ SUS_STAT#	TMS	PWRGD	TRST#	TDI	SPDIF1/ SPDIF_15	LPC_FRAME#		LPC_AD3		SP_DGND		SP_TERMP	
AD			CPUVDD_EN	THERM#/ GPIO_32	TCK	V3P3_DEEP	GND	SERIRQ	GND	LPC_AD2	GND	SP_DGND	+3.3V_PLL_ SP_CORE	SP_ REFCLKN	+1.5V_SP_ A
AE	GND	RTC_RST#	HTVDD_EN	GND	TEST	LID#/ GPIO_7	LPC_RESET#	LPC_PWRDWN#/ GPIO_39		LPC_AD1		+1.5V_PLL_ SP_CORE		SP_ REFCLKP	
AF	BUF_ SIO_CLK	KBRDRSTIN#/ GPIO_30	SPKR	+3.3V_ USB_DUAL	XTALIN_RTC	SLP_DEEP#	LPC_DRQ0#	GND	LPC_AD0	GND	GND_PLL_SP	+1.5V_PLL_ SP_AVDD	SP_ATEST	SP_TESTN	+1.5V_SP_ A
AG	+1.5V_ DUAL	+1.5V_DUAL	PWRGD_SB	XTALOUT_ RTC	SUSCLK/ GPIO_31	GND	A20GATE/ GPIO_40	GPIO_1	GND	GND	SP_RXN1	+1.5V_PLL_ SP_DVDD	SP_TXP2	SP_TESTP	SP_AGND
AH	+3.3V_PLL_ USB	GND	GND	+3.3V_VBAT	EXT_SMI#/ GPIO_29	LLB#	SLP_S3#	LPC_CS#/ LPC_DRQ1#	GND	SP_RXP0	SP_TXN1	SP_RXP1	SP_TXN2	SP_TXN3	SP_RXP3
AJ	GND	PWRBTN#	RI#/ GPIO_30	CPU_VLD	SIO_PME#/ GPIO_28	RSTBTN#	SLP_S5#		SP_TXN0	SP_RXN0	SP_TXP1		SP_RXP2	SP_TXP3	SP_RXN3
AK		GND	INTRUDER#	MEM_VLD	HT_VLD	GND			SP_TXP0	GND			SP_RXN2	SP_AGND	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Ballout (Top Right View)

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
	PE0_TX1	PE0_TX0			PE4_TX#	PE4_TX			PE_REFCLK_IN	GND_PLL_PE	+1.5V_PLL_PE_AVDD	+1.5V_PLL_PE_DVDD	+3.3V_PLL_DUAL		A
	PE0_TX1#	PE0_TX0#	PE0_REFCLK		PE2_TX	PE3_TX#	PE3_REFCLK#		PE_REFCLK_IN#	+3.3V_PLL_PE_CORE	+1.5V_PE_A	+1.5V_PLL_PE_CORE	+1.5V_PE_A	+1.5V	B
PE0_TX3	PE0_TX2	PE0_REFCLK#	PE1_TX#	PE1_REFCLK#	PE2_TX#	PE3_TX	PE3_REFCLK	PE2_REFCLK	PE_CLK_TEST	+1.5V_PE_A	+1.5V_PE_A	+1.5V_PE_A	+1.5V	+1.5V_PE_D	C
PE_AGND	PE0_TX2#	PE1_RX	PE1_TX	PE_AGND	PE1_REFCLK	PE0_PRSNT#	PE2_REFCLK#	PE_CLK_TEST#	PE_AGND	+1.5V_PE_A	+1.5V	+1.5V	+1.5V_PE_D	+1.5V_PE_D	D
PE0_RX4	PE0_RX1#	PE1_RX#	PE_AGND	PE2_RX#	PE3_PRSNT#	PE_RST#	PE_WAKE#	PECLK_COMP_GND	+1.5V_PE_A	+1.5V	+1.5V_PE_D	+1.5V_PE_D	RGMII_VREF/MII_VREF	RGMII_RXD1/MII_RXD1	E
PE0_RX4#		PE0_RX1		PE2_RX		PE2_PRSNT#		+1.5V_PE_A	+1.5V	+1.5V_PE_D	+1.5V_PE_D	RGMII_RXD3/MII_RXD3	RGMII_RXD2/MII_RXD2	GND	F
PE0_RX3#	PE_AGND	PE0_RX0#	PE_AGND	PE3_RX#	PE_AGND	PE1_PRSNT#	+1.5V_PE_A	+1.5V	+1.5V_PE_D	+1.5V_PE_D	GND	RGMII_RXCTL/MII_RXDV	RGMII_RXD/MII_RXD0		G
PE0_RX3		PE0_RX0		PE3_RX		+1.5V_PE_A		+1.5V_PE_D	GND	RGMII_TXCLK/MII_TXCLK	RGMII_RXCLK/MII_RXCLK	RGMII_TXD0/MII_TXD0			H
PE0_RX6	PE0_RX2#	PE0_RX2	PE4_RX#	PE_AGND	+1.5V	+1.5V_PE_D		+1.5V_PE_D		RGMII_TXCTL/MII_TXEN	RGMII_TXD1/MII_TXD1	RGMII_TXD2/MII_TXD2	RGMII_TXD3/MII_TXD3	RGMII_MIDIO/MII_MDIO	J
PE_DGND	PE_DGND	PE_DGND	PE4_RX	+1.5V	+1.5V_PE_D	+1.5V_PE_D	+1.5V_PE_D	RGMII_MDC/MII_MDC	RGMII_PWRDWN/MII_PWRDWN/GPIO20	MII_COL	MII_CRS	RGMII_INTR/MII_INTR/GPIO_11	MII_RXER/GPIO_21	GND	K
					+1.5V_PE_D	+1.5V_PE_D		GND		GND	CPU_CLK_66	CPU_CLK	CPU_CLK#		L
GND	GND	GND	GND		+3.3V_DUAL	HT_REQ#/GPIO_10	GND	BUF_25MHZ	CPU_COMP	CPU_PWROK	GND	CPU_RST#			M
GND	GND	GND	GND		+1.2V_HT	HT_STOP#		GND		HT_TXD9#	HT_TXD0	HT_TXD0#	HT_TXD1	HT_TXD1#	N
GND	GND	GND	GND		+1.2V_HT	HT_TXD10	HT_TXD10#	HT_TXD8#	HT_TXD8	HT_TXD9	GND	HT_TXD3	HT_TXD2	HT_TXD2#	P
GND	GND	GND	GND		GND	GND		GND		GND	HT_TXCLK0#	HT_TXCLK0	HT_TXD3#		R
GND	GND	GND	GND		+1.2V_HT	HT_TXD12#	HT_TXCLK1	HT_TXCLK1#	HT_TXD11	HT_TXD11#	GND	HT_TXD4			T
GND	GND	GND	GND		GND	HT_TXD12		GND		HT_TXD13#	HT_TXD4#	HT_TXD5	HT_TXD5#	HT_TXD6	U
GND	GND	GND	GND		+1.2V_HT	HT_TXD15	HT_TXD15#	HT_TXD14	HT_TXD14#	HT_TXD13	GND	HT_TXD7#	HT_TXD7	HT_TXD6#	V
GND	GND	GND	GND		+1.2V_HT	GND		GND		GND	HT_RXCTL#	HT_TXCTL#	HT_TXCTL		W
					+1.5V_PLL_HT	HT_RXD13	HT_RXD14#	HT_RXD14	HT_RXD15#	HT_RXD15	GND	HT_RXCTL			Y
GND	IDE_DATA_P1	+3.3V	IDE_IOR_P#	+3.3V	GND	HT_RXD13#		GND		GND	HT_RXD7#	HT_RXD7	HT_RXD6#	HT_RXD6	AA
GND	IDE_DATA_P8	IDE_DATA_P2	GND	IDE_IOW_P#	IDE_DATA_S5	GND	HT_RXCLK1#	HT_RXCLK1	HT_RXD12#	HT_RXD12	GND	HT_RXD4#	HT_RXD5#	HT_RXD5	AB
GND		IDE_DATA_P12		IDE_DREQ_P		IDE_DATA_S11		HT_RXD10	HT_RXD11#	HT_RXD11	HT_RXCLK0	HT_RXCLK0#	HT_RXD4		AC
IDE_COMP_3P3V	IDE_DATA_P7	IDE_DATA_P3	GND	IDE_DATA_P15	GND	IDE_DATA_S9	GND	HT_RXD10#	HT_RXD9#	HT_RXD9	HT_RXD3	HT_RXD3#			AD
IDE_COMP_GND		IDE_DATA_P4		IDE_DATA_P0		IDE_DATA_S10		IDE_IOW_S#	GND	HT_RXD8	GND	HT_RXD2#	HT_RXD2	GND	AE
PCI_RESET3#	GND	IDE_DATA_P11	GND	IDE_DATA_P14	IDE_DATA_S6	IDE_DATA_S4	IDE_DREQ_S	IDE_DATA_S15	THERMTRIP#/GPIO_26	HT_RXD8#	HT_CAL_GND1	HT_CAL_GND2	HT_RXD1#	HT_RXD1	AF
SP_AGND	IDE_DATA_P6	IDE_DATA_P13	CABLE_DET_P	GND	IDE_ADDR_P2	IDE_DATA_S8	IDE_DATA_S1	IDE_DATA_S0	GND	IDE_CS1_S#	+3.3V_PLL_CPU	+3.3V_PLL_HT	HT_RXD0#	HT_RXD0	AG
SP_AGND	IDE_DATA_P9	IDE_DACK_P#	IDE_ADDR_P1	IDE_ADDR_P0	IDE_CS1_P#	IDE_DATA_S12	IDE_DATA_S13	IDE_DATA_S14	IDE_IOR_S#	IDE_ADDR_S2	IDE_CS3_S#	GND	XTAL_OUT	+5V	AH
	IDE_DATA_P5	IDE_RDY_P	IDE_INTR_P		IDE_CS3_P#	IDE_DATA_S3	IDE_DATA_S2		IDE_RDY_S	IDE_INTR_S	IDE_ADDR_S1	IDE_ADDR_S0	XTAL_IN	GND	AJ
	IDE_DATA_P10	GND			IDE_DATA_S7	GND			GND	IDE_DACK_S#	GND	CABLE_DET_S	GND		AK
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