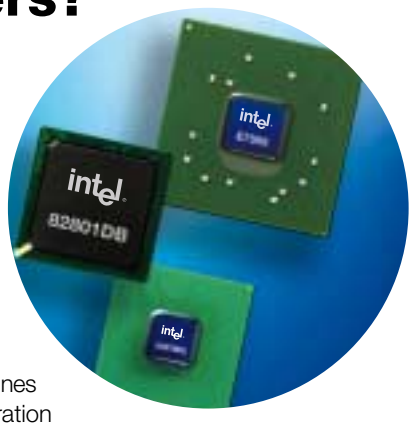
Can one chipset deliver advanced technology and I/O flexibility for both workstations and servers?

The Intel® E7505 chipset takes full advantage of the latest Intel® Xeon™ processors to deliver performance-packed workstation and server platforms!



Intel® E7505 Chipset

The E7505 chipset represents the next step in Intel® workstation and server chipset technology. The latest in a family of volume enterprise chipsets, the E7505 chipset supports dual-processor platforms optimized for the Intel® Xeon™ processor with 533 MHz system bus and Intel® NetBurst™ microarchitecture. The E7505 chipset design combines 533 MHz system bus with faster memory speed, next-generation AGP 8X graphics, and improved I/O bandwidth. Intel Xeon processor-based platforms with the E7505 chipset deliver higher performance than previous Intel® processor-based systems for mechanical design and analysis, digital content creation and a variety of other demanding high-performance computing tasks.

Advanced Technology, Next-Generation Graphics, and I/O Flexibility

The E7505 chipset is comprised of three core components, which offer platform implementation flexibility to meet the demanding needs of dual-processor (DP) systems.

The E7505 Chipset Memory Controller Hub (MCH) is the central hub for all data passing through core system elements, such as: the dual Intel Xeon processors via the system bus interface; the memory subsystem through a dual-channel DDR memory interface; the graphics subsystem over an AGP 8X interface; I/O controller hubs via Intel® Hub Interface architecture. The E7505 chipset delivers the compelling performance of 4.3 GB/s of bandwidth across a 533 MHz system bus and up to 4.3 GB/s of bandwidth across two high-performance Double-Data-Rate (DDR) SDRAM memory channels. The MCH offers the designer the flexibility to support either unbuffered or registered memory. The high data throughput of these interfaces augment the direct-attach AGP 8X interface, which delivers up to 2.1 GB/s of graphics data.

The Intel® 82870P2 64-bit PCI/PCI-X Controller Hub 2 connects to the MCH through a point-to-point 16-bit Hub Interface connection. The Intel 82870P2 64-bit PCI/PCI-X controller hub 2 device extends over 1.0 GB/s of I/O bandwidth to two independent 64-bit PCI-X segments operating at 133/100/66 MHz. Each 64-bit PCI-X segment supports next-generation components such as Intel® Gigabit Ethernet adapters and multiple PCI-X or PCI slots.

The Intel® 82801DB I/O Controller Hub (ICH4) connects to the MCH through a point-to-point Hub Interface 1.5 connection. The Intel® ICH4 offers greater bandwidth for I/O-intensive peripherals through an integrated controller for six ports Hi-Speed USB 2.0. In addition, the ICH4 adds new audio and power management capabilities.

Features that Balance the Platform and Maximize Performance

- Dual Intel Xeon processors with 533 MHz system bus provides up to 4.3 GB/s of available bandwidth.
- Dual DDR266 memory channels provide up to 4.3 GB/s of memory bandwidth.
- The direct attach AGP 8X port provides 2.1 GB/s of graphics bandwidth directly out of the MCH.
- The Hub Interface connection allows high-bandwidth I/O configurations; exceeding 1.0 GB/s of I/O bandwidth.

Features	Benefits
Intel® Xeon™ processors with 533 MHz system bus for dual-processing platforms	Brings increased system bus performance and Hyper-Threading Technology of the Intel Xeon processor to workstations and servers.
533 MHz system bus capability	Supports a high-performance, balanced platform by enabling a 4.3 GB/s system bus bandwidth that can support greater memory, graphics and I/O bandwidths.
Dual-channel DDR266	Provides 4.3 GB/s of memory bandwidth for balanced performance on the Intel Xeon processor with 533 MHz system bus platforms.
APG 8X Interface	Next-generation graphics interface, delivering 2.1 GB/s of graphics bandwidth directly from the MCH, for use with the most advanced AGP 8X graphics cards.
Unbuffered or Registered DDR Memory	Allows design flexibility for diverse enterprise applications.
Memory ECC	Memory error correction code for greater reliability.
Intel® Hub architecture	Dedicated data paths for transferring greater than 1.0 GB/s of data to and from the MCH, which support I/O segments with greater reliability and faster access to high-speed networks.
Intel® x4 Single Device Data Correction (x4 SDDC)**	Allows continued memory operation in the event of a single device failure.
Integrated Hi-Speed USB 2.0	Six ports offer up to 40 times greater bandwidth over the original USB 1.1 for the most demanding I/O peripherals.
Alert on LAN* 2.0	Emits an alert in case of software failures or system intrusion, even when the O/S is not present or the system is suspended.
Intel® Application Accelerator	Software that helps accelerate boot time and application launch time.
AC'97 controller	Supports Dolby* Digital 5.1 Surround Sound, delivering up to six channels of enhanced sound quality.
Low-power sleep mode	Saves energy.

Products	Package
Intel® Xeon™ Processor with 533 MHz System Bus	604 Flip Chip-Pin Grid Array (FC-PGA)
Intel® E7505 Memory Controller Hub (MCH)	1005 Flip Chip-Ball Grid Array (FC-BGA)
Intel® 82870P2 64-bit PCI/PCI-X Controller Hub 2	567 Flip Chip-Ball Grid Array (FC-BGA)
Intel® 82801DB I/O Controller Hub	421 Micro Ball Grid Array (µBGA*)

Intel Access

Products Web Site	http://www.intel.com/products/server
Intel® Chipsets Home Page	http://www.intel.com/products/server/chipsets
Intel® Xeon™ Processor with 533 MHz System Bus	http://www.intel.com/design/xeon
Intel® Gigabit Ethernet Controllers	http://developer.intel.com/design/network/products/ethernet/index.htm
Intel® I/O Processor	http://developer.intel.com/design/iio/index.htm
Other Intel Support: Intel Literature Center	http://developer.intel.com/design/litcentr/ (800) 548-4725 7 am–7 pm CST (USA and Canada) International locations please contact your local sales office.
General Information Hotline	(800) 628-8686 or (916) 356-3104 5 am–5 pm PST

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**In a x4 DDR memory device, the Intel® x4 Single Device Data Correction (x4 SDDC), provides error detection and correction for 1, 2, 3, or 4 data bits within that single device and provides error detection, up to 8 data bits, within two devices.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

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