Intel® Xeon™ Processor and Intel® E7505 Chipset

Platform Design Guide

For Use with Intel® Xeon™ Processor with 512-KB L2 Cache and Intel® Xeon™ Processor with 533 MHz System Bus

December 2002

Document Number: 251934-003

Contents

Figures

Tables

Revision History

Revision	Description	Date
–001	Initial release.	November 2002
–002	Updated Title Page and documentation to include ***Intel® Xeon™ Processor with 533 MHz System Bus*** **references**	November 2002
-003	Updated for MCH Core voltage of 1.3 V Updated Memory Routing section with DIMM ordering recomendation Added RCOMP value for VCC1_3	December 2002

This page is intentionally left blank.

Introduction 1

The *Intel® Xeon™ Processor and Intel® E7505 Chipset Platform Design Guide* describes Intel's design recommendations for systems that are based on the Intel® Xeon™ processor with 512-KB L2 cache, Intel® Xeon™ processor with 533 MHz System Bus, and the Intel® E7505 chipset. The document provides motherboard design recommendations such as layout and routing guidelines, and addresses other system design issues such as power delivery. For specific design issues such as thermal considerations, refer to the design guides and application notes listed in Section 1.1, "Reference Documentation".

asf

In this document, "processor" and "chipset" refer to the Intel Xeon processor with 512-KB L2 cache, Intel® Xeon™ processor with 533 MHz System Bus, and the E7505 chipset. Where a reference is intended to refer to a specific processor, the specific processor is listed.

The *Intel® Xeon™ Processor / Intel® E7505 Chipset Platform Design Guide* has been developed to ensure maximum flexibility for board designers, while reducing board design risks. The design information provided in this document falls under one of the two following categories:

- *Design Recommendations.* These are items that are based on Intel's simulations and lab experience, are strongly recommended, and may be necessary to meet timing and signal quality specifications.
- *Design Considerations.* These are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel and should be used as examples, but may not be applicable to specific designs.

Note: The guidelines recommended in this document are based on experience, simulation, and validation work performed by Intel during development of Intel® Xeon™ Processor / Intel® E7505 chipset-based systems. This work is ongoing, and the recommendations are subject to change.

Platform schematics are included in Appendix A. The schematics are for a specific design implementation, but the core schematics remain the same for most platforms that are based on the chipset. The schematic set provides a reference schematic for each chipset component, as well as common motherboard options. Additional flexibility is possible through other permutations of these options and components.

1.1 Reference Documentation

Item	Document Location/Number
Intel® Xeon Processor with 512-KB L2 Cache Datasheet.	298642
Intel® Xeon Processor with 533 MHz Sysytem Bus Datasheet.	252135
ITP700 Debug Port Design Guide	http://developer.intel.com/design/Xeon/guides/249679.htm
Intel® Xeon™ Processor Thermal Design Guidelines	http://developer.intel.com/design/Xeon/guides/298348.htm
Intel® Xeon™ Processor Thermal Solution Functional Specifications	http://developer.intel.com/design/Xeon/applnots/249673.htm
603-Pin Socket Design Guidelines	http://developer.intel.com/design/Xeon/guides/249672.htm
Intel® Xeon™ Processor with 512-KB L2 Cache Thermal Models	http://developer.intel.com/design/Xeon/devtools/
Intel® Xeon™ Processor with 512-KB L2 Cache Mechanical Model in IGES Format	http://developer.intel.com/design/Xeon/devtools/
Intel® Xeon™ Processor with 512-KB L2 Cache Mechanical Model in ProE* Format	http://developer.intel.com/design/Xeon/devtools/
Intel® E7505 Chipset Memory Controller Hub (MCH) Datasheet	251932
Intel® E7505 Chipset Signal Length Matching Spreadsheet	Note 1
Intel® NetBurst™ Microarchitecture BIOS Writer's Guide	Note 1
Voltage Regulator Module (VRM) 9.1 DC-DC Converter Design Guidelines	http://developer.intel.com/design/Xeon/guides
Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines	http://developer.intel.com/design/Xeon/guides/298644.htm
Intel® Xeon™ Processor with 512-KB L2 Cache System Compatibility Guidelines	Note 1
Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet	290732
Intel® P64H2 Thermal Design Guidelines	Note 1
PCI Local Bus Specification	http://www.pcisig.com/
PCI-PCI Bridge Specification	http://www.pcisig.com/
PCI Bus Power Management Interface Specification	http://www.pcisig.com/
PCI-X Specification	http://www.pcisig.com/
Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet	http://www.intel.com/design/chipsets/datashts/290744.HTM
ICH/ICH4/ICH4-M/ICH3-S/ICH3-M Real Time Clock (RTC) Accuracy and Considerations Under Test (Application Note AP-728)	http://www.intel.com/design/chipsets/applnots/292276.htm
JEDEC DDR SDRAM Unbuffered DIMM Design Specification	www.jedec.org
JEDEC DDR SDRAM Unbuffered DIMM Design Specification Addendum	http://www.intel.com/technology/memory/ddr/specs/ddr200_unbuff_dimm_spec_09.htm
JEDEC DDR SDRAM Registered DIMM Design Specification	http://www.intel.com/technology/memory/ddr/specs/ddr200_reg_dimm_spec_10.htm/

Item	Document Location/Number
Intel® 82562ET 10/100 Mbps Platform LAN Connect (PLC) Networking Silicon Datasheet	http://fdbl.intel.com/servlet/opencontentservlet?OBJID=09000d2980129c13
CK408 Clock Synthesizer/Driver Specification	Note 1
AC '97 Component Specification, Revision 2.3	http://developer.intel.com/ial/scalableplatforms/audio/
ATA/ATAPI-6 Standard	http://T13.org
Accelerated Graphics Port Interface Specification 3.0, Revision 0.95	http://www.agpforum.org/
Low Pin Count Interface Specification, Revision 1.0	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus 2.0 Specification	http://www.usb.org/
Advance Configuration and Power Interface (ACPI) Specification	http://www.teleport.com/~acpi/
Microsoft Windows* Logo Program System and Device Requirements	www.microsoft.com/hwdev/winlogo

NOTES:
1. Contact your Intel representative for the latest version of this item.

1.2 Terminology

This section defines conventions and terminology that is used throughout the design guide.

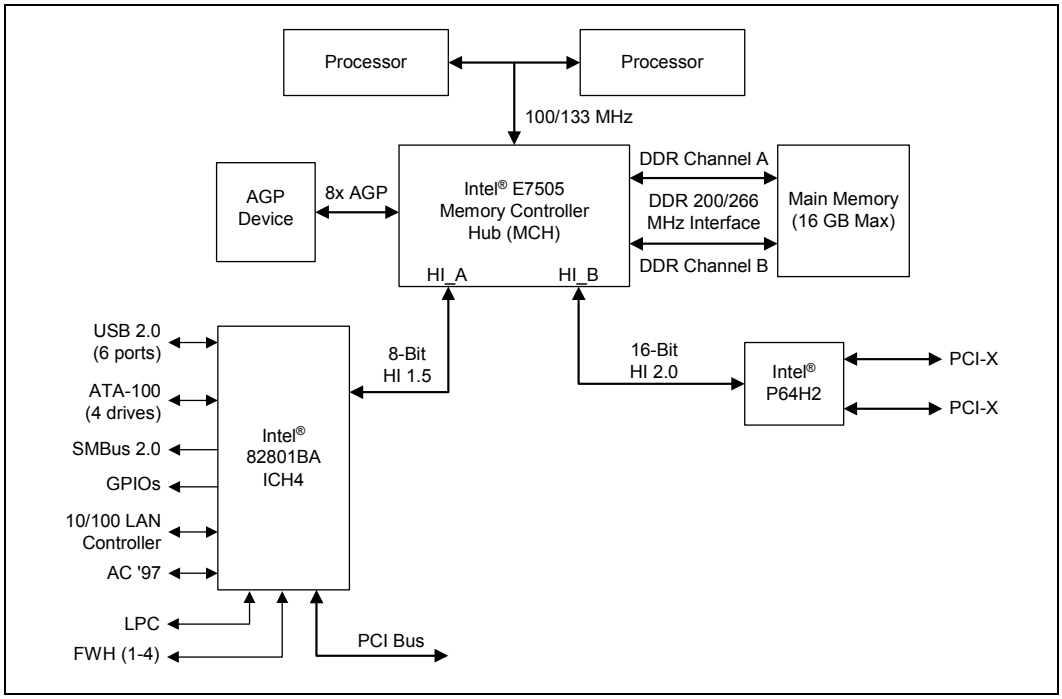
Term	Description
Aggressor	A network that transmits a coupled signal to another network.
AGTL+	The processor's system buses use a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to assist the pull-up resistors during the first clock of a low-to-high voltage transition.
Asynchronous GTL+	Intel® Pentium 4 processors with 512-KB L2 cache on 0.13 micron process do not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output FERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to HCLKINP/HCLKINN. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two HCLKINs in order for the processor to recognize them.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk - Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. • Forward Crosstalk - Coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal. • Even Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the Tco of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, flight time is defined as: • The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings. • Maximum and Minimum Flight Time - Flight time variations are caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects. • Maximum flight time is the largest acceptable flight time a network will experience under all conditions. Minimum flight time is the smallest acceptable flight time a network will experience under all conditions.
Flip Chip Ball Grid Array (FCBGA)	Microprocessor packaging using "flip chip" design, where the processor is attached to the substrate face-down for better signal integrity, more efficient heat removal and lower inductance.

Term	Description
FC-mPGA2	Packaging technology with the processor die mounted directly to a micro-Pin Grid Array substrate with an integrated heat spreader (IHS).
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line, and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes and electrical connection between two or more components.
Overshoot	The maximum voltage observed for a signal at the device pad, measured with respect to VCC_CPU.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.
Pin	The contact point of a component package to the traces on a substrate, such as the motherboard. Signal quality and timings can be measured at the pin.
Power-Good	“Power-Good” or “PWRGOOD” (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.
Ringback	The voltage that a signal changes to after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.
System Bus	The System Bus is the microprocessor bus of the processor.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
SSO	Simultaneous Switching Output (SSO) effects are differences in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (“push-out”) or a decrease in propagation delay (“pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	The minimum voltage extending below VSS observed for a signal at the device pad.
VCC_CPU	VCC_CPU is the core power for the processor. The System Bus is terminated to VCC_CPU.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.

1.3 System Overview

The E7505 chipset is designed for use with the Intel® Xeon™ processor with 533 MHz System Bus and the Intel Xeon processor with 512-KB L2 cache. The architecture of the E7505 chipset provides the performance and feature-set required for dual processor-based workstation systems. Figure 1-1 shows an example processor / chipset system configuration for workstation platforms.

Figure 1-1. Example Processor / Chipset-Based System Configuration



1.3.1 Intel® Xeon™ Processor

The processor is the second generation of microprocessors using the Intel® NetBurst™ microarchitecture. The processor delivers performance levels that are significantly higher than previous generations of IA-32 processors. The E7505 chipset supports the Intel® Xeon™ processor with 533 MHz System Bus and the Intel Xeon processor with 512-KB L2 cache.

The processors are available in the following packages. The Intel® Xeon™ processor with 533 MHz System Bus will be offered only in the FC-mPGA2 package. The Intel Xeon processor with 512-KB L2 cache will be offered only in the Interposer Micro-Pin Grid Array (INT-mPGA) package. A major difference between these two processors is that Intel® Xeon™ processor with 533 MHz System Bus lacks the Processor Information ROM (PIROM), OEM EEPROM, thermal sensor, and SMBus that are available on the INT-mPGA package.

- The PIROM is a 128-byte read-only device that incorporates Intel processor-specific data.
- The OEM EEPROM, also known as the “scratchpad EEPROM”, is a 128-byte read/write EEPROM in which an OEM may program system specific data.
- The thermal sensor monitors the temperature of the processor die.

The processors in the FC-mPGA2 package still contain the thermal diode, but also provide direct access to the diode output pins. These output pins can interface with a thermal sensor device that is placed on the motherboard.

Another difference is that the Intel Xeon processor with 533 MHz Sysytem Bus in the FC-mPGA2 package require a new socket termed "604-pin socket." Table 1-1 summarizes the main features offered in the different versions of the processor. Chapter 6 contains additional guidelines for systems that are intended to support the processor with 533 MHz system bus support. Refer to the *Intel® Xeon Processor with 533MHz Sysytem Bus Datasheet* for complete details about the processor.

Table 1-1. Processor Feature Set Overview

Feature	Intel Xeon processor with 512-KB L2 cache **(INT-mPGA Package)**	Intel Xeon processor with 533 MHz System Bus **(FC-mPGA2 Package)**
L2 Cache	512 KB	
Data Bus Transfer Rate	3.2 GB/s	4.3 GB/s
Multi-Processor Support	1 – 2 Processors	
Manageability Features	PIROM and Scratch EEPROMs and Thermal Sensor on Package	Direct Thermal Diode Access
Socket	603-Pin Socket	604-Pin Socket Only
Package Dimensions	X-Y: 53.5 mm Z: 5.0 mm	X-Y: 42.5 mm Z: 3.6 mm

The processor includes the following advanced Intel NetBurst microarchitecture features:

- Hyper Pipelined Technology
- Advanced Dynamic Execution
- Execution Trace Cache
- Streaming SIMD (Single Instruction, Multiple Data) Extensions 2
- Advanced Transfer Cache
- Enhanced Floating Point and Multimedia Engine
- Hyper-Threading Technology

The processor system bus utilizes a split-transaction, deferred reply protocol similar to that of the P6 bus. However, the system bus is not compatible with the P6 bus. The processor system bus is compatible with the Intel Xeon processor system bus. The system bus uses source-synchronous transfer of address and data to improve performance, and enables addressing at 2X the system bus frequency and data transfers at 4X the system bus frequency of 100 MHz or 133 MHz. This allows the processor with 400 MHz system bus support to transfer data at 3.2 GB/s, and the processor with 533 MHz system bus support to transfer data at 4.3 GB/s, as indicated in Table 1-1.

1.3.2 Intel® E7505 Chipset

The chipset consists of three major components: the Memory Controller (MCH), the I/O Controller 4 (ICH4), and the PCI-X 64-bit 2.0 (P64H2). All of these components are interconnected via an Intel proprietary interface called the Hub Interface that is designed to provide efficient communications between components.

Additional hardware platform features include:

- AGP 8X and 4X modes
- DDR PC2100 system memory
- Ultra ATA/100
- Low Pin Count (LPC) interface
- Integrated LAN
- Universal Serial Bus 2.0.

The platform is also ACPI compliant, and supports Full-on, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-off power management states.

1.3.2.1 Intel® E7505 Chipset Memory Controller Hub (MCH)

The MCH is available in a 1005-ball FC-BGA package.

1.3.2.1.1 System Bus Features

- Supports dual processors at 400 or 533 MHz
- System bus bandwidth of 3.2 or 4.3 GB/s
- Supports 36-bit system bus addressing model
- 12 deep in-order queue, 2 deep defer queue

1.3.2.1.2 Memory Bus Features

- 144-bit wide, DDR PC2100 memory interface. Memory bandwidth of 4.3 GB/s
- Supports x72, ECC, registered or unbuffered DDR PC2100 DIMMs using 128 Mb, 256 Mb, 512 Mb, and 1 GB DRAMs
- Supports a maximum of 16 GB of memory[1]
- Supports Intel® x4 Single Device Data Correction (x4 SDDC) technology (x4 DRAM devices only)[2]
- Supports up to 32 simultaneous open pages

Note:

1. Maximum usable address space is 15.94 GB
2. In a x4 DDR memory device, the Intel® x4 Single Device Data Correction (x4 SDDC) provides error detection and correction for 1, 2, 3, or 4 data bits within that single device and provides error detection, up to 8 data bits, with two devices.

1.3.2.1.3 AGP 8X Bus Features

- Single AGP device
- AGP interface asynchronously coupled to core
- AGP 3.0 Specification
- AGP 8X / 4X at 1.5 V
- 0.8 V and 1.5 V AGP electrical. No 3.3 V support
- Isochronous support for AGP 8X, non-snooped
- 32 deep AGP request queue
- 32-bit upstream address support for inbound AGP and PCI cycles
- 32-bit downstream address support for outbound PCI and Fast Write cycles

1.3.2.1.4 I/O Features

- HI 1.5 Connection for ICH4 (Hub Interface A)
- Hl1.5 = HI 1.0 protocols with HI 2.0 electrical characteristics
- 266 MB/s point-to-point connection for ICH4 with parity protection
- 8-bit wide, 66 MHz base clock, 4X data transfer
- Parallel termination mode for longer trace lengths
- 64-bit inbound addressing, 32-bit outbound addressing
- 1 HI 2.0 Connection for P64H2 (Hub Interface B)
- 1 GB/s point-to-point connection for I/O bridges with ECC protection
- 16-bit wide, 66 MHz base clock, 8X data transfer
- Parallel termination mode for longer trace lengths
- 64-bit inbound addressing, 32-bit outbound addressing

1.3.2.2 Intel® I/O Controller Hub 4 (ICH4)

The ICH4 provides the legacy I/O subsystem for E7505 chipset-based platforms. Additionally, it integrates many advanced I/O functions. The ICH4 includes:

- HI 1.5 Connection to MCH
  - 266 MB/s point-to-point connection for ICH4 with parity protection
  - 8-bit wide, 66 MHz base clock, 4X data transfer
  - Parallel termination mode for longer trace lengths
  - 64-bit inbound addressing, 32-bit outbound addressing
- 2 channel Ultra ATA/100 bus master IDE controller
- 3 Universal Host Controller Interface (UHCI) USB host controllers (capabilities for six ports)
- USB 2.0 High Speed Debug Port
- SMBus 2.0 controller

- LPC interface
- AC '97 v2.3 interface
- PCI v2.2 interface
- Integrated LAN Controller

1.3.2.3 Intel® PCI-X 64-Bit Hub 2 (P64H2)

The P64H2 provides the PCI-X, high-performance I/O capability on this processor/chipset platform. The P64H2 component includes:

- 16-bit, HI 2.0 Connection to MCH
  - 1 GB/s point-to-point connection for I/O bridges with ECC protection
  - 16-bit wide, 66 MHz base clock, 8X data transfer
  - Parallel termination mode for longer trace lengths
  - 64-bit inbound addressing, 32-bit outbound addressing
- Two Independent, 64-bit PCI-X interfaces
  - PCI-X specification, version 1.0 compliant
  - PCI specification, version 2.2 compliant
  - PCI-PCI Bridge specification revision 1.1 compliant
  - PCI peer-to-peer write capability between PCI ports
  - SM Bus target for Out-of-Band (OOB) access to all internal PCI registers
- Two IOxAPICs
  - 16 external/18 internal interrupts

1.3.3 Processor Support

Table 1-2 provides a summary of the supported processor configurations for the chipset-based platform.

Table 1-2. Supported Processor Configurations

Processor (P0) System Bus (MHz)	Processor (P1) System Bus (MHz)	Installed Memory	Allowable	Comment
400	400	DDR PC1600	Yes	Validated
400	400	DDR PC2100	Yes	Validated
400	533	DDR PC1600	No	Not validated
400	533	DDR PC2100	No	Not validated
533	400	DDR PC1600	No	Not validated
533	400	DDR PC2100	No	Not validated
533	533	DDR PC1600	No	Not validated
533	533	DDR PC2100	Yes	Validated

1.3.4 DIMM Support

Table 1-3 provides a summary of the supported memory configurations for the chipset-based platform.

Table 1-3. DIMM Support Summary

Type	Unbuffered	Registered
Dual Channel	1 to 2 pairs of DIMMs (4 rows)	1 to 2 pairs of DIMMS (6 rows max)

1.3.5 Bandwidth Summary

Table 1-4 describes the clock speed, sample rate, and bandwidth for each of the interfaces in the chipset-based platform.

Table 1-4. Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth (MB/s)
System Bus (Data)	133	4	8	4300
System Bus (Address)	133	2	4	1066
DDR Interface	133	2	16	4300
DDR Interface	100	2	16	3200
Hub Interface A	66	4	1	266
Hub Interface B	66	8	2	1066
AGP 8X	66	8	4	2032
PCI-X	133	1	8	1066

This page is intentionally left blank.

Component Quadrant Layout 2

The following quadrant layout figures do not show exact component ball counts – only general quadrant information. Use only exact ball assignments to conduct routing analyses. Refer to the following documents for ball assignment information.

- *Intel® E7505 Chipset Memory Controller Hub (MCH) Datasheet*
- *Intel® Xeon Processor with 512-KB L2 Cache Datasheet*
- *Intel® Xeon Processor with 533 MHz System Bus Datasheet*
- *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*

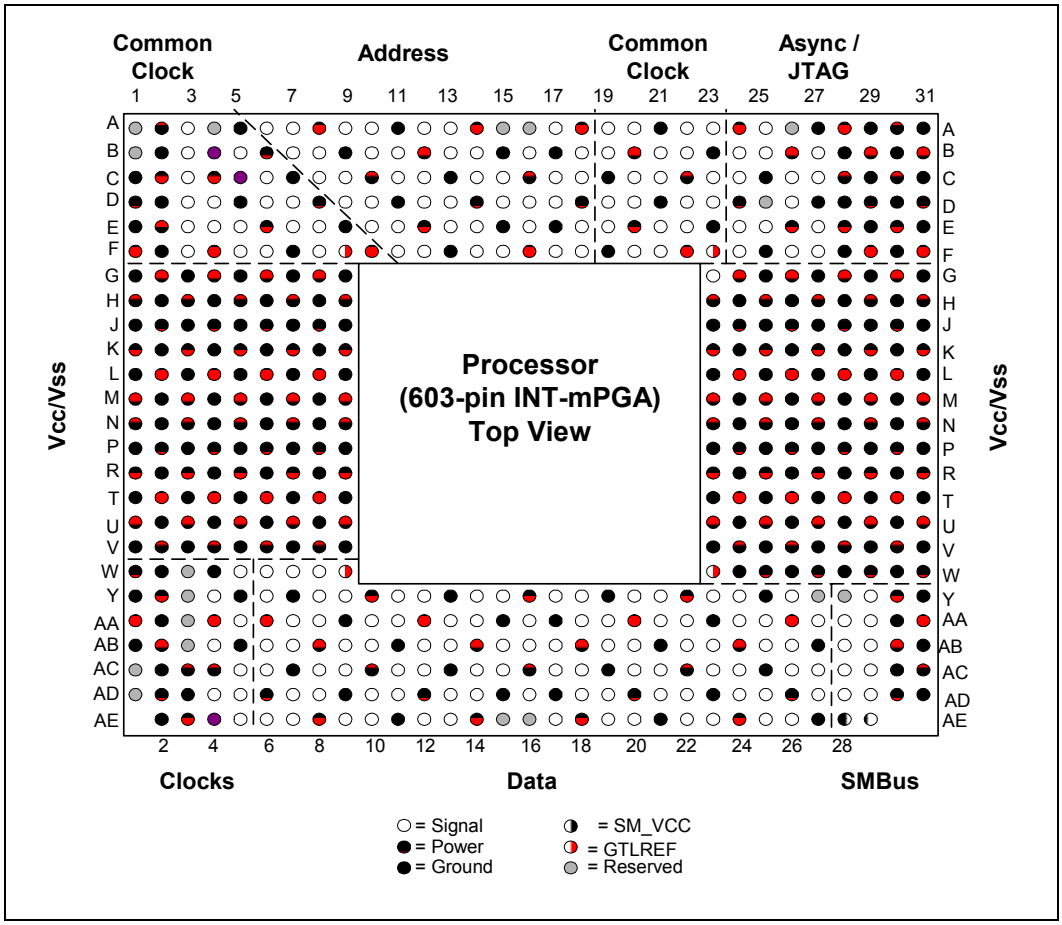
Note: All figures in this section show top views.

2.1 Processor Quadrant Layout

2.1.1 Processor in the 603-Pin INT-mPGA Package Quadrant Layout

Figure 2-1 shows the quadrant layout of the processor in the 603-pin INT-mPGA package.

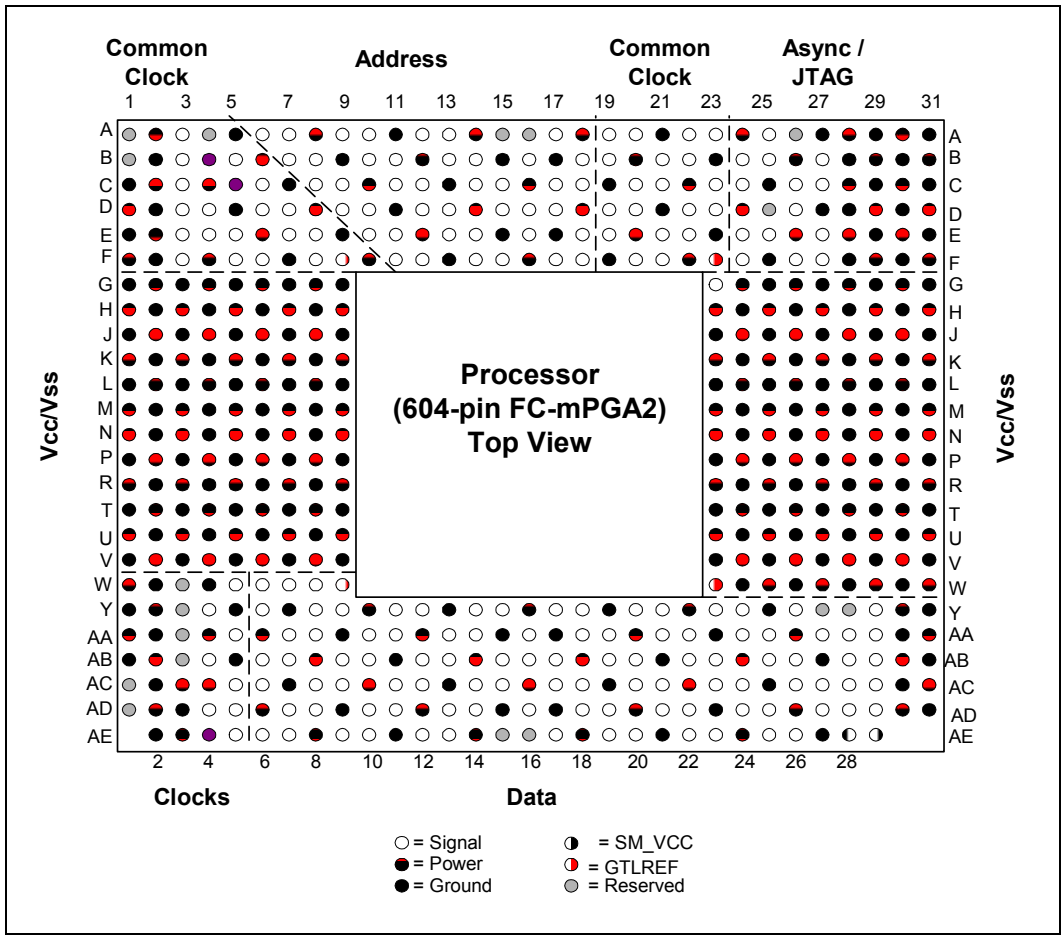
Figure 2-1. Processor in the 603-pin INT-mPGA Package Quadrant Layout (Top View)



2.1.2 Processor in the 604-Pin FC-mPGA2 Package Quadrant Layout

Figure 2-2 shows the quadrant layout of the processor in the 604-pin FC-mPGA2 package.

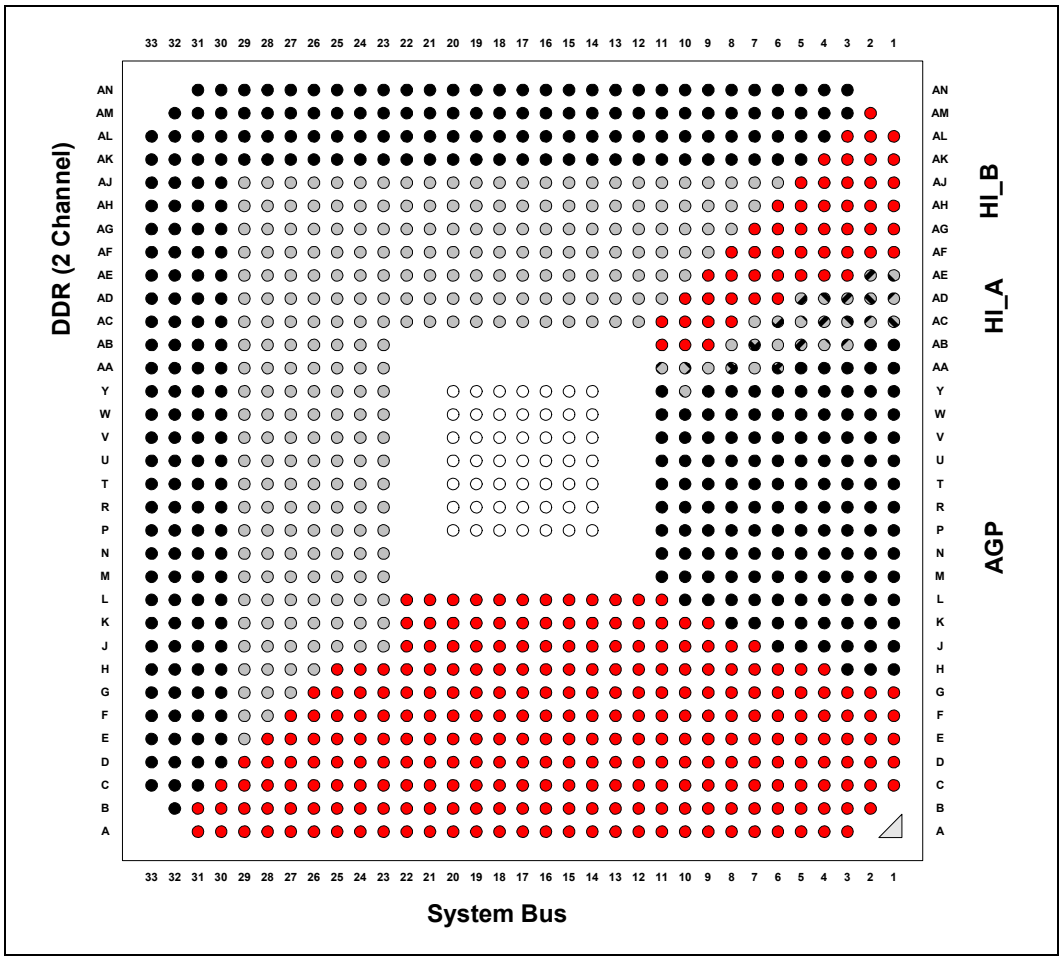
Figure 2-2. Processor in the 604-pin FC-mPGA2 Package Quadrant Layout (Top View)



2.2 MCH Quadrant Layout

Figure 2-3 shows the quadrant layouts of the MCH chipset component.

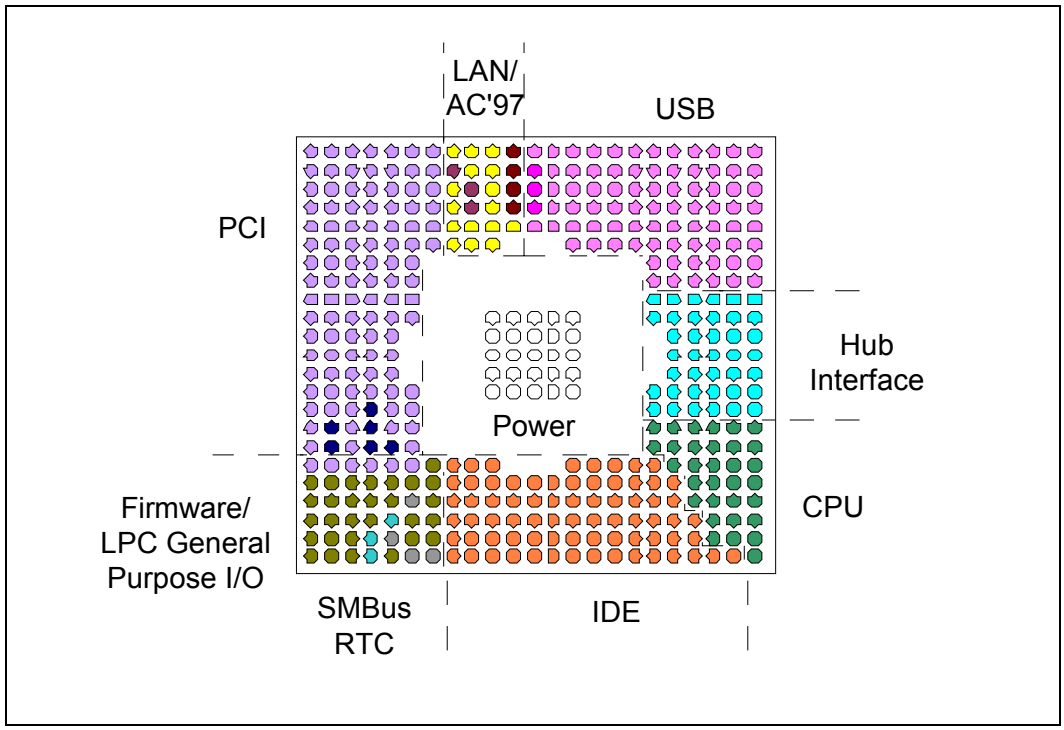
Figure 2-3. MCH Quadrant Layout (Top View)



2.3 Intel® ICH4 Quadrant Layout

Figure 2-4 shows the quadrant layout of the ICH4 chipset component.

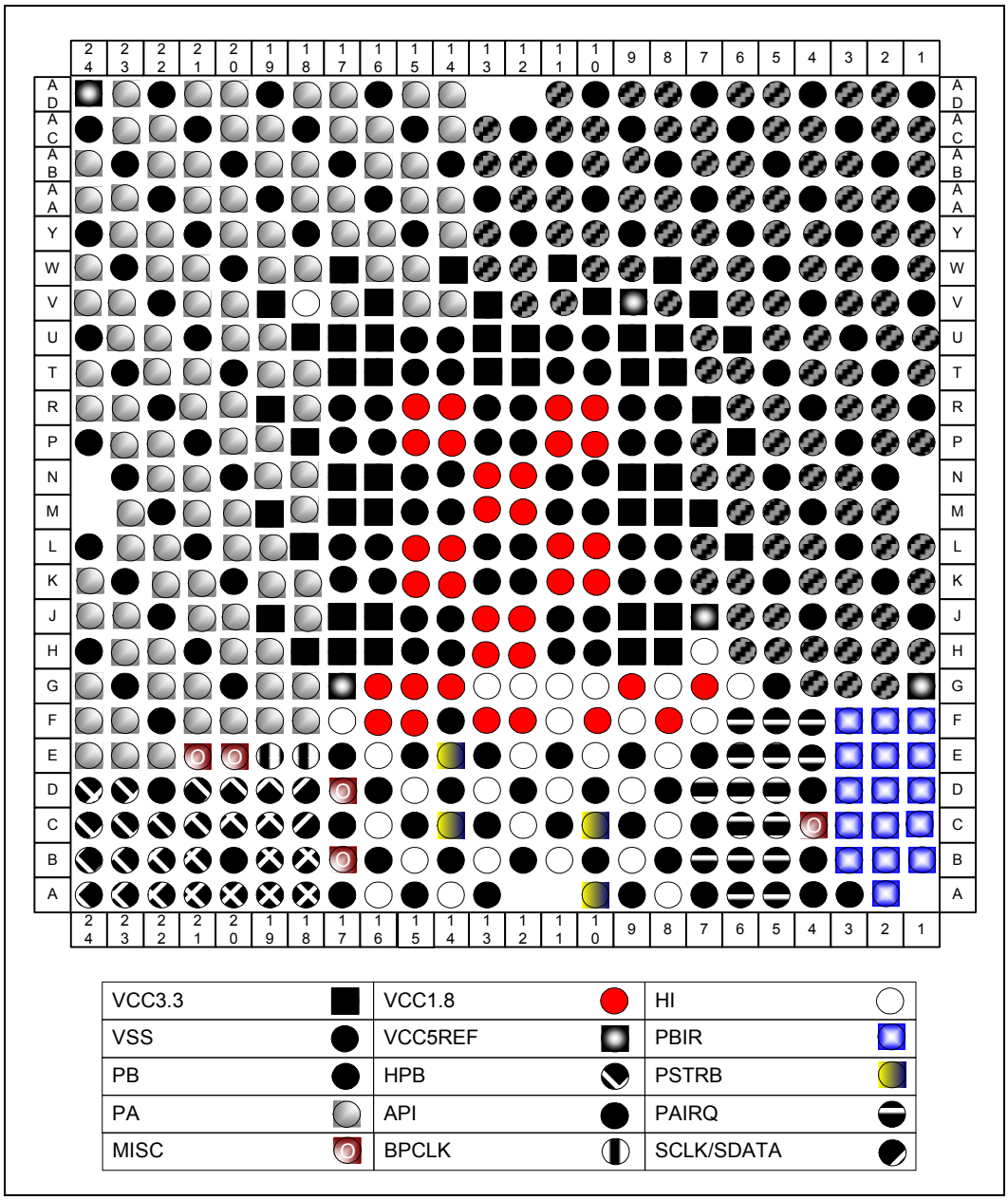
Figure 2-4. Intel® ICH4 Quadrant Layout (Top View)



2.4 Intel® P64H2 Quadrant Layout

Figure 2-5 shows the quadrant layouts of the P64H2 chipset component.

Figure 2-5. Intel® P64H2 Quadrant Layout



Platform Clock Routing Guidelines 3

To minimize jitter, improve routing, and reduce cost, this processor/chipset based system will use a single chip clock solution, the CK408. The CK408 provides three 133/100 MHz differential output pairs for all of the bus agents, and six 66 MHz speed clocks that drive all I/O buses. Figure 3-1 shows the implementation of the bus clocks for this configuration. For more information on CK408, refer to the *CK408 Clock Synthesizer/Driver Specification* listed in Section 1.1.

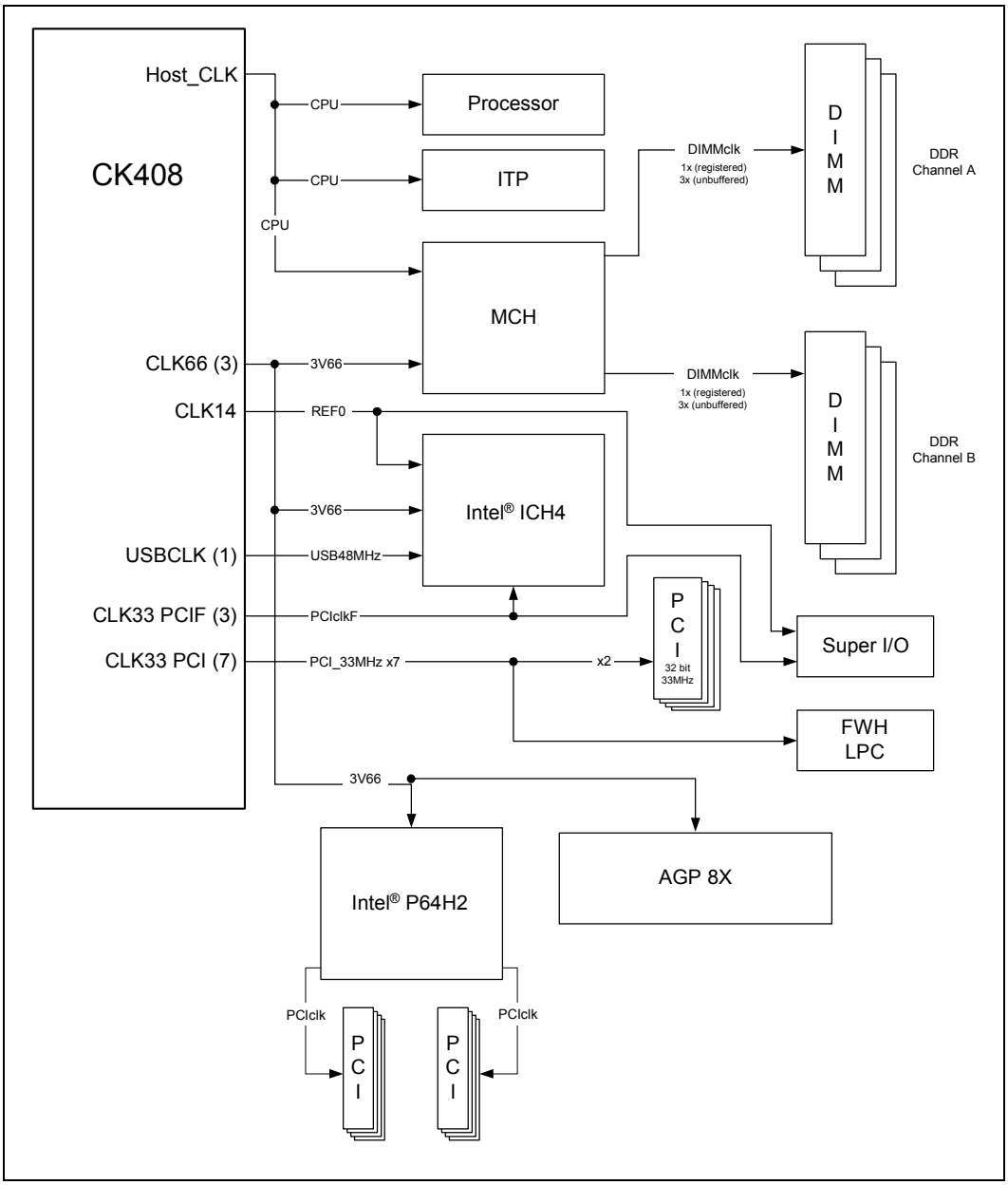
Table 3-1. Intel® E7505 Chipset Platform Clock Groups

Clock Name	Frequency (MHz)	Receiver
Host_CLK	133/100	CPU0, CPU1, MCH, Debug Port
CLK66	66	MCH, Intel® ICH4, AGP, Intel® P64H2
CLK33	33	PCI Connector, ICH4, SIO, FWH
CLK14	14.318	ICH4, SIO
USBCLK	48	ICH4

Table 3-2. Platform System Clock Cross-Reference

Clock Group	CK-408	Component	Component Pin Name
HOST_CLK	CPU3#	Debug Port	BCLK1
	CPU3	Debug Port	BCLK0
	CPU0#	CPU0	BCLK1
	CPU0	CPU0	BCLK0
	CPU1#	CPU1	BCLK1
	CPU1	CPU1	BCLK0
	CPU2#	MCH	HCLKINN
	CPU2	MCH	HCLKINP
CLK66	3V66_5	Intel® ICH4	CLK66
	3V66_4	Intel® P64H2	CLK66
	3V66_3	MCH	GCLKIN
	3V66_2	AGP	AGPCLK
	3V66_1	Debug Header	N/A
	3V66_0	Debug Header	N/A
CLK33	PCI_33MHz	Slot 4	CLK
		Slot 5	CLK
		Port 80	CLK
		FWH, LPC	CLK, CLK
		PCI ROM	N/A
		Available Clock	N/A
		Available Clock	N/A
	PCIclkF	ICH4	PCICLK
		SIO	PCICLK
		Available Clock	N/A
CLK14	REF0	ICH4	CLK14
		SIO	CLOCKI
USBCLK	USB48MHz	ICH4	CLK48

Figure 3-1. Intel® E7505 Chipset-Based System Clocking Diagram



3.1 Clock Groups

3.1.1 HOST_CLK Clock Group

3.1.1.1 HOST_CLK Clock Topology

The CK408 clock synthesizer provides three sets of 133/100 MHz differential clock outputs. The differential clocks are driven to the processors, the chipset, and the processor debug port as shown in Figure 3-1.

The clock driver differential bus output structure is a “Current Mode Current Steering” output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors, R_T. The resulting amplitude is determined by multiplying I_{OUT} by the value of R_T. The current I_{OUT} is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of R_T to match impedances or to accommodate future load requirements.

The recommended termination for the differential bus clock is a “Shunt Source Termination.” Refer to Figure 3-2 for an illustration of this terminology method. Parallel R_T resistors perform a dual function: converting the current output of the clock driver to a voltage, and matching the driver output impedance to the transmission line. The series resistors, R_S,, provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor, R_T.

The value of R_T should be selected to match the characteristic impedance of the motherboard, and R_S should be between 20 Ω and 33 Ω. Simulations indicate that R_S values above 33 Ω provide no benefit to signal integrity and degrade the edge rate.

Figure 3-2. Source Shunt Termination

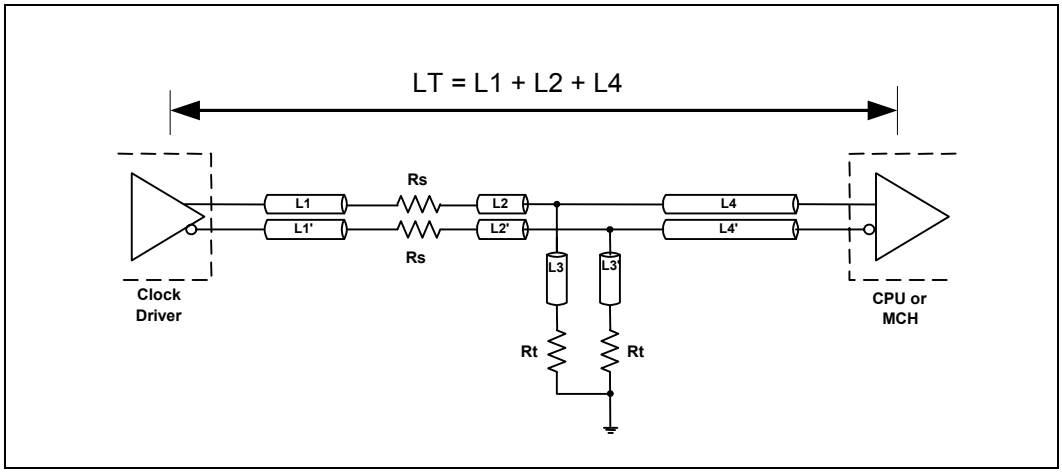


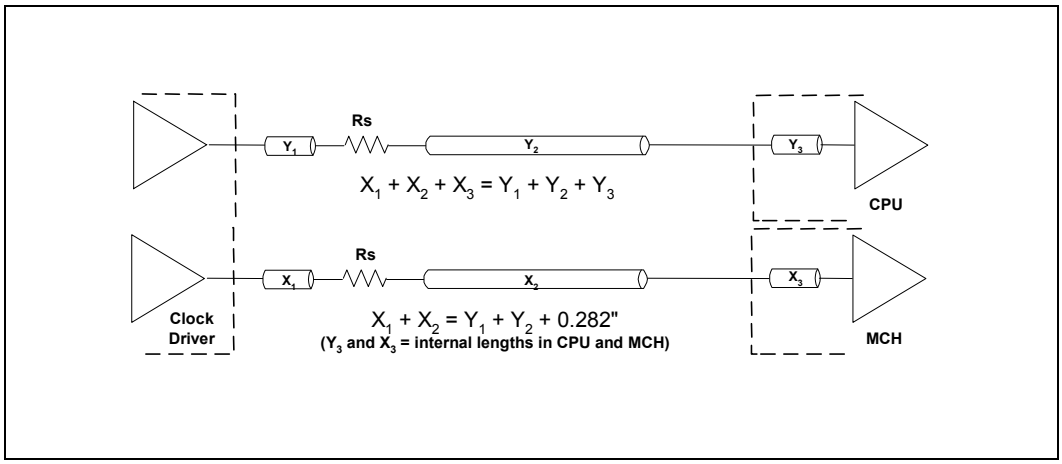
Table 3-3. HOST_CLK Routing Guidelines

Layout Guideline	Value	Illustration	Notes
HCLKIN skew between agents	300 ps total Budget: 150 ps for clock driver 150 ps for interconnect	Figure 3-2 and Figure 3-4	1,2,3,4
Differential pair spacing	20 – 25 mils	Figure 3-5	5,6
Spacing to other traces	25 mils	Figure 3-5	
Serpentine spacing	Maintain a minimum S/h ratio of > 5/26 Keep parallel serpentine sections as short as possible. Minimize 90 degree bends. Make 45 degree bends, if possible.	Figure 3-5	
Motherboard impedance – differential	100 Ω typical		8
Motherboard impedance – single ended	50 Ω ± 10%		9
Processor routing length – L1, L1': Clock driver to R_S	0.5 inch max	Figure 3-2	13
Processor routing length – L2, L2': R_S to R_S-R_T node	0 – 0.2 inch"	Figure 3-2	13
Processor routing length – L3, L3': R_S-R_T node to R_T	0 – 0.2 inch	Figure 3-2	13
Processor routing length – L4, L4': R_S-R_T Node to Load	0 – 22 inches	Figure 3-2	
MCH routing length – L1, L1': Clock Driver to R_S	0.5 inch max	Figure 3-2	13
MCH routing length – L2, L2': R_S to R_S-R_T node	0 – 0.2 inch	Figure 3-2	13
MCH routing length – L3, L3': R_S-R_T node to R_T	0 – 0.2 inch	Figure 3-2	13
MCH routing length – L4, L4': R_S-R_T Node to Load	0 – 22 inches	Figure 3-2	
Processor to CS length matching (LT)	0.282" ± 0.010" Chipset LT must be 0.282 inch longer than Processor LT	Figure 3-2	10
Processor to processor length matching (LT)	± 10 mils	Figure 3-2	15
HCLKINP – HCLKINN length matching	± 10 mils		
R_S series termination value	33 Ω ± 5%	Figure 3-2	11
R_T shunt termination value	49.9 Ω ± 1% (for 50 Ω MB impedance)	Figure 3-2	12

NOTES:
1. The skew budget includes clock driver output pair to output pair jitter (differential jitter), and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes that clock pairs are routed on multiple routing layers, and are routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two-bus agents. Measured at the crossing point.
5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.

6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing because this will degrade the noise rejection of the network.
7. Set line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack up.
8. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1-2*Kb), where Kb is the backwards crosstalk coefficient. For the recommended trace spacing, Kb is very small and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
9. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the HCLKIN traces vary within the tolerances specified, both traces of a differential pair must vary equally.
10. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the motherboard trace length for the chipset will be longer than that for the processor.
11. Rs values between 20 Ω – 33 Ω have been shown to be effective.
12. R_T shunt termination value should match the motherboard impedance.
13. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination, and contribute to ring back.
14. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in Er and the impedance variations due to physical tolerances of circuit board material.
15. Length of LT for one processor must match the LT of all other HCLKIN traces to other processor within specified tolerance.

Figure 3-3. Length Matching of Host Clocks With Package Compensation



It's important that the host clocks from the clock driver pin to the processor silicon die pad match the length from the clock driver pin to the MCH silicon die pad. Length-matching must consider the difference in processor/chipset package length, and the additional flight time included in the processor BCLK path as the signal travels across the 603-pin or 604-pin socket.

The In-Target Probe clock lengths require a defined relationship to the processor and MCH host clock lengths. For more information on this relationship, refer to the *ITP700 Debug Port Design Guide* for the design of your platform.

Figure 3-4. Clock Skew As Measured from Agent to Agent

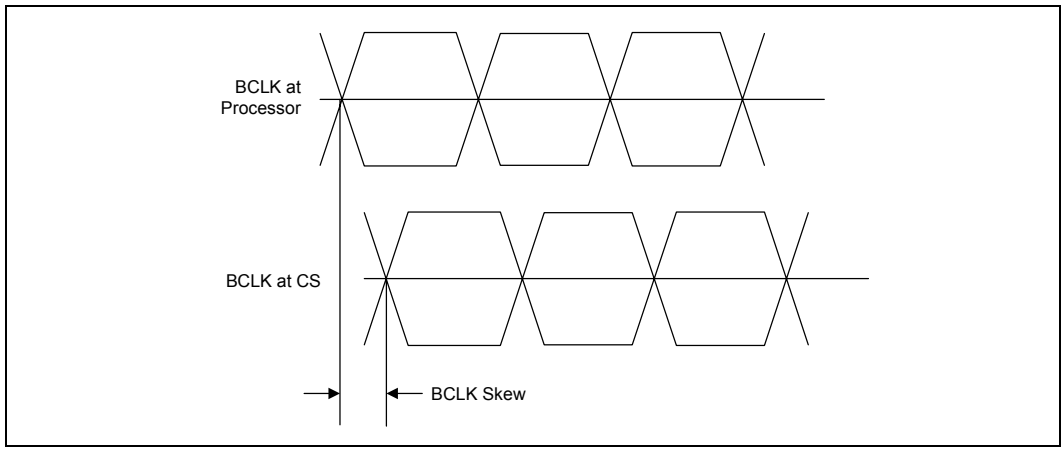
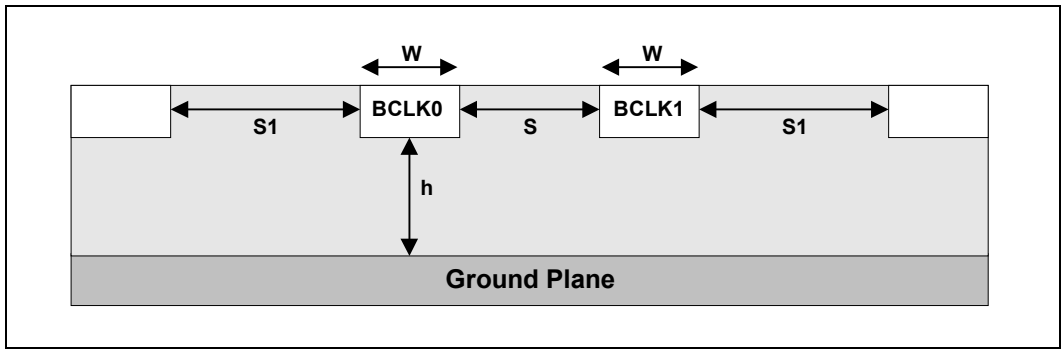


Figure 3-5. Trace Spacing



3.1.1.2 HOST_CLK General Routing Guidelines

- Route differential clock pairs with both halves of the pair on the same layer. Also route each pair to all agents on the same physical routing layer referenced to ground.
- Do not route with any layer changes.
- Do not place vias between adjacent complementary clock traces.
- Avoid differential vias whenever possible. When differential vias are necessary, they must be matched on each trace of the pair.

Note: Differential vias can be placed within length L1, between the clock driver and R_S to shorten length L1.

3.1.2 CLK66 Clock Group

The driver is the clock synthesizer's 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the MCH, ICH4, P64H2, and AGP.

Figure 3-6. Topology for CLK66

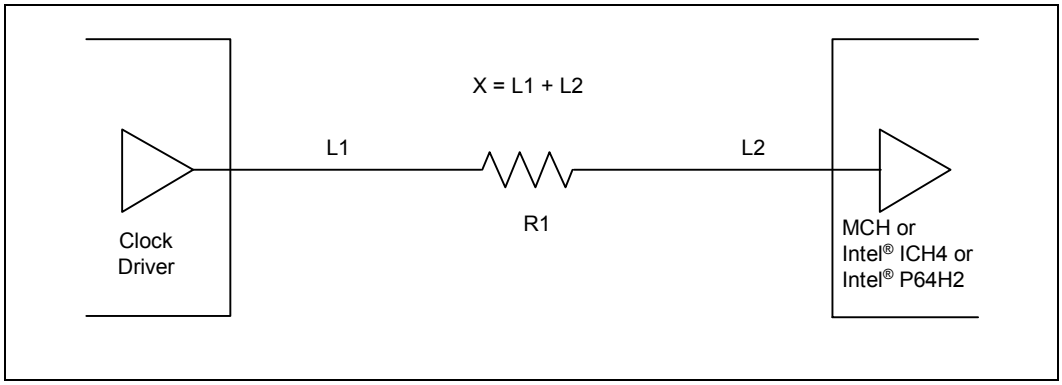


Table 3-4. CLK66 Routing Guidelines

Parameters	Routing Guidelines
Clock Group	CLK66
Topology	Point to Point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	6 mils on external layers and 5 mils on internal layers
Trace Spacing	25 mils
Spacing to Other Traces	25 mils
Trace Length – L1	0.00 inch – 0.50 inch
Trace Length – L2	3.00 inches – 9.00 inches
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	The CLK66 group should minimize skew (~0) between each other.
Clock Driver to MCH	X (X can be between 3 inches– 9.5 inches)
Clock Driver to Intel® ICH4	X
Clock Driver to Intel® P64H2	X
Clock Driver to AGP connector	X– 4.6 inches (4 inches add-in card clock length plus 0.6 inch approximation for connector delay)

3.1.2.1 CLK66 Group to AGP Connector

The driver is the clock synthesizer's 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the AGP device. Use these guidelines when routing to an AGP connector.

Figure 3-7. Topology for CLK66 to AGP Connector

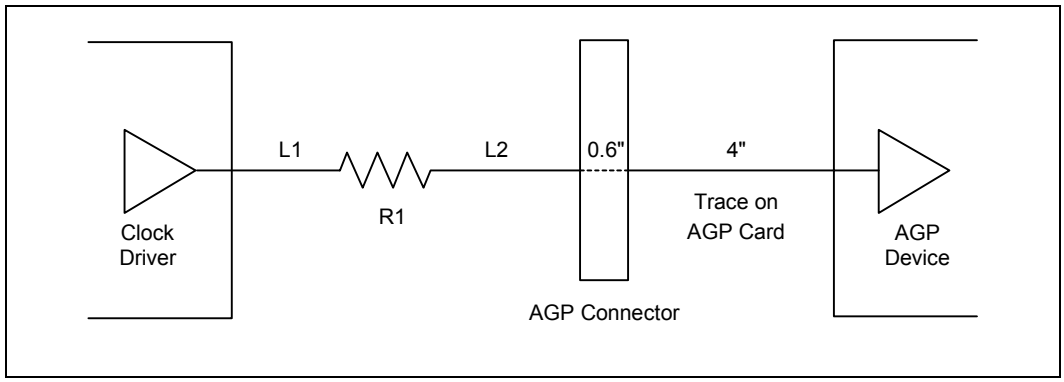


Table 3-5. CLK66 Routing Guidelines (for AGP Connector)

Parameters	Routing Guidelines
Topology	Point to Point
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Spacing to Other Traces	25 mils
Trace Length – L1	0.00 – 0.50 inch
Trace Length – L2	MCH 66 MHz Clock – L1 – 4.6 inches
AGPCLK Total Length (L1+L2)	MCH 66 MHz Clock – 4.6 inches (Must be matched to ± 100 mils of the CLK66 total length)
Resistor	R1 = 33 Ω ± 5%

3.1.2.2 CLK66 Skew Requirements

All 66 MHz clock lengths require length matching. All devices down on the motherboard must have matching clock lengths. The AGP connector is equivalent to approximately 0.6 inches of trace, and the add-in card has 4 inches of clock trace. Therefore, the AGP clock is routed 4.6 inches shorter than the clocks to down devices (See Figure 3-8).

The skew between clocks can be further reduced by including the package lengths internal to the MCH, ICH4, and P64H2 in the length matching equations. This is not a requirement but improves timing margins. Figure 3-9 shows the relationship between the 66 MHz clocks when accounting for internal package lengths.

Figure 3-8. Clock Skew and Tracing Requirements Without Package Compensation

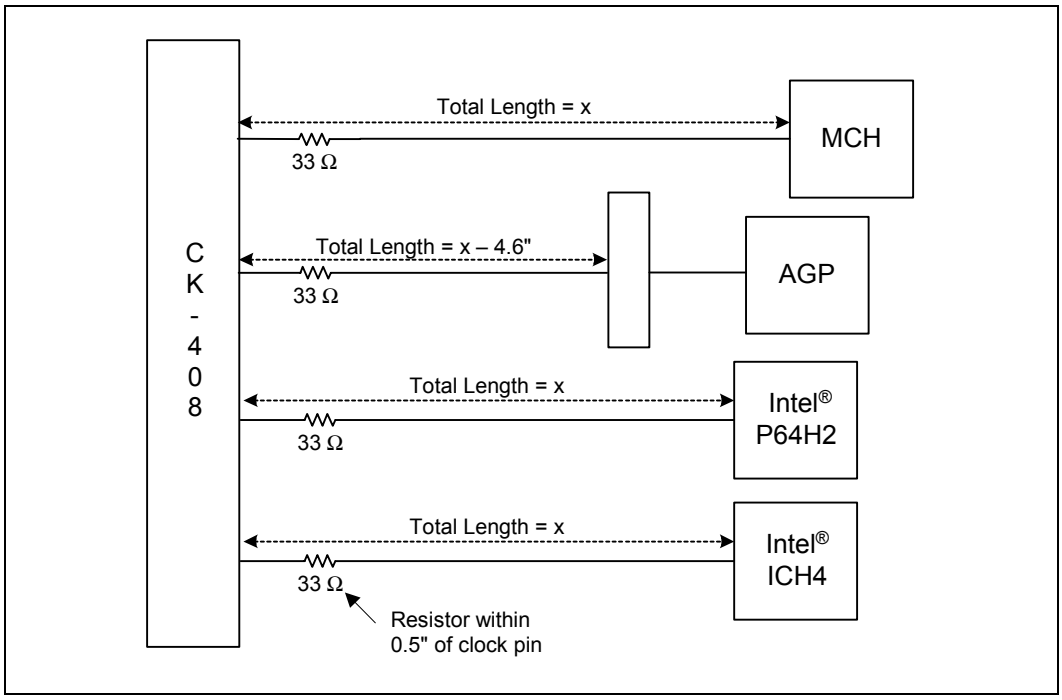
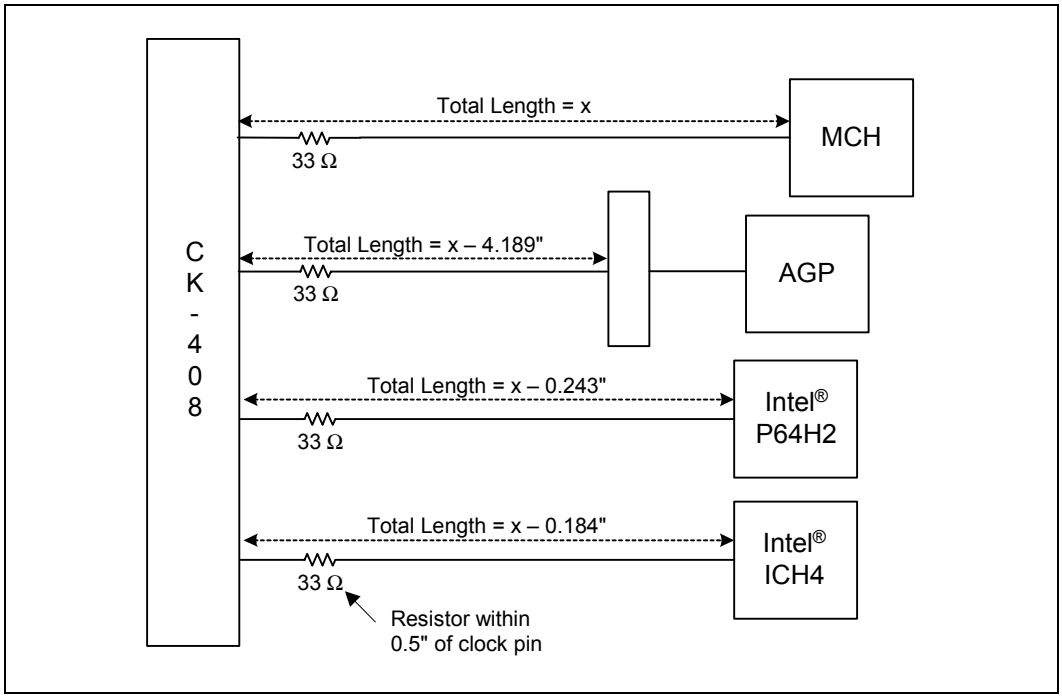


Figure 3-9. Clock Skew and Trace Requirements With Package Compensation



3.1.3 CLK33 Clock Group

The driver is the clock synthesizer's 33 MHz clock output buffer, and the receiver is the 33 MHz clock input buffer at the PCI devices on the PCI cards.

Figure 3-10. Topology for CLK33 to PCI Device Down

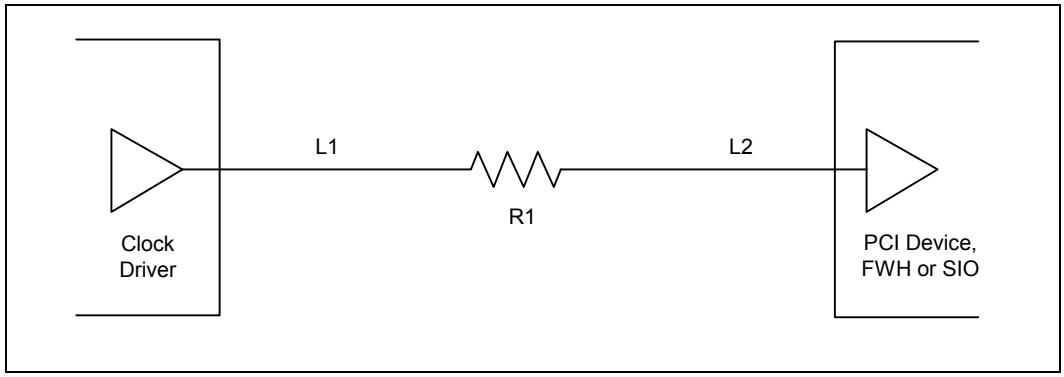


Table 3-6. CLK33 Routing Guidelines (PCI Device Down)

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point-to-Point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 – 0.50 inch
Trace Length – L2	ICH 66 MHz Clock – L1(1)
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	The maximum PCI device to PCI device skew allowed by the PCI Specification is 2 ns. All PCI devices must be within 2 ns of Intel® ICH4 clock. The clock generator spec allows for 500 ps skew; therefore up to ± 1 ns may be used to ease routing.

NOTES:
1. The 66 MHz total clock length must equal the 33 MHz total clock length which is a requirement of the ICH4.
2. The designer must ensure that the total device to device skew on PCI bus does not exceed 2 ns, including clock generator skew.

Figure 3-11. Topology for CLK33 to PCI Connector

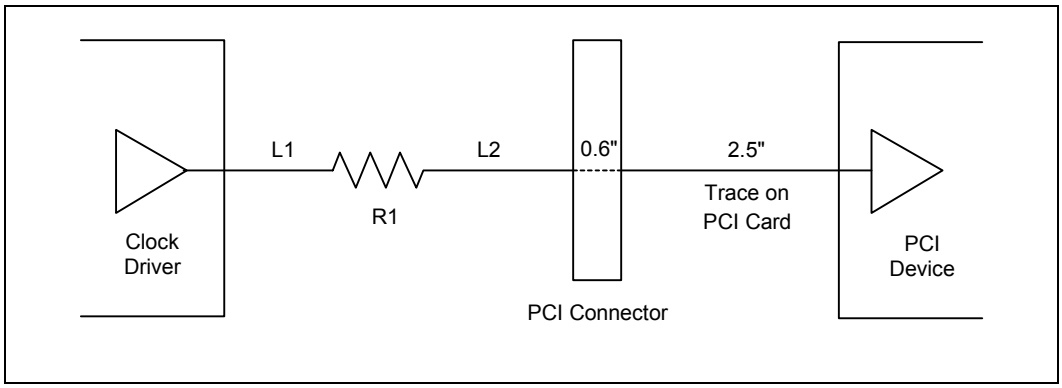


Table 3-7. CLK33 Routing Guidelines for PCI Connector

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point-to-Point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 – 0.50 inch
Trace Length – L2	ICH 66 MHz Clock – L1 – 3.1”
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	The maximum PCI device to PCI device skew allowed by the PCI Spec is 2 ns. All PCI devices must be within 2 ns of Intel® ICH4 clock. The clock generator spec allows for 500 ps skew; therefore up to ±1 ns may be used to ease routing.

3.1.3.1 CLK33 Skew Requirements

All 33 MHz clocks to PCI devices must match in length. In addition, the traces that route the 33 MHz clock to the ICH4 must match the length of those traces that route the 66 MHz clock to the ICH4. The PCI connector is equivalent to approximately 0.6 inches of trace, and the add-in card has 2.5 inches of trace. Therefore, to ensure that the trace length between the clock chip and all PCI devices is equal, the total trace length from the clock to PCI slot must be 3.1 inches shorter than the total trace length from the clocks to down devices.

The skew between clocks can be further improved by including the package lengths internal to the MCH, ICH4, and P64H2. This is not a requirement, but improves timing margins. Figure 3-13 shows the relationship between the 33 MHz clocks when accounting for internal package lengths.

Figure 3-12. Clock Skew and Tracing Requirements Without Package Compensation

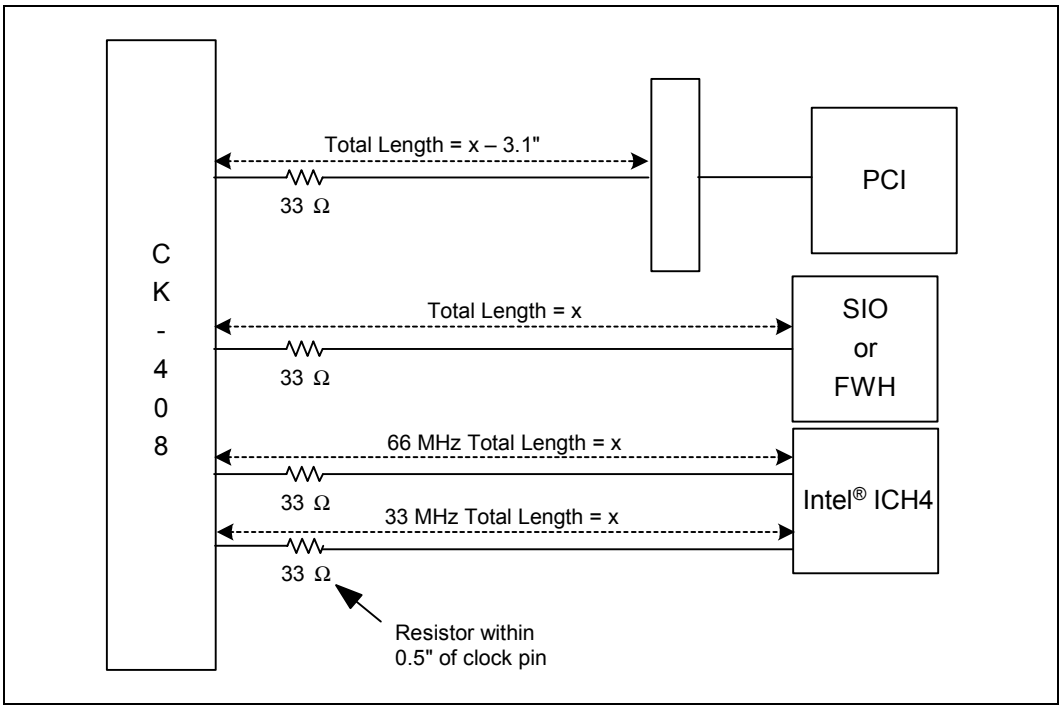
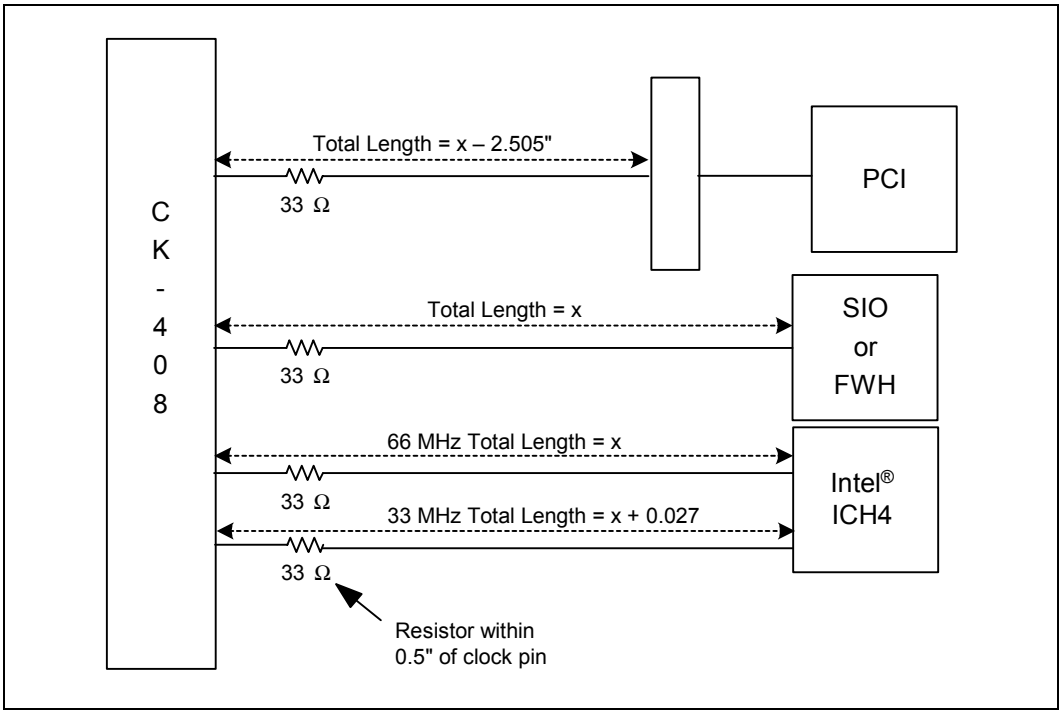


Figure 3-13. Clock Skew and Trace Requirements With Package Compensation



3.1.4 CLK14 Clock Group

The driver is the clock synthesizer's 14.318 MHz clock output buffer, and the receiver is the 14.318 MHz clock input buffer at the ICH4 and SIO.

Figure 3-14. Topology for CLK14

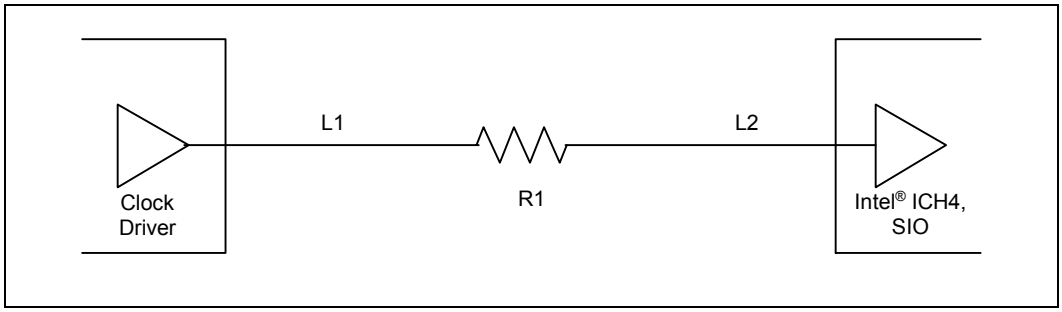


Table 3-8. CLK14 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK14
Topology	Point-to-Point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 – 0.50"
Trace Length – L2	3.00 – 9.00"
Resistor	R1 = 33Ω ± 5%
Skew Requirements	Should have minimal skew (~ 0) between each other. However, each of the clocks in this group is asynchronous to clocks of any other group.

3.1.5 USBCLK Clock Group

The driver is the clock synthesizer's USB clock output buffer, and the receiver is the USB clock input buffer at the ICH4.

Figure 3-15. Topology for USB_CLK

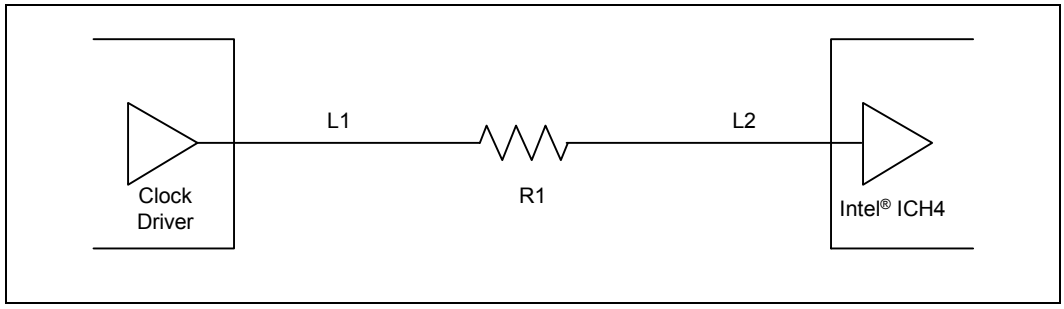


Table 3-9. USBCLK Routing Guidelines

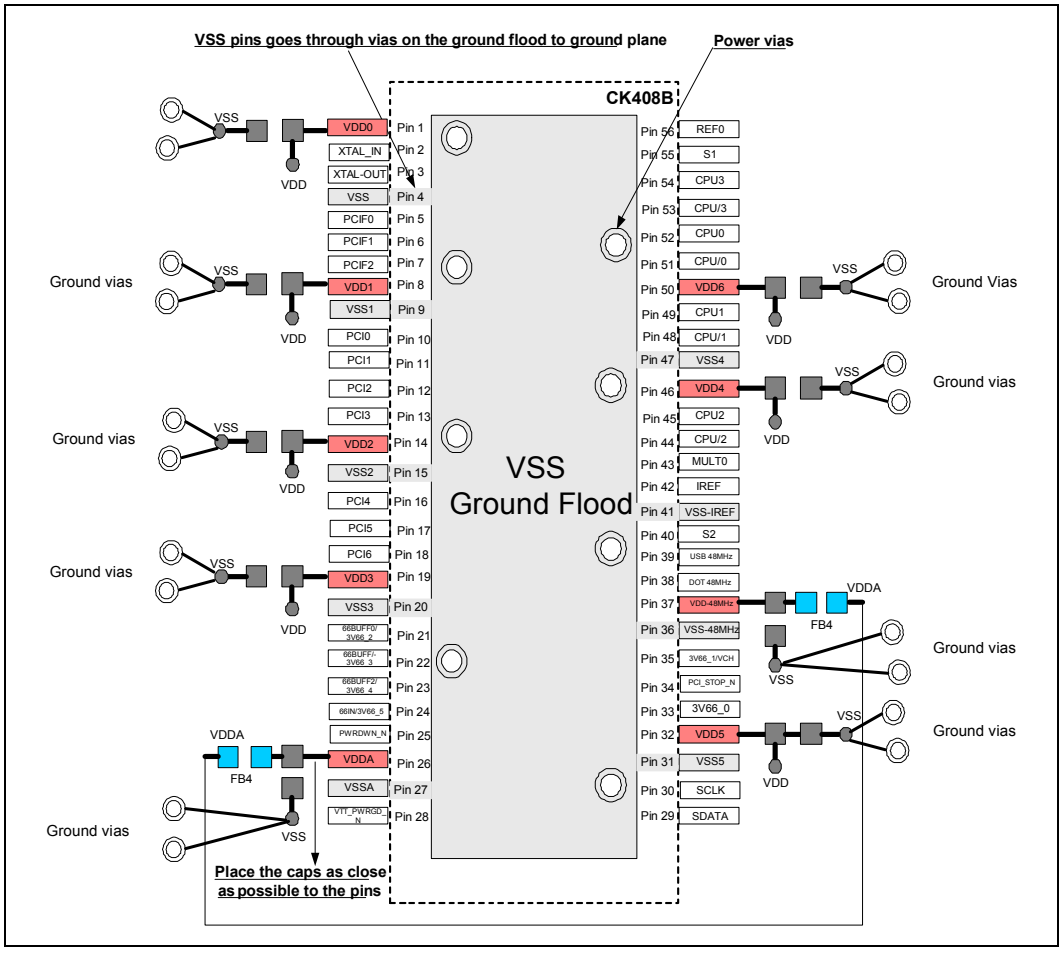
Parameter	Routing Guidelines
Clock Group	USBCLK
Topology	Point-to-Point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 inch – 0.50 inch
Trace Length – L2	3.00 inches – 12.00 inches
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	None – USBCLK is asynchronous to any other clock on the board.
Maximum Via Count per Signal	2

3.2 Clock Driver Decoupling

The decoupling requirements for a CK408 compliant clock synthesizer are as follows:

- One 22 µF polarized (decoupling) cap placed close to the V_{DD} generation circuitry.
- Eleven 0.1 µF high-frequency decoupling caps placed close to the V_{DD} pins on the Clock driver.
- Three 0.1 µF high-frequency decoupling caps placed close to the V_{DDA} pins on the Clock driver.
- One 10 µF polarized (decoupling) cap placed close to the V_{DDA} pins on the Clock driver.
- One 0.1 µF high-frequency decoupling cap placed close to the V_{DDA} generation circuitry.
- All decoupling caps should be placed close to the Clock driver pins. Refer to Figure 3-16.

Figure 3-16. Decoupling Capacitors Placement and Connectivity



3.3 Clock Driver Power Delivery

Special care must be taken to provide a quiet V_{DDA} supply to the Ref V_{DD}, V_{DDA}, and the 48 MHz V_{DD}. These V_{DDA} signals are especially sensitive to switching noise induced by the other V_{DD}s on the clock chip. They are also sensitive to switching noise generated elsewhere in the system, such as CPU VRM. It is recommended that a ground flood be placed directly under the clock chip to provide a low impedance connection for the VSS pins. In addition, power vias should be distributed evenly throughout the ground flood.

Note: For all power connections to planes, decoupling caps, and vias, the maximum trace width allowable and shortest possible lengths should be used to ensure the lowest possible inductance.

3.4 EMI Constraints

Clocks are a significant contributor to EMI. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to a VSS reference plane only.

Baseboard Requirements 4

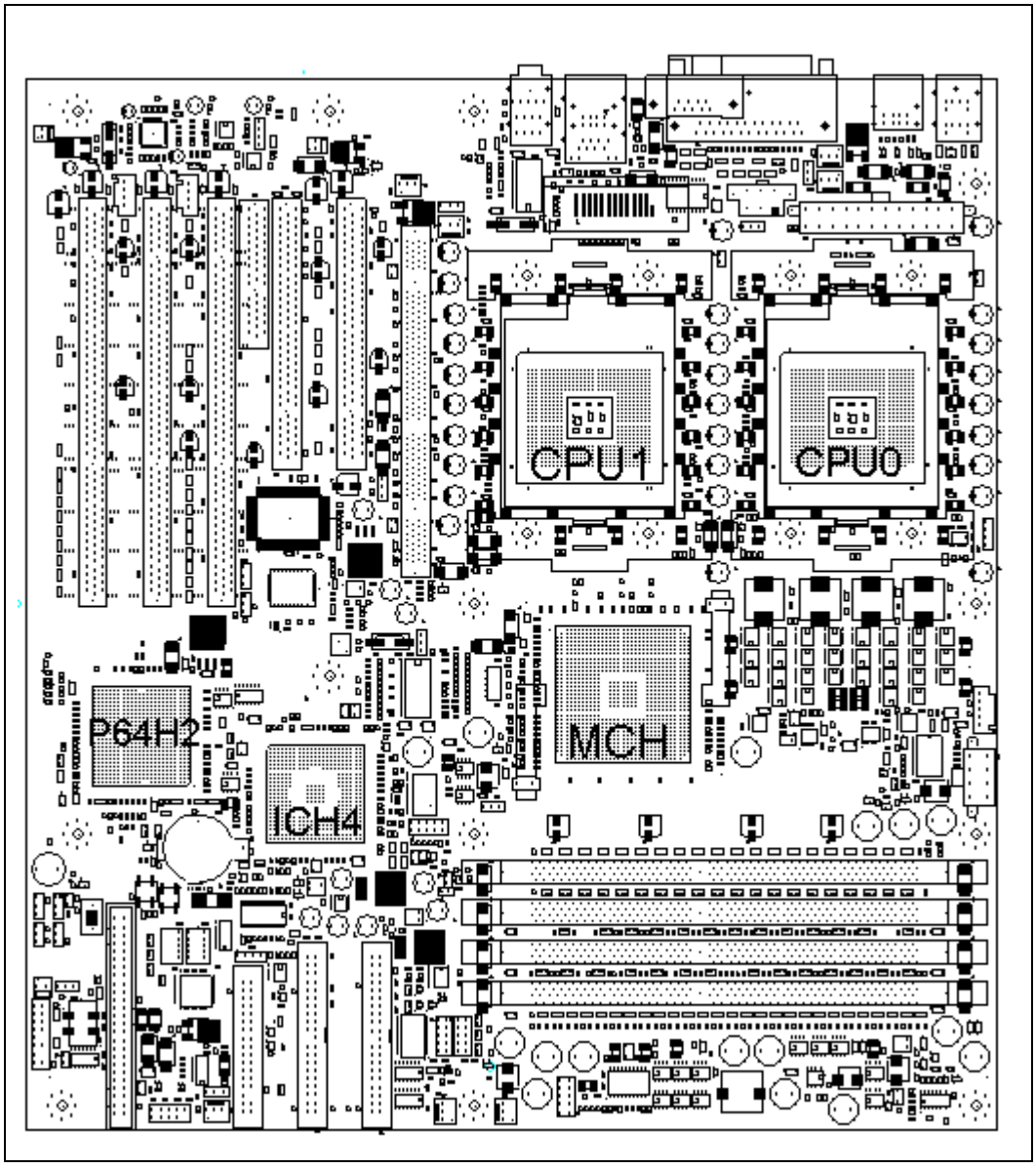
4.1 Platform Component Placement

Figure 4-1 illustrates the general component placement for the processor / chipset-based customer reference platform. Table 4-1 lists the assumptions used for the component placement. Refer to www.ssiforum.org for detailed information on the SSI specification.

Table 4-1. Assumptions for System Placement Example

System Configuration	Assumptions		
	SSI-EEB (12” X 13”)	Number of PCB Layers	Assembly
Workstation (DP)	Midrange SSI (13”x16”)	8 Layers	Single/Double Sided

Figure 4-1. Intel® Xeon™ Processor with 512-KB L2 Cache and Intel® Xeon™ Processor with 533 MHz System Bus / Intel® E7505 Chipset-Based System Placement Example



4.2 Platform Stack-Up

Figure 4-2 shows the recommended platform stack-up. All layers are 1 oz. copper. The processor requires at least 2 oz. of copper to deliver power, and at least 2 oz. of copper to deliver ground. Vias are 14-mil. finished hole with 39-mil anti-pads and 25-mil pads.

Route signals layers as asymmetric stripline on layers 3 and 6. The system bus 4X and 2X group signals should be routed on layers 3 and 6 only with 50 Ω ±10%. Refer to Section 6.1 for DDR routing recommendations, and Chapter 7 for Hub Interface routing recommendations. All signal layers should reference ground for the entire length of the signal path.

Intel strongly recommends that system designers use the stack-up shown in Figure 4-2. Intel encourages platform designers to perform comprehensive simulation analysis to ensure that all timing specifications will be met. This is particularly important if a design deviates from the design guidelines provided.

Figure 4-2. 8 Layer, 50 Ω Board with 5-mil Traces

Layer Number	Plane Description	Layer Thickness (mil)	Copper Weight (Oz)	Impedance (Width/Spacing)
LAYER 1	**SIGNAL**	2.1	1.5 (plated)	60Ω (4.25/15)
	prepreg	3.8		
LAYER 2	**GND**	1.4	1	
	CORE	5.2		
LAYER 3	**SIGNAL**	1.4	1	55Ω (4/15), 50Ω (5/15), 45Ω (6/15)
	prepreg	10.5		
LAYER 4	**POWER**	2.8	2	
	CORE	7.6		
LAYER 5	**POWER**	2.8	2	
	prepreg	10.5		
LAYER 6	**SIGNAL**	1.4	1	55Ω (4/15), 50Ω (5/15), 45Ω (6/15)
	CORE	5.2		
LAYER 7	**GND**	1.4	1	
	prepreg	3.8		
LAYER 8	**SIGNAL**	2.1	1.5 (plated)	60Ω (4.25/15)

Panel Thickness (mil) : 62.0 (Note: Assumes finished thickness on Microstrip layers)

Dielectric Constant (Er) : 4.3 (Note: Frequency range: 100Mhz - 533Mhz)

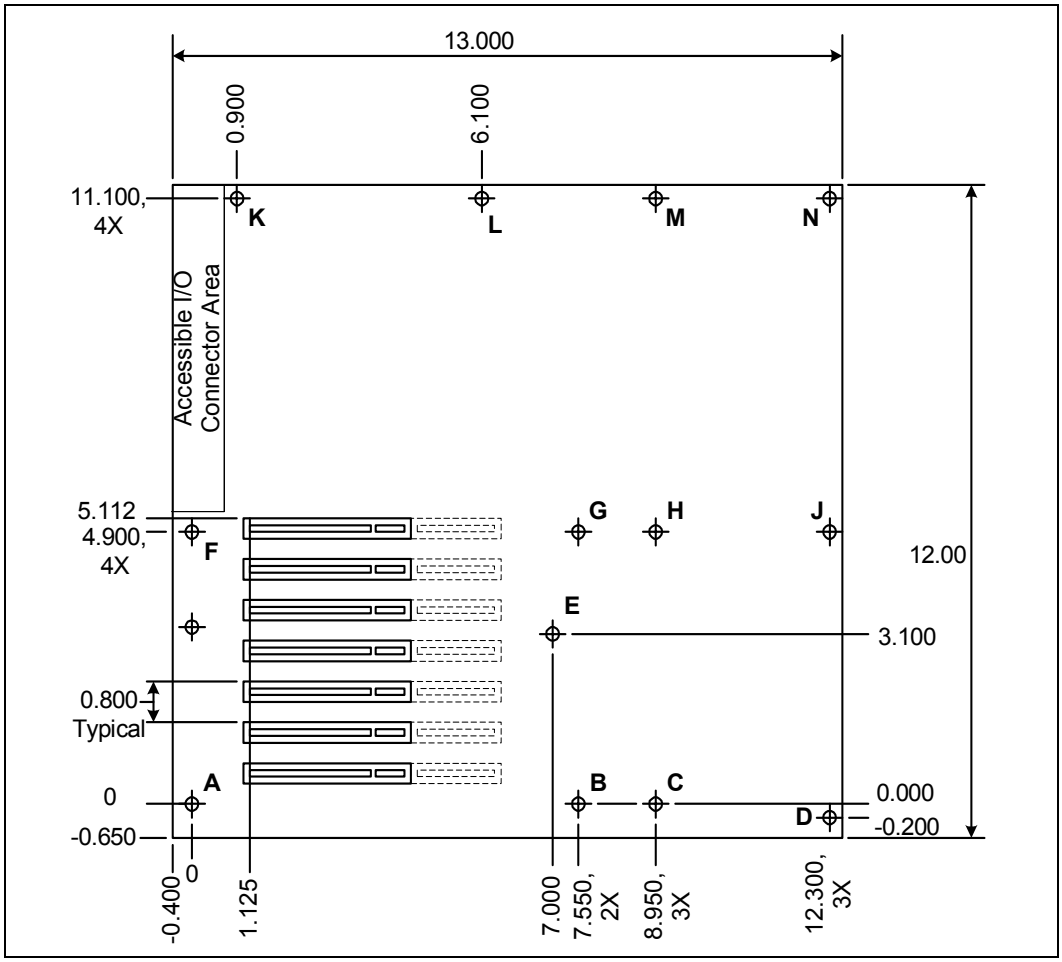
4.3 SSI Compliance

If your motherboard is intended to meet Server System Infrastructure (SSI) Specifications, it must meet a minimum set of requirements. All requirements from the *Entry-level Electronics-Bay Specification: A Server System Infrastructure (SSI) Specification for Entry Server Version 3.0* (SSI EEB) are highlighted here. Where anything conflicts with the SSI specification, the SSI specification supercedes this document.

4.3.1 Mounting Hole Placement

The SSI Specification requires that every SSI compliant chassis provides a mounting hole at each of the locations enumerated in Figure 4-3.

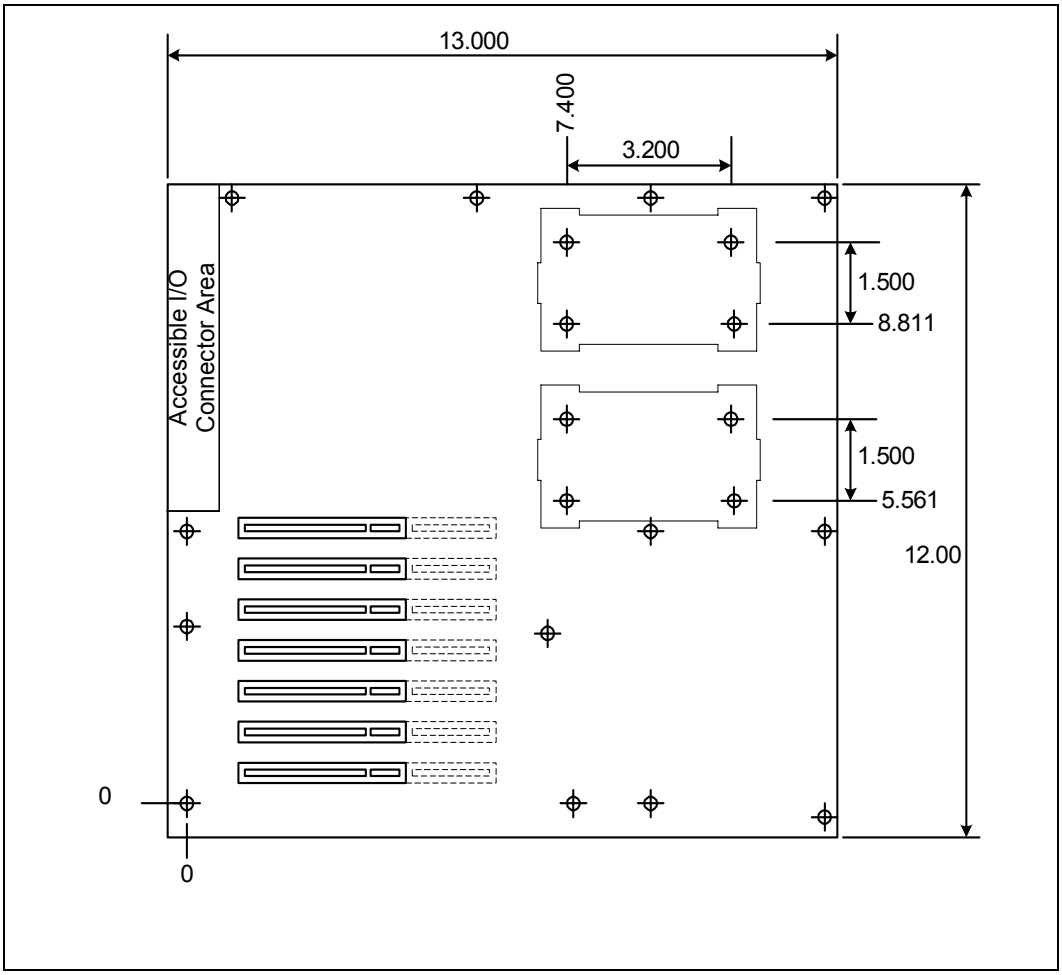
Figure 4-3. Available Baseboard Mounting Holes supported by the Chassis



NOTE: This figure is a copy of the SSI EEB Specification, Version 3.0, Figure 1: Available Baseboard Mounting Holes Supported by the Chassis. All dimensions are in inches.

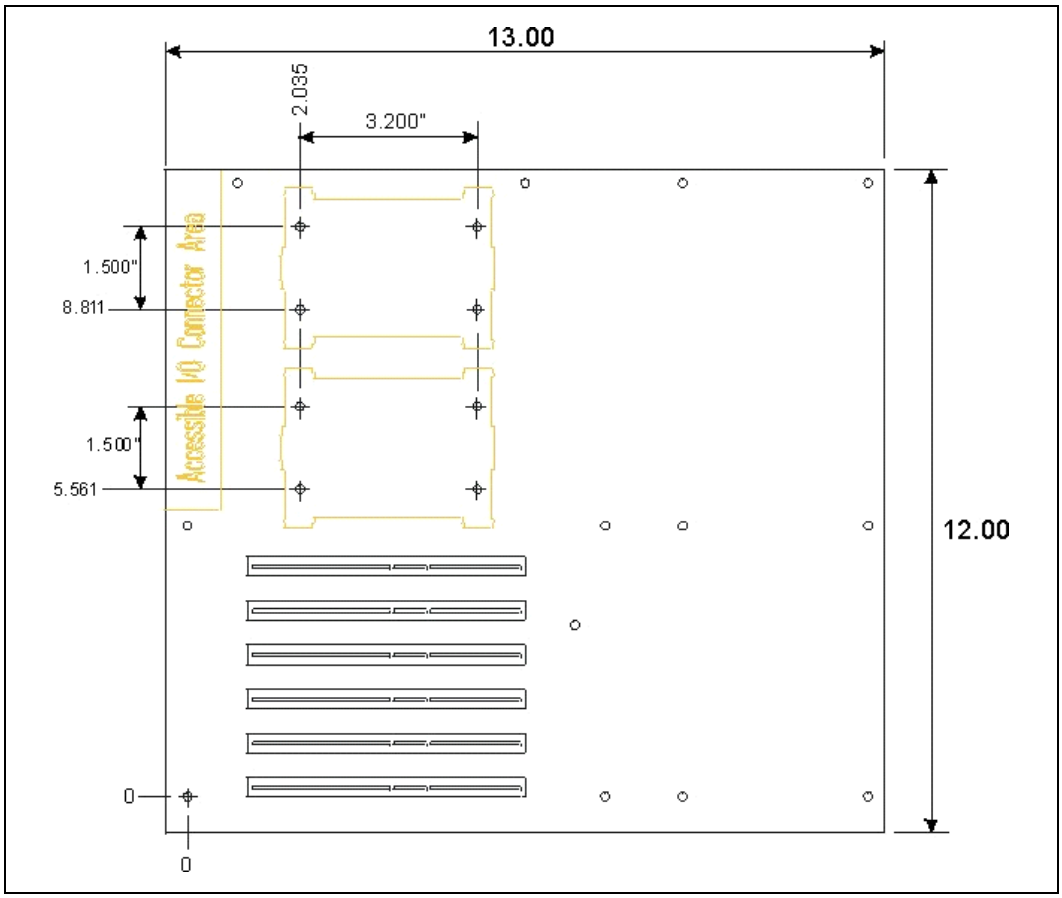
The SSI EEB specification enumerates various processor mounting locations. A board based on the Intel Xeon Processor with E7505 chipset must use the hole locations as specified in Figure 4-4 (SSI EEB Section 7.1, Figure 18). The baseboard manufacturer must work closely with the chassis manufacturer to ensure these holes are available. Figure 4-5 enumerates all holes used by the reference design.

Figure 4-4. Available Baseboard Mounting Holes supported by the Chassis for the Processor



NOTE: This figure is a copy of the SSI EEB Specification, Version 3.0, Figure 18: Mouting Hole Option for Next Generation Intel® Xeon™ Processor Baseboards. All dimensions are in inches.

Figure 4-5. Baseboard Mounting Holes Used by E7505 Chipset Reference Board



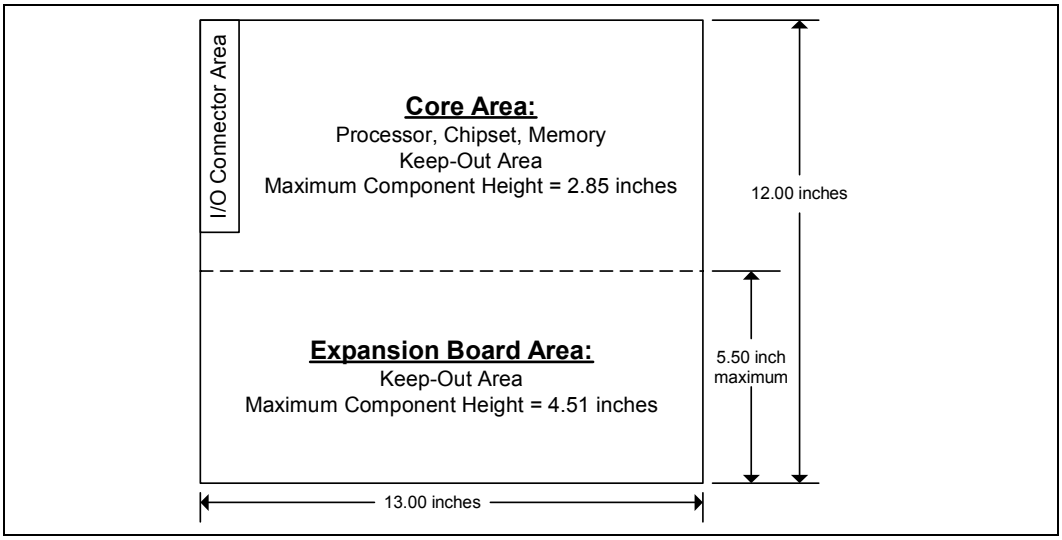
NOTE: All dimensions are in inches.

4.3.2 Volume Constraints for Typical General Purpose Baseboards

Figure 4-6 and Figure 4-7 show the minimum outer dimensions of the Electronics Bay and the height above the baseboard that must remain clear of chassis features. The keep-out height of the core area (processor, chipset, memory) is defined for Workstations. These are the volumetric constraints to which the reference board is designed. To ensure the mainboard will fit within your chassis, the baseboard must fall within these constraints.

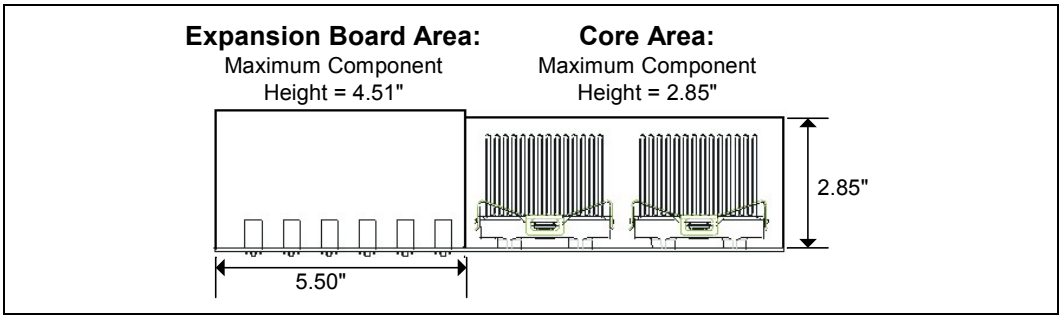
This core area keep-out zone differs from the ATX specification. Overhanging peripherals (e.g., CD-ROM drives, floppy disk drives, and hard disk drives) and chassis features must not intrude into any portion of the keep out area.

Figure 4-6. Typical Baseboard Maximum Height Restrictions



NOTE: This figure is a copy of the SSI EEB Specification version 3.0 Figure 2: Typical Baseboard Maximum Height Restrictions.

Figure 4-7. EEB Case-2: 2-Dimensional End View of a Low Profile / High-Density Server Application

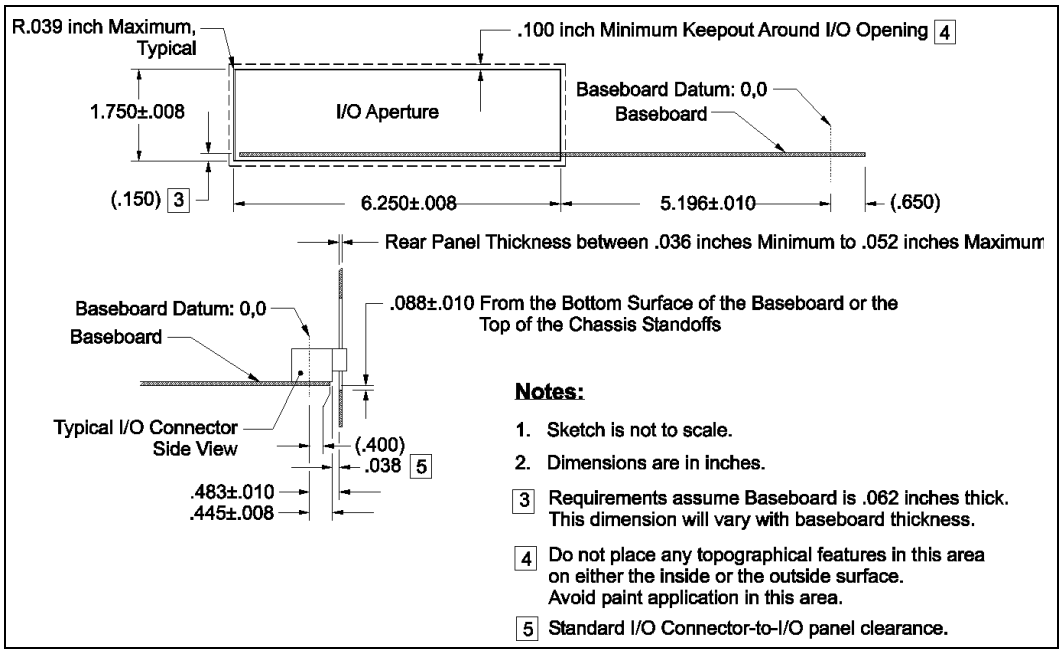


NOTE: This figure is a copy of the SSI EEB Specification version 3.0 Figure 6: EEB Case-1: 2-Dimensional End View of a General Purpose Server 3U or Greater.

4.3.3 Standard Cutout for Onboard I/O Ports

The Entry Electronics-Bay Specification includes the I/O aperture of the ATX 2.03 specification and uses the same dimensions. Because the same dimensions are used, a baseboard manufacturer can create just one thin metal shield for the rear I/O connectors, a shield that works in any chassis that meets this specification. This chassis-independent shield closes the Electronics-Bay, except for small openings that allow access to board-mounted connectors such as, but not limited to, network, serial, parallel, video, and mouse/keyboard. The shield provides the chassis shielding and connector grounding that a system requires to meet emissions and susceptibility regulations. Figure 4-8 shows the Electronics-Bay aperture.

Figure 4-8. Standard I/O Cutout



NOTE: This figure is a copy of the SSI EEB Specification, version 3.0, Figure 6: Standard I/O Cutout.

4.3.4 Connectors

The SSI Spec requires that your baseboard have the following connectors: Main Power Connector, +12 Volt Power Connector, Auxillary Signal Connector, and cooling fan connectors. All of this information is in the SSI Specification, but is presented here for convenience.

4.3.4.1 Entry SSI Main Power Connector

The baseboard must have a 24-pin Molex 44472 family connector or equivalent. The header must have the pin-out as enumerated in Table 4-2. The PWR OK signal has strict electrical requirements, as documented in the SSI EEB Specification, version 3.0, Section 5.3.1.5 (Power OK).

Table 4-2. Entry SSI Main Power Connector Pin-out

Pin	Signal	Pin	Signal
1	+3.3 VDC	13	+3.3 VDC
2	+3.3 VDC	14	-12 VDC
3	COM	15	COM
4	+5 VDC	16	PS ON
5	COM	17	COM
6	+5 VDC	18	COM
7	COM	19	COM
8	PWR OK	20	Res
9	5 VSB	21	+5 VDC
10	+12V2 VDC	22	+5 VDC
11	+12V2 VDC	23	+5 VDC
12	+3.3 VDC	24	COM

NOTE: This table is a copy of the SSI EEB Specification, Version 3.0, Table 3: Entry SSI Main Power Connector Layout.

4.3.4.2 +12 Volt Power Connector

The baseboard must have an 8-pin Molex 44472 family connector or equivalent. The header must have the pin-out as enumerated in Table 4-3. The SSI Specification dictates that the +12V3 rail on the motherboard must be separate from the +12V2 rail.

Table 4-3. Entry SSI +12 Volt Power Connector Pin-out

Pin	Signal	Pin	Signal
1	COM	5	+12V3 VDC
2	COM	6	+12V3 VDC
3	COM	7	+12V3 VDC
4	COM	8	+12V3 VDC

NOTE: This table is a copy of the SSI EEB Specification, Version 3.0, Table 4: Electronics-Bay +12 Volt Power Connector Layout.

4.3.4.3 Auxiliary Signal Connector

The baseboard must have a 5-pin Molex 70545 family connector or equivalent. The header must have the pin-out as enumerated in Table 4-4. The PS Alert signal has strict electrical requirements, as documented in the SSI EEB Specification, version 3.0, Section 5.3.1.6 (PS Alert).

Table 4-4. Entry Auxiliary Signal Connector Pin-out

Pin	Signal
1	SMBus Clock
2	SMBus Data
3	PS Alert
4	ReturnS
5	3.3 RS

NOTE: This table is a copy of the SSI EEB Specification, Version 3.0, Table 5: Electronics-Bay Server Signal Connector.

4.3.4.4 Cooling Fan Connector

The baseboard must have a 3-pin AMP 644953-3 connector or equivalent. The header must have the pin-out as enumerated in Table 4-5.

Table 4-5. Cooling Fan Pin-out

Pin	Wire Color	Signal
1	Black	COM
2	Red	Fan-V
3	Yellow	TACH

NOTE: This table is a copy of the SSI EEB Specification, version 3.0, Table 11: Cooling Fan Pinout.

System Bus Routing Guidelines 5

This chapter describes the recommended system bus source synchronous, common clock, and asynchronous GTL+ signal routing for dual-processor/E7505 chipset systems. Table 5-1 lists the signals and their signal types. The signals listed are processor signal names. For the MCH, the corresponding signal name may be slightly different. For example, the address signals A[35:3] on the processor are called HA[35:3] on the MCH.

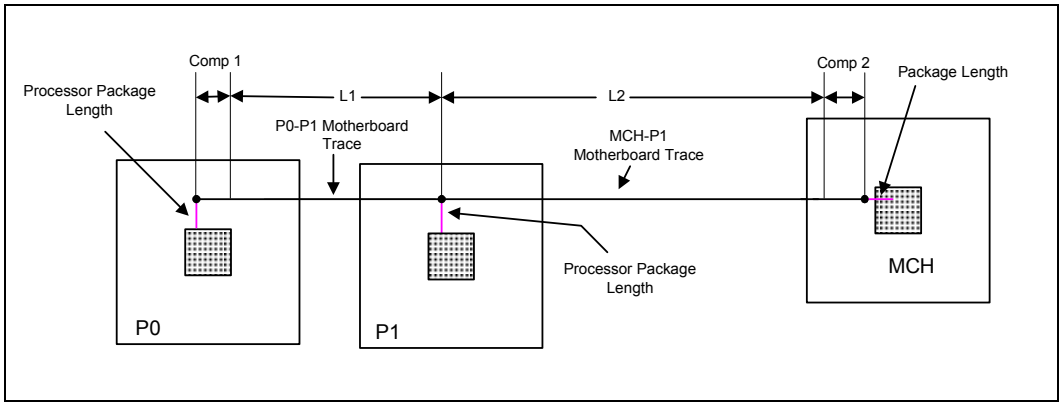
Table 5-1. System Bus Signal Groups

Signal Group	Type	Signals
AGTL+ Common Clock Input	Synchronous to HCLKIN	BPRI#, BR[3:1]#[1,2], DEFER#, RESET#[1,6], RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to HCLKIN	ADS#, AP[1:0]#, BINIT#[3], BNR#[3], BPM[5:0]#[1,6], BR0#[1], DBSY#, DP[3:0]#, DRDY#, HIT#[3], HITM#[3], LOCK#, MCERR#[3]
AGTL+ Source Synchronous I/O: 4X Group	Synchronous to assoc. strobe	D[63:0]#, DBI[3:0]#
AGTL+ Source Synchronous I/O: 2X Group	Synchronous to assoc. strobe	A[35:3]#[4], REQ[4:0]#
AGTL+ Strobes	Synchronous to HCLKINP/ HCLKINN	ADSTB[1:0]#, DSTBN[3:0]#, DSTBP[3:0]#
AGTL+ Input[1]	Asynchronous	A20M#, IGNNE#, INIT#[4], LINT0/INTR, LINT1/ NMI, SMI#[4], SLP#, STPCLK#
AGTL+ Output[1]	Asynchronous	FERR#, IERR#, THERMTRIP#, PROCHOT#
System Bus Clock	Clock	HCLKINP, HCLKINN
TAP Input[1]	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output[1]	Synchronous to TCK	TDO
SMBus Interface[1]	Synchronous to SM_CLK	SM_EP_A[2:0], SM_TS_A[1:0], SM_DAT, SM_CLK, SM_ALERT#, SM_WP
Power/Other	Power/Other	GTLREF[3:0], BSEL[1:0], COMP[1:0], XSWING/YSWING, OTDEN, PWRGOOD, RESERVED, SKTOCC#, SMB_PRT[7], TESTHI[6:0], THERMDA[7], THERMDC[7], VID[4:0], VCC_CPU, SM_VCC[5], VID_VCC[7], VCCA, VSSA, VCCIOPLL, VSS, VCC_SENSE, VSS_SENSE

NOTES:
1. These signals do not have on-die termination on the processor. They must be terminated properly on the motherboard. If the signal is not connected, it must be pulled to the appropriate voltage level through a 1 kΩ resistor.
2. Intel Xeon processors with 512-KB L2 cache use only BR0# and BR1#. BR2# and BR3# are not driven by the processor but must be terminated to VCC. See Section 5.2.1 for details.
3. These signals are 'wired-OR' signals and may be driven simultaneously by multiple agents.
4. The value of these pins driving the active edge of RESET# determine processor configuration options.
5. SM_VCC has critical power sequencing requirements. Refer to the *Intel® Xeon Processor with 512-KB L2 Cache Datasheet* for further details.
6. Critical terminations and routing for RESET#, BPM[5:0], and TAP signals are found in the *ITP700 Debug Port Design Guide*.
7. These signals are defined and driven only by the FC-mPGA2 package processor.

The dual-processor topology requires that the MCH be at one end of the bus, Processor 0 be at the other end of the bus, and Processor 1 be in the middle of the bus as shown in Figure 5-1. The motherboard routing to Processor 1 must not create a stub on the system bus signals at the socket. This requires routing into the socket and back out of the socket. For UP operation, the single processor must be installed in the Processor 0 socket, at the end of the bus. Figure 5-1 shows the recommended dual-processor topology used for system bus routing.

Figure 5-1. Dual-Processor System Bus Topology



Refer to Table 5-2 for a summary of the dual-processor system bus routing recommendations. The following sections provide additional information for each signal group. Intel strongly recommends simulation of all signals to ensure that setup and hold times are met.

Table 5-2. System Bus Routing Summary

Parameter	Platform Routing Guidelines
Trace width/spacing	5/15 mils Serpentine ratio of 5:1.
2X and 4X Signal Group (agent to agent length)	Processor to Processor (L1) = 3.0 – 7.0 inches. MCH to Processor (L2) = 3.0 – 6.5 inches. Total bus length must not exceed 13.5 inches. All 2X and 4X signals of the same group (Refer to Table 5-3) must be routed within ± 25 mils between agents. Route all signals within the same strobe group on the same layer for the entire length of bus. Never change layers on 2X and 4X signals. Never route over a plane split.
DSTBN[3:0]#, DSTBP[3:0]#, and ADSTB[1:0]#	Follow the same routing rules as the 2X and 4X Signal Group. Maintain a 25-mil spacing around each strobe signal.
Common Clock, Asynchronous GTL+ and Other Signals	Follow the same routing rules as the 2X and 4X Signal Group. However, no length compensation is necessary. If a layer change must occur, use vias connecting the two reference planes to provide a low impedance path for the return current. Vias should be as close as possible to the signal via.
Topology	Daisy chain with the chipset at one end of the system bus, and Processor 0 at the other. End processor must have on-die termination enabled.
Routing requirements	No motherboard contribution to stub length of middle processor (35-mil max trace via to pad). All system bus signals must be stripline, ground referenced only. Use the recommended asymmetric stripline stack-up detailed in Section 4.2. Ensure the signal layers are 2X closer to the ground reference plane than the VCC_CPU plane.
Motherboard Impedance	50 Ω ± 10%

5.1 Routing Guidelines for the 2X and 4X Groups

The 4X group of signals uses four times the frequency of the base clock, or 533 MHz. The 2X group uses twice the frequency of the base clock, or 266 MHz. The 2X and 4X signals are listed in Table 5-3. Table 5-4 lists the 2X and 4X signals with their associated strobes

Table 5-3. 2X and 4X Signal Groups

2X Group	4X Group
A[35:3]# REQ[4:0]#	D[63:0]# DBI[3:0]#

Table 5-4. Source Synchronous Signals with the Associated Strobes

Signal Group	Signals	Associated Strobe
Address Group 0	REQ[4:0]#, A[16:3]#	ADSTB0#
Address Group 1	A[35:17]#	ADSTB1#
Data Group 0	D[15:0]#, DBI0#	DSTBP0#, DSTBN0#
Data Group 1	D[31:16]#, DBI1#	DSTBP1#, DSTBN1#
Data Group 2	D[47:32]#, DBI2#	DSTBP2#, DSTBN2#
Data Group 3	D[63:48]#, DBI3#	DSTBP3#, DSTBN3#

Routing guidelines are specified in Table 5-2.

Trace length matching is required within each source synchronous group to compensate for the package trace length differences between signals. This balances the strobe-to-signal skew in the middle of the setup and hold window. Additional compensation must be added to account for the capacitive loading effects of the processor socket stubs.

Each trace length is determined based on a base length (L1 or L2) and a compensation (L1 Comp and L2 Comp). The base length must be determined based on the layout constraints of the individual design. The compensation lengths are based only on the processor and MCH package lengths.

The following formulas are used to determine the compensation values:

- Compensation due to P0:

  P0 Comp = (Processor Reference Package Length – Processor “Current Net” Package Length)

- Compensation due to P1:

  P1 Comp = 0.78 * (Processor Reference Package Length – Processor “Current Net” Package Length)

- Compensation due to MCH:

  MCH Comp = (MCH Reference Package Length – MCH Current Package Length)

- Total Compensation for each trace:

  L1 Comp = P1 Comp + P0 Comp
  L2 Comp = P1 Comp + MCH Comp

- Length to route:

  P0 to P1 = L1 + L1 Comp
  MCH to P1 = L2 + L2 Comp

Note: “Current Net” refers to the signal for which compensation is being determined.

The reference signal can by any signal in the group. This signal will usually be either the strobe or the signal with the longest package length in the group. When a package length other than the longest is used, the formulas yield negative values. These negative values result in a routed length on the motherboard less than the value of L1 or L2.

P1 Comp is derived based on simulation results. The factor of 0.78 has been determined to yield results that work for most board designs. Intel recommends simulations based on each design to determine if setup and hold times are met.

Example 5-1. Signal Length Matching using Formulas and Package Lengths

For one motherboard design, at least 6400 mils are required for L1 and 4500 mils are required for L2 for Address Group 0. Using the longest package lengths as the reference signal, for signal HADSTB0#:

P0 Comp = 521 – 98 = 423 mils
P1 Comp = 0.78 (521 - 98) = 330 mils
MCH Comp = 938 – 789 = 149 mils
L1 Comp = 330 + 423 = 753 mils
L2 Comp = 330 + 150 = 480 mils
P0 to P1 = 6400 + 753 = 7153 mils
MCH to P1 = 4500 + 480 = 4980 mils

These trace lengths must be routed to within 25 mils to yield ranges of 7128 mils to 7178 mils for the first length, and 4955 mils to 5005 mils for the second length.

5.2 Routing Guidelines for Common Clock Signals

Table 5-5 lists the Common Clock signals.

Table 5-5. AGTL+ Common Clock Signals

Signal Type	Signals
Input	BPRI#, BR[3:1]#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
I/O	ADS#, AP[1:0]#, BINIT#, BNR#, BR0#, DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#

Route the source synchronous signals according to the processor system bus topology shown in Figure 5-1. Routing guidelines for the source synchronous signal group are given in Table 5-2. Common Clock signals may change layers.

5.2.1 BR[3:0]# Routing Guidelines

Because the processor does not contain on-die termination for the BR[3:0]# signals, connect these signals as shown in Figure 5-2 and using the guidelines provided in Table 5-6. The processor only utilizes BR0# and BR1#. BR2# and BR3# are not driven by the processor, but must be terminated to VCC to keep the signals from floating low.

Figure 5-2. BR[1:0]# Routing Guidelines

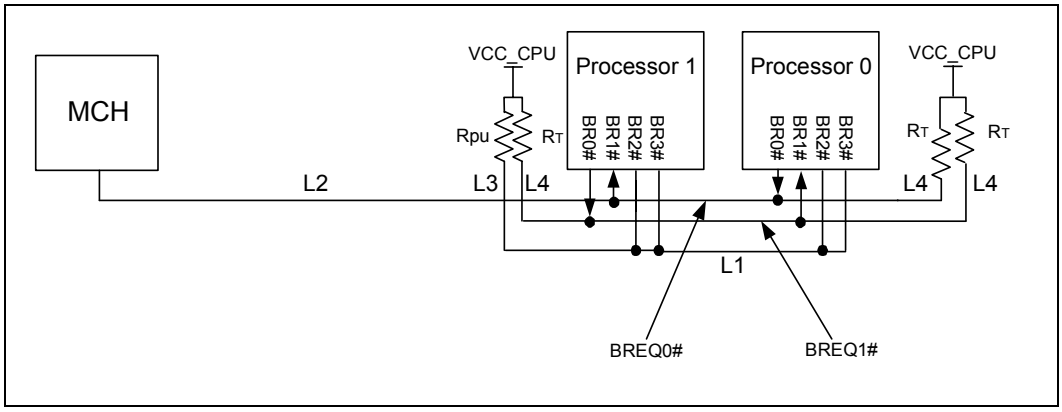


Table 5-6. BR[3:0]# Routing

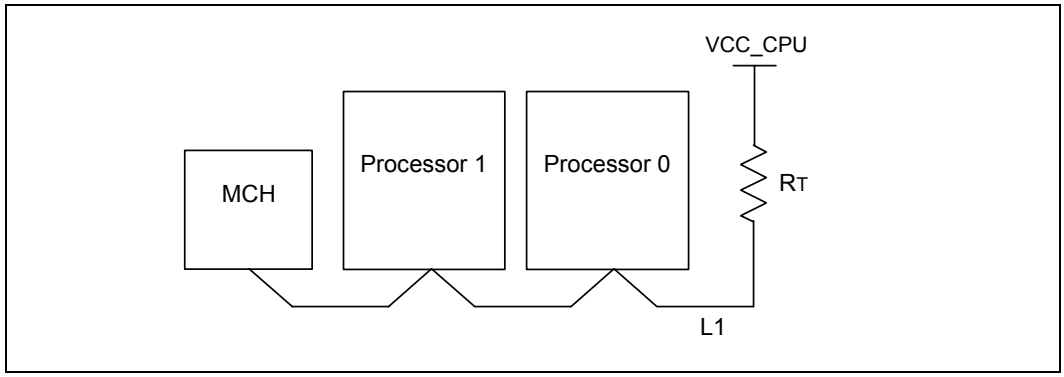
Trace Impedance	L1 Agent-to-Agent	L2 Processor 1 (BR1#) to MCH	L3 Agent-to-R_{PU} stub	L4 Agent-to-R_T stub	R_T	R_{PU}
50 Ω	3 to 10”	0 to 15.7”	0 to 3”	0 to 1”	50 Ω ± 5%	50 Ω ± 5%

5.2.2 RESET# Routing Guidelines

Because the processor does not contain on-die termination for the RESET# input signal, follow the same routing guidelines given for common clock signals in Section 5.2, but with the following additional layout guidelines pertaining to the termination resistor:

- Add a 50 Ω ± 5% termination resistor (denoted "R_T" in Figure 5-3) to the baseboard near Processor 0.
- The baseboard trace length from Processor 0's pin to the termination resistor should be 0 to 1 inch.

Figure 5-3. RESET Routing Guidelines

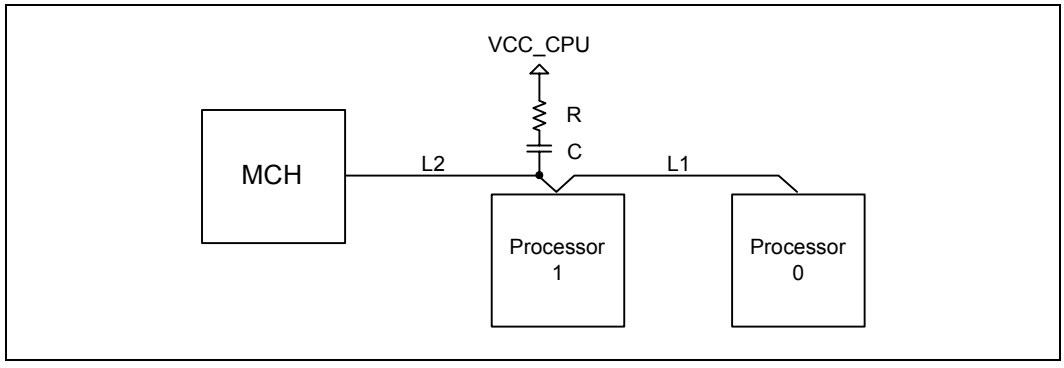


5.2.3 Wired-OR Signals

There are five “wired-OR” signals on the system bus. These signals are HIT#, HITM#, MCERR#, BINIT#, and BNR#. These signals differ from the other system bus signals in that more than one agent can be driving the signal at the same time. Timing and signal integrity must be met for the cases where one agent is driving, all agents are driving, and any combination of agents are driving. Adhere to the layout guidelines presented in Table 5-2.

Initial design studies indicate that RC termination for wired-OR signals, as shown in Figure 5-4, is not required for this platform with the Intel Xeon processor with 512-KB L2 cache.

Figure 5-4. Wired-OR Topology



5.3 Routing Guidelines for Asynchronous GTL+ and Miscellaneous Signals

This section provides routing guidelines for the signals listed in Table 5-7.

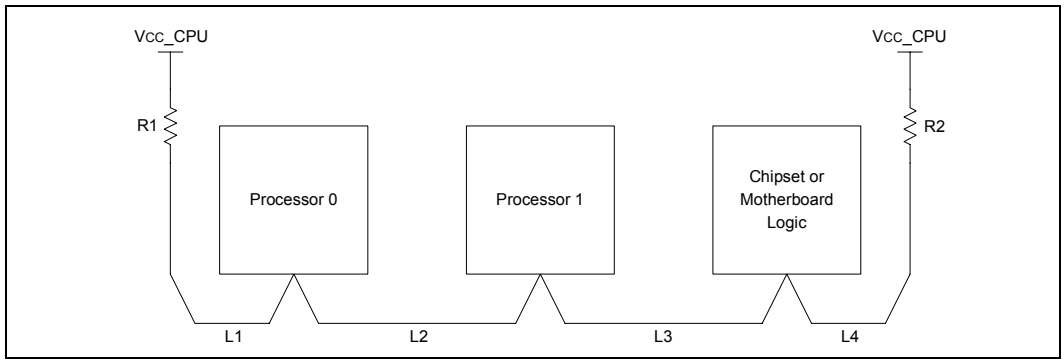
Table 5-7. Assisted GTL+ and Miscellaneous Signals

Signal Name	Type	Processor I/O Type	Driven by	Received by
A20M#	Asynchronous GTL+	I	Intel® ICH4	Processor
BINIT#	Asynchronous GTL+	I/O	Processor/Chipset	Processor
BR[3:1]#	Asynchronous GTL+	I	Processor	Processor
BR0#	Asynchronous GTL+	I/O	Processor	Processor/Chipset
BSEL[1:0]	Other	O	Processor	External Logic
COMP[1:0]	Analog	I	Pull-down	Processor
FERR#	Asynchronous GTL+	O	Processor	Chipset
IERR#	Asynchronous GTL+	O	Processor	External Logic
IGNNE#	Asynchronous GTL+	I	ICH4	Processor
INIT#	Asynchronous GTL+	I	ICH4	Processor
LINT[1:0]	Asynchronous GTL+	I	ICH4	Processor
ODTEN	Other	I	Pull-up / Pull-down	Processor
PROCHOT#	Asynchronous GTL+	O	Processor	External Logic
PWRGOOD	Other	I	ICH4	Processor
SLP#	Asynchronous GTL+	I	ICH4	Processor
SM_ALERT#	SMBus (3.3 V)	O	Chipset / Processor	Chipset
SM_CLK	SMBus (3.3 V)	I/O	Chipset	Processor
SM_DAT	SMBus (3.3 V)	I/O	Chipset / Processor	Chipset / Processor
SM_EP_A[2:0]	SMBus (3.3 V)	I	Pull-up / Pull-down	Processor
SM_TS_A[1:0]	SMBus (3.3 V)	I	Pull-up / Pull-down	Processor
SM_WP	SMBus (3.3 V)	I	Pull-up / Pull-down or external logic	Processor
SMI#	Asynchronous GTL+	I	ICH4	Processor
STPCLK#	Asynchronous GTL+	I	ICH4	Processor
TAP signals	TAP	See Chapter 12		
THERMDA	Other	O	Processor	Thermal Sensor
THERMDC	Other	O	Processor	Thermal Sensor
THERMTRIP#	Asynchronous GTL+	O	Processor	External Logic
VCCA	Power	I	RLC Filter Circuit	Processor
VCCIOPLL	Power	I	RLC Filter Circuit	Processor
VCC_SENSE	Other	O	Processor	Test Point
VID[4:0]	Other	O	Processor	Voltage Regulator
GTLREF	Power	I	Pull-up / Pull-down	Processor
VSSA	Power	I	RLC Filter Circuit	Processor
VSS_SENSE	Other	O	Processor	Test Point

5.3.1 Asynchronous GTL+ Signals Driven by the Processor

Follow the topology shown in Figure 5-5 and guidelines in Table 5-8 when routing FERR#, IERR#, and THERMTRIP#. Note that FERR# and THERMTRIP# connect both processors to the ICH4 on the customer reference board. Follow the topology in Figure 5-5 when connecting IERR# and PROCHOT# to other motherboard logic for system management and thermal monitoring. Do not route a stub to connect to Processor 1.

Figure 5-5. Topology for Asynchronous GTL+ Signals Driven by the Processor



NOTE: If IERR is used, follow the topology shown in Figure 5-5. If MCERR is used, no pull-ups are required.

Intel recommends using dual termination for THERMTRIP# signal routing implemented according to Figure 5-5. Another option is to individually route each processor's THERMTRIP# output to its own receiver logic to detect Thermtrip conditions on each processor. If routed separately, each signal must be terminated at the receiver end only.

Table 5-8. Routing Guidelines for Asynchronous GTL+ Signals Driven by the Processor

Parameter	Routing Guideline	Reference
Characteristic Trace Impedance (Z_O)	50 Ω	Figure 5-5
Nominal Trace Spacing	10 mil for Layers 3 & 6 routing (stripline), 15 mils for Layer 1 & 8 routing (microstrip).	Figure 5-5
L1	0.1" – 1.5"	Figure 5-5
L2	0.1" – 10"	Figure 5-5
L3	0.1" – 10"	Figure 5-5
L4	0.1" – 1.5"	Figure 5-5
R1	56 Ω ± 5%	Figure 5-5
R2	56 Ω ± 5%	Figure 5-5

5.3.2 Proper THERMTRIP# Usage

To protect the processors from damage in over-temperature situations, power to the processor core must be removed within 0.5 seconds of the assertion of THERMTRIP#. If power is applied to a processor when no thermal solution is attached, normal leakage currents can cause the die temperature to rapidly rise to levels at which permanent silicon damage is possible. This high temperature will cause THERMTRIP# to go active. All power supply sources to all processors must be disabled when any installed processor signals THERMTRIP#. In the customer reference board schematics, this is implemented by connecting the THERMTRIP# signals from both processors to the ICH4 THERMTRIP# input pin.

5.3.3 Asynchronous GTL+ Signals Driven by the Chipset

Follow the topology shown in Figure 5-6 and guidelines in Table 5-9 when routing A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI# and STPCLK#. INIT# routing requirements are unique as it is routed to the voltage translator circuitry. See Section 10.4.4 for details regarding INIT# voltage translation circuitry. Do not route a stub to connect to Processor 1.

Figure 5-6. Topology for Asynchronous GTL+ Signals Driven by the Chipset

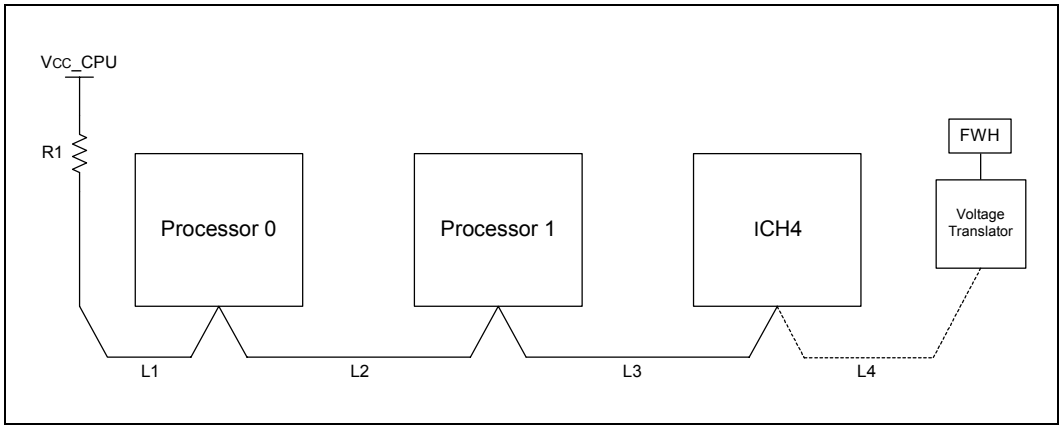


Table 5-9. Routing Guidelines for Asynchronous GTL+ Signals Driven by the Chipset

Parameter	Routing Guideline	Reference
Characteristic Trace Impedance (Z_O)	50 Ω	Figure 5-6
Nominal Trace Spacing	10 mil for Layers 3 and 6 routing (stripline), 15 mils for Layer 1 and 8 routing (microstrip)	Figure 5-6
L1	0.1” – 1.5”	Figure 5-6
L2	2.0” – 10”	Figure 5-6
L3	0.1” – 10”	Figure 5-6
L4[1]	0.1” – 9.0”	Figure 5-6
R1	200 Ω ± 5%	Figure 5-6

NOTE: L4 used for INIT# routing to FWH from ICH4. See Section 10.4.4 for INIT# voltage translation circuitry.

Route PWRGOOD as shown in Figure 5-7 and described in Table 5-10. You may choose to isolate PWRGOOD for each VRM and processor pair to recognize individual VRM failures.

Figure 5-7. Topology for PWRGOOD

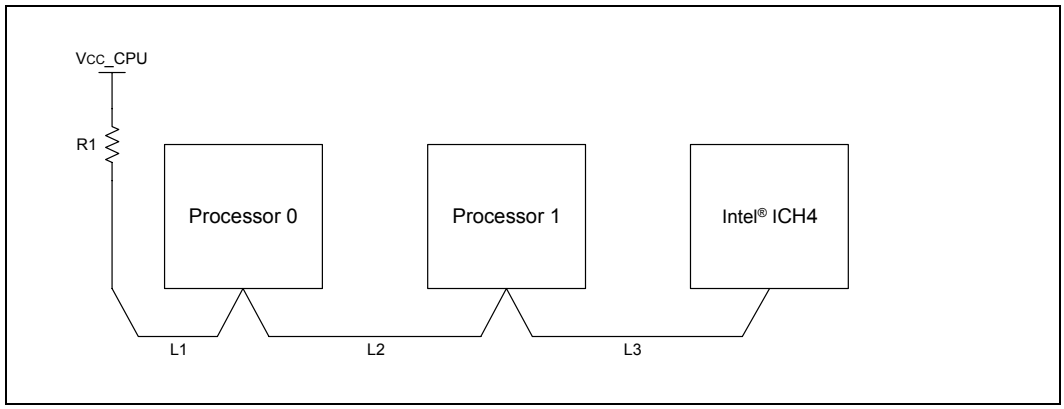


Table 5-10. Routing Guidelines for PWRGOOD

Parameter	Routing Guideline	Reference
Characteristic Trace Impedance (Z_O)	50 Ω	Figure 5-7
Nominal Trace Spacing	10 mil for Layers 3 and 6 routing (stripline), 15 mils for Layer 1 and 8 routing (microstrip).	Figure 5-7
L1	0.1” – 1.5”	Figure 5-7
L2	0.1” – 10”	Figure 5-7
L3	0.1” – 10”	Figure 5-7
R1	300 Ω ± 5%	Figure 5-7

5.3.4 VID[4:0]

Route the VID[4:0] signals of the processor to the VID[4:0] inputs of the voltage regulator controller. The voltage regulator controller should provide internal pull-up resistors for these signals. Refer to the *VRM 9.1 DC-DC Converter Design Guidelines* and the specification of the voltage controller specific to your design for further details.

Because both processors must operate at the same voltage, you should provide a way to check the VID[4:0] signals to ensure a processor does not operate out of specification.

5.3.5 COMP[1:0] Routing Guidelines

Terminate the COMP[1:0] pins to ground through 49.9 Ω ± 1% resistors. Refer to the latest schematics for the resistor values. Do not wire the COMP pins together — connect each pin to its own termination resistor.

5.3.6 ODTEN Signal Routing Guidelines

Processor 0 must have its on-die termination enabled. To enable the on-die termination, pull the ODTEN pin to a high state by terminating it to VCC_CPU through a resistor that falls within the range of 50 Ω ± 20%. Processor 1 must have its on-die termination disabled. To disable on-die termination, pull the ODTEN pin to ground through a resistor that falls within the range of 50 Ω ± 20%.

5.3.7 TESTHI[6:0] Routing Guidelines

All TESTHI[6:0] pins must be connected to VCC via pull-up resistors that fall within the range of 50 Ω ± 20%. TESTHI[3:0] may all be tied together and pulled up to VCC with a single 50 Ω ± 20% resistor if desired. TESTHI[6:5] may also be tied together and pulled up to VCC with a single 50 Ω ± 20% resistor. However, boundary scan testing will not be functional if any TESTHI pins are pulled up together. TESTHI4 must always be pulled up independently from the other TESTHI pins regardless of the usage of boundary scan.

5.3.8 SKTOCC# Signal Routing Guidelines

The SKTOCC# signal is an output from the processor that is used as an indication of whether a processor is installed or not. It will be asserted low when a processor is installed in the socket, and will float when there is no processor present. SKTOCC# can be used to disable the VRM output for unpopulated processor sockets or the power supply output when no processors are installed, and for other features.

5.3.9 XSWING/YSWING Routing Guidelines

Terminate the MCH HXSWNG/HYSWNG pins to an RC resistor divider. Refer to the latest schematics for the resistor values. Do not wire the SWING pins together — connect each pin to its own termination resistor.

FC-mPGA2 Package and 604-pin Socket Guidelines 6

This chapter provides the updated guidelines required for the Intel Xeon processor with 512-KB L2 cache/E7505 chipset platforms operating with 400 MHz or 533 MHz system bus. Because of the two package type offerings, the platform designer must understand the feature differences between the packages and how to design a platform that supports each package type. Additional system bus routing guidelines, unrelated to package type, are located in Chapter 5.

6.1 FC-mPGA2 Package Identification

Processors available in the FC-mPGA2 package provide both an electrical and mechanical method for the motherboard to identify this package. The FC-mPGA2 package contains an extra pin (located at location AE30) not found the INT-mPGA package. This additional pin is a keying mechanism that prevents the FC-mPGA2 package from being installed in the 603-pin socket because processors in the FC-mPGA2 package are supported only in the 604-pin socket. The FC-mPGA2 package contains a pin solder fillet that prevents complete insertion in the 603-pin socket. Section 6.2 contains more details about the 604-pin socket.

The FC-mPGA2 package utilizes a signal at pin AE4 named “SMB_PRT (SMBus Present)” that is defined as a reserved signal on the INT-mPGA package. This signal can be used by the motherboard logic to detect processor package type. For example, platforms with the 604-pin socket may implement logic that determines proper support for the manageability features found on the INT-mPGA or FC-mPGA2 package as described in Section 6.3. Table 6-1 summarizes the behavior of pin AE4 on both package types.

Table 6-1. Pin AE4 Signal Level Based on Package Type

Processor Package Type	Pin AE4 Definition	Output
INT-mPGA	Reserved	Z (High Impedance)
FC-mPGA2	SMB_PRT	L (Grounded on package)

6.2 604-Pin Socket

The 604-pin socket contains an additional contact to accept the additional keying pin on the processor in FC-mPGA2 packages at pin location AE30 (described in Section 6.1). The 604-pin socket also accepts processors with the INT-mPGA package. Because the additional contact for pin AE30 is electrically inert, the 604-pin socket does not have a bottom-side contact for soldering onto the motherboard. Therefore, the additional keying pin does not require a motherboard via nor a surface-mount pad.

6.3 SMBus Implementation

Processors available in the FC-mPGA2 package (*Intel® Xeon Processor with 533 MHz Sysytem Bus)*do not contain the SMBus devices (i.e., PIROM, OEM EEPROM and thermal sensor) that are provided in the INT-mPGA package. The following sections provide guidelines for designing a platform to operate with both processor package types with respect to these SMBus features.

6.3.1 INT-mPGA SMBus Signals

The INT-mPGA processor package contains SMBus devices (i.e., PIROM, Scratch EEPROMs and thermal sensor). The SMBus signals provide access to the thermal sensor and memory device on the processor. The signaling protocol adheres to the specification of the System Management Bus. Refer to the *Intel® Xeon Processor with 512-KB L2 Cache Datasheet* for complete details on the processor SMBus implementation and addressing scheme.

Connect the SM_ALERT#, SM_CLK, and SM_DAT signals to the SMBus controller in adherence to the *System Management Bus (SMBus) Specification, Version 1.1*. These signals can be connected to other processors on the same SMBus.

The SM_EP_A[2:0] signals set the SMBus address for the memory device on the processor. These signals must be set at power up with a unique address per bus. They have an internal 10 kΩ ± 5% pull-down. To pull the SM_EP_A[2:0] signals to a logic high level, connect each signal to a 100 Ω ± 5% resistor tied to SM_VCC/VID_VCC. Refer to the section on SMBus Device Addressing in the processor datasheet for addressing details.

The SM_TS_A[1:0] signals set the SMBus address for the thermal device on the processor. These signals must be set at power up with a unique address per bus. The SM_TS_A[1:0] can be set to logic high, logic low, or a high impedance state giving nine possible combinations of addresses. Refer to the section on SMBus Device Addressing in the processor datasheet for addressing details. The SM_TS_A[1:0] signals do not have an internal pull-down and thus must be pulled to VSS or SM_VCC/VID_VCC with a 1 kΩ ± 5% or smaller resistor. Leaving the pins floating achieves a high-Z state.

The SM_WP signal is a write protect signal for the memory device. Pulling this signal to SM_VCC/VID_VCC with a 100 Ω ± 5% resistor enables write protection. SM_WP has an internal 10 kΩ pull-down.

6.3.2 Thermal Diode and SMBus Interface

Processors available in the FC-mPGA2 package (*Intel® Xeon Processor with 533 MHz System Bus)*provide voltage readings directly from the processor core's thermal diode via the THERMDA (pin Y27) and THERMDC (pin Y28) signals. Note that these signals are not used on processors in the INT-mPGA package because thermal data is provided via the SMBus from the thermal sensor. Table 6-2 summarizes the functionality of the thermal diode and applicable SMBus pins on both processor package types.

Table 6-2. Functionality of SMBus and Thermal Diode Pins

Signal	INT-mPGA	FC-mPGA2
THERMDA (Pin Y27)	N/C: Not used by processor	Output: Provides access to anode of thermal diode
THERMDC (Pin Y28)	N/C: Not used by processor	Output: Provides access to cathode of thermal diode
SM_CLK (Pin AC28)	Input: SMBus clock	N/C: Not used by processor
SM_DAT (Pin AC29)	I/O: SMBus data signal	N/C: Not used by processor
SM_ALERT# (Pin AD28)	Output: Asserted by thermal sensor device	N/C: Not used by processor
SM_TS1_A0 (Pin AA28)	Input: Thermal Sensor Select Address	N/C: Not used by processor
SM_TS1_A1 (Pin Y29)	Input: Thermal Sensor Select Address	N/C: Not used by processor

A platform designed to support both package versions of the processor must include a method for selecting SMBus versus direct diode reading to obtain thermal data and properly interface with all signals listed in Table 6-2. The following sections describe a hardware and firmware method for supporting both package types.

6.3.2.1 Hardware Selection of SMBus Thermal Devices

Figure 6-1 illustrates a hardware method for selecting the correct thermal sensor device when either a processor in the INT-mPGA package or FC-mPGA2 package is installed. This example implementation scheme is different from what is designed in the E7505 chipset Customer Reference Board. The Customer Reference Board utilizes an integrated ASIC instead of the discrete multiplexer logic described below. When using any of the 3 discrete logic solutions discussed later in this section, the reference circuits must apply to both processor sockets. When using the integrated ASIC, as called out in the Customer Reference Board schematics, only one device is required to support both sockets. Refer to the schematics to understand the selection mechanism scheme when using the integrated ASIC.

The reference circuit in Figure 6-1 contains a multiplexer device (U3) that uses the System Management Bus Present (SM_PRT) signal to select between the system SMBus interfacing with the SMBus from the motherboard's thermal sensor (U2) versus the processor SMBus. The mux will only select the processor's SMBus interface when an INT-mPGA processor package (High-Z SM_PRT signal, which goes high with the pull-up) is present, resulting in the IN[3:1] inputs driven high. Installation of a processor with the FC-mPGA2 processor package (Grounded SM_PRT signal) will result in the mux selecting the motherboard thermal sensor to interface with the SMbus, resulting in the IN[3:1] inputs driven low.

Note that the SMBus address of the motherboard thermal sensor and processor thermal sensor are configured identically to each other and are transparent to Server Management software/firmware regardless of which processor package type is installed. Both the processor and thermal sensor

inject current onto their three-state address pins to determine their address. The thermal sensor does this every time it does an A/D conversion. As a result, both devices should not share the same address resistors.

Figure 6-1. Circuit Implementation for Hardware-Based SMBus Selection Using Mux

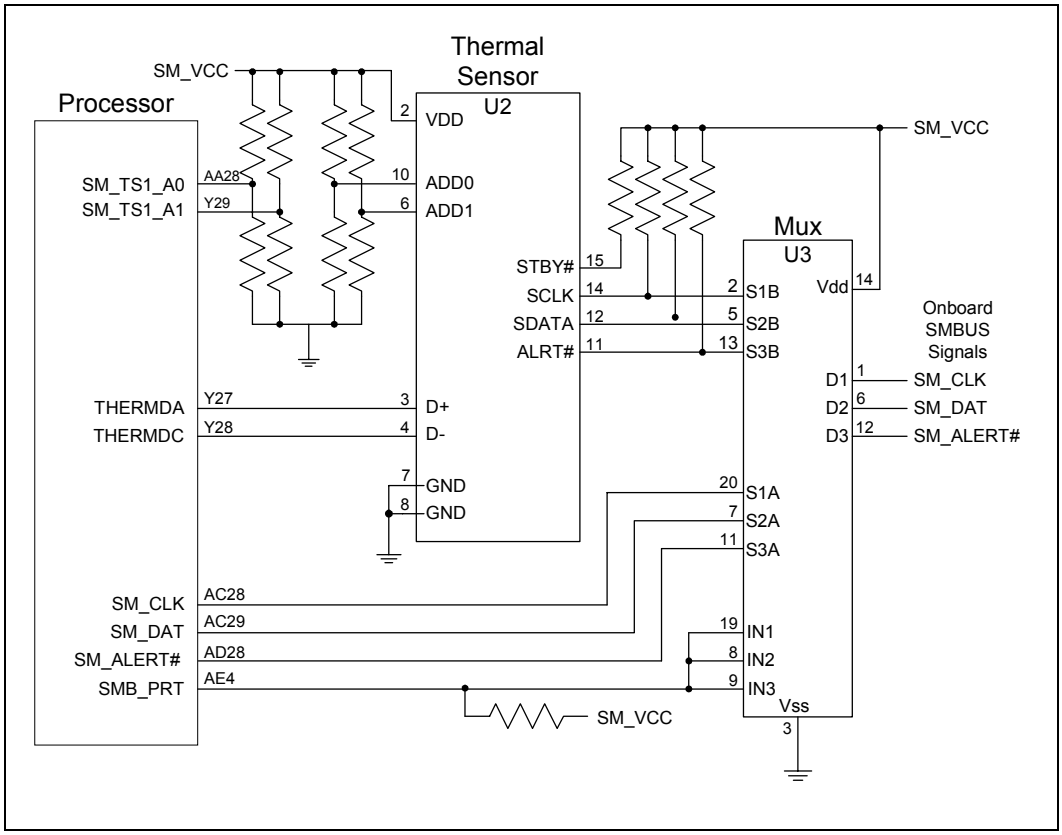


Figure 6-2. Circuit Implementation for Hardware-Based SMBus Selection Using FET

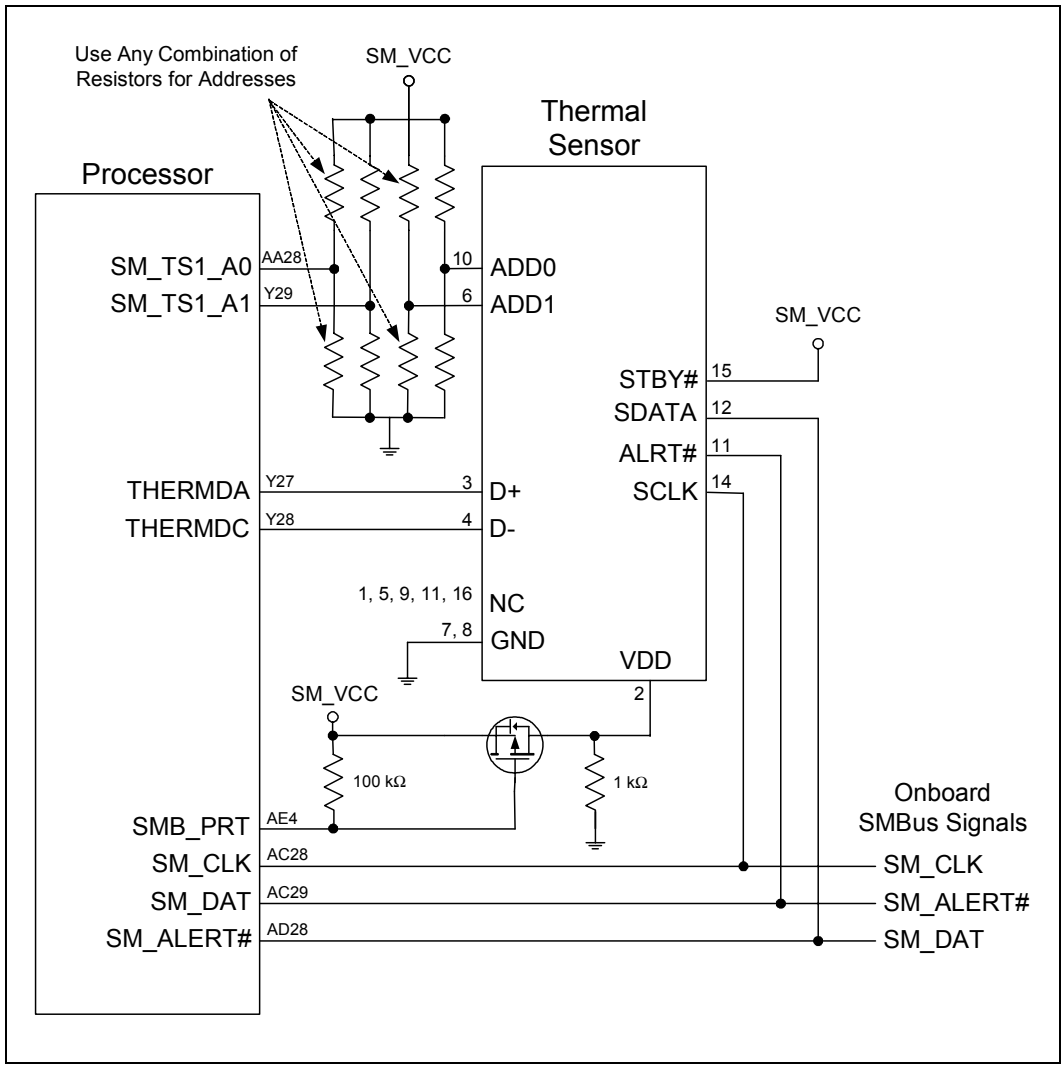


Figure 6-2 shows a shows a reference circuit similar to Figure 6-1. This circuit requires all of the following thermal sensor properties be properly electrically isolated from the SMBus when the sensor is disabled by the P-channel FET circuit. Refer to the vendor thermal sensor documentation to confirm these requirements:

The SCLK, SDATA, and ALRT# signals must exhibit a high-Z state. For example, high input current due to backpowering of the device or unpredictable I/O logic behavior as a result of a grounded VDD may prevent correct SMBus operation by pulling any of these signals to an electrically low state.

The SCLK, SDATA, and ALRT# must not exhibit increased leakage current when the VDD supply is grounded. If this is the case, the motherboard pull-up resistance must be evaluated for acceptable VIHMIN levels due to the increased leakage current.

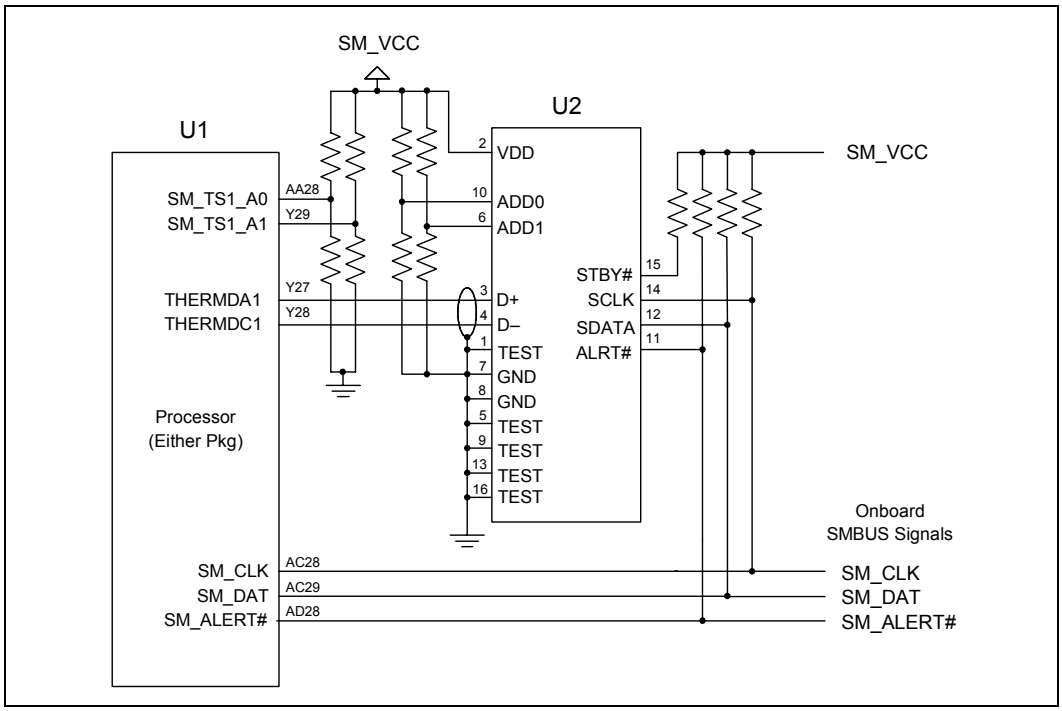
The reference circuit shown in Figure 6-2 assumes the Field Effect Transistor (FET) is a P-channel logic type with low source-to-drain on-resistance and source-to-drain current capacity to supply power to the thermal sensor. Based on the thermal sensor components listed in Figure 6-3, the FET should be capable of handling a minimum of 180 µA source-drain current and have less than 1 Ω source-drain resistance. The FET also needs specific gate electrical specifications to support the two logic levels presented by a processor-driven grounded or open SMB_PRT signal (state depends on processor type), and the associated pull-up resistor\voltage used in the reference circuit. The FET should have a maximum gate input leakage current of 1 µA when the FET is in the OFF state.

The FET should have a minimum\maximum VGS-Thresh (Gate-Source Threshold Voltage) of approximately -0.4 V\-1.0 V. The “minimum” value of -0.4 V will prevent leakage current when pulling an open SMB_PRT signal to an electrically low state. And the “maximum” -1.0 V value will still allow a grounded SMB_PRT signal to switch the FET's gate to an ON state.

6.3.2.2 Firmware Selection of SMBus Thermal Devices

This section describes a firmware method for supporting a processor in either the INT-mPGA package or FC-mPGA2 package. This method is based on the thermal sensor implementation illustrated in Figure 6-3. The SMBus is connected to the motherboard thermal sensor and processor SMBus signals. The motherboard thermal sensor (U2) must have a different SMBus address than the processor's thermal sensor. SMBus software then attempts to read from the address used to define the processor thermal sensor. If a processor with INT-mPGA package is installed, the SMBus controller will receive the data it expects. If a processor with FC-mPGA2 is installed, a time-out occurs. The SMBus software reads from the alternate SMBus address defined for the motherboard thermal sensor (U2). The advantage of this method over the hardware discussed in the previous section is that a mux device is not required. However, in the event of a thermal sensor failure on a processor with the INT-mPGA package, the SMBus software will falsely assume that the processor is an FC-PGA2 package.

Figure 6-3. Circuit Implementation for Firmware-Based SMBus Selection



6.3.3 Thermal Sensor Selection

The example thermal sensor implementations described in the previous sections assume that the same thermal sensor device that is used on the INT-mPGA package (See Table 6-3 for details) is also placed on the motherboard to provide equivalent thermal sensor operation between INT-mPGA and FC-mPGA2 processors. Use of either of the thermal sensor devices listed in Table 6-3 is not required because device selection should be based on the features, operating requirements, or other factors defined by the platform.

Table 6-3. Thermal Sensor Part Details

Vendor	Part Number
Philips Semiconductor	NE1617A
Analog Devices, Inc.	ADM1021A

6.3.4 Thermal Sensor Layout and Routing Considerations

Because the motherboard thermal sensor device is measuring very small voltages from the processor (FC-mPGA2 package only) thermal diode, extreme care must be taken to minimize the noise induced on the thermal sensor input pins. The following are guidelines that help ensure a clean thermal sensor implementation:

- Place the thermal sensor device as close to the processor socket as possible. Intel strongly recommends surrounding the signal pair with ground guard traces and adding component pad sites close to the thermal sensor input to support a shunt capacitor between the THERMDA and THERMDC signal traces. Consult your thermal sensor vendor for specific details regarding these recommendations.
- Route the processor thermal diode output signals close together and in parallel. If possible, provide ground guard traces on each side of the signal pair
- Use wide traces and spacing to route the processor thermal diode output signals. This will minimize induction and reduce the noise on these signals
- Keep noisy sources (e.g., clock generators and high-speed data and address buses) away from the thermal sensor and the processor thermal diode output signals to help minimize noise

For more in-depth layout and routing considerations, refer to documentation provided by your thermal sensor device vendor.

6.3.5 Alternatives Methods to Obtain PIROM Data

Because the processor in the FC-mPGA2 package does not contain a PIROM device, systems must not rely upon this data content. However, some of the PIROM data field contents may be obtained by alternative methods either by using the CPUID instruction, or by reading specific processor Model Specific Registers. Table 6-4 summarizes the information available and the method for obtaining the data. Refer to the *Intel® NetBurst™ Microarchitecture BIOS Writer's Guide* for complete details.

Table 6-4. Alternatives Methods to Obtain Processor Information on FC-mPGA2-Packaged Processors

PIROM Data Field	Alternative Method for Obtaining Information
Processor Core Data	
Processor Core Type	CPUID with input 1
Processor Core Model	CPUID with input 1
Processor Core Family	CPUID with input 1
Processor Core Stepping	CPUID with input 1
System Bus Speed	MSR_EBC_FREQUENCY_ID
Maximum Core Frequency	MSR_EBC_FREQUENCY_ID[1]
Cache Size	
L2 Cache Size	CPUID with input 2
L3 Cache Size	CPUID with input 2

NOTE:
1. This register provides the core frequency-to-system bus ratio. Processor core frequency may be obtained by multiplying the ratio times the system bus frequency.

6.4 Boot Critical Signals

Processors can run only in certain dual-processor configurations. The following section discusses how certain processor signals are used in sample circuits to operate with correct dual-processor operation.

6.4.1 VID[4:0]

Route the VID[4:0] signals of the processor to the VID[4:0] inputs of the voltage regulator controller. The voltage regulator controller should provide internal pull-up resistors for these signals. Refer to the *VRM 9.1 DC-DC Converter Design Guidelines* and the specification of the voltage controller specific to your design for further details.

Because both processors must operate at the same voltage, provide a way to check the VID[4:0] signals to ensure that a processor does not operate out of specification. Refer to Figure 6-4 for more information.

6.4.2 SKTOCC# Signal Routing Guidelines

The SKTOCC# signal is an output from the processor that is used as an indication of whether a processor is installed or not. It is asserted low when a processor is installed in the socket, and floats when no processor is present. If this signal is used on the board, the designer can use a pull-up to prevent floating. SKTOCC# can be used to disable the VRM or VRD output for unpopulated processor sockets or the power supply output when no processors are installed and other features.

6.4.3 BSEL[1:0] Implementation

The processor provides two output signals named "BSEL[1:0]" for the motherboard to identify the system bus frequency supported by the processor installed. The BSEL[1:0] output values are shown in Table 6-5.

These outputs may be used by motherboard logic to:

- Automatically select the proper system bus clock frequency driven by the CK408 clock driver.
- Verify that both processors support the same system bus frequency. If processor system bus frequencies do not match, then disable the voltage regulator output that supplies power to the processors.

Table 6-5. BSEL[1:0] Implementation

System Bus Frequency	BSEL1	BSEL0
400 MHz	L	L
533 MHz	L	H

6.4.4 Sample Implementation Circuit

Figure 6-4 shows an example BSEL[1:0] motherboard implementation that is incorporated into the Customer Reference Board. This circuit performs those functions mentioned in Section 6.4.3 and leverages the VID comparator logic. The BSEL[1:0] outputs from both processor sockets are routed to the P6/P5 and Q6/Q5 inputs of the VID comparator. The comparator checks that all VID[4:0] and BSEL[1:0] signal values match on both processors. The SKTOCC# signal is also utilized to determine when Socket 1 is not populated.

The first condition of this circuit that enables the voltage regulator is when the VIDs and BSELs match. If both processors are installed and running with the same VID and BSEL values, a low goes to the input of the NAND from the comparator, enabling the voltage regulator.

The second condition of this circuit that enables the voltage regulator is when Socket 1 is not populated. If a processor is present only in Socket 0, an erroneous mismatch signal is ignored, and the low asserted from the inverter ensures the NAND outputs a high, enabling the voltage regulator.

The condition that disables the voltage regulator is when both inputs to the NAND are high. In this case, there is both a mismatch (comparator outputs a high) and a populated Socket 1 (the SKTOCC# inverter outputs a high). In this instance, the NAND outputs a low, disabling the voltage regulator. If both processors are present, the VIDs and BSELs do not match. If Socket1 is populated and Socket 0 is not, a mismatch occurs, disabling the voltage regulator.

The BSEL0 output from the processor 0 socket is also connected to the CK408 and GPI to program both devices to operate at either 100 MHz or 133 MHz based on the processor installed. Table 6-6 summarizes the operation of the reference circuit.

Figure 6-4. VID[4:0] and BSEL[1:0] Reference Circuit

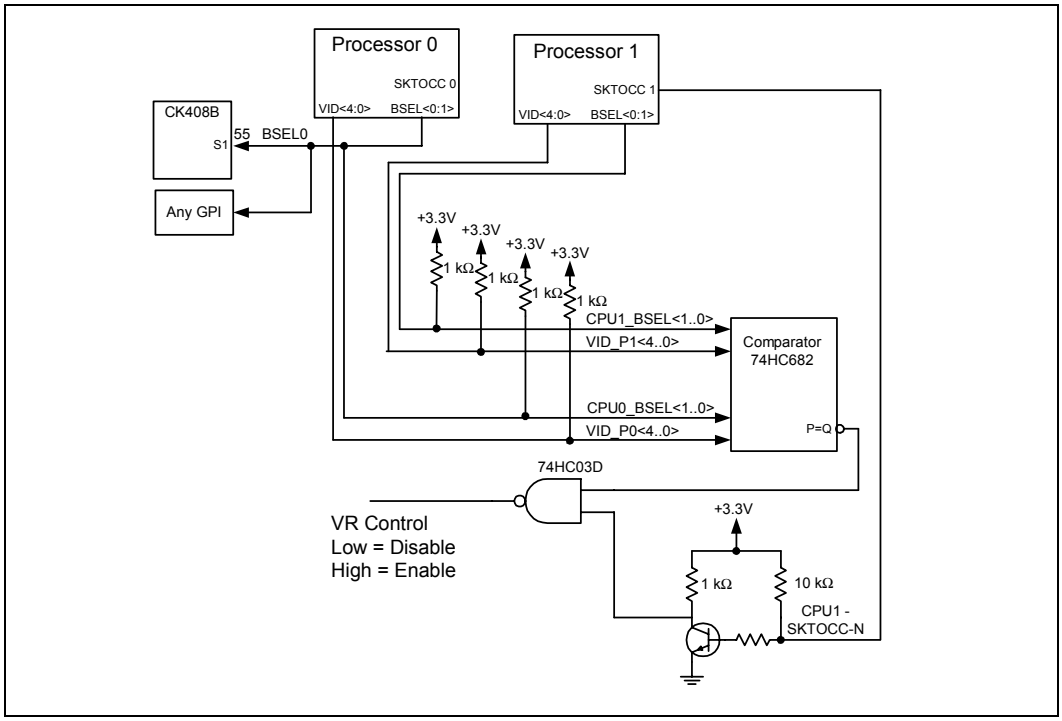


Table 6-6. Functionality of SKTOCC# and VR Output

Processor 0 Socket	Processor 1 Socket	SKTOCC#	VR Control Output Low = Disable High = Enable	Functionality
533	533	L	H	Operates system in DP mode with 133 MHz system bus clock
400	533	L	L	Disables voltage regulator to prevent processor operation
533	400	L	L	Disables voltage regulator to prevent processor operation
400	400	L	H	Operates system in DP mode with 100 MHz system bus clock
533	None	H	H	Operates system in UP mode with 133 MHz system bus clock
None	533	L	L	Disables voltage regulator to prevent processor operation
400	None	H	H	Operates system in UP mode with 100 MHz system bus clock
None	400	L	L	Disables voltage regulator to prevent processor operation

NOTE: VID[4:0] has been omitted from this table to simplify the description. Described functionality assumes that VID values match when both processors are installed. When VID values do not match, the circuit disables the voltage regulator to prevent unsupported processor operation.

DDR System Memory Design Guidelines 7

This chapter contains information and details for designing an E7505 chipset-based platform with DDR266. The chapter provides information on the DDR reference stack-up, topologies and DDR layout, and routing guidelines for each system memory interface signal group. This chapter also provides system memory bypass capacitor guidelines and DDR power deliver requirements. Together, these guidelines provide a robust DDR solution for E7505 chipset-based designs. The MCH supports both registered and unbuffered memory. Section 7.3 deals with the unbuffered memory topologies, and Section 7.4 deals with the registered memory topologies.

As system memory transfer rates increase, careful attention must be placed on all of these E7505 chipset guidelines to provide system robustness.

The MCH has a dual-channel memory interface. The pinout for the two channels has been optimized for a motherboard design with interleaved DIMMs. The DIMM closest to the MCH is DIMM0 on channel A, followed by DIMM0 on Channel B. The DIMMs continue to alternate between Channel A and B to the termination resistors.

The E7505 chipset Double Data Rate (DDR) SDRAM system memory interface provides support for unbuffered and registered memory. The system memory interface can be divided into six signal groups: Data, Address/Command, Control, Feedback, Clocks, and DC bias signals. Table 7-1 summarizes the signal groupings. Refer to the *Intel® E7505 Chipset Memory Controller Hub (MCH) Datasheet* for more details on these signals.

The E7505 chipset supports Error Checking and Correction (ECC).

7.1 DDR DIMM Ordering

Figure 7-1 and Figure 7-2 show both channels being routed to a single "bank" of eight DIMMs. The DIMMs are physically interleaved. Intel recommends using this interleaving, starting with Channel B closest to the MCH, for optimal routing.

The platform requires DDR DIMMs to be populated in-order, starting with the DIMMs furthest from the MCH in a "fill-farthest" approach (see Figure 7-1 and Figure 7-2). In addition, single rank DIMMs should be populated furthest when a combination of single ranked and double ranked DIMMs are used. This recommendation is based on the signal integrity requirements of the DDR interface. Intel's recommendation is to check for correct DIMM placement during BIOS initialization. For a 2-DIMM board, follow the same methodology.

Figure 7-1. 3-DIMM per-Channel Implementation

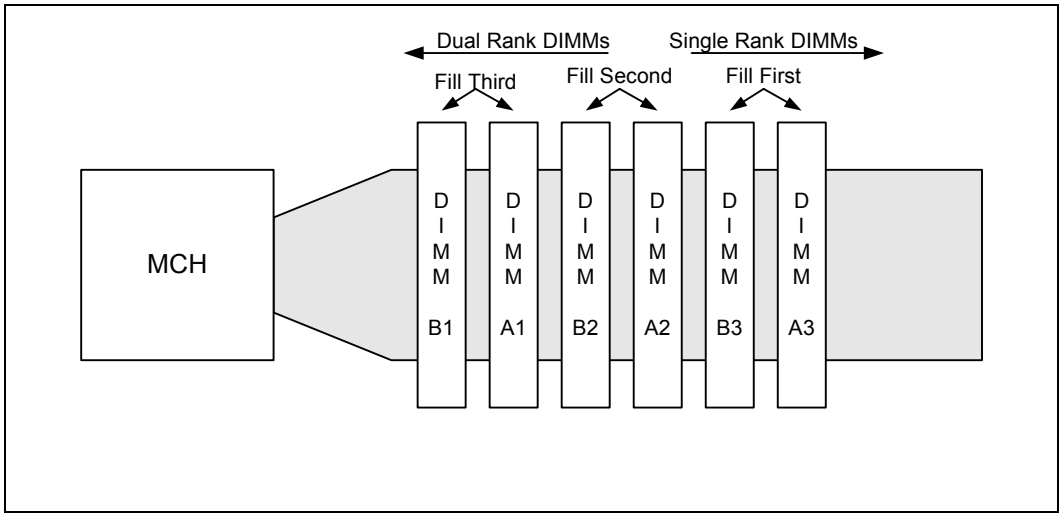
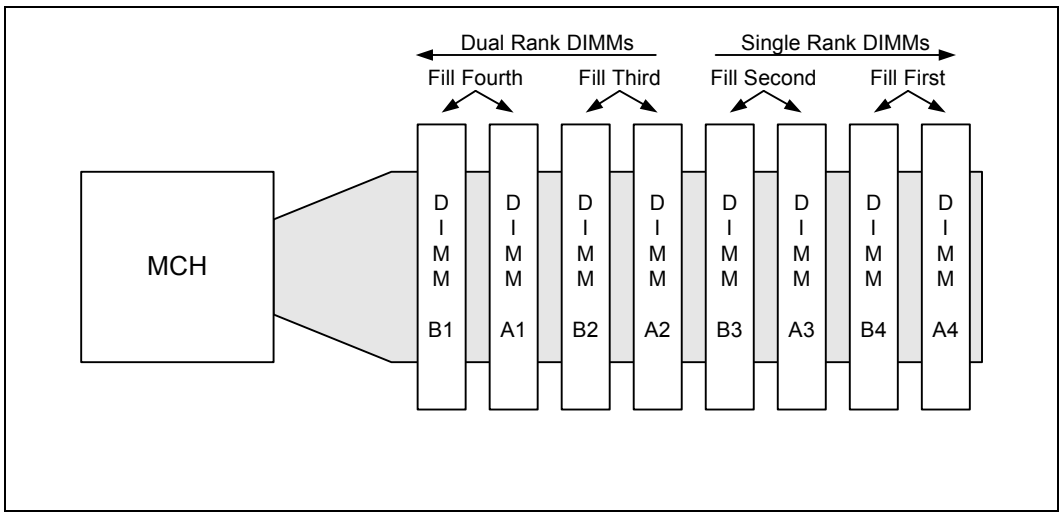


Figure 7-2. 4-DIMM per-Channel Implementation



Certain combinations of DIMM types in 3-DIMM and 4-DIMM per channel systems have been found to violate the JEDEC write ring back measurement specification. 1-DIMM and 2-DIMM per channel systems do not violate the JEDEC write ring back specification. When combining double-rank DIMMs (x4 or x8) with single-rank DIMMs (x4 or x8), if the first populated slot (closest to the MCH) contains a single-ranked DIMM, the write ringback at that DIMM violates the JEDEC DRAM specification. To reduce write ring back, populate single-ranked DIMMs furthest from the MCH when a combination of single-ranked and double-ranked DIMMs is used.

To determine if a registered DDR DIMM is a single-bank DIMM or a double-bank DIMM, please refer to Application Note (AP-727) *Distinguishing Between Single-Rank And Double-Rank Registered DDR DIMM Modules*.

Figure 7-3. Example of Proper Single and Dual Rank Mixing

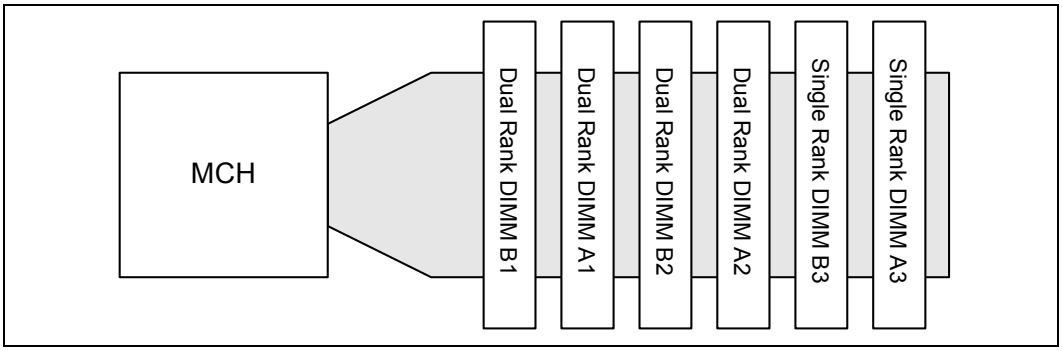


Figure 7-4. Example of Incorrect Single and Dual Rank Mixing

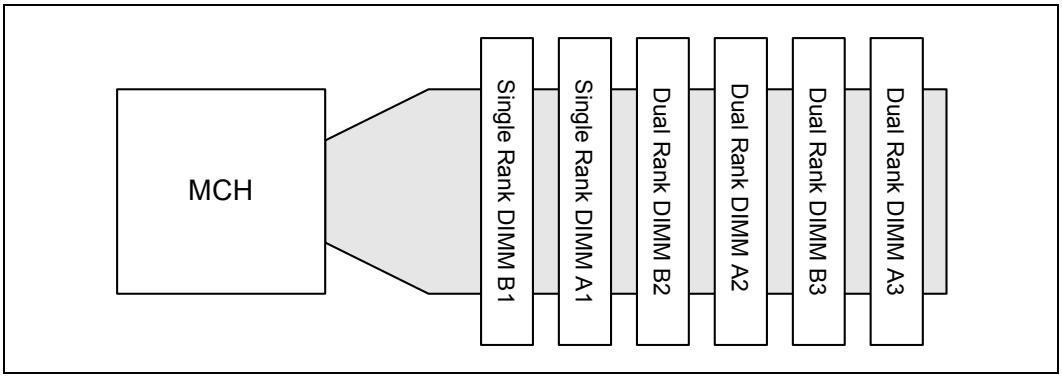


Table 7-1. Intel® E7505 Chipset DDR Signal Groups

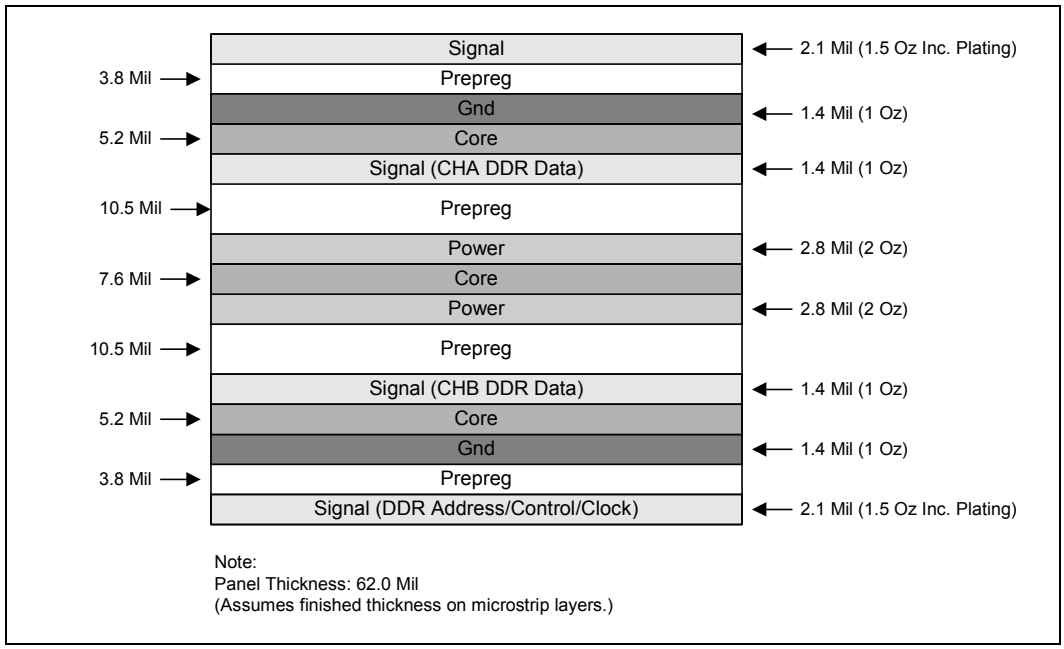
Group	Signal Name	Description
Data	DQ_x[63:0]	Data Bus
	DQS_x[17:0]	Data Strobes
	CB_x[7:0]	ECC Check Bits
Address / Command	MA_x[13:0]	Memory Address Bus
	BA_x[1:0]	Bank Address (Bank Select)
	RAS_x#	Row Address Select
	CAS_x#	Column Address Select
	WE_x#	Write Enable
Control	CKE_x[3:0]	Clock Enables – (One per Device Row)
	CS_x[3:0]# CS_x[7:4]#	Chip Selects – (One per Device Row) Chip Selects Multiplexed with CMDCLKs (Multiplexing will be detailed in Section 7.4.2)
Clocks	CMDCLK_x[7:0]	Differential Clocks • 3 pairs per DIMM unbuffered • 1 pair per DIMM registered
	CMDCLK_x[7:0]#	Inverted Differential Clocks
DC Biasing	RCVENOUT_x#	Receive Enable Output
	DRCOMP_H	Compensation for DDR Horizontal Direction Buffers
	DRCOMP_V	Compensation for DDR Vertical Direction Buffers
	ODTCOMP	Compensation for On-Die Termination Resistors
	DRCOMPVREF_H	Resistive Compensation for Horizontal Buffers
	DRCOMPVREF_V	Resistive Compensation for Vertical Buffers
	DDR_STRAP	DDR Strap Input
	DVREF_A / DVREF_B	Voltage Reference

7.2 DDR-SDRAM Stack-Up and Referencing Guidelines

Intel E7505 chipset platform designs using the DDR-SDRAM memory sub-system require continuous ground referencing for all DDR signals. Based on the eight-layer stack-up shown in Figure 7-5, the DDR channel is completely ground referenced. Although the DDR bus is technically referencing both power and ground, it is more tightly coupled to the ground plane because of closer proximity to the ground plane than the power plane. Attention must still be paid to ensure that DDR signals do not cross power plane splits because a small percentage of the return current will travel through the power planes.

All DDR signals must be ground referenced to provide an optimal current return path. To do this, the ground plane must be solid and continuous from the MCH DDR signal pins to beyond the VTT termination capacitors at the end of the channel.

Figure 7-5. Board Stack-Up



7.3 Unbuffered DDR System Memory Topology and Layout Design Guidelines

This section contains information and details on the unbuffered DDR topologies, layout and routing guidelines. The guidelines are provided for each corresponding signal group: Data, Address/Command, Control, Feedback, Clock, and DC biasing. These recommendations are based on the stack-up detailed previously.

The general routing strategy in the 8-layer board is to route all the data and strobes for Channel B (closest to the edge of the MCH package) on layer 6. The Channel A data and strobes are routed entirely on Layer 3. The address, control and clock signals for both channels can be routed entirely on the bottom layer. With this strategy, the whole interface is ground referenced. The following sections describe these topologies.

The following signaling group sections are intentionally ordered in the same fashion that Intel recommends approaching the length matching criteria. The CKE and CS# signals should be routed first and made as short as possible. From those lengths, the required command clock group lengths are determined, which drives the required lengths for the data/strobe groups and address/control groups, respectively.

7.3.1 Control Signals — CKE_x[3:0], CS_x[3:0]#

The MCH control signals are source-clocked signals that include four clock enable (CKE) and four chip select (CS#) signals. These control signals are clocked into the DIMMs using the positive edge of the differential clock signals. Only one chip select (CS#) and one clock enable (CKE) signal are needed for each DDR-SDRAM physical DIMM device row.

Two chip selects and two clock enables are routed to each DIMM (one for each side) to support double-sided DDR DIMMs. Table 7-2 summarizes the CKE/CS# to DIMM and DIMM pin mapping.

Table 7-2. Control Signal DIMM Pin Mapping

Signal	Relative to	DIMM pin
CS_x0#	DIMM0	157
CS_x1#	DIMM0	158
CS_x2#	DIMM1	157
CS_x3#	DIMM1	158
CKE_x0	DIMM0	21
CKE_x1	DIMM0	111
CKE_x2	DIMM1	21
CKE_x3	DIMM1	111

Resistor packs are acceptable for the parallel (R_{TT}) control termination resistors, but the control signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, address/command signals.

Table 7-3 and Figure 7-6, Figure 7-7, and Figure 7-8 show the recommended topology and layout routing guidelines for the DDR-SDRAM control signals for the first and second DIMM.

The tuning of control and differential clock signals must take into account the package lengths internal to the MCH package. Matching requires tuning the control signals from the MCH pad to the pins of the DIMM connector to the differential clock signals.

7.3.2 Clock Signals — CMDCLK_x[7:0], CMDCLK_x[7:0]#

The MCH clock signals include eight differential clock pairs CMDCLK_x[7:0] and CMDCLK_x[7:0]#. In an unbuffered configuration, CMDCLK_x[3:2] and CMDCLK_x[3:2]# are left as no-connects at the MCH because only six pairs are needed for a 2-DIMM per channel configuration (more information on the purpose of the two extra clocks is described in the registered memory routing guidelines). The MCH generates and drives these differential clock signals required by the DDR interface. Therefore, no external clock driver is required for the DDR interface. Three differential clock pairs are routed to each DIMM connector. Table 7-3 summarizes the clock signal mapping.

Table 7-3. Clock Signal Routing

Signal	Routed to
CMDCLK_x[0,4,6], CMDCLK_x[0,4,6]#	DIMM0
CMDCLK_x[1,5,7], CMDCLK_x[1,5,7]#	DIMM1
CMDCLK_x[2,3],CMDCLK_x[2,3]#	No Connect

The differential clock pairs must be routed differentially from the MCH to their associated DIMM pins and must maintain the correct isolation spacing from other signals. When the signals serpentine, it is important to maintain the minimum spacing to other DDR signals. While serpentining, the differential clock pair must maintain correct spacing to remain differential, as well.

To help the routing of the clock signals, Table 7-3 is provided. This table summarizes a typical clock signal to DIMM pin mapping on an E7505 chipset DDR platform.

Table 7-4. Clock Signal DIMM Pin Mapping

Signal	Relative to	DIMM pin
CMDCLK_x0	DIMM0	137
CMDCLK_x0#	DIMM0	138
CMDCLK_x4	DIMM0	16
CMDCLK_x4#	DIMM0	17
CMDCLK_x6	DIMM0	76
CMDCLK_x6#	DIMM0	75
CMDCLK_x1	DIMM1	137
CMDCLK_x1#	DIMM1	138
CMDCLK_x5	DIMM1	16
CMDCLK_x5#	DIMM1	17
CMDCLK_x7	DIMM1	76
CMDCLK_x7#	DIMM1	75

The CS# and CKE lengths drive the minimum length requirements for the command clocks. The rest of the DDR system memory signals are tuned to CMDCLK/CMDCLK#. The individual group signal length matching requirements are detailed in their corresponding section for each system memory group. It is required to length match command clocks and their complements to each other (e.g., CMDCLK_x1 and CMDCLK_x1#).

No external termination resistors are needed for the clock signals. Table 7-5 and Figure 7-6, Figure 7-7, and Figure 7-8 describe the recommended topology and layout routing guidelines for the DDR-SDRAM differential clocks.

Table 7-5. Clock Signal Group Routing Guidelines

Parameter	Routing Guidelines	Reference
Signal Group	CMDCLK_x[7:4, 1:0]/CMDCLK_x[7:4, 1:0]#	
Topology	Point to point	Figure 7-6 Figure 7-7
Reference Plane	Ground Referenced Microstrip	
Characteristic Trace Impedance (Zo)	Differential = 100 Ω ± 10%	Figure 7-6 Figure 7-7
Nominal Trace Width	4.75 mils	Figure 7-8
Nominal Differential Trace Spacing	7 mils	Figure 7-8
Group Spacing	20 mils minimum from another DDR signal group 20 mils minimum from non-DDR signal group	Figure 7-8
Serpentine Spacing	20 mils minimum	
Trace Length A (CMDCLK_x[0,4,6]) – MCH Signal Ball to pin of first DIMM	Min = 3.5” (See Section 7.3.2.1) Max = 8.5” (See Section 7.3.2.1)	Figure 7-6
Trace Length A (CMDCLK_x[1,5,7]) – MCH Signal Ball to pin of second DIMM	Min = 3.5” (See Section 7.3.2.1) Max = 8.5” (See Section 7.3.2.1)	Figure 7-7
MCH Breakout Guidelines	5-mil width / 5-mil spacing for a max length of 500 mils. This length should be minimized.	
Length Matching	See Section 7.3.2.1	

Figure 7-6. DDR Clock Routing Topology (CMDCLK_x[0,4,6]/CMDCLK_x[0,4,6]#)

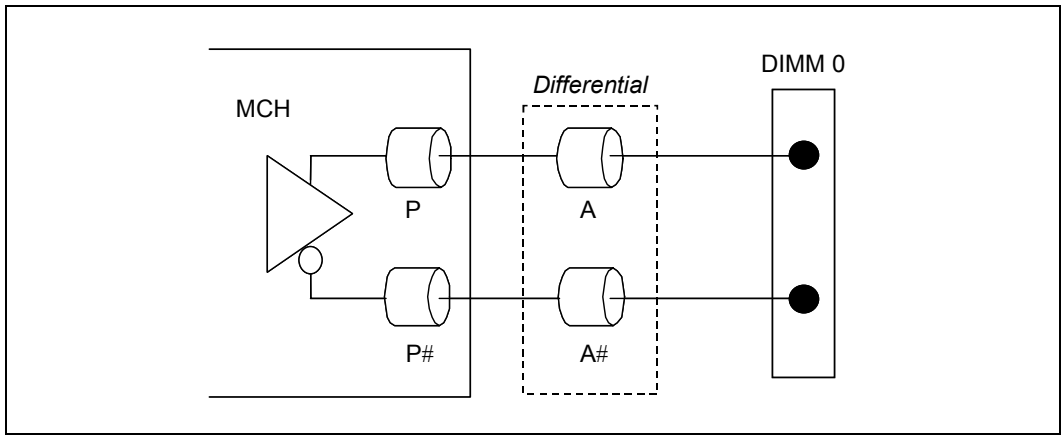


Figure 7-7. DDR Clock Routing Topology (CMDCLK_x[1,5,7]/CMDCLK_x[1,5,7]#)

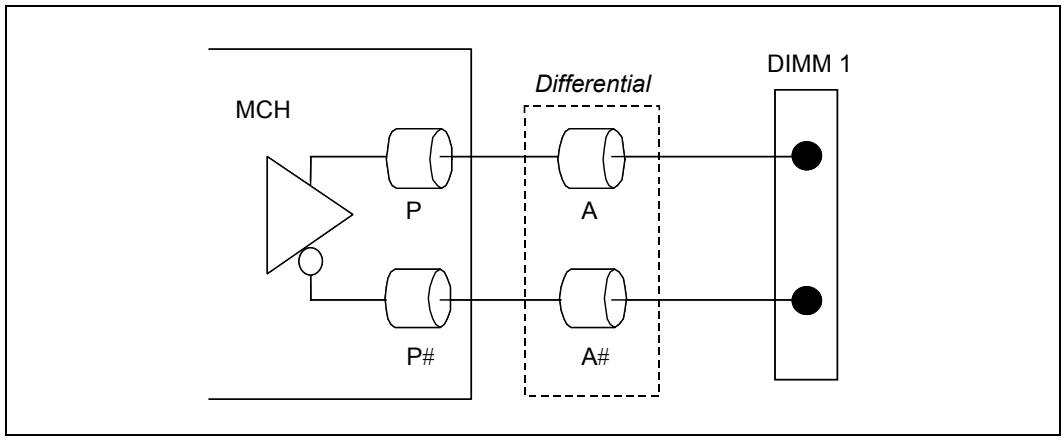
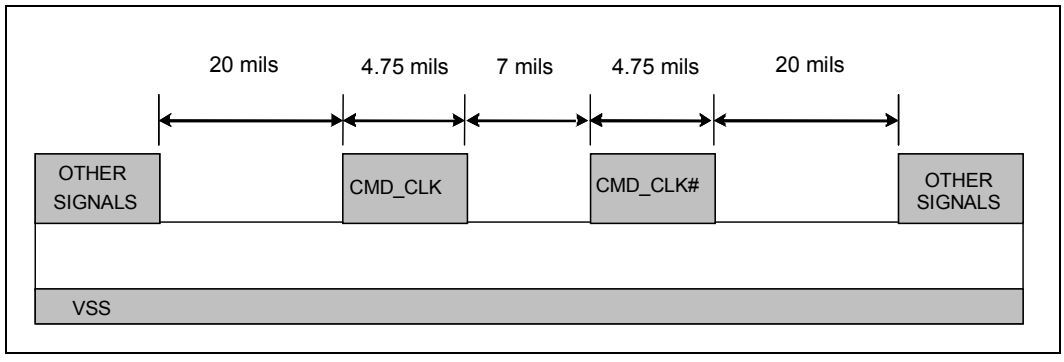


Figure 7-8. Clock Signal Trace Width/Spacing Routing Cross Section



7.3.2.1 Clock Group Signal Length Matching Requirements

The MCH provides three differential clock pair signals for each DIMM. A differential clock pair consists of a CMDCLK signal and its complement signal CMDCLK#. The minimum clock length is dependent on the maximum CS# or CKE length to the corresponding DIMM. In the previous section, it was advised that the CS# and CKE signals be routed as short as possible. Including the MCH internal package lengths in the comparison, the longest CS# or CKE is determined. From this net, the minimum length of the command clocks is determined. The longest net with CS_x[1:0]# and CKE_x[1:0] determines the minimum length of CMDCLK_x[0,4,6], and the longest net within CS_x[3:2]# and CKE_x[3:2] determines the minimum length of CMDCLK_x[1,5,7].

If the longest CKE has a lead-in length of:

≤ 4.0 inches, the minimum CMDCLK length ≥ CKE + 2.0 inches
or
> 4.0 inches, the minimum CMDCLK length ≥ CKE + 2.5 inches

If the longest CS# has a lead-in length of:

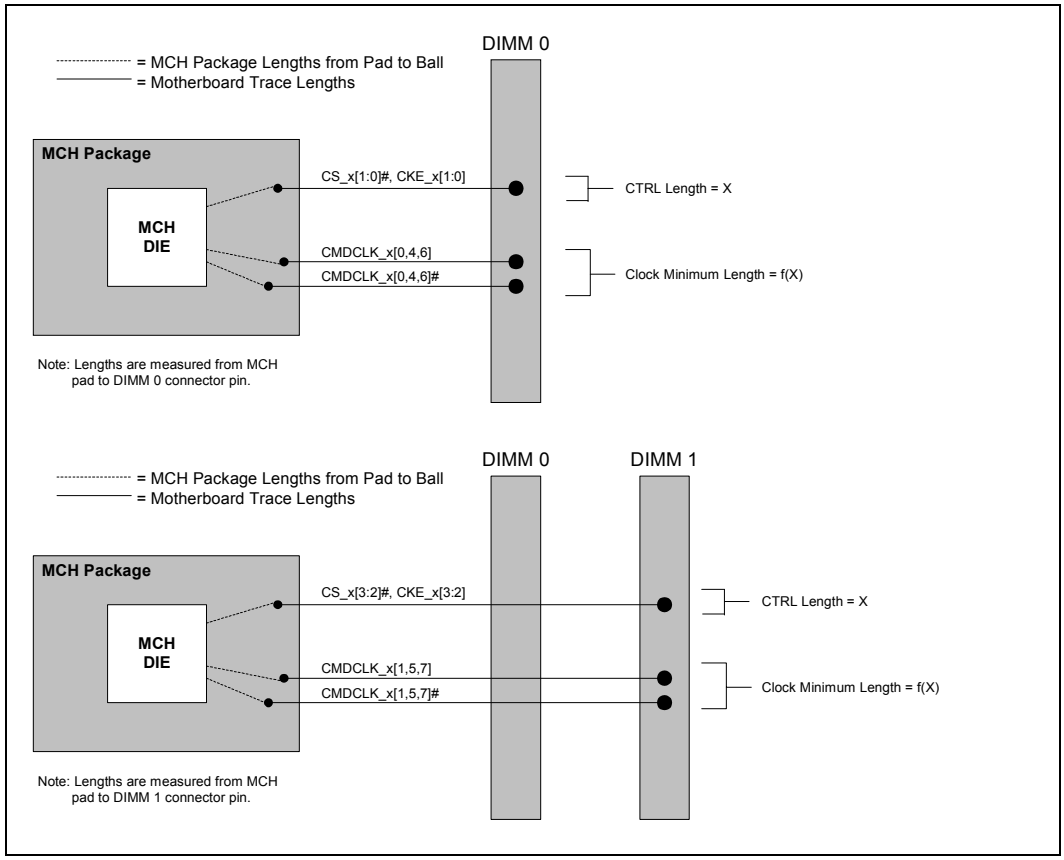
≤ 3.5 inches, the minimum CMDCLK length ≥ CS + 1.0 inch
or
3.5 – 5.0 inches, the minimum CMDCLK length ≥ CS + 1.5 inches
or
> 5.0 inches, the minimum CMDCLK length ≥ CS + 2.0 inches

It is important to include the MCH internal package lengths in these equations and length comparisons. It's equally important to compare the CS# and CKE lengths after the previous equations have been applied to determine the minimum command clock length. For instance, a CS# length of 2 inches and a CKE length of 1.9 inches would suggest the CS# signal would create the longest minimum command clock length requirement. After applying the equations, the CS# length would require a minimum clock length of 3 inches (2 inches + 1 inches), and the CKE length would require a minimum clock length of 3.9 inches (1.9 inches + 2.0 inches). In this case, the shorter CKE signal actually requires a longer minimum command clock length.

From the equations it is clear why the CS# and CKE signals must be as short as possible. The maximum control signal length drives the command clocks to be longer. This requires the data and strobe signals to increase in length as well.

Figure 7-9 shows the length matching requirements between the control and clock signals.

Figure 7-9. Control Signal to CMDCLK Trace Length Matching Requirements



CMDCLK and its complement CMDCLK# within each differential clock pair requires exact length matching from the MCH pad to the pins of the DIMM connector.

In addition, clock length matching is required between clock pairs routed to the same DIMM. The differential clock pairs to the first DIMM connector (CMDCLK_x[0,4,6]/CMDCLK_x[0,4,6]#) require exact matching of the trace lengths from MCH internal pad to the pins of the first DIMM connector. The differential clock pairs for the second DIMM connector (CMDCLK_x[1,5,7]/ CMDCLK_x[1,5,7]#) require exact matching of the trace lengths from MCH internal pad to the pins of the second DIMM connector.

CMDCLK_x0 = CMDCLK_x0# = CMDCLK_x4 = CMDCLK_x4# = CMDCLK_x6 = CMDCLK_x6#

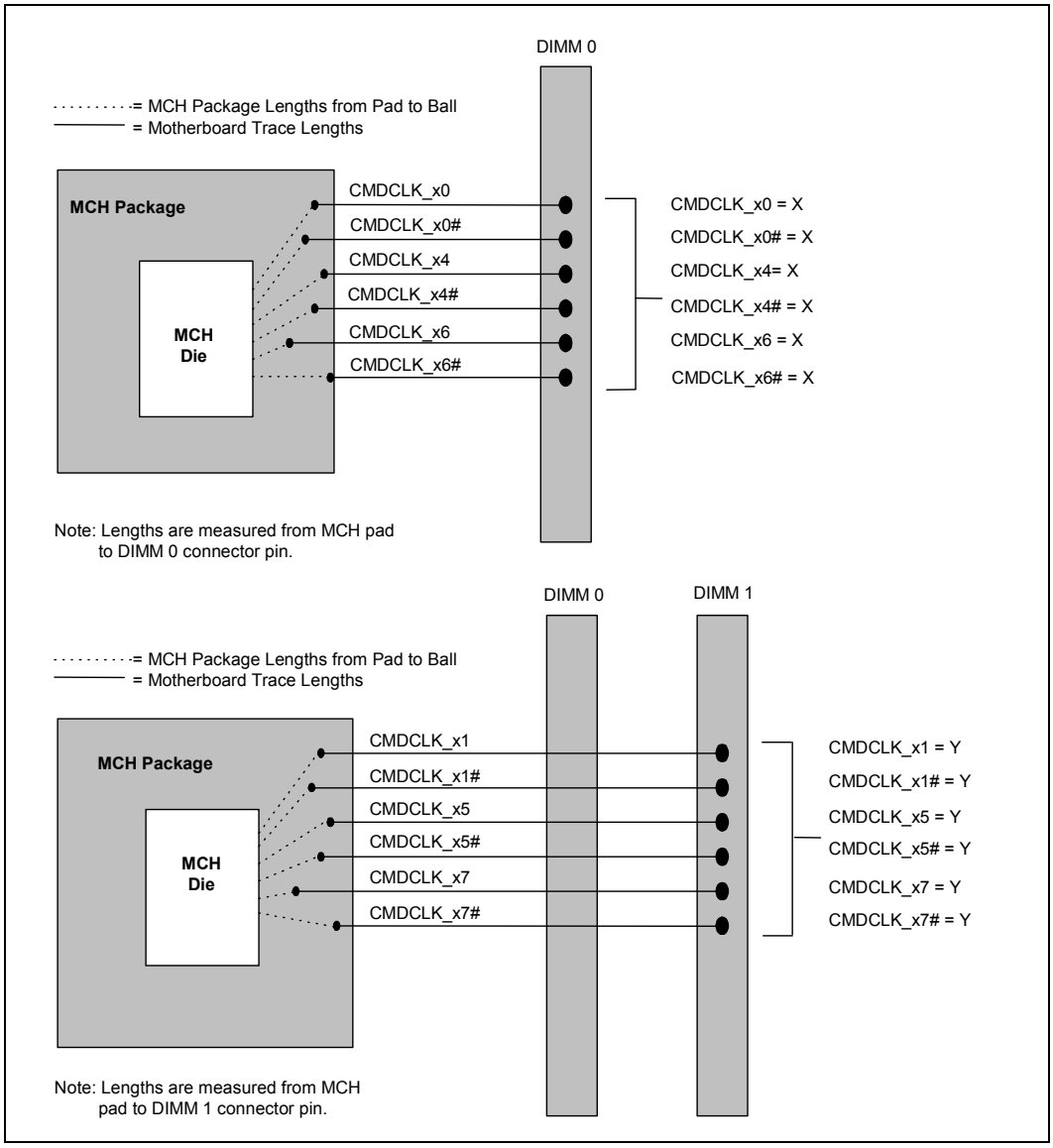
and

CMDCLK_x1 = CMDCLK_x1# = CMDCLK_x5 = CMDCLK_x5# = CMDCLK_x7 = CMDCLK_x7#

The length of the CMDCLK and its complement to first and second DIMM include the MCH package length + the motherboard trace length. The internal package trace lengths are listed in the *Intel® E7505 Chipset Memory Controller Hub (MCH) Datasheet*.

Figure 7-10 shows the length matching requirements for the differential clock signals.

Figure 7-10. CMDCLK to CMDCLK# Trace Length Matching Requirements



7.3.3 DIMM RESET# Signal Implementation

Intel® E7505 chipset-based systems that use registered memory must derive the DIMM RESET# signal from the ICH4 PWR_GOOD signal.

7.3.4 Data Signals — DQ_x[63:0], DQS_x[17:0], CB_x[7:0]

The MCH data signals are source synchronous signals that include the 64-bit wide data bus, 8 check bits, and 18 data strobe signals. DQS_x[17:9] are needed only for x4 devices that are unique to registered memory. Only x8 and x16 devices are available in an unbuffered design. Therefore, DQS_x[17:9] should be left floating at the MCH and grounded at the DIMM. Table 7-6 summarizes the DQ/CB to DQS mapping.

Table 7-6. Signals and Associated Strobe

Signal	Associated Strobe
DQ_x[7:0]	DQS_x0
DQ_x[15:8]	DQS_x1
DQ_x[23:16]	DQS_x2
DQ_x[31:24]	DQS_x3
DQ_x[39:32]	DQS_x4
DQ_x[47:40]	DQS_x5
DQ_x[55:48]	DQS_x6
DQ_x[63:56]	DQS_x7
CB_x[7:0]	DQS_x8

It is important to note that the DQ and CB signals must be length matched only to their associated DQS in board etch length – package compensation does not have to be considered. The DQSs and DQ/CBs must match in length only from the MCH ball to DIMM pin. However, the strobe signals (DQS) must package compensate when determining their minimum length relative to the command clocks. The following sections provide more information on the length tuning method.

Resistor packs are acceptable for the parallel (R_{TT}) data and data strobe termination resistors, but data and strobe signals should not be routed to the same R_{TT} resistor pack (RPACK) used by address/command, or control signals.

Table 7-7, Figure 7-11, and Figure 7-12 show the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Note: It is important to note that the data/strobe groups require a “mixed impedance” topology. The lead-in length from the MCH to the first DIMM is a lower impedance than the segment connecting the first DIMM to the second DIMM and continuing to the termination resistor.

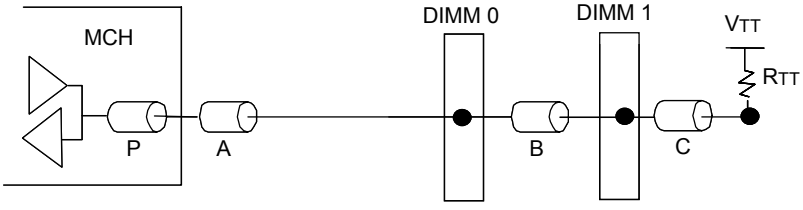
The variables in the figure are:

P = MCH package trace from silicon to the package ball
A = Board trace from the ball of the MCH to the first DIMM pin
B = Board trace from the first DIMM to the second DIMM pin
C = Board trace from the second DIMM pin to the termination resistor pin

Table 7-7. Data Signal Group Routing Guidelines

Parameter	Routing Guidelines	Reference
Signal Group	DQ_x[63:0], CB_x[7:0], DQS_x[8:0]	
Topology	Daisy Chain	Figure 7-11
Reference Plane	Ground Referenced Stripline	
Characteristic Trace Impedance (Zo)	A = 45 Ω, B = C = 55 Ω ± 10%	Figure 7-11 Figure 7-12
Nominal Trace Width	A = 6 mils B = C = 4 mils	Figure 7-11 Figure 7-12
Nominal Trace Spacing	MCH to first DIMM = 15 mils Within DIMM Pin Field = 7 mils minimum From DIMM to DIMM = 15 mils Second DIMM to R_{TT} = 15 mils minimum	Figure 7-12
Group Spacing	15 mils minimum from non-DDR related signals	Figure 7-12
Trace Length A – MCH Ball to first DIMM Pin	Min = 1.0 inch Max = 6.0 inches	Figure 7-11
Trace Length B – DIMM Pin to DIMM Pin	Min = 1.1 inches Max = 1.2 inches	Figure 7-11
Trace Length C – Last DIMM Pin to Parallel termination Resistor Pad	Min = 0.4” Max = 1.2”	Figure 7-11
Termination Resistor (R_{TT})	39 Ω ± 5%	Figure 7-11
MCH Breakout Guidelines	5-mil width / 5-mil spacing for a max length of 500 mils. This length should be minimized	
Length Tuning Method	See Section 7.3.4.1.2 for strobe to clock relationship. See Section 7.3.4.1.1 for data to strobe relationship.	

Figure 7-11. Data Signal Routing Topology



NOTE: The variables in the figure are:

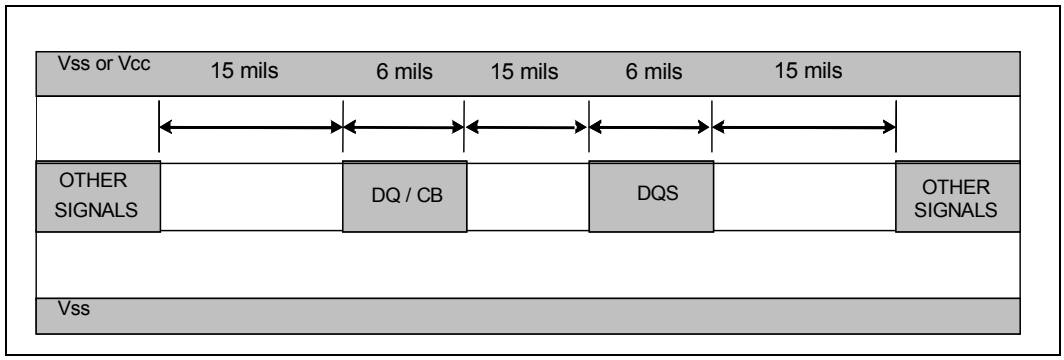
P = MCH package trace from silicon to the package ball

A = Board trace from the ball of the MCH to the first DIMM pin

B = Board trace from the first DIMM to the second DIMM pin

C = Board trace from the second DIMM pin to the termination resistor pin

Figure 7-12. Data Group Signal Trace Width/Spacing Routing on Lead-in Length Only



7.3.4.1 Data Group Signal Length Matching Requirements

7.3.4.1.1 Strobe to Command Clock Length Matching Requirements

The tuning of strobe and differential clock signals must take into account the package lengths internal to the MCH package. Matching requires tuning from the MCH internal pad to the pins of the DIMM connector for strobe to the differential clock signals.

CMDCLK_x/CMDCLK_x# Length = X
then the minimum DQS length = Y
where Y ≥ X - 3.0 inches

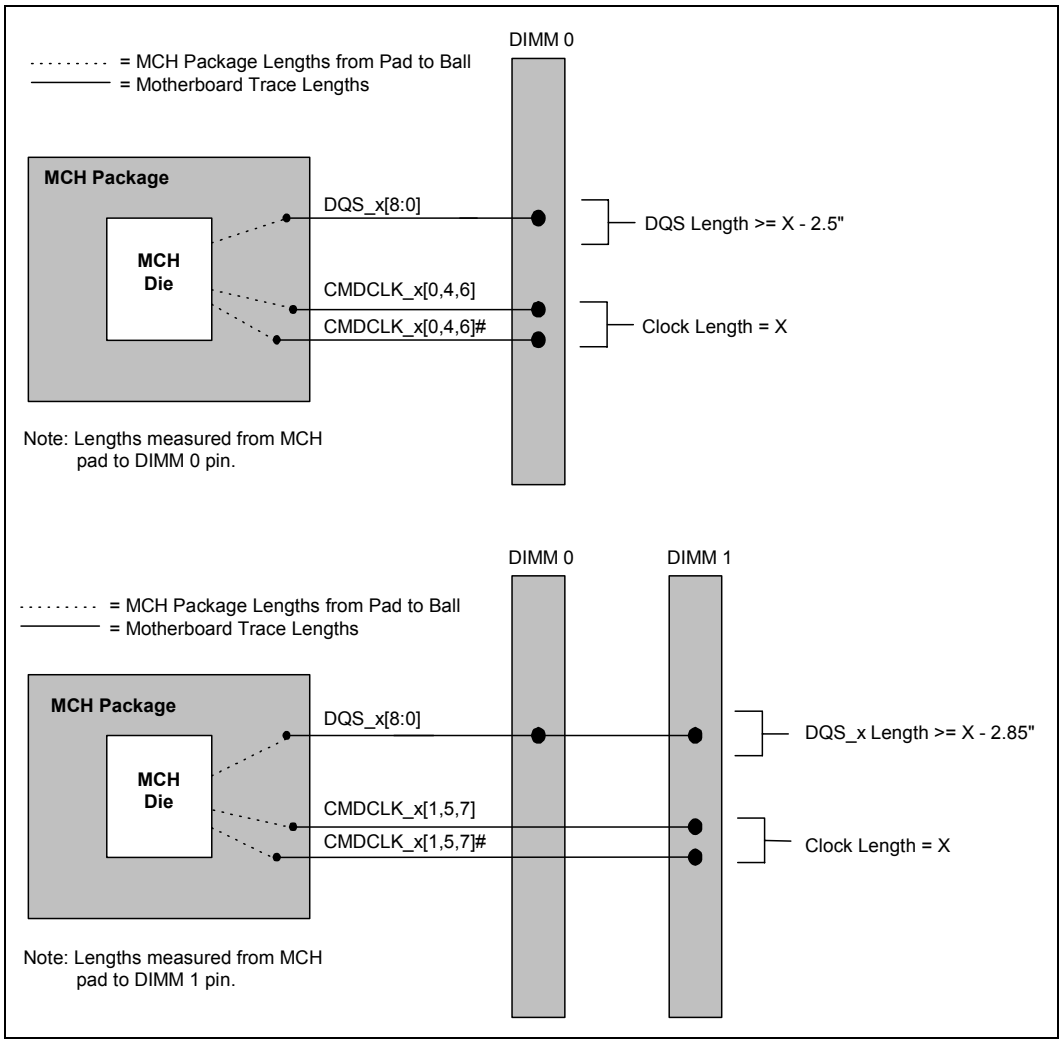
Length X and Y to the first and second DIMM includes the MCH package length + the motherboard trace length from the ball of the MCH to the DIMM. No length matching is required from the second DIMM to the parallel termination resistors. Refer to the length matching spreadsheet that provides MCH internal package lengths.

Notes:

1. CMDCLK_x[0,4,6] governs the length range of DQS_x[8:0] signals at DIMM0.
2. CMDCLK_x[1,5,7] governs the length range of DQS_x[8:0] signals at DIMM1.
3. The length of DQS at DIMMs 0 and 1 must still meet the lead-in length and DIMM to DIMM length requirements outlined in Table 7-7.

Figure 7-13 shows the length matching requirements between the DQS and clock signals.

Figure 7-13. DQS to CMDCLK/CMDCLK# Trace Length Matching Requirements



7.3.4.1.2 Data to Strobe Length Matching Requirements

The tuning of the data strobes to the associated data and check bit signals does not have to take package length compensation into account. It is required that the strobes use package compensation when determining the required lengths relative to the command clocks as described in the previous section. However, length matching of the strobe to its associated data and check bits must account only for the board etch. For instance, a command clock length to the first DIMM of 8 inches would require that the strobe length to the first DIMM have a minimum length of 5 inches (8 inches –3 inches) from die pad to DIMM. If DQS_x0 has 500 mils of internal package length, the board etch must be 4.5 inches. The eight signals, DQ_x[7:0], would then have to be routed to 4.5 inches and do not require package compensation.

The length relationship between data and check bit signals to the associated strobe is:

DQS Length = X,

Associated DQ/CB Byte Group Length = Y,

(X - 25 mils) ≤ Y ≤ (X + 25 mils)

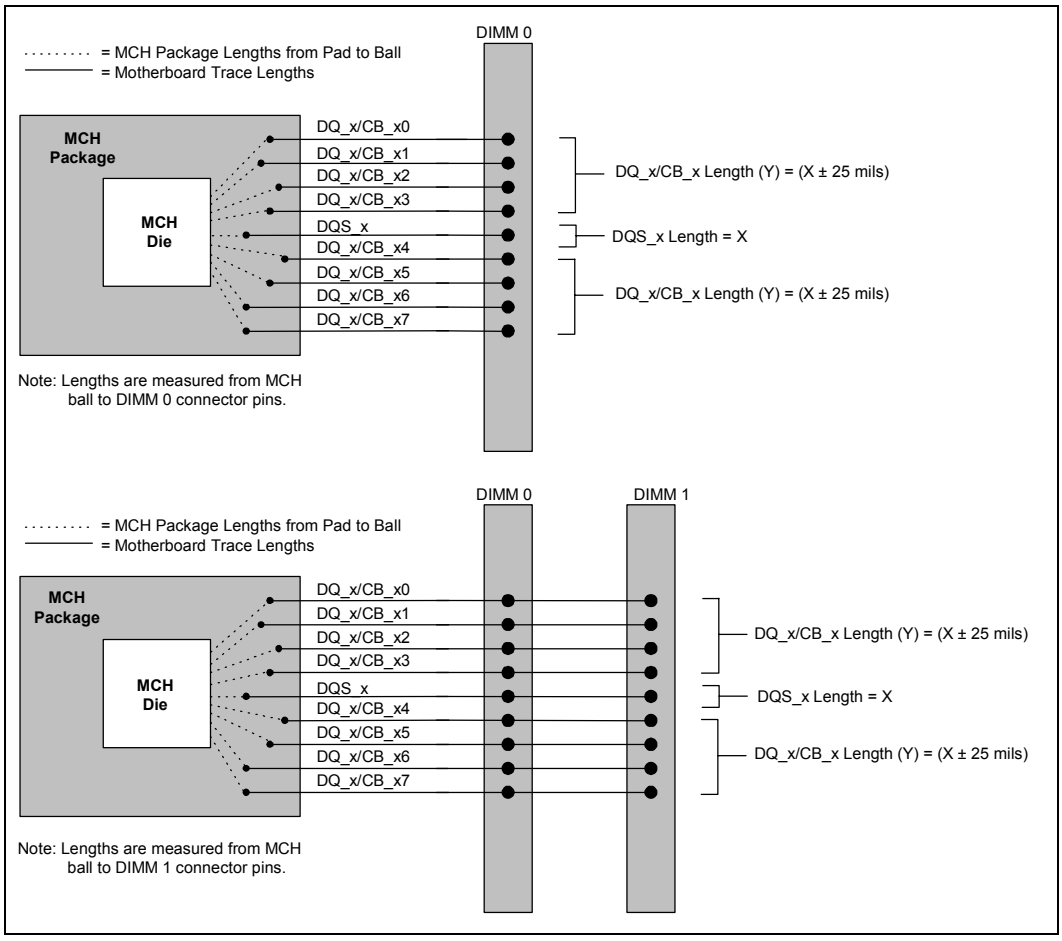
Length X and Y to first and second DIMM do not include the MCH package length, only the motherboard trace length. No length matching is required from the second DIMM to the parallel termination resistors.

Table 7-8 and Figure 7-14 describe the length matching requirements between the DQ, CB, and DQS signals. It is important to note that the ± 25 mils tolerance must be divided between the segment from the MCH to the first DIMM, and the first DIMM to the second DIMM. For instance, a designer may use ± 15 mils of tolerance on the lead-in length to the first DIMM, and use ± 10 mils on the DIMM to DIMM segment. This ensures that the overall ± 25 mils requirement is met. If the ± 25 mils tolerance were used on each segment individually, a data signal's length could theoretically be out specification by 25 mils at the second DIMM. The division of the tolerance is arbitrary, but allowing more lenience on the lead-in length is typically the easiest from a routing standpoint.

Table 7-8. DQ/CB to DQS Length Matching Mapping

Signals	Length Mismatch	Relative to
DQ_x[7:0]	± 25 mils	DQS_x0
DQ_x[15:8]	± 25 mils	DQS_x1
DQ_x[23:16]	± 25 mils	DQS_x2
DQ_x[31:24]	± 25 mils	DQS_x3
DQ_x[39:32]	± 25 mils	DQS_x4
DQ_x[47:40]	± 25 mils	DQS_x5
DQ_x[55:48]	± 25 mils	DQS_x6
DQ_x[63:56]	± 25 mils	DQS_x7
CB_x[7:0]	± 25 mils	DQS_x8

Figure 7-14. DQ/CB to DQS Length Matching



7.3.5 Address/Command Signals — MA_x[13:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#

The MCH address/command signals are source-clocked signals that include 14 system memory address signals (MA_x[13:0]), 2 bank addresses (BA), row address select (RAS_x#), column address select (CAS_x#), and write enable (WE_x#). The address/command signals are “clocked” into the DIMMs using the positive edge of the differential clock signals.

Resistor packs are acceptable for the parallel (R_{TT}) address/command termination resistors, but address/command signals cannot be routed to the same resistor pack (RPACK) used by data and/ or data strobe signals.

There is a required length relationship between the command clocks and the address/command signals but the requirement is usually met through normal routing without extra consideration.

Table 7-9, Figure 7-15, and Figure 7-16 describe the recommended topology and layout routing guidelines for the DDR-SDRAM address/command signals.

Figure 7-15. Address/Command Signal Routing Topology

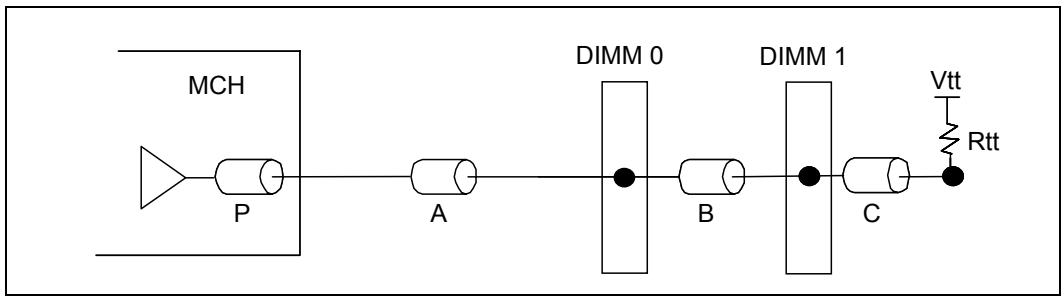
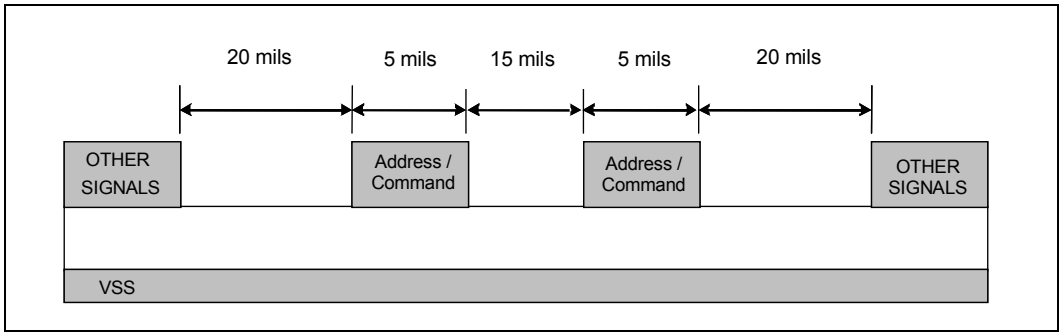


Table 7-9. Address/Command Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	MA_x[13:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#
Topology	Daisy chain
Reference Plane	Ground Referenced Microstrip
Characteristic Trace Impedance (Zo)	A, B, C = 55 Ω ± 10%
Nominal Trace Width	A, B, C = 5 mils
Nominal Trace Spacing from MCH	MCH to first DIMM = 15 mils minimum Within DIMM Pin Field = 7 mils minimum From DIMM to DIMM = 15 mils minimum Second DIMM to R_{TT} = 15 mils minimum
Group Trace Spacing	20 mils from non-DDR related signals
Trace Length A – MCH Signal Ball to DIMM pin	Min = 1.5 inches Max = 6.0 inches
Trace Length B – DIMM pin to DIMM pin	Min = 1.1 inches Max = 1.2 inches
Trace Length C – Last DIMM pin to parallel termination resistor pad	Min = 0.1 inch Max = 1.2 inches
Termination Resistor (R_{TT})	56 Ω ± 5%
MCH Breakout Guidelines	5-mil width / 5-mil spacing for a max length of 500 mils. This length should be minimized.
Length Tuning Method	See Section 7.3.5.1 for details.

Figure 7-16. Address/Command Signal Width/Spacing Routing on Lead-in Length



7.3.5.1 Address/Command Group Signal Length Matching Requirements

The tuning of the address/command signals (MA_x[13:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#) and differential clock signals must take into account the internal package lengths of the MCH package. Matching requires tuning of the address/command signals to the differential clock signals from the MCH pad to the pins of the DIMM connector. The differential clock should be routed at least 1.0 inch longer than the longest address/command signal (MA_x[13:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#) to the associated DIMM.

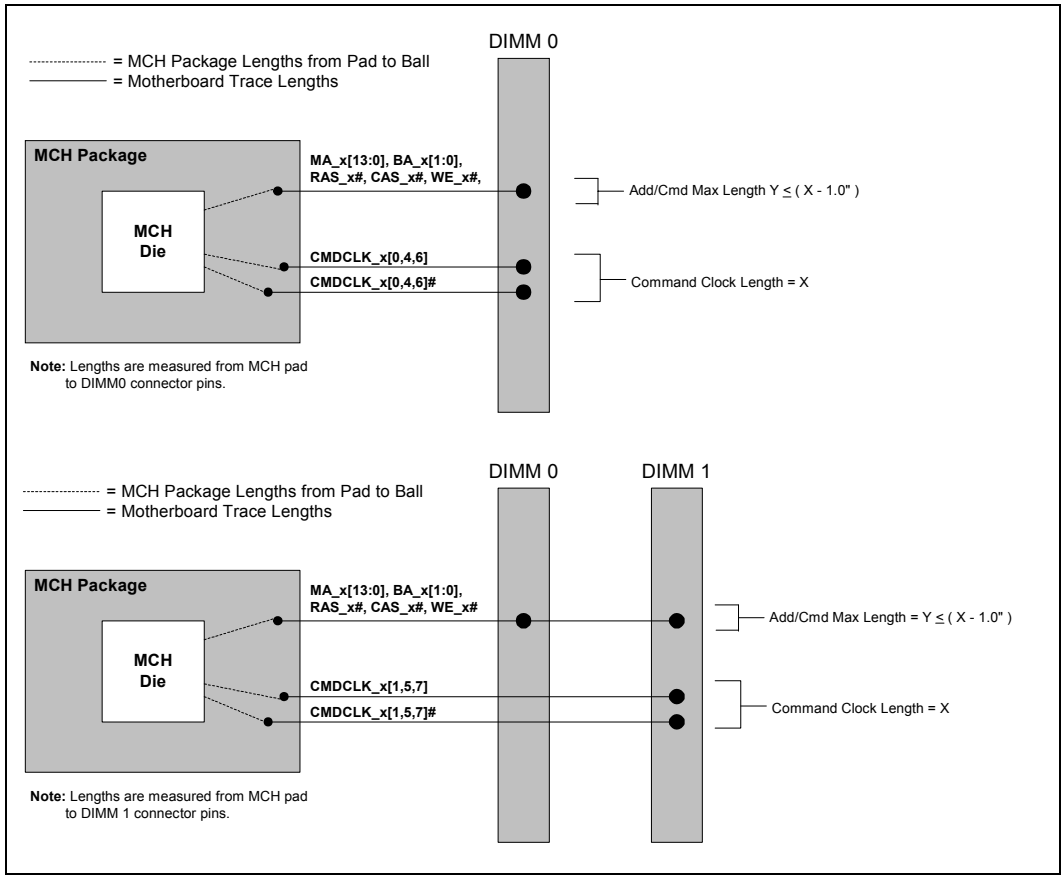
CMDCLK/CMDCLK# Length = X,

Associated Address / Command Length = Y,

where Y ≤ X - 1.0 inch

Length X and Y to first and second DIMM include the MCH package length + the motherboard trace length A. While the equations set the boundary conditions, the length requirements can usually be met without extra consideration because the address/command signals routed usually fall short of the maximum length requirement naturally. No length matching is required from the DIMM to the parallel termination resistors. Figure 7-17 shows the length matching requirements between the address/command signals and the clock signals.

Figure 7-17. Address /Command Signal to CMDCLK Trace Length Matching Requirements



7.4 Registered DDR System Memory Topology and Layout Design Guidelines

This section contains information and details on the registered DDR topologies, layout, and routing guidelines. The guidelines are provided for each corresponding signal group: Data, Address/ Command, Control, Feedback, Clock. In a registered memory configuration, the E7505 chipset will support three DIMMs per channel. (Note that the unbuffered configuration supports two DIMMs per channel.)

Based on the eight-layer stack-up described previously, the MCH system memory ball field, and the fact that all DDR signals must be ground referenced, the following DDR-SDRAM system memory guidelines should be followed in an E7505 chipset-based system.

7.4.1 Data Signals — DQ_x[63:0], DQS_x[17:0], CB_x[7:0]

The MCH data signals are source synchronous signals that include the 64-bit wide data bus, 8 check bits, 18 data strobe signals. DQS_x[17:9] are needed only for x4 devices that are unique to registered memory. Because registered memory modules may use x4 devices, it is important to route the DQS_x[17:9] signals to the DIMMs, while in an unbuffered only design the signals are unused. Table 7-10 summarizes DQ/CB to DQS mapping.

Table 7-10. DQ/CB to DQS Mapping

Data Group	Associated Strobe(1)
DQ_x[7:0]	DQS_x0, DQS_x9
DQ_x[15:8]	DQS_x1, DQS_x10
DQ_x[23:16]	DQS_x2, DQS_x11
DQ_x[31:24]	DQS_x3, DQS_x12
DQ_x[39:32]	DQS_x4, DQS_x13
DQ_x[47:40]	DQS_x5, DQS_x14
DQ_x[55:48]	DQS_x6, DQS_x15
DQ_x[63:56]	DQS_x7, DQS_x16
CB_x[7:0]	DQS_x8, DQS_x17

NOTE:

1. In x4 configurations, the high DQS is associated with the high nibble, and the low DQS is associated with the low nibble. In x8 configurations, only the low DQS is used.

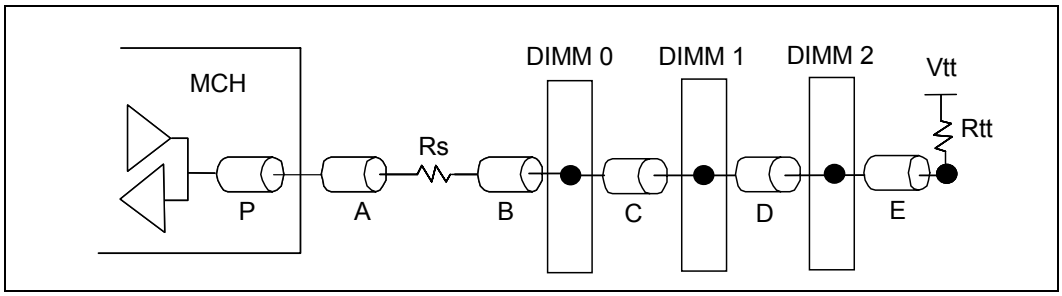
It is important to match the DQ/CB signals to their associated DQS from MCH ball to DIMM pin. Refer to Section 7.4.1.1 for more information on length matching. With the stack-up described previously, one channel of data/strobes is routed entirely on layer 3, and the second channel's data/ strobes is routed entirely on layer 6.

Table 7-11 and Figure 7-18 and Figure 7-19 describe the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Table 7-11. Data Signal Group Routing Guidelines

Parameter	Routing Guidelines	Reference
Signal Group	DQ_x[63:0], CB_x[7:0], DQS_x[17:0]	
Topology	Daisy chain	Figure 7-18
Reference Plane	Ground Referenced	
Characteristic Trace Impedance (Zo)	A = B = 45 Ω C = D = E = 55 Ω ± 10%	Figure 7-18
Nominal Trace Width	A = B = 6 mils C = D = E = 4 mils	Figure 7-19
Nominal Trace Spacing	MCH to first DIMM = 15 mils Within DIMM Pin Field = 7 mils minimum From DIMM to DIMM = 15 mils Last DIMM to R_{TT} = 15 mils minimum	Figure 7-19
Group Spacing	20 mils minimum from non-DDR related signals	Figure 7-19
Total lead-in trace length (sum of A and B) – MCH signal ball to first DIMM pin	Min = 2.0 inches Max = 5.0 inches	Figure 7-18
Trace Length B – Series Termination Resistor (R_S) Pad to first DIMM Pin	Min = 500 mills Max = 700 mils	Figure 7-18
Trace Length C and D – DIMM Pin to DIMM Pin	Min = 1.1 inches Max = 1.2 inches	Figure 7-18
Trace Length E – Last DIMM Pin to Parallel termination Resistor Pad	Min = 0.1 inch Max = 0.8 inches	Figure 7-18
Series Resistor (R_S)	Min = 4.7 Ω ± 5% Max = 10 Ω ± 5%	Figure 7-18
Termination Resistor (R_{TT})	Min = 33 Ω ± 5% Max = 39 Ω ± 5%	Figure 7-18
MCH Breakout Guidelines	5-mil width / 5-mil spacing for a max length of 500 mils. This length should be minimized	
Length Tuning Method	See Section 7.4.1.1 for details.	

Figure 7-18. Data Signal Routing Topology



NOTE: The variables in the figure are:

P = MCH package trace from silicon to the package ball

A = Board trace from the ball of the MCH to the series resistor pin

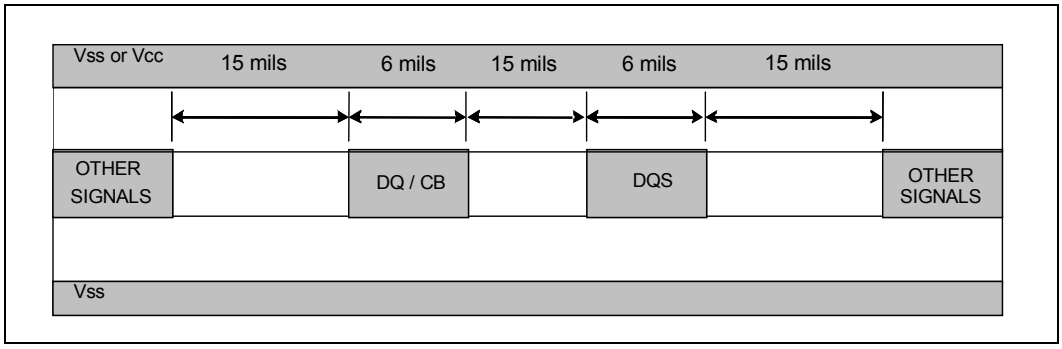
B = Board trace from the series resistor to the first DIMM pin

C = Board trace from the first DIMM to the second DIMM pin

D = Board trace from the second DIMM to the third DIMM pin

E = Board trace from the third DIMM pin to the termination resistor pin

Figure 7-19. Data Group Signal Trace Width/Spacing Routing on Lead-in Length



7.4.1.1 Data Group Signal Length Matching Requirements

7.4.1.1.1 Data to Strobe Length Matching Requirements

The tuning of data/check bits (DQ_x[63:0], CB_x[7:0]) and data strobe (DQS_x[17:0]) signals requires tuning from the MCH ball to the DIMM connector pins. The data and check bit signals must length match the associated data strobe within each byte group.

DQS Length = X,

Associated DQ/CB Byte Group Length = Y,

$(X - 25 \text{ mils}) \leq Y \leq (X + 25 \text{ mils})$

Lengths X and Y to first DIMM include motherboard trace length A + motherboard trace length B.

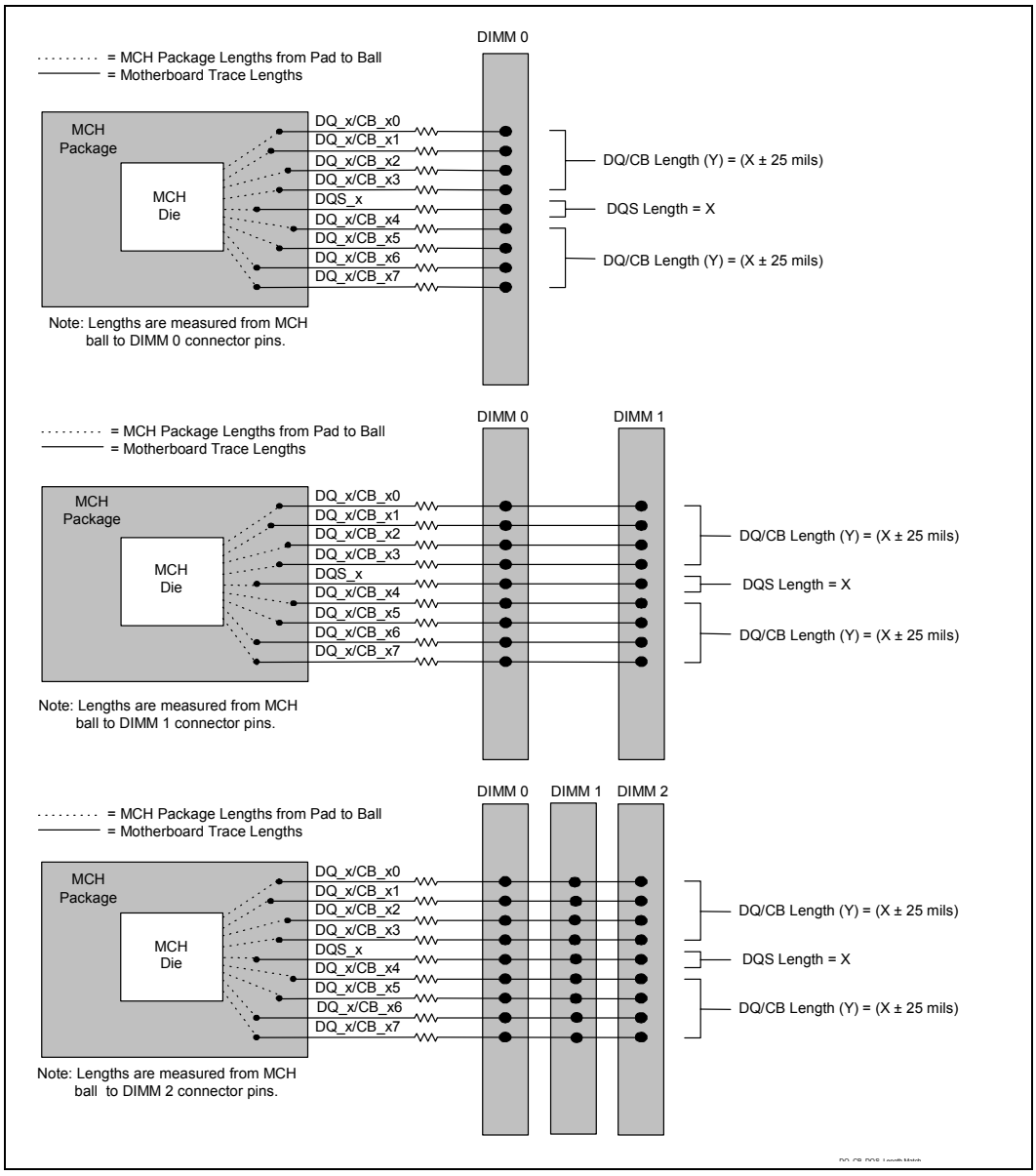
Lengths X and Y to second DIMM include motherboard trace length A + motherboard trace length B + motherboard trace length C. Lengths X and Y to the third DIMM include motherboard trace lengths A, B, C and D. Data and strobe trace length guidelines for lengths A, B, C and D are documented in Table 7-11. No length matching is required from the third DIMM to the parallel termination resistors.

Table 7-12 and Figure 7-20 describe the length matching requirements between the DQ, CB, and DQS signals.

Table 7-12. DQ/CB to DQS Length Matching Mapping

Signals	Length Mismatch	Relative to
DQ_x[7:0]	± 25 mils	DQS_x0 / DQS_x9
DQ_x[15:8]	± 25 mils	DQS_x1 / DQS_x10
DQ_x[23:16]	± 25 mils	DQS_x2 / DQS_x11
DQ_x[31:24]	± 25 mils	DQS_x3 / DQS_x12
DQ_x[39:32]	± 25 mils	DQS_x4 / DQS_x13
DQ_x[47:40]	± 25 mils	DQS_x5 / DQS_x14
DQ_x[55:48]	± 25 mils	DQS_x6 / DQS_x15
DQ_x[63:56]	± 25 mils	DQS_x7 / DQS_x16
CB_x[7:0]	± 25 mils	DQS_x8 / DQS_x17

Figure 7-20. DQ/CB to DQS Length Matching



For registered memory, the required clock length is specified at an absolute length. Therefore, as long as the min and max DQS lengths are observed in Table 7-16, there is no DQS to CMDCLK length requirement.

7.4.2 Control Signals — CS_x[7:0]#

In a registered memory configuration, the MCH provides eight chip select (CS#) signals. These control signals are “clocked” into the DIMMs using the positive edge of the differential clock signals. In a three registered DIMM per channel configuration, only six chip selects are required — two for each DIMM.

In the unbuffered memory section, only four CS# signals were detailed. The extra chip selects for a registered configuration are gained through the multiplexing capabilities of the CMDCLK_x[7:6]/ CMDCLK_x[7:6]# pins. Table 7-13 describes the multiplexing of the CMDCLK_x[7:6]/ CMDCLK_x[7:6]# signals. Only one chip select (CS#) is needed for each DDR-SDRAM physical DIMM device row.

Table 7-13. CMDCLK and CS Multiplexing

MCH Pin Number	2 DIMM per Channel	3 DIMM per Channel
AG8	CMDCLK_A6	CS_A5#
AG9	CMDCLK_A6#	CS_A4#
AJ6	CMDCLK_A7	CS_A7#
AJ7	CMDCLK_A7#	CS_A6#
AH7	CMDCLK_B6	CS_B5#
AH8	CMDCLK_B6#	CS_B4#
AK5	CMDCLK_B7	CS_B7#
AK6	CMDCLK_B7#	CS_B6#

Two chip selects are routed to each DIMM (one for each side) to support double-sided DDR DIMMs. Table 7-14 summarizes the CS# to DIMM pin mapping. Note that CS_x[7:6]# may be left unconnected at the MCH because they are not used in an E7505 chipset platform.

Table 7-14. Control Signal DIMM Mapping

Signal	Relative To	DIMM Pin
CS_x0#	DIMM0	157
CS_x1#	DIMM0	158
CS_x2#	DIMM1	157
CS_x3#	DIMM1	158
CS_x4#	DIMM2	157
CS_x5#	DIMM2	158

Resistor packs are acceptable for the parallel (R_{TT}) control termination resistors, but the control signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, or address/ command signals.

Table 7-15 and Figure 7-21 through Figure 7-24 describe the recommended topology and layout routing guidelines for the DDR-SDRAM control signals that are connected to the first and second DIMM.

Table 7-15. Control Signal Group Routing Guidelines

Parameter	Routing Guidelines	Reference
Signal Group	CS_x#	
Topology	Point to point	Figure 7-23
Reference Plane	Ground Referenced Microstrip	
Characteristic Trace Impedance (Zo)	A = B = 50 ± 10%	Figure 7-24
Nominal Trace Width	A = B = 6 mils	
Nominal Trace Spacing	MCH to each DIMM = 15 mils minimum Within DIMM Pin Field = 7 mils minimum Within DIMM to DIMM = 15 mils minimum Second DIMM to R_{TT} = 15 mils minimum	Figure 7-24
Group Spacing	Isolation spacing from non-DDR related signals = 20 mils	Figure 7-24
Trace Length A (CS_x[1:0]#) – MCH Signal Ball to DIMM Pins on first DIMM	Min = 5.1 inches Max = 7.1 inches	Figure 7-21
Trace Length A (CS_x[3:2]#) – MCH Signal Ball to DIMM Pins on second DIMM	Min = 8.1 inches Max = 10.1 inches	Figure 7-22
Trace Length A (CS_x[5:4]#) – MCH Signal Ball to DIMM Pins on third DIMM	Min = 9.8 inches Max = 11.8 inches	Figure 7-23
Trace Length B (CS_x[5:0]#) – DIMM pins on first, second, or third DIMM to R_{TT} Pad	Min = 0.1 inches Max = 1.5 inches	Figure 7-23
Termination Resistor (R_{TT})	Min = 39 Ω ± 5% Max = 47 Ω ± 5%	Figure 7-21 Figure 7-22 Figure 7-23
MCH Breakout Guidelines	5-mil width / 5-mil spacing for a max length of 500 mils. This length should be minimized	

Figure 7-21. DIMM-0 Control Signal Routing Topology (CS_x[1:0]#)

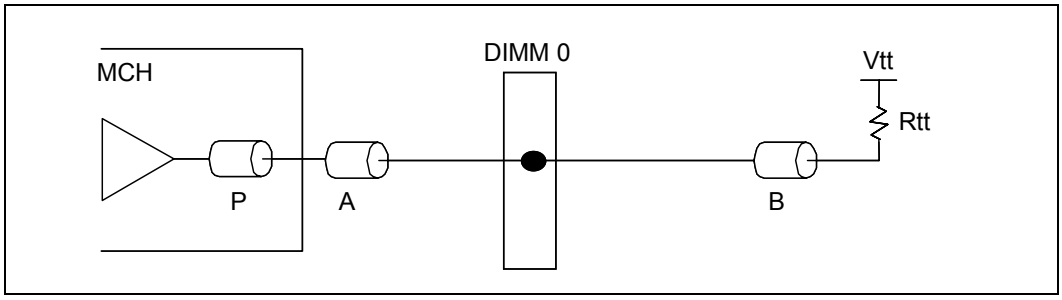


Figure 7-22. DIMM-1 Control Signal Routing Topology (CS_[3:2]#)

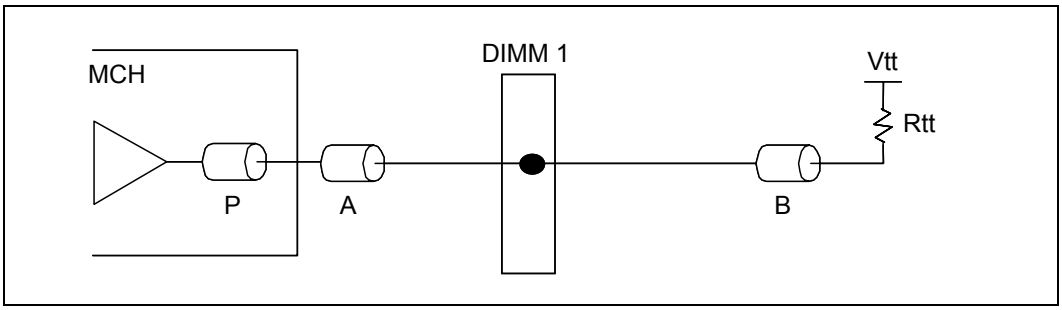


Figure 7-23. DIMM-2 Control Signal Routing Topology (CS_[5:4]#)

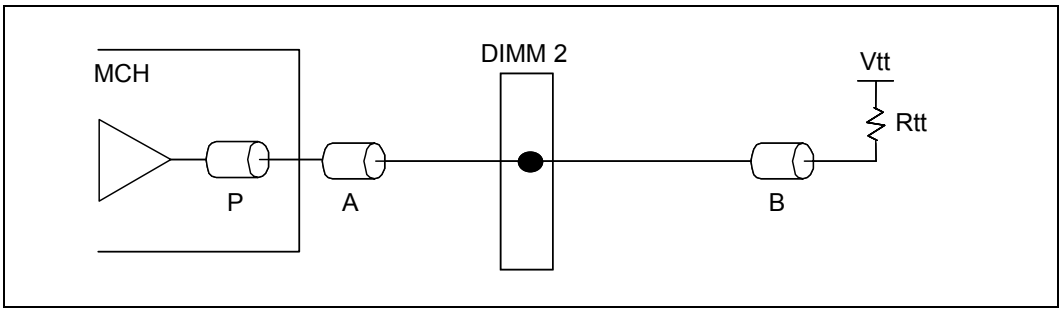
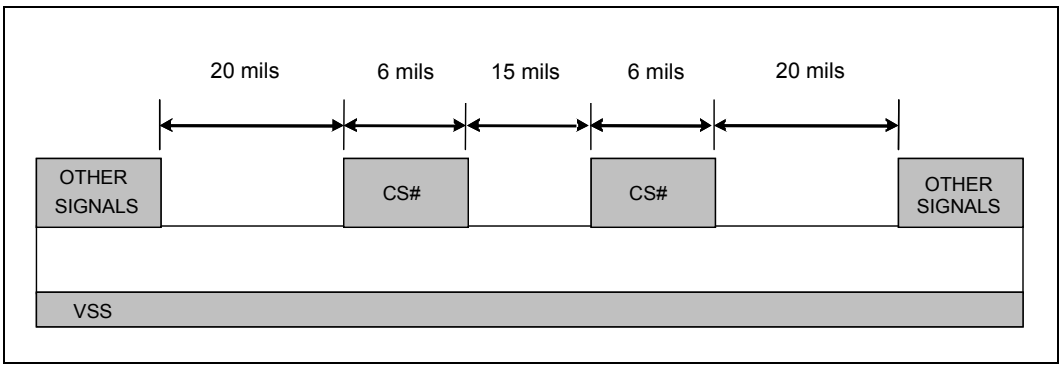


Figure 7-24. Control Signal Trace Width/Spacing Routing on Lead-in Length



7.4.2.1 Control Group Signal Length Matching Requirements

For registered memory configurations, the clock length is specified as an absolute length. Therefore, as long as the min and max CS# lengths in Table 7-15 are observed, there is no CS# to CMDCLK length requirement.

7.4.3 Address, Command, and CKE Signals — MA_x[13:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#, CKE_x[3:0]

The MCH address/command signals are source-clocked signals that include 14 system memory address signals (MA_x[13:0]), 2 bank addresses (BA), row address select (RAS_x#), column address select (CAS_x#), and write enable (WE_x#), as well as the CKE signals. In an unbuffered memory configuration, the CKE signals' topology matches the chip select topology, point to point. In a registered configuration, the CKE signals are routed the same as the address/command signals' topology, daisy-chained.

The address/command signals are "clocked" into the DIMMs using the positive edge of the differential clock signals. The MCH drives the address/command and clock signals together.

Only two of the four CKE signals are needed for a registered solution—CKE_x0 and CKE_x1 can connect to the CKE_x0 and CKE_x1 of all three registered DIMMs. CKE_x[3:2] are not used. Table 7-16 summarizes the CKE to DIMM and DIMM pin mapping.

Table 7-16. Control Signal DIMM Mapping

Signal	Relative To	DIMM Pin
CKE_x0	DIMM0	21
CKE_x1	DIMM0	111
CKE_x0	DIMM1	21
CKE_x1	DIMM1	111
CKE_x0	DIMM2	21
CKE_x1	DIMM2	111

Resistor packs are acceptable for the parallel (R_{TT}) address/command termination resistors, but address/command signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, or control signals.

Table 7-17, Figure 7-25, and Figure 7-26 describe the recommended topology and layout routing guidelines for the DDR-SDRAM address/command signals.

Figure 7-25. Address/Command Signal Routing Topology

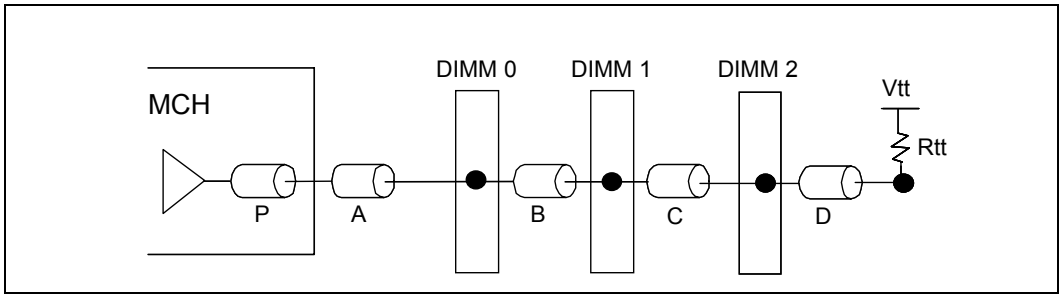
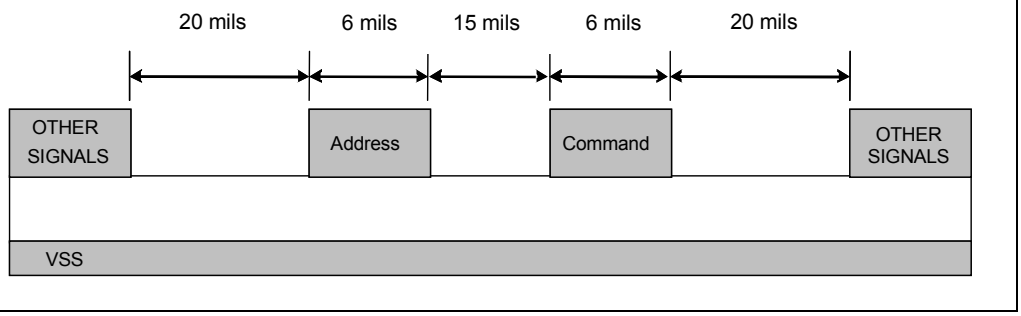


Table 7-17. Address/Command Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	MA_x[13:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#, CKE_x[1:0]
Topology	Daisy chain
Reference Plane	Ground Referenced Microstrip
Characteristic Trace Impedance (Zo)	A = B = C = D = 50 Ω ± 10%
Nominal Trace Width	A = B = C = D = 6 mils
Nominal Trace Spacing from MCH	MCH to first DIMM = 15 mils Within DIMM Pin Field = 7 mils minimum From DIMM to DIMM = 15 mils Second DIMM to R_{TT} = 15 mils minimum
Group Spacing	Isolation spacing from non-DDR related signals = 20 mils
Serpentine Spacing	20 mils minimum
Trace Length A – MCH Signal Ball to DIMM1 Pin	Min = 2.0 inches Max = 5.0 inches
Trace Length B – DIMM Pin to DIMM Pin	Min = 1.1 inches Max = 1.2 inches
Trace Length C – DIMM Pin to DIMM Pin	Min = 1.1 inches Max = 1.2 inches
Trace Length D – Last DIMM Pin to Parallel Termination Resistor Pad	Min = 0.1 inch Max = 0.8 inches
Termination Resistor (R_{TT})	Min = 39 Ω ± 5% Max = 47 Ω ± 5%
MCH Breakout Guidelines	5-mil width / 5-mil spacing for a max length of 500 mils. This length should be minimized

Figure 7-26. Address/Command Signal Width/Spacing Routing on Lead-in Length



7.4.3.1 Address/Command Group Signal Length Matching Requirements

For registered DDR, the clock length is specified at an absolute length. Therefore, as long as the min and max Address/Command/CKE lengths in Table 7-17 are observed, there is no CMDCLK length matching requirement.

7.4.4 Clock Signals — CMDCLK_x[5:0], CMDCLK_x[5:0]#

In a three registered DIMM per channel design, the MCH provides six differential clock pairs: CMDCLK_x[5:0] and CMDCLK_x[5:0]#. Of these pairs, CMDCLK_x[5:3]/CMDCLK_x[5:3]# can be left floating because only three clock pairs are required (1 pair per slot). The MCH generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. The differential clock pairs are routed to each DIMM connector. Table 7-18 summarizes the clock signal mapping.

Table 7-18. Clock Signal Mapping

Clock Signal Mapping	Routed To
CMDCLK_x0 / CMDCLK_x0#	DIMM0
CMDCLK_x1 / CMDCLK_x1#	DIMM1
CMDCLK_x2 / CMDCLK_x2#	DIMM2
CMDCLK_x[5:3] / CMDCLK_x[5:3]#	No Connect

The differential clock pairs must be routed differentially from the MCH pad to their associated DIMM pins and must maintain the correct isolation spacing from other signals. When the signals serpentine, it is important to maintain the minimum spacing to other DDR signals. While serpentining, the differential clock pair must maintain correct spacing to remain differential as well. Table 7-19 summarizes a typical clock signal-to-DIMM pin mapping on an E7505 chipset DDR platform.

Table 7-19. DDR Clock Signal DIMM Pin Mapping

Signal	Relative To	DIMM Pin
CMDCLK_x0	DIMM0	137
CMDCLK_x0#	DIMM0	138
CMDCLK_x1	DIMM1	137
CMDCLK_x1#	DIMM1	138
CMDCLK_x2	DIMM2	137
CMDCLK_x2#	DIMM2	138

There are no external termination resistors required for the clock signals. Table 7-20 and Figure 7-27 through Figure 7-30 describe the recommended topology and layout routing guidelines for the DDR-SDRAM differential clocks.

Table 7-20. Clock Signal Group Routing Guidelines

Parameter	Routing Guidelines	Reference
Signal Group	CMDCLK_x[2:0]/CMDCLK_x[2:0]#	
Topology	Point-to-point	Figure 7-27 Figure 7-28 Figure 7-29
Reference Plane	Ground Referenced	
Characteristic Trace Impedance (Zo)	Differential = 100 Ω ± 10%	
Nominal Trace Width	4.75 mils	Figure 7-30

Table 7-20. Clock Signal Group Routing Guidelines

Parameter	Routing Guidelines	Reference
Differential Trace Spacing	7 mils	Figure 7-30
Group Spacing	20 mils minimum from any other DDR signal group 20 mils minimum from any non-DDR signal group	Figure 7-30
Serpentine Spacing	20 mils minimum	
Trace Length A (CMDCLK_x0/CMDCLK_x0#) – MCH Signal Ball to pin of first DIMM	Min = Max = 6.1 inches ± 10 mils	Figure 7-27
Trace Length A (CMDCLK_x1/CMDCLK_x1#) – MCH Signal Ball to pin of second DIMM	Min = Max = 9.1 inches ± 10 mils	Figure 7-28
Trace Length A (CMDCLK_x2/CMDCLK_x2#) – MCH Signal Ball to pin of third DIMM	Min = Max = 10.8 inches ± 10 mils	Figure 7-29
MCH Breakout Guidelines	5-mil width / 5-mil spacing for a max length of 500 mils. This length should be minimized	
Length Tuning Method	Note: Package length matching from MCH internal die pad to DIMM connector pin is required for CMDCLK/CMDCLK#. CMDCLK length must match CMDCLK# length	

Figure 7-27. DDR Clock Routing Topology (CMDCLK_x0/CMDCLK_x0#)

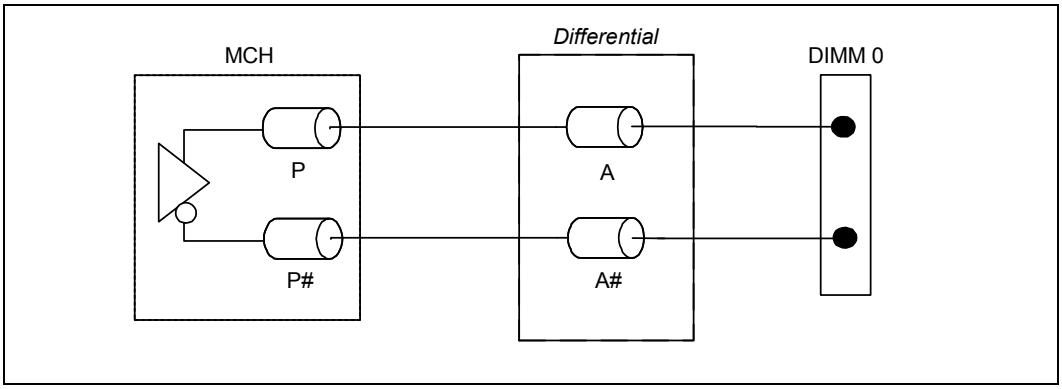


Figure 7-28. DDR Clock Routing Topology (CMDCLK_x1/CMDCLK_x1#)

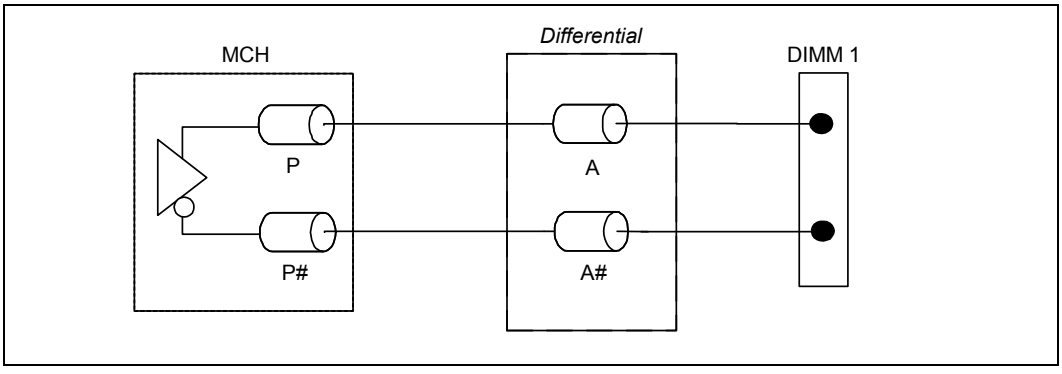


Figure 7-29. DDR Clock Routing Topology (CMDCLK_x1/CMDCLK_x1#)

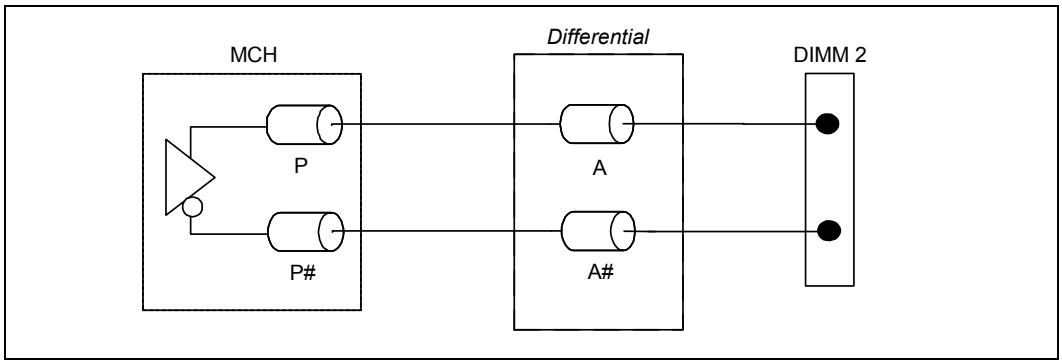
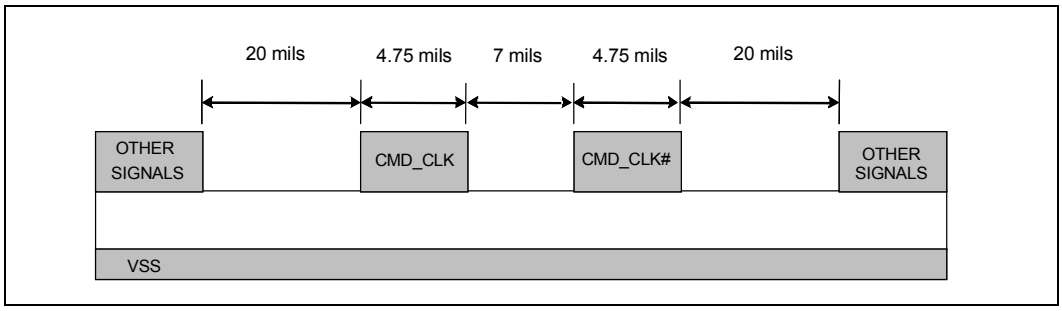


Figure 7-30. Clock Signal Trace Width/Spacing Routing Cross Section



7.4.4.1 Clock Group Signal Length Matching Requirements

For registered DDR, the clock length is specified at an absolute length. The MCH provides three differential clock pair signals for each DIMM. A differential clock pair consists of a CMDCLK signal and its complement signal CMDCLK#. CMDCLK and its complement CMDCLK# within each differential clock pair requires exact length matching from MCH die to the pins of the DIMM connector. The clock pair has been length matched on the E7505 chipset package so die to DIMM length matching is maintained when the board route lengths are matched.

Length of CMDCLK_x0 = Length of CMDCLK_x0#
Length of CMDCLK_x1 = Length of CMDCLK_x1#
Length of CMDCLK_x2 = Length of CMDCLK_x2#

7.5 DC Biasing

7.5.1 RCVENOUT_A#, RCVENOUT_B#

The MCH provides two pins called RCVENOUT_A# and RCVENOUT_B#. This provides a RCVENOUT# signal for both memory channels. This signal provides timing/synchronization information to the MCH. The signal must be tied to a resistor divider between the 2.5 V rail and ground. The high and low side resistor values are shown in Figure 7-31. It is important that the two signals pins do not share a single resistor divider even though the recommended circuit is identical for both. Figure 7-31 and Table 7-21 describe the recommended topology and layout routing guidelines for the RCVENOUT# signal.

Figure 7-31. DDR Feedback RCVENOUT_A#, RCVENOUT_B# Routing Topology

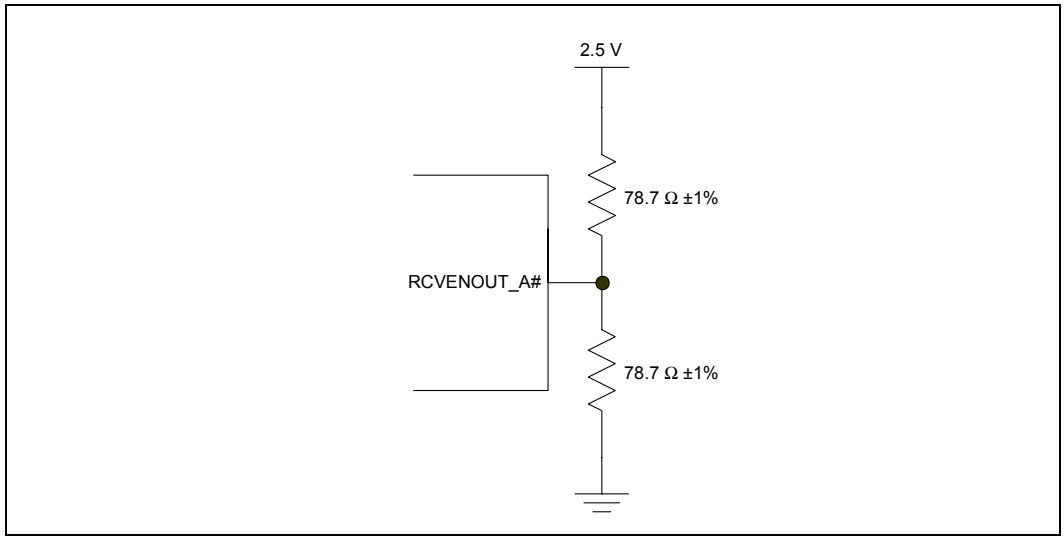


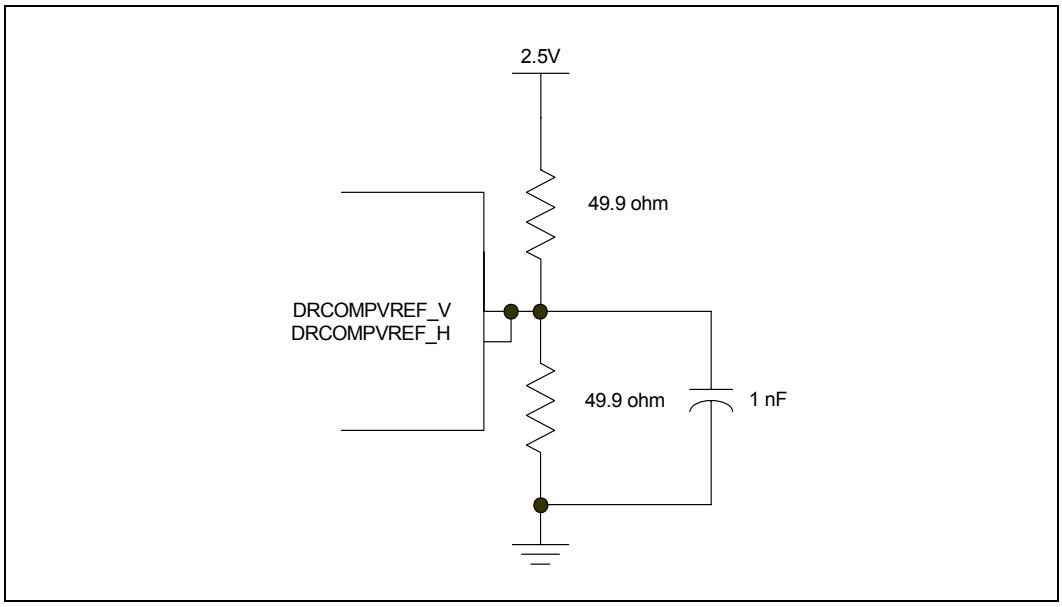
Table 7-21. RCVEN_OUT_A#, RCVENOUT_B# Routing Guidelines

Parameter	Routing Guidelines
Signal Group	RCVENOUT#
Topology	Point to point with resistor divider
Nominal Trace Width	6 mils
Max Trace Length to Resistor Divider	Minimize

7.5.2 DRCOMPVREF_H, DRCOMPVREF_V

The MCH provides signals DRCOMPVREF_H and DRCOMPVREF_V for voltage referencing. DRCOMPVREF_H and DRCOMPVREF_V are used for both channel A and B, and are used as voltage referencing for the horizontal and vertical buffer resistive compensation circuitry. The DRCOMPVREF_H and DRCOMPVREF_V signals can be shorted together and tied to a single resistor divider network. The routing topology and values for the biasing circuitry are described in Figure 7-32 and Table 7-22.

Figure 7-32. DRCOMPVREF_H, DRCOMPVREF_V Routing Topology



NOTE: The capacitor in the figure is 1 nanoFarad.

Table 7-22. DRCOMPVREF_H, DRCOMPVREF_V Routing Guidelines

Parameter	Routing Guidelines
Signal Group	DRCOMPVREF_H, DRCOMPVREF_V
Topology	Point-to-point with resistor divider
Nominal Trace Width	20 mils
Max Trace Length to Resistor Divider	Minimize

7.5.3 VREF_A, VREF_B

VREF_A and VREF_B are addressed in Section 7.7.4.

7.5.4 DRCOMP_H, DRCOMP_V

The MCH provides two signals for resistive compensation. The DRCOMP_H and DRCOMP_V signals are used to calibrate the horizontal and vertical DDR buffers, respectively. It is important that these signals do not share biasing circuitry. The individual signal must tie to its own individual resistor that ties to ground. The routing topology and values for the biasing circuitry and are described in Figure 7-33 and Table 7-23.

Figure 7-33. DRCOMP_H, DRCOMP_V Routing Topology

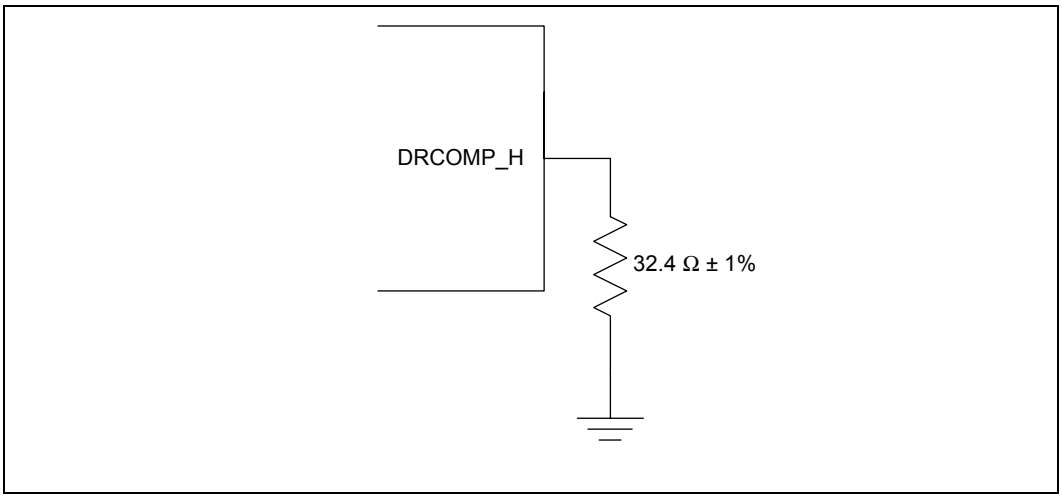


Table 7-23. DRCOMP_H, DRCOMP_V Routing Guidelines

Parameter	Routing Guidelines
Signal Group	DRCOMP_H, DRCOMP_V
Topology	Point-to-point with pull-down resistor
Reference Plane	Ground referenced
Characteristic Trace Impedance (Zo)	50 Ω ± 10%
Nominal Trace Width	6 mils
Max Trace Length to Resistor Divider	Minimize

7.5.5 DDR_STRAP

The MCH provides a signal that is used to indicate to the BIOS what type of memory is used in the motherboard. This signal should be grounded on a motherboard that uses registered DDR DIMMs. It should be tied to 2.5 V on a motherboard that uses unbuffered DDR DIMMs. Figure 7-34 and Figure 7-35 show the topologies.

Figure 7-34. DDR_STRAP Routing Topology (Unbuffered DIMMs)

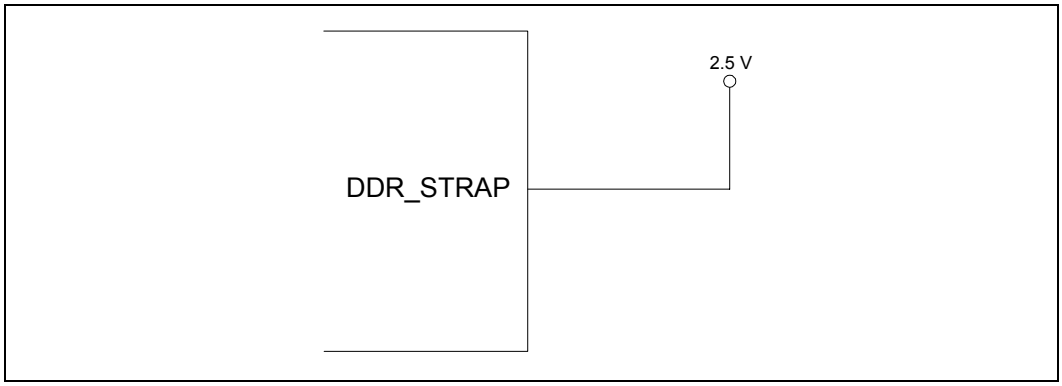


Figure 7-35. DDR_STRAP Routing Topology (Registered DIMMs)

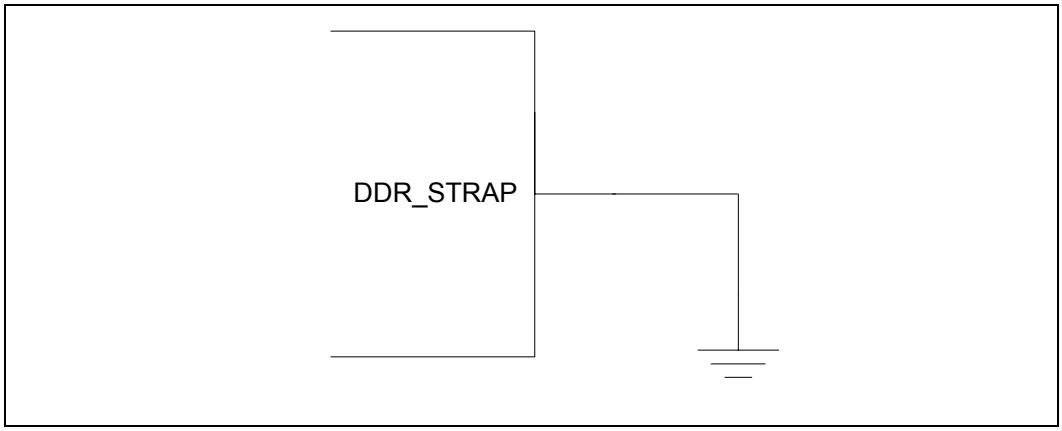


Table 7-24. DDR_STRAP Routing Guidelines

Parameter	Routing Guidelines
Signal Group	DDR_STRAP
Topology	Pull-up or pull-down
Nominal Trace Width	6 mils

7.5.6 ODTCOMP

The MCH provides a signal that is used to tune the on-die termination resistors on the DDR interface. This signal should be tied to a resistor to ground. Figure 7-36 shows the topology and resistor value.

Figure 7-36. ODTCOMP Routing Topology

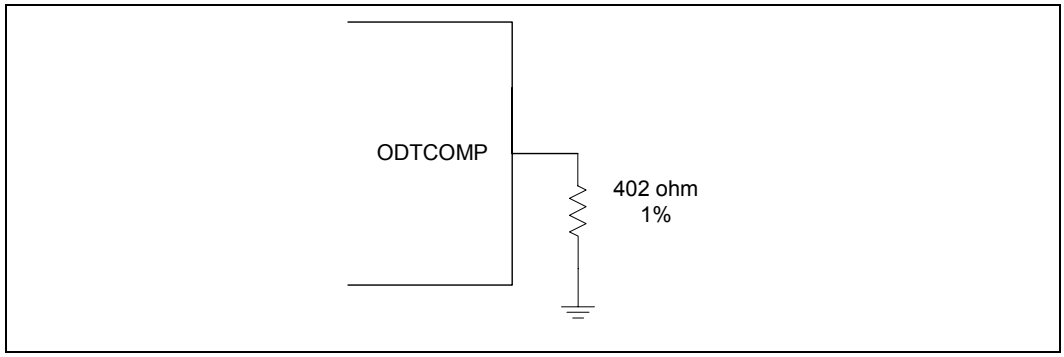


Table 7-25. ODTCOMP Routing Guidelines

Parameter	Routing Guidelines
Signal Group	ODTCOMP
Topology	Point-to-point with pull-down resistor
Reference Plane	Ground referenced
Characteristic Trace Impedance (Zo)	50 Ω ± 10%
Nominal Trace Width	6 mils
Max Trace Length to Resistor Divider	Minimize

7.6 System Memory Bypass Capacitor Guidelines

7.6.1 MCH System Memory Interface Decoupling Requirements

7.6.1.1 MCH System Memory High-Frequency Decoupling

Every MCH ground and power ball in the system memory interface should have its own via. For 2.5 V high-frequency decoupling, a minimum of ten 0603 0.1 µF high-frequency capacitors are required and must be located within 100 mils of the MCH package. The vias should be placed within 25 mils of the capacitor pads. The traces from the ground and power vias to the capacitor pad must be as wide as possible. Figure 7-37 show MCH DDR 2.5 V high-frequency decoupling .

Figure 7-37. MCH DDR 2.5 V Decoupling Picture

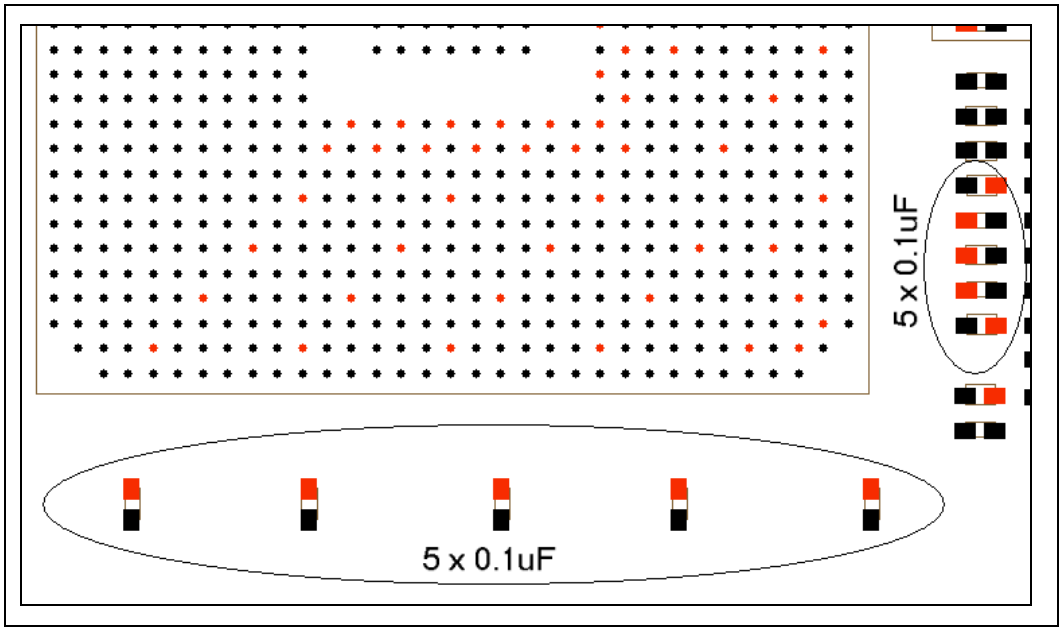


Table 7-26. MCH System Memory Decoupling Capacitor Requirements

Parameter	Guideline
Capacitor number	Ten 0603 0.1 µF MLC capacitors placed near MCH (see Figure 7-37)
Capacitor placement	Within 100 mils of the MCH
Capacitor pad to ground via trace width	Route as wide as possible with a minimum width of 18 mils
Vias (Power and Ground)	Placed within 25 mils of the capacitor pad

7.6.1.2 MCH System Memory Low-Frequency Bulk Decoupling

The MCH system memory interface requires low-frequency bulk decoupling. Place two 100 µF electrolytic capacitors and one 22 µF capacitor between the MCH and the first DIMM connector. These capacitors are in addition to the bulk decoupling required by the 2.5 V regulator (regulator bulk decoupling is design specific).

Figure 7-38. Shared MCH/DIMM 2.5 V Bulk Decoupling Example

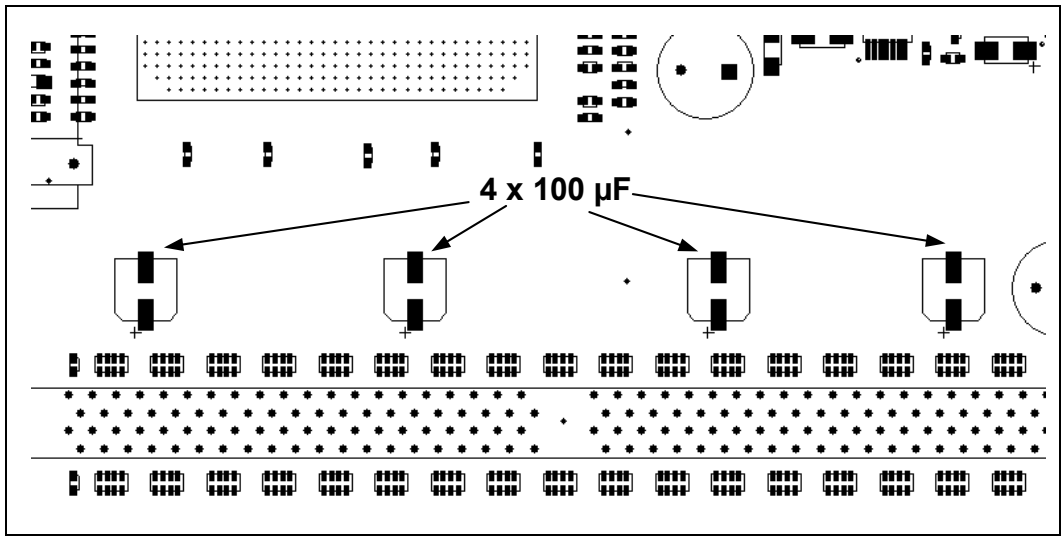


Table 7-27. MCH System Memory Bulk Capacitor Requirements

Parameter	Guideline
Capacitor number	Four 100 µF capacitors (see Figure 7-38)
Capacitor placement	Evenly placed between the MCH and first DIMM pin

7.6.2 DDR-DIMM Decoupling Requirements

The DDR DIMMs require bulk decoupling in addition to decoupling that is required by the MCH. Place two more 100 µF capacitors at the upper left corner and the two bottom corners of the DIMM connectors as shown in Figure 7-39.

Figure 7-39. DDR DIMM 2.5 V Bulk Decoupling Example

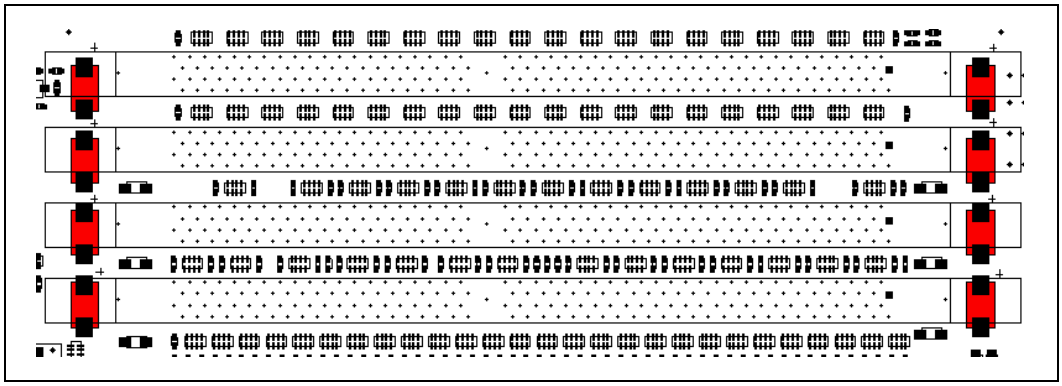


Table 7-28. MCH System Memory Bulk Capacitor Requirements

Parameter	Guideline
Capacitor number	Eight 100 µF capacitors (2 per DIMM) (see Figure 7-39)
Capacitor placement	One placed at the upper right side of the DIMM sockets, one at the bottom-left of the DIMM sockets, and one placed at the bottom-right side of the DIMM sockets

7.7 Power Delivery

The following guidelines are recommended for an E7505 chipset DDR system memory design. The main focus of these MCH guidelines is to minimize signal integrity problems and to improve the power delivery of the MCH system memory interface and the DDR-DIMMs.

7.7.1 DDR Voltage Regulator Guidelines

E7505 chipset designs using the DDR-SDRAM memory sub-system require 2.5 V, 1.25 V, and VREF. To generate these voltages, a 2.5 V and a 1.25 V regulator are required and must be designed to supply the required voltage and current levels to meet both the MCH and DDR-SDRAM device requirements. DDR voltage regulation will be governed by either an on-motherboard regulator circuitry or a module with the necessary complement of external capacitance, and will vary according to requirements of specific OEM design targets.

7.7.2 Power Delivery Guidelines for 2.5 V

Attention must be paid to the 2.5 V power plane to ensure proper MCH and DIMM power delivery. This 2.5 V plane must extend from the MCH's 2.5 V power vias to the 2.5 V DDR voltage regulator and its bulk capacitors. The 2.5 V copper plan under the DIMM connectors must encompass all the DIMM 2.5 V pins.

The 2.5 V power plane, which is generated by the 2.5 V regulator, is used to supply power to the MCH 2.5 V I/O Ring, the DDR-SDRAM 2.5 V Core, and the DDR-SDRAM 2.5 V I/O Ring. The 2.5 V regulator should be placed at the end of the DDR channel near the VTT Termination Island.

Platforms implementing S3 mode must provide a 2.5 V-standby supply.

7.7.3 Power Delivery Guidelines for 1.25 V

The 1.25 V power plane, which is generated by the 1.25 V regulator, is used to supply the DDR termination voltage (VTT). Special considerations must be taken for the 1.25 V regulator design because it must be able to source and sink a significant amount of current. The 1.25 V regulator should be placed at the end of the DDR channel near the VTT Termination Island. VTT should track VREF. This is accomplished by connecting the output of the VREF divider to the sense input of the VTT 1.25 V voltage regulator.

7.7.4 DDR Reference Voltage

The DDR system memory reference voltage (VREF) is used by the DDR-SDRAM devices to compare the input signal levels of the data, command, and control signals, and is also used by the MCH to compare the input data signal levels. VREF must be generated as shown in Figure 7-40. It should be generated from a typical resistor divider using 1%-tolerance resistors, with a 0.1 µF cap tied to VREF. The VREF resistor divider should be placed as close to the MCH as possible. Additionally, VREF must be decoupled locally at each DIMM connector. Finally, the VREF signal should be routed with as wide a trace as possible (20 mils suggested), and isolated from other signals with a minimum of 12 mils spacing (during breakout from the MCH a minimum of 5 mil spacing can be maintain for a maximum length of 500 mils).

Figure 7-40. DDR VREF Generation Example Circuit

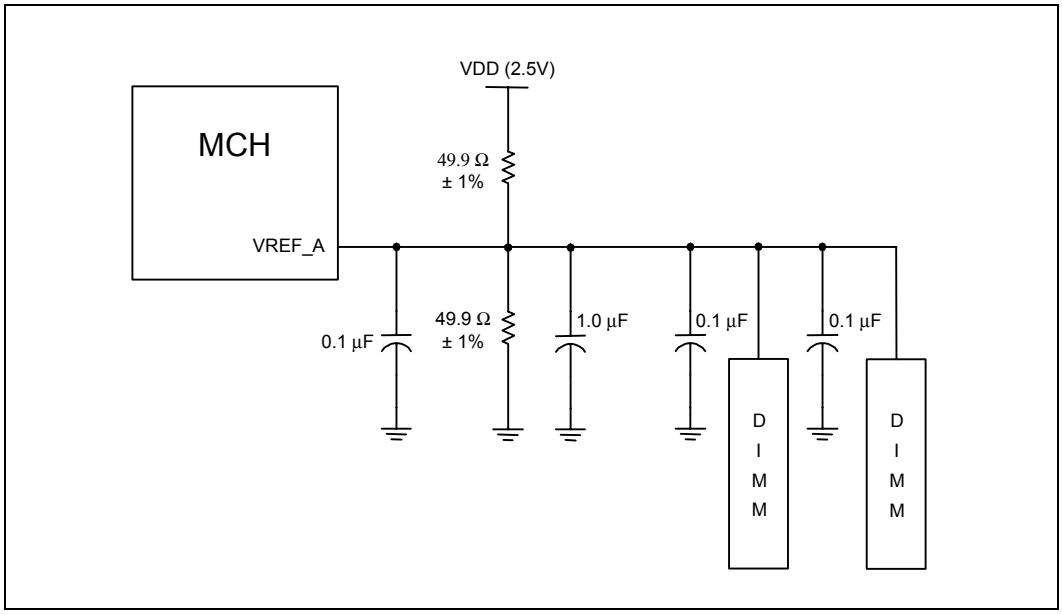


Table 7-29. DDR VREF Generation Requirements

Parameter	Guideline
VREF Routing	Minimum 12 mils wide and separated from other traces with a minimum 12 mils spacing, except during breakout, which is allowed 7 mil spacing to other signals for no more than 350 mils.
Voltage Divider	Place resistor divider consisting of two 49.9 Ω ± 1% resistors. Minimize distance from MCH to resistor divider.
Decoupling Requirements	Three 0603 0.1 µF capacitors One 0603 1.0 µF capacitor
Decoupling Placement	Place one 0.1 µF decoupling cap at each of the DIMM sockets, and one 0.1 µF decoupling cap at the MCH. Place the 1.0 µF decoupling cap near the voltage divider.

7.7.5 DDR VTT Termination

All DDR signals except the command clocks must be terminated to 1.25 V (VTT) using 1% resistors at the end of the channel opposite the MCH. Place a solid 1.25 V (VTT) termination island on the top signal layer surrounding the last 2 DIMM connectors on the board. The size of the island should be approximately 1.3 inches x 6.0 inches. A second VTT island should be placed on Layer 3 around the last DIMM connector, termination resistors, and decoupling caps. The size of this island should also be approximately 1.3 inches x 6.0 inches. Use this termination island to terminate all DDR signals using one resistor per signal. Resistor packs are acceptable, with the understanding that the RPACKs cannot be shared between Data signals and Address/Command/Control signals. The parallel termination resistors connect directly to the VTT islands. Because of space constraints for the Channel A termination RPACKs, half of the RPACKs will be placed prior to the DIMM2 connector (the last DIMM in Channel A), and the other half will be placed after DIMM2 connector.

Figure 7-41. DDR VTT Termination Island Example (Layer 1)

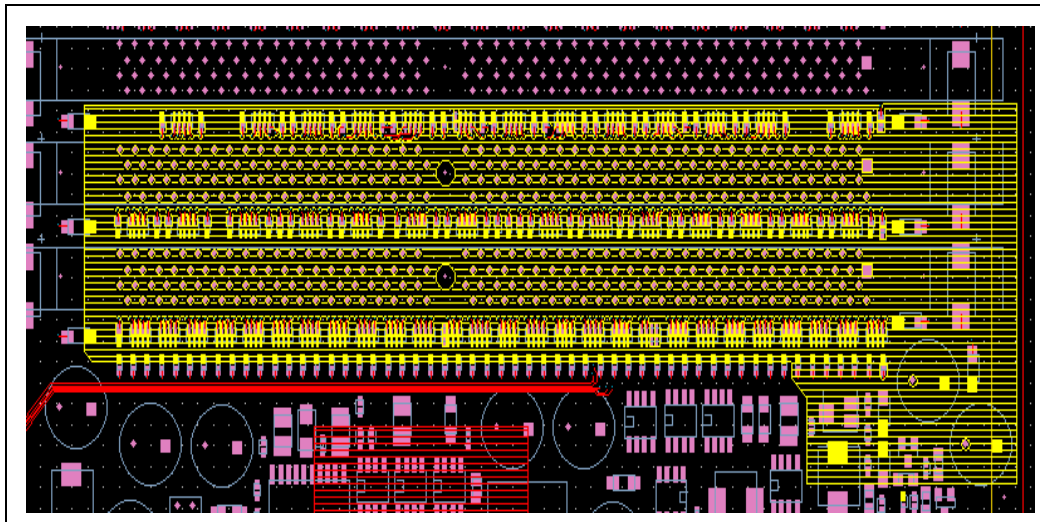


Figure 7-42. DDR VTT Termination Island Example (Layer 3)

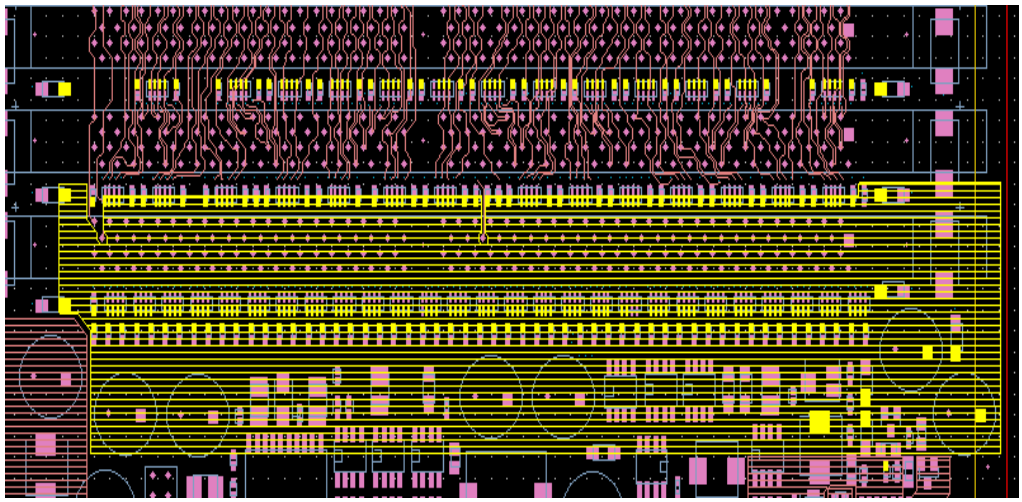


Table 7-30. DDR VTT Termination Island Requirements

Parameter	Guideline
Island Dimensions	1.3 inches x 6.0 inches (Top Layer and Layer 3)
Resistor and capacitor connectivity	Connect termination resistors and decoupling capacitors directly to the termination island

7.7.5.1 VTT Termination Island High-Frequency Decoupling Requirements

The VTT Island must be decoupled using high-speed bypass capacitors—one 0603 0.1 µF capacitor per two DDR signals (or two capacitors per RPACK). These decoupling capacitors connect directly to the VTT island and to ground and must be spread-out across the termination island so that all the parallel termination resistors are near high-frequency capacitors. The capacitor ground via should be within 25 mils of the capacitor pad, and the via and the pad should be connected with as wide a trace as possible. The distance from any DDR termination resistor pin to a 0.1 µF VTT capacitor pin must not exceed more than 100 mils. Because Channel A termination and decoupling components are space constrained between DIMM connectors, two caps must be placed between every two RPACKs.

Finally, place one 4.7 µF ceramic capacitor on each end of the termination island, and place one 4.7 µF ceramic capacitor near the center of the termination row.

Figure 7-43. DDR VTT Termination 0.1 µF High-Frequency Capacitor Example 1

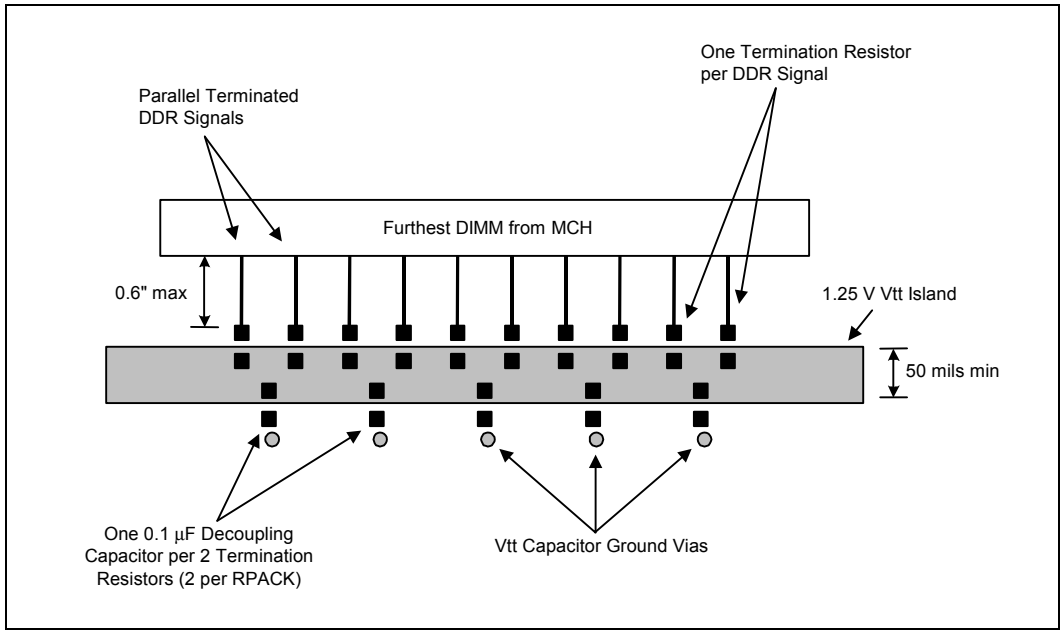


Figure 7-44. DDR VTT Termination 0.1 µF High-Frequency Capacitor Example 2

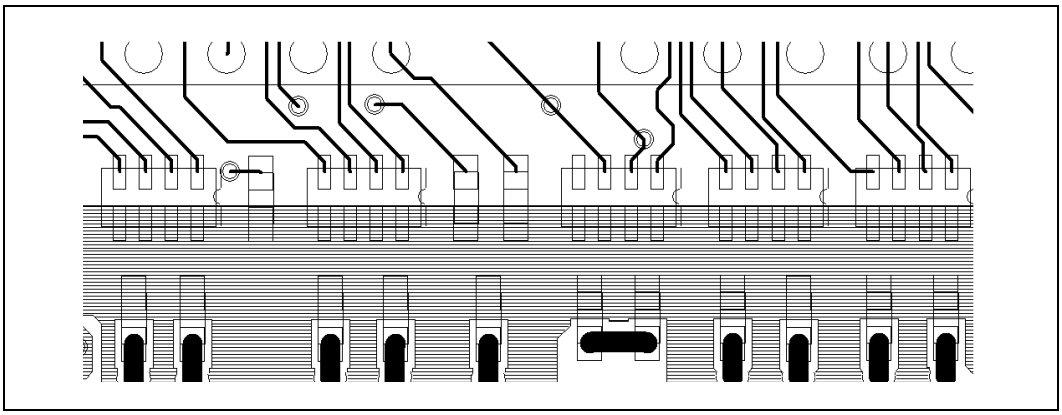


Figure 7-45. DDR VTT Termination 4.7 µF High-Frequency Capacitor Example

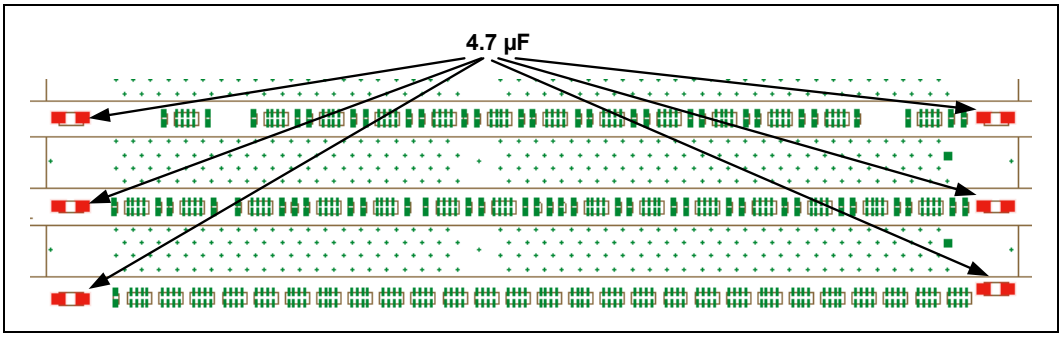


Table 7-31. DDR VTT Termination Island High-Frequency Decoupling Requirements

Parameter	Guideline
0.1 µF capacitors	Place one decoupling cap for every two DDR signals/termination resistors (or two caps for every RPACK). The distance from any termination resistor to decoupling capacitor should not exceed 100 mils
4.7 µF capacitors	Six capacitors are needed. Place three on each side of the termination island. Caps should be placed one on each end of the RPACK rows.

7.7.6 Power Sequencing Requirements

7.7.6.1 MCH Power Sequencing Requirements

There are no MCH power sequencing requirements. All MCH power rails should be stable before deasserting reset, but the power rails can be brought up in any order desired. Good design practice has all MCH power rails come up as close in time as practical, with the core voltage (1.2 V / 1.3 V) coming up first.

7.7.6.2 DDR-SDRAM Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements except that 1.25 V comes up after the 2.5 V rail. Because of this requirement, designs should have the 1.25 V rail derived from a regulator with 2.5 V as its input.

Hub Interface 8

This chapter discusses Hub Interface 2.0 (HI 2.0) and Hub Interface 1.5 (HI 1.5) implementations on the E7505 chipset. The MCH hub interface A to the ICH4 uses a HI 1.5 implementation. The MCH hub interface B to the P64H2 uses a HI 2.0 implementation.

8.1 Hub Interface 2.0 Interface Implementation

Hub interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of the Interface specification. The following are general guidelines that should be followed. Trace lengths included in this section are guidelines only. It is recommended that the board designer simulate the routes to verify that specifications are met.

The P64H2 ballout assignments have been optimized to simplify the hub interface routing between devices. It is required that the hub interface signals be routed directly from the MCH to P64H2, with all signals referenced to VSS. A consistent VSS reference layer must be maintained at all times. In addition, all signals within a bundle (consisting of 9 bits of data and a pair of strobes) must be routed on the same layer and must be referenced to the same VSS plane. Layer transitions should be kept to a minimum. If a layer change is required, use only two vias per net, and keep all signals within a bundle on the same layer. For the 16-bit hub interface, HI[7:0] and HI20 are associated with PSTRBS and PSTRBF, and HI[15:8] and HI21 are associated with PUSTRBS and PUSTRBF.

For HI 2.0 devices on the motherboard, trace length matching of ± 0.25 inches (including package length compensation) is required among all signals within a data group. If the HI 2.0 device is on an adapter, length matching of ± 0.125 inches (including package length compensation) is required among all signals within a data group.

Figure 8-1 shows the length matching rules for a hub device on the motherboard. All of the hub interface data signals must be length matched within 0.25 inch. The figure shows HIx and HIy with the maximum allowed difference in length, with HIz somewhere in the middle. The strobe pair (PSTRBF and PSTRBS) are also matched to each other within 0.25 inch. However, the absolute length of the strobe pair is adjusted according to the *longest Hub Interface Data line.* The upper pair shows the case where one of the strobes is the same *exact* length as the longest hub interface data line (which is the longest possible length one of the strobes can be). In this case, the other signal *must* be shorter, and must be no shorter than 0.25 inch. The lower strobe pair shows the case where one of the strobes is *exactly* 1.0 inch shorter than the longest hub interface data line (which is the shortest possible length one of the strobes can be). In this case, the other signal *must* be longer, but no longer than 0.25 inch.

The hub interface strobe trace lengths should be 0 mils–400 mils shorter than the longest hub interface data trace length. See Table 8-2 for hub interface matching requirements.

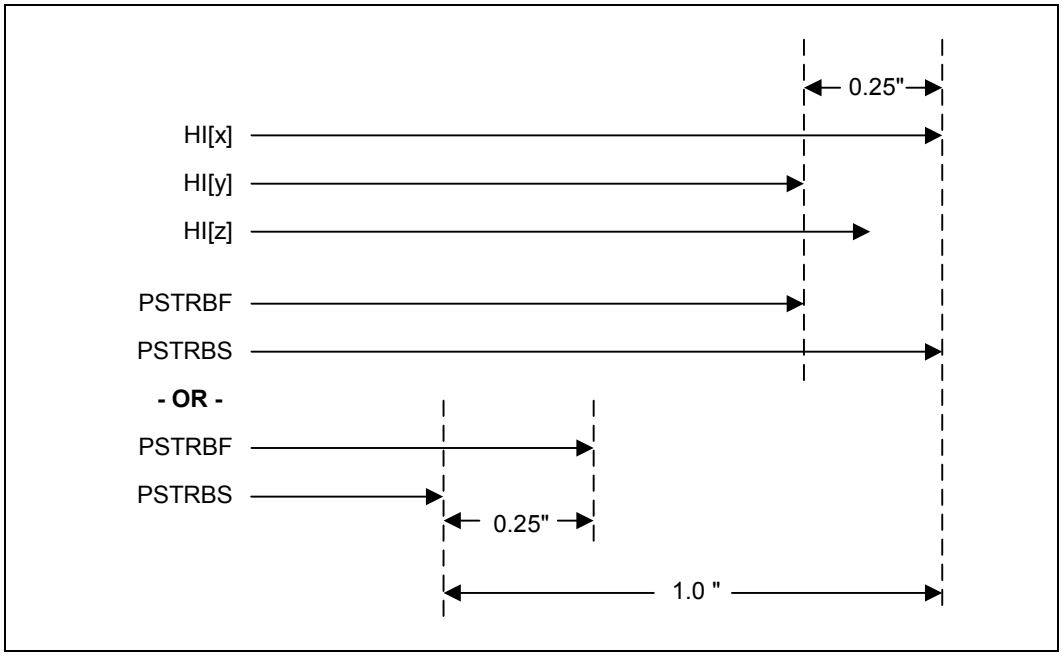
Table 8-1. HI 2.0 Signal/Strobe Association

Data Group	Associated Strobes
HI_[7:0] HI_20	PSTRBF PSTRBS
HI_[15:8] HI_21	PUSTRBF PUSTRBS

Table 8-2. HI 2.0 Length Matching Requirements

Signal	Topology	Matching Requirement
HI[7:0], HI20	Device on motherboard	± 0.25 inches to other signals in this group
	Device on adapter	± 0.125 inches to other signals in this group
HI[15:8], HI21	Device on motherboard	± 0.25 inches to other signals in this group
	Device on adapter	± 0.125 inches to other signals in this group
PSTRBS, PSTRBF		0 – 400 mils shorter than HI[7:0], HI20
PUSTRBS, PUSTRBF		0 – 400 mils shorter than HI[15:8], HI21

Figure 8-1. HI 2.0 Length Matching Example



NOTES:
1. All signal lines with arrows show the total length of the signal including the mother board trace length, MCH package trace length, and Hub Interface 2.0 device trace length.
2. This figure is only an example for an implementation with the device on the motherboard. For an implementation with the hub interface device on a riser card, simply replace both instances of 0.250” with 0.125”.
3. In the figure, HIx, HIy, and HIz represent hub interface data signals. The other six data signals in the group must also be matched within 0.25”. The associated strobe pair must be within 1.0” of the longest data signal.

8.1.1 High-Speed Routing Guidelines

This section documents the routing guidelines for the 16-bit HI 2.0. The HI 2.0 signal groups are listed in Table 8-3. The general routing guidelines for the HI 2.0 signals are listed in Table 8-2.

Figure 8-2. 16-Bit Hub Interface Routing Example

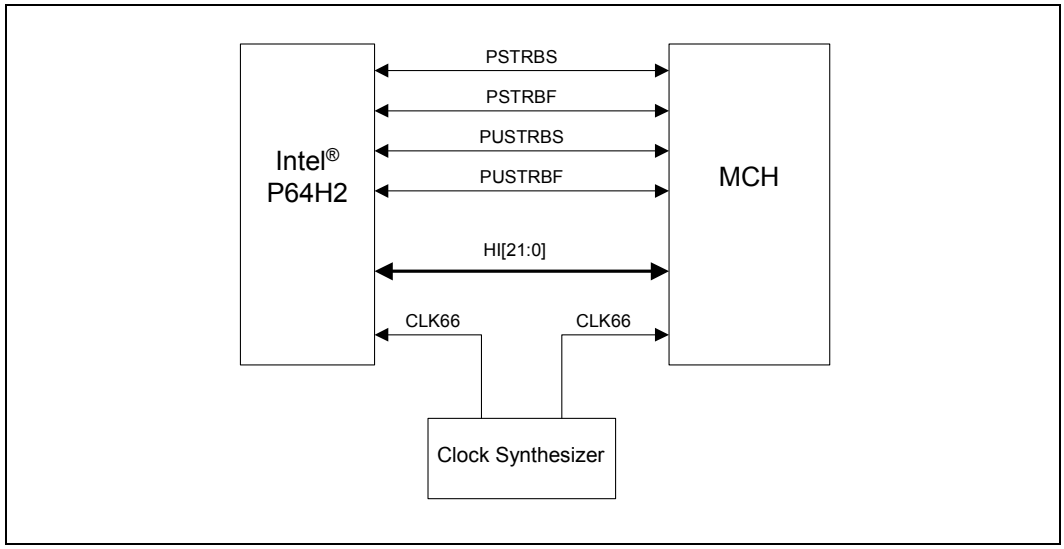


Table 8-3. HI 2.0 Signal Groups

Group	Signals
Common Clock Signals	HI_[19:16]
Source Synchronous Signals	HI_[21:20],HI_[15:0],PSTRBF,PSTRBS,PUSTRBF,PUSTRBS
Miscellaneous Signal	HI_RCOMP, HI_VSWING, HI_VREF

8.1.2 PCB Stack-Ups for HI 2.0

There are two types of PCB stack-up that must be considered for HI 2.0: 4-layer low cost boards utilizing microstrip only, and 6+ layer PCBs that can be routed as microstrip in the outer layers and stripline on the inner layers. For this discussion we will restrict board thickness to 63 mils, a standard that is compatible with Slot type edge connectors. The 63-mil board thickness is also a manufacturing standard, and any deviation will therefore lead to increased costs primarily due to the need for nonstandard connectors.

- Material: FR4
- Dielectric constant: 4.2 ± 0.3
- Board thickness: 63 mils ± 10%

8.1.2.1 Recommended PCB Trace Geometry

The practically achievable impedance ranges of stripline and microstrip differ considerable. For 63-mil PC board with 5 mil or greater line widths, stripline has a practical Z_0 range of between 35 Ω and 70 Ω, while microstrip ranges between 45 Ω and 80 Ω. In both cases higher impedances are impractical because it would require that either the trace width be reduced to less than 5 mils, that the dielectric thickness be increased, or that a dielectric with a lower ER be used. Obtaining a lower impedance is straightforward and may be achieved by increasing the trace width above the nominal 5.0-mil figure. However, it does require that the spacing be increased, or that a higher crosstalk figure be accepted. In any case, 2-D field solutions are required to achieve an accurate impedance prediction. Microstrip calculations must include the effect of solder mask and plating.

To utilize a common receive buffer R_{TT} setting, an interconnect Z_0 of 50 Ω is recommended for both source synchronous and common clock signal lines on all parallel terminated hub interface interconnects. (R_{TT} is the parallel mode termination impedance for parallel terminated Hub Interface as seen at the receiver).

8.1.2.2 Minimum and Maximum Trace Lengths

The hub interface bus consists of signals that are switched via common clock, and others that use source synchronous signaling. The combined timing requirements of these two signaling methods define the minimum and maximum bus lengths that can be supported as listed in Table 8-4. For all cases in the table, the bus length includes the connector length.

Table 8-4. HI 2.0 Routing Parameters

System Type	Trace Length Min-Max (For HI 2.0 Device Down)	Trace Length Min-Max (For HI 2.0 Card Solution)	Trace Z_0	Trace Width/Spacing	Breakout Width/Spacing
533 MT/s Platform	3” – 20”	3”– 14” (max on-card length = 5”)	50 Ω ± 10%	5/15 mils	5/5 mils (max dist = 0.5”)

For HI 2.0, the maximum bus lengths are dictated by the signal integrity of the source synchronous signaling. The minimum bus length is dictated by the hold time for the common clock signals.

The minimum bus length is dictated by the hold time for the common clock signals. Referring to the hub interface AC timing specifications, using the worst case common clock skew of ± 1.0 ns, the fast corner t_{CO} of 0.5 ns, and a zero t_H yields a minimum allowable t_{FLT} of 0.5 ns. This equates to a 3 inch minimum interconnect length, where this delay number includes both PCB trace and any connectors. There is also an allowance for bus lengths less than 3.0 inches if the clock skew is 0.5 ns or better.

8.1.2.3 Impedance Variations vs. Mechanical Tolerances

Table 8-5 shows the nominal trace dimensions that are used to achieve characteristic impedances of 50 Ω and 60 Ω. The breakout spacing acknowledges that when exiting from under a device it may not be possible to meet the optimal spacing requirements because of routing density. Because the breakout region increases line to line coupling and hence crosstalk, it should be kept to a length of no more than 0.5 inches. If there is a need to increase the breakout length (e.g., to accommodate bypass capacitors), it may be necessary to reduce the overall PCB trace length. Determining the amount of length reduction requires that the particular layout be simulated on a case by case basis.

Table 8-5. Trace Impedance Guidelines

Interconnect Type	Trace Z_O	PCB width/spacing	Breakout width/spacing	Dialectric Thickness
stripline	50 Ω ± 10/%	5/15	5/5 mils	14 mils
stripline	60 Ω ± 10%	5/15	5/5 mils	19 mils
ustrip	50 Ω ± 10%	7.5/22.5	7.5/7.5 mils	4 mils

8.1.3 VREF/VSWING Generation

This section describes the preferred modes of VREF and VSWING generation and the characteristics as applicable to HI 2.0. VREF will be the signal used to set the trip point of the incoming DATA signals and STRB signals when they are sensed single-endedly. VSWING is the reference voltage used by the RCOMP impedance compensation circuitry.

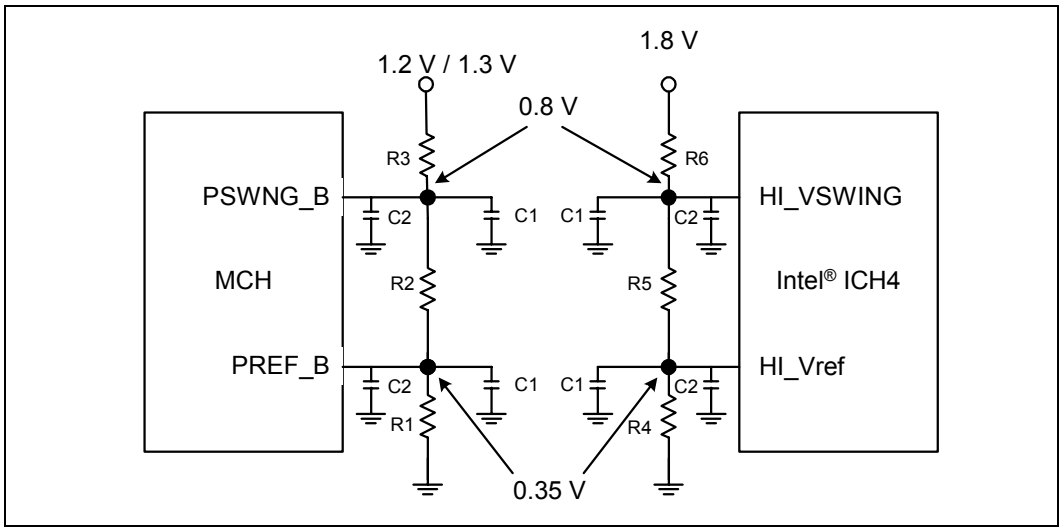
The nominal HI 2.0 reference voltage is 0.350 V ± 5%. In addition to the reference voltage, a reference swing voltage must be supplied to control buffer voltage swing characteristics. The nominal HI 2.0 reference swing voltage should be 0.8 V ± 5%. Both of these reference voltages can be generated locally with a single voltage divider circuit. Figure 8-3 shows an example voltage divider circuit. A single voltage divider circuit can be used if the components are not spaced far apart (< 4–5 inches), and are on the same board.

Table 8-6. HI 2.0 Reference Circuit Specifications

Reference Voltage Specification (V)	Reference Swing Voltage Specification (V)	1.2 V Voltage DIvider Circuit Recommended Resistor Values (Ω)	1.3 V Voltage DIvider Circuit Recommended Resistor Values (Ω)	1.8 V Voltage DIvider Circuit Recommended Resistor Values (Ω)		Capacitor Values
				Group 1[1]	Group 2[1]	
0.350 ± 5%	0.800 V ± 5%	R1 = 392 ± 1% R2 = 499 ± 1% R3 = 453 ± 1%	R1 = 402 ± 1% Ω R2 = 511 ± 1% Ω R3 = 549 ± 1% Ω C1 = 0.1 µF C2 = 0.01 µF	R4 = 255 ± 1% R5 = 332 ± 1% R6 = 732 ± 1%	R4 = 261 ± 1% R5 = 332 ± 1% R6 = 750 ± 1%	C1 = 0.1 µF C2 = 0.01 µF

NOTE:
1. Use only resistors from group 1 or 2; do not mix values from these groups.

Figure 8-3. HI 2.0 with Locally Generated Voltage Divider Circuit



The resistor values R1, R2, and R3 must be rated at ± 1% tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A 0.1 µF capacitor (C1 in the circuit) should be placed close to each resistor divider, and a 0.01 µF bypass capacitor (C2 in the circuit) should be placed near each reference voltage pin. If the length of the trace from the voltage divider to the pin is greater than 1 inch, place more than one 0.01 µF capacitor near the reference voltage pin. The trace length from the voltage divider circuit to the corresponding pin must be no longer than 3.5 inches.

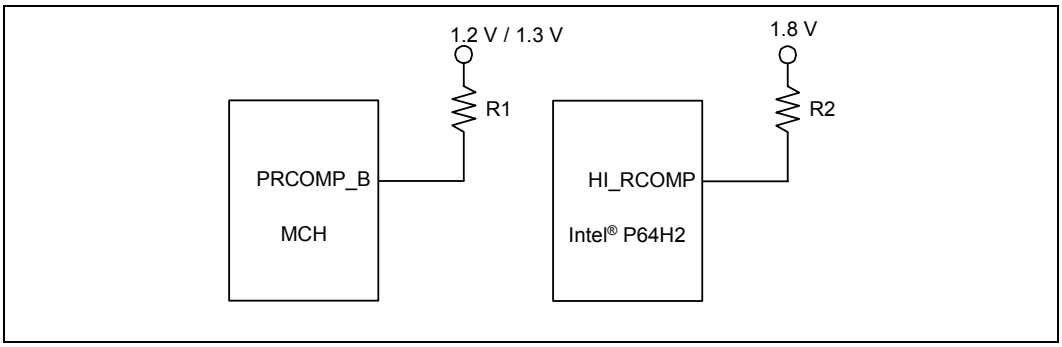
8.1.3.1 HI 2.0 Resistive Compensation

The hub interface uses a resistive compensation signal (RCOMP) to compensate buffer characteristics of temperature, voltage and process. The RCOMP resistor values are given in Table 8-7. Figure 8-4 shows the RCOMP circuits.

Table 8-7. HI 2.0 RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
MCH	50 Ω ± 10%	R1 = 24.9 Ω ± 1%	VCC1_2
		R1 = 32.4 Ω ± 1%	VCC1_3
Intel® P64H2	50 Ω ± 10%	R2 = 61.9 Ω ± 2%	VCC1_8

Figure 8-4. HI 2.0 RCOMP Circuits



8.1.3.2 16-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use three 0.1 µF capacitors per P64H2 component. These capacitors should be placed as close as possible to the P64H2 within a maximum of 150 mils, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC side of the capacitors to the VCC power pins. Similarly, if layout allows, metal fingers running on the VCC side of the board should connect the ground side of the capacitors to the VSS power pins.

8.1.3.2.1 PC Boards and Bypass Capacitors

PC boards provide the mounting space for low-frequency bulk capacitance. The effective capacitance is a function of the PC board's intrinsic sheet capacitance plus that of the bypass capacitors. Achieving a specific power delivery network impedance requires that the number, value and locations (relative to the hub interface device package such as the P64H2) of bypass capacitors be specified.

Figure 8-5 shows the P64H2 mounted on a PC board with associated capacitors connecting between the VCC and VSS planes. The two key parameters in determining the effectiveness of bypass capacitors are the effective capacitance and the effective inductance as seen by the power pins at the package. Simulations have shown that each byte of the hub interface should have associated with it a pair of bypass capacitors with a combined value of at least 2 µF.

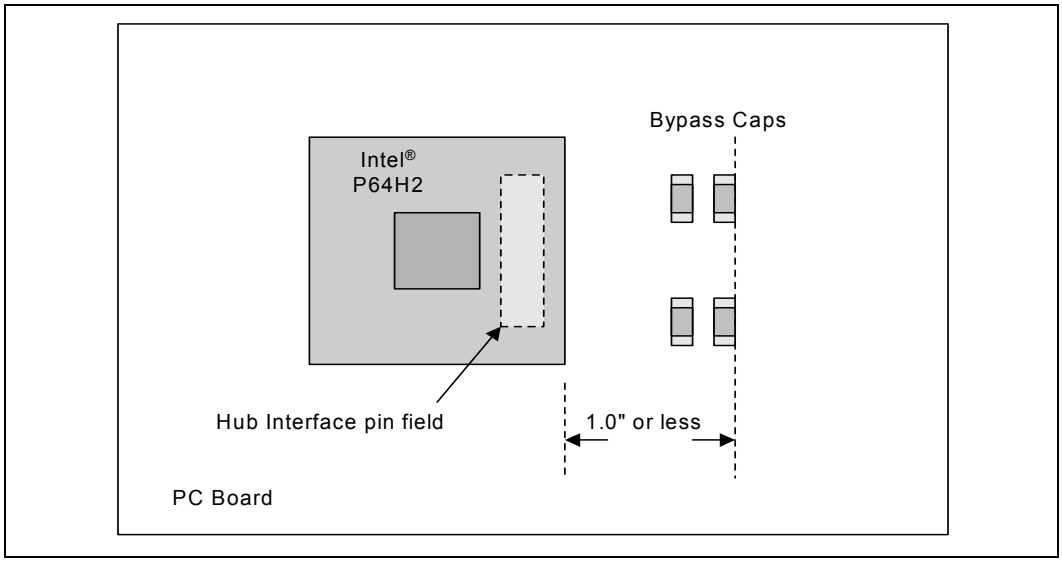
The inductance seen by the P64H2 hub interface package power connections is a function not only of the capacitor (typical surface mount bypass capacitors have a parasitic inductance in the 0.5–1.0 nH range), but also the inductance caused by the solder pads, the vias to the VCC and VSS planes, and the intrinsic sheet inductance of the power planes between the caps and the package. Simulations have shown that a sufficiently low loop inductance can be achieved if the bypass capacitors are placed within 1.0 inch of the edge of the device as shown in Figure 8-5. If there are multiple VCC and VSS planes connecting to the hub interface power pins, it is necessary to make sure that the bypass capacitors connect to each layer.

Additional reduction in inductance can be achieved by minimizing loop area (and hence the loop inductance) between the capacitor solder pad and the PCB power planes. This may be achieved by the following techniques:

- Via in pad technology
- Multiple vias per pad
- Place vias on the inside of the pad

- Use multi-pad low impedance capacitors

Figure 8-5. Bypass Capacitor Placement



8.1.3.2.2 Bulk Capacitors

Bulk capacitors serve two functions: they minimize differential noise originating from the power supply between VCC and VSS, and they provide a low impedance path at frequencies below those covered by the bypass capacitors and above those supplied by the power supply itself. Bulk capacitors should be located as close to the power supply as is practical. The aggregate value of the bulk capacitance should be in the 1000 µF – 5000 µF range, and is best implemented by paralleling several smaller capacitors thereby lowering both ESR and ESL. Bulk capacitors are usually tantalum or aluminum electrolytic.

8.1.3.3 Unused HI 2.0 Interfaces

The recommended termination for unused HI 2.0 interfaces is as follows:

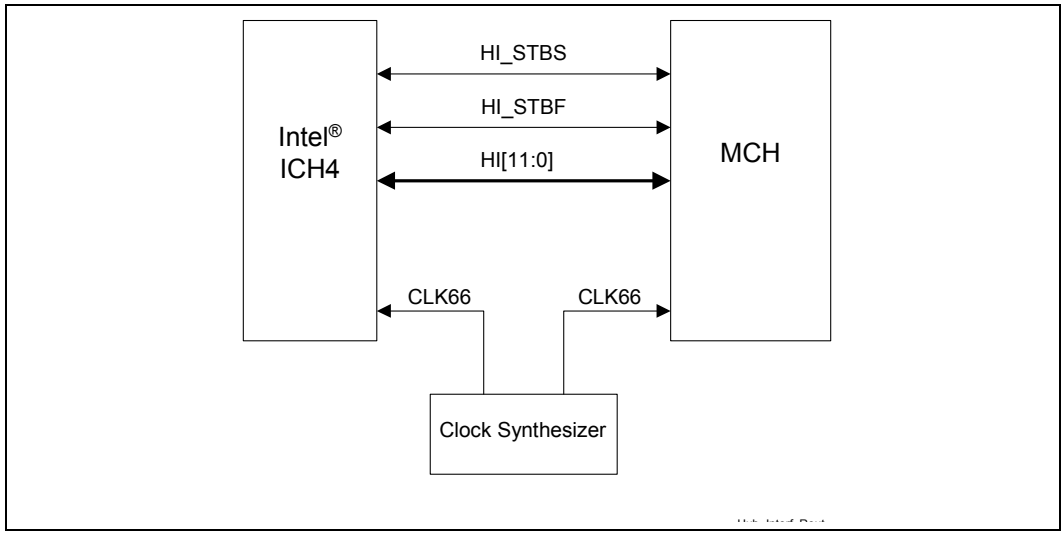
- All hub interface data and strobe signals can be left as no connects.
- HI_VREF must remain connected to the reference voltage divider circuit.
- HI_VSWING must remain connected to the reference voltage swing divider circuit.

8.2 Hub Interface 1.5 Implementation

The MCH and ICH4 ball assignments are optimized to simplify the hub interface routing between these devices. The hub interface signals must be routed directly from the MCH to ICH4 with all signals referenced to VSS. Layer transitions should be keep to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer.

The 8-bit hub interface signals are all in the same data group. That is, all signals are associated with HI_STBS / HI_STBF. Note that these signals are called PSTRBS_0 / PSTRBF_0 on the MCH

Figure 8-6. 8-Bit Hub Interface 1.5 Routing



This section documents the routing guidelines for the 8-bit HI 1.5. This hub interface connects the MCH to the ICH4. This interface supports only the parallel termination mode. As a result, the DPRSLPVR pin on the ICH4 must be tied to ground to ensure that it will run in parallel mode.

8.2.1 Hub Interface 1.5 High-Speed Routing Guidelines

The HI 1.5 signal groups are listed in Table 8-8. The general routing guidelines for the HI 1.5 signals are listed in Table 8-9.

Table 8-8. HI 1.5 Signal Groups

Group	Signals
Common Clock Signal	HI[11:8]
Source Synchronous Signal	HI[7:0], HI_STBF, HI_STBS
Miscellaneous Signal	HIRCOMP, HISWNG, HIVREF

Table 8-9. HI 1.5 Routing Parameters

System Type	Trace Length Min-Max	Trace Zo	Trace Width/Spacing	Breakout Width/Spacing
266 MT/s	3”–20”	50Ω ± 10%	5/15 mils	5/5 mils (max dist = 0.3”)

Using the recommended stack-up, the 8-bit hub interface data signal traces must be routed 5 mils wide. There must be 15 mils spacing between traces (5/15). To break out of the MCH and ICH4 package, the hub interface data signals can be routed 5/5. The signals must be separated to 5/15 within 0.3 inches of the package.

For HI 1.5 devices on the motherboard, each strobe signal trace must be the same length, and each data signal trace must be matched within ± 100 mils.

8.2.2 Generation/Distribution of Reference Voltages

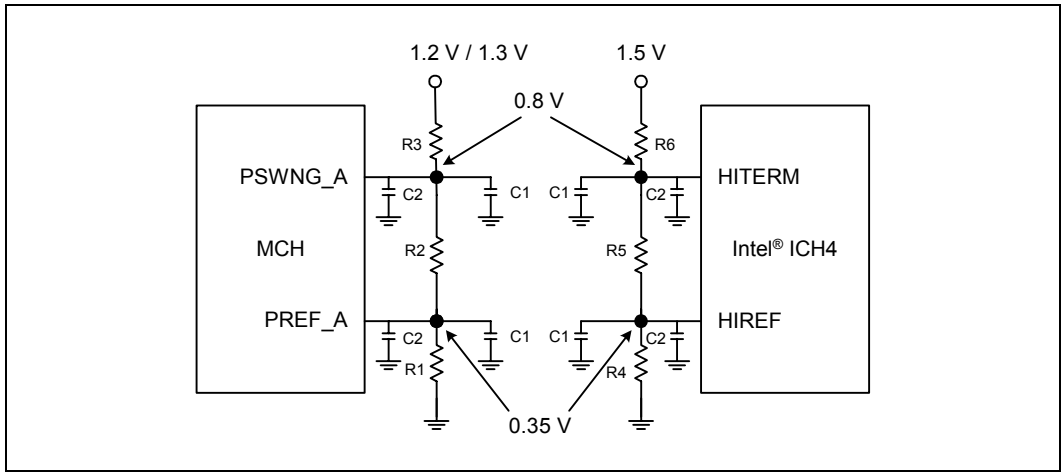
The nominal HI 1.5 reference voltage is 0.35 V ± 5%. The 8-bit hub interface on the MCH has a dedicated HI VREF pin (PREF_A) to sample this reference voltage. In addition to the reference voltage, a reference swing voltage must be supplied to control buffer voltage swing characteristics. The nominal HI 1.5 reference voltage swing must be 0.8 V for the MCH and ICH4. The hub interface on the MCH has a dedicated HI SWING pin (PSWNG_A) to sample this reference swing voltage. The ICH4 also has a dedicated reference swing voltage pin (HITERM). Refer to the Table 8-10. Both of these reference voltages can be generated locally with a single voltage divider circuit. Figure 8-7 shows an example voltage divider circuit.

Table 8-10. HI 1.5 Reference Circuit Specifications

Reference Voltage Specification (V) (HIREF)	Reference Swing Voltage Specification (V) (HITERM)	1.2 V Voltage DIvider Circuit Recommended Values	1.3 V Voltage DIvider Circuit Recommended Values	1.5 V Voltage DIvider Circuit Recommended Values	
				Group 1[1]	Group 2[1]
0.350 ± 5%	For Intel® ICH4 = 0.8 For MCH = 0.8	R1 = 392 ± 1% Ω R2 = 499 ± 1% Ω R3 = 453 ± 1% Ω C1 = 0.1 µF C2 = 0.01 µF	R1 = 402 ± 1% Ω R2 = 511 ± 1% Ω R3 = 549 ± 1% Ω C1 = 0.1 µF C2 = 0.01 µF	R6 = 80.6 ± 1% Ω R5 = 51.1 ± 1% Ω R4 = 40.2 ± 1% Ω C1 = 0.1 µF C2 = 0.01 µF	R6 = 226 ± 1% R5 = 147 ± 1% R4 = 113 ± 1% C1 = 0.1 µF C2 = 0.01 µF

NOTE:
1. Use only resistors from group 1 or 2, do not mix values from these groups.

Figure 8-7. HI 1.5 Locally Generated Reference Divider Circuits



All resistor values must be rated at ± 1% tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A 0.1 µF capacitor (C1 in Figure 8-7) should be placed close to each resistor divider, and a 0.01 µF bypass capacitor (C2 in Figure 8-7) should be placed within 0.25 inches of reference voltage pins. The trace length from the voltage divider circuit to the HIREF and PREF_A pins must be no longer than 3.5 inches.

Both the voltage reference and the voltage swing reference signals should be routed at least 20 mils to 25 mils from all other signals.

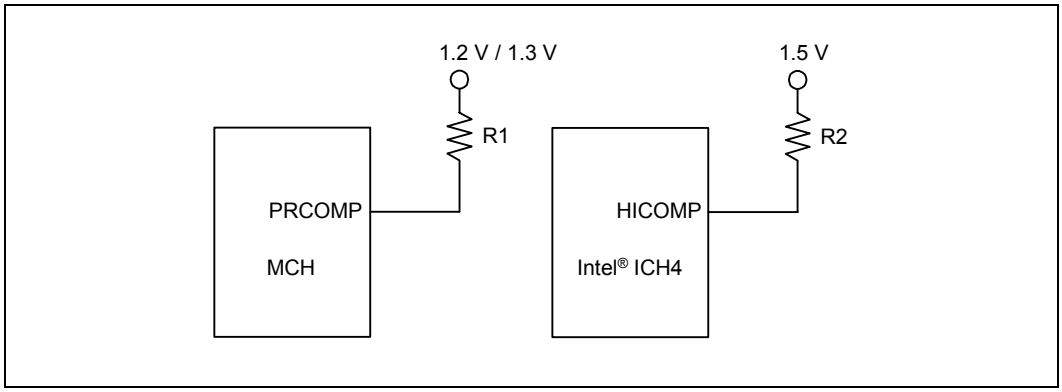
8.2.3 HI 1.5 Resistive Compensation

The hub interface uses a resistive compensation signal (RCOMP) to compensate buffer characteristics for temperature, voltage, and process.

Table 8-11. HI 1.5 RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
MCH	50Ω ± 10%	R1 = 24.9 Ω ± 1%	VCC1_2
		R1 = 32.4Ω ± 1%	VCC1_3
Intel® ICH4	50Ω ± 10%	R2 = 43.3Ω ± 2%	VCC1_5

Figure 8-8. HI 1.5 RCOMP Circuits



8.2.4 8-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors per component (i.e., the ICH4 and MCH). These capacitors should be placed within 150 mils of each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1_5/VCC1_2* side of the capacitors to the VCC1_5/VCC1_2* power pins. Similarly, if layout allows, metal fingers running on the VCC1_5/VCC1_2 *side of the board should connect the ground side of the capacitors to the VSS power pins.

* Applies to 1.3 V MCH Core Voltage (VCC1_3)

AGP 8X 9

9.1 AGP 8X Implementation

This section contains information for one possible routing and layout solution that is based on the reference platform. Other implementations of AGP routing may be used with proper simulation based on parameters specified in the AGP design guide, available at www.agpforum.org.

Refer to Section 15.6 and Section 16.7 for schematic and layout checklists for AGP 8X. Table 9-1 and Table 9-2 show the signal groups and associated strobes.

Note: The AGP supports both 4X and 8X operation.

Table 9-1. Signal Groups

Group	Signals
1	GAD[15:0], GC#/BE[1:0], AD_STBF0, AD_STBS0
2	GAD[31:16], GC#/BE[3:2], DBI_HI, DBI_LO (AGP 3.0), AD_STBF1, AD_STBS1
3	SBA[7:0] (AGP 2.0), SBA[7:0]# (AGP 3.0), SB_STBF, SB_STBS
4	GIRDY, GTRDY, GFRAME, SERR# (AGP 2.0), SERR (AGP 3.0), STOP, GDEVSEL, GPAR
5	RBF# (AGP 2.0), RBF (AGP 3.0), WBF# (AGP 2.0), WBF (AGP 3.0), GREQ, GGNT

Table 9-2. Associated First and Second Strobes

Group	Signals	First Strobe	Second Strobe
1	GAD[15:0], GC#/BE[1:0]	AD_STBF0	AD_STBS0
2	GAD[31:16], GC#/BE[3:2], DBI_HI, DBI_LO (AGP 3.0)	AD_STBF1	AD_STBS1
3	SBA[7:0] (AGP 2.0), SBA[7:0]# (AGP 3.0)	SB_STBF	SB_STBS

9.1.1 Recommended AGP 8X Routing Parameters

The AGP 8X signals must be routed directly from the MCH to the AGP connector with all signals referenced to VSS. A consistent VSS reference plane must be maintained at all times. In addition, all signals within a address/data group must be routed on the same layer (see Table 9-1 for address/data groups). Table 9-3 summarizes the routing parameters for the AGP interface.

Table 9-3. AGP 8X Routing Parameters

Signal Group	Trace Impedance (Z_0)[1]	Layer	Spacing	Min Length	Max Length
Strobe to Strobe	60 Ω[1]	Stripline	20 mil	2.5”	7.0”
		Microstrip	25 mil	2.5”	6.0”
Strobe to Data		Stripline	20 mil	2.5”	7.0”
		Microstrip	25 mil	2.5”	6.0”
Data to Data		Stripline	20 mil	2.5”	7.0”
		Microstrip	20 mil	2.5”	6.0”
Common Clock		Stripline	15 mil	2.5”	7.5”
		Microstrip	15 mil	2.5”	7.5”

NOTE:
1. To meet the 60 Ω trace impedance requirement, a trace width of 4 mils was used based on the board stack-up described in Section 4.2. The trace width needed to meet the 60 Ω requirement will vary for different platforms based on platform stack-up.

9.1.2 Length Matching

The data groups shown in Table 9-2 must match the strobes within 25 mils. First and second strobes must match to within 5 mils. There are no requirements for length matching between groups, and there are no length matching requirements for signals in groups 4 and 5.

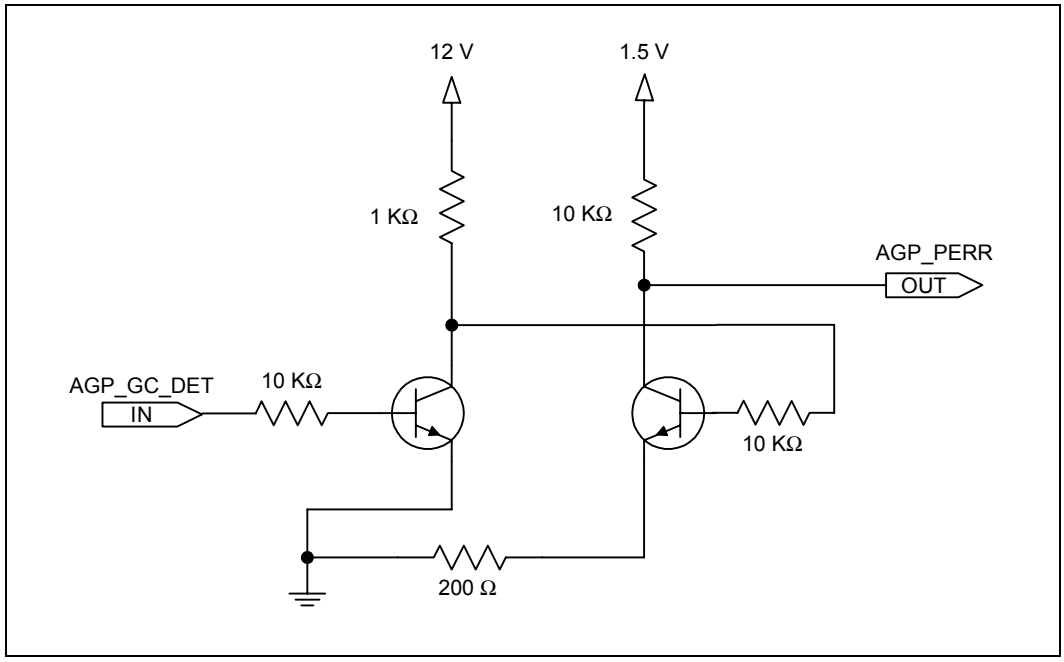
Note: MCH package lengths must be considered when tuning the AGP bus.

9.1.3 Miscellaneous Signal Requirements

9.1.3.1 SERR/PERR

The PERR signal is not supported by E7505 chipset and must be supplied to the card based on the GC_8XDET signal. SERR routes between the connector and the MCH with no special termination. See Figure 9-1 for a PERR reference circuit. The circuit provides a pull-down to ground during 8X operation, and a pull-up to 1.5 V during 4X operation.

Figure 9-1. PERR Reference Circuit



9.1.3.2 TYPEDET

The TYPEDET signal is not required because of the use of a 1.5 V connector.

9.1.3.3 PRCOMP_AGP[1:0]

These signals are used to calibrate the AGP buffers. The PRCOMP signals each require a 43 Ω resistor to VDDQ.

9.1.3.4 PREF_AGP[1:0]

A complex VREF circuit is required to meet the reference voltage requirements for AGP 4X and 8X. One possible implementation of this circuit can be found in the AGP design guide, available at www.agpforum.org.

While the VREF voltage for AGP 8X mode is 0.35 V, the circuit implemented in the CRB schematics seems to show a voltage of only 0.3 V. If the resistance across the transistor is taken into account, it can be shown that the circuit generates the required 0.35 V.

9.1.3.5 PSWNG_AGP[1:0]

Provide the reference voltages used by the AGP RCOMP circuits. PSWNG_AGP is based on a resistor divider circuit, and is derived from 1.5 V. The voltage level is 0.8 V for 8X mode, and is the maximum voltage for the AGP signal bus. For AGP 4X mode, the PSWNG_AGP level is a “don’t care.”

Intel® I/O Controller Hub 4 (ICH4) 10

10.1 System Overview

The ICH4 is designed for a variety of processors/memory controller hubs, and has improved enhancements over the ICH2 and ICH3. The ACPI compliant ICH4 platform can support the Full-on, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-Off power management states. Through the use of the integrated LAN functions, the ICH4 also supports Wake-on-LAN for remote administration and troubleshooting.

The ICH4 integrates an UltraATA/100 controller, one EHCI host controller and three UHCI host controllers supporting six external ports, an LPC interface controller, a FWH interface controller, a PCI interface controller, an AC ’97 digital controller, an integrated LAN controller, and a hub interface for communication with the MCH. The ICH4 component provides the data buffering and interface arbitration required to ensure that system interfaces operate efficiently and provide the bandwidth necessary to enable the system to obtain peak performance.

10.1.1 Intel® ICH4 System Features

The I/O Controller Hub provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions:

- Upstream hub interface for access to the MCH
- 2 channel Ultra ATA/100 Bus Master IDE controller
- 1 EHCI USB 2.0 Host Controller and 3 UHCI USB 1.1 Host Controllers (Expanded capabilities for six ports)
- SMBus 2.0 controller
- FWH interface
- LPC interface
- *AC ’97 Component Specification, Revision 2.3* interface (*AC ’97, r2.3*)
- *PCI Local Bus Specification, Revision 2.2* interface
- Integrated System Management Controller
- Integrated LAN Controller

The ICH4 also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces. Refer to Section 10.2 for more information about these interfaces.

10.1.2 Bandwidth Summary

Table 10-1 is a summary of the bandwidth requirements for the ICH4.

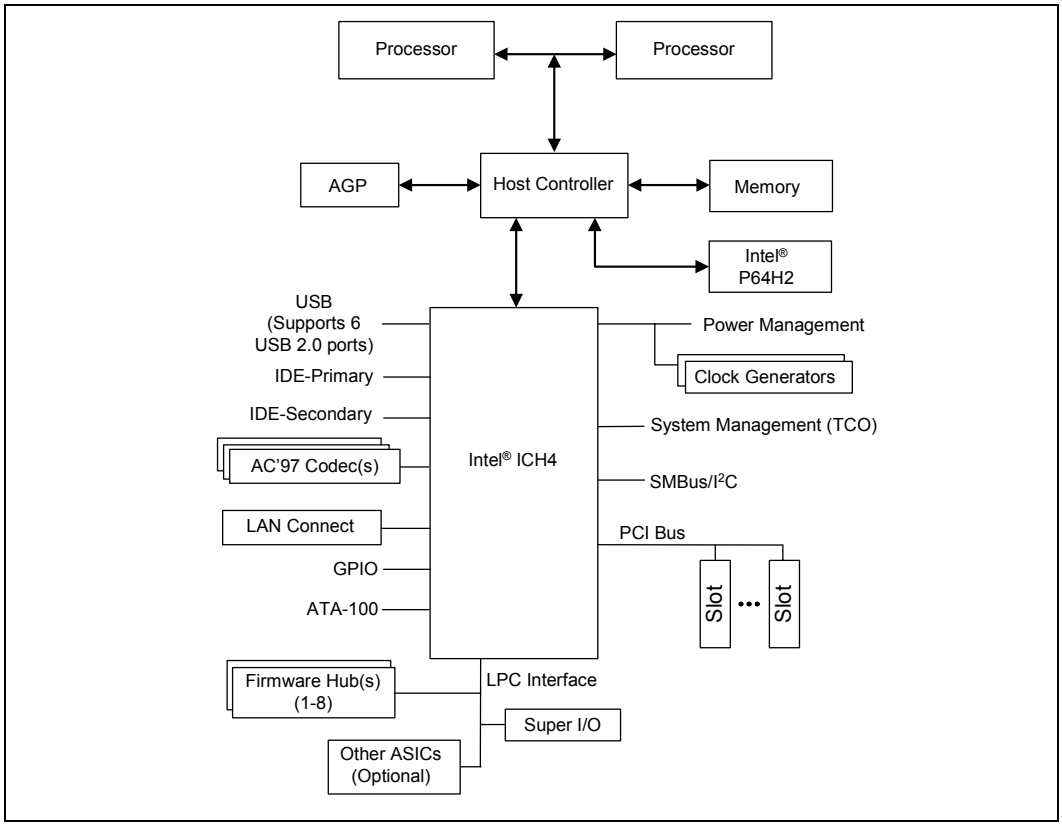
Table 10-1. Intel® ICH4 System Bandwidth Summary

Interface	Clock Speed (MHz)	Samples Per Clock	Data Rate (Mega-samples/s)	Data Width (bits)	Bandwidth (MB/s)
Hub Interface	66	4	266	8	266
PCI 2.2	33	1	33	32	133
IDE	Up to 44.444 Write Up to 50 Read	1	44.444 (Write 50 (Read)	16	88.9 (Write) 100 (Read)
LCI	5 – 50	1	5 – 50	3	1.875 – 18.75
AC '97	12.288	1	12.288	1	1.536
LPC	33	1	33	4	16.5
USB 2.0 High Speed	Up to 240 (embedded in data)	Up to 2	480	1	60
SMBus	10	1	10	1	1.25

10.1.3 System Configurations

Figure 10-1shows a typical platform configuration using the ICH4 component.

Figure 10-1. Intel® ICH4 System Block Diagram



10.1.4 Intel® ICH4 Conventions and Terminology

Table 10-2 defines the conventions and terminology that are used in the following ICH4 descriptions

Table 10-2. Intel® ICH4 Conventions and Terminology

Convention/ Terminology	Definition
AC	Audio Codec.
ASF	Alert Standards Forum.
AMC	Audio/Modem Codec.
Anti-Etch	Any plane-split, void or cutout in a VCC or GND plane is referred to as an anti-etch.
BER	Bit Error Rate.
CMC	Common Mode Choke.
EMI	Electro Magnetic Interference.
ESD	Electro Static Discharge.
FS	Full Speed. Refers to USB 1.1 Full Speed.
FWH	Firmware Hub. A non-volatile memory device used to store the system BOIS
HS	High Speed. Refers to USB 1.1 High Speed.
Intel® ICH4	I/O Controller Hub Fourth Generation.
LCI	LAN Connect Interface.
LOM	LAN on Motherboard.
LPC	Low Pin Count.
LS	Low Speed. Refers to USB 1.1 Low Speed.
MC	Modem Codec.
PCM	Pulse Code Modulation.
PLC	Platform LAN Connect.
RTC	Real Time Clock
SMBus	System Management Bus. A two-wire interface through which various system components can communicate
SPD	Serial Presence Detect.
S/PDIF	Sony/Phillips Digital Interface.
STD	Suspend To Disk.
STR	Suspend to RAM.
TCO	Total Cost of Ownership.
TDM	Time Division Multiplexed.
TDR	Time Domain Reflectometry.
UBGA	Micro Ball Grid Array.
USB	Universal Serial Bus.

10.2 Platform Initiatives

10.2.1 Integrated LAN Controller

The ICH4 incorporates an integrated LAN Controller. Its bus master capabilities enable the component to process high level commands and perform multiple operations, which lowers processor utilization by off-loading communication tasks from the processor.

The ICH4 supports several components depending upon the target market. Available LAN components include the 82562ET/82562EZ for basic Ethernet 10/100 connection, the 82562EM/ 82562EX component which provides an Ethernet 10/100 connection with the added manageability capabilities, the 82540EM Gigabit Ethernet Controller, and the 82551QM Fast Ethernet Controller.

Table 10-3. Platform LAN Component Overview

Platform LAN Connect Component	Interface to Intel® ICH4	Connection	Features
Intel® 82562EM (196 BGA)	PCI	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82551QM (196 BGA)	PCI	Performance 10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible
82562EM (48 pin SSOP) Intel® 82562EX (196 BGA)	LCI	10/100 Ethernet with Alert on LAN* (AoL) alerting	Ethernet 10/100 connection, Alert on LAN (AoL)
Intel® 82562ET (48 pin SSOP) Intel® 82562EZ (196 BGA)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

10.2.2 Ultra ATA/100 Support

The ICH4 supports the IDE controller with two sets of interface signals (Primary and Secondary) that can be independently enabled, tri-stated, or driven low. The component supports Ultra ATA/100, Ultra ATA/66, Ultra ATA/33, multiword PIO modes for transfers up to 100 MB/s.

10.2.3 Expanded USB Support

The ICH4 contains three UHCI Host Controllers and one EHCI Host Controller. Each UHCI Host Controller includes a root hub with two separate USB ports each for a total of six legacy USB ports. The EHCI Host Controller includes a root hub that supports up to six USB 2.0 ports. The ICH4 supports a maximum of six USB ports at any given time. The connection to either a UCHI or the EHCI is dynamic and is dependent on the USB device capability, meaning that all ports support HS/FS/LS.

10.2.4 Manageability and Other Enhancements

The ICH4 platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

10.2.4.1 SMBus 2.0

The ICH4 integrates an SMBus 2.0 controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on RAM, thermal sensors, PCI cards, etc. The slave interface allows an external microcontroller to access system resources.

The ICH4 platform integrates several functions designed to expand the capability of interfacing several components to the system.

10.2.4.2 Interrupt Controller

The interrupt capabilities of the ICH4 platform maintain the support for up to eight PCI interrupt pins and PCI 2.2 message-based interrupts. In addition, the ICH4 supports system bus interrupt delivery.

10.2.4.3 Intel® Compatible Firmware Hub (FWH)

The ICH4 platform supports the Intel® Compatible Firmware Hub BIOS memory size up to 8 MB for increased system flexibility.

10.2.5 AC ’97 6-Channel Support

The *Audio Codec ’97 Specification* (AC ’97) defines a digital interface that can be used to attach an audio codec (AC), a modem codec (MC), and/or an audio/modem codec (AMC) in various configurations. The AC ’97 defines the interface between the system logic and the audio or modem codec known as the “AC-link.”

The ICH4 platform's AC ’97 (with the appropriate codecs) improves overall platform integration by incorporating the AC-link. By using an audio codec, the AC-link allows for cost-effective, high-quality, integrated audio on the ICH4 platform. In addition, an AC ’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC ’97. The ICH4 integrated digital link allows several external codecs to be connected to the ICH4. The system designer can provide audio with an audio codec, a modem with a modem codec, or an integrated audio/modem codec (Figure 10-2). The digital link is expanded to support three audio codecs, or a combination two audio codecs and a modem codec (Figure 10-3 and Figure 10-5).

The digital link in the ICH4 is AC ’97 compliant, supporting up to three codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec.

The ICH4 expands audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center, and SubWoofer for a complete surround sound effect. The ICH4 has expanded support for three audio codecs on the AC-link.

Figure 10-2. AC ’97 with Audio/Modem Codec

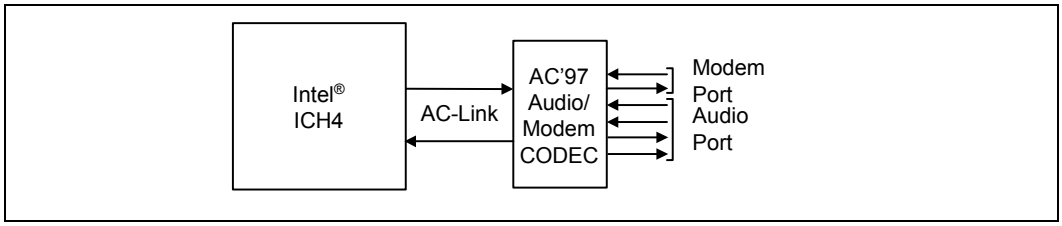


Figure 10-3. AC ’97 with Audio Codecs (4 Channel Secondary)

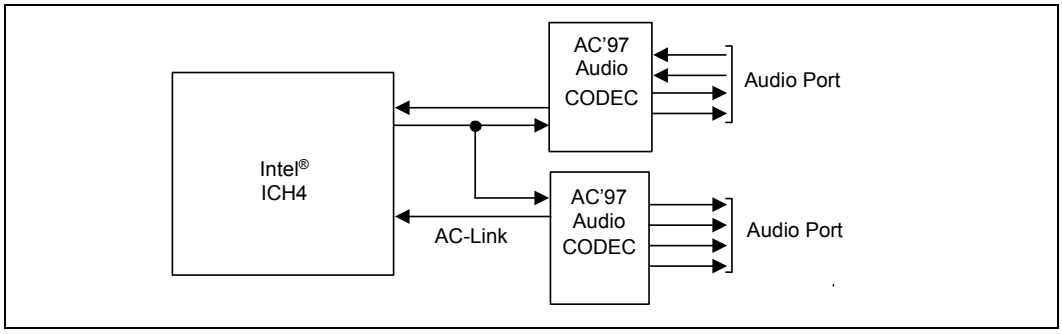


Figure 10-4. AC '97 with Audio and Modem Codec

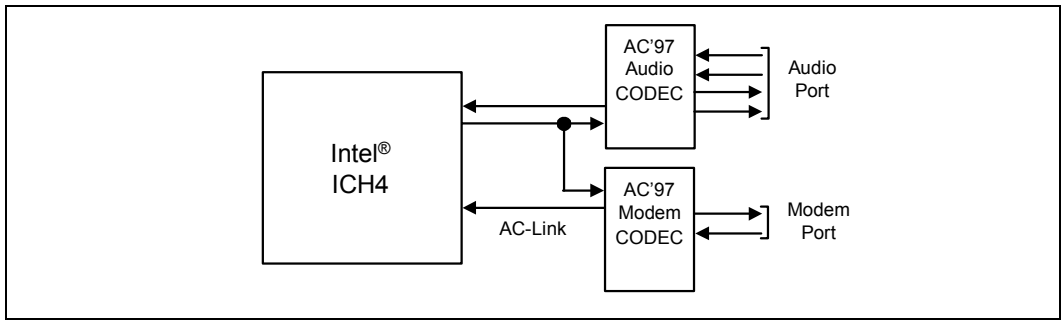
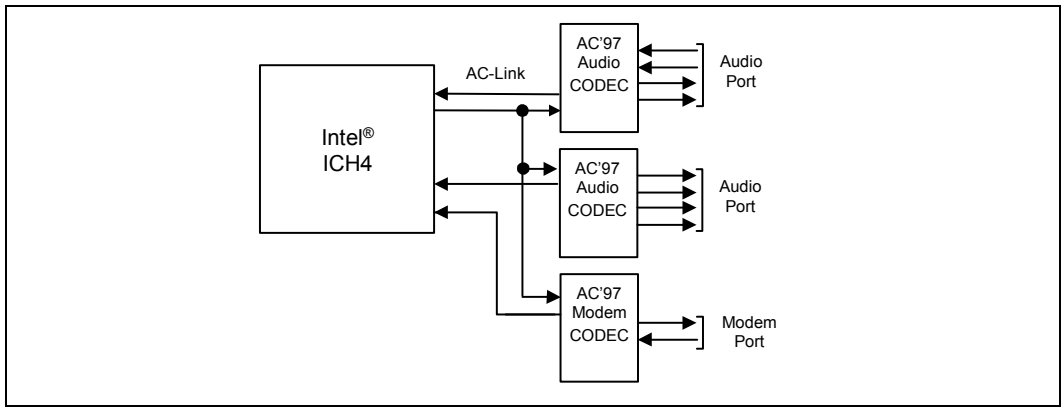


Figure 10-5. AC '97 with Two Audio and a Modem Codec (4 Channel Secondary)



10.3 Layout/Routing Guidelines

This section describes motherboard layout and routing guidelines for ICH4-based systems. This section does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

Warning: If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations be completed for each design.

Even when the guidelines are followed, critical signals should still be simulated to ensure proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely.

Warning: Any deviation from these guidelines must be simulated!

10.3.1 General Recommendations

The trace impedance typically noted (i.e., 60 Ω ± 15%) is the “nominal” trace impedance. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. Wider spaces also reduce crosstalk and settling time.

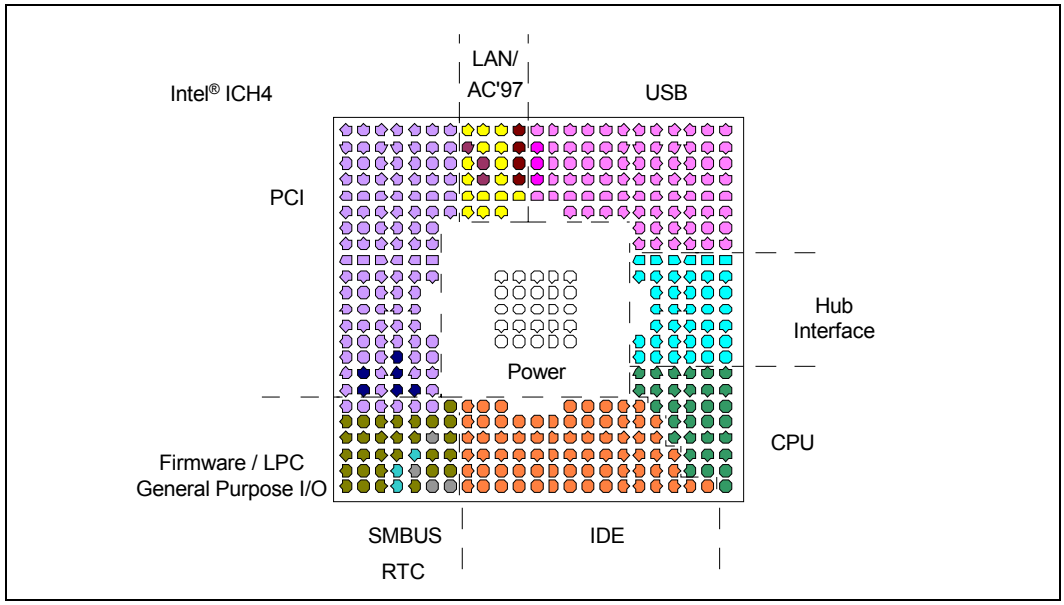
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. See Figure 4-2 for recommended trace width and spacing.

If this stack-up is not used, extremely thorough simulations of all interfaces must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

10.3.2 Component Quadrant Layout

The quadrant layouts shown are approximate, and the exact ball assignments should be used to conduct routing analysis. These quadrant layouts are designed for use during component placement.

Figure 10-6. Intel® ICH4 Component Quadrant Layout (Top View)



10.3.3 IDE Interface

This section contains guidelines for connecting and routing the ICH4 IDE interface. The ICH4 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement and signal termination for both IDE channels. The ICH4 has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 60 Ω traces (see Figure 4-2 for trace width and spacing), and must be less than 8 inches long (from ICH4 to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inch.

Table 10-4. IDE Routing Summary

Trace Impedance	IDE Routing Requirements	Maximum Trace Lengths	IDE Signal Length Matchin
51 Ω – 69 Ω, 60 Ω target	5 on 7	8 inches	No more than 0.5 inches (500 mils) between the shortest data signal and the longest strobe signal.

10.3.3.1 Cabling

Length of cable: Each IDE cable must be equal to or less than 18 inches.

Capacitance: Less than 35 pF.

Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).

Grounding: Provide a direct, low impedance chassis path between the motherboard ground and hard disk drives.

10.3.4 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH4 IDE Controller supports PIO, Multi-word (8237 style) DMA, Ultra DMA modes 0 through 5, and Native Mode IDE. Note that there are no motherboard hardware requirements for supporting Native Mode IDE. Native Mode IDE is supported through the operating system and system drivers. The ICH4 must determine the type of cable that is present to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra DMA modes greater than 2 (Ultra ATA/33). This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, grounnd, etc. All the ground wires are tied together on the cable, and are tied to the ground on the motherboard through the ground pins in the 40-pin connector. This cable conforms to the Small Form Factor Specification SFF-8049., which can be obtained from the Small Form Factor Committee.

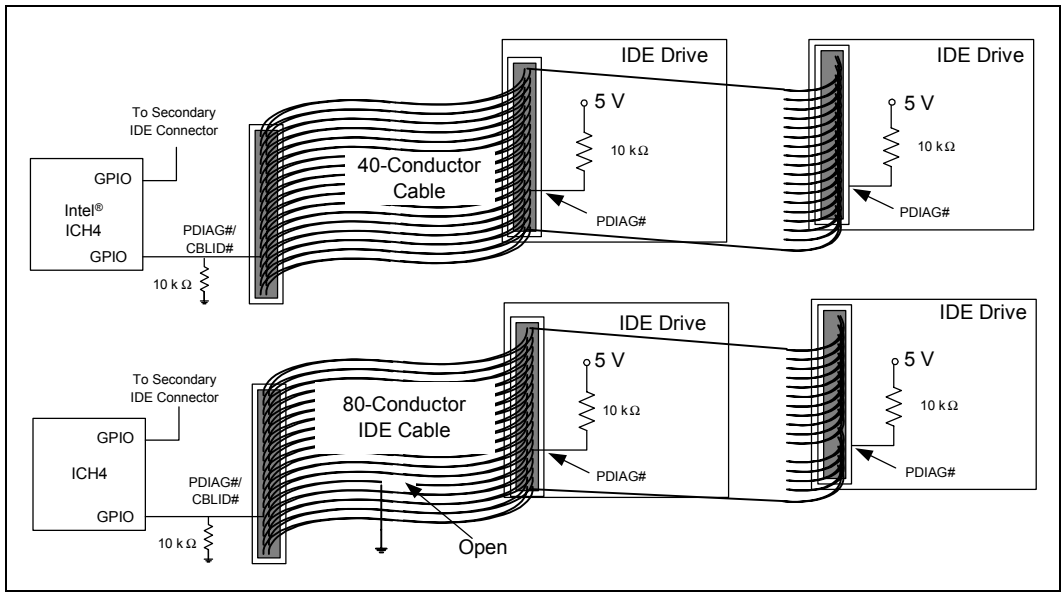
To determine if Ultra DMA modes greater than 2 (Ultra ATA/33) can be enabled, the ICH4 requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be performed using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system because this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

10.3.4.1 Combination Host-Side/Device-Side Cable Detection

Host side detection (described in the ATA/ATAPI-6 Standard) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 10-7. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. A 10 kΩ pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present, and allows for use of a non-5 V tolerant GPIO.

Figure 10-7. Combination Host-Side/Device-Side IDE Cable Detection



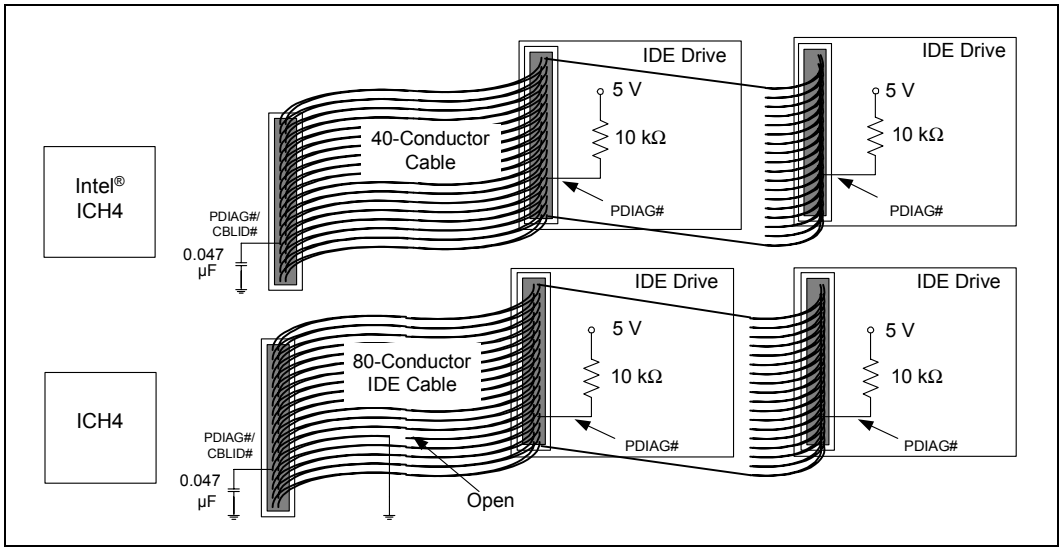
This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high there is 40-conductor cable in the system and Ultra DMA modes greater than 2 (Ultra ATA/33) must not be enabled.

If PDIAG#/CBLID# is detected low, there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-6 standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13 is a 1, an 80-conductor cable is present. If this bit is 0, a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present and should notify the user of the problem.

10.3.4.2 Device-Side Cable Detection

For platforms that must implement Device-Side detection only (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 10-8. This capacitor should not be populated when implementing the recommended combination Host-Side/Device-Side cable detection mechanism. Note that some drives may not support device-side cable detection.

Figure 10-8. Device Side IDE Cable Detection



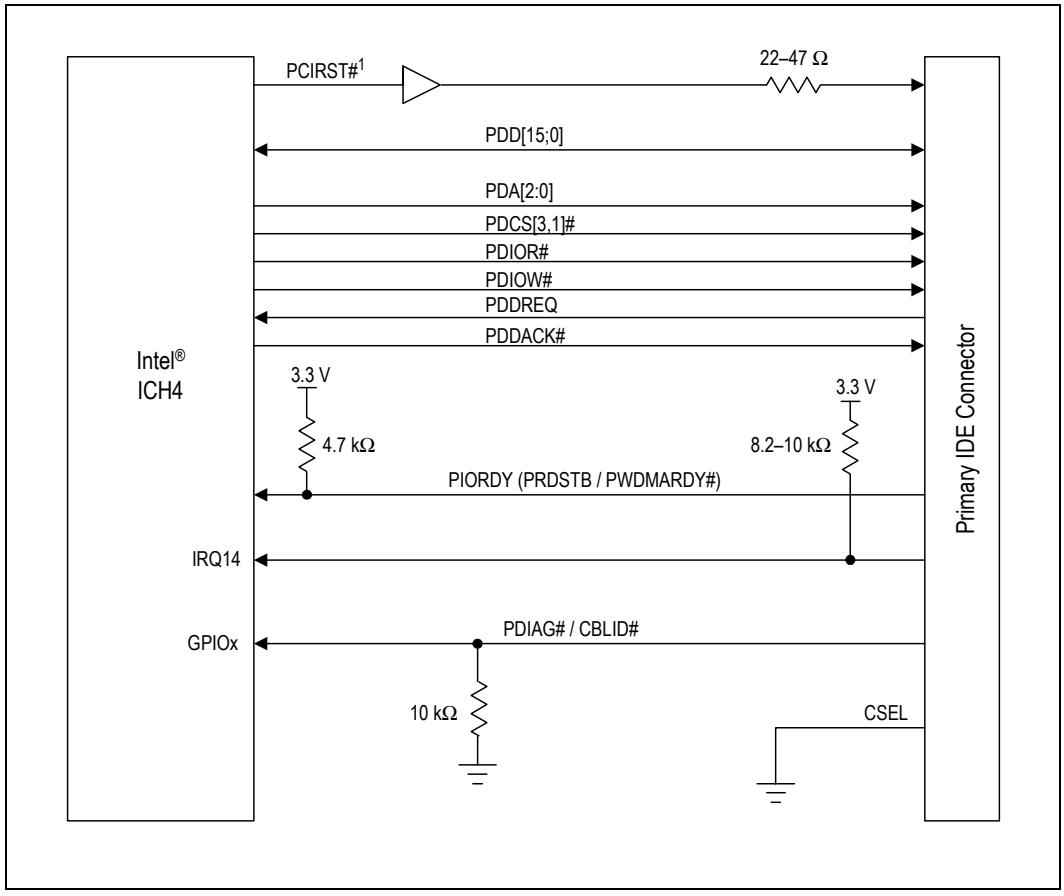
This mechanism creates a resistor-capacitor (RC) time constant. Drives supporting Ultra DMA modes greater than 2 (Ultra DMA/33) will drive PDIAG#/CBLID# low then release it (pulled up through a 10 kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host and therefore the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host. Therefore the signal will rise more slowly, as the capacitor charges. The drive can detect the difference in rise times and will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/ATAPI-4 Standard.

10.3.4.3 Primary IDE Connector Requirements

The requirements for the primary IDE connector are shown in Figure 10-9.

- A 22 Ω – 47 Ω series resistor is required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and to VCC3_3.
- A 4.7 kΩ pull-up resistor to VCC3_3 is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface

Figure 10-9. Connection Requirements for Primary IDE Connector



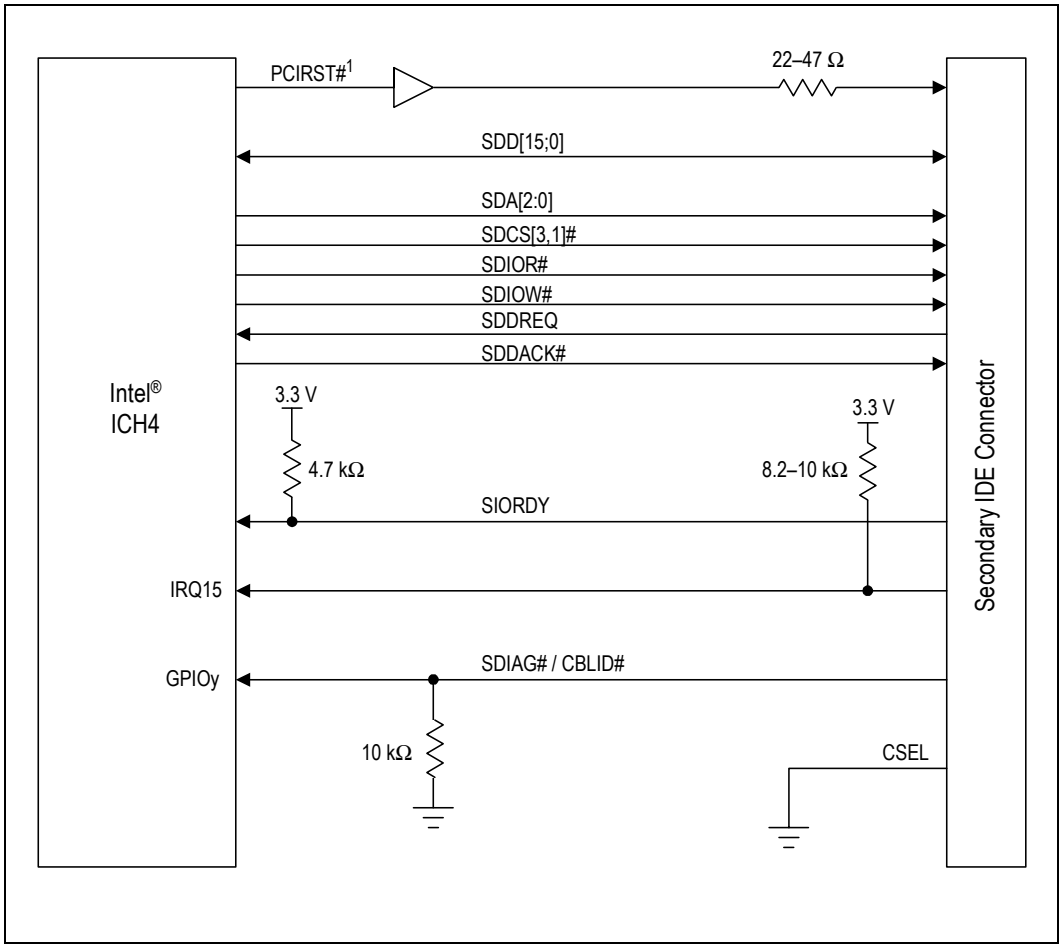
NOTES:
1. Due to ringing, PCIRST# must be buffered.

10.3.4.4 Secondary IDE Connector Requirements

The requirements for the secondary IDE connector are shown in Figure 10-10.

- 22 Ω – 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and to VCC3_3.
- A 4.7 kΩ pull-up resistor to VCC3_3 is required on PIORDY and SIORDY
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Secondary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

Figure 10-10. Connection Requirements for Secondary IDE Connector



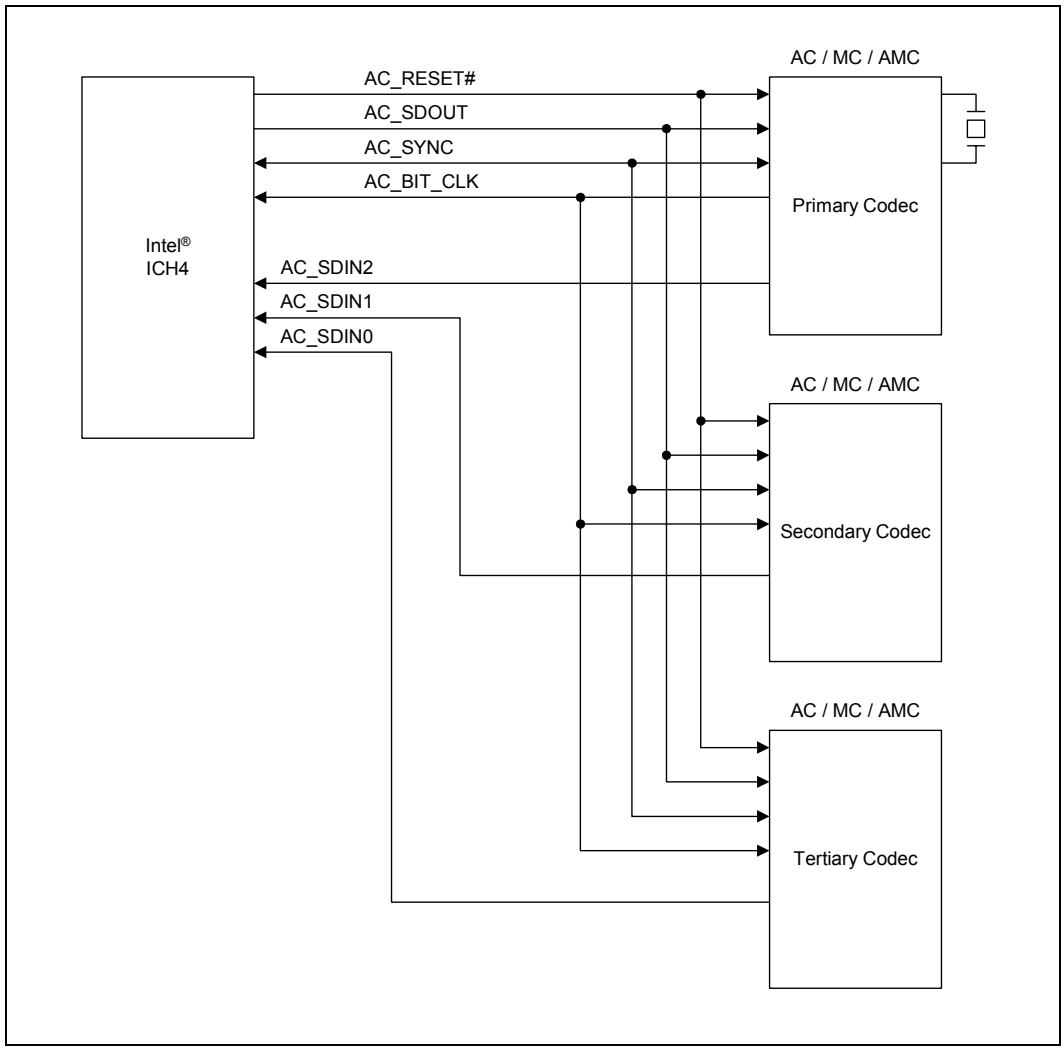
10.3.5 AC ’97

The ICH4 implements an AC ’97 compliant digital controller. Contact your codec IHV (Independent Hardware Vendor) for information on AC ’97 compliant products. The AC ’97 specification is on the Intel website:

http://developer.intel.com/ial/scalableplatforms/audio/

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams as well as control register accesses, employing a time division multiplexed (TDM) method. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH4 AC-link allows a maximum of three codecs to be connected. Figure 10-11 shows a three codec ICH4 AC-link topology.

Figure 10-11. Intel® ICH4 AC ’97—Codec Connection



NOTE: If a modem codec is configured as the primary AC-link Codec, there should not be any Audio Codecs residing on the AC-link.

Using the assumed 8-layer stack-up, the AC '97 interface can be routed using 60 Ω trace impedance (see Figure 4-2 for trace width and spacing). Maximum length between ICH4 to CODEC is 14 inches.

Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH4) and to any other codec present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK from the CK408 14.31818 MHz clock is not supported.**

The ICH4 supports wake on ring from S1-S5 via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4 has weak pull-downs/pull-ups that are always enabled. This keeps the link from floating when the AC-link is off, and when there are no codecs present.

Shut-off bit not set implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT will be driven by the codec and ICH4 respectively. However, AC_SDIN0, AC_SDIN1, and AC_SDIN2 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

Figure 10-12. Intel® ICH4 AC '97—Bitclock Topology

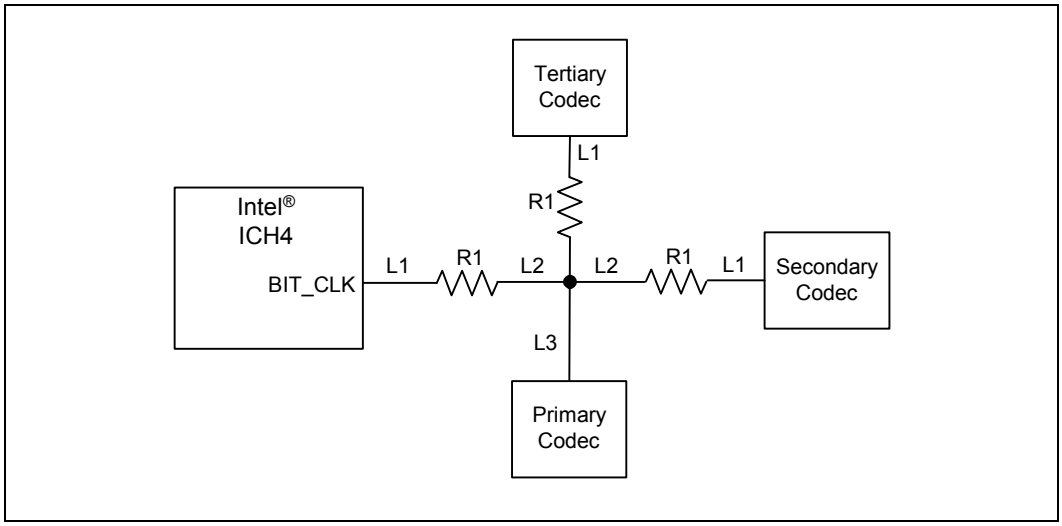


Table 10-5. Bitclock Routing Summary

AC '97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	Bit Clock Signal Length Matching
60 Ω trace impedance (see Figure 4-2 for trace width and spacing).	L1 = 1 inch to 8 inches L2 + L3 = 0.1 inch to 6.4 inches.	R1 = 33 to 47 Ω R2 = Optional 0 Ω resistor for debug purposes.	N/A

Figure 10-13. Intel® ICH4 AC '97—AC_SDOUT/AC_SYNC Topology

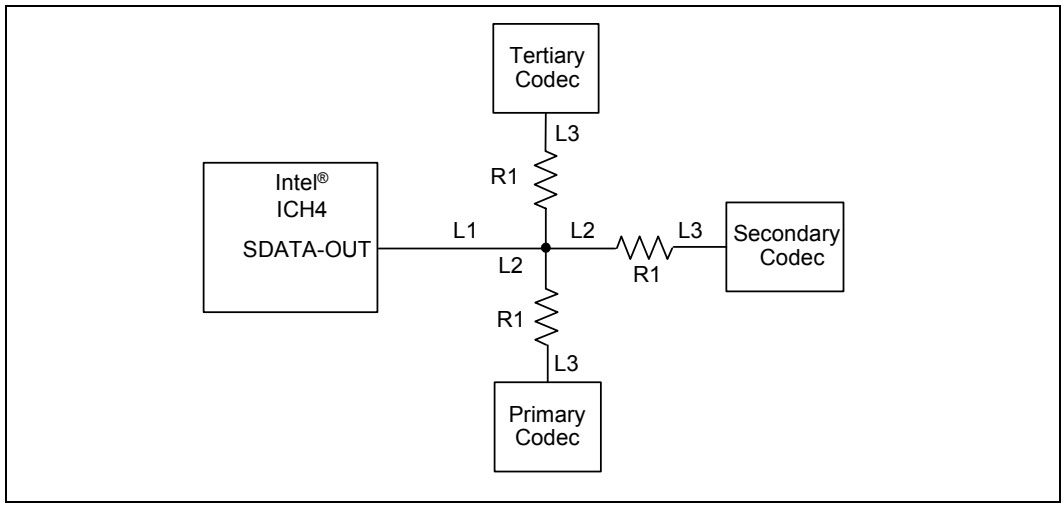


Table 10-6. AC_SDOUT/AC_SYNC Routing Summary

AC '97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	AC_SDOUT Signal Length Matching
60 Ω trace impedance (see Figure 4-2 for trace width and spacing).	L1 + L2 = 1 inch to 8 inches L3 = 1 inch to 4 inches.	R1 = 33 Ω (best if using an AD1885 codec) R1 = 47 Ω (best if using a CS4205b codec)	N/A

Figure 10-14. Intel® ICH4 AC '97—AC_SDIN Topology

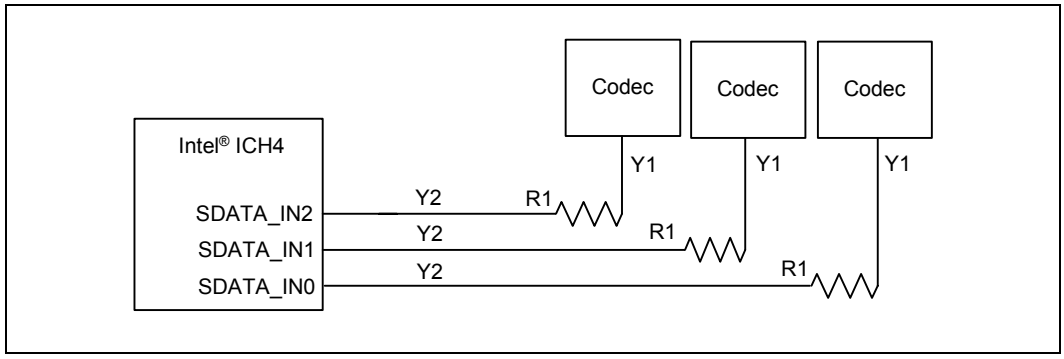


Table 10-7. AC_SDIN Routing Summary

AC '97 Routing Requirements	Maximum Trace Length	Series Termination Resistance	AC_SDIN Signal Length Matching
60 Ω trace impedance (see Figure 4-2 for trace width and spacing)	Y1 = 0.1 inch to 4 inches Y2 = 16 inches - Y1 inches	R1 = 33 Ω (best if using an AD1885 codec) R1 = 47 Ω (best if using a CS4205b codec)	N/A

10.3.5.1 AC ’97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area, and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins or should be positioned for the shortest connections to pins, and should have wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

10.3.5.2 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH4 platform using AC ’97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, and are based on the ICH4 platform.

- Active components such as FET switches, buffers and logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH4 supports wake-on-ring from S1 – S5 states via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs prevent the inputs from floating, so external resistors are not required.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

10.3.5.2.1 Valid Codec Configurations

Table 10-8. Valid Codec Configurations

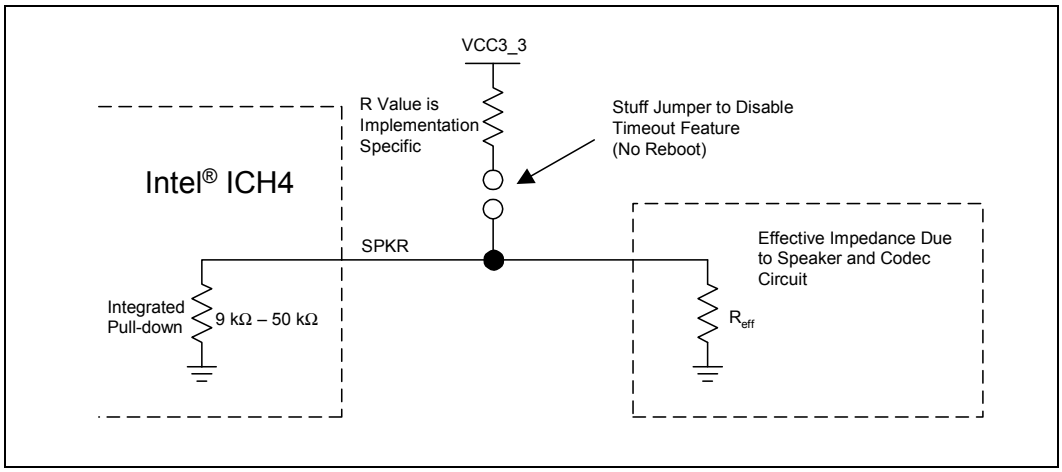
Option	Primary Codec	Secondary Codec	Tertiary Codec
1	Audio	Audio	Audio
2	Audio	Audio	Modem
3	Audio	Audio	Audio/Modem
4	Audio	Modem	Audio
5	Audio	Audio/Modem	Audio
6	Audio/Modem	Audio	Audio

NOTES:
1. For power management reasons, codec power management registers are in audio space. As a result, if there is an audio codec in the system it must be Primary. In addition, there cannot be two modems in a system because there is only one set of modem DMA channels.
2. The ICH4 supports a modem codec on any of the AC_SDIN lines. However, the Modem Codec ID must be either 00 or 01.

10.3.5.3 SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see Figure 10-15). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{eff}), and the ICH4's integrated pull-down resistor will be read as logic high (0.5 VCC3_3 to VCC3_3 + 0.5 V).

Figure 10-15. Example Speaker Circuit



10.3.6 USB 2.0

10.3.6.1 Layout Guidelines

10.3.6.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems

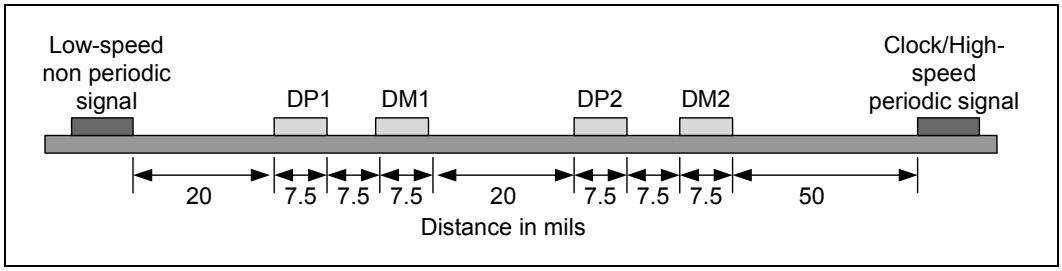
- Place the ICH4 and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, and power connectors).
- USB 2.0 signals should be **ground referenced**.
- Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
- When it becomes necessary to turn 90 degrees, use two, 45 degree turns or an arc (as shown in Figure 10-39) instead of making a single, 90 degree turn. This reduces reflections on the signal by minimizing impedance discontinuities .
- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Stubs on high speed USB signals should be avoided because stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.
- Route all traces over continuous planes (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 10.3.6.2.
- Separate signal traces into similar categories, and route similar signal traces together (such as routing differential pairs together).
- Keep USB 2.0 USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
- Follow the 20*h rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack-up, the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires, and helps prevent free radiation of the signal from the edge of the PCB.

10.3.6.1.2 USB 2.0 Trace Separation

Use the following separation guidelines. Figure 10-16 shows the recommended trace spacing.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. Deviations normally occur because of package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimum signal quality. This helps to prevent crosstalk.

Figure 10-16. Recommended USB Trace Spacing



10.3.6.1.3 USBRBIAS/USBRBIAS# Connection

The USBRBIAS pin and the USBRBIAS# pin can be shorted and routed 5 on 5 to one end of a 22.6 Ω ± 1% resistor to ground. Place the resistor within 500 mils of the ICH4 and avoid routing next to clock pins.

Figure 10-17. USBRBIAS/UBSRBIAS# Connection

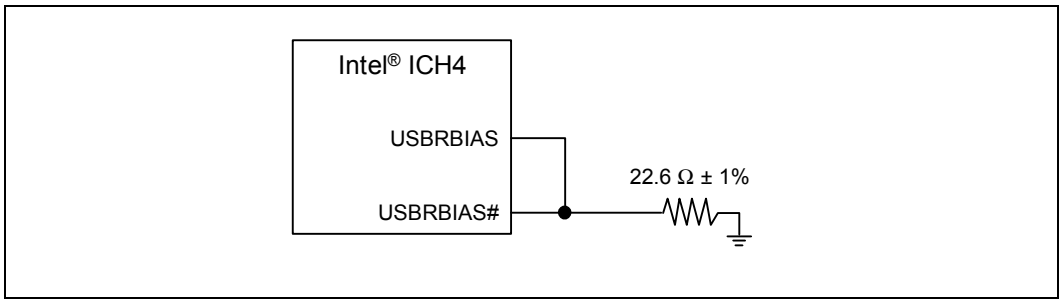


Table 10-9. USBRBIAS/USBRBIAS# Routing Summary

Trace Impedance	USBRBIAS/ USBRBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
51 Ω – 69 Ω, 60 Ω target	5 on 5	500 mils	N/A	N/A

10.3.6.1.4 USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See Section 10.3.6.4 for common-mode choke details.

10.3.6.1.5 USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should be no greater that 150 mils.

10.3.6.1.6 USB 2.0 Trace Length Guidelines

Use the trace length guidelines described in Table 10-10.

Table 10-10. USB 2.0 Trace Length Guidelines

<table>
<tr><th>USB 2.0 Routing Require-ments/ Trace Impedance</th><th>Config.</th><th>Signal Ref.</th><th>Signal Matching</th><th>Motherboard Trace Length</th><th>Card Trace Length</th><th>Maximum Total Length</th></tr>
<tr><td>7.5 on 7.5 /
77 Ω – 103 Ω differential,
90 Ω differential target</td><td>Back Panel</td><td rowspan="2">Ground</td><td rowspan="2">The max mismatch between data pairs should not be greater than 150 mils</td><td>17 inches</td><td>N/A</td><td>17 inches</td></tr>
<tr><td>7.5 on 7.5 /
77 Ω – 103 Ω differential,
90 Ω differ-ential target</td><td>Front Panel</td><td colspan="3"><table>
<tr><th>Cable Lengths</th><th>Motherboard Trace Length</th><th>Daughter Card Trace Length</th><th>Maximum Total Length</th></tr>
<tr><td>9</td><td>6</td><td>2</td><td>17</td></tr>
<tr><td>10.5</td><td>5</td><td>2</td><td>17.5</td></tr>
<tr><td>12</td><td>4</td><td>2</td><td>18</td></tr>
<tr><td>13.5</td><td>3</td><td>2</td><td>18.5</td></tr>
<tr><td>15</td><td>2</td><td>2</td><td>19</td></tr>
</table></td></tr>
</table>

NOTES:
1. These lengths are based upon simulation results and may be updated in the future.
   All lengths are based upon using a common-mode choke (see Section 10.3.6.4.1 for details on common-mode choke).
2. Numbers in this table are based on the following simulation assumption: an approximate 1:1 trade-off can be assumed for Motherboard Trace Length vs. Daughter card Trace Length (e.g., trade 1 inch of Daughter card for 1 inch of Motherboard Trace Lengths).
3. Routing guidelines are based on the stack-up assumptions described in Section 4.2).
4. Numbers in this table are based on the following simulation assumptions: (a) Trace length on front panel connector card assumed a maximum of 2 inches; (b) USB twisted-pair shielded cable as specified in USB 2.0 specification was used.
5. For front panel solutions, signal matching is considered from the ICH4 to the front panel header.

10.3.6.2 Plane Splits, Voids and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits, voids, and cut-outs.

10.3.6.2.1 VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the VCC plane:

1. Traces should not cross anti-etch because this greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces, as well as slower signal traces that might be coupled to them. USB signaling is not purely differential in all speeds (i.e., the Full-speed Single Ended Zero is common mode).
2. Avoid routing of USB 2.0 signals within 25-mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge or bypass power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates VCC5 and VCC3_3 planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to VCC5, and the other side should tie to VCC3_3. Stitching caps provide a high-frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

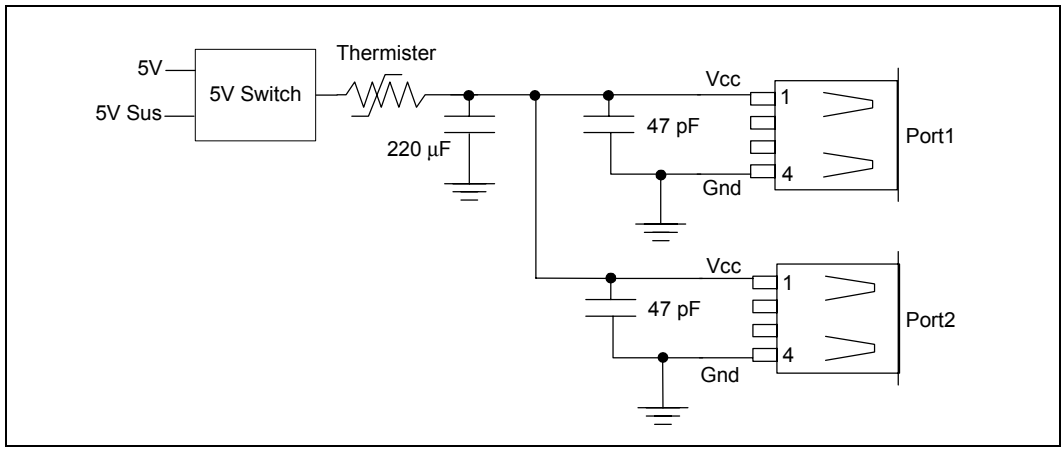
10.3.6.2.2 GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

10.3.6.3 USB Power Line Layout Topology

The following is a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop), and dynamic detach flyback protection. These two situations require both bulk capacitance (droop), and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port, and the power-carrying traces should be as wide as possible, preferably, a plane. A good practice is to make the power-carrying traces wide enough to allow the system fuse will blow during an over current event. If the system fuse is rated at 1 amp, the power-carrying traces should be wide enough to carry at least 1.5 amps.

Figure 10-18. Good Downstream Power Connection



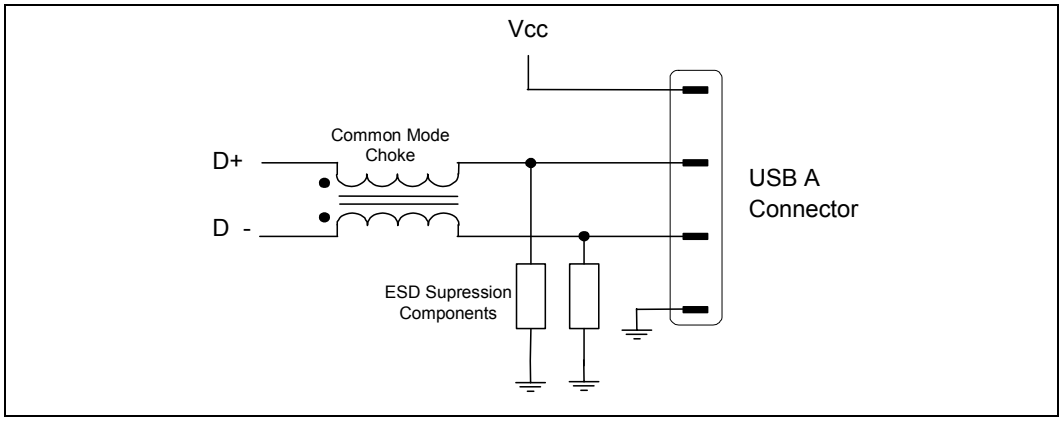
10.3.6.4 EMI Considerations

The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

10.3.6.4.1 Common Mode Chokes

Testing has shown that common-mode chokes can provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. The choke should be placed as close as possible to the USB connector signal pins. In systems that route USB to a front panel header, the choke should be placed on the front panel card. See Section 10.3.6.6.3.

Figure 10-19. A Common-Mode Choke



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion increases, so you should test the effects of the common mode choke on full speed and high-speed signal quality. Common Mode Chokes with a target impedance of 80 to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen, and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
2. Once you have a part that gives passing EMI results, test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed, and high-speed USB operation.

10.3.6.5 ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common mode choke and the USB connector data pins as shown in Figure 10-18. Other types of low-capacitance ESD protection devices may work as well, but were not investigated. As with the common mode choke solution, it is recommended that you include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

10.3.6.6 Front Panel Solutions

10.3.6.6.1 Cables

The front panel cable solution must meet all the requirements of Chapter 6 of the USB 2.0 Specification for high-/full-speed cabling for each port with the exceptions described in Cable Option 2. For more information, refer to the Intel FPIO design guideline available at:

http://www.formfactors.org/developer/fpio_design_guideline.pdf.

Internal Cable Option 1

Use standard High-speed/Full-speed compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the *USB 2.0 Specification*. Recommended motherboard mating connector pin-out is covered in detail later in this document.

Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 of the *USB 2.0 Specification* with the following additions/exceptions:

- They can share a common jacket, shield, and drain wire.
- Two ports with signal pairs that share a common jacket may combine Vbus and ground wires into a single wire provided the following conditions are met:
  - The bypass capacitance required by Section 7.2.4.1 of the *USB 2.0 Specification* is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughter card). Refer to the front panel daughter card referenced later for details.
  - Selecting proper wire size: A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the *USB 2.0 Specification* that has less than or equal to ½ the resistance of either of the two wires being combined. The data is provided for reference in Table 10-11.

Table 10-11. Conductor Resistance

American Wire Gauge (AWG)	Ohm (Ω) / 100 meters maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

NOTE: This is Table 6-6, USB 2.0 Specification.

Example: Two 24 gauge (AWG) power or ground wires can be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the USB 2.0 specification at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure that the system passes droop requirements. Cables that provide individual power and ground conductors for each port can usually meet droop requirements by providing adequate capacitance near the motherboard mating connector because droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients will be seen/dampened by the capacitance at the motherboard mating connector before they can cause problems with the adjacent port sharing the same cable. See Section 7.2.2 and 7.2.4.1 of the *USB 2.0 Specification* for more details.

Cables that contain more than two signal pairs are not recommended due to unpredictable impedance characteristics.

10.3.6.6.2 Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure that signal quality is not adversely affected because of a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the *USB 2.0 Specification*.

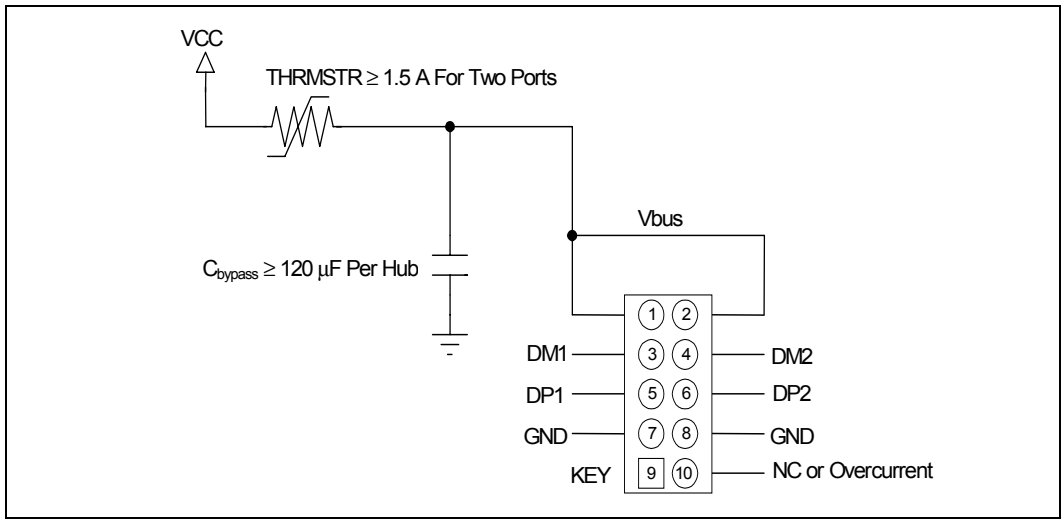
Pinout

A ten pin, 0.1-inch pitch stake pin assembly is recommended with the pinout listed in Table 10-12 and schematic shown in Figure 10-20.

Table 10-12. Front Panel Header Pinout

Pin	Description
1	VCC
2	VCC
3	dm1
4	dm2
5	dp1
6	dp2
7	Gnd
8	Gnd
9	key
10	No Connect or Over-Current Sense

Figure 10-20. Front Panel Header Schematic



It is **highly** recommended that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage.

- This protects the motherboard from damage in the case where an un-fused front panel cable solution is used.
- It also provides protection from damage if an un-keyed cable is inadvertently plugged onto the front panel USB connector.
- It provides protection to the motherboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between Vbus and ground.

Routing Considerations

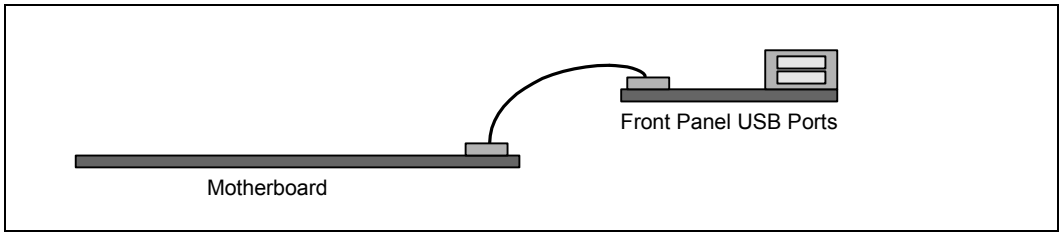
- Traces or surface shapes from VCC to the thermistor, to Cbypass, and to the connector power and ground pins should be at least 50 mils wide to ensure adequate current carrying capability.
- There should be double vias on power and ground nets, and the trace lengths should be kept as short as possible.

10.3.6.6.3 Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 10-21 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card. For more information, refer to the Intel FPIO design guideline available at:

http://www.formfactors.org/developer/fpio_design_guideline.pdf.

Figure 10-21. Motherboard Front Panel USB Support



When designing the motherboard with front/side panel support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure that there aren't duplicate EMI/ESD/thermistor components placed on the motherboard because this will usually cause drop/droop and signal quality degradation or failure.

Front Panel Daughter Card Design Guidelines

- Place the Vbus bypass capacitance, Common Mode Choke, and ESD suppression components on the daughter card as close as possible to the connector pins.
- Follow the same layout, routing and impedance control guidelines as specified for motherboards.
- Minimize the trace length on the front panel connector card. Less than 2-inch trace length is recommended.
- Use the same mating connector pin-out as outlined for the motherboard in Section 10.3.6.6.2.
- Use the same routing guidelines as described in Section 10.3.6.1.
- Trace length guidelines are given in Table 10-10.

10.3.7 I/O APIC Design Recommendation

The processor does not support I/O APIC. Follow these recommendations.

- **On the ICH4**
  - — Tie APICCLK directly to ground
  - — Tie APICD0, APICD1 to ground through a 10 kΩ resistor (Separate pull-downs are required if using XOR chain testing.)
- **On the Processor**
  - — Consult processor documentation

10.3.8 SMBus 2.0/SMLink Interface

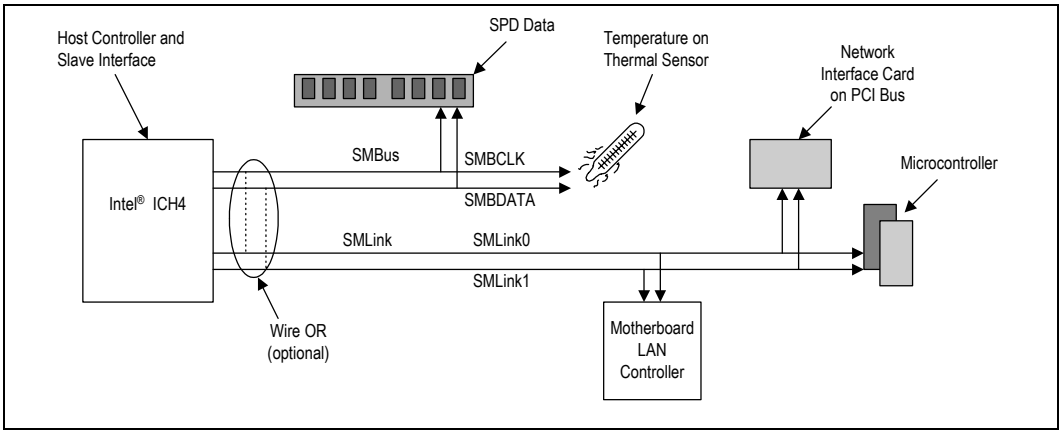
The SMBus interface on the ICH4 uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH4.

The ICH4 incorporates an SMLink interface that supports Alert on LAN*, Alert on LAN2*, and a slave functionality. It uses two signals SMLINK[1:0]. SMLINK0 corresponds to an SMBus clock signal, and SMLINK1 corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert on LAN* functionality, the Intel ICH4 transmits heartbeat and event messages over the interface. When using the 82562EM/82562EX Platform LAN Connect Component, the ICH4's integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert on LAN2-enabled LAN Controller (e.g., 82562EM/82562EX 10/100 Mbps Platform LAN Connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4 SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (e.g., 82562EM/82562EX 10/100 Mbps Platform LAN Connect) to access targets on the SMBus as well as the ICH4 Slave interface. Additionally, the ICH4 supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals must be tied together externally. This is done by connecting SMLink0 to SMBCLK, and SMLink1 to SMBDATA.

Figure 10-22. SMBUS 2.0/SMLink Interface



NOTE: Intel does not support external access of the ICH4's Integrated LAN Controller via the SMLink interface, and does not support access of the ICH4's SMBus Slave Interface by the ICH4's SMBus Host Controller. Refer to the ICH4 datasheet for full functionality descriptions of the SMLink and SMBus interface.

10.3.8.1 SMBus Architecture and Design Considerations

10.3.8.1.1 SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging because they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise times.

Primary considerations in the design process are:

- Device class (High/Low power). Most designs use primarily high-power devices.
- Are there devices that must run in S3?
- Amount of VCC_suspend current available (i.e., minimizing load of VCC_suspend).

10.3.8.1.2 General Design Issues / Notes

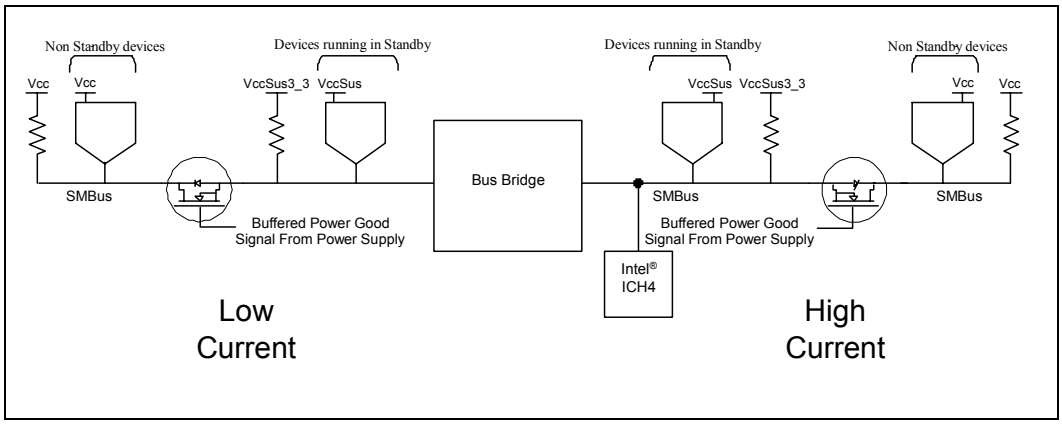
Regardless of the architecture used, there are some general considerations.

- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor can not be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and fall time specification.
- The maximum bus capacitance that a physical segment can reach is 400 pF.
- The ICH4 does not run SMBus cycles while in S3.
- SMBus devices that can operate in STR must be powered by the VCC_suspend supply.
- If SMBus is to be connected to PCI it must be connected to all PCI slots.

10.3.8.1.3 High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices while allowing SMBus devices to communicate while in S3. VCC_suspend leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of an “FET” to isolate the devices powered by the core and suspend supplies (See Figure 10-23).

Figure 10-23. High Power/Low Power Mixed Vcc_suspend/VCC Architecture



Added Considerations for Mixed Architecture

- The bus switch must be powered by VCC_suspend.
- Devices that are powered by the VCC_suspend well must not drive into other devices that are powered off. This is accomplished with the “bus switch.”
- The bus bridge can be a device like the Phillips PCA9515.

10.3.8.2 Calculating The Physical Segment Pull-Up Resistor

Table 10-13 and Table 10-14 are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. If any physical bus segment exceeds 400 pF, a bus bridge device like the Phillips PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 10-13. Bus Capacitance Reference Chart

Device	No. of Devices / Trace Length	Capacitance Includes	Capacitance (pF)
Intel® ICH4	1	Pin Capacitance	12
CK408	1	Pin Capacitance	10
DIMMS	2	Pin Capacitance (10 pF) + 1 inch worth of trace capacitance (2 pF/inch) per DIMM and 2 pF connector capacitance per DIMM	28
	3		42
PCI Slots	2	Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector	86
	3		129
	4		172
	5		215
	6		258
SMBus Trace Length (inches)	≥24	2 pF per inch of trace length	48
	≥36		72
	≥48		96

Table 10-14. Bus Capacitance/Pull-Up Resistor Relationship

Physical Bus Segment Capacitance	Pull-Up Range (For VCC = 3.3 V)
0 to 100 pF	8.2 kΩ to 1.2 kΩ
100 to 200 pF	4.7 kΩ to 1.2 kΩ
200 to 300 pF	3.3 kΩ to 1.2 kΩ
300 to 400 pF	2.2 kΩ to 1.2 kΩ

10.3.9 PCI

The ICH4 provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH4 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

The ICH4 supports six PCI Bus masters (excluding the ICH4) by providing six REQ#/GNT# pairs. In addition, the ICH4 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

10.3.9.1 PCI Routing Summary

The following represents a summary of the routing guidelines for the PCI Slots. Simulations assume that PCI cards follow the *PCI Local Bus Specification, Revision 2.2* trace length guidelines.

Figure 10-24. PCI Bus Layout Example

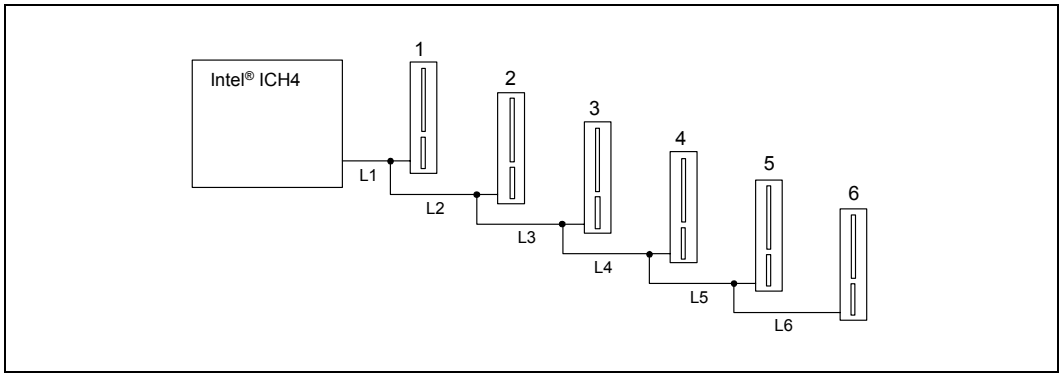


Figure 10-25. PCI Bus Layout Example with IDSEL

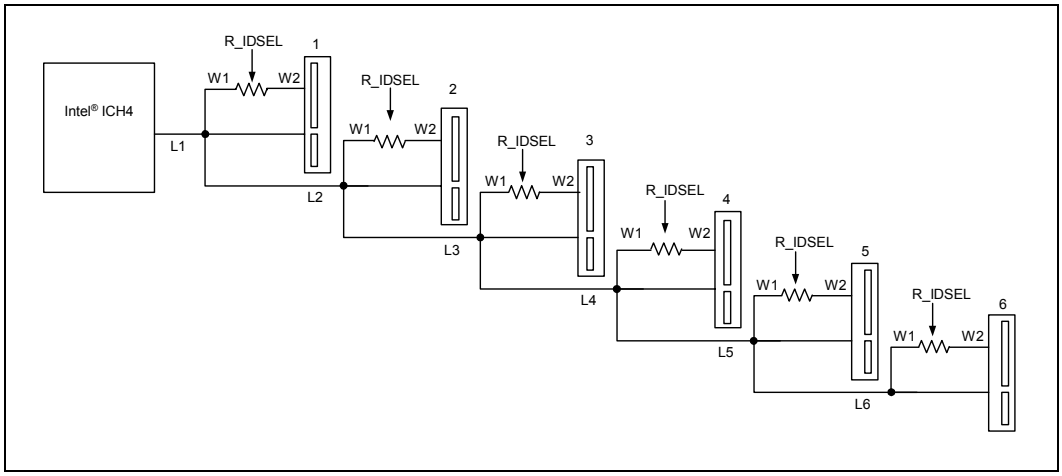


Table 10-15. PCI Data Signals Routing Summary

PCI Routing Requirements	Trace Impedance	Topology	Maximum Trace Length					
			L1	L2	L3	L4	L5	L6
5 on 7 (Based on stack-up described in Chapter 5).	47 Ω – 69 Ω, 60 Ω target	2 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	4 to 10 inches	1.5 inches	N/A	N/A	N/A	N/A
		3 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	4 to 10 inches	1.5 inches	1.5 inches	N/A	N/A	N/A
		4 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	4 to 10 inches	1.0 inches	1.0 inches	1.0 inches	N/A	N/A
	51 Ω – 69 Ω, 60 Ω target	5 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	5 to 8 inches	1.0 inches	1.0 inches	1.0 inches	1.0 inches	N/A
		6 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	5 to 7 inches	1.0 inches	1.0 inches	1.0 inches	1.0 inches	1.0 inches

Figure 10-26. PCI Clock Layout Example

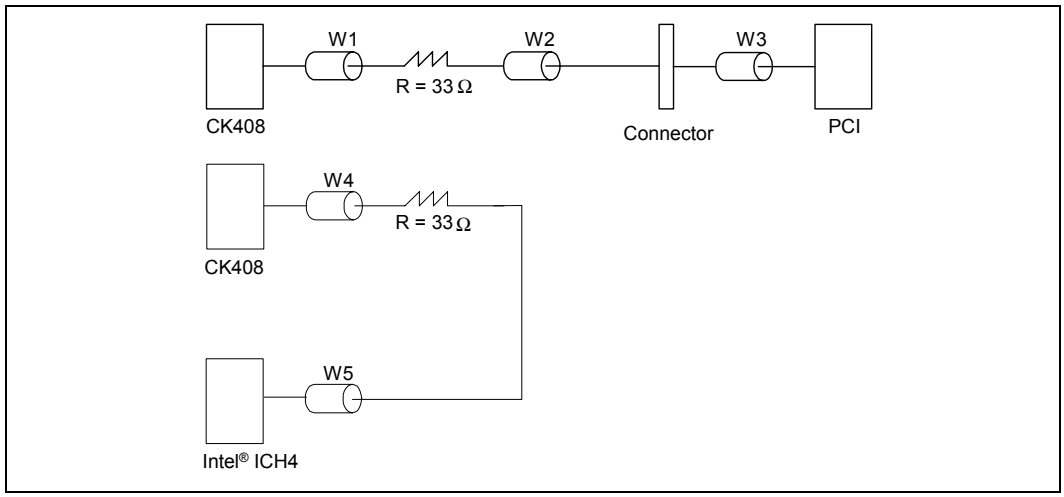


Table 10-16. PCI Clock Signals Routing Summary

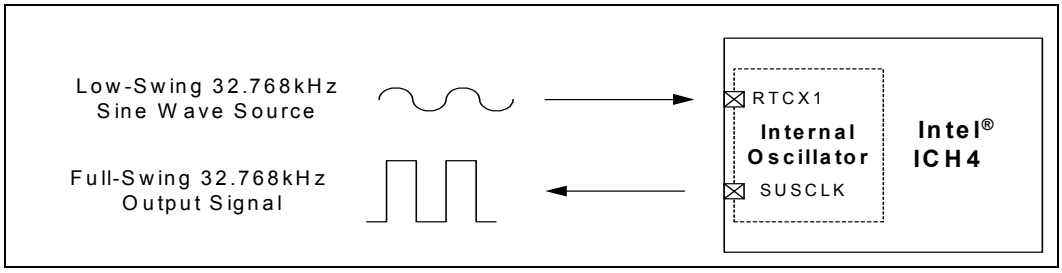
Trace Impedance	PCI Routing Requirements	Topology	Maximum Trace Length				
			W1	W2	W3	W4	W5
51 Ω – 69 Ω, 60 Ω target	5 on 7	2 – 6 slots	0.5 inches	(W5 – 4.5) inches	2.5 inches (shown as reference only)	0.5 inches	Can be as long as needed as long as W2 is scaled accordingly

10.3.10 RTC

The ICH4 contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time, and storing system data in its RAM when the system is powered down.

The ICH4 uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4, the RTCX1 signal is amplified to drive internal logic as well as to generate a free running full swing clock output for system use. This output ball of the ICH4 is called SUSCLK. This is shown in Figure 10-27.

Figure 10-27. RTCX1 and SUSCLK Relationship in Intel® ICH4

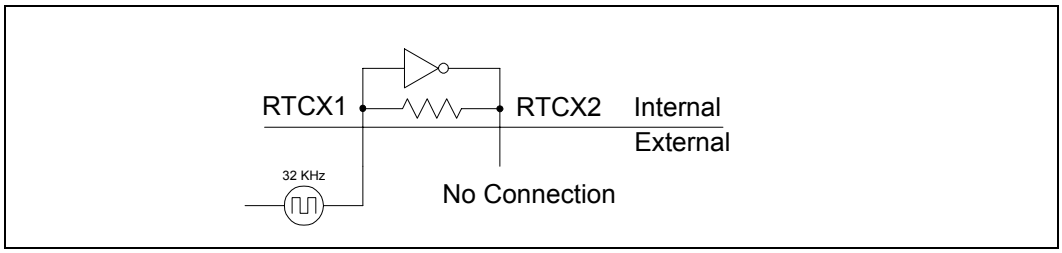


For further information on the RTC, consult Application Note AP-728 *ICH/ICH4/ICH4-M/ ICH3-S/ICH3-M Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*. This application note is valid for ICH4.

Even if the ICH4 internal RTC is not used, it's still necessary to supply a clock input to RTCX1 of the ICH4 because other signals are gated from that clock in suspend modes. However, in this case the frequency accuracy (32.768 kHz) of the clock inputs is not critical; a cheap crystal can be used, or a single clock input can be driven into RTCX1 with RTCX2 left as no connect. Figure 10-28 shows the connection. This is not a validated feature on ICH4.

Note: The peak-to-peak swing on RTCX1 cannot exceed 1.0 V.

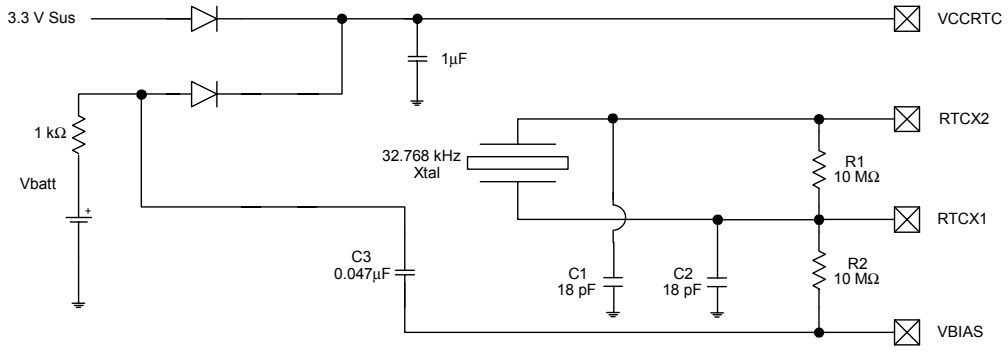
Figure 10-28. External Circuitry for the Intel® ICH4 (Internal RTC is Not Used)



10.3.10.1 RTC Crystal

The ICH4 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. The following figure documents the external circuitry that comprises the oscillator of the ICH4 RTC.

Figure 10-29. External Circuitry for the Intel® ICH4 RTC



Notes:
1. Reference designators are arbitrarily assigned.
2. 3.3V Sus is active whenever the system is plugged In.
3. Vbatt is the voltage provided by the battery .
4. VBIAS, VCCRTC, RTCX1, and RTCX2 are Intel® ICH4 pins.
5. VBIAS is used to bias the ICH4 Internal Oscillator.
6. VCCRTC powers the RTC well of the ICH4.
7. RTCX1 is the input to the Internal Oscillator.
8. RTCX2 is the feedback for the external crystal.

NOTES:
1. The exact capacitor value must be based on the crystal maker recommendations. (Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF).
2. VccRTC: Power for RTC Well.
3. RTCX2: Crystal Input 2 – connected to the 32.768 kHz crystal.
4. RTCX1: Crystal Input 1 – connected to the 32.768 kHz crystal.
5. VBIAS: RTC BIAS Voltage – This ball is used to provide a reference voltage, and this DC voltage sets a current that is mirrored throughout the oscillator and buffer circuitry.
6. VSS: Ground.

Table 10-17. RTC Routing Summary

Trace Impedance	RTC Routing Requirements	Maximum Trace Length to Crystal	Signal Length Matching	R1, R1, C1, and C2 Tolerances	Signal Referencing
51 Ω – 69 Ω, 60 Ω target	5-mil trace width (results in ~2 pF per inch)	1 inch	N/A	R1 = R2 = 10 MΩ ± 5% C1 = C2 = (NPO class) See Section 10.3.10.2 for calculating a specific capacitance value for C1 and C2	Ground

10.3.10.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C3 must be 0.047 µF, and capacitor values C1 and C2 should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})] / [(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

- C_{load} = Crystal's load capacitance. This value can be obtained from Crystal's specification.
- C_{in1}, C_{in2} = input capacitances at RTCX1, RTCX2 balls of the ICH4. These values can be obtained in the ICH4 datasheet.
- C_{trace1}, C_{trace2} = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 pins. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. Typical value, based on a 5-mil wide trace and a ½ ounce copper pour, is approximately equal to:

  C_{trace} = trace length * 2 pF/inch (assuming a 5-mil trace ½ oz. copper)

- $C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the exist of 2 electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C1, C2 can be chosen such that C1 = C2. Using the equation of C_{load} above, the value of C1, C2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C2 can be chosen such that C2 > C1. Then C1 can be trimmed to obtain the 32.768 kHz.

In certain conditions, both C1, C2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C1, C2 value are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example illustrates the use of the practical values C1, C2 in the case that theoretical values can not guarantee the accuracy of the RTC in low temperature condition.

Example

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH4, the calculated values of C1 = C2 is 10 pF at room temperature (25 °C) to yield an 32.768 kHz oscillation.

At 0 °C the frequency stability of crystal gives -23 ppm (assumed that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C1, C2 are chosen to be 6.8 pF instead of 10 pF, the RTC oscillates at higher frequency at room temperature (+23 ppm), but this configuration of C1 / C2 makes the circuit oscillate closer to 32.768 kHz at 0 °C. The 6.8 pF value of C1 and C2 is the practical value.

Note that the temperature dependency of crystal frequency is a parabolic relationship (ppm / degree square). The effect of changing crystal's frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature).

10.3.10.3 RTC Layout Considerations

Because the RTC circuit is very sensitive and requires highly accurate oscillation, reasonable care must be taken during RTC circuit layout and routing . Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. ICH4 requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn pin). Routing the RTC circuit should be kept simple to simplify the trace length measurement and to increase accuracy when calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board material. On FR-4, a 5-mil trace has approximately 2 pF per inch.
- Trace signal coupling must be reduced by avoiding routing of adjacent PCI signals close to RTCX1 and RTCX1, VBIAS.
- Ground guard plane is highly recommended.
- The oscillator VCC should be clean—use a filter (e.g., a RC low-pass) or a ferrite inductor.

10.3.10.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH4 is not powered by the system.

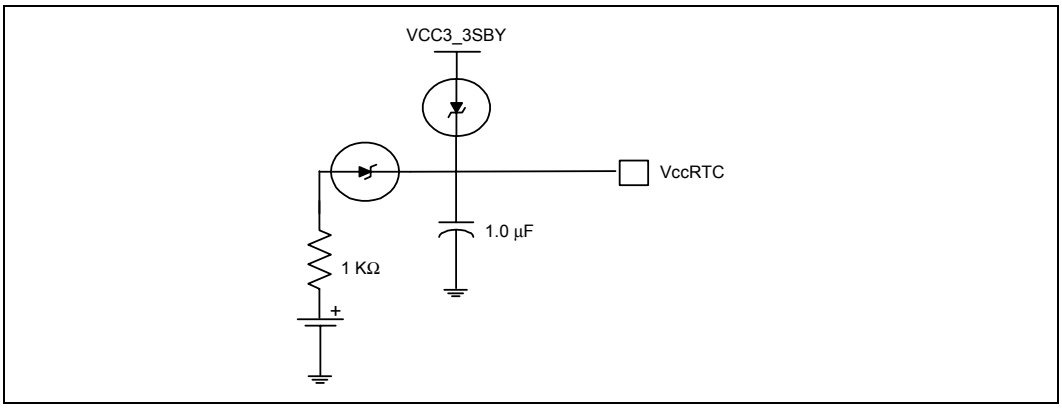
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 µAh (assumed usable) and the average current required is 3 µA, the battery life will be at least:

170,000 µAh / 5µA = 34,000 h = 3.9 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH4 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH4 RTC well to be powered by the battery when the system power is not available, and by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 10-30 is an example of a diode circuit that is used.

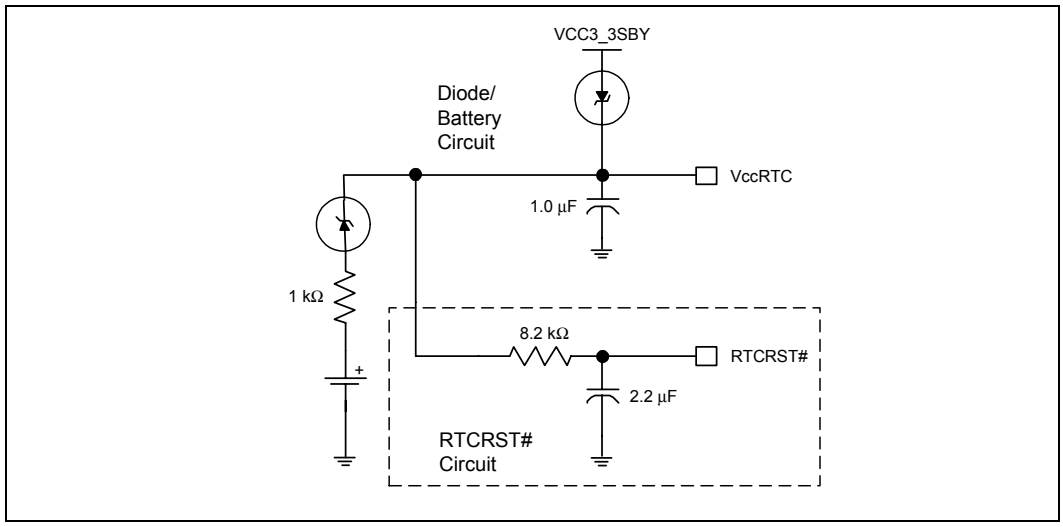
Figure 10-30. A Diode Circuit to Connect RTC External Battery



A standby power supply should be used to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

10.3.10.5 RTC External RTCRST# Circuit

Figure 10-31. RTCRST# External Circuit for the Intel® ICH4 RTC



The ICH4 RTC requires additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18 ms–25 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1 and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in the Figure 10-30) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 10-31 is and example of this circuitry that is used in conjunction with the external diode circuit.

10.3.10.6 VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC Network of R2 and C3 (see Figure 10-29). Therefore, it is a self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200 mV DC. The RC network of R2 and C3 will filter out most of AC signal that exists on this ball. However, the noise on this ball should be kept minimal to guarantee the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details on measuring techniques.

Note: VBIAS is also very sensitive to environmental conditions.

10.3.10.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30%–70%. If the SUSCLK duty cycle is beyond the 30%–70% range, the oscillation signal on RTCX1 and RTCX2 is poor.

SUSCLK can be probed directly using normal probe (50 Ω input impedance probe), and is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH4's RTC Clock (see Application Note AP-728 for further details).

10.3.10.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VccRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 10-31 meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VccRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent I_{CCRTC} leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

10.3.11 Internal LAN Layout Guidelines

The ICH4 provides several options for LAN capability. The platform supports several components, depending upon the target market. Available LAN components include the the 82540EM Gigabit Ethernet Controller, the 82551QM Fast Ethernet Controller, the 82562EZ/82562ET, and the 82562EX/82562EM Platform LAN Connect components.

Table 10-18. Platform LAN Component Overview

Platform LAN Connect Component	Interface to Intel® ICH4	Connection	Features
Intel® 82562EM (196 BGA)	PCI	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82551QM (196 BGA)	PCI	Performance 10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible
82562EM (48 pin SSOP) Intel® 82562EX (196 BGA)	LCI	10/100 Ethernet with Alert on LAN (AoL) alerting	Ethernet 10/100 connection, Alert on LAN (AoL)
Intel® 82562ET (48 pin SSOP) Intel® 82562EZ (196 BGA)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

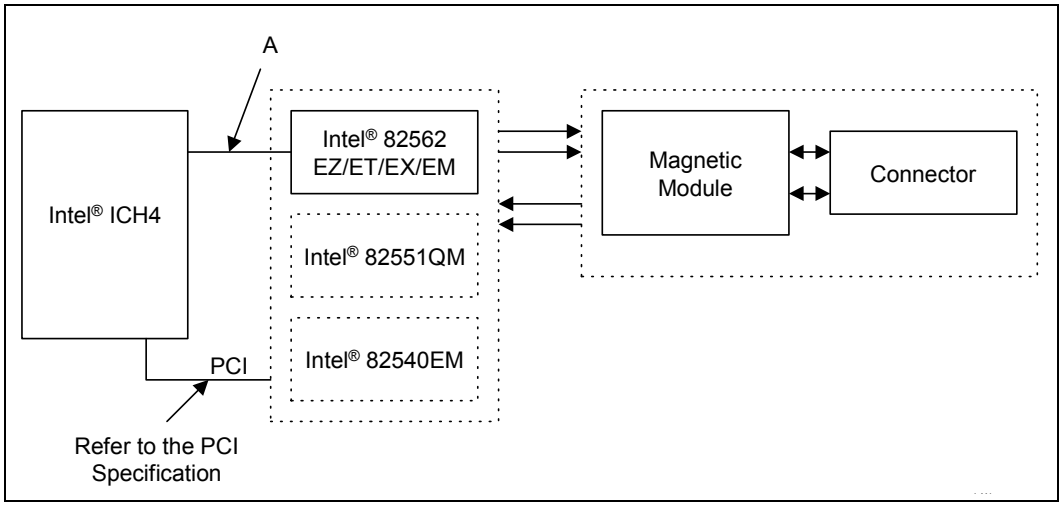
Which LAN component to use on the ICH4 platform will depend on the end-user's need for connection speed, manageability needs, and bus connection type. In addition, footprint compatible packages make it possible to design a platform that can use any of the LAN components without the need for a motherboard redesign.

10.3.11.1 Footprint Compatibility

The 82540EM Gigabit Ethernet Controller, 82551QM Fast Ethernet Controller, and the 82562EX/82562EZ Platform LAN Connect devices are all manufactured in a footprint compatible 15 mm x 15 mm (1 mm pitch), 196-ball grid array package. Many of the critical signal pin locations on the 82540EM, 82551QM, and 82562EX/82562EZ are identical, allowing designers to create a single design that accommodates any one of these parts. Because the usage of some pins on the 82540EM differ from the usage on the 82551QM or the 82562EX/82562EZ, the parts are not referred to as "pin compatible." The term "footprint compatible" refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design. Therefore, it is easy to populate a single board design with either part to maximize value while matching the customers' performance needs.

Design guidelines are provided for each required interface and connection. Refer to Figure 10-32 and Table 10-19 for the corresponding section of the design guide. The guidelines use the 82546EZ to refer to both the 82562EZ and 82562EX. The 82562EX is specified in those cases where there is a difference.

Figure 10-32. Intel® ICH4/Platform LAN Connect Sections



NOTE: 82562EZ/EX, 82551QM, and 82540EM are footprint compatible with each other. 82562ET/EM are footprint compatible with each other.

Table 10-19. LAN Design Guide Section Reference

Layout Section	Figure 10-32 Reference	Design Guide Section
ICH4 – LAN Connect Interface (LCI)	A	Section 10.3.11.2, "Intel® ICH4 – LAN Connect Interface Guidelines"
Intel® 82562EZ/EX Intel® 82562ET/EM	A	Section 10.3.11.2, "Intel® ICH4 – LAN Connect Interface Guidelines"

10.3.11.2 Intel® ICH4 – LAN Connect Interface Guidelines

This section contains guidelines on how to implement a Platform LAN Connect device on a system motherboard. It should not be treated as a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals. The following are guidelines for the ICH4 to LAN Connect Interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports 82562ET and 82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD0, and LAN_TXD0 are shared by all components.

10.3.11.2.1 Bus Topologies

The Platform LAN Connect Interface can be configured in several topologies:

- Direct point-to-point connection between the ICH4 and the LAN component
- LOM Implementation

LOM (Lan On Motherboard) Interconnect:

The following are guidelines for a single solution motherboard. Either 82562EZ/ET, 82562EX/EM are uniquely installed.

Figure 10-33. Single Solution Interconnect

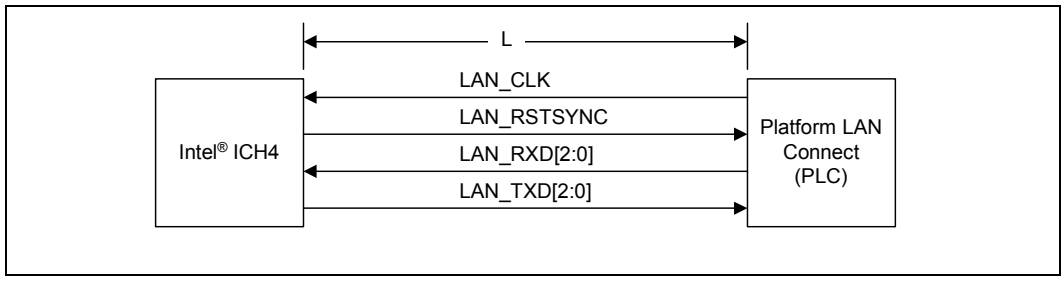


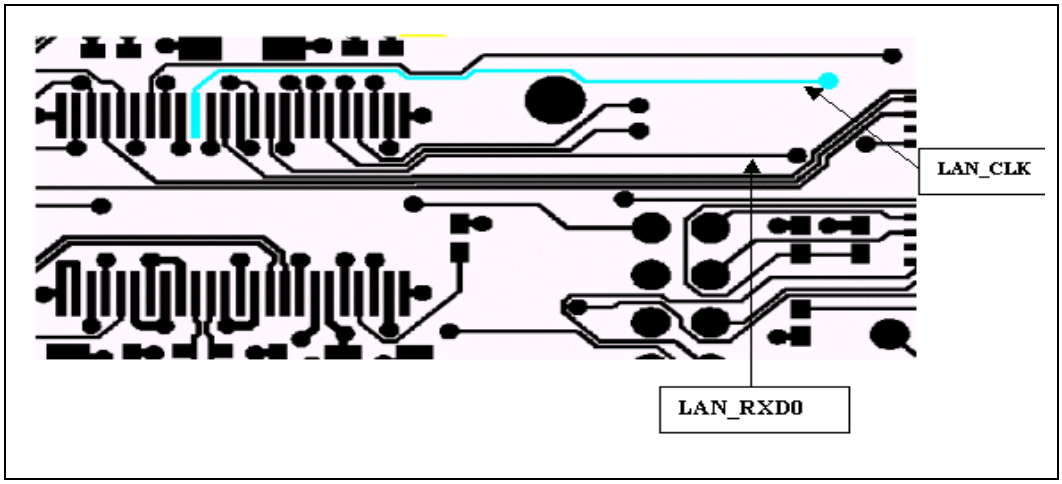
Table 10-20. LAN LOM Routing Summary

Component	Maximum Trace Length	Trace Impedance	LAN Routing Requirements	Signal Referencing	LAN Signal Length Matching
Intel® 82562EZ/ ET/EX/EM	4.5 to 12 inches	51 Ω – 69 Ω, 60 Ω target	5 on 10 (Based on stack-up described in Chapter 5.)	Ground	Data signals must be equal to or no more than 0.5 inches (500 mils) shorter than the LAN clock trace.

10.3.11.2.2 Signal Routing and Layout

Platform LAN Connect Interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace, or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 10-34. LAN_CLK Routing Example



10.3.11.2.3 Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter. t_{RMATCH} is the sum of the trace length mismatch between LAN_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

10.3.11.2.4 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω ± 15% is strongly recommended; otherwise, signal integrity requirements may be violated.

10.3.11.2.5 Line Termination

Line termination mechanisms are not specified for the LAN Connect Interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 0 Ω to 33 Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

10.3.11.2.6 Terminating Unused LAN Connect Interface Signals

The LAN Connect Interface on the ICH4 can be left as a no-connect if it is not used.

10.3.12 Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM

For correct LAN performance, designers must follow the general guidelines outlined in Section 10.3.11.1. Additional guidelines for implementing an 82562EZ/ET/EX/EM Platform LAN Connect component are provided in the following section.

10.3.12.1 Guidelines for Intel® 82562EZ/ET/EX/EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

10.3.12.1.1 Crystals and Oscillators

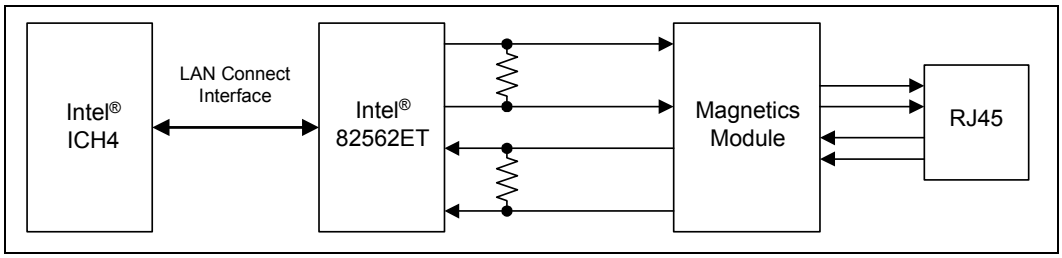
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility of radiation from the crystal case, and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562EZ/ET/EX/EM keeping the trace length as short as possible, and do not route any noisy signals in this area.

10.3.12.1.2 Intel® 82562EZ/EX / Intel® 82551QM Termination Resistors

The 100 Ω (± 1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 121 Ω ± 1% receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN connect component 82562EZ/ET/EX/EM) as possible. This is because these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

Figure 10-35. Intel® 82562EZ/ET/EX/EM Termination



NOTE: Place termination resistors as close to the 82562ET as possible.

10.3.12.1.3 Critical Dimensions

There are two dimensions to consider during layout. Distance A from the line RJ45 connector to the magnetics module and distance B from the 82562EZ/ET/EX/EM to the magnetics module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches) (See Figure 10-36).

Figure 10-36. Critical Dimensions for Component Placement

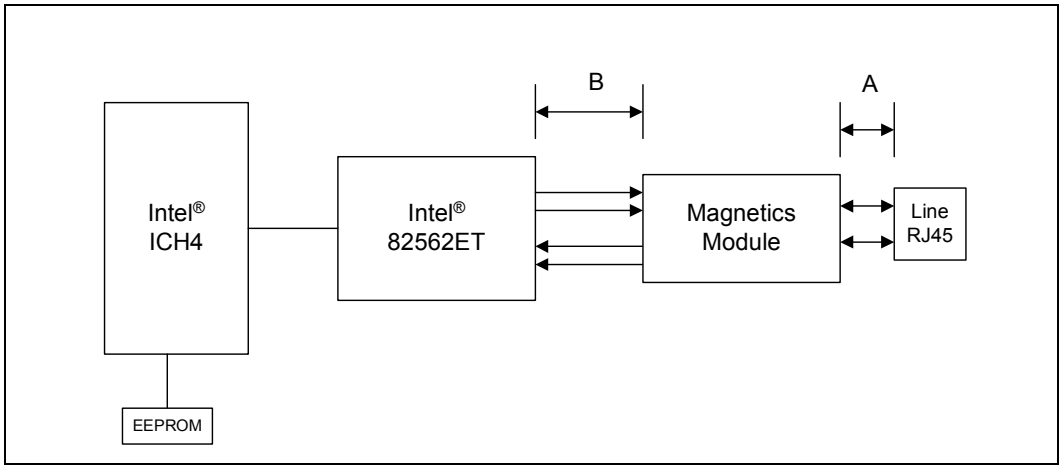


Table 10-21. Dimensions for Figure 10-36

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

Distance from Magnetics Module to RJ45 (Distance A)

The distance A in Figure 10-36 should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation.

The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 60 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562EZ/ET/EX/EM must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562EZ/ET/EX/EM and RJ45 as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 Ω – 110 Ω should compensate for second order effects.

Distance from Intel® 82562EZ/ET/EX/EM / 82551QM to Magnetics Module (Distance B)

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and have equal length within each differential pair.

10.3.12.1.4 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area because this increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane, and every power via should be connected to every power plane that is at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high-frequency harmonics, they can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This results in a smaller loop area and reduces the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

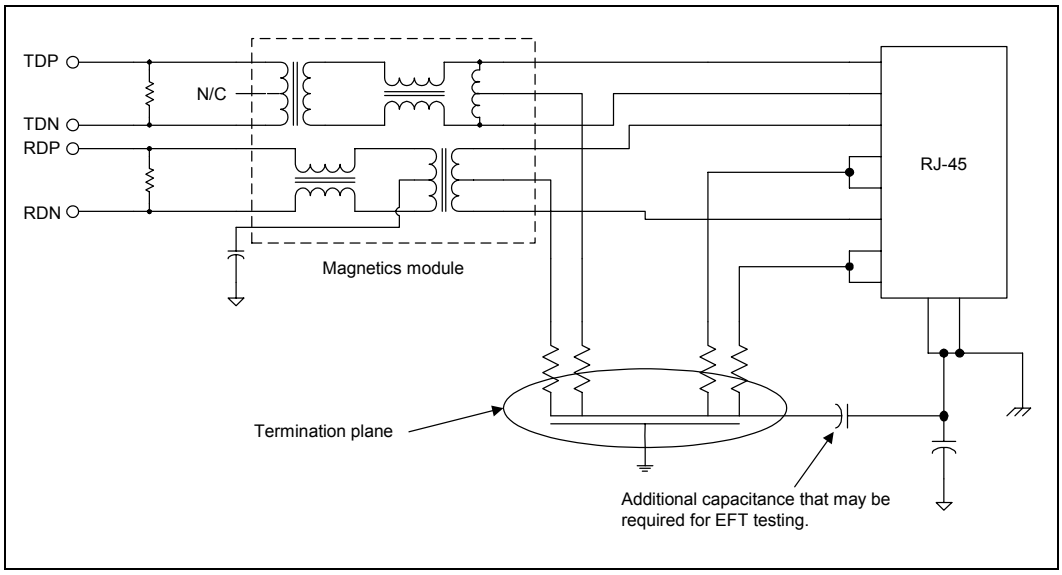
Terminating Unused Connections

In Ethernet designs it is common practice to terminate unused connections on the RJ45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, to signal ground, or to a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

10.3.12.1.5 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, it should be rated for at least 1000 Vac to meet the EFT requirements .

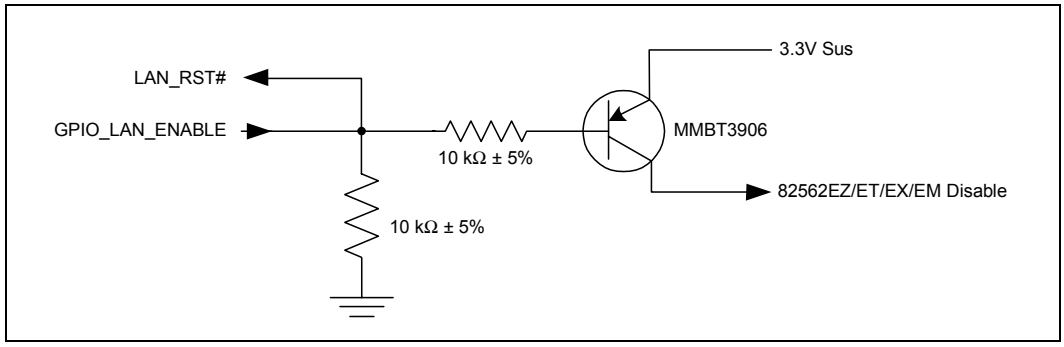
Figure 10-37. Termination Plane



10.3.12.2 Intel® 82562EZ/ET/EX/EM Disable Guidelines

To disable the 82562EZ/ET/EX/EM, the device must be isolated (disabled) before reset (RSM_PWROK) is asserted. Using a GPIO such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown in Figure 10-38 allows this operation. The BIOS controlling the GPIO can disable the LAN PHY.

Figure 10-38. Intel® 82562EZ/ET/EX/EM Disable Circuitry



There are four pins that are used to put the 82562EZ/ET/EX/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 10-22 describes the operational/disable features for this design.

The four control signals shown in Table 10-22 should be configured as follows:

- Test_En should be pulled-down through a 100 Ω resistor.
- The remaining three control signals should each be connected through 100 Ω series resistors to the common node “82562EZ/ET/EX/EM_Disable” of the disable circuit.

Table 10-22. Intel® 82562EZ/ET/EX/EM Control Signals

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled with Clock (low power)
1	1	1	1	Disabled without Clock (lowest power)

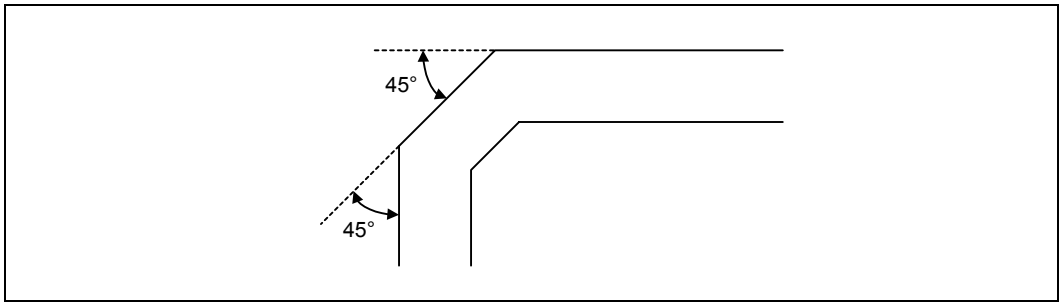
10.3.12.2.1 General LAN Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance:

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).]
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90 degree bend is required, it is recommended to use two 45 degree bends instead. Refer to Figure 10-39.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 10-39. Trace Routing



Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length, and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and reduce the intended effect of decoupling capacitors. For similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

Signal Isolation

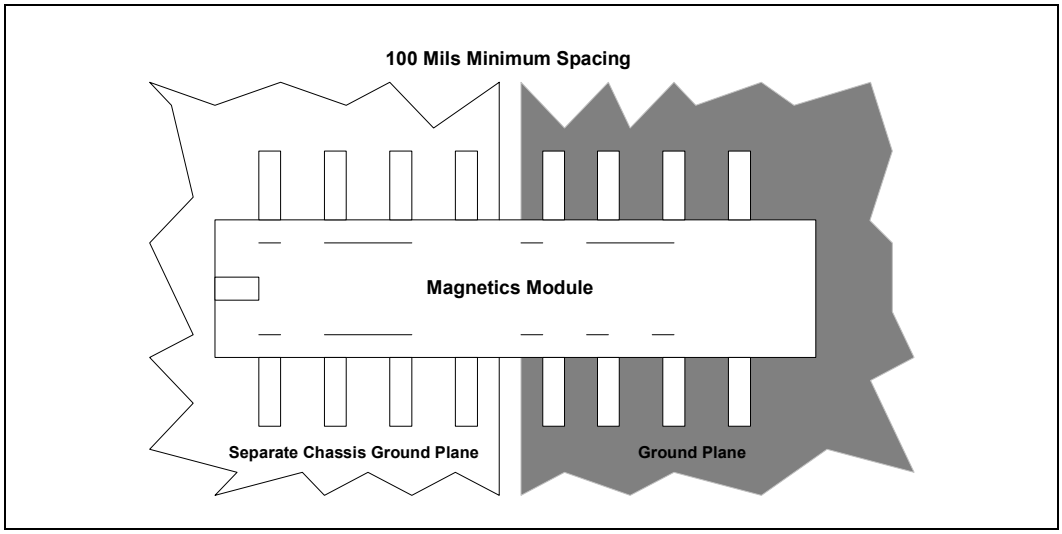
Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 10-40. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections, and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return will significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in both back planes and motherboards:

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics that can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ-45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath the transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

10.3.12.2.2 Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs:

- Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and distort the transmit or receive waveforms.
- Lack of symmetry between the two traces within a differential pair. (Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise and distort the waveforms.
- Excessive distance between the PLC and the magnetics, or between the magnetics and the RJ45 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer (see below). The magnetics should be as close to the connector as possible (≤ one inch).
- Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel causes degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC), and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
- Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ45, and the PLC.
- Use of an inferior magnetics module. The magnetics modules that Intel uses have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.
- Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or application note.
- Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The application notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
- Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they've designed for 100 Ω. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close[2] to each other, the edge coupling can lower the effective differential impedance by 5 Ω – 20 Ω. A 10 Ω – 15 Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.

- Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies, and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These caps are not necessary,unless there is some overshoot in 100 Mbps mode.

Note:

1. It is important to keep the two traces within a differential pair close[2] to each other. Keeping them close[2] helps make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e. FCC compliance) from the transmit traces, and better receive BER for the receive traces.
2. Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

10.4 FWH Guidelines

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the FWH BIOS Specification or equivalent.

10.4.1 FWH Vendors

The following vendors manufacture firmware hubs that conform to the Intel FWH Specification. Contact the vendor directly for information on packaging and density.

- SST http://www.ssti.com/
- STM http://us.st.com/stonline/index.shtml
- ATMEL http://www.atmel.com

10.4.2 FWH Decoupling

A 0.1 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high-frequency noise that may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple low-frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

10.4.3 In Circuit FWH Programming

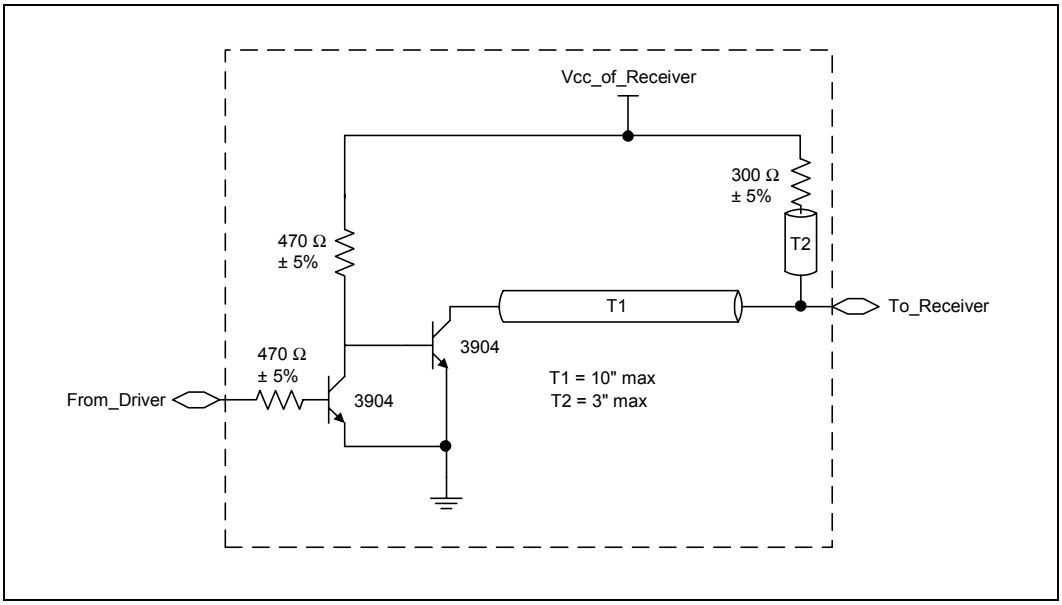
All cycles destined for the FWH will appear on PCI. The ICH4 hub interface to PCI Bridge will put all processor boot cycles out on PCI (before sending them out on the FWH interface). If the ICH4 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH4 in subtractive decode mode. If a PCI boot card is inserted and the ICH4 is programmed for positive decode, there will be two devices positively decoding the same cycle.

10.4.4 FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points must be considered because they are **not** consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the ICH4 INIT# signal must be at a value slightly higher than the VIH min FWH INIT# pin specification. The ICH4 inactive state of this signal is typically governed by the formula V_CPU_IOmin – noise margin. Therefore, if the V_CPU_IOmin of the processor is 1.6 V, the noise margin is 200 mV, and the VIH min spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because 1.6 V – 0.2 V = 1.40 V, which is greater than the 1.35 V minimum of the FWH. If the VIH min of the FWH was 1.45 V, there would be an incompatibility, and logic translation would have to be used. Note that these examples do not take into account actual noise that may be encountered on INIT#. Care must be taken to ensure that the VIH min specification is met with ample noise margin.

See Section 5.3.3 for INIT# topology and guidelines. The voltage translator circuitry is shown in Figure 10-41.

Figure 10-41. FWH Level Translation Circuit

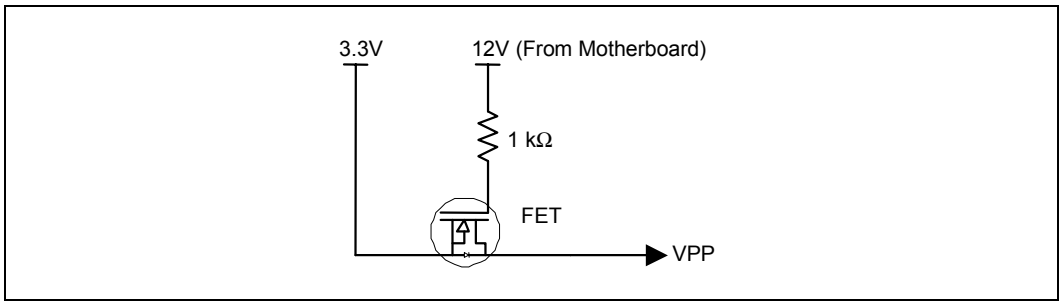


10.4.5 FWH V_{PP} Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports V_{PP} of 3.3 V or 12 V. If V_{PP} is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH supports 12 V V_{PP} for only 80 hours (3.3 V on V_{pp} does not affect the life of the device). The 12 V V_{PP} would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin **must** be tied to 3.3 V on the motherboard.

In some instances it is desirable to program the FWH during assembly, with the device soldered down on the board. To decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit allows testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 10-42. FWH V_{PP} Isolation Circuitry



10.5 Power Management Interface

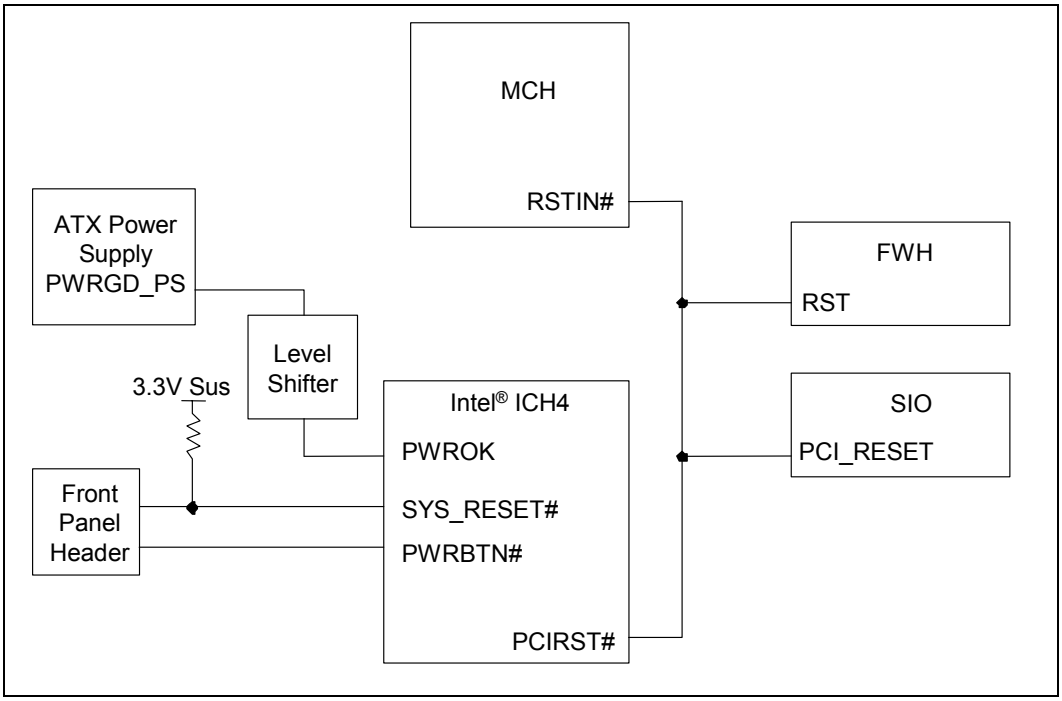
10.5.1 SYS_RESET# Usage Model

The System Reset ball (SYS_RESET#) on the ICH4 can be connected directly to the reset button on the systems front panel provided that the front panel header pulls this signal up to 3.3 V standby through a weak pull-up resistor. The ICH4 debounces signals on this pin (16 ms) and allows the SMBus to go idle before resetting the system, thus helping prevent a slave device on the SMBus from "hanging" by resetting in the middle of a cycle.

10.5.2 PWRBTN# Usage Model

The Power Button ball (PWRBTN#) on the ICH4 can be connected directly to the power button on the systems front panel. This signal is internally pulled-up in the ICH4 to 3.3 V standby through a weak pull-up resistor (24 kΩ nominal). The ICH4 has 16 ms of internal debounce logic on this pin.

Figure 10-43. SYS_RESET# and PWRBTN# Connection

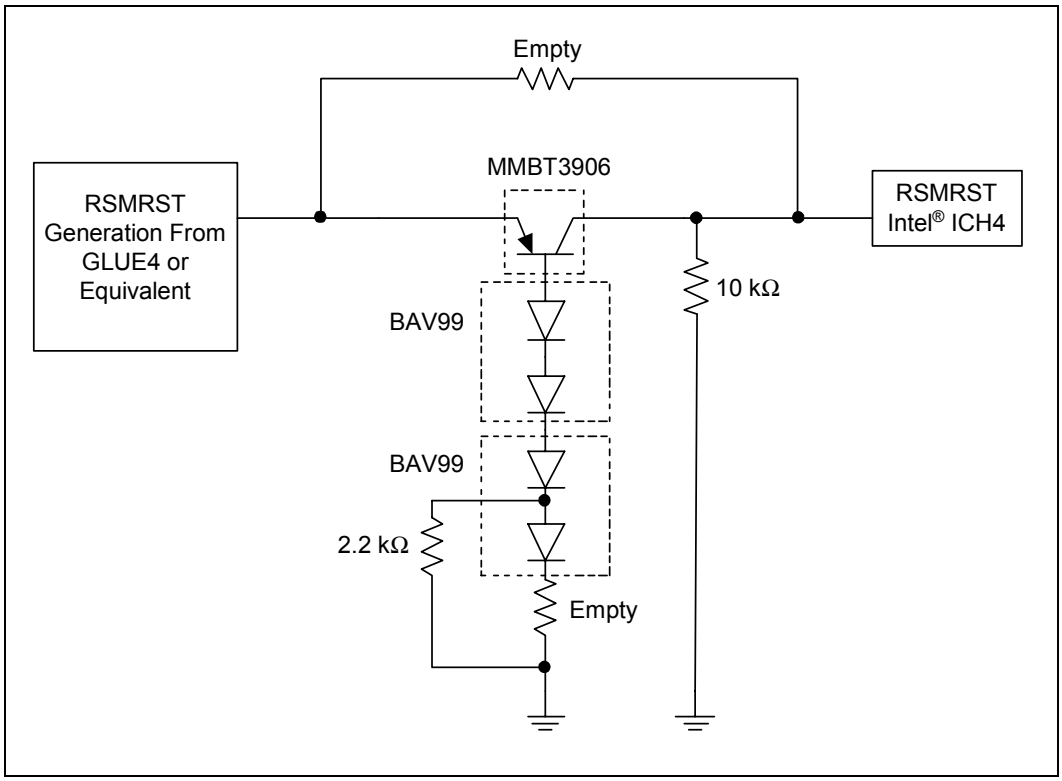


10.6 Power-Well Isolation Control Requirements

The RSMRST# signal of the ICH4 must transition from 20% signal level to 80% signal level and vice-versa in 50 µs. Slower transitions may result in excessive droop on the VccRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node can potentially cause the CMOS to be cleared or corrupted, the RTC to loose time after several AC power cycles, or the intruder bit to assert erroneously.

The circuit shown in Figure 10-44 can be implemented to control well isolation between the VccSus3_3 and RTC power-wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail, or does not meet the above rise/fall time.

Figure 10-44. RTC Power Well Isolation Control



10.7 General Purpose I/O

10.7.1 GPIO Summary

The ICH4 has 12 general purpose inputs, 8 general purpose outputs, and 16 general purpose inputs/outputs. Some of these general purpose inputs and outputs have native functions assigned to them.

Table 10-23. GPIO Summary (Sheet 1 of 2)

GPIO#	Available	Power Well	Input/Output/ Input-Output	Tolerance
0	Yes[2]	Core	Input	5 V
1	Yes[2]	Core	Input	5 V
2	Yes[2]	Core	Input	5 V
3	Yes[2]	Core	Input	5 V
4	Yes[2]	Core	Input	5 V
5	Yes[2]	Core	Input	5 V
6	Yes	Core	Input	5 V
7	Yes	Core	Input	5 V
8	Yes	Resume	Input	3.3 V
9	Yes	Resume	Input	3.3 V
10	Yes	Resume	Input	3.3 V
11	Yes[2]	Resume	Input	3.3 V
12	Yes	Resume	Input	3.3 V
13	Yes	Resume	Input	3.3 V
14	Yes	Resume	Output	3.3 V
15	Yes	Resume	Output	3.3 V
16	Yes[2]	Core	Output	3.3 V
17	Yes[2]	Core	Output	3.3 V
18	Yes	Core	Output	3.3 V
19	Yes	Core	Output	3.3 V
20	Yes	Core	Output	3.3 V
21	Yes	Core	Output	3.3 V
22	Yes	Core	Output (open drain)	3.3 V
23	Yes	Core	Output	3.3 V
24	Yes	Resume	Input-Output[1]	3.3 V
25	Yes	Resume	Input-Output[1]	3.3 V
26	Yes	Resume	Input-Output[1]	3.3 V
27	Yes	Resume	Input-Output[1]	3.3 V
28	Yes	Resume	Input-Output[1]	3.3 V
29	Yes	Resume	Input-Output[1]	3.3 V
30	Yes	Resume	Input-Output[1]	3.3 V

Table 10-23. GPIO Summary (Sheet 2 of 2)

GPIO#	Available	Power Well	Input/Output/ Input-Output	Tolerance
31	Yes	Resume	Input-Output[1]	3.3 V
32	Yes	Core	Input-Output[1]	3.3 V
33	Yes	Core	Input-Output[1]	3.3 V
34	Yes	Core	Input-Output[1]	3.3 V
35	Yes	Core	Input-Output[1]	3.3 V
36	Yes	Core	Input-Output[1]	3.3 V
37	Yes	Core	Input-Output[1]	3.3 V
38	Yes	Core	Input-Output[1]	3.3 V
39	Yes	Core	Input-Output[1]	3.3 V
40	Yes	Core	Input-Output[1]	3.3 V
41	Yes	Core	Input-Output[1]	3.3 V
42	Yes	Core	Input-Output[1]	3.3 V
43	Yes	Core	Input-Output[1]	3.3 V

NOTES:
1. Defaults as an Output to the ICH4.
2. Can be used as GPIO if the native function is not needed. ICH4 defaults these signals to native functionality.

10.8 System Design Considerations

10.8.1 Power Delivery

Table 10-24. Power Delivery Terminology

Term	Description
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory, and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered. This state is used in the Customer Reference Board to satisfy the S3 ACPI power management state.
Full-power Operation	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state, and the S1 (processor stop-grant state) state.
Suspend Operation	During suspend operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3), and Soft-off (S5).
Power Rails	An ATX power supply has 6 power rails: +5 V, –5 V, +12 V, –12 V, +3.3 V, and 5 VSB. In addition to these power rails, several other power rails are created with voltage regulators on the Intel® ICH4 Chipset Reference Board.
Core Power Rail	A power rail that is on only during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX power supply are ±5 V, ±12 V and +3.3 V.
Standby Power Rail	A power rail that is on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is 5 VSB (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived Power Rail	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3 VSB is usually derived (on the motherboard) from 5 VSB using a voltage regulator.
Dual Power Rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation, and is derived from a core supply during full-power operation. Note that the voltage on a dual power rail may be misleading.

10.8.1.1 Intel® ICH4 Reference Board Power Delivery

Figure 10-45. Intel® ICH4 Platform Power Delivery Example

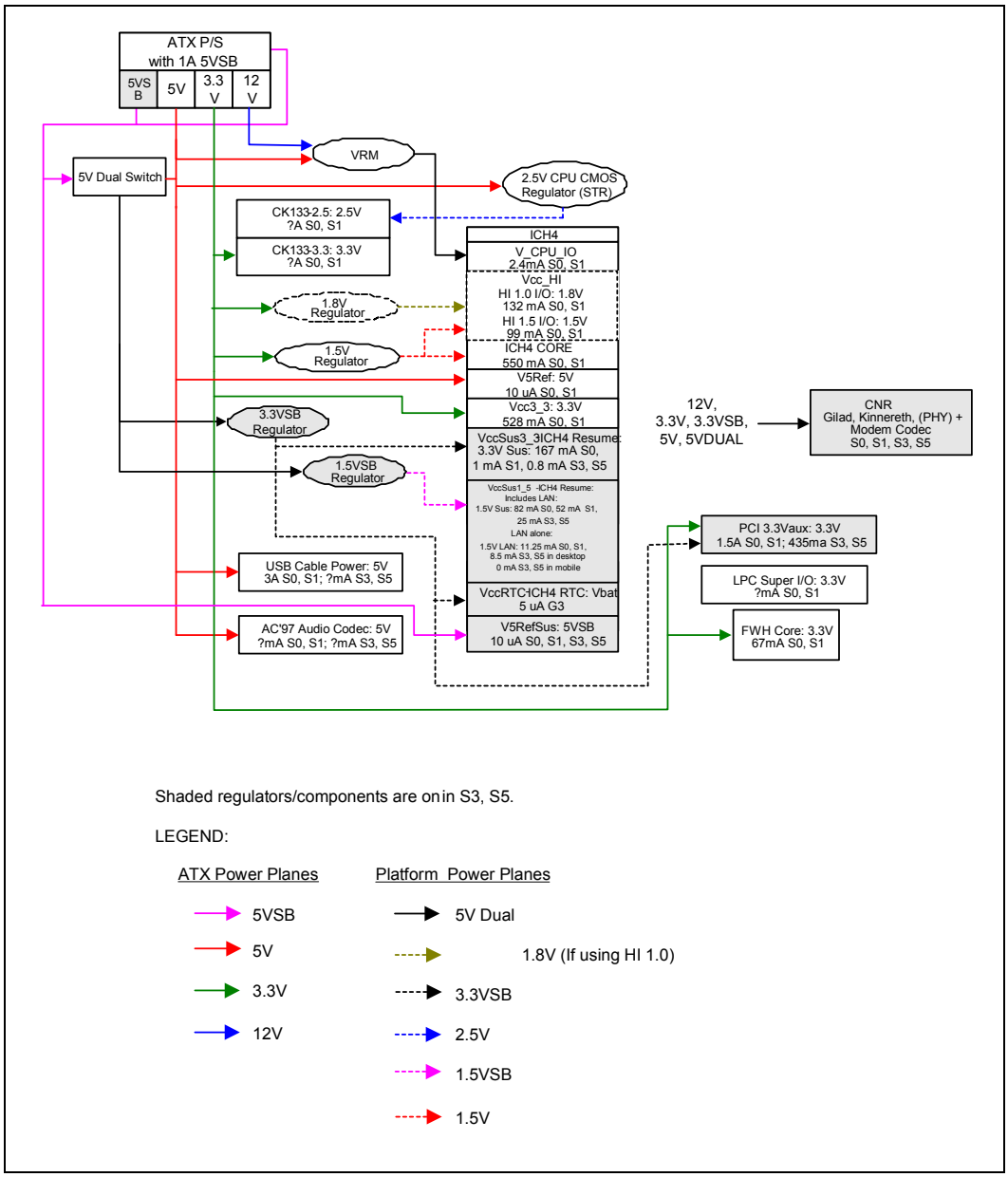


Figure 10-45 shows the suggested power delivery architecture for the ICH4 chipset. This power delivery architecture supports the "Instantly Available PC Design Guidelines" via the suspend-to-RAM (STR) state. During STR, only the necessary devices are powered. These devices include: main memory, the ICH4 resume well, PCI wake devices (via 3.3 Vaux), and USB (USB can only be powered if sufficient standby power is available). To ensure that enough power is available during STR, a thorough power budget must be completed. The power requirements must include each device's power requirements, both in suspend and in full-power. The power requirements

must be compared against the power budget supplied by the power supply. Due to the requirements of main memory and PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a dual power rail.

The models given in this Design Guide are only examples. There are many power distribution methods that achieve the similar results. It is critical when deviating from these examples in any way to consider the effect of the change.

In addition to the power planes provided by the ATX power supply, an instantly available ICH4 chipset-based system (using Suspend-to-RAM) requires 7 power planes to be generated on the board. The requirements for each power plane are documented in this section. In addition to on-board voltage regulators, the ICH4 Chipset Reference Board will have a 5 V Dual Switch.

5 V Dual Switch

This switch powers the 5 V Dual plane from the 5 V core ATX supply during full-power operation. During Suspend-to-RAM, the 5 V Dual plane is powered from the 5 V Standby power supply.

Note: The voltage on the 5 V Dual plane is not 5 V.

There is a resistive drop through the 5 V Dual Switch that must be considered. Therefore, **no components** should be connected directly to the 5 V Dual plane. On the ICH4 Reference Board, the only devices connected to the 5 V Dual plane are voltage regulators (to regulate to lower voltages).

Note: This switch is not required in an ICH4 chipset-based system that does not support Suspend-to-RAM (STR).

1.8 V

The 1.8 V plane powers the ICH4 Hub Interface 1.0 I/O buffers. If using Hub Interface 1.5, the Hub Interface power signals should be connected to 1.5 V.

Note: This regulator **is not** required in all designs

1. 5 V

The 1.5 V plane powers the ICH4 hub interface 1.5 I/O buffers, as well as other components. For ICH4 power requirements for this rail, see Table 10-25. For decoupling considerations, refer to Section 10.8.1.5.

Note: This regulator **is** required in **all** designs.

3.3 VSB

The 3.3 VSB plane powers the I/O buffers in the resume well of the ICH4, and the PCI 3.3 Vaux suspend power pins. The 3.3 Vaux requirement states that during suspend, the system must deliver 375 mA to each wake-enabled card, and 20 mA to each non wake-enabled card. During full-power operation, the system must be able to supply 375 mA to EACH card. Therefore, the total current requirement is:

- Full-power Operation: 375 mA * number of PCI slots
- Suspend Operation: 375+20 * (number of PCI slots – 1)

In addition to the PCI 3.3 Vaux, the ICH4 suspend well power requirements must be considered as shown in Figure 10-45.

Note: This regulator **is** required in **all** designs.

1.5 VSB

The 1.5 VSB plane powers the logic to the resume well of the ICH4.

10.8.1.2 Power Supply PS_ON Consideration

If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10–100 ms) such that PS_ON is driven active during the exponential decay of the power rails, a few power supply designs may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never powers back up. These power supplies would have to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with the affected power supply.

The ATX specification does not specify a minimum pulse width on PS_ON deassertion. This means that power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Because of variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that the power supply used with the platform is not affected by this problem.

10.8.1.3 Intel® ICH4 Analog Power Delivery

There are no analog ICH4 circuits that require filters.

10.8.1.4 Intel® ICH4 Power Delivery

Figure 10-46. Intel® ICH4 Top Layer Power Delivery

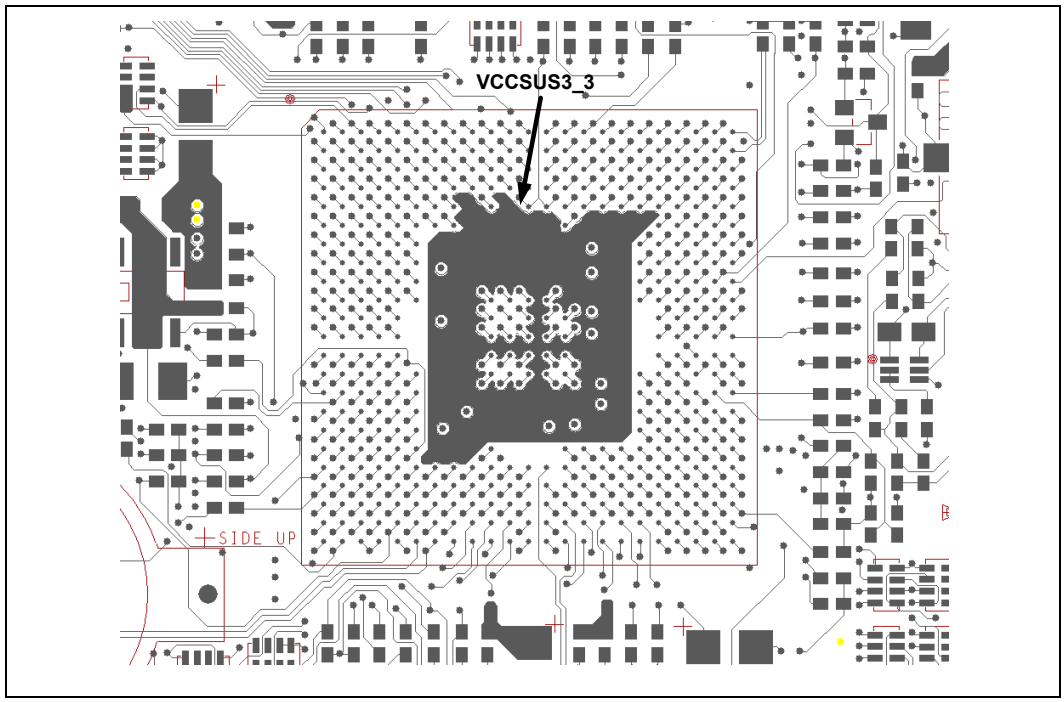


Figure 10-47. Intel® ICH4 Layer 3 Power Delivery

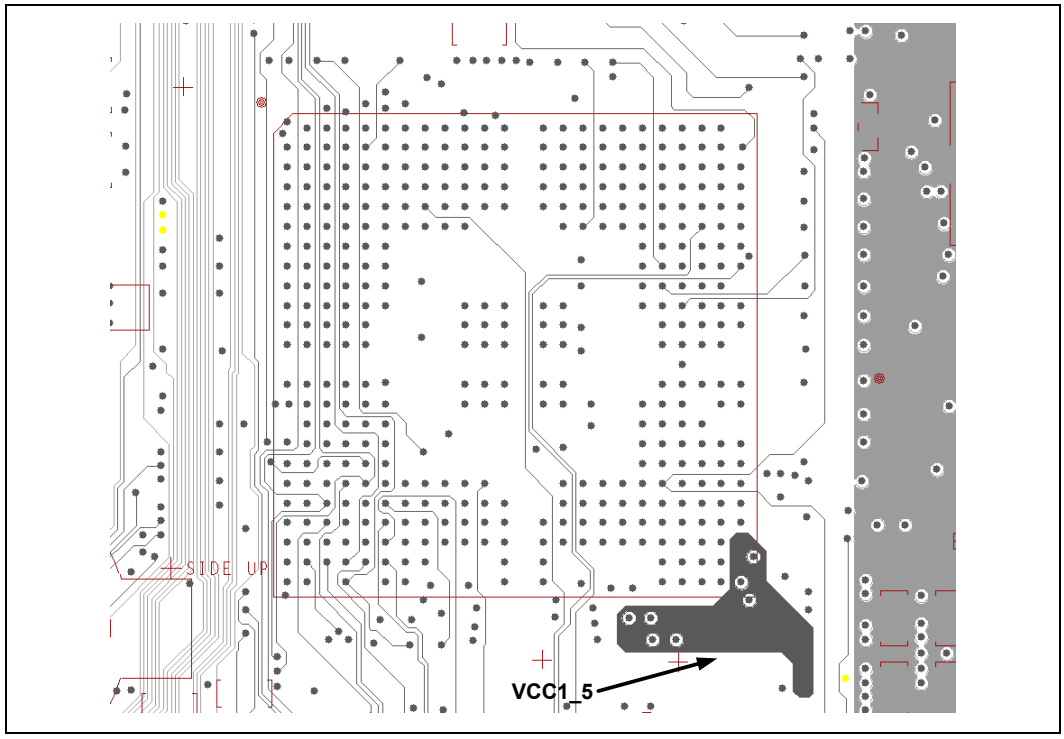


Figure 10-48. Intel® ICH4 Layer 4 Power Delivery

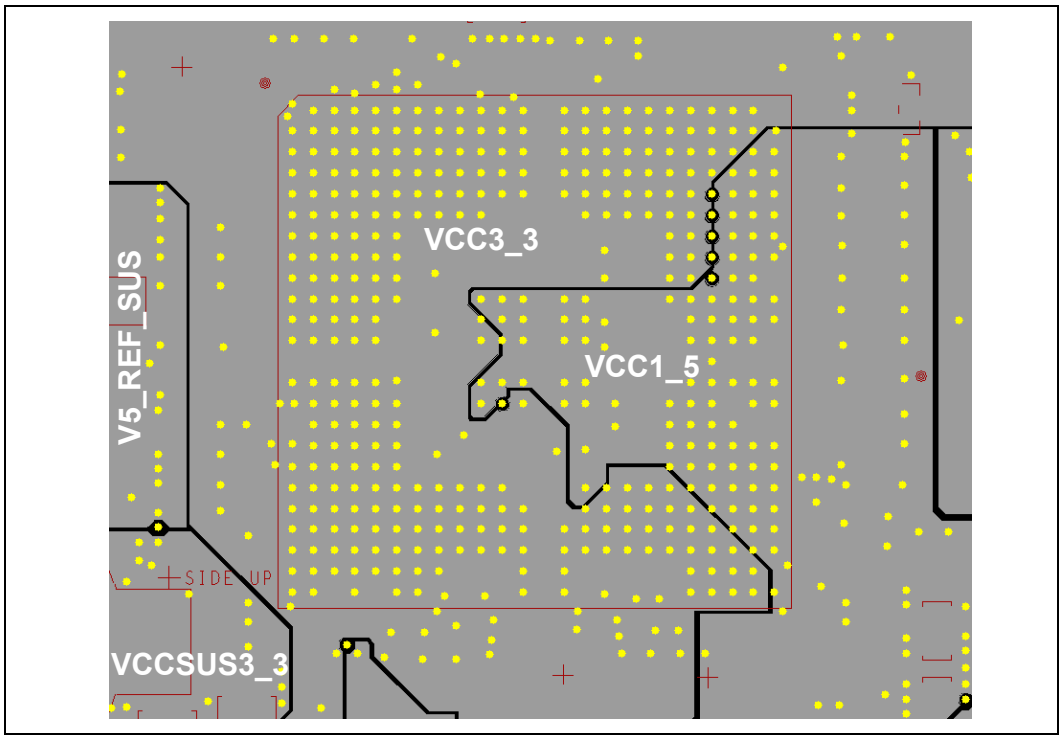
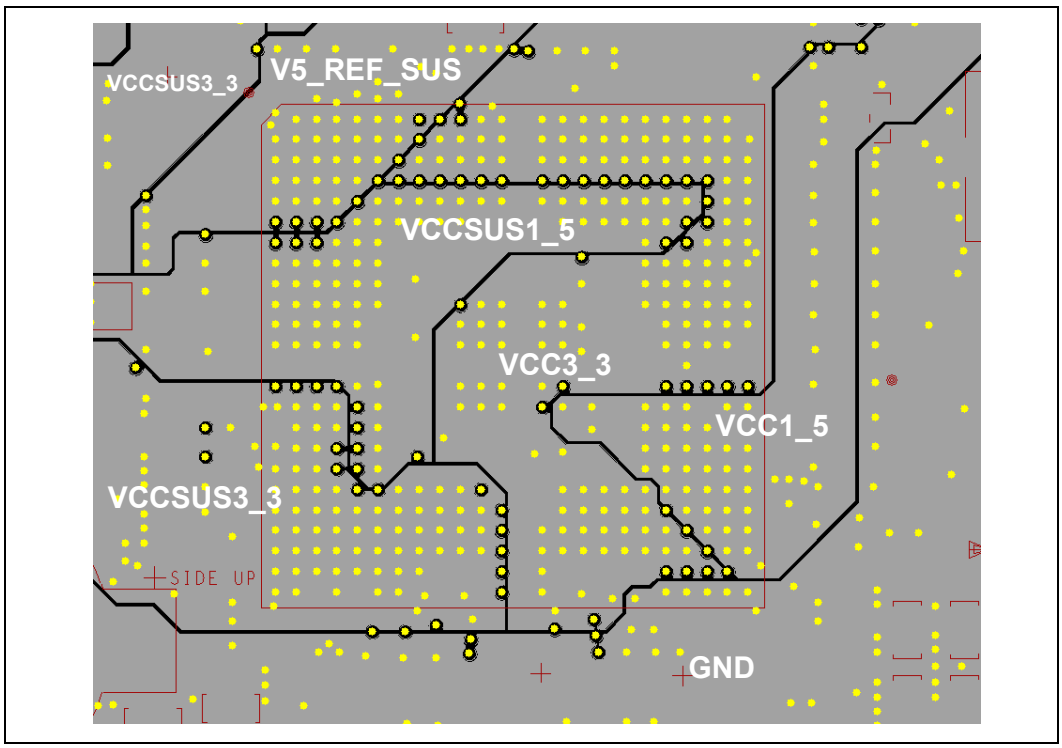


Figure 10-49. Intel® ICH4 Layer 5 Power Delivery



10.8.1.5 Intel® ICH4 Decoupling Recommendations

The ICH4 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in Table 10-25 to ensure that the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible (100 mils nominal). Rotate caps that set over power planes so that the loop inductance is minimized. The basic theory for minimizing loop inductance is to consider which voltage is on layer two (power or ground), and spin the decoupling cap with the opposite voltage towards the BGA (Ball Grid Array). This greatly minimizes the total loop inductance. It is recommended that for prototype board designs, the designer include pads for extra power plane decoupling caps.

Table 10-25. Decoupling Requirements for Intel® ICH4

Pin	Decoupling Requirements	Decoupling Type (Pin Type)	Decoupling Placement
VCC3_3	(6) 0.1 µF	Decoupling Cap (VSS)	Place near balls: A4, A1, H1, T1, AC10, and AC18
VccSus3_3	(2) 0.1 µF	Decoupling Cap (VSS)	Place near balls: A22 and AC5
V_CPU_IO	(1) 0.1 µF	Decoupling Cap (VSS)	Place near ball: AA23
VC1_5	(2) 0.1 µF	Decoupling Cap (VSS)	Place near balls: K23 and C23
VccSus1_5	(2) 0.1 µF	Decoupling Cap (VSS)	Place near balls: A16 and AC1
V5REF	(1) 0.1 µF	Decoupling Cap (VSS)	Place near ball: E7
V5REF_Sus	(1) 0.1 µF	Decoupling Cap (VSS)	Place near ball: A16
VccRTC	(1) 0.1 µF	Decoupling Cap (VSS)	Place near ball: AB5
VCCHI	(2) 0.1 µF	Decoupling Cap (VSS)	Place near balls: T23 and N23
VCCPLL	(1) 0.1 µF and (1) 0.01 µF	Decoupling Cap (VSS)	Place near ball: C22

NOTE: Capacitors should be placed less than 100 mils from the package.

10.8.1.6 3.3 V/1.5 V and 3.3 V/1.8 V Power Sequencing

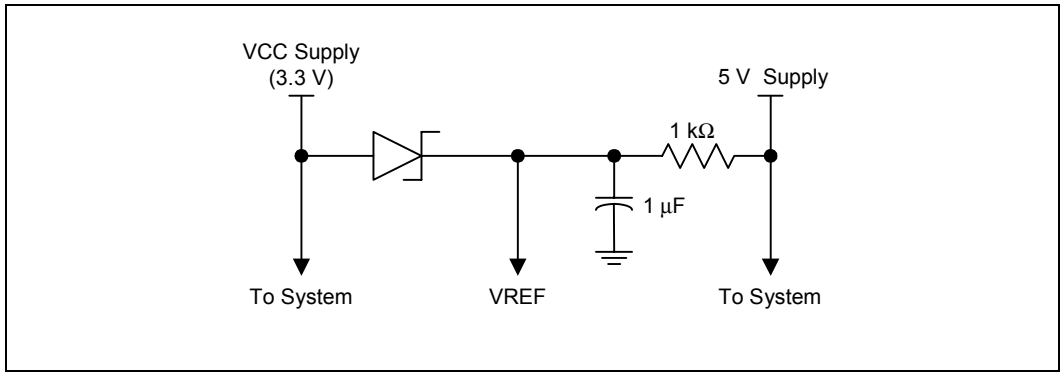
There are no power sequencing requirements for the associated 3.3 V/1.5 V rails or the 3.3 V/1.8 V rail of the ICH4. It is generally good design practice to core power up before or at the same time as the other rails.

10.8.1.7 V5REF/ 3.3 V Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH4. V5REF must be powered up before VCC3_3, or after VCC3_3 within 0.7 V. Also, V5REF must power down after VCC3_3, or before VCC3_3 within 0.7 V. This rule must be followed to ensure the safety of the ICH4. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 10-50 shows a sample implementation of how to satisfy the V5REF/VCC3_3 sequencing rule.

This rule also applies to the stand-by rails, but in most platforms the VccSus3_3 rail is derived from the VccSus5 rail. Therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_SUS will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be adhered to in the platform design.

Figure 10-50. Example V5REF / 3.3 V Sequencing Circuitry



10.8.1.8 Intel® ICH4 Power Consumption Numbers

Table 10-26 describes ICH4 power consumption.

Table 10-26. Intel® ICH4 Power Consumption Measurements

Power Plane	Maximum Power Consumption				
	S0	S1	S3	S4/S5	G3
1.5 V Core	550 mA	266 mA	N/A	N/A	N/A
3.3 V I/O	528 mA	0.76 mA	N/A	N/A	N/A
1.5 V SUS	82 mA	52 mA	25 mA	25 mA	N/A
3.3 V SUS [1]	167 mA	1 mA	0.8 mA		N/A
VccRTC	N/A	N/A	N/A	N/A	5 µA
V_CPU_IO [2]	2.4 mA	2.4 mA	N/A	N/A	N/A
VCCHI [3]					
HI 1.0 (1.8 V)	132 mA	132 mA	N/A	N/A	N/A
HI 1.5 (1.5 V)	99 mA	99 mA	N/A	N/A	N/A
V5REF	10 µA	10 µA	N/A	N/A	N/A
V5REF_SUS	10 µA	10 µA	10 µA	10 µA	10 µA

NOTES:
1. 3.3 V SUS S0 assumes maximum USB 2.0 traffic (6 ports populated).
2. V_CPU_IO S1 state primarily due to STPCLK# activity.
3. VCCHI power consumption is dependant on the Hub Interface being used

10.8.2 Thermal Design Power

For information on ICH4 thermal design refer to the
Intel® I/O Controller Hub 4 (ICH4) Thermal Design Guidelines

10.8.3 Glue Chip 4 (Intel® ICH4 Glue Chip)

To reduce the component count and the BOM cost of the ICH4 platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The ICH4 Glue Chip is designed to integrate the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost is reduced.

Features:

- Dual, Strapping, Selectable Feature Sets
- Audio-disable circuit
- Mute Audio Circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3V) signal generation
- Power Sequencing / BACKFEED_CUT
- Power Supply turn on circuitry
- RSMRST# generation
- Voltage translation for DDC to VGA monitor
- HSYNC / VSYNC voltage translation to VGA monitor
- Tri-state buffers for test
- Extra GP Logic Gates
- Power LED Drivers
- Flash FLUSH# / INIT# circuit

More information regarding this component is available from the following vendors:

Vendor	Contact Information
Philips Semiconductors	6028 44th Way NE Olympia, WA 98516-2477 Phone: (360) 413-6900 Fax: (360) 438-3606
Fujitsu Microelectronics	3545 North 1st Street, M/S 104 San Jose, CA 95134-1804 Phone:1-800-866-8600 Fax: 1-408-922-9179

Note: These vendors are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of the vendors' devices. This list is subject to change without notice.

This page is intentionally left blank.

Intel® P64H2 11

The P64H2 is a peripheral chip that performs PCI bridging functions between Hub Interface and the PCI bus. The P64H2 is an integral part of the E7505 chipset, bridging the Server I/O Hub (SIOH) or the MCH (Memory Controller Hub) and the PCI bus. On the primary bus, the P64H2 utilizes a 16-bit data bus to interface with the Hub Interface, and on the secondary bus it supports two 64-bit PCI bus segments. The primary bus operates in 8X (Hub Interface 2.0) mode. Either one of the secondary PCI bus interfaces can be configured to operate in PCI or PCI-X mode. Each PCI interface contains an I/OxAPIC with 24 interrupts.

11.1 PCI/PCI-X Design Guidelines

The P64H2 contains two PCI/PCI-X interfaces. The PCI Interface has a 33/66 MHz bus speed, and PCI-X has a 66/100/133 MHz bus speed, as described in Table 11-1.

Table 11-1. PCI/PCI-X Frequencies

PCI		
Frequency	**Maximum Slots**	**Voltage**
33 MHz	6	3.3 V, 5 V
66 MHz	2	3.3 V

PCI-X		
Frequency	**Maximum Slots**	**Voltage**
66 MHz	4	3.3 V
100 MHz	2	3.3 V
133 MHz	1	3.3 V

The PCI/PCI-X bus topologies shown in Section 11.1.1 were simulated by Intel. If a platform implements a PCI/PCI-X topology that is not described, it is the responsibility of the system designer to ensure that the system meets the specified timings. The recommended lengths that are specified are not intended to replace thorough system simulations and validation.

11.1.1 PCI / PCI-X Routing Requirements

The P64H2 supports a large number of PCI/PCI-X configurations. The basic topology of the bus is shown in Figure 11-1. Multiple connectors and devices down on the motherboard are connected in a daisy chain topology. Table 11-2 lists the lengths for the more commonly implemented configurations that were simulated by Intel.

Figure 11-1. Typical PCI Routing

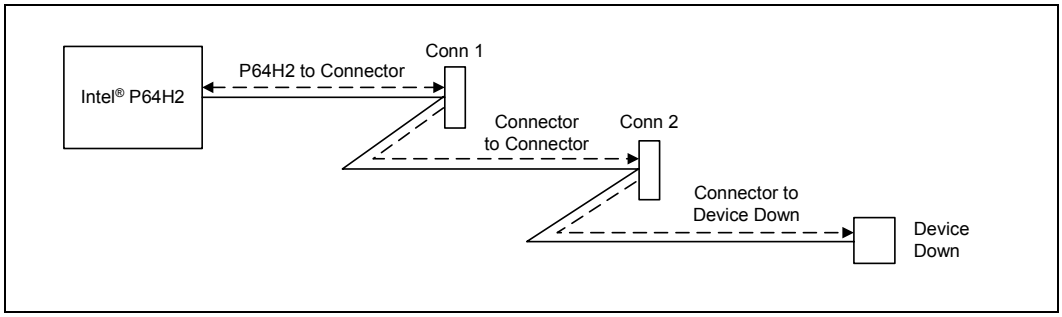


Table 11-2. Intel® P64H2 PCI / PCI-X Configuration Length Requirements

Config (Slot#,Dev#)	Intel® P64H2 to Connector	Connector 4 to Connector	Connector to Device Down
33 MHz, 5 slots / 1 device down	2.0” – 7.0”	1.0”	3.0” - 6.0”
66 MHz, 4 slots / 0 devices down	6.0” – 8.0”	1.5”	N/A
100 MHz, 2 slots / 0 devices down	5.0” – 8.0”	1.0” – 1.75”	N/A
100 MHz, 2 slots / 1 device down	3.0” – 6.0”	0.8”	4.0” – 6.5”
100 MHz, 1 slot / 1 device down	3.0” – 7.0”	N/A	4.0” – 7.0”
100 MHz, 1 slot / 2 devices down	2.0” – 4.0”	(device to device) 2.0”	5.0”
133 MHz, 1 slot / 0 devices down	3.0” – 7.1”	N/A	N/A

NOTE: During simulation, connector to connector lengths were held constant for some configurations. Therefore, no range can be given for these length requirements.

11.1.2 Intel® P64H2 Clock Signal Configuration

The six PCI clocks (PxPCLKO[5:0]) are individually routed point-to-point. All PCI clocks must be disabled in the BIOS for any unused/unpopulated PCI-X slots. The PxPCLKO[5:0] pins can each be disabled by writing to the Disable PCLKOUT 5 - 0 bits (DPCLK, bits 15:10, config register offset 40h in each bridge).

Figure 11-2. Clock Configuration

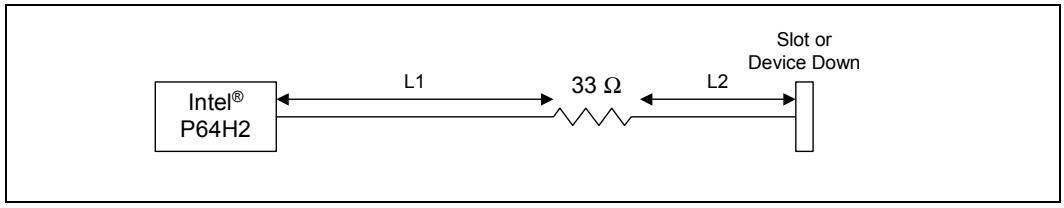


Table 11-3. Clock Routing Length Parameters

Clock Speed	L1 (inches)	L2 (inches) Slot	L2 (inches) Device Down
33 MHz	3.5 – 5.5	0.5 – 5.0	2.9 – 7.9
66 MHz	3.5 – 4.5	0.5 – 1.0	3.0 – 3.5
100 MHz	≤ 1.0	$L_{fbi} - 2.5$[1]	L_{fbi}[1]
133 MHz	≤ 1.0	$L_{fbi} - 2.5$[1]	L_{fbi}[1]

NOTE:
1. The clock signal and feedback loops are closely related. Refer to Figure 11-3.

11.1.3 Intel® P64H2 Loop Clock Configuration

You must tie PxPCLKO6 to PxPCLKI because this clock will always run and is needed by the internal PCI PLLs to properly align output signals with the external clocks by removing clock insertion delay. The PxPCLKO6 signal does not have to be routed through a bus switch before returning to PxPCLKI.

Figure 11-3. Loop Clock Configuration

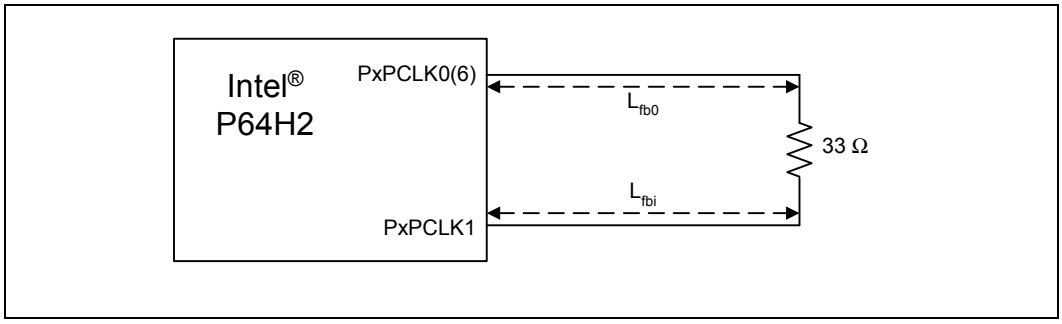


Table 11-4. Loop Clock Configuration Routing Length Parameters

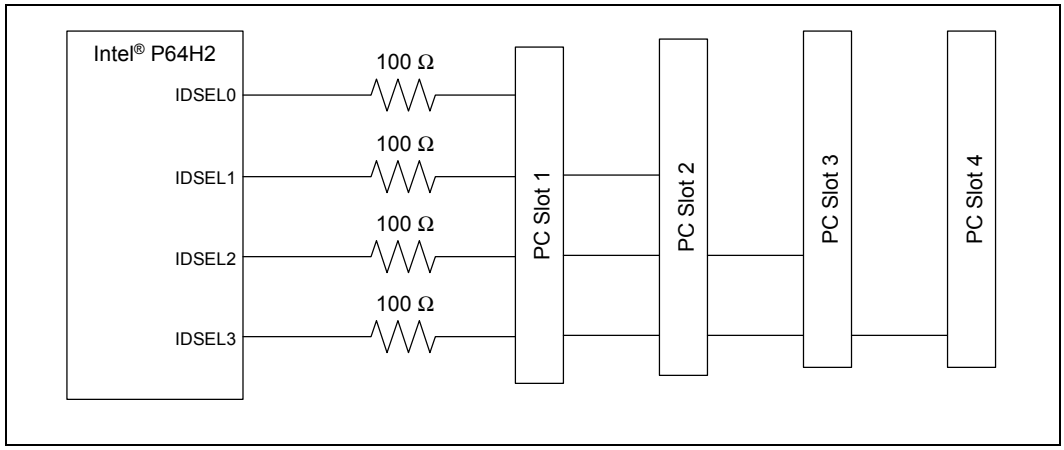
Clock Speed	L_{fbo} (inches)	L_{fbi} (inches)
33 MHz	3.5 – 5.5	2.9 – 7.9
66 MHz	4.5 – 5.5	3.9 – 4.9
100 MHz	<= 1.0	L2 + 2.5
133 MHz	0.25 – 1.0	L2 + 2.5

NOTE: The clock signal and feedback loops are closely related. Refer to Figure 11-2 and Figure 11-3.

11.1.4 IDSEL Implementation

Designers should use a 100 Ω series coupling resistor on the IDSEL signal when implementing PCI-X. The original PCI-X 1.0 specification calls for a 2 kΩ resistor, but the spec is being modified to allow for other resistor values. See Figure 11-4 for an example of how to implement the coupling resistor. IDSEL mapping per P64H2 pin is arbitrary. However, AD16 is reserved.

Figure 11-4. IDSEL Sample Implementation Circuit



11.1.5 SMBus Address

11.1.5.1 Fixed and Non-Fixed Address

The P64H2 has three bit positions that are fixed, and four bit positions that are configurable.

Table 11-5. SMBus Address Configuration Table

Bit	Value
7	1
6	1
5	PA_GNT5
4	0
3	PA_GNT4
2	PB_GNT5
1	PB_GNT4

NOTE: There is no bit 0 because it is the read/write direction indicator.

11.1.5.2 Address Latching

The SMBus address is set upon PWROK by sampling the pins enumerated in Table 11-5. Refer to the P64H2 datasheet for a more detailed description of P64H2 strap latching.

11.2 Intel® P64H2 Power Requirements

11.2.1 Intel® P64H2 Current Requirements

Table 11-6. Intel® P64H2 Max Sustained Currents

Voltage at PCI/PCI-X Interface	Maximum Sustained Current
1.8 V at 33 MHz PCI (both segments)	1970 mA
1.8 V at 66 MHz PCI/PCI-X (both segments)	2170 mA
1.8 V at 100 MHz PCI-X (both segments)	2550 mA
1.8 V at 133 MHz PCI-X (both segments)	2660 mA
3.3 V at 33 MHz PCI 6 loads (both segments)	930 mA
3.3 V at 66 MHz PCI 2 loads (both segments)	690 mA
3.3 V at 66 MHz PCI-X 4 loads (both segments)	1300 mA
3.3 V at 100 MHz PCI-X 2 loads (both segments)	1050 mA
3.3 V at 133 MHz PCI-X 1 load (both segments)	770 mA

For more information, refer to the P64H2 Thermal Design Guide.

11.2.2 Intel® P64H2 Decoupling Requirements

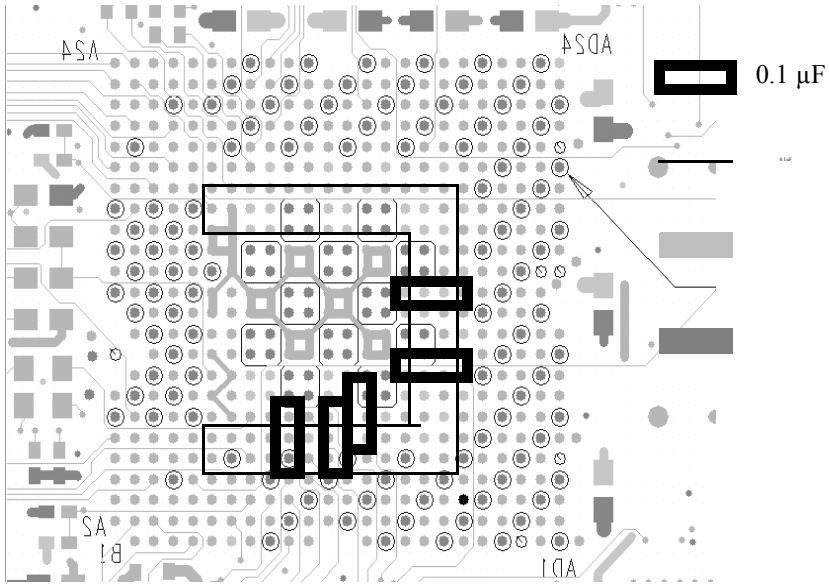
The P64H2 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in Table 11-7 to ensure that the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible.

Table 11-7. Decoupling Capacitor Recommendations

Power Plane/Pins	No. of High-Frequency Decoupling Capacitors	High-Frequency Capacitor Values	No. of Bulk Decoupling Capacitors	Bulk Capacitor Values
1.8V Core (VCC)	8	0.1 µF	2	4 µF (near Intel® P64H2)
1.8V HI 2.0 (VCC1_8)	2	1.0 µF	1	100 µF (near regulator)
3.3V PCI/PCI-X (VCC3_3)	20[1]	0.1 µF	2	4 µF (near P64H2)
	6	1.0 µF	1	100 µF (near regulator)

NOTE:
1. In the case of the 20 0.1 µF decoupling capacitors for the VCC 3.3V plane, it is recommended that at least 5 of these capacitors be placed near the die on the back of the board between ground and the VCC-PCI vias, as shown in Figure 11-5. This is not a strict requirement but is recommended to reduce the power resonance frequency at 66 Hz.

Figure 11-5. 3.3 V PCI/PCI-X (VCC3_3) Capacitor Placement



11.2.3 PCIRST# Implementation

PCI-X requires a 100 ms delay from valid power (PWRGD) to reset deassertion (PCIRST#). The system design must ensure that this requirement is met.

Debug Port 12

Refer to the *ITP700 Debug Port Design Guide* for information necessary to develop a Debug Port on this platform, including electrical specifications, mechanical requirements, and all In-Target Probe (ITP) signal layout guidelines.

This page is intentionally left blank.

Power Distribution Guidelines 13

Note: Intel recommends that this platform utilize voltage regulator modules based on the *Voltage Regulator Module (VRM) 9.1 DC-DC Converter Design Guidelines,* or voltage regulator down solutions based on the *Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines*. The VR guidelines and recommendations included in this chapter are required to meet the current requirements of the processors.

As computer performance demands increase, new higher speed logic with increased transistor density is fulfilling these needs. To reduce power dissipation, modern microprocessors are being designed with lower voltage requirements. This requires power supplies that provide lower voltages with higher current capability. Because of this, processor power is becoming a significant portion of the system design that demands special attention. The processor has unique requirements for the voltages supplied to it. The system bus with AGTL+ technology, the processor core, and the cache are powered from the same voltage supply. The demand on the supply current and transient specification has increased drastically by the processor core. As the differences in processor current between the low power state and the high power state increase, the cost of the power distribution system becomes significant enough to merit careful calculation. Centralized distribution of power, for example, is no longer the effective solution to power distribution.

This chapter describes the power requirements of the processor. In addition, the chapter discusses simulation and power implementation techniques. It is assumed the reader is familiar with power distribution for the Pentium® III, Pentium® II Xeon™, and Pentium® III Xeon™ processors.

Table 13-1. Power Delivery Terminology

Item	Description
Power-Good (PWRGOOD)	An active-high signal that indicates that all of the supplies and clocks within the system are stable. *PWRGOOD* should go active a predetermined time after system voltages are stable, and should go inactive as soon as any of these voltages fail their specifications. Refer to the *Intel® Xeon Processor with 512-KB L2 Cache Datasheet* for details on the *PWRGOOD* timing requirements.
VCC_CPU	In this section, *VCC_CPU* refers to the appropriate processor core voltage, cache supply voltage, and AGTL+ supply voltage. The processor core and cache are on the same silicon and are powered from the same power plane unlike the Pentium® II Xeon™ and Pentium® III Xeon™ processors, which required different power planes.
SM_VCC\ VID_VCC	The INT-mPGA package processors define these signals as *SM_VCC*, whereas the FC-mPGA2 package processors define these as *VID_VCC* because of the absence of SMBus components. *SM_VCC* provides power to the SMBus components on the INT-mPGA processor package. Additionally, *SM_VCC* and *VID_VCC* provide power for the VID and BSEL logic for both processor package types. Baseboards MUST provide *SM_VCC\VID_VCC* power. These signals have specific power sequencing issues described in Section 13.4.3.
VRD	*Voltage Regulator Down* for the processors. It is an embedded voltage regulator that supplies the required voltage and current for one or more processors.
VRM 9.1	*Voltage Regulator Module* for the processors. It is a DC-DC converter module that supplies the required voltage and current to a single processor.

13.1 Power Delivery Overview

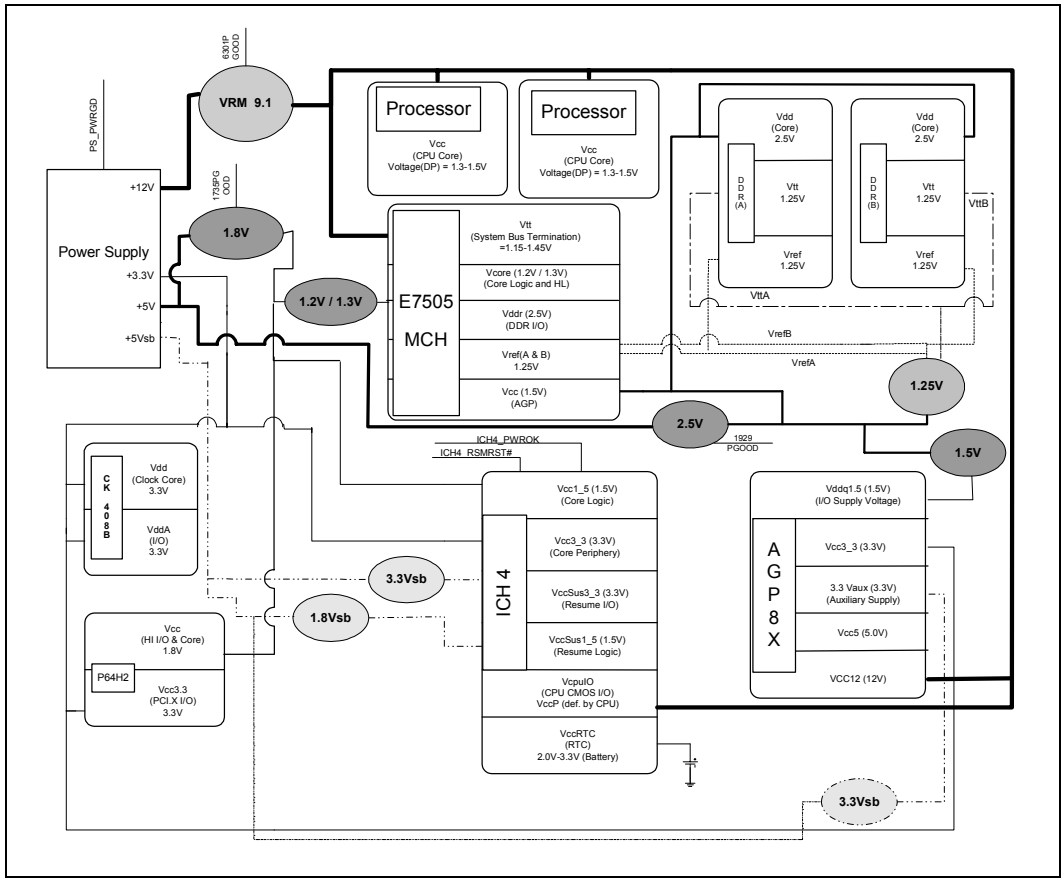
Power distribution is generally thought of as supplying power to the components that require it. Most digital designers assume that an ideal supply will be provided. The printed circuit board (PCB) designers attempt to create this ideal supply with two power planes in the PCB, or by using large width traces to distribute power. High-frequency noise that is created when logic gates switch is typically controlled with high-frequency ceramic capacitors that are recharged from lower frequency bulk capacitors. Various “rule of thumb” methods exist for determining the amount of each type of required capacitance. For this platform, the system designer must design beyond the “rule of thumb” and architect a power distribution system that meets appropriate processor specifications.

The processor core and all caches operate at the same voltage level (i.e., VCC_CPU). On-die termination is used to pull the AGTL+ bus up to VCC_CPU to control reflections on the transmission line. The chipset also provides on-die termination to eliminate the need to terminate the bus on the system board. The data bus must route over a uniform power plane because of signal quality constraints. Consequently, in a multiprocessor system design, a single power plane should be used for power delivery to all processors. Hence, the mixing of processors operating at different voltages is not supported and will not be validated by Intel.

13.2 Customer Reference Board Power Delivery

Figure 13-1 shows the power delivery architecture for the E7505 chipset Customer Reference Board.

Figure 13-1. Intel® E7505 Chipset Power Delivery Example



NOTE: The recommendations given in this Design Guide are only examples. Many power distribution methods achieve similar results. It is critical when deviating from these recommendations in any way to consider the effects of the change.

13.2.1 Voltage Rail and Max Current Specifications

13.2.1.1 1.500 V (CPU VID)

The processor core voltage power plane powers the processors. The core voltage operates between 1.3 V and 1.5 V. The VRM or VRD equivalent will be a VRM 9.1 design. Refer to the *Voltage Regulator Module (VRM) 9.1 DC-DC Converter Design Guidelines* for more information. A VRM 9.1 compatible design is required for all E7505 chipset platforms.

13.2.1.2 2.5 V

The 2.5 V power plane powers the DDR DRAM core, the MCH DDR I/O ring, and the 2.5 V-to-1.25 V switching regulator. The 2.5 V power plane is created using a switching regulator, which should be able to support the specification listed in Table 13-2. This switching regulator receives its input directly from the 5 V power rail of the power supply. Refer to the DRAM specification for vendor specific maximum current.

13.2.1.3 1.5 V

The 1.5 V power plane powers the AGP 8X component and the AGP 8X interface located in the MCH. Refer to Table 13-2 for details.

13.2.1.4 1.25 V

The voltage regulator produces two 1.25 V rails. One rail is for DDR VREF. The other rail is for DDR VTERM. The switching regulator divides the 2.5 V power rail by two to drive 1.25 V reference voltage. This provides some common mode noise rejection between the DDR termination and I/O voltages. Because of power sequencing requirements, the 1.25 V power rail must be derived by the 2.5 V regulator. Refer to Table 13-2 for details.

13.2.1.5 1.8 V

The 1.8 V power plane is created using a switching regulator sourcing from the 5 V power rail on the power supply. The 1.8 V plane powers the ICH4 core logic and the hub interface I/O rings of the P64H2. Refer to Table 13-2 for maximum current specification.

13.2.1.6 1.2 V/ 1.3 V

The 1.2 V / 1.3 V power plane powers the MCH core logic. Refer to Table 13-2 for maximum current specification.

13.2.1.7 5 VSB

The 5 VSB power plane comes directly from the 5 VSB power rail and has two functions: to provide power to resume functions in I/O devices off of the ICH4, and to provide 1.8 VSB power through a linear regulator. Refer to Table 13-2 for the maximum current specification.

13.2.1.8 3.3 VSB

The 3.3 VSB power plane is the output of a 5 VSB-to-3.3 VSB voltage regulator. The power plane is used solely for the resume I/O features of the ICH4. Refer to Table 13-2 for maximum current specification.

13.2.1.9 1.8 VSB

The 1.8 VSB provides power to the resume logic within the ICH4. Refer to Table 13-2 for maximum current specification.

Table 13-2. Platform Component Max Current Specifications

Platform Component	Voltage Rail (V) / Max Current Specification (A)						
	1.2 / 1.3	1.25	1.500 (VID)	1.5	1.8	2.5	3.3
MCH	3.20	–	2.10	0.6	–	6.80	–
Intel® ICH4	–	–	–	0.97	–	–	0.61
DDR	–	6.2	–	–	–	21.00[3]	–
Intel® P64H2	–	–	–	–	2.66[1]	–	1.30[2]
CK408	–	–	–	–	–	–	0.36
Rail Totals (A)	3.2	6.2	2.10	1.03	2.66	27.80	2.27

NOTES:
1. P64H2 max current for 1.8 V based on 133 MHz (both segments) configuration.
2. P64H2 max current for 3.3 V based on PCI-X 66, 4 loads configuration.
3. Value will increase for 3 DIMM registered configurations.

13.3 Processor Power Delivery Ingredients

Discussions of processor power delivery can be broken down into seven ingredients:

- System Design
- Processor Load
- Voltage Regulator
- Power Planes
- Decoupling Capacitors
- Component Placement and Modeling
- Validation Testing

13.4 System Design

13.4.1 Power Delivery Layout Requirements

This section provides processor power delivery layout requirements that are common to both VR Module (VRM) and VR Down (VRD) based designs. Designing a dual-processor system which shares the same power plane requires careful consideration of how the VRM or VRD delivers power to two processors that can vary their DC and AC loading requirements. Specific placement recommendations for the VRM and VRD are detailed in Section 13.4.4 and Section 13.4.5 respectively. Note that the Voltage Regulator must be placed as close as possible to its processor, on one of the two sides of the socket that has the greatest density of power and ground pins.

The maximum distance between each processor and its voltage regulator module or the output inductors of an embedded Voltage Regulator should not be greater than 1.5 inches. To be more specific, the distance between the facing edges of the Voltage Regulator connector and the socket should be no more than 0.5 inch.

Processor VCC_CPU static and transient tolerances and the corresponding Voltage Regulator tolerances assume power distribution paths with resistances no greater than 0.4 mΩ and inductances no greater than 0.1 nH. Meeting these limits can be a challenge because of system layout constraints.

Refer to Figure 4-2 for the recommended stackup showing power and ground layer implementation. Power must be distributed as a plane. This plane can be constructed as an island on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the PCB. Processor power should never be distributed by traces alone.

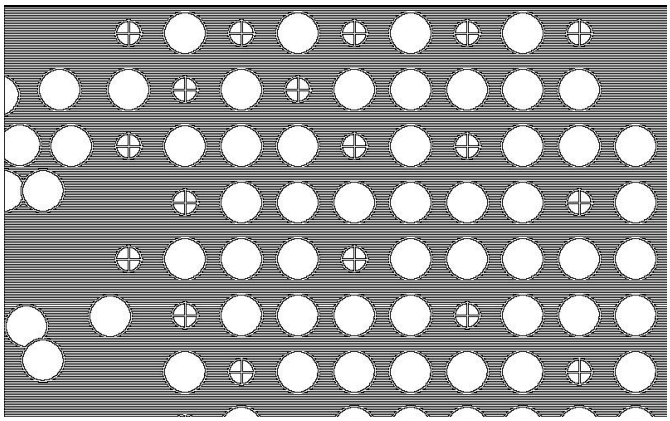
Because processor voltage is unique to most system designs, a voltage island is probably the most cost-effective means of distributing power to the processors. This island should not have any breaks from the source of power to the load to minimize inductance in the plane. It should completely surround all of the pins of the source and all of the pins of the load.

Use a 2 oz. copper power plane for VCC_CPU and a 2 oz. copper power plane for ground. Using the recommended power and ground plane copper weight and geometries minimizes resistance and inductance in the planes that affects the ability of the voltage regulator and decoupling to meet the DC and AC power requirements of the processors. This can be implemented on two 1 oz. copper layers or four 1/2 oz. copper layers. The bulk capacitors can be placed close to the processors, and the high-frequency capacitors should be placed next to the processors. Distribute the bulk and high-frequency capacitors equally on both sides of the socket where the power/ground pins are located.

The Intel Xeon processor socket has 603 or 604 pins (depending on processor package) with a 50 mil pitch. The routing of the signals, power, and ground pins require creation of may vias. These vias cause a “swiss cheese” effect in the power and ground planes beneath the processor, resulting in increased inductance of these planes. To minimize this swiss cheese effect, the power / ground planes should completely surround all of the pins of the VRM or VRD and processor socket. Also minimize the size of the processor socket vias’ anti-pads where possible. Anti-pads should be no larger than 35 mils. Figure 13-2 shows an example of good socket power/ground plane routing for an inner layer. Note the absence of plane cuts or other plane discontinuities that inhibit the current flow to these power pins. Bad power/ground routing to the processor socket pin vias and large anti-pads reduce the amount of effective copper, which may result in highly inductive current paths in the socket breakout region. Locations of the capacitor pads on the outer power layer should not hinder power distribution by creating a “slot”-shaped geometry in the plane. This can limit the ability of the decoupling capacitors and/or voltage regulator to supply the necessary current

response to processor transients. It is recommended that you place as many high-frequency capacitors as possible inside the cutout of the processor socket. The remaining high-frequency capacitors should be placed next to the processor, specifically near the power/ground pins.

Figure 13-2. Example of Good Plane Distribution to Power or Grounds of the Processor Socket



The data bus must route over a uniform power plane because of signal quality constraints. Consequently, in a multiprocessor system design, a single power plane should be used for power delivery to all processors. Multiple processors operating at different voltages are not supported, and will not be validated by Intel.

The processor VCC_SENSE and VSS_SENSE pins must be routed to vias. The vias should be as close to the socket pins as possible and should be connected with low impedance traces. Because these signals provide measurement points to verify adherence to the processor's VCC_CPU specifications, the vias need to be accessible to measurement equipment. These pins must not be used as SENSE lines to the VRs.

13.4.2 Multiple Voltages

The voltage regulator or voltage regulator modules provide the VCC_CPU supply to the processor and have the capability of supplying voltages from +1.1 V to +1.85 V. VCC_CPU supplies power to the processor core and on-die termination used for the system bus. The voltage regulator down solution is recommended only for dual processor systems. Refer to *Voltage Regulator Module (VRM) 9.1 DC-DC Converter Design Guidelines* or *Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines* for available voltage details.

Multiple voltages required for the processor are VCC_CPU = 1.5 V and SM_VCC = 3.3 V. VCCIOPLL, VCCA, and VSSA are the power supplies to the internal PLL. VCCIOPLL, VCCA and VSSA must be connected to VCC_CPU through a discrete RLC filter as described in Section 13.10. Refer to appropriate processor document for the pin location of these voltages.

13.4.3 Voltage Sequencing

When designing a system with multiple voltages, always ensure that no damage occurs to the system during voltage sequencing. Voltage sequencing is the timing relationship between two or more voltages, such as VCC_CPU and SM_VCC as shown in Figure 13-3. SM_VCC is required for correct operation of the processor VID logic.

The processor's VID outputs use an active driver. A 3.3 V source connected to the processor's SM_VCC pins supplies the VID output devices. As shown in Figure 13-4, the VID outputs are valid within 1 ms after the 3.3 V supply reaches 95% of its nominal value. The system power supply should generate PWR_OK no less than 100 ms after all of its outputs reach their respective 95% values. PWR_OK may be used to enable the VR output. For example a supply adhering to ATX12V design guidelines meets this requirement. The VR's PWRGD output may be used to generate the PWRGOOD input to the processor. PWR_OK should be de-asserted when any output of the supply falls below 95% of its nominal value (also consistent with ATX12V). It is important to maintain SM_VCC anytime the output of the VR is enabled. Driving the VR's OUTEN control input with the PWR_OK signal ensures correct sequencing at both power-up and power-down. In addition, when a processor asserts its THERMTRIP# signal, VCC_CPU must be disabled within 0.5 seconds.

Figure 13-3. VID Routing

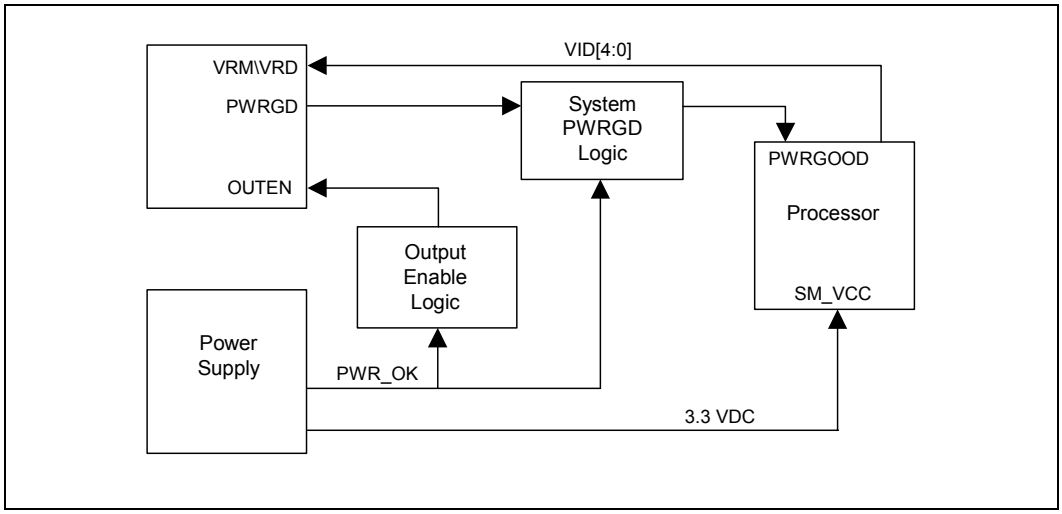
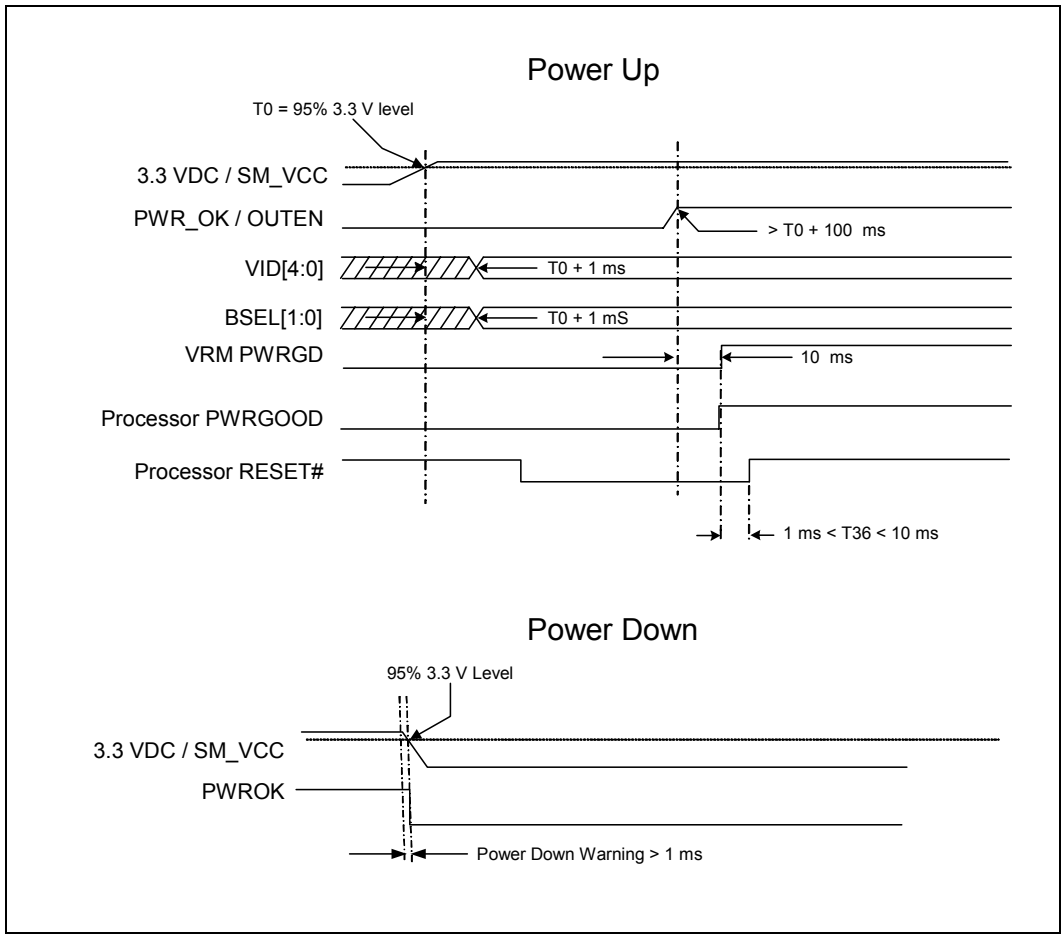


Figure 13-4. Power-Up and Power-Down Timing



13.4.4 Voltage Regulator Module 9.1 Recommendations

Figure 13-5 depicts the recommended two-way baseboard solution using VRMs. The block diagram also depicts the implementation of logic for monitoring the VID [4:0] of all processors. This logic should determine that all of the installed processors are requesting the same VCC_CPU. If mixed voltage processors are detected, the output enable signal (OUTEN) of all voltage regulators must be disabled. Note that if a processor is not installed, the VID [4:0] of that processor are high, and this should not cause disabling of the output of other VRMs.

Figure 13-5. Power Distribution Block Diagram for Two-Way System Motherboard with Voltage Regulator Modules

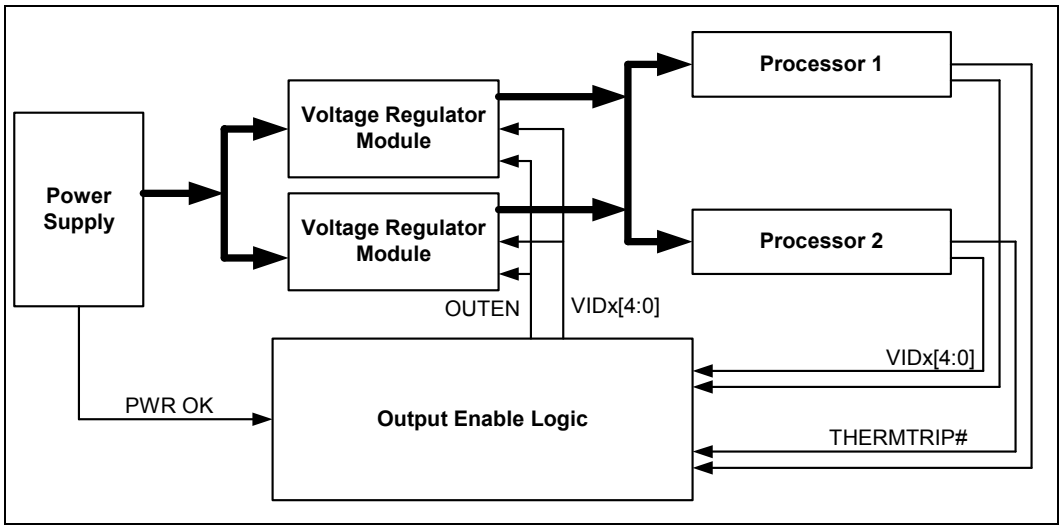
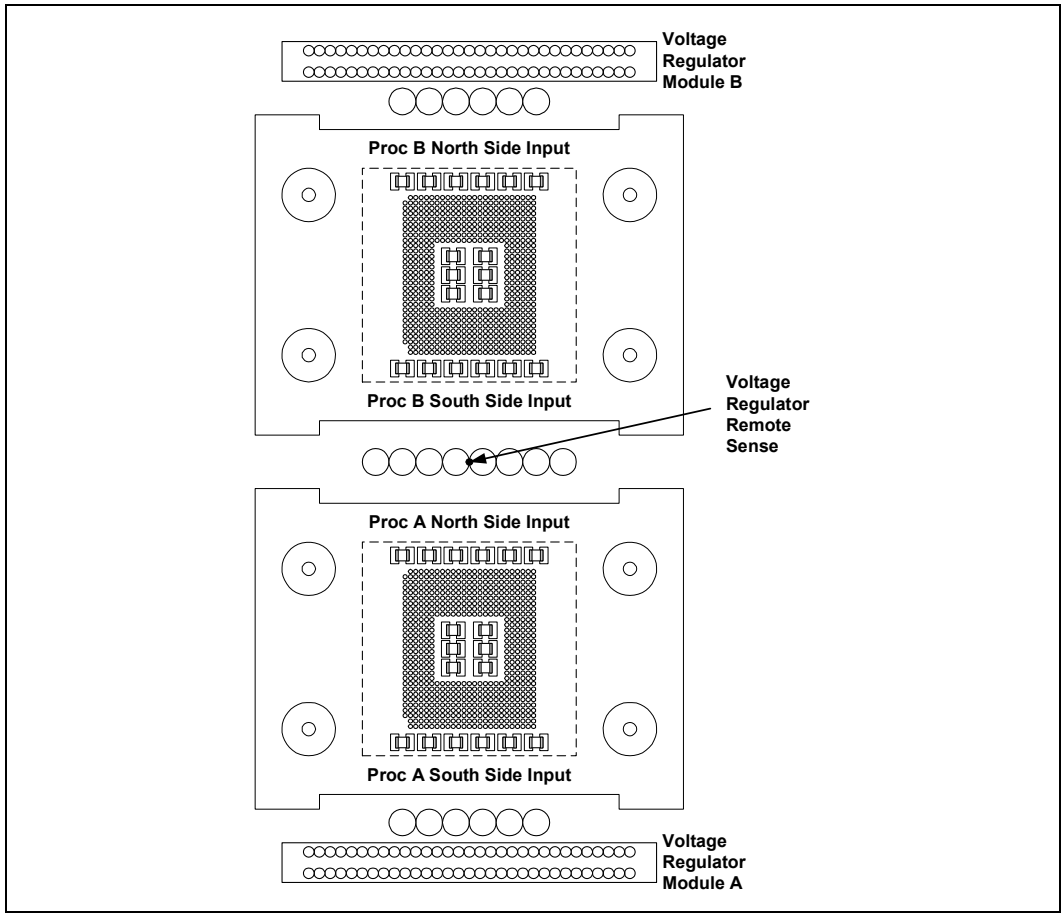


Figure 13-6 shows the recommended VRM implementation referred to as the “Row” pattern since the VRM and processor sockets are placed in a row with on another. The advantages of this placement is that the VRM current flow to its adjacent processor socket is not restricted by the other VRM.

Figure 13-6. “Row” Pattern with Voltage Regulator Modules



If available on the VRM, route the differential remote SENSE input signals (VO-sen+ and VO-sen-) from both VRM connectors to the middle of the VCC_CPU plane. These input signals allow the VRMs to sense output voltage and compensate for DC losses in the power distribution path. The round trip trace resistance of these signals should not be greater than 1 ohm. These voltage SENSE signals draw little current and should only have a minute voltage drop from the remote sense connection to the VRM socket.

Route the VO-sen+ signal for each VRM to the same point on the VCC_CPU power plane in the middle of and equidistant from both processors. Middle is defined as a point that provides the shortest geometrical mid-point between the centers of the processor sockets. Route the VO-sen- signal for each VRM to the same point at the corresponding X-Y location for the VO-sen+ route, but on the VCC_VSS ground plane. See Figure 13-6 for an example of sense point locations for the example VRM topology. The VO-sen+/VO-sen- signals should be routed directly from the VRM to the remote sense point without exceeding 5 inches in trace length.

13.4.5 Embedded Voltage Regulator Recommendations

Figure 13-7 shows the recommended two-way system baseboard solution involving a local embedded VRD. The block diagram depicts the implementation of logic for monitoring the VID [4:0] of both processors. This logic should determine that both of the installed processors are requesting the same VCC_CPU. If mixed voltage processors are detected, the OUTEN input signal of the voltage regulator must be disabled. Note that if a processor is not installed, the VID [4:0] of that processor are high, and this should cause the load line of the voltage regulator to adjust. The socket occupied pin, SKTOCC#, may also be used to detect the presence of a processor. See the *Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines*.

Figure 13-7. Power Distribution Block Diagram for Two-Way System Motherboard with Single Embedded Voltage Regulator

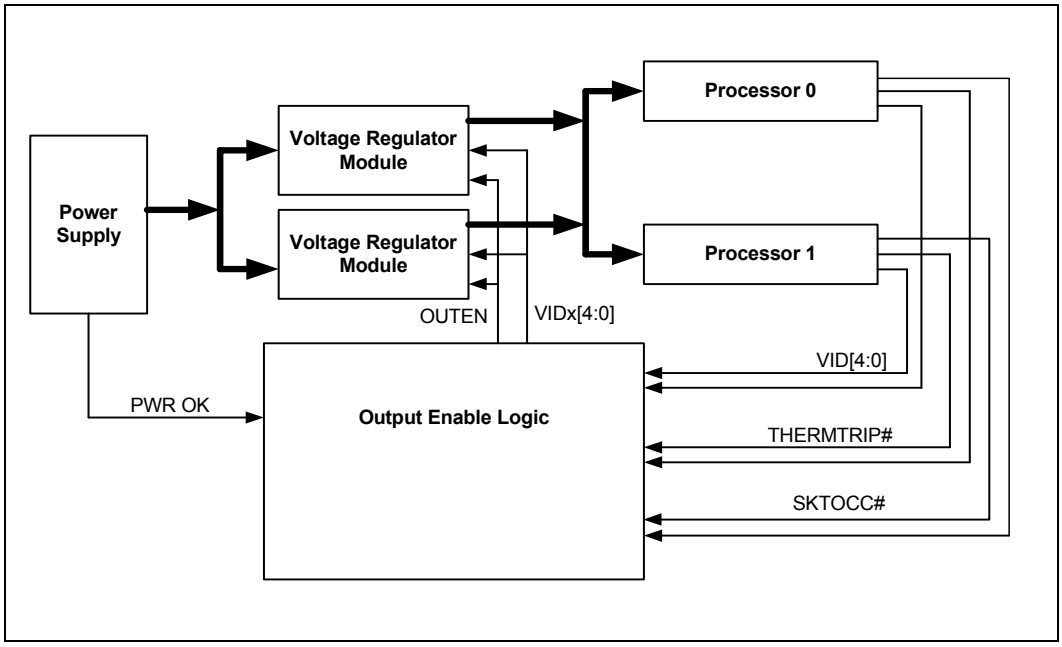


Figure 13-8 and Figure 13-9 show the two recommended VRD placements. Figure 13-8 is referred to as the "L" pattern since it has the two processor sockets and the VRD placed in an offset manner in the shape of an L. Figure 13-9 is referred to as the "Row" pattern since the two sockets are placed in the same line, with the VRD directly beneath both sockets. The advantage of both VRD placements are that the VRD current can flow to both processor sockets without overlapping currents or causing interference between both sockets. These placements also minmize and equalize the distance from the VRD to each socket.

Figure 13-8. “L” Pattern with Voltage Regulator Down

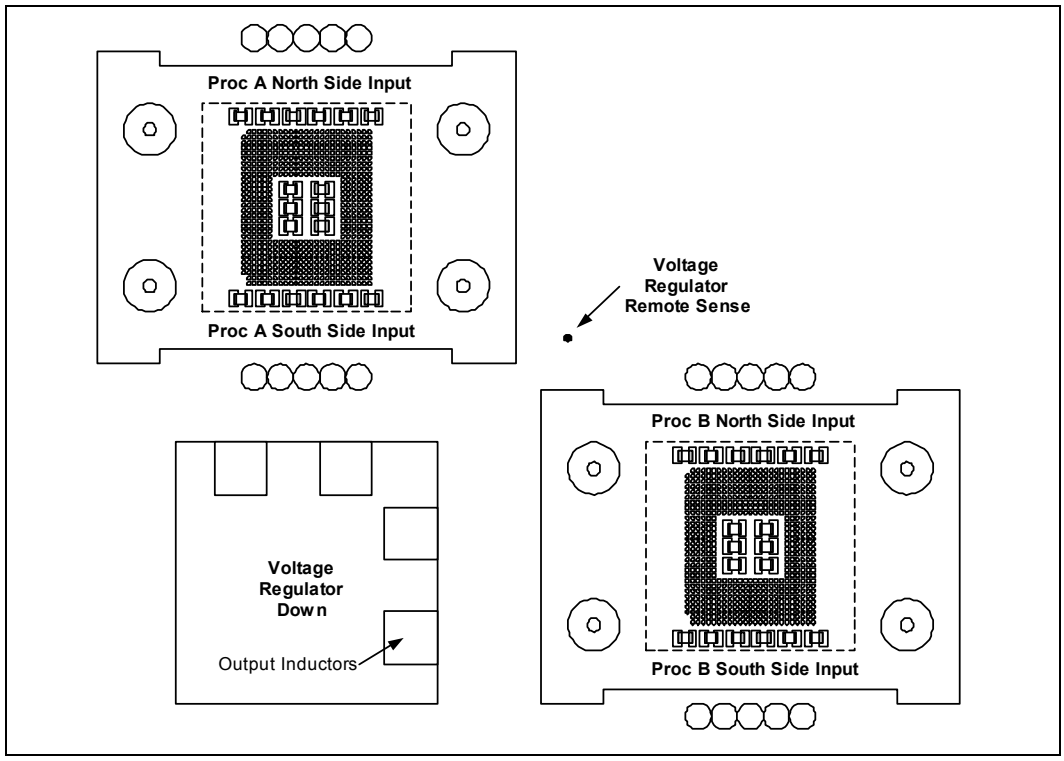
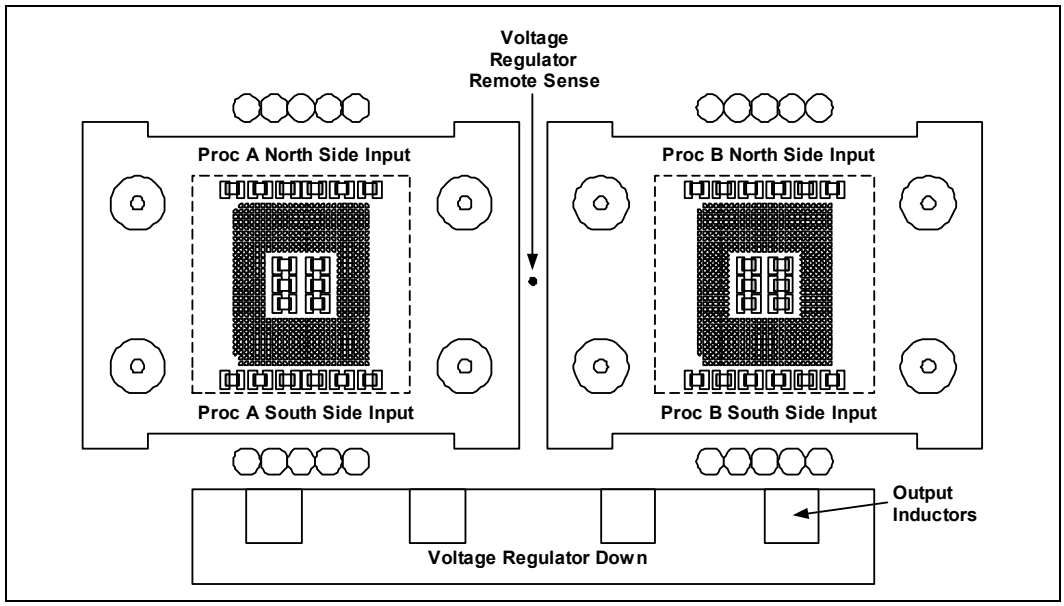


Figure 13-9. “Row” Pattern with Voltage Regulator Down



13.4.5.1 VRD Circuit Implementation

This section contains general VRD circuit and layout implementation recommendations. For specific VRD design details, refer to the *Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines* and VRD vendor documentation.

Route the VRD's voltage sense input signal to the middle of the VCC_CPU plane. The location of this plane connection and route is not critical. The voltage regulator Pulse Width Modulation (PWM) uses the voltage sense pin to monitor the VRD output voltage, which is used to generate the VRD power good signal.

The VRD circuit should contain low-pass filters (RC) on the output of each MOSFET phase. This filter reduces output noise and helps stabilize the VRD's operation. The exact filter values will depend on the voltage regulator PWM controller and MOSFET components used. Include series inductors at the output of each MOSFET phase. The exact value should be carefully chosen and will depend on the actual VR components used. Lowering the inductance value increases the transient current (dI/dt) capability of each output phase, but will increase power dissipation from the MOSFETs.

Carefully select the switching frequency of the PWM controller using the methods specified by the PWM vendor. The switching frequency should be chosen to support the static and transient requirements of both processors. Increasing the frequency will increase the response of the VRD, but will also increase the power dissipation of the phase drivers and MOSFETs.

Route the positive (and negative if the VRD provides differential inputs) voltage feedback inputs for the VRD to the VCC_CPU plane with the following conditions.

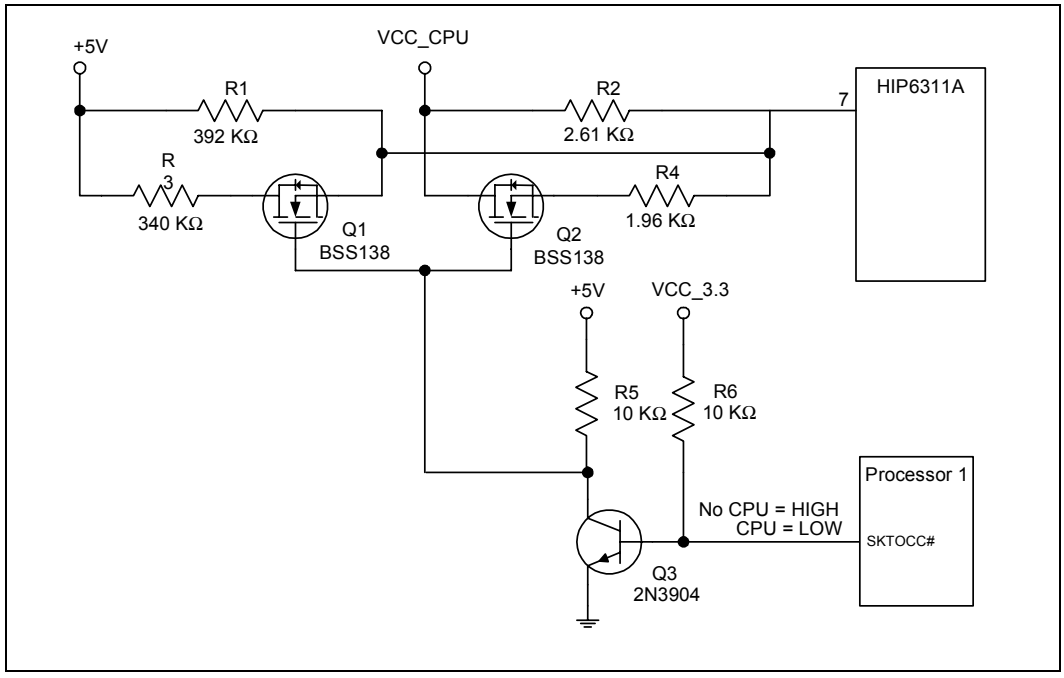
- They must be connected to the power plane through a series resistor. This resistor should be sized to provide the correct droop to satisfy the load line requirement.
- They must affect less than 1 Ω roundtrip resistance to minimize the voltage drop between the sense point and VR input.
- Route the positive feedback line to a point on the VCC_CPU power plane in the middle of and equidistant from both processors. Middle is defined as a point that provides the shortest geometrical mid-point between the centers of the processor sockets.
- Route the negative feedback line to the corresponding X-Y location, but on the VCC_VSS ground plane. See Figure 13-8 and Figure 13-9 for an example of sense point locations for the example VR topologies.
- Route each of the feedback lines with less than 5 inches total trace length. Do not route near signal lines unless shielding is provided.

The trace(s) should be carefully routed to avoid picking up noise.

13.4.5.2 Loadline Selection Circuitry

Many OEMs require that a dual-processor VRD supplying an Intel processor's common voltage plane operate with either one or two processors installed on the board (i.e., the design must meet the static and transient voltage characteristics of both the dual- and single-processor load lines). Failure to adjust the voltage regulator's loadline output based on the number of processors installed will deterioriate the regulator's ability to meet the processor's static loadline requirements under varying loads when one and two processors are installed. A solution is to adjust the load line for the number of installed processors. OEMs that want jumper-free systems can do this with logic that detects the presence of processors in each of the sockets, and selects resistor combinations to produce the right slopes. For example: no processors (00) = disable VRD;
one processor (01 or 10) = single-processor load line; both processors (11) = dual-processor load line. Figure 13-10 shows an example of how to implement such circuitry.

Figure 13-10. Example Load Line Selection Circuit



The theory of operation of the dual processor load line selection circuit is straightforward. If a second processor (Processor 1) is not present, then the base of Q3 will be pulled high. This will cause Q3's collector to go to ground, turning off Q1 and Q2. The VCC_CPU voltage will then go through R2 (droop resistor) to pin 7 (FB) of the HIP6311A controller. The offset voltage comes from the +5 V source through R1 into pin 7 of the controller. R3 and R4 will have no effect.

If a second processor is present, then the base of Q3 will be pulled low and Q3's collector will be high, turning on Q1 and Q2. The droop resistor, R2, will now be paralleled by R4, providing the droop required for a two-processor system. The offset resistor, R1, will be paralleled by R3 providing the offset for a two-processor system.

13.5 Power Planes

VCC_CPU static and transient tolerances of the processor and the corresponding voltage regulator tolerances assume power distribution paths with round trip resistances no greater than 300 µΩ and inductances no greater than 100 pH. Power must be distributed as a plane. This plane can be constructed as an *island* on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the PCB. Processor power should never be distributed by traces alone.

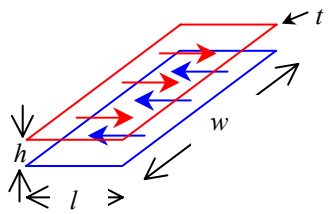
Because processor voltage is unique to most system designs, a voltage island will probably be the most cost-effective means of distributing power to the processors. This island from the source of power to the load should not have any breaks to minimize inductance in the plane. It should also completely surround all of the pins of the source, and all of the pins of the load.

13.5.1 Sheet Inductance/Resistance and Emission Effects of Power Plane

The imperfections of the power planes themselves may introduce unwanted resistance and inductance into the power distribution system. Assuming layer thickness is smaller than skin depth, the metal layer resistance can be calculated as:

$$R = \rho \cdot \frac{l}{w \cdot t}$$

Where ρ is the copper resistivity (ρ = 0.667 mΩ-mil), *l*, *w*, and *t* are the length, width and thickness of the metal layer, respectively.



The loop inductance can be calculated as:

$$L = 31.9 \frac{\text{pH}}{\text{mil}} \cdot \frac{l \cdot h}{w \cdot (N-1)}$$

Where *N* is the number of VCC_CPU/VSS_CPU planes. To minimize parasitic layer inductance, it is important to reduce the distance from decoupling capacitors to the processor socket (reducing *l*), and to use islands for power distribution (increasing *w*). To reduce *h*, it is recommended to select the VCC_CPU/VSS_CPU planes in the layer stack up that are interleaved and have small spacing in between. As a practical matter it is impossible to get the requisite baseboard inductance without locally dedicating at least 4 planes to carry power from the baseboard capacitors to the power pins of the processor.

There are impedance consequences for signals that cross over or under the edges of the Power Island that exists on another layer. While neither of these may be necessary for most designs, there are two reasonable options to consider that can protect a system from these consequences:

- Processor power islands can be isolated from signals by one of the solid power plane layers such as the ground layer. This forces a particular stack-up model.
- Another option that helps, but does not completely eliminate, radiation effects is to decouple the edges of the processor power islands to ground on regular intervals of about 1 inch using good high-frequency decoupling capacitors (1206 packages). This requires more components, but does not require any particular board stack-up.

In either case, for controlling emissions, all planes and islands should be well decoupled. The exact board layout and the chassis design will determine the amount of decoupling required for controlling emissions. Proper designs will incorporate additional pads for capacitors to be added in case they are found to be necessary during EMI testing.

Signals routed over power islands or islands in the ground plane create a discontinuity in the return path of that signal. This discontinuity can have detrimental effects on the timing and signal quality of that signal and on other signals that reference the same planes. Avoid routing signals over splits in power planes or ground planes at all times.

Example

Given power bussing area from the regulator to the socket approximated as a rectangle, with the following dimensions for the power and ground plane: l = 0.279 inch; w = 2.09 inch; t = 1.24 mils (1 oz. copper):

$$R = 0.677\ \text{m}\Omega \cdot \text{mil} \cdot \frac{0.279"}{2.09 \cdot 1.24\ \text{mil}} = 0.073\ \text{m}\Omega$$

The total resistance of the round trip is:

$$R = 2 \cdot 0.073\ \text{m}\Omega = 0.15\ \text{m}\Omega$$

With the VCC_CPU – VSS_CPU separated by 4.5 mils, the loop inductance is:

$$L = 31.9\frac{\text{pH}}{\text{mil}} \cdot \frac{0.279\ \text{mil} \cdot 4.5\ \text{mil}}{2.09\ \text{mil} \cdot (2-1)} = 19.2\ \text{pH}$$

13.6 Decoupling Capacitors

13.6.1 Decoupling Technology and Transient Response

The inductance of the system due to cables and power planes slows the power supply's ability to respond quickly to a current transient. Decoupling a power plane can be broken into several independent parts. The closer to the load the capacitor is placed, the more inductance that is bypassed. By bypassing the inductance of leads, power planes, etc., less capacitance is required. However, there is less room for capacitance closer to the load . Therefore trade-offs must be made.

The processor causes very large switching transients. These sharp surges of current occur at the transition between low power mode and high power mode. It is the responsibility of the system designer to provide adequate high-frequency decoupling to manage the highest frequency components of the current transients. To lower total board inductance and resistance, the processor is designed with 188 VCC_CPU and 189 VSS_CPU (ground) pins. The designer must support a current slew rate of 450 A/µs at the socket pins. Larger bulk storage, such as OSCON capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition.

All of this power bypassing is required due to the relatively slow speed at which a DC-to-DC converter can react. A typical voltage converter has a reaction time on the order of 1 µs to 10 µs, while the processor's current steps are on the order of 100 ns to 200 ns. Bulk capacitance supplies energy from the time the high-frequency decoupling capacitors are drained until the power supply can react to the demand. More correctly, the bulk capacitors in the system slow the transient requirement seen by the power source to a rate that it is able to supply, while the high-frequency capacitors slow the transient requirement seen by the bulk capacitors to a rate that they can supply.

A load-change transient occurs when coming out of or entering a low power mode. This load-change transient can be on the order of 55 amps. These are not only quick changes in current demand, but are also long lasting average current requirements. These load change transients are observed when the processor enters or leaves a low power state. Refer to the appropriate processor documentation listed in Section 1.1 for further information regarding the low power states. Note that even during normal operation, the processor current requirements can change by as much as 70% (± 10%) of the max current very quickly.

Maintaining voltage tolerance during these changes in current requires high-density bulk capacitors with low Effective Series Resistance (ESR) and low Effective Series Inductance (ESL). Use thorough analysis when choosing these components.

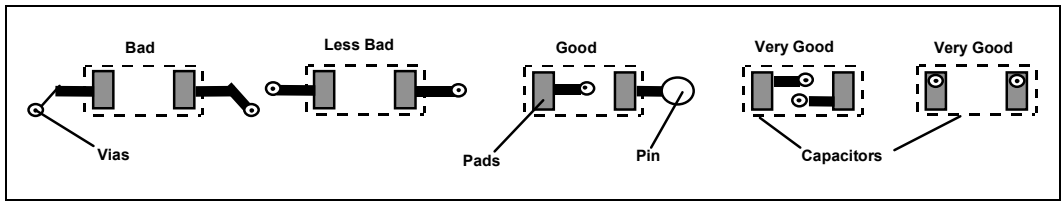
Using capacitors with the wrong ESR, ESL, and/or package can mitigate their intended operation and result in violations of the processor power specifications. For example, capacitors with the wrong package or with ESR/ESL properties in excess of the recommendations may have increased transient response times that are unable to respond to the processor’s current transients.

13.6.2 Location of High-Frequency Decoupling

A system designer for the processor should design properly for high-frequency decoupling. High-frequency decoupling should be placed as close to the power pins of the processor as physically possible. Use both sides of the board if necessary for placing components to achieve the optimum proximity to the power pins. This is vital because the inductance of the board's metal plane layers could cancel the usefulness of these low inductance components.

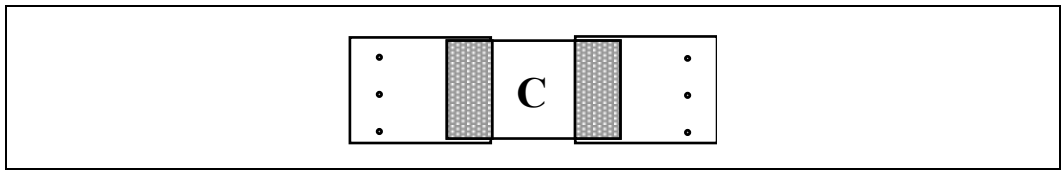
Another method to lower the inductance is to shorten the path from the capacitor pads to the pins that it is decoupling. If possible, place the vias connecting to the planes within the pad of the capacitor. If this is not possible, keep the traces as short and wide as is feasible. Possibly one or both ends of the capacitor can be connected directly to the pin of the processor without the use of via. Even if simulation results look good, these practical suggestions can help to improve the decoupling situation where they can be applied in layout. Figure 13-11 illustrates these concepts.

Figure 13-11. 1206 Capacitor Pad and Via Layouts



If polymer capacitors or large ceramics are used, avoid the loss of the low ESL characteristic by connecting via patterns as wide as the capacitor with multiple via holes per connection, as shown in Figure 13-12.

Figure 13-12. Connections to Via Patterns



13.6.3 Location of Bulk Decoupling

The location of bulk capacitance is not as critical as the high-frequency decoupling because more inductance is already expected for these components. However, good placement of these components will improve the transient response of the system, as shown in simulation. In addition to the bulk capacitors on the voltage converter module (which are electrically **behind** the inductance of the converter pins), several bulk capacitors must be placed close to the processor socket.

Place half on one side of the processor socket, half on the other side as close as the logic analyzer interface (LAI), retention mechanism (RM) and heatsink keep-out zones allow. Capacitors should be placed a maximum of 0.5 inches from the processor socket. Check with your LAI, RM and heatsink vendors for those keep-out zone requirements. When using the Intel Xeon processor boxed processor solution, refer to the *Intel® Xeon Processor with 512-KB L2 Cache Datasheet* for keep-out zone details.

13.6.4 Decoupling Recommendation

Intel recommends that the baseboard design incorporate at least ten 560 µF OSCON bulk capacitors and twenty 22 µF ceramic capacitors per processor. The bulk capacitors should be placed half on one side of the processor and half on the other as close to the processor package as the keep-out zone allows. One quarter of the ceramic capacitors should be placed on one side of the processor, one quarter on the other side, and half in the processor cavity using both sides of the board. See Section 13.7 for placement options. Check with the voltage regulator designer for optimum choice of bulk capacitors. Some very high switching regulators are better served by replacing the OSCON bulk capacitors with additional high-frequency ceramics. Table 13-3 provides the parameters for bulk and high-frequency capacitors.

13.7 Component Placement and Modeling

Intel recommends using simulation to design and verify Intel Xeon processor with 512-KB L2 and Intel Xeon processor with 533 MHz system bus based systems. The models in the following sections can be used to piece together a complete base board spice circuit.

The maximum distance between each processor and its voltage regulator module or the output inductors of an embedded voltage regulator should not be greater than 1.5 inches. To be more specific, the distance between the facing edges of the VRM connector (or the output terminal of the output inductor of an embedded voltage regulator) and the socket should be no more than 0.5 inches. The bulk capacitors can be placed close to and the high-frequency capacitors should be placed next to the processors. Distribute the bulk and high-frequency capacitors equally on both sides of the socket where the power/ground pins are located (the east and west side).

The routing of the signals, power, and ground pins require numerous vias. These vias cause a “Swiss cheese” effect in the power and ground planes beneath the processor, resulting in increased inductance of these planes. Because of this “Swiss cheese” effect, the minimum manufacturable antipad should be used for the power and ground vias under the processors. The smaller the antipad, the more copper that will be available. Place as many high-frequency capacitors as possible inside the cutout of the processor socket. The remaining high-frequency capacitors should be placed next to the processor, specifically the power/ground pins.

Processors should be placed with respect to the voltage regulator or voltage regulator modules and bulk decoupling capacitors such that current to one processor does not flow in the same path as that of any other processor.

13.7.1 Component Models

Acquire component models from their respective manufacturers. Intel does not guarantee the specifications of another manufacturer's components. This section contains some of the models developed by Intel for internal simulations.

Table 13-3. Various Component Models Used at Intel (Not Vendor Specifications)

Component of Simulation	ESR (Ω)	ESL (nH)
0.1 µF Ceramic 0603 package	0.006	0.63
1 µF Ceramic 0805 package	0.080	0.702
10.0 µF Ceramic 1206 package	0.010	1.1
22.0 µF Ceramic 1210 package	0.010	1.1
560 µF OSCONS	0.012	3.1

13.7.2 Processor Socket-Package Lump Model

Figure 13-13 shows the lump electrical model for the high-frequency baseboard capacitors, the processor socket, and the processor package. Figure 13-14 shows a physical picture of the model which serves as a sub-circuit for the following baseboard models in this section. Table 13-4 lists the model's component values. L2 and L6 refer to the inductance and resistance of the power plane next to the processor socket area (i.e., “before Swiss cheese” area). L3 and L5 refer to the inductance and resistance of the power plane within the processor socket area, i.e., “after Swiss cheese” area. The inductance and resistance of the power plane between voltage regulator and bulk capacitors and the processor is shown as L1 and L7. A current step from 0 A to 55 A should be applied with a rise time of 308 ns, or the PWL values may be used.

Figure 13-13. Processor Lump Model Drawing

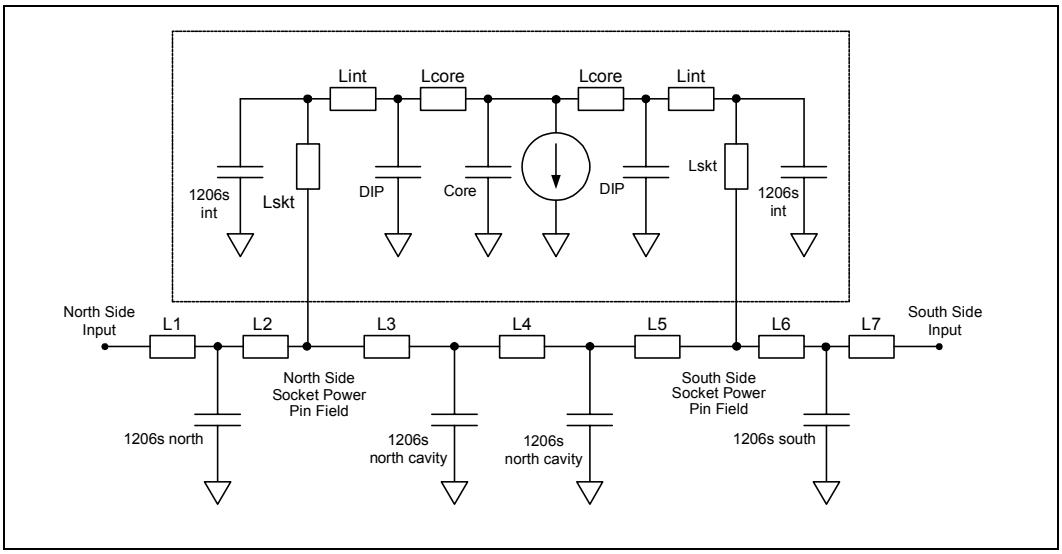
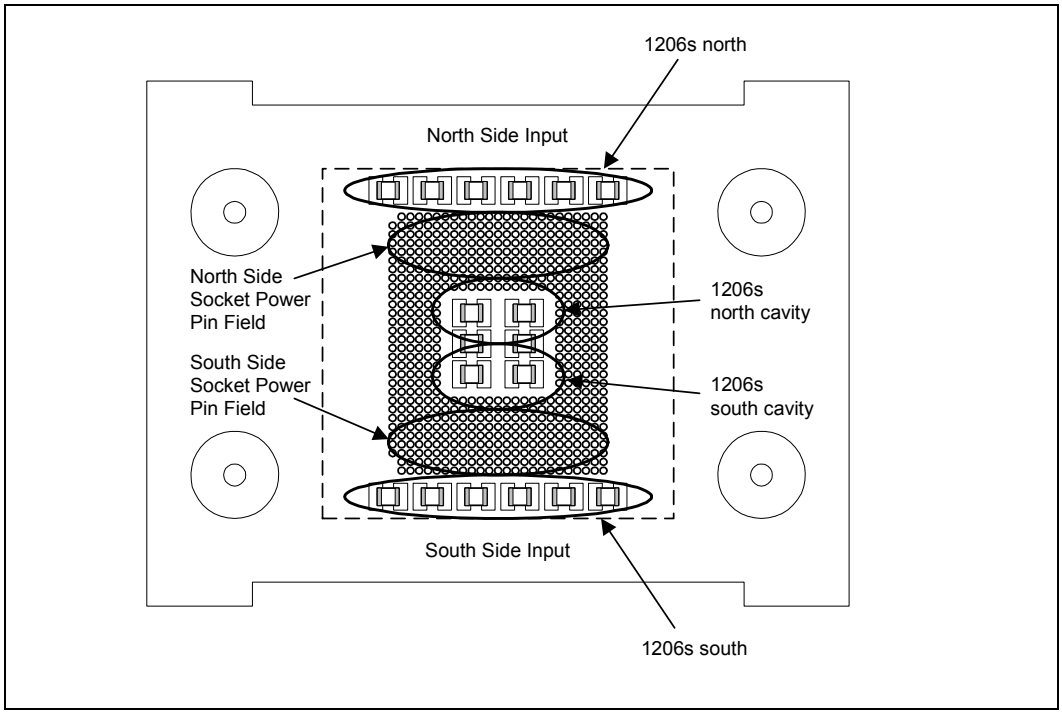


Table 13-4. Processor Lump Model Component Values

Component	Description	Value		
		Resistance	Inductance	Capacitance
1206s north/south	Five 22 µF MLCC	10 mΩ / 5	1.1 nH / 5	5 * 22 µF
1206s north/south cavity	Five 22 µF MLCC	10 mΩ / 5	1.1 nH / 5	5 * 22 µF
1206s int	Interposer MLCC	833 µΩ	45 pH	120 µF
DIP capacitors	Package Capacitors	270 µΩ	2.35 pH	36 µF
Core capacitors	Die Capacitance	146 µΩ	0	541 nF
L1	North side Input	170 µΩ	23 nH	N/A
L2	North side pin field input	150 µΩ	23 nH	N/A
L3	North side cavity input	120 µΩ	18 nH	N/A
L4	Cavity	130 µΩ	20 nH	N/A
L5	South side cavity input	120 µΩ	18 nH	N/A
L6	South side pin field input	150 µΩ	23 nH	N/A
L7	South side input	170 µΩ	23 nH	N/A
Lskt	Socket Impedance	326 µΩ	24 pH	N/A
Lint	Interposer Impedance	125 µΩ	12 pH	N/A
Lcore	Package Impedance	25 µΩ	1 pH	N/A

Figure 13-14. "Row" Pattern with Embedded Voltage Regulator



13.7.3 Dual-Processor Component Placement and Models

This section provides recommended placement diagrams and lump electrical model schematics for dual processor systems. Baseboard impedances are estimates based on minimum copper weight requirements.

Figure 13-15. Dual-Processor "Row" Pattern with Embedded Voltage Regulator

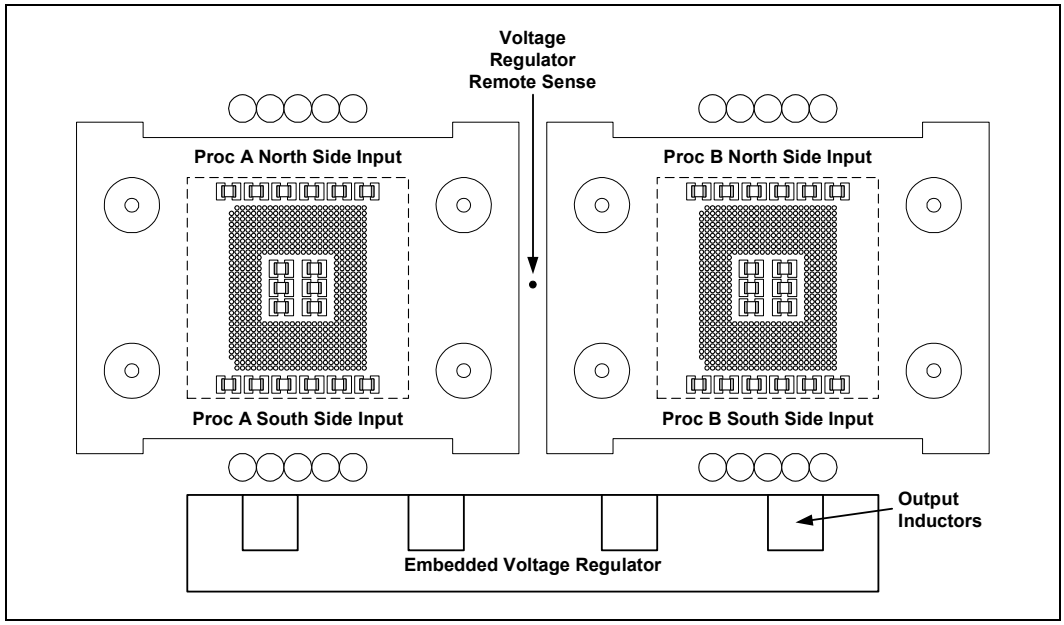


Figure 13-16. Processor Lump Model Drawing

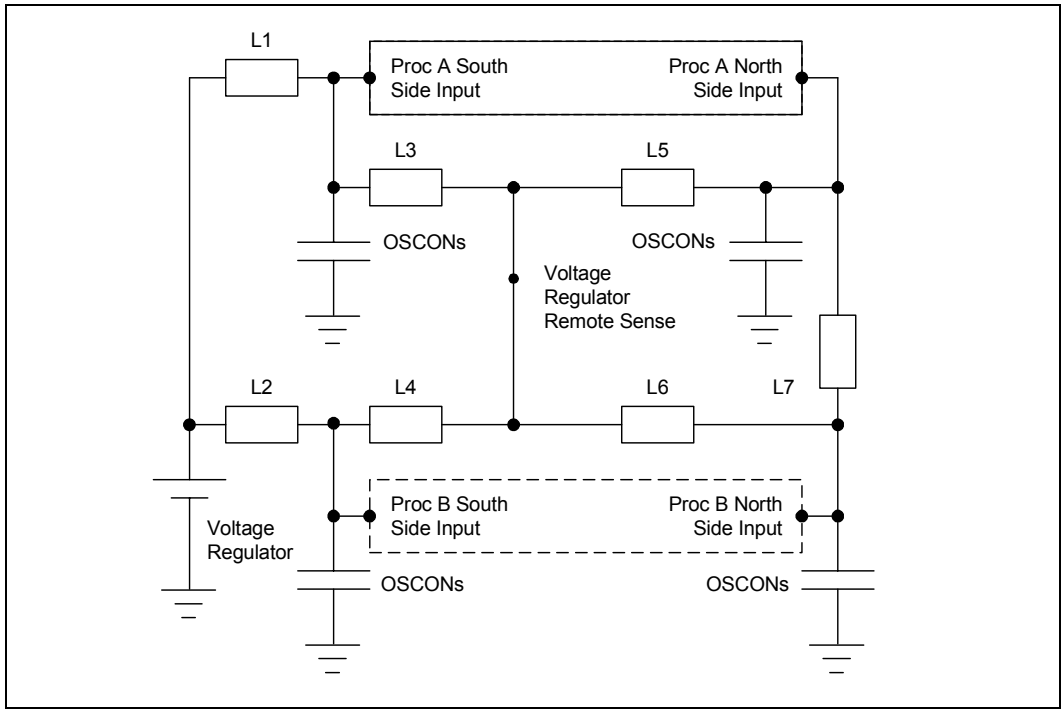


Table 13-5. "Row" Pattern with Embedded Voltage Regulator Schematic Values

Component	Description	Value		
		Resistance	Inductance	Capacitance
OSCONs	Bulk Capacitors	12 mΩ / 5	3.1 nH / 5	5 x 560 µF
L1	VRM A – Proc A south	75 µΩ	20 pH	N/A
L2	VRM A – Proc B south	75 µΩ	20 pH	N/A
L3	Proc A south – sense	600 µΩ	160 pH	N/A
L4	Proc B south – sense	600 µΩ	160 pH	N/A
L5	Proc A north – sense	600 µΩ	160 pH	N/A
L6	Proc B north – sense	600 µΩ	160 pH	N/A
L7	Proc A north – Proc B north	1.2 µΩ	320 pH	N/A

13.8 Validation Testing

The processor VCC_SENSE and VSS_SENSE pins should be routed to vias. The vias should be as close to the socket pins as possible, and should be connected with a low impedance trace. Because these signals provide measurement points to verify adherence to the processor's VCC_CPU specifications, the vias must be accessible to measurement equipment.

Intel recommends the following guideline when measuring the transients on the processor VCC_CPU:

- The measurement should be performed across the VCC_CPU and VSS_CPU pins on the processor socket.
- Use an oscilloscope with 100 MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 mΩ minimum impedance.
- The maximum length of ground wire on the probe should be less than 5 mm.
- Ensure that external noise from the system is not coupled in the scope probe. Some probes have a very significant level of inherent noise. Attempt to minimize noise by investigating different probes. Use a differential probe to make the voltage measurements.
- The bandwidth of the probe should be no less than the oscilloscope.
- Ensure that all connections from the oscilloscope to the motherboard pin are good, and that they have a very low contact resistance.

13.9 Generating and Distributing GTLREF[3:0]

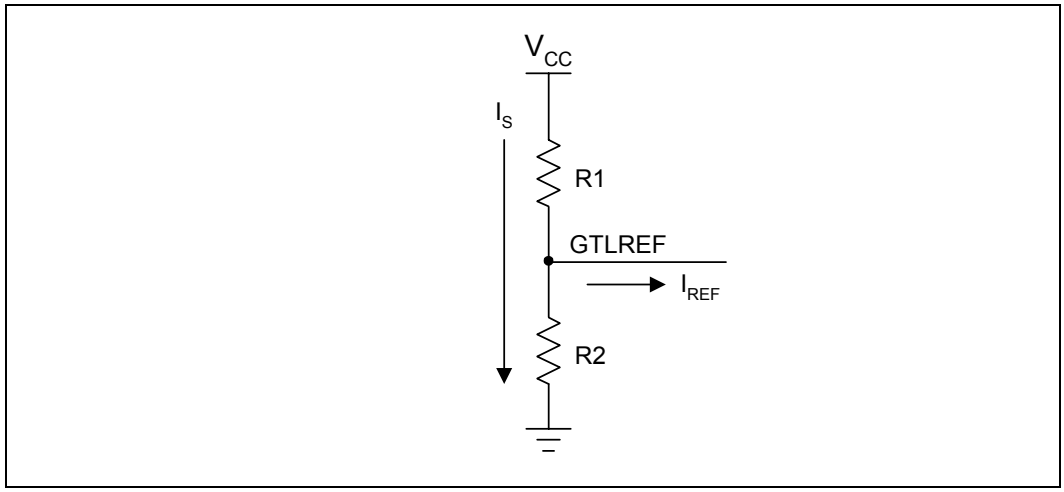
GTLREF[3:0] are low current inputs (less than 15 µA each) to the differential receivers within each of the components on the AGTL+ bus. A simple voltage divider can generate GTLREF[3:0]. The GTLREF[3:0] inputs must meet the 2% specification.

Equation 13-1 uses R1 = 2 * R2 to generate a GTLREF set at a nominal value of 0.63 VCC_CPU. Figure 13-17 illustrates using 1% resistors to generate the GTLREF specification of 0.63 VCC_CPU ± 2%.

Equation 13-1. Creating GTLREF of .63 VCC_CPU

$$V_{REF} = V_{CC} \times \frac{R_1}{R_1 + R_2} = V_{CC} \times \frac{2 \times R_2}{2 \times R_2 + R_2} = .63 V_{CC}$$

Figure 13-17. GTLREF



R1 and R2 should be small enough values that the current drawn by the GTLREF inputs (I_{REF}) is negligible with respect to the current caused by R2 and R1.

A complete analysis of all circuit currents going into and out of the center node, as in Equation 13-2, will provide the final GTLREF of the circuit. The parameter "n" is the number of I_{REF} inputs supplied by the divider.

Equation 13-2. Node Analysis

$$I(R_2) = I(R_1) + n \times I_{REF}$$

Plugging in for the currents and rearranging the equation provides the following:

Equation 13-3. Node Analysis in Terms of Voltage

$$\frac{V_{CC} - GTLREF}{R_2} - \frac{GTLREF}{R_1} = n \times I_{REF}$$

The above equation leads to the following:

Equation 13-4. Solving for GTLREF

$$GTLREF = \frac{V_{CC}/R_2 - n \times I_{REF}}{1/R_2 + 1/R_1}$$

The worst case GTLREF should be analyzed with I_{REF} at the maximum and minimum values determined for the number of loads being supplied. If the number of loads can change from model to model because of upgrades, this should be taken into account as well. Analyze Equation 13-4 with R_1 and R_2 at the extremes of their tolerance specifications.

13.9.1 GTLREF [3:0]

Intel recommends two voltage dividers for each processor, and one for the chipset component. Assume a maximum of 15 µA of leakage current per load. Note that these leakage currents can be positive or negative.

The following describes using a single voltage divider to support two GTLREF Loads, assuming VCC_CPU of 1.7 V. Using 1% resistors for the voltage divider in Figure 13-18, make R_1 a 84.5 Ω resistor, and use 49.9 Ω for R_2. This creates a static usage of 11.2 mA (1.5 V / 134.4 Ω) per voltage divider. After looking at all combinations of R_1 and R_2 (above and below tolerance) and I_{REF} (±30 µA), the worst case solution for Equation 13-4 can be found with I_{REF} at 30 µA, R_1 at the low end of its tolerance specification (83.7 Ω), and R_2 at the high end of its tolerance specification (50.4 Ω). This yields:

Equation 13-5. Node Analysis

$$V_{REF} = \frac{1.5/50.4 - .000030}{1/50.4 + 1/83.7} = 0.9353V$$

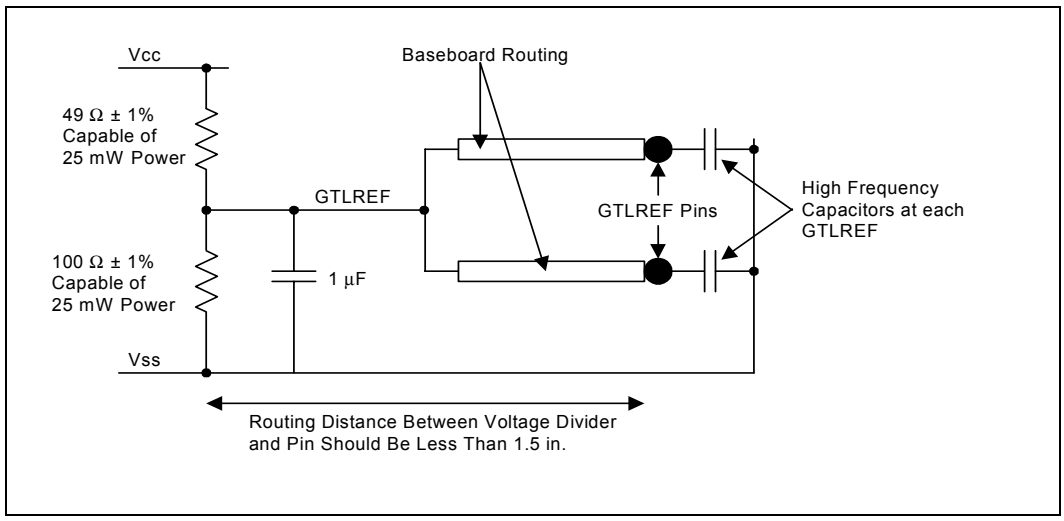
Because the target of 0.63 of VCC_CPU is 0.945 V, this setting is within 1.0% of the 0.63 point and satisfies the 2% specification. A spreadsheet program allows the reader to easily verify the other corners. Varying over its tolerance range has minimum effect.

These values chosen for R_1 and R_2 have additional benefits: The parallel combination terminates the GTLREF line to 31.4 Ω. These generally available resistance values reduce resistor cost.

Decouple GTLREF[3:0] at each pin with a 220 pF capacitor to VSS_CPU. Decoupling GTLREF to VSS_CPU at the voltage dividers with a 1 µF capacitor may further enhance the ability for GTLREF to track VCC_CPU.

When routing GTLREF to the pins, use a 30-mil–50-mil trace (the wider the better), and keep it as short as possible (less than 1.5 inches). Also, keep all other signals at least 20 mils away from the GTLREF trace. This provides a low impedance line without the cost of an additional plane or island. Because of the placement of the GTLREF pins on the processor, it may not be possible or convenient to route all four pins from one voltage divider. It is acceptable to use more than one voltage divider with decoupling at each voltage divider and each pin.

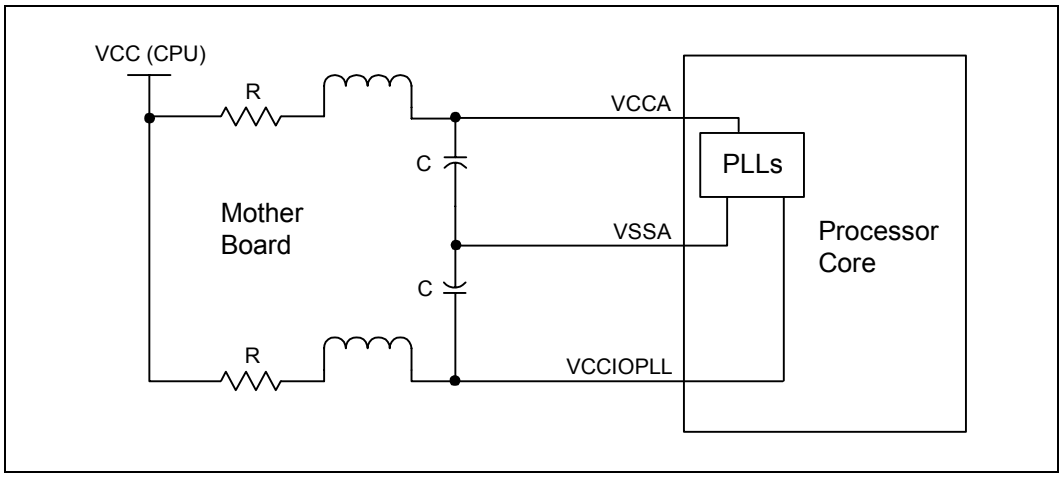
Figure 13-18. Suggested GTLREF Generation



13.10 Filter Specifications for VCCA, VCCIOPLL, and VSSA

VCCA and VCCIOPLL are required by the processor's internal PLL. These voltages are created by using a low pass filter on VCC_CPU. The processor has internal analog PLL clock generators that require quiet power supplies for minimum jitter. Jitter is detrimental to a system. It degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). The filter topology is shown in Figure 13-19. Not shown in the figure are the parasitics of connecting traces, circuits, and components.

Figure 13-19. Processor Filter Topology



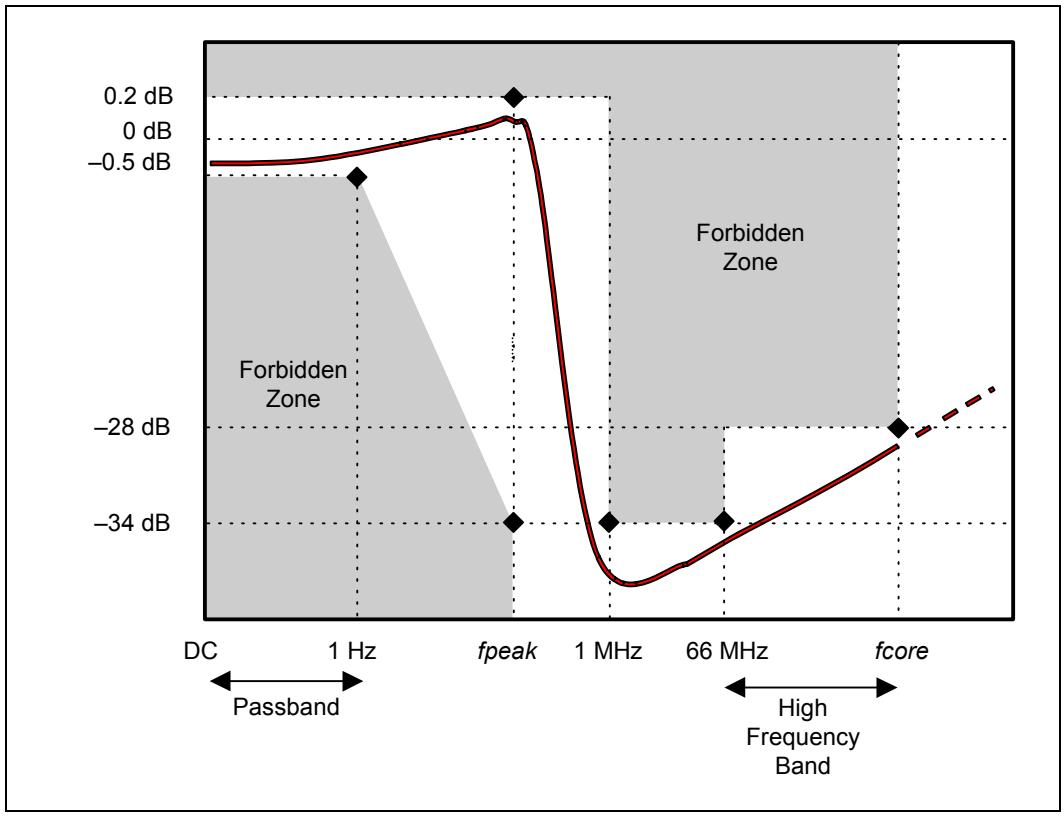
The filter has two functions. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity, we are addressing the recommendation for VCCA filter design. The same characteristics and design approach are applicable for VCCIOPLL filter design.

The AC low-pass specification, with input at VCC_CPU and output measured across the capacitor, is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- 34 dB attenuation from 1 MHz to 66 MHz
- 28 dB attenuation from 66 MHz to core frequency

The filter specification (AC) is graphically shown in Figure 13-20.

Figure 13-20. AC Filter Specification



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond fcore.
3. Fpeak, if existent, should be less than 0.05 MHz.

Other requirements:

- Use shielded type inductor to minimize magnetic pickup.
- Filter should support DC current > 30 mA.
- DC voltage drop from VCC_CPU to VCCA should be < 33 mV, which in practice implies series R < 1.1 Ω. Also means pass band (from DC to 1 Hz) attenuation < 0.5 dB for VCC_CPU = 1.1 V, and < 0.35 dB for VCC_CPU = 1.7 V.

Table 13-6 and Table 13-7 list recommended filter components.

Table 13-6. Component Recommendation—Inductor

Part Number (Ref Designator)	Value	Tol	SRF	Rated I	DCR
TDK MLF2012A4R7KT **(L1)**	4.7 µH	10%	35 MHz	30 mA	0.56 Ω (1 Ω max)
Murata LQG21N4R7K10 **(L2)**	4.7 µH	10%	47 MHz	30 mA	0.7 Ω (±50%)

Table 13-7. Component Recommendation—Capacitor

Part Number (Ref Designator)	Value	Tol	ESL	ESR
Kemet T495D336M016AS	33 µF	20%	2.5 nH	0.225 Ω
AVX TPSD336M020S0200	33 µF	20%		0.2 Ω

To satisfy damping requirements, total series resistance in the filter (from VCC_CPU to the top plate of the capacitor) must be at least 0.35 Ω. This includes the DCR of the inductor, and any resistance (routing or discrete components) between VCC_CPU and capacitor top plate. Keep the routing short and wide. If the total is less than 0.35 Ω, add a discrete resistor to make up the difference. For example, if the selected filter inductor has a minimum of 0.1 Ω DCR and a negligible routing resistance (less than 10 mΩ), add a discrete resistor R1 of approximately 0.3 Ω.

The total maximum resistance in each route cannot be more than 1.1 Ω as measured from VCC_CPU (the baseboard via that connects the PLL filter to the VCC_CPU plane) to the processor interposer pin. It is important to keep the total resistance of each of the PLL filter circuits on the motherboard no larger than necessary. Figure 13-21 and Figure 13-22 illustrate the recommended filter circuit. This path includes the total trace resistance (denoted “R-TRACE” in Figure 13-21 and Figure 13-22), discrete resistor (if needed), inductor DCR, and Socket 603 resistance (0.025 Ω). It is important to note that “R-TRACE” includes the total trace resistance between VCC_CPU and the processor socket pin, but is represented in the figures as a single resistor to simplify the circuit representation.

Other routing requirements:

- C should be as close as possible to the VCCA and VSSA pins in the socket (typically < 0.02 Ω per route).
- Route away from clocks and fast switching signals.
- VCC_CPU route should be parallel and next to VSSA route (to minimize loop area).
- VCCIOPLL route should be parallel and next to VSSA route (to minimize loop area).
- L should be close to C; any routing resistance should be inserted between VCC_CPU and L.
- Any discrete R should be inserted between VCC_CPU and L.

Figure 13-21. Filter Implementation 1—Using Discrete Resistors

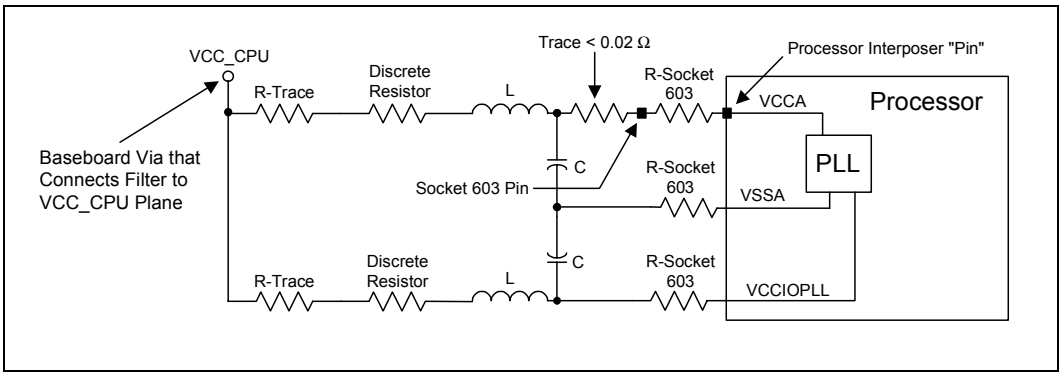
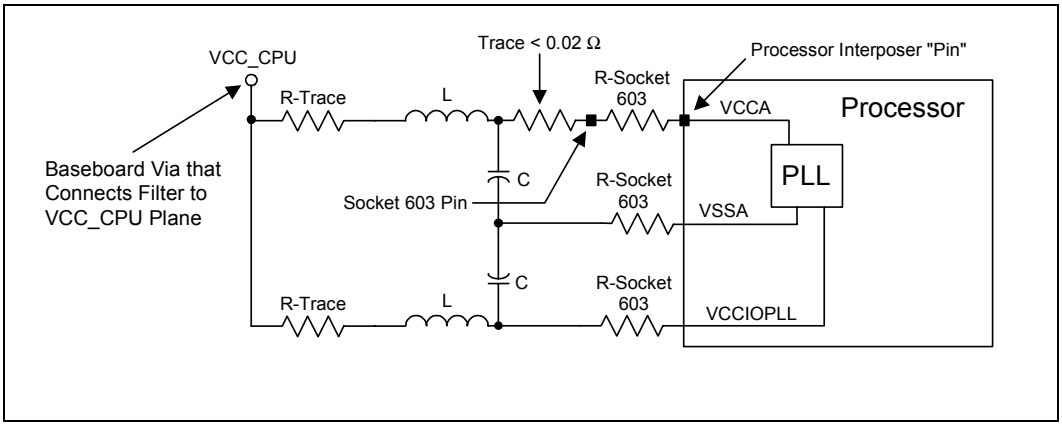


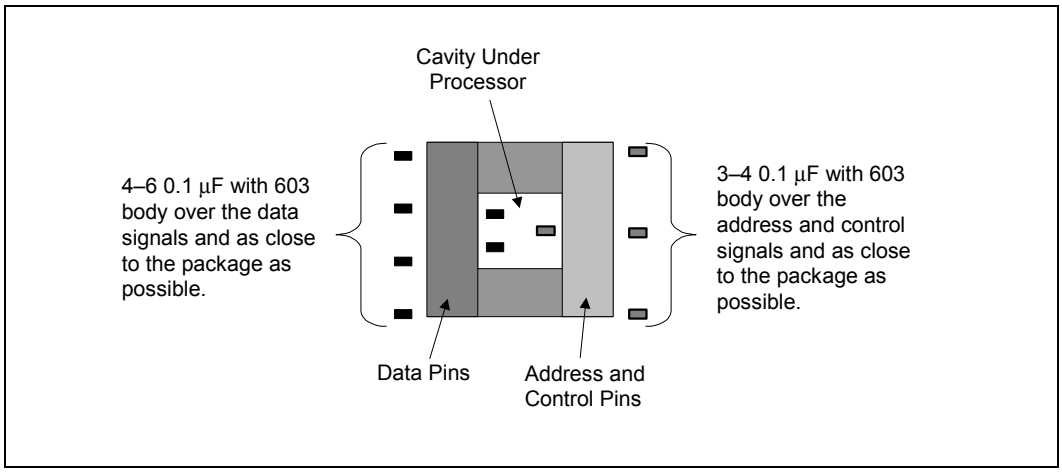
Figure 13-22. Filter Implementation 2—No Discrete Resistors



In addition, high-frequency decoupling may be required for signal integrity. System boards designed using striplines with VCC_CPU and VSS_CPU references should not require high-frequency decoupling beyond the recommended decoupling. For systems using microstrip configurations, a return path discontinuity will exist between the processor and the baseboard because the baseboard traces have only one reference plane. These systems should distribute decoupling capacitors as shown in Figure 13-23 and described as follows:

- Four minimum, six preferred 1 µF capacitors with 0805 packages distributed evenly over the data lines.
- Three minimum, four preferred 1 µF capacitors with 0805 packages distributed evenly over the address and control lines.
- All capacitors placed as close to the processor package as the keep-out zone allows.

Figure 13-23. Decoupling Example for a Microstrip Baseboard Design



13.11 Processor Over-Temperature Protection

To protect these processors from damage in over-temperature situations, power to the processor core must be removed within 0.5 seconds of the assertion of THERMTRIP#.

If power is applied to a processor when no thermal solution is attached, normal leakage currents will cause the die temperature to rapidly rise to levels at which permanent silicon damage is possible. This high temperature will cause THERMTRIP# to go active. Because this platform utilizes a shared processor power plane, all power supply sources to both processors must be disabled when either installed processor signals THERMTRIP#.

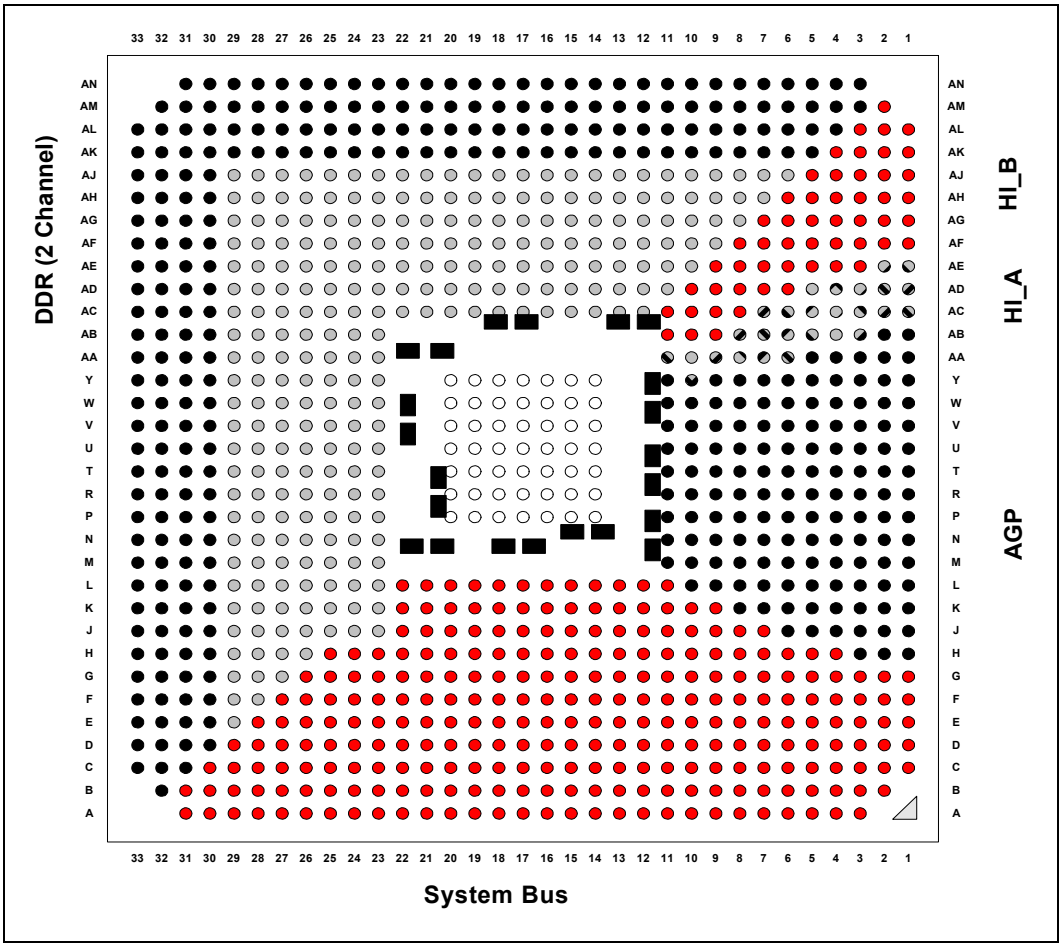
On this platform, the ICH4 integrates the THERMRTIP# circuitry. A low THERMTRIP# signal indicates that a thermal trip from the processor occurred, and the ICH4 will immediately transition to an S5 state. The ICH4 will not wait for the processor stop grant cycle because a processor has overheated.

13.12 MCH Power Delivery Guidelines

13.12.1 Decoupling Recommendations

The following guidelines are recommended for optimum MCH power delivery. The main focus of these guidelines is to minimize power noise and signal integrity problems to the E7505 chipset. The guidelines below are not intended to replace thorough system validation on E7505 chipset-based products.

Figure 13-24. Intel® MCH Decoupling (Backside View)



13.12.2 2.5 V Power Plane (DDR)

See Section 7.6.1.1 and Section 7.7.2.

13.12.3 1.25 V Power Plane (DDR_VTT)

See Section 7.7.3.

13.12.4 1.45 V Power Plane (VCC_CPU)

A maximum of five 0.1 µF capacitors are recommended (at least four (4) with 900 pH to 1.1 nH inductance must be placed under the MCH) for FSB 1.45 V power plane decoupling. Evenly distribute placement of decoupling capacitors among the FSB interface signal field. In addition to the minimum decoupling capacitors under the MCH, place a maximum of nine evenly-spaced capacitors for FSB (at least seven must be within 0.5 inch of the outer row of balls to the MCH).

13.12.5 1.5 V Power Plane (AGP)

Ten 0.1 µF high-frequency decoupling capacitors (package 0603) should be placed near the MCH to assist in the signal integrity areas of via stitching and return paths for the read condition of the AGP interface.

13.12.6 1.2 V / 1.3 V Power Plane (VCC_CORE)

There are no additional decoupling requirements for the 1.2V / 1.3 V power plane.

13.12.7 Filter Specifications

VCCAHI and VCCAFSB are required by the MCH's internal PLLs and DLLs. VCCAHI is created by using a low pass filter on VCC1_2, and VCCAFSB is created by using a low pass filter on VCC1_2. The MCH has internal analog PLL clock generators that require quiet power supplies for minimum jitter. Jitter degrades external I/O timings as well as internal core timings (i.e., maximum frequency). The filter topologies are shown in Figure 13-25 and Figure 13-26.

When designing the VCCAHI and VCCAFSB filters (Figure 13-25 and Figure 13-26), abide by the following guidelines:

- One Inductor 100 nH close to the edge of the package (within 1 inch form the die).
- One LF capacitor 100 µF or 150 µF close to the edge of the package.
- At least one Low ESL HF 0.1 µF capacitor on the backside of the motherboard under the die.

Figure 13-25. Intel® MCH Filter Topology for VCCAHI (HUB Interface)

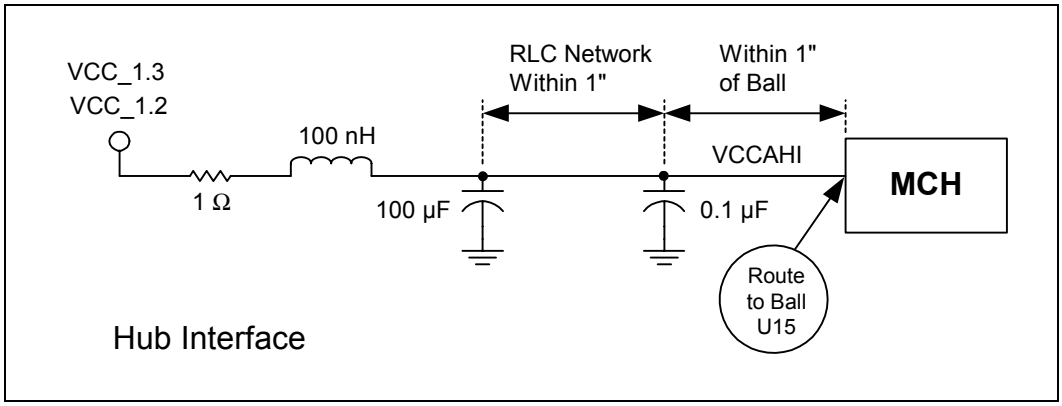
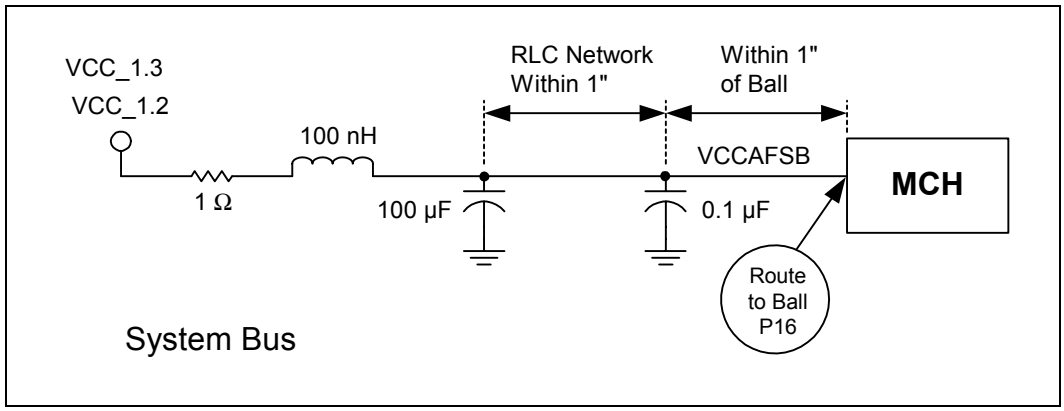


Figure 13-26. Intel® MCH Filter Topology for VCCAFSB (System Bus)



This page is intentionally left blank.

Mechanical Design Considerations 14

14.1 Retention Mechanism Placement and Keep-Outs

The retention mechanism (RM) for the processors requires two keep-out zones: one for the EMI ground pads, and another for a limited component height area under the RM, as shown in Figure 14-1. Figure 14-2 shows the relationship between the RM mounting holes and pin one of the socket. Figure 14-2 also shows the ground pads and keep-outs.

The EMI ground pads under the retention mechanism must have at least eight vias connecting the pad to the baseboard ground plane. The retention holes must be non-plated. It is not necessary to have a ground pad on the secondary side of the baseboard when using the push-pin fasteners. The push-pins protrude approximately 0.200 inch from the secondary side of the board.

The ground pads for the EMI ground frame must have at least six vias each connecting the pads to the ground plane. The suggested via size is 12 mils. This allows sufficient clearance to route traces between the vias on the secondary side of the PB or on internal layers.

Figure 14-1. Retention Mechanism Outline and Ground Pad Detail

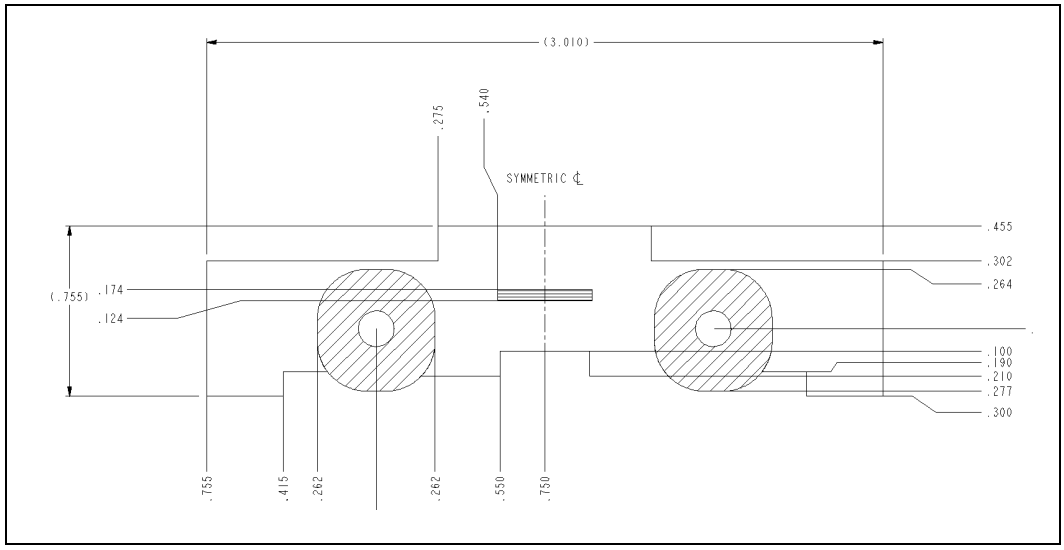
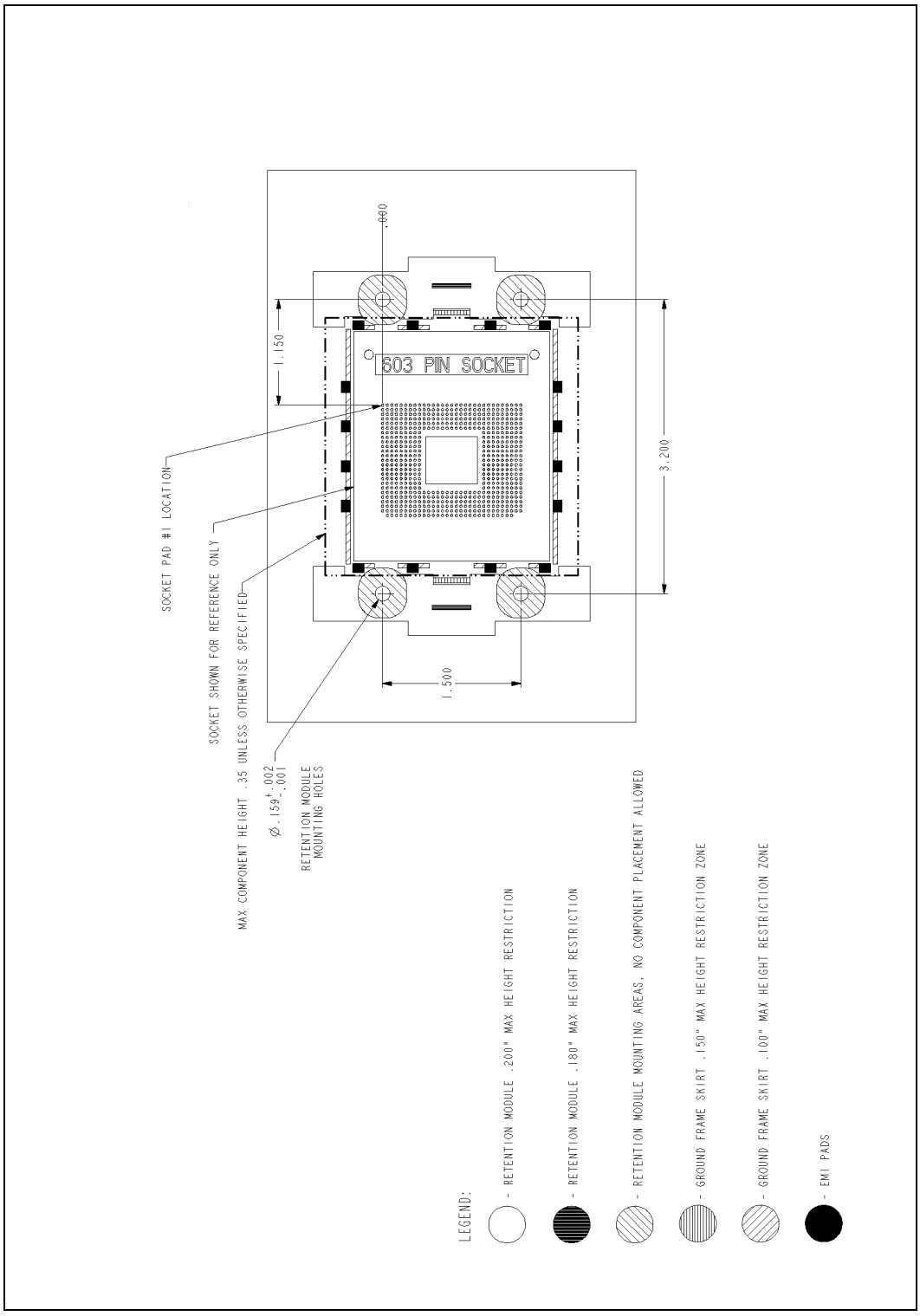


Figure 14-2. Retention Mechanism Placement and Keep-Out Overview

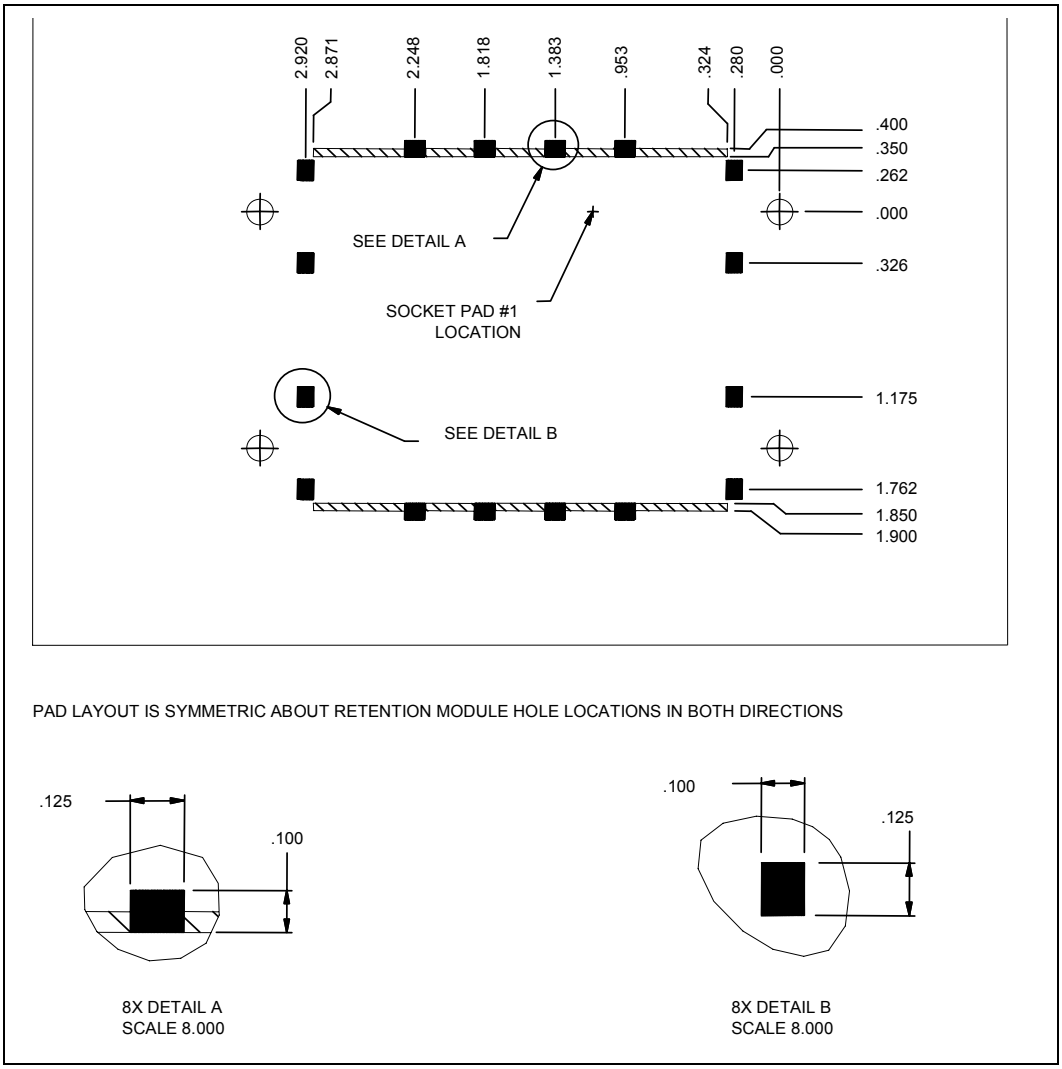


14.2 EMI Design Considerations

In an effort to be proactive regarding electromagnetic interference (EMI) reduction, Intel is enabling a reduction technique. The solution is comprised of a metal grounding frame that contacts the heatsink on all four sides and provides grounding to the motherboard. A second, optional solution is the DC grounding strips, which provide the heatsink a two point electrical connection to ground, and insert into the retention mechanism pieces.

The grounding frame for the processor is meant to provide grounding of AC currents seen on the heatsink, and has been shown to be the most effective design in EMI reduction for the processor. The metal frame is installed after the processor and retention mechanisms have been inserted. It fits around the processor and inside of the retention mechanisms. Fingers on the top of the metal frame provide contact to the heatsink, and fingers along the bottom contact the ground pads on the motherboard. The grounding frame requires the placement of a series of ground pads surrounding the processor, as shown in Figure 14-3.

Figure 14-3. EMI Ground Pad Size and Location

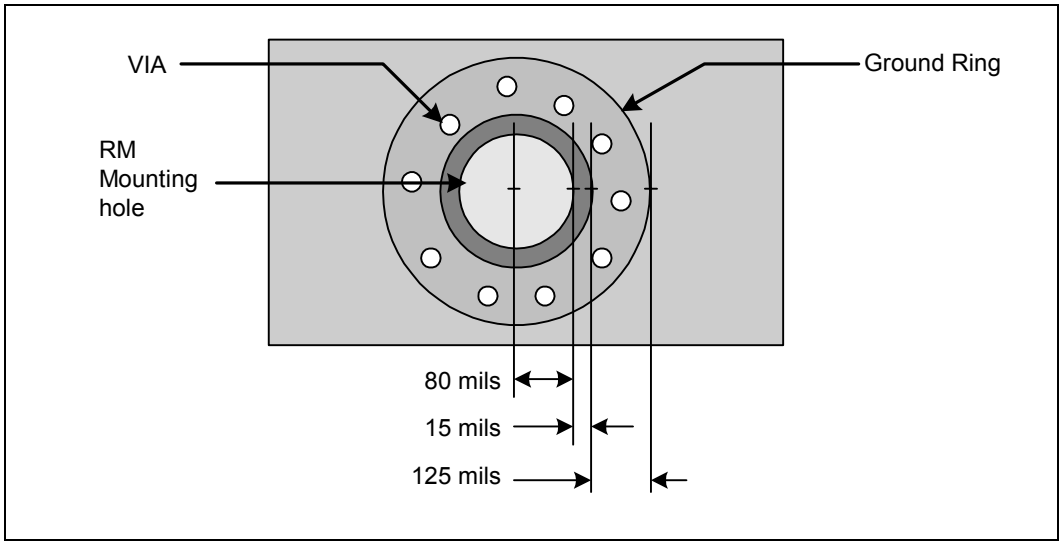


Utilization of the DC grounding strips requires ground pads around the mounting holes for the retention mechanism. Metal inserts are pre-assembled on the retention modules to establish DC contact between heatsink base plate and the motherboard ground. The inserts are grounded to the baseboard at mounting hole ground pads. Fingers on top of the insert connect to the base of the heatsink. The requirements for the DC grounding insert are as follows:

- All four RM mounting holes must have ground pad rings.
- Ground pad annular ring should be no less than 125-mil wide. Try to cover the entire keep-out zone, if possible. See the following illustration for better dimensions.
- Place 8–12 vias in the annular ring, which connects the pad to internal ground planes.
- Anodizing or any form of insulated coating of the heatsink is strongly discouraged.

Refer to Figure 14-4 for specific details regarding the required ground pads.

Figure 14-4. Retention Mechanism Ground Ring



Schematic Checklist 15

15.1 Processor Checklist

Note: For specific layout recommendations, refer to the appropriate section of this document.

Table 15-1. Processor Schematic Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Comments	√
A20M#, IGNNE#, LINT[1:0], SMI#, SLP#, STPCLK	• Connect to both processors and Intel® ICH4. Include 200 Ω ± 5% pull-up to VCC_CPU. Include 10 Ω ± 5% series resistor between processor middle agent and ICH4. See Section 5.3.3.	• Asynchronous GTL+ Input Signal	
A[35:3]#[1], REQ[4:0]#, ADSTB[1:0]#, D[63:0]#[2], DBI[3:0]#, DSTBN[3:0]#, DSTBP[3:0]#	• Connect to both processors and the MCH. Balance signal lengths within each strobe group.	• AGTL+ Source Synchronous I/O	
ADS#, AP[1:0], DBSY#, DP[3:0]#, DRDY#, HLOCK# (LOCK#), BPRI#, DEFER#, RS[2:0]#, RSP#, TRDY#	• Connect to both processors and the MCH.	• AGTL+ Common Clock I/O	
HCLKINP/ HCLKINN	• Connect to CK-408 clock driver. HCLKIN's to all processors should be length matched, and the HCLKIN to the MCH should be offset accordingly.	• All processor system bus agents must receive these signals to drive their outputs and latch their inputs. • System Bus Clock	
BINIT#, BNR#, HIT#, HITM#, MCERR#	• Connect to both processors and the MCH. • Wired-OR signal: Route as common clock signal.	• AGTL+ Common Clock I/O	
BPM[5:0]#	• For all ITP interface signal schematic, layout and routing recommendations, refer to the ITP700 Debug Port Design Guide.		

Table 15-1. Processor Schematic Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Comments	√
BREQ[3:0]#	• Connect BR0# to the MCH's BREQ0# pin, Processor 0's BR0# pin, and Processor 1's BR1# pin. Terminate using a 50 Ω pull-up resistor at Processor 0. • Connect BR1# signal to Processor 0's BR1# pin and Processor 1's BR0# pin. Terminate both ends of the bus using 50 Ω pull-up resistors. • BR[3:2]# should be terminated individually at each processor or be connected between processors and terminated at one end using a 50 Ω pull-up resistor. • Refer to Figure 5-2 for clarification.	• These signals do not have on-die processor termination and must be terminated on the motherboard. • BR0# is an AGTL+ Common Clock I/O. • BR[3:1]# are AGTL+ Common Clock Inputs.	
COMP[1:0]	• Terminate separately to ground using 49.9 Ω ± 1% resistors	• Sets the processor's on-die termination.	
FERR#	• Connect to FERR# on ICH4. • Pull-up with 56 Ω ± 5% at processor end agent, and 56 Ω ± 5% at ICH4 to VCC_CPU. See Section 5.3.1.	• Asynchronous GTL+ Output	
IERR#	• Pull-up with 56 Ω ± 5% at processor end agent, and 56 Ω ± 5% to VCC_CPU at other motherboard receiver logic such as a Baseboard Management Controller (BMC). See Section 5.3.1. • If IERR# is not supported, leave as no-connect.	• Asynchronous GTL+ Output	
INIT#	• Connect to both processors and ICH4. Include 200 Ω ± 5% pull-up to VCC_CPU. Include 10 Ω ± 5% series resistor between processor middle agent and ICH4. See Section 5.3.3 • Voltage translator circuit is required for interfacing with the FWH. Refer to Section 10.4	• Asynchronous GTL+ Input	
ODTEN	• Enable ODT (on-die termination) on Processor 0 (end processor) by pulling up to VCC_CPU with a resistor that falls within the range of 50 Ω ± 20%. Disable ODT for Processor 1 by pulling down to VSS with a resistor that that falls in the range of 50 Ω ± 20%.	• Enables processor on-die termination. • Input	
PROCHOT#	• Pull-up with 56 Ω ± 5% at processor end agent and other motherboard receiver logic such as a Baseboard Management Controller (BMC). See Section 5.3.1.	• Indicates that the processor Thermal Control Circuit has been activated. • Asynchronous GTL+ Output	
PWRGOOD (CPUPWRGOOD)	• Connect to both processors and ICH4. Include 300 Ω ± 5% pull-up to VCC_CPU. Include 10 Ω ± 5% series resistor between processor middle agent and ICH4. See Section 5.3.3.	• Asserted by ICH4 when all processor voltage supplies are stable.	
Reserved	• Reserved signals must remain as a No Connect (NC)		

Table 15-1. Processor Schematic Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Comments	√
RESET#	• Recommend 51 Ω ± 5% pull-up to VCC_CPU. Connect to MCH and both processors. Note that this signal is dual terminated at both ends of transmission line. • If using ITP, for signal connection to ITP, refer to the *ITP700 Debug Port Design Guide* for schematic, layout, and routing recommendations.	• AGTL+ Common Clock Input	
SKTOCC#	• SKTOCC# can be used to disable VRM or VRD output supply for unpopulated processors when processors are not installed.	• Output of this signal indicates whether a processor is installed or not; prevents powering up the voltage regulators for the CPUs.	
SM_ALERT#	• Should be connected to the SMBUS controller.	• SMBus I/O	
SM_CLK	• Connect to both processors and SMBus controller. Recommend a pull-up resistor to VCC3_3. Resistor value is based on the number of devices on the SMBus.	• SMBus Input	
SM_DAT	• Connect to both processors and SMBus controller. Recommend a pull-up resistor to VCC3_3. Resistor value is based on the number of devices on the SMBus.	• SMBus Input	
SM_EP_A[2:0]	• Leave as no connect to set bit low, or pull-up to SM_VCC through 100 Ω to set bit high. • Use these address bits to set a unique SMBus address for the memory devices on the processor. See the processor datasheet for more details.	• Set the SMBus address for the memory device on the processor. These signals must be set at power up with a unique address per bus. • These signals have 10 kΩ pull-downs on the processor. • SMBus Input	
SM_TS_A[1:0]	• Leave as no connect to set bit to high-impedance state. Pull-up to SM_VCC through 1 kΩ ± 5% to set bit high. Pull-down to VSS through 1 kΩ ± 5% to set bit low. Use these address bits to set a unique SMBus address for the thermal devices on the processor. See the processor datasheet for more details.	• These signals do not have internal pull-downs. Leaving the pins floating causes a high impedance state. • SMBus Input	
SM_WP	• Pull to VCC_SMBus with 100 Ω resistor to write-protect the processor's Scratch EEPROM. Leave as no connect (NC) to disable write-protecting of Scratch EEPROM.	• Pulling this signal to VCC_SMBus will enable write protection. on the processor scratchpad memory device. • SMBus Input	
STPCLK#	• Connect to both processors and ICH4. Include 200 Ω ± 5% pull-up to VCC_CPU. Include 10 Ω ± 5% series resistor between processor middle agent and ICH4. See Section 5.3.3.	• Causes processors to enter a low power Stop-grant state. • Asynchronous GTL+ Input	

Table 15-1. Processor Schematic Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Comments	√
TESTHI[6:0]	• **Option 1:** All TESTHI[6:0] pins may be individually pulled-up to VCC_CPU with resistors that fall within the range of 50 Ω ± 20%. • **Option 2:** TESTHI[3:0] and TESTHI[6:5] may all be tied together and pulled up to VCC_CPU with a single resistor that falls within the range of 50 Ω ± 20%. However, utilization of boundary scan test will not be functional if these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins.		
THERMDA1 THERMDC1	• Connect to the onboard thermal sensor. See Section 6.3.2 for details.	• Processor thermal diode anode and cathode signals	
THERMTRIP#	• Connect to THRMTRIP# on ICH4 • Pull-up with 56 Ω ± 5% at processor end agent, and 56 Ω ± 5% at ICH4 to VCC_CPU. See Section 5.3.1.	• Disables the VCC_CPU supply to the processors should it ever become asserted. • Asynchronous GTL+ Output	
VCCA	• Use discrete RLC filter to provide clean power. Refer to Section 13.10	• An isolated power for internal PLL	
VCCIOPLL	• Use discrete RLC filter to provide clean power. Refer to Section 13.10	• An isolated power for internal PLL	
VCC_SENSE	• Place via next to the processor socket's VCC_SENSE pin for measurement of VCC_CPU/VSS.	• Isolated low impedance connection to processor core VCC_CPU.	
VID[4:0]	• Should be routed individually from each processor to the voltage regulator supplying its VCC_CPU supply. Refer to the *VRM 9.1 DC-DC Converter Design Guidelines* or the *Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines* for voltage regulator details. • Compare VIDs from both processors using glue logic to disable VR/VRM if VIDs of both processors do not match.	• Processor drives these signals to indicate maximum core voltage allowed. SM_VCC must be correct and stable before the VRM should rely on these outputs. • Output	
VSSA	• Use discrete RLC filter to provide clean power. Refer to Section 13.10	• Isolated ground for internal PLLs	
VSS_SENSE	• Place via next to the processor socket's VSS_SENSE pin for measurement of VCC_CPU/VSS.	• An isolated low impedance connection to processor core VSS.	

NOTES:
1. A[35:3]# pins on the processor correspond to HA[35:3]# pins on the MCH
2. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the MCH

Table 15-2. Processor Bus Signals

Bus Signal	Agent 0 Pins	Agent 1 Pins
BREQ0#	BR0#	BR1#
BREQ1#	BR1#	BR0#

NOTE: BR2# and BR3# must not be used in 2-way platform designs.

15.2 MCH Checklist

Note: For specific layout recommendations, refer to the appropriate section of this document.

Table 15-3. MCH Schematic Checklist (Sheet 1 of 3)

Checklist Items	Recommendations	Comments	√
Host Interface			
ADS# AP[1:0] BNR# BPRI# BREQ0# DBSY# DEFER# HA[35:3]# HD[63:0]# HADSTB[1:0]# HDSTBP[3:0]# HDSTBN[3:0]# HIT# HITM# HLOCK# HREQ[4:0]# HTRDY# DP[3:0] DRDY# RS[2:0]# RSP# CPURST# XERR#	• See Processor section of this checklist		
DBI[3:0]#	• Connect to Processor DBI[3:0]#		
Hub Interface A			
HI_A[11:0]	• Maximum length of 20 inches (stripline routing)		
PSTRBF_0 PSTRBS_0	• Connect to Intel® ICH4 • Must **not** have pull-up, pull-down, or series resistors	• The length of each data signal must be matched within ± 0.1 of the associated HIA_STRBF / HIA_STRBS differential pair	
Hub Interface B			
HI_B[18:0] HI_B[21:20]	• Maximum length of 20 inches (stripline routing)		
PSTRBF_B PSTRBS_B PUSTRBF_B PUSTRBS_B	• Connect to Intel® P64H2 • Must **not** have pull-up, pull-down, or series resistors	• The length of each data signal must be matched within ± 0.1 of the associated HIB_STRBF / HIB_STRBS differential pair	

Table 15-3. MCH Schematic Checklist (Sheet 2 of 3)

Checklist Items	Recommendations	Comments	√
Clocks, Reset, Miscellaneous Signals			
HCLKINP HCLKINN	• Route to the CK408 with a 49.9 Ω pull-down resistor to ground.		
RSTIN#	• Connect to PCIRST# output of the ICH4		
PRCOMP_A	• Tie the COMP pin to a 24.9 Ω ± 1% pull-up to VCC1_2 • Tie the COMP pin to a 32.4 Ω ± 1% pull-up to VCC1_3	• Used to calibrate the I/O Buffers • Resistive compensation is used by the ICH4 and MCH to adjust the buffer characteristics to specific board characteristic. Same compensation must be used on both ICH4 and MCH side.	
Unused 16 bit interfaces	• All data and strobe signals can be left as no connect. • HIREF must be connected to the reference voltage divider circuit. • PSWNG must be connected to the reference voltage swing divider circuit.	• The MCH has integration detection logic that will detect unpopulated 16-bit interfaces without external pull-ups and pull-downs.	
PRCOMP_B	• Tie the COMP pin to a 24.9 Ω ±1% pull-up to VCC • Tie the COMP pin to a 32.4 Ω ± 1% pull-up to VCC1_3	• Used to calibrate the I/O Buffers • Resistive compensation is used by the P64H2 and MCH to adjust the buffer characteristics to specific board characteristics. Same compensation must be used on both P64H2 and MCH side.	
HYRCOMP HXRCOMP	• Tie the COMP pin to a 20 Ω ±1% pull-down resistor to ground.	• This signal is used to calibrate the Host AGTL+ I/O buffers characteristics to specific board characteristic	
PRCOMP_AGP0 PRCOMP_AGP1	• Tie the COMP pin to a 43.2 Ω ± 1% to 1.5 V	• Resistive compensation is used by the AGP to adjust the buffer characteristics to specific board characteristics.	

Table 15-3. MCH Schematic Checklist (Sheet 3 of 3)

Checklist Items	Recommendations	Comments	√
Voltage References - Power Planes			
HDVREF[3:0] HAVREF[1:0] HCCVREF	• Use one dedicated voltage divider for all these signals. Decouple the voltage divider with 1 µF capacitor	• To provide constant and clean power delivery to the data, address and common clock signals of the host AGTL+ interface.	
VREF_DDR	• Route from VR to DIMMs and MCH		
HIVREF[A:D]	• Hub reference voltage = 0.350 V ± 1% • R1 = 392 ± 1% Ω R2 = 499 ± 1% Ω R3 = 453 ± 1% Ω C1 = 0.1 µF C2 = 0.01 µF	• HIVREF should be generated locally with a voltage divider circuit. The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification.	
HXSWNG HYSWNG	• The host compensation reference voltage can be implemented using a simple voltage divider circuit. • R1 =150 ± 1% and R2 =301± 1% C1 = C2 = 0.01 µF	• The HSWNG inputs of MCH are used provide reference voltage for the compensation logic.	
HISWNG[A:D]	• Hub reference swing voltage = 0.800 V ±1% R6[1] = 80.6 ± 1% Ω or R6[2] = 226 ± 1% R5[1] = 51.1 ± 1% Ω or R5[2] = 147 ± 1% R4[1] = 40.2 ± 1% Ω or R4[2] = 113 ± 1% C1 = 0.1 µF C2 = 0.01 µF	• The MCH 16- bit hub interfaces use a compensation voltage to control the buffer voltage characteristics. If a multiple 16-bit hub interfaces are used, a HLSWNG divider circuit can be shared among the interfaces as long as the trace length from the divider circuit is less than 3.5”. **NOTE:** Use only resistors from group 1 or 2 (see 1 and 2 in previous column), do not mix values from these groups.	

15.3 Intel® ICH4 Checklist

Note: For specific layout recommendations, refer to the appropriate section of this document.

Table 15-4. Intel® ICH4 Schematic Checklist (Sheet 1 of 8)

Checklist Items	Recommendations	Comments	√
PCI Interface			
PERR#, SERR# (AGP 2.0), SERR (AGP 3.0), PLOCK#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, REQ[4:0]#, GPIO0/ REQA#, GPIO1/ REQB# / REQ5#	• These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3_3 or a 2.7 kΩ pull-up resistor to VCC5.	• See PCI 2.2 Component Specification for pull-up recommendations for VCC3_3 and VCC5.	
PCIRST#	• The PCIRST# signal should be buffered to form the IDERST# signal 33 Ω series resistor to IDE connectors.	• Improves Signal Integrity.	
PCIGNT[4:0]#	• No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented they must be pulled up to VCC3_3.	• These signals are actively driven by the Intel® ICH4.	
PME#	• No extra pull-up resistor .	• This signal has integrated pull-up of 18 kΩ to 42 kΩ.	
GNTA# /GPIO16, GNTB/ GNT5#/ GPIO17	• No extra pull-up needed.	• These signals have integrated pull-ups of 24 kΩ. • GNTA has an added strap function of “top block swap”. The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull-down resistor can be added to manually enable the function.	
IDSEL	• The series resistor on IDSEL should be 300 Ω to 900 Ω.	• See Figure 10-28.	
Hub Interface			
HICOMP	• Tie the HICOMP pin to a 43.3 Ω ± 1% (if trace impedance is 60 Ω) or 48.7 Ω ± 1% (if trace impedance is 56 Ω) or 43.2 Ω ± 1% (if trace impedance is 50 Ω) pull-up resistor (to VCC1_5).	• ZCOMP No longer supported.	
HI_VSWING	• 800 mV.	• See Section 8.2.2.	

Table 15-4. Intel® ICH4 Schematic Checklist (Sheet 2 of 8)

Checklist Items	Recommendations	Comments	√
LAN Interface			
LAN_CLK	• Connect to LAN_CLK on Platform LAN Connect Device.	• ICH4 contains integrated 100 kΩ nominal pull-down resistor on signal.	
LAN_RXD[2:0]	• Connect to LAN_RXD on Platform LAN Connect Device.	• ICH4 contains integrated 10 kΩ pull-up resistors on interface.	
LAN_TXD[2:0], LAN_RSTSYNC	• Connect to LAN_TXD on Platform LAN Connect Device.		
If the LAN connect interface is not used	• Platform LAN connect interface can be left NC if not used.	• Input buffers internally terminated.	
EEPROM Interface			
EE_DOUT	• Prototype Boards should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. Connect to EE_DIN of EEPROM.	• ICH4 contains integrated pull-up resistor for this signal • Connected to EEPROM data input signal (Input from EEPROM perspective and output from ICH4 perspective).	
EE_DIN	• No extra circuitry required. Connect to EE_DOUT of EEPROM.	• ICH4 contains integrated pull-up resistor for this signal • Connected to EEPROM data output signal (Output from EEPROM perspective and input from ICH4 perspective).	
FWH/LPC Interface			
FWH[3:0] / LAD[3:0], LDRQ[1:0]	• No extra pull-ups required. Connect straight to FWH/LPC.	• ICH4 Integrates 24 kΩ pull-up resistors on these signal lines.	
FWH Decoupling	• Follow vendor recommendation.		
Interrupt Interface			
PIRQ[D:A]#	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3_3.	• The PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15.	
PIRQ[H:E]#/ GPIO[5:2]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3_3.	• The PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15.	
APIC	• The APICCLK should be tied directly to GND. Pull APICD[1:0] to GND through a 10 kΩ pull-down resistor. If using XOR chain testing, a pull-down for each APIC signal is required (i.e., two 10 kΩ pull-down resistors).		
SERIRQ	• External weak (8.2 kΩ) pull-up resistor to VCC3_3 is recommended.	• Open drain signal.	

Table 15-4. Intel® ICH4 Schematic Checklist (Sheet 3 of 8)

Checklist Items	Recommendations	Comments	√
GPIO			
GPIO Pins	GPIO[7:0]: • These pins are in the main power well. Pull-ups must use the VCC3_3 plane. • Unused core well inputs must be pulled up to VCC3_3. • GPIO[1:0] can be used as REQ[B:A]# • GPIO1 can be used as PCI REQ5# • GPIO[5:2] can be used as PIRQ[H:E]# • GPIO6 • These signals are 5 V tolerant • These pins are inputs GPIO8 and [13:11]: • These pins are in the resume power well. Pull-ups must use the VccSus3_3 plane • Unused resume well inputs must be pulled up to VccSus3_3 • These signals **are not** 5 V tolerant • GPIO11 can be used as SMBALERT# • These pins are inputs GPIO[23:16]: • Fixed as output only. Can be left NC • GPIO22 is open drain • GPIO[17:16] can be used as GNT[B:A]# • GPIO17 can be used as PCI GNT5# • GPIO18 • GPIO19 • GPIO20 • GPIO21 • GPIO22 (open drain) • GPIO23 • These signals **are not** 5 V tolerant GPIO[28, 27, 25, 24]: • I/O pins. Default as outputs so can be left as NC • These pins are in the Resume Power Well • GPIO[28:27, 25] from resume power well. (Note: use pull-up to VccSus3_3 if these signals are pulled-up) • GPIO24 • These signals **are not** 5 V tolerant GPIO[43:32]: • I/O pins. From main power well. • Default as outputs • These signals **are not** 5 V tolerant	Ensure ALL unconnected signals are OUTPUTS ONLY!	

Table 15-4. Intel® ICH4 Schematic Checklist (Sheet 4 of 8)

Checklist Items	Recommendations	Comments	√
USB			
USBRBIAS	• 22.6 kΩ ± 1% connected to ground		
USBRBIAS#	• Connected to the same 22.6 kΩ ±1% resistor to ground as USBRBIAS		
USBP[5:0]P, USBP[5:0]N	• No external resistors required	• Output driver impedance of 45 Ω provided	
OC[5:0]	• If not used, use 10 kΩ to VccSus3_3	• Inputs must not float	
Unconnected USB data signals	• Unconnected USB data signals can be left as no-connects		
Power Management			
THRM#	• Connect to temperature Sensor. • Pull-up if not used (an 8.2 kΩ pull-up resistor to VCC3_3)	• Input to ICH4 cannot float. THRM# polarity bit defaults THRM# to active low, so pull-up	
THRMTRIP#	• See Section 5.3.1	• Input to ICH4 cannot float	
SLP_S3# SLP_S4# SLP_S5#	• No pull-up/down resistors needed. Signals driven by ICH4.	• Signals driven by ICH4	
PWROK	• Recommend a 10 kΩ pull-down to ground. • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCC3_3 and VCC1_5 have reached their nominal voltages	• Timing requirement	
PWRBTN#	• No extra pull-up resistors	• This signal has an integrated pull-up of 18 kΩ – 42 kΩ	
SYS_RESET#	• Recommend an 8.2 kΩ pull-up resistor to VccSus3_3. Also a (100 Ω to 8.2 kΩ) pull-down resistor isolated from SYS_RESET# by means of a normally open switch	• Input to ICH4 cannot float. This pin forces an internal reset to the ICH4 after the signal is internally debounced	
RI#	• RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to resume well	• If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.	
RSMRST#	• Recommend a 10 kΩ pull-down to ground. • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to LAN_RST#.	• Timing requirement	

Table 15-4. Intel® ICH4 Schematic Checklist (Sheet 5 of 8)

Checklist Items	Recommendations	Comments	√
LAN_RST#	• Recommend a 10 kΩ pull-down to ground. • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to RSMRST#	• Timing requirement	
Processor Signals			
A20M#, CPU_SLP#, IGNNE#, INTR, NMI, SMI#, STPCLK#	• Point-to-point connection. No external termination required at the ICH4. See Section 5.3.3 for processor guidelines.		
INIT#	• See Section 10.4.4		
FERR#	• Requires external pull-up resistor to V_CPU_IO. See Section 5.3.1 for processor guidelines.		
RCIN#, A20GATE	• pull-up signals to VCC3_3 through a 10 kΩ resistor	• Typically driven by open drain external micro-controller	
CPUPWRGD	• Connect to the processor's CPUPWRGD input. Requires external pull-up resistor. See Section 15.1 for processor guidelines.	• Refer to processor Documentation of the processor that platform utilizes for specific values. This signal represents a logical AND of the Intel ICH4's PWROK and VRMPWRGD signals	
System Management			
SMBDATA, SMBCLK	• Require external pull-up resistors. See Section 10.3.8.1 to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination. • Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. • Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK0 and SMBDATA should be tied to SMLINK1	• Value of pull-ups resistors determined by line load. Typical value used is 8.2 kΩ	
SMBALERT# / GPIO11	• See GPIO section if SMBALERT# not implemented.		

Table 15-4. Intel® ICH4 Schematic Checklist (Sheet 6 of 8)

Checklist Items	Recommendations	Comments	√
SMLINK[1:0]	• Requires external pull-up resistors. See Section 10.3.8.1 to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination) • Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections • Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK0 and SMBDATA should be tied to SMLINK1	• Value of pull-ups resistors determined by line load. Typical value used is 8.2 kΩ	
INTRUDER#	• Pull signal to VccRTC (VBAT) through ~10 kΩ	• Signal in VccRTC (VBAT) well	
RTC			
VBIAS	• The VBIAS pin of the ICH4 is connected to a 0.047 µF capacitor. See Figure 10-29	• For noise immunity on VBIAS signal	
RTCX1,RTCX2	• Connect a 32.768 kHz crystal oscillator across these pins with a 10 MΩ resistor. See Section 10.3.10.1 for capacitor guidelines.	• The external circuitry shown in Figure 10-29 will be required to maintain the accuracy of the RTC. • The circuitry is required because the new RTC oscillator is sensitive to step voltage changes in VccRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds	
RTCRST#	• Time constant due to RC filter on this line should be 18–25 ms. Recommended value for Resistor = 180 kΩ and capacitor is 0.1 µF	• Timing Requirement	
AC'97			
AC_SDOUT	• Requires a jumper to 8.2 kΩ pull-up resistor. Should not be stuffed for default operation. • Series termination resistor 0 Ω to 47 Ω on board codec.	• This pin has a weak internal 20 kΩ nominal pull-down. To properly detect a safe_mode condition a strong pull-up will be required to over-ride this internal pull-down.	
AC_SDIN1, AC_SDIN0	• Internal pull-downs in ICH4; no external pull-downs required • Series termination resistor 0 Ω to 47 Ω from the AC_SDIN lines to the ICH4	• These pins have a weak internal 20 kΩ nominal pull-down.	
AC_SDIN2	• Series termination resistor 33 Ω to 47 Ω from the AC_SDIN lines to the ICH4.	• This pin has a weak internal 20 kΩ nominal pull-down.	

Table 15-4. Intel® ICH4 Schematic Checklist (Sheet 7 of 8)

Checklist Items	Recommendations	Comments	√
AC_BITCLK	• No extra pull-down resistors required • Series termination resistor 33 Ω to 47 Ω from the motherboard codec to the ICH4	• This pin has a weak internal 20 kΩ nominal pull-down.	
AC_SYNC	• No extra pull-down resistors required	• Some implementations add termination for signal integrity. Platform specific.	
Miscellaneous Signals			
SPKR	• See Section 10.3.5.3	• Has integrated pull-down. The integrated pull-down is only enabled at boot/ reset for strapping functions; at all other times, the pull-down is disabled.	
TP0	• TP0 requires external pull-up resistor to VccSus3_3		
Power			
V_CPU_IO[2:0]	• The power pins should be connected to the proper power plane for the processor's CMOS compatibility signals. Use one 0.1µF decoupling capacitor.	Used to pull-up all processor interface signals	
VccRTC	• Use one 0.1 µF decoupling capacitor. • No clear CMOS jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safe mode strapping for clear CMOS.		
VCC3_3	• Use six 0.1µF decoupling capacitors		
VccSus3_3	• Use two 0.1µF decoupling capacitors		
VCC1_5	• Use two 0.1µF decoupling capacitors		
VccSus1_5	• Use two 0.1µF decoupling capacitors		
V5REF_Sus	• Use one 0.1µF decoupling capacitor • V5REF is the reference voltage for 5 V tolerant inputs in the ICH4. V5_REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. For most platforms this is not an issue because VccSus3_3 is usually derived from V5_REF_Sus.		
V5_REF	• Use one 0.1 µF decoupling capacitor. • V5REF is the reference voltage for 5 V tolerant inputs in the ICH4. V5_REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.		
VCCPLL	• Use one 0.1 µF decoupling capacitor and one 0.01 µF decoupling capacitor.		
VCCHI	• Use two 0.1 µF capacitors.		
HIREF	• 350 mV		

Table 15-4. Intel® ICH4 Schematic Checklist (Sheet 8 of 8)

Checklist Items	Recommendations	Comments	√
IDE Checklist			
PDD[15:0], SDD[15:0]	• No extra series termination resistors or other pull-ups/pull-downs are required. • PDD7/SDD7 does not require a 10 kΩ pull-down resistor • Refer to ATA ATPI-6 Specification	• These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.	
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	• No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	• These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.	
PDREQ, SDREQ	• No extra series termination resistors. • No pull-down resistors needed.	• These signals have integrated series resistors in the ICH4.	
PIORDY, SIORDY	• No extra series termination resistors. • Pull-up to VCC3_3 via a 4.7 kΩ resistor.	• These signals have integrated series resistors in the ICH4.	
IRQ14 IRQ15	• Recommend 8.2 kΩ – 10 kΩ pull-up resistors to VCC3_3. • No extra series termination resistors	• Open drain outputs from drive	
IDERST#	• The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal.		
Cable Detect	• Host Side/Device Side Detection (*recommended method*): • Connect IDE pin PDIAG#/CBLID to an ICH4 GPIO pin. Connect a 10 kΩ resistor to GND on the signal line. • Device Side Detection: • Connect a 0.047 µF capacitor from IDE pin PDIAG#/CBLID to GND. No ICH4 connection.	• The 10 kΩ resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. **NOTE:** All Ultra DMA drives supporting modes greater than Mode 2 will have the capability to detect cables	

15.4 Hub Interface Checklist

Table 15-5. Hub Interface Checklist

Checklist Items	Recommendations	Comments	√
MCH / Intel® ICH4 Signals			
HI[11:0]	• Connect together		
HI_STB	• Connect together		
HI_STB#	• Connect together		
HI_REF	• Connect voltage divider circuit with R1=R2=150 Ω ± 1% • Use two 0.1 µF capacitors within 150 mils of the ICH4. The MCH should be decoupled with one 0.1 µF capacitor within 150 mils of the package and one 10 µF capacitor nearby. • Bypass to GND through a 0.1 µF capacitor located near each component's (MCH and ICH4) HIREF pin • Decouple with a 0.1 µF capacitor placed near the divider circuit.		
VCC1_8	• Connect to 1.8 V power supply.		
MCH Signals Only			
HLRCOMP	• Pull-up to VCC1_8 through a 40.2 Ω ±1% resistor.		
ICH4 Signals Only			
HICOMP	• Terminate to VCC1_8 through a 40.2 Ω ± 1% resistor ZCOMP is no longer supported.		

15.5 DDR SDRAM Checklist

15.5.1 Unbuffered DDR Checklist

Table 15-6. Unbuffered DDR Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Comments	√
MCH / DIMM Signals			
DQ_x[63:0] CB_x[7:0] DQS_x[8:0]	• Connect from MCH to first and second DIMM in channel, then terminate to DDR_VTERM (1.25 V) through a 39 Ω resistor. Resistor packs can be used, but don't use address/command or control signals on the same RPACK as these signals.	ChA	
		ChB	
DQS_x[17:9]	• These signals are left floating at the MCH. Ground them at the DIMM.	ChA	
		ChB	
MA_x[13:0] BA_x[1:0] RAS_x# CAS_x# WE_x#	• Connect from MCH to first and second DIMM in channel, then terminate to DDR_VTERM (1.25 V) through a 56 Ω resistor. Resistor packs can be used, but do not use data/strobe or control signals on the same RPACK as these signals.	ChA	
		ChB	
CS_x[3:0]# CKE_x[3:0]	• Connect to a single DIMM, then terminate to DDR_VTERM (1.25 V) through a 56 Ω resistor. Refer to Table 7-2 for correct DIMM pin mapping. Resistor packs can be used, but don't use data/strobe or address/command signals on the same RPACK as these signals.	ChA	
		ChB	
CMDCLK_x[7:4,1:0] CMDCLK_x[7:4,1:0]#	• Route each signal and its complement differentially to the DIMM. Signal does not route to termination. Refer to Table 7-4 for correct DIMM pin mapping.	ChA	
		ChB	
VREF	• Connect to a resistor divider, 49.9 Ω to both 2.5 V and GND near the MCH, and add a 1 µF decoupling capacitor from VREF to ground near the divider. Connect to the VREF pin on each DIMM in the channel. Decouple each DIMM with a 0.1 µF capacitor. Decouple with a 0.1 µF capacitor near the MCH. See Section 7.7.4 for details.	ChA	
		ChB	
MCH Signals Only			
CMDCLK_x[3:2] CMDCLK_x[3:2]#	• These signals are left floating at the MCH	ChA	
		ChB	
RCVENOUT_x#	• Connect to a resistor divider, 78.7 Ω to both 2.5 V and ground.	ChA	
		ChB	
DRCOMPVREF_HDR COMPVREF_V	• Connect these signals together and to a resistor divider, 49.9 Ω to both 2.5 V and ground, decoupled with a 1 nF capacitor from DRCOMPVREF to ground.		
DRCOMP_H DRCOMP_V	• Connect to ground through a 24.9 Ω resistor for VCC1_2 • .Connect to ground through a 32.4 Ω resistor for VCC1_3		
DDR_STRAP	• Connect directly to 2.5 V.		
ODTCOMP	• Connect to ground through a 402 Ω resistor.		
VCCDDR	• Connect to 2.5 V.		

Table 15-6. Unbuffered DDR Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Comments	√
DIMM Signals Only			
FETEN VDDID	• No Connect.		
SDA	• Connect to SMBus Data.		
SCL	• Connect to SMBus Clock.		
VDD VDDQ	• Connect to 2.5 V.		
VSS	• Connect to ground.		
VDDSPD	• Connect to power (from a minimum of 2.3 V to a maximum of 3.6 V Strongly recommended connecting to 3.3 V.		
Decoupling Capacitors			
MCH High-Frequency Decoupling	• Place ten 0603 0.1 µF MLC capacitors near the MCH. Connect from 2.5 V to ground.		
MCH Bulk Decoupling	• Place four 100 µF capacitors between the MCH and the first DIMM. Connect from 2.5 V to ground.		
DIMM Decoupling	• Place two 100 µF capacitors per DIMM, one each on either side of the DIMM socket. Connect from 2.5 V to ground.		
VTT Decoupling	• Place one 0.1 µF capacitor for every two termination resistors (or 2 capacitors/RPACK). Place six 4.7 µF capacitors around the termination island, three on either side. Connect from 1.25 V to ground. See Figure 7-45.		

15.5.2 Registered DDR Checklist

Table 15-7. Registered DDR Checklist

Checklist Items	Recommendations	Comments	√
MCH / DIMM Signals			
DQ_x[63:0] CB_x[7:0] DQS_x[17:0]	• Connect from MCH to series resistor, 4.7 Ω (min) to 10 Ω (max) value. Connect to first, second, and third DIMM in channel, then terminate to DDR_VTERM (1.25 V) through a 33 Ω (min) to 39 Ω (max) resistor. Resistor packs can be used, but do not use address/command or control signals on the same RPACK as these signals.	ChA	
		ChB	
MA_x[13:0] BA_x[1:0] RAS_x# CAS_x# WE_x# CKE_x[1:0]	• Connect from MCH to first, second, and third DIMM in channel, then terminate to DDR_VTERM (1.25 V) through a 39 Ω (min) to 47 Ω (max) resistor. Resistor packs can be used, but do not use data/strobe or control signals on the same RPACK as these signals.	ChA	
		ChB	
CS_x[5:0]#	• Connect to a single DIMM, then terminate to DDR_VTERM (1.25 V) through a 39 Ω (min) to 47 Ω (max) resistor. Refer to Table 7-14 for correct DIMM pin mapping. Resistor packs can be used, but do not use data/strobe or address/command signals on the same RPACK as these signals.	ChA	
		ChB	
CMDCLK_x[2:0] CMDCLK_x[2:0]#	• Route each signal and its complement differentially to the DIMM. Signal does not route to termination. Refer to Table 7-19 for correct DIMM pin mapping.	ChA	
		ChB	
VREF	• Connect to a resistor divider, 49.9 Ω to both 2.5 V and GND near the MCH, and add a 1 µF decoupling capacitor from VREF to ground near the divider. Connect to the VREF pin on each DIMM in the channel. Decouple each DIMM with a 0.1 µF capacitor. Decouple with a 0.1 µF capacitor near the MCH. See Section 7.7.4 for details.	ChA	
		ChB	
MCH Signals Only			
CMDCLK_x[5:3] CMDCLK_x[5:3]# CKE_x[3:2]	• These signals are left floating at the MCH	ChA	
		ChB	
RCVENOUT_x#	• Connect to a resistor divider, 78.7 Ω to both 2.5 V and ground	ChA	
		ChB	
DRCOMPVREF_H DRCOMPVREF_V	• Connect these signals together and to a resistor divider, 49.9 Ω to both 2.5 V and ground, decoupled with a 1 nF capacitor from DRCOMPVREF to ground.		
DRCOMP_H DRCOMP_V	• Connect to ground through a 24.9 Ω resistor.		
DDR_STRAP	• Connect directly to GND.		
ODTCOMP	• Connect to ground through a 402 Ω resistor.		
VCCDDR	• Connect to 2.5 V.		

Table 15-7. Registered DDR Checklist

Checklist Items	Recommendations	Comments	√
DIMM Signals Only			
FETEN VDDID	• No Connect.		
SDA	• Connect to SMBus Data.		
SCL	• Connect to SMBus Clock.		
VDD VDDQ	• Connect to 2.5 V.		
VSS	• Connect to ground.		
VDDSPD	• Connect to power (from a minimum of 2.3 V to a maximum of 3.6 V). Strongly recommended connecting to 3.3 V.		
Decoupling Capacitors			
MCH High-Frequency Decoupling	• Place ten 0603 0.1 µF MLC capacitors near the MCH. Connect from 2.5 V to ground.		
MCH Bulk Decoupling	• Place four 100 µF capacitors between the MCH and the first DIMM. Connect from 2.5 V to ground		
DIMM Decoupling	• Place two 100 µF capacitors per DIMM, one each on either side of the DIMM socket. Connect from 2.5 V to ground.		
VTT Decoupling	• Place one 0.1 µF capacitor for every two termination resistors (or 2 capacitors/RPACK). Place six 4.7 µF capacitors around the termination island, three on either side. Connect from 1.25 V to ground. See Figure 7-45.		

15.6 AGP Interface Checklist

Table 15-8. AGP Interface Checklist (Sheet 1 of 2)

Checklist Items[1]	Recommendations	Comments	√
MCH / Connector Signals			
AD_STB[1:0] (AGP 2.0)/ AD_STBF[1:0] (AGP 3.0)	• No external termination required		
AD_STB[1:0]#/ AD_STBS[1:0]			
DBI_LO (AGP 3.0)			
GAD[31:0]			
GC/BE[3:0]# (AGP 2.0)/ GC#/BE[3:0] (AGP 3.0)			
GC_DET#	• See Figure 9-1		
GDEVSEL# (AGP 2.0)/ GDEVSEL (AGP 3.0)	• No external termination required		
GFRAME# (AGP 2.0)/ GFRAME (AGP 3.0)			
GGNT# (AGP 2.0)/ GGNT (AGP 3.0)			
GIRDY# (AGP 2.0)/ GIRDY (AGP 3.0)			
GPAR			
GREQ# (AGP 2.0)/ GREQ (AGP 3.0)			
GSTOP# (AGP 2.0)/ GSTOP (AGP 3.0)			
GTRDY# (AGP 2.0)/ GTRDY (AGP 3.0)			
MB_DET#	• Terminate to GND		
PIPE#/DBI_HI	No external termination required		
RBF#/RBF			
SBA[7:0] (AGP 2.0)/ SBA[7:0]# (AGP 3.0)			
SB_STB (AGP 2.0)/ SB_STBF (AGP 3.0)			
SB_STB# (AGP 2.0)/ SB_STBS (AGP 3.0)			
ST0			
ST1			
ST2			
WBF# (AGP 2.0) / WBF (AGP 3.0)			
VCC1_5	Connect to 1.5 V power supply		

Table 15-8. AGP Interface Checklist (Sheet 2 of 2)

Checklist Items[1]	Recommendations	Comments	√
Connector Signals Only			
3.3Vaux	• Connect to PCI 3.3VAUX		
12V	• Connect to 12 V		
AGPCLK	• Connect to CK408		
INTA#	• See recommendations for PIRQ[D:A]# signals in the ICH4 Section of this document		
INTB#	• See recommendations for PIRQ[D:A]# signals in the ICH4 Section of this document		
PERR	• Refer to Section 9.1.3.1		
SERR# (AGP 2.0) SERR (AGP 3.0)	• No external termination required		
OVRCNT	• Not required		
PCIRST	• Connect to PCI slot PCIRST		
PME#	• Connect to PCI PME#		
TYPEDET#	• Refer to Section 9.1.3.2		
USB+	• Not required		
USB-	• Not required		
VCC	• Connect to VCC3_3		
VCC5	• Connect to VCC		
VDDQ	• Connect to V1.5CORE		
VREFCG	• Connect to VREF divider network at the AGP connector		
MCH Signals Only			
AGPREF	• Connect to VREFCG pin on connector Terminate to ground through a 0.1 µF capacitor at the MCH		
GRCOMP	• Pull to VCC_AGP through a 43 Ω ± 1% resistor		

NOTE:
1. Checklist items may have differing names depending on the AGP signaling mode being used. In these cases, the differing names are separated by a slash with AGP2.0 signal names listed first, followed by AGP3.0 signal names.

15.7 CK 408 Clock Interface Checklist

Table 15-9. CK 408 Clock Interface Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Comments	√
66BUFF0	• Connect to MCH. • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
66BUFF1	• Connect to Intel® ICH4. • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
66BUFF2	• Connect to AGP. • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
66IN	• No Connect		
CPU[1:0]	• Connect to processor. • Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor.		
CPU[1:0]#	• Connect to processor. • Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor.		
CPU2 CPU2#	• Connect to MCH. • Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor.		
CPU_STOP#	• Terminate to VCC3_3 through a 1 kΩ ± 1% resistor.		
DOT48MHz	• No Connect.		
IREF	• Terminate to GND through a 475 Ω ± 1% resistor.		
MULT0	• Connected from the VCC3_3 through a series 10 kΩ ± 5% resistor and terminate to GND through a parallel 1 kΩ ± 1% resistor.		
PCI[6:0]	• Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
PCIF[2:0]	• Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
PCI_STOP#	• Terminate to VCC3_3 through a 1 kΩ ± 1% resistor.		
PWRDWN#	• Terminate to VCC3_3 through a 1 kΩ ± 1% resistor.		
REF0	• Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
S[1:0]	• Terminate to VCC3_CLK through a 1 kΩ ± 5% resistor.		
S2	• Terminate to GND through a 1 kΩ ± 5% resistor.		
SCLK	• Connect to DIMMs.		
SDATA	• Connect to DIMMs.		
USB48MHz	• Connect to ICH4. • Terminate to GND through a 33 Ω ± 5% resistor and a 10 pF ± 5% capacitor.		
VDD	• Terminate to VCC3_CLK.		

Table 15-9. CK 408 Clock Interface Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Comments	√
VDD48MHz	• Terminate to VCC3_CLK.		
VDDA	• Terminate to GND through a 0.1 µF ± 5% capacitor.		
VSS	• Terminate to GND.		
VSSA	• Terminate to GND.		
VSS48MHz	• Terminate to GND.		
VSSIREF	• Terminate to GND.		
VTT_PWRGD#	• Connect to an inverted copy of VCC_CPU. Refer to the respective section of the design guide for more details.		
XTAL_IN	• Terminate to GND through a 10 pF ± 5% capacitor.		
XTAL_OUT	• Terminate to GND through a 10 pF ± 5% capacitor.		

15.8 SSI Checklist

Table 15-10. SSI Schematic Checklist

Checklist Items	Recommendations	Comment	√
Main Power Connector	• Use a 24 pin Molex 44472 family connector or equivalent. • Refer to Table 4-2 for pinout.	• *SSI EEB Specification*, Section 5.3.1.2	
+12 Volt Power Connector	• Use an 8 pin Molex 44472 family connector or equivalent. • Refer to Table 4-3 for pinout.	• *SSI EEB Specification*, Section 5.3.1.3	
Auxiliary Connector	• Use a 5 pin Molex 70545 family connector or equivalent. • Refer to Table 4-4 for pinout.	• *SSI EEB Specification*, Section 5.3.1.4	
Cooling Fan Connector	• Use a 3 pin AMP 644953-3 connector or equivalent. • Refer to Table 4-5 for pinout.	• *SSI EEB Specification*, Section 5.3.4	

15.9 Intel® P64H2 Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements P64H2 product. The items contained within this checklist attempt to address important connections to these devices and any critical supporting circuitry. This is not a complete list and does not guarantee that a design will function properly.

Table 15-11. Hub Interface

Signals	Recommendations	Comments	√
CLK200 CLK200#	• If not used, 8.2 kΩ pull-up resistor to VCC3_3.		
HI_RCOMP	• For a 50 Ω ± 10% board, RCOMP = 61.9 Ω ±1%. Connect to VCC1_8. The trace length between the Intel® P64H2 pin and the resistor lead should be < 1 inch.		
HI_VREF	• 0.350 V ± 2%. It is recommended that this be generated on the motherboard through a voltage divider.	• Refer to Section 8.1.1 for circuit implementation.	
HI_VSWING	• 0.800 V pp ±2%. It is recommended that this be generated on the motherboard through a voltage divider.	• Refer to Section 8.1.1 for circuit implementation.	
HI19	• HI19 can be left as no connect if parity is not going to be used.		
BPCLK100 BPCLK133	• These can be left as no connects.	• These clock signals are used for testing modes.	

Table 15-12. PCI/PCI-X Interface

Signals	Recommendations	Comments	√
PxAD[63:32] PxC/BE[7:4]# PxDEVSEL# PxFRAME# PxIRDY# PxTRDY# PxSTOP# PxPERR# PxSERR# PxREQ[5:0]# PxPLOCK# PxPAR64 PxACK64# PxREQ64#	• 8.2 kΩ pull-up resistor to VCC3_3.	• See PCI Specification, Revision 2.2.	
GNTA# /GPIO16, GNTB/ GNT5#/ GPIO17	• No extra pull-up needed.	• These signals have integrated pull-ups of 24 kΩ	
PAGNT3#	• If not using CLK200, CLK200# clocks, connect to ground through an 8.2 kΩ pull-down resistor.	• 1 = Use CLK66 • 0 = Use CLK200/ CLK200#	

Table 15-12. PCI/PCI-X Interface

Signals	Recommendations	Comments	√
PBGNT3#	• Connect to ground through an 8.2 kΩ pull-down resistor.	• 1 = Disable Hub Interface RCOMP • 0 = Enable Hub Interface RCOMP	
PCIXCAP	• Connect to 3.3 V through a 10 kΩ pull-up.	• See PCI-X Specification 1.0 recommendations for PCIXCAP connection.	
PA_133EN	• Enable PCI-X at 133 MHz for PCI Bus A: This pin, when high, allows the PCI-X segment to run at 133 MHz when PA_PCIXCAP is sampled high. When low, the PCI-X segment will only run at 100 MHz when PA_PCIXCAP is sampled high. • For 133 MHz (max) PCI-X capable slot, use 8.2 kΩ pull-up resistor to VCC3_3. • For 100 MHz (max) PCI-X capable slot, use 8.2 kΩ pull-down resistor to ground.	• Only active if PA_PCIXCAP pin is high.	
PB_133EN	• Enable PCI-X at 133 MHz for PCI Bus B: This pin, when high, allows the PCI-X segment to run at 133 MHz when PB_PCIXCAP is sampled high. When low, the PCI-X segment will only run at 100 MHz when PB_PCIXCAP is sampled high. • For 133 MHz (max) PCI-X capable slot, use 8.2 kΩ pull-up resistor to VCC3_3. • For 100 MHz (max) PCI-X capable slot, use 8.2 kΩ pull-down resistor to ground.	• Only active if PB_PCIXCAP pin is high.	
3.3Vaux	• Leave this as unconnected on the PCI slots	• The P64H2 does not support PCI bus power management.	
IDSEL	• The series resistor on IDSEL should be 100 Ω.	• This has changed from the PCI-X 1.0 Specification. There is reflected in a Spec change to PCI-X 1.0 which allows for values other than the original 2 kΩ value.	

Table 15-13. Interrupt Interface

Signals	Recommendations	Comments	√
PAIRQ[15:0] PBIRQ[15:0]	• Unused PxIRQ lines should be terminated using an approximately 8.2 kΩ pull-up resistor to VCC3_3.		
APICCLK	• If APIC is not used, terminate using an (approximately) 8.2 kΩ pull-up resistor to VCC3_3.		
APICD[1:0]	• If APIC is not used, terminate using an (approximately) 8.2 kΩ pull-up resistor to VCC3_3.		

Table 15-14. Hot Plug Disabled

Signals	Recommendations	Comments	√
HPxSLOT[2:0]	• If disabling hot plug mode, connect these signals to ground through an 8.2 kΩ resistor.	• HPxSLOT[2:0] signals should be strapped to zero to disable hot plug mode.	
HPx_SID	• Connect to ground through an 8.2 kΩ resistor.	• Unused inputs should not float.	
HPx_SIC HPx_SIL# HPx_SOR# HPx_SORR# HPx_SOC HPx_SOL HPx_SOLR HPx_SOD	• If disabling hot plug mode, these signals can be left as no connect.		
PCIXCAP	• Connect to 3.3 V through a 10 kΩ pull-up.		

Table 15-15. Miscellaneous Signals

Signal	Recommendations	Comments	√
TP0	• 8.2 kΩ pull-up resistor to VCC3_3.		
RSTIN#	• Connect to the PCIRST# output of the Intel® ICH4.	• Reset In: When asserted this signal asynchronously resets the Intel® P64H2 logic and asserts PCIRST# active output from each PCI interface.	
TEST#	• 8.2 kΩ pull-up resistor to VCC3_3.	• Intel test mode.	
RASERR#	• 8.2 kΩ pull-up resistor to VCC3_3.		

Table 15-16. Power

Signal	Recommendations	Comments	√
VCC	• Connect to 1.8 V Power Supply. • Decoupling: 8 X 0.1 µF capacitors near Intel® P64H2 2 X 4 µF capacitors (near regulator)	• 1.8 V Core Voltage.	
VCC1_8	• Connect to 1.8 V Power Supply. • Decoupling: 2 X 1.0 µF capacitors near P64H2 1 X 100 µF capacitor (near regulator)	• 1.8 V Hub Interface Voltage.	
VCC3_3	• Connect to 3.3 V Power Supply. • Decoupling: 20 X 0.1 µF capacitors near P64H2 6 X 1.0 µF capacitors near P64H2 2 X 4 µF capacitors (near regulator) 1 X 100 µF capacitor (near regulator)	• 3.3 V	
VCC5REF	• Connect to 5 V Power Supply.	• 5 V	

This page is intentionally left blank.

Layout Checklist 16

16.1 Processor Checklist

Table 16-1. Processor Layout Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Comments	√
A20M# IGNNE# INIT# LINT0/INTR LINT1/NMI SMI# SLP# STPCLK#	• Trace impedance = 50 Ω ± 10%. • Route traces using 5/10 mil spacing. • Try to keep signals on the same layer for the whole bus, but not at expense of AGTL+ Source Synchronous I/O. • Maximum agent to agent length is 10". Place pull-up resistor within 3" of Processor 1.	• Asynchronous GTL+ Input Signals. • Refer to Section 5.3.3.	
A[35:3]#[1] ADSTB[1:0]#[2] DSTBN[3:0]#[3] DSTBP[3:0]#[4] DBI3:0]# D[63:0]#[5] REQ[4:0]#[6]	• Trace impedance = 50 Ω ± 10%. • Route Strobes 5/25 and others 5/15. • Route all signals as groups, on the same layer (do not change layer), and balance within group ± 25 mils with respect to the strobe. • The distance from processor pin to processor pin is between 3.0" and 7.0". • The distance from processor pin to MCH pin is between 3.0" and 6.5". • Do not route a stub to Processor 1.	• AGTL+ Source Synchronous I/O. • Refer to Section 5.1.	
ADS# AP[1:0] BINIT# BNR# BR0# DBSY# DP[3:0]# DRDY# HIT# HITM# LOCK# MCERR# BPRI# BR[3:0]# DEFER# RESET#[7] RS[2:0]# RSP# TRDY#[8]	• Trace impedance = 50 Ω ± 10%. • Route traces using 5/15 mil spacing. • May change layers throughout the bus. • Route traces with at least 50% of the trace width directly over a reference plane. • The distance from processor pin to processor pin is between 3.0" and 7.0". • The distance from processor pin to MCH pin is between 3.0" and 6.5". • Do not route a stub to Processor 1. • Total bus length must not exceed 13.5".	• AGTL+ Common Clock Signals. • Refer to Section 5.2.	
BCLK[1:0]	• BCLKs to all processors should be length matched, and the BCLK to the MCH should be offset accordingly. See Table 3-3.	• System Bus Clock. • Refer to Section 3.1.	

Table 16-1. Processor Layout Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Comments	√
BPM[5:0]#		• For all ITP interface signal schematic, layout and routing recommendations, refer to the *ITP700 Debug Port Design Guide*.	
FERR#/PBE# IERR# PROCHOT# THERMTRIP#	• Connect to both processors and Intel® ICH4. • Trace impedance = 50 Ω ± 10%. • Route traces using 5/15 mil spacing. • Try to keep signals on the same layer for the whole bus, but not at expense of AGTL+ Source Synchronous I/O. • Maximum agent to agent length is 10". Place pull-up resistor within 3" of Processor 1 and ICH4.	• Async GLT+ Output. • Refer to Section 5.3.1.	
COMP[1:0] ODTEN SKTOCC# TESTHI[6:0] VID[4:0]	• There are no routing requirements for these signals.	• Input. • Refer to Section 5.3.4 through Section 5.3.8.	
Reserved	• Reserved signals must remain as a No Connect (NC).		
VCCA	• To satisfy damping requirements, total series resistance in the filter (from VCC_CPU to the top plate of the capacitor) must be at least 0.35 Ω. It includes the minimum DCR of the inductor, and any resistance (routing or discrete components) between VCC_CPU and capacitor top plate. • The total maximum resistance cannot be greater than 1.1 Ω as measured from VCC (more specifically, the baseboard via that connects the PLL filter to the VCC plane) to the processor VCCA interposer pin. Also, maximum trace resistance from the filter capacitor to processor socket pin should be less than 0.02 Ω.	• An isolated power for internal PLL. • Refer to Section 13.10.	
VSSA VCCIOPLL	• There are no routing requirements for these signals.	• Refer to Section 13.10	
VCC_SENSE VSS_SENSE	• Route traces using 5/15 mil spacing. • Place via next to the processor socket's pin for measurement of VCC_CPU/VSS.	• Refer to Section 13.4.1.	

NOTES:
1. A[35:3]# pins on the processor correspond to HA[35:3]# pins on the MCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the MCH.
3. DSTBN[3:0]# pins on the processor correspond to HADSTBN[3:0]# pins on the MCH.
4. DSTBP[3:0]# pins on the processor correspond to HADSTBP[3:0]# pins on the MCH.
5. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the MCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the MCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the MCH.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the MCH.

16.2 Processor Power Delivery Layout Checklist

All recommendations in this checklist apply to the power distribution design of the processor's "VCC_CPU" and ground supply. This checklist assumes the voltage regulator solution adheres to the guidelines documented in either the *VRM 9.1 DC-DC Converter Design Guidelines* or *Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines* depending on which solution is implemented.

Table 16-2. Processor Power Delivery Layout Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Comments	√
Power / Ground Plane Copper Weight	• Use at least 2 oz total copper for the combined weight of all processor power planes (VCC_CPU). • Use at least 2 oz copper for the combined weight of all processor ground planes. • These layers can be implemented using two 1 oz copper layers or four ½ oz copper layers.	• Refer to Section 13.4.1.	
Power / Ground Plane Geometry	• The power / ground supply to both processor sockets can be distributed as a dedicated layer of the PCB, a voltage supply plane with other power islands, or an island on a signal layer. • Never distribute processor power with traces. • Do not route capacitors to the processor socket using traces. • The island or plane connecting the Voltage Regulator Module (VRM) or Voltage Regulator Down (VRD) supply to both processor sockets should not have any breaks or voids.	• A "trace" is any etch that is less than the width of the processor socket.	
Power / Ground Plane Processor Socket Breakout	• The power / ground planes should completely surround all of the pins of the VRM or VRD and processor socket. • Minimize the size of the processor socket vias anti-pads where possible. Anti-pads should be no larger than 35 mils. • Locations of the capacitor pads on the outer power layer should not hinder power distribution by creating a "slot"-shaped geometry in the plane. • Avoid vias around the socket breakout area as much as possible.	• Refer to Section 13.4.1. • Section 13.4.1 contains an example of good socket power / ground plane routing for an inner layer.	
Voltage Regulator Placement and Sense / Feedback Lines			
VRM-based topology	• Use the "Row" pattern topology.	• Refer to Figure 13-6.	
VRD-based topology	• Use the "L" pattern or "Row" pattern topology.	• Refer to Figure 13-6 and Figure 13-9	
VRD sense point	• Route the VRD's voltage sense input signal to the middle of the VCC_CPU plane. The location of this plane connection and route is not critical.		

Table 16-2. Processor Power Delivery Layout Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Comments	√
Power / Ground Planes			
VRM VO-sen+ / VO-sen- remote sense	• If available on the VRM, route the VR's differential remote sense input signals to the middle of the VCC_CPU plane. • Route the positive feedback line to a point on the VCC_CPU power plane in the middle of and equidistant from both processors. Route the negative feedback line to the corresponding X-Y location, but on the VCC_VSS ground plane. • The traces should be carefully routed to avoid picking up noise • They must affect less than 1 Ω roundtrip resistance to minimize the voltage drop between the sense point and VR input. • Route each of the feedback lines with less than 5 inches total trace length. Do not route near signal lines unless shielding is provided.	• Middle is defined as a point that provides the shortest geometrical mid-point between the centers of the processor sockets.	
VRD voltage feedback	• Route the positive (and negative if the VRD provides differential inputs) voltage feedback inputs for the VRD to the VCC_CPU plane with the following conditions. • They must be connected to the power plane through a series resistor. This resistor should be sized to provide the correct droop to satisfy the load line requirement. • They must affect less than 1 Ω roundtrip resistance to minimize the voltage drop between the sense point and VR input. • Route the positive feedback line to a point on the VCC_CPU power plane in the middle of and equidistant from both processors. • Route the negative feedback line to the corresponding X-Y location, but on the VCC_VSS ground plane. • Route each of the feedback lines with less than 5 inches total trace length. Do not route near signal lines unless shielding is provided. • The trace(s) should be carefully routed to avoid picking up noise.	• Contact your VRD component vendors for their specific recommended implementation. Refer to the applicable CRB schematics for feedback details specific to these platforms and specific VRD solution used. The recommendations included in this entry are generic. • Middle is defined as a point that provides the shortest geometrical mid-point between the centers of the processor sockets.	
VCC_SENSE / VSS_SENSE	• Do not connect the VRD / VRM inputs to the processor VCC_SENSE / VSS_SENSE signals.	• These processor SENSE signals are measurement points used for processor power validation purposes only. • Connecting these processor signals to the VRD/VRM will result in incorrect VRD/VRM sensing operation.	

Table 16-2. Processor Power Delivery Layout Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Comments	√
Voltage Regulator Down Circuit Implementation (for VRD designs only!)			
Loadline Selection Circuit	• For designs based on a VRD solution, the system must include loadline selection circuitry that adjusts the voltage regulator's loadline output (offset and slope) based on whether one or two processors are installed.		
Low-pass filter on output of MOSFET phases	• Include an RC filter at the output of each of the four MOSFET phases. The exact value will depend on the actual voltage regulator Pulse Width Modulation (PWM) controller component and MOSFETs used.	• Contact your VRD component vendors for their suggested implementation.	
Series inductors on output of MOSFET phases	• Include series inductors at the output of each of the four MOSFET phases. Exact value will depend on the actual VR components used.	• Contact your VRD component vendors for their suggested implementation. Refer to the applicable CRB schematics for inductor values specific to these platforms and VRD solution.	
Switching frequency	• Carefully select the switching frequency of the PWM controller for each of the four MOSFET phases.	• Contact your VRD component vendors for their suggested implementation. Refer to the applicable CRB schematics for details on the switching frequency setting specific to these platforms and VRD solution.	
Decoupling Capacitors			
OSCON decoupling capacitors and placement	• Use at least ten 560 µF OSCON capacitors per processor socket. Place half on one side of the processor socket, half on the other side as close as the logic analyzer interface (LAI), retention mechanism (RM) and heatsink keep-out zones allow. Capacitors should be placed a maximum of 0.5 inches from the processor socket.	• Check with your LAI, RM and heatsink vendor for those keep-out zone requirements. When using the Intel Xeon processor boxed processor solution, refer to the *Intel® Xeon Processor with 512-KB L2 Cache Datasheet* for keep-out zone details.	

Table 16-2. Processor Power Delivery Layout Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Comments	√
1.0 and 22.0 µF decoupling capacitor quantity and placement	• Use at least twenty 22.0 µF ceramic capacitors per processor socket. • Use at least eight 1.0 µF ceramic capacitors per processor socket. • Place one quarter of the capacitors on one side of the processor socket, one quarter on the other side, and half in the processor socket cavity if using both sides of the motherboard. • If using single-sided motherboards, place as close to half the total quantity as possible, and place the remaining capacitors on the outside of the socket. • Place capacitors as close to the power/ground pins of the processor socket as physically possible. • Place capacitor vias within their pad. If this technology is not feasible, then keep traces between the pad and via as short and as wide as feasible. Possibly one or both ends of the capacitor may be connected directly to the processor socket pin without the use of a via. • Microstrip confifgurations require additional decoupling capacitors.	• Refer to the *Intel® Xeon Processor with 512-KB L2 Cache Datasheet* for the processor pinout.	
0.1 µF decoupling capacitor quantity and placement	• Distribute four minimum (six preferred) 0.1 µF capacitors evenly across the VCC_CPU / ground pins that are located in the portion of the processor socket pinout where system bus data lines are located. • Distribute three minimum (four preferred) 0.1 µF capacitors evenly across the VCC_CPU / ground pins that are located in the portion of the processor socket pinout where address and common clock signals are located. • Place all capacitors as close to the power/ground pins of the processor socket as physically possible. • Place capacitor vias within their pad. If this technology is not feasible, then keep traces between the pad and via as short and as wide as feasible. Possibly one or both ends of the capacitor may be connected directly to the processor socket pin without the use of a via.	• Refer to the *Intel® Xeon Processor with 512-KB L2 Cache Datasheet* for the processor pinout.	

16.3 System Bus Layout Checklist

Table 16-3. System Bus Layout Checklist

No.	Layout Recommendations	Comments	√
Data Signals: D[63:0]#, DBI[3:0]# Address Signals: A[31:3]#, REQ[4:0]			
1	• Point to Point Topology. No layer changes allowed. All signals and associated strobes in the same group must be routed on the same layer.	• See Table 5-2 for topology details	
2	• Traces should be 5 mils wide with 15 mil spacing.	• See Table 5-2 for signal lengths	
4	• Balance all data and address signals within ± 25 mils pad-to-pad with respect to their associated strobes between agents.		
Data Strobes: DSTBN/P[3:0] Address Strobes: ADSTB[1:0]			
1	• Point to Point Topology. No layer changes allowed. All signals and associated strobes in the same group must be routed on the same layer.	• See Table 5-2 for topology details	
2	• Traces should be 5 mils wide with 25 mil spacing.	• See Table 5-2 for signal lengths	
3	• Balance all data and address signals within ± 25 mils pad-to-pad with respect to their associated strobes between agents.		
Clocks: HCLKINP/HCLKINN			
1	• These should be routed as a differential pair with 7-mil traces and 7-mil spacing between them.		
2	• See Table 5-2 and Table 3-3 for signal lengths.		
3	• 25-mil spacing should be maintained around all clocks.		
Processor AGTL+: FERR#, PROCHOT#, THERMTRIP#			
1	• Traces should be 5 mils wide with 7-mil spacing		
2	• 1.0 inches to 12.0 inches max from processor to Intel® ICH4.		
3	• 3.0 inches max from ICH4 to VDD.		
ICH4 AGTL+: A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI#, STPCLK			
1	• Traces should be 5-mils wide with 5-mil spacing.		
2	• 12.0 inches max from ICH4 to processor.		
3	• Level shifting is required from the INIT# pin to FWH.		
ICH4 Open Drain AGTL+: PWRGOOD			
1	• 7-mil spacing.		
2	• 1.0 inch to 12.0 inches max from ICH4 to processor.		
3	• 1.1 inches max breakout length.		
4	• 3.0 inches max from Processor to VDD.		

Table 16-3. System Bus Layout Checklist

No.	Layout Recommendations	Comments	√
Miscellaneous AGTL+: BR0#, RESET#			
1	• Terminate using discrete components on the system board.		
2	• Minimize the distance between the terminating resistors and the processors.		
3	• Connect the signals between these components.		
Miscellaneous AGTL+: COMP[1:0]			
1	• Minimize the distance from terminating resistor.		
Miscellaneous AGTL+: THERMDA, THERMDC			
1	• 10-mils wide by 10-mil spacing.		
2	• Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4.0 inches to 8.0 inches away as long as the worst noise sources such as clock generators, data, buses and address buses, etc. are avoided.		
3	• Route in parallel and close together with ground guards enclosed.		

16.4 Intel® ICH4 Layout Checklist

Table 16-4. Intel® ICH4 Layout Checklist (Sheet 1 of 5)

No.	Layout Recommendations	Comments	√
1	• Board impedance must be 50 Ω ± 10% if using Hub Interface 1.5.		
2	• Traces must be routed 5-mils wide with 15-mils spacing.		
3	• To breakout of the MCH and Intel® ICH4 package, the Hub Interface signals can be routed 5 on 5. Signals must be separated to 5 on 15 within 300 mils of the package.		
4	• Max trace length 20” is dependant on MCH/ICH4 simulations.		
5	• Data signals must be matched within ± 0.1 inches of the HI_STB differential pair.		
6	• HI_STB/HI_STBS and HI_STB#/HI_STBF lengths’ must be matched.		
7	• (Local Reference Divider Circuit only) HIREF dividers should be placed no more than 4 inches of away from MCH or ICH4.		
8	• HI signals must be referenced to ground.		
IDE Interface			
1	• 5-mil wide and 7-mil spaces (using given example 4-layer 4.3-mil prepreg stack-up).		
2	• Max trace length is 8 inches long.		
3	• The maximum length difference between the data and strobe lengths is 0.5 inches.		
USB 2.0			
1	• With minimum trace lengths, route high-speed clock and USB differential pairs first.		
2	• Route USB signals ground referenced.		
3	• Route USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.		
4	• When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.		
5	• Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.		
6	• Stubs on USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs on a given data line should not be greater than 200 mils.		

Table 16-4. Intel® ICH4 Layout Checklist (Sheet 2 of 5)

No.	Layout Recommendations	Comments	√
7	• Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.)		
8	• Keep USB signals clear of the core logic set. High current transients are produced during internal state transitions, which can be very difficult to filter out.		
9	• Keep traces at least 90 mils away from the edge of the plane (VCC or GND depending on which plane to which the trace is routed). This helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB.		
10	• Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90Ω differential impedance. (Recommended: 7.5 on 7.5 spacing with 4-layer, 4.3-mil prepreg stack-up).		
11	• Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 50 mils.		
12	• Use 20-mil minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk.		
13	• USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pair (such as DM1 and DP1) should be no greater than 150 mils.		
14	• No termination resistors needed for USB.		
15	• USBRBIAS (ball A23) and USBRBIAS# (ball B23) should be routed 5 on 5 with a single trace 500 mils or less to the 22.6 ohm 1% resistor to ground.		
16	• Maximum length from the ICH4 to the backpanel should not be greater than 17 inches.		
Platform LAN Connect Interface			
1	• Trace spacing: 5-mils wide, 10-mil (using given example 4-layer 4.3-mil prepreg stack-up).		
2	• Stubs due to R-pak LOM stuffing option should not be present.	• To minimize inductance.	
3	• Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inches (clock must be longest trace).	• To meet timing and signal quality requirements.	
4	• Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN PHY.	• To meet timing and signal quality requirements.	
5	• Keep the total length of each differential pair (from PHY to connector) under 4 inches (preferably less than 2 inches).	• Issues found with traces longer than 4 inches: IEEE phy conformance failures, excessive EMI and or degraded receive BER.	

Table 16-4. Intel® ICH4 Layout Checklist (Sheet 3 of 5)

No.	Layout Recommendations	Comments	√
6	• Do not route the transmit differential traces closer than 100 mils to the receive differential traces.	• To minimize crosstalk.	
7	• Distance between differential traces and any other signal line is 100 mils. (300 mils recommended).	• To minimize crosstalk.	
8	• Route 5 mils on 10 mils for differential pairs (out of LAN phy).	• To meet timing and signal quality requirements.	
9	• Differential trace impedance should be controlled to be ~100 Ω.	• To meet timing and signal quality requirements.	
10	• For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two 45-degree bends.	• To meet timing and signal quality requirements.	
11	• Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	• This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.	
12	• Do not route traces and vias under crystals or oscillators.	• This will prevent coupling to or from the clock.	
13	• Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	• To control trace EMI radiation.	
14	• Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	• Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.	
15	• Vias to decoupling capacitors should be sufficiently large in diameter.	• To decrease series inductance.	
16	• Avoid routing high-speed LAN near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.	• To minimize crosstalk.	
17	• Isolate I/O signals from High-speed signals.	• To minimize crosstalk.	
18	• Place the Intel® 82562ET/EM part more than 1.5 inches away from any board edge.	• This minimizes the potential for EMI radiation problems.	
19	• Place at least one bulk capacitor (4.7 µF or greater OK) on each side of the 82562ET/EM.	• Research and development has shown that this is a robust design recommendation.	
20	• Place decoupling capacitors (0.1 µF) as close to the 82562ET/EM as possible.		

Table 16-4. Intel® ICH4 Layout Checklist (Sheet 4 of 5)

No.	Layout Recommendations	Comments	√
AC'97			
1	• Z_0 AC97 = 60 Ω ± 15%		
2	• 5-mil trace width, 5-mil spacing between traces		
3	• AC_SDIN Max Trace Lengths • ICH4 to primary codec: L = 14 inches		
4	• AC_SDOUT Max Trace Lengths • ICH4 to primary codec: L = 14 inches		
5	• AC_BIT_CLK Max Trace Lengths • ICH4 to primary codec: L = 13.6 inches		
6	• Series termination resistor on AC_BIT_CLK line should be no more than 0.9 to 7.6 inches from the ICH4.		
7	• Series termination resistors on AC_SDIN lines if needed should be no more than 100 to 400 mils from the on board codec.		
Clocking			
1	• CLK_33 goes to ICH4, FWH, and SIO. • Clock chip to series resistor 0.5 inches and from series resistor to receiver 15 inches max. Routed on one Layer.		
2	• PCI_33 goes to PCI Device or PCI Slot; there are 5 clocks. • Clock chip to series resistor 0.5 inches and from series resistor to receiver 13 inches max. Routed on one layer.		
3	• CLK_66 goes to ICH4 and MCH. • Clock chip to series resistor 0.5 inches and from series resistor to receiver 14 inches max. Routed on one layer.		
RTC			
1	• RTC LEAD length = 1.0 inches Maximum.		
2	• Minimize capacitance between RTCX1 and RTCX2.		
3	• Put GND plane underneath Crystal components.		
4	• Do not route switching signals under the external components (unless on other side of board).		

Table 16-4. Intel® ICH4 Layout Checklist (Sheet 5 of 5)

No.	Layout Recommendations	Comments	√
PCI Guidelines			
1	• For 2 to 4 slot boards (4 to 10 inches to the first slot and then 1 inch to each subsequent slot). • For 5 slot boards (4 to 8 inches to the first slot and then 1 inch to each subsequent slot) • For 6 slot boards (4 to 6 inches to the first slot and then 1 inch to each subsequent slot) • PCI clocks and loop-back clocks are scaled accordingly. (See Figure 10-26)		
2	• IDSEL (See Figure 10-25)		
Processor CMOS Guidelines			
1	• Series termination should be less than 2000 mils from the ICH4. Total length from the ICH4 to the processor should be no more than 19 inches.		
FWH Decoupling Guidelines			
1	• 0.1 µF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins.		
2	• 4.7 µF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins.		

16.4.1 Intel® ICH4 Decoupling

Table 16-5. Intel® ICH4 Decoupling Checklist

No.	Layout Recommendations	Comments	√
1	• VCC3_3: Six 0.1 µF capacitors. • Less than 100 mils from package: Place near balls: A4, A1, H1, T1, AC10, and AC18.		
2	• VccSus3_3: Two 0.1 µF capacitors. • Less than 100 mils from package: Place near balls: A22 and AC5.		
3	• $V_{\_CPU\_IO}$: One 0.1 µF capacitor. • Less than 100 mils from package: Place capacitor near ball AA23		
4	• VCC1_5: Two 0.1 µF capacitors. • Less than 100 mils from package: Place near balls: K23 and C23		
5	• VccSus1_5: Two 0.1 µF capacitors. • Less than 100 mils from package Place near balls: A16 and AC1		
6	• V5REF: One 0.1 µF capacitor. • Less than 100 mils from package: Place capacitor near balls: E7 • V5REF is the reference voltage for 5 V tolerant inputs in the Intel® ICH4. Tie to pins V5REF[2:1]. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3		
7	• V5REF_Sus: One 0.1 µF capacitor. • Less than 100 mils from package: Place capacitor near ball: A16 • V5REF_Sus only affects 5 V-tolerance for USB OC[5:0]# pins and can be connected to VccSus3_3 if 5 V tolerance on these signal is not required.		
8	• VccRTC: One 0.1 µF capacitor. • Place near ball: AB5		
9	• VCCHI: Two 0.1 µF capacitor. • Less than 100 mils from package: Place near balls: T23 and N23		
10	• VCCPLL: One 0.1 µF and one 0.01 µF capacitor. • Within 100 mils of package: Place near ball: C22		

16.5 Hub Interface Layout Checklist

Table 16-6. Hub Interface Layout Checklist

No.	Layout Recommendations	Comments	√
General Recommendations			
1	• It is recommended that all signals be referenced to VSS.		
2	• Board impedance must be 60 Ω ± 10%.		
3	• Traces must be routed 5-mils wide with 15-mils spacing.		
4	• Max trace length is 8 inches.		
Data Signals			
1	• Can be routed to 5 on 5 for breakout, but must be separated to 5 on 15 within 300 mils of the package.		
2	• No explicit matching requirements between individual data signals.		
Strobe Signals			
1	• Strobe pair should have a minimum of 15-mils spacing from any adjacent signals.		
2	• Each strobe signal must be the same length.		
3	• Strobe trace lengths should be 0–400 mils shorter than the longest data trace length.		

16.5.1 Hub Interface Decoupling, Compensation, and VREF

Table 16-7. Hub Interface Decoupling, Compensation, and VREF Checklist

No.	Layout Recommendations	Comments	√
VCC1_8 Decoupling			
1	• Decouple the Intel® ICH4 with two 0.1 µF capacitors within 150 mils from the package.		
2	• Decouple the MCH with one 0.1 µF capacitor within 150 mils of the package and one 10 µF capacitor nearby.		
3	• Capacitors should be adjacent to hub interface rows.		
HLRCOMP			
1	• Place resistor using a 10 mils wide and 0.5 inch max trace length.		
2	• 7 mil group spacing.		
3	• Minimize the distance between HLRCOMP resistor and MCH.		
HI_REF			
1	• Should be placed no more than 4 inches of away from MCH or ICH4.		
2	• Bypass to ground with a 0.1 µF capacitor located within 0.25 inches of each component's HIREF pin.		
3	• Place one 0.1 µF capacitor at the divider .		

16.6 System Memory Layout Checklist

16.6.1 Unbuffered DDR (2 DIMM) Checklist

Table 16-8. Unbuffered DDR (2 DIMM) Checklist

Checklist Items	Recommendations	Comments	√
MCH / DIMM Signals			
DQ_x[63:0] CB_x[7:0] DQS_x[8:0]	• Route on a ground-referenced stripline layer. MCH to first DIMM should be 1.0–6.0 inches, Z_O = 45 Ω, 6/15. First DIMM to DIMM should be 1.1–1.2 inches, 55 Ω, 4/15. Second DIMM to termination should be 0.4–1.2 inches, 55 Ω, 4/15. DQ/CB lengths should be within 25 mils of associated DQS. Make sure to match the strobe lengths to the clocks as described in Section 7.3.4.1.1.	ChA	
		ChB	
MA_x[13:0] BA_x[1:0] RAS_x# CAS_x# WE_x#	• Route on a ground-referenced microstrip layer, Z_0 = 55 Ω, 5/15. MCH to first DIMM should be 1.5–6.0 inches. First DIMM to second DIMM should be 1.1–1.2 inches. Second DIMM to termination should be 0.1– 1.2 inches. Make sure to match the signal lengths to the clocks as described in Section 7.3.5.1.	ChA	
		ChB	
CS_x[3:0]# CKE_x[3:0]	• Route on a ground-referenced microstrip layer, Z_0 = 50 Ω, 6/18. MCH to DIMM should be 1.5–5.5 inches. DIMM to termination should be 0.1–1.2 inch. Make sure to match the signal lengths to the clocks as described in Section 7.3.2.1.	ChA	
		ChB	
CMDCLK_x[7:4,1:0] CMDCLK_x[7:4,1:0]#	• Route differentially on a ground-referenced microstrip layer. MCH to DIMM should be 3.5–8.5 inches, diff. Z_0= 100 Ω, 4.75/7. Keep clock pairs 20 mils from any other signals. Make sure to adhere to length matching rules for above signals.	ChA	
		ChB	
VREF	• Route a 20 mil wide trace to the resistor divider and to each DIMM in the channel. Keep all other signals at least 20 mils away.	ChA	
		ChB	
MCH Signals Only			
RCVENOUT_x#	• Connect to resistor divider with a 6 mil wide trace. Keep the trace length to a minimum.	ChA	
		ChB	
DRCOMPVREF_HDR COMPVREF_V	• Connect to resistor divider with a 20 mil wide trace. Keep the trace length to a minimum.		
DRCOMP_H DRCOMP_V	• Connect to pull-down resistor with a 6 mil wide trace. Keep the trace length to a minimum.		
DDR_STRAP	• Connect to 2.5 V with a 6 mil wide trace. Keep the trace length to a minimum.		
ODTCOMP	• Connect to pull-down resistor with a 6 mil wide trace. Keep the trace length to a minimum.		

16.6.2 Registered DDR (3 DIMM) Checklist

Table 16-9. Registered DDR (3 DIMM) Checklist

Checklist Items	Recommendations	Comments	√
MCH / DIMM Signals			
DQ_x[63:0] CB_x[7:0] DQS_x[17:0]	• Route on a ground-referenced stripline layer. MCH to Rs should be 2.0– 5.0 inches, Z_0= 45 Ω, 6/15. Rs to first DIMM should be 0.5– 0.7 inches, 45 Ω, 6/15. DIMM to DIMM should be 1.1–1.2 inches, 55 Ω, 4/15. Last DIMM to termination should be 0.1–0.8 inches, 55 Ω, 4/15. DQ/CB lengths should be within 25 mils of associated DQS.	ChA	
		ChB	
MA_x[13:0] BA_x[1:0] RAS_x# CAS_x# WE_x# CKE_x[1:0]	• Route on a ground-referenced microstrip layer, Z_0 = 50 Ω, 6/18. MCH to first DIMM should be 2.0–5.0 inches. DIMM to DIMM should be 1.1–1.2 inches. Last DIMM to termination should be 0.1–0.8 inches.	ChA	
		ChB	
CS_x[5:0]#	• Route on a ground-referenced microstrip layer, Z_0 = 50 Ω, 6/15. MCH to DIMM should be as follows: 5.1– 7.1 inches to first DIMM 8.1– 10.1 inches to second DIMM 9.8–11.8 inches to third DIMM • DIMM to termination should be 0.1–1.5 inches	ChA	
		ChB	
CMDCLK_x[2:0] CMDCLK_x[2:0]#	• Route differentially on a ground-referenced microstrip layer, diff. Z_0 = 100 Ω, 4.75/7. MCH to first DIMM should be 6.1 inches. MCH to second DIMM should be 9.1 inches. MCH to third DIMM should be 10.8 inches. Keep clock pairs 20 mils from any other signals. • Make sure to adhere to length matching rules for above signals.	ChA	
		ChB	
VREF	• Route a 20 mil wide trace to the resistor divider and to each DIMM in the channel. Keep all other signals at least 20 mils away.	ChA	
		ChB	
MCH Signals Only			
RCVENOUT_x#	• Connect to resistor divider with a 6 mil wide trace. Keep the trace length to a minimum.	ChA	
		ChB	
DRCOMPVREF_H DRCOMPVREF_V	• Connect to resistor divider with a 20 mil wide trace. Keep the trace length to a minimum.		
DRCOMP_H DRCOMP_V	• Connect to pull-down resistor with a 6 mil wide trace. Keep the trace length to a minimum.		
DDR_STRAP	• Connect to GND with a 6 mil wide trace. Keep the trace length to a minimum.		
ODTCOMP	• Connect to pull-down resistor with a 6 mil wide trace. Keep the trace length to a minimum.		

16.7 AGP 8X Layout Checklist

Table 16-10. AGP 8X Layout Checklist (Sheet 1 of 3)

No.	Layout Recommendations	Comments	√
Power Plane Decoupling			
1	• Use high-frequency decoupling capacitors in the range of (0.001 µF - 1 µF).		
2	• Use bulk decoupling capacitors in the range of (0.001 µF – 1 µF).		
3	• Capacitors should be as close to the power pins as possible. If possible, capacitors should be mounted on the backside of the graphics card under the controller package. Bulk decoupling can be mounted near the chipset interface and near the connector for power delivery and signaling reasons.		
AC Signal Decoupling Requirements			
1	• Place 3 0.01 µF or larger, low ESL capacitors as close as possible to a VCC3_3 pair of pins on the connector.		
2	• Place 6 0.01 µF or larger, low ESL capacitors as close as possible to a VDDQ pair of pins on the connector.		
3	• Place 1 0.01 µF or larger, low ESL capacitor as close as possible to the +5 V connector pin.		
4	• Place 1 0.01 µF or larger, low ESL capacitor as close as possible to the +12 V connector pin.		
5	• Place 1 0.01 µF or larger, low ESL capacitor as close as possible to the 3.3 V aux connector pin.		
6	• All power and ground pins must be connected to the motherboard to guarantee power delivery and proper AC signal return paths.		
7	• All ground pins on the add-in cards must be connected for proper grounding and AC return paths. All VDDQ pins must be connected on the add-in card to the local VDDQ power plane. All used power pins must be bypassed to ground close to the connector with a 0.01 µF or larger, low ESL/ESR capacitor to provide good AC coupling to the adjacent signaling pins.		

Table 16-10. AGP 8X Layout Checklist (Sheet 2 of 3)

No.	Layout Recommendations	Comments	√
Motherboard Layout Requirements			
1	• AGP strobe signals must be grouped with associated data signals. It is also recommended that the strobe be centered within its associated group to minimize the signal to strobe skew.		
2	• AD_STB0 and AD_STB0# (AGP 2.0) or AD_STBFO and AD_STBSO (AGP 3.0) should be grouped with AD[15:0] and C#/BE[1:0].		
3	• AD_STB1 and AD_STB1# (AGP 2.0) or AD_STBF1 and AD_STBS1 (AGP 3.0) should be grouped with AD[31:16], C#/BE[3:2], DBI_HI, DBI_LO (AGP 3.0).		
4	• SB_STB and SB_STB# should be grouped with SBA[7:0] (AGP 2.0) or • SB_STBF and SB_STBS should be grouped with SBA[7:0]# (AGP 3.0).		
5	• Traces should as short and direct as possible. Avoid changing the power plane reference during routing.		
6	• PCB should be fabricated using FR-4 with an overall board thickness of 62 miles ± 10%. The outer layers should use ½ Copper and the inner layers should use 1 oz copper.		
7	• AGP signals must be carefully routed on the motherboard and graphics card to meet the timing and signal quality requirements of the specification.		
Trace Length Mismatch Requirements			
1	• Avoid signal mismatch by routing all lines within a group using the same type (either stripline or microstrip).		
2	• For add-in cards, the data lines should be kept within ± 0.025 inches from their respective strobe.		
3	• For motherboards, the data lines should be kept within ± 0.025 inches from their respective strobe.		
Strobe Trace Routing Considerations			
1	• The strobe signals should be routed together, but separated by at least five times the maximum dielectric thickness to each other and to any other signal routed adjacent to the strobe.		
Board Constraints			
1	• Impedance of required microstrip traces is specified at 60 Ω ± 10% and the impedance for stripline traces is specified at 56 Ω ± 10% for add-in cards and motherboards.		
2	• Reduce crosstalk by decreasing the distance of a trace to the nearest reference plane (dielectric thickness/height); or increase the distance to adjacent traces.		
3	• The 8X mode source synchronous signals and the 66 MHz clock signal should not cross any split planes. Ensure signal quality is not compromised.		
4	• All 8X mode source synchronous signals should be routed on a layer reference to a ground plane.		
5	• Dummy vias should be used to match the total via count for each group.		

Table 16-10. AGP 8X Layout Checklist (Sheet 3 of 3)

No.	Layout Recommendations	Comments	√
Control Signal and Clock Recommendations			
1	• There are no external pull-up or pull-down resistors for control signals on the AGP 8X mode board design because resistors are integrated inside the device buffers.		
Ground Plane References			
1	• Each source synchronous signal group must be routed on the same layer referenced to ground with the same layer transitions.		
VDDQ Plane			
1	• The plane from the voltage regulator source to the AGP connector VDDQ pins should be wide enough to minimize the inductance path.		
2	• Buffer I/O rail on the add-in card should connect to the VDDQ plane directly.		
Connector Impedance Matching			
1	• The motherboard designer can put short trace stubs near each connector pin to increase the equivalent capacitance which can help reduce the AGP connector impedance.		
Trace Bends and Serpentines			
1	• Void 90 degrees bends, instead use two 45 degree bends. Trace bends and serpentines generate coupling causing the line to be shorter electrically.		

16.8 CK 408 Layout Checklist

Table 16-11. CK 408 Layout Checklist (Sheet 1 of 3)

No.	Layout Recommendations	Comments	√
Host Clock: CPU#/CPU			
1	• 7-mils wide.		
2	• Differential pair spacing should be based on a distance from HCLKINN to HCLKINP.		
3	• Spacing to other traces should 4 times to 5 times greater than distance from HCLKINN to HCLKINP.		
4	• Processor routing length- Clock driver to R_S should be 0.5 inch maximum.		
5	• Processor routing length- R_S to R_S-R_T should be 0 inch to 0.2 inch.		
6	• Processor routing length- R_S-R_T node to R_T should be 0 inch to 0.2 inch.		
7	• Processor routing length- R_S-R_T node to load should be 2 inches to 9 inches.		
8	• MCH routing length- Clock driver to R_S should be 0.5 inch maximum.		
9	• MCH routing length- R_S to R_S-R_T should be 0.5 inch maximum.		
10	• MCH routing length- R_S-R_T node to R_T should be 0.0 inch to 0.2 inch maximum.		
11	• MCH routing length- R_S-R_T node to load should be 2.0 inches to 9.0 inches maximum.		
12	• Clock driver to processor and clock driver to chipset length matching should be 600 mils.		
13	• 10-mil length matching between HCLKINN to HCLKINP.		
14	• Do not split up the two halves of a differential clock pair between layers.		
15	• Route all agents on the same physical routing layer referenced to ground of the differential clock.		
16	• Make sure that the skew induced by the vias is compensated in the traces to other agents.		
17	• Do not place vias between adjacent complementary clock traces.		
18	• Maintain uniform spacing between the two halves of differential clocks.		
19	• Route clocks on physical layers adjacent to the VSS reference plane only.		

Table 16-11. CK 408 Layout Checklist (Sheet 2 of 3)

No.	Layout Recommendations	Comments	√
66 MHz Clock Group			
1	• Point to Point Topology.		
2	• 5-mils wide and 20-mil spacing.		
3	• 20-mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• Trace length from series termination to receiver on the motherboard between 4.0 inches and 8.5 inches.		
6	• The total trace lengths must be matched to ± 100 mils of each other.		
7	• Follow these guidelines when routing to an AGP device down on the motherboard.		
AGP Clock (when routing to an AGP connector)			
1	• Point to Point Topology.		
2	• 5-mils wide and 20-mil spacing.		
3	• 20-mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• The total trace length must be 4.0 inches less than the CLK66 total trace lengths ± 100 mils.		
33 MHz Clock Group			
1	• Point to Point Topology.		
2	• 5-mils wide and 15-mil spacing.		
3	• 15-mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• The total mismatch between any two 33 MHz clocks must be less than 7.5 inches. If routing to a PCI connector, 2.6 inches of routing on the PCI card must be included in the 7.5 inches total mismatch.		
6	• The 33 MHz clock to the ICH4 must be matched to ± 100 mils of the 66 MHz clock to the ICH4.		
14 MHz Clock Group			
1	• Balanced T Topology.		
2	• 5-mils wide and 10-mil spacing.		
3	• 10-mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• The total trace length from the clock driver to SIO and clock driver must be matched to 0.5 inch.		
6	• Signal must T within 12 inches of the series termination. • Max trace length of stubs is 6 inches.		
7	• Total trace length matched to ± 0.5 inch of each other.		

Table 16-11. CK 408 Layout Checklist (Sheet 3 of 3)

No.	Layout Recommendations	Comments	√
USB Clock			
1	• Point to Point Topology.		
2	• 5-mils wide.		
3	• 15-mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• Trace length from series termination to receiver on the motherboard between 3.0 inches and 12 inches.		

16.8.1 CK 408 Decoupling Checklist

Table 16-12. CK 408 Decoupling Checklist

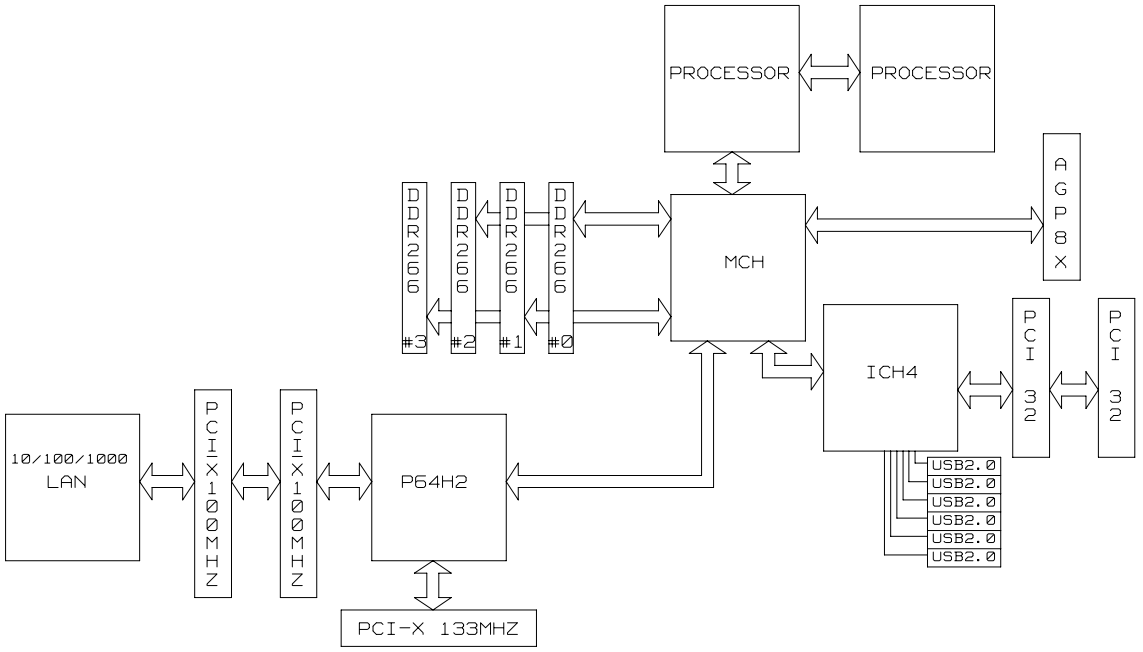
No.	Layout Recommendations	Comments	√
VDDA/VDD Decoupling			
1	• Place one 10 µF capacitor close to the VDD generation circuitry.		
2	• Place six 0.1 µF capacitors close to the VDD pins on the clock driver.		
3	• Place three 0.01 µF capacitors close to the VDDA pins on the clock driver.		
4	• Place one 10 µF bulk decoupling capacitor close to the VDDA generation circuitry.		
5	• Host clock pairs must be differentially routed on the same physical routing layer.		
6	• Differential clocks must not have more than two via transitions.		
7	• Ground referencing is strongly recommended for all platform clocks.		
8	• Motherboard layer transitions and power plane splits must be kept to a minimum.		

Schematics A

This appendix contains a set of schematics for the Intel® Xeon™ processor / Intel® E7505 chipset platform Customer Reference Board (CRB).

PAGE	COMPONENT / FUNCTION
1	TITLE / TABLE OF CONTENTS
2	VOLTAGE TABLE
3	DEVICE TABLE
4	SYSTEM BLOCK DIAGRAM
5	IRQ DIAGRAM
6	RESET DIAGRAM
7	CLOCKING BLOCK DIAGRAM
8	VRM AND REGULATOR BLOCK DIAGRAM
9	SMBUS ADDRESS PARTITION
10-13	PROCESSOR P0 / P1
14	PROCESSOR DECOUPLING
15	ITP, FUTURE PROCESSOR SUPPORT
16-19	MCH
20	CLOCK GENERATOR
21-24	DDR CHANNEL A DIMMS AND TERMINATION
25-28	DDR CHANNEL B DIMMS AND TERMINATION
29	DDR VREFS AND DECOUPLING
30	AGP 8X CONNECTOR
31-33	82801DB I/O CONTROLLER HUB 4 (ICH 4)
34-36	PCI32 SLOTS 4-5 AND TERMINATION
37	IDE
38-39	82870P2 PCI/PCI-X 64 BIT HUB (P64H2)
40-44	PCI-X SLOT1-3 AND TERMINATION
45	HECETA 6
46	GLUECHIP 4
47	FIRMWARE HUB
48	SUPER I/O
49-52	LEGACY I/O
53	USB BACK PANEL CONNECTORS
54	WAKE ON USB
55-57	AUDIO AD1885 AND SUPPORT CIRCUITRY
58	CHASSIS INTRUSION, BATTERY
59	FRONT PANEL HEADER AND SPEAKER
60-61	GIGABIT LAN
62	VREF CIRCUITS
63	POWER SUPPLY CONNECTORS
64-69	VOLTAGE REGULATORS
70	FAN CONTROL
71	VID CIRCUIT
72	STOP CLOCK INJECTION CIRCUIT, IDROM
73	BLANK PAGE
74	MOUNTING HOLES, PORT 80, LED'S
75-76	BLANK PAGES
77	FUTURE PROCESSOR SUPPORT
78	BLANK PAGE
79	SPARE COMPONENTS
80	BLANK PAGE
81-91	COMPONENT AND SIGNAL CROSS REFERENCE

INTEL(R) XEON (TM) PROCESSOR / INTEL(R) E7505 CHIPSET DUAL-PROCESSOR CUSTOMER REFERENCE SCHEMATICS



AA# A65795-300
PBA# A65800-300
PB# A80991-003
DOC# C1109901

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
TITLE / TABLE OF CONTENTS

REV: 1.5

INTEL EPG PAE
1900 PRAIRIE CITY RD.
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:02:30 2002

PAGE: 1

VOLTAGE TABLE

SYMBOL	NETNAME	
+12V :	+12V	:POWER SUPPLY OUTPUT
+3.3V:	+3_3V	:POWER SUPPLY OUTPUT
-12V :	-12V	:POWER SUPPLY OUTPUT
+5V :	P5V	:POWER SUPPLY OUTPUT
SB5V :	SB5V	:POWER SUPPLY OUTPUT
N\A :	P12V_CPU	:POWER SUPPLY OUTPUT
N\A :	GND	:SYSTEM DC GROUND
+1.2V:	P1_2V	:VOLTAGE REGULATOR OUTPUT FROM +5V
+1.25V:	VCC1_25V	:VOLTAGE REGULATOR OUTPUT FROM +2.5V
+1.5V:	VCC1_5V	:VOLTAGE REGULATOR OUTPUT FROM +3.3V (MCH-AGP ONLY)
+1.8V:	P1_8V	:VOLTAGE REGULATOR OUTPUT FROM +2.5V
+2.5V:	P2_5V	:VOLTAGE REGULATOR OUTPUT FROM +12V
SB1_5V:	SB1_5V	:VOLTAGE REGULATOR OUTPUT FROM SB5V
SB2_5V:	SB2_5V	:VOLTAGE REGULATOR OUTPUT FROM SB5V
SB3V :	STANDBY3V	:VOLTAGE REGULATOR OUTPUT FROM SB5V
N\A :	VCC_CORE	:VR OUTPUT FROM P12V_CPU
N\A :	VCC3_CLK	:CK408B FILTERED POWER FROM +3.3V
N\A :	VCC3_CLKA	:CK408B FILTERED POWER FROM +3.3V
N\A :	AGND	:ISOLATED GND FOR SERIAL,PARALLEL,USB,KEYBRD,MOUSE
N\A :	AUD_GND	:ISOLATED GND ISLAND FOR AUDIO
N\A :	AUD_VCC	:+5V VOLTAGE REGULATOR OUTPUT FROM +12V
N\A :	CHGND	:CHASSIS GND FOR LAN CONNECTORAND MAGNETICS
N\A :	VCCAFSB	:FILTERED MCH POWER FROM VCC_CORE
N\A :	VCCAHI	:FILTERED MCH POWER FROM +1.2V
N\A :	P1_5V_ICH4	:VOLTAGE REGULATOR OUTPUT FROM 3.3V (ICH4 ONLY)
PWR_GND:	PWR_GND	:ISOLATED GND FOR CPU D2D
PWR_GND:	PWR1_GND	:ISOLATED GND FOR 1.2V D2D
PWR_GND:	PWR2_GND	:ISOLATED GND FOR 2.5V D2D
PWR_GND:	PWR3_GND	:ISOLATED GND FOR 1.25V D2D

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB		
PAGE TITLE: VOLTAGE TABLE		REV: 1.5
INTEL EPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:30 2002	PAGE: 2

DEVICE TABLE

DEVICE	POWER	PINS
MCH	VCC_CORE	A30, B2, B8, B14, B20, B26, D3, D9, D15, D21, D27, F4, F10, F16, F22, H5, H11, H17, H23, K10, K12, K14, K16, K18, K20, K22, L11, L13, L15, L17, L19, L21
	+1.5V	L2, L8, M4, M10, N6, N11, P10, R11, T10, U2, U8, U11, V4, V10, W6
	+1.2V	AA11, AB6, AB10, AC2, AC11, AD4, AD10, AE6, AG4, AJ2, P14, P18, P20, R15, R17, R19, T14, T16, T18, T20, U17, U19, V14, V16, V18, V20, W15, W17, W19, Y10, Y14, Y16, Y18, Y20
	SB2_5V	AA23, AB24, AB30, AC13, AC15, AC17, AC19, AC21, AC23, AD12, AD14, AD16, AD18, AD20, AD22, AD24, AD28, AF11, AF17, AF23, AF32, AH9, AH15, AH21, AH27, AH30 AK7, AK13, AK19, AK25, AK31, AL32, AM5, AM11, AM17, AM23, AM29, AM31, B32, D30, F28, H26, H32, K24, K30, L23, L24, M24, M28, N23, P24, P26, P32, R23, T24, T30 U23, V24, V28, W23, Y24, Y26, Y32
	GND	A6, A9, A12, A15, A18, A21, A24, A27, AA1, AA4, AA7, AA10, AA24, AA27, AA28, AA31, AB3, AB9, AB11, AB23, AB27, AB28, AB33, AC5, AC8, AC10, AC12, AC14 AC16, AC18, AC20, AC22, AC26, AC29, AC32, AD1, AD7, AD11, AD13, AD15, AD17, AD19, AD21, AD23, AD31, AD33, AE3, AE9, AE25, AE27, AE30, AE33, AF2, AF5 AF8, AF14, AF20, AF28, AF29, AG1, AG7, AG10, AG13, AG16, AG19, AG22, AG23, AG25, AG28, AG31, AH3, AH6, AH12, AH14, AH16, AH18, AH19, AH24, AH26, AH29 AH33, AJ5, AJ8, AJ9, AJ11, AJ14, AJ16, AJ17, AJ20, AJ23, AJ26, AJ29, AJ32, AK1, AK4, AK10, AK12, AK16, AK22, AK28, AL3, AL6, AL9, AL12, AL15, AL18 AL19, AL21, AL24, AL25, AL27, AL30, AL31, AL33, AM2, AM8, AM14, AM20, AM21, AM26, AM32, AN4, AN5, AN6, AN7, AN10, AN13, AN15, AN17, AN19, AN22, AN25 AN28, AN29, AN31, B5, B11, B17, B23, B29, C1, C4, C7, C10, C13, C16, C19, C22, C25, C28, C31, D6, D12, D18, D24, D33, E2, E5, E8, E11, E14, E17, E20, E23 E26, E29, E30, E32, F1, F7, F13, F19, F25, F29, F31, F33, G3, G6, G9, G12, G15, G18, G21, G24, G27, G30, G33, H2, H8, H14, H20, H28, H29, J1, J4, J7, J10, J13 J14, J15, J19, J22, J25, J28, J31, K3, K6, K9, K11, K13, K15, K17, K19, K21, K23, K27, K33, L5, L10, L12, L14, L16, L18, L20, L22, L26, L29, L30, L32, M1 M7, M11, M23, M27, M31, M32, N3, N9, N10, N24, N27, N28, N30, N33, P2, P5, P8, P11, P15, P17, P19, P23, P29, R1, R4, R7, R10, R14, R16, R18, R20, R24, R28 R31, T3, T6, T9, T11, T15, T17, T19, T23, T26, T27, T33, U5, U10, U14, U16, U18, U20, U24, U25, U26, U29, U32, V1, V7, V11, V15, V17, V19, V23, V27, V31, V33 W3, W9, W10, W14, W16, W18, W20, W24, W27, W30, W33, Y2, Y5, Y8, Y15, Y17, Y19, Y23, Y25, Y29
PROCESSORS	+3.3V	AE28, AE29
	GND	A5, A11, A21, A27, A29, A31, AA2, AA9, AA15, AA17, AA23, AA30, AB1, AB5, AB11, AB21, AB27, AB31, AC2, AC7, AC13, AC19, AC25, AC30, AD3, AD9, AD15, AD17 AD23, AD31, AE2, AE11, AE21, AE27, B2, B9, B15, B17, B23, B28, B30, C1, C7, C13, C19, C25, C29, C31, D2, D5, D11, D21, D27, D28, D30, E1, E9, E15, E17, E23 E29, E31, F2, F7, F13, F19, F25, F28, F30, G1, G3, G5, G7, G9, G25, G27, G29, G31, H2, H4, H6, H8, H24, H26, H28, H30, J1, J3, J5, J7, J9, J23, J25, J27, J29 J31, K2, K4, K6, K8, K24, K26, K28, K30, L1, L3, L5, L7, L9, L23, L25, L27, L29, L31, M2, M4, M6, M8, M24, M26, M28, M30, N2, N4, N6, N8, N24, N26, N28, N30 P1, P3, P5, P7, P9, P23, P25, P27, P29, P31, R2, R4, R6, R8, R24, R26, R28, R30, T1, T3, T5, T7, T9, T23, T25, T27, T29, T31, U2, U4, U6, U8, U24, U26, U28, U30 V1, V3, V5, V7, V9, V23, V25, V27, V29, V31, W2, W4, W24, W26, W28, W30, Y1, Y5, Y7, Y13, Y19, Y25, Y31
	VCC_CORE	A2, A8, A14, A18, A24, A28, A30, AA1, AA4, AA6, AA12, AA20, AA26, AA31, AB2, AB8, AB14, AB18, AB24, AB30, AC3, AC4AC10, AC16, AC22, AC31, AD2AD6, AD12 AD20, AD26, AD30, AE3, AE8, AE14, AE18, AE24, B4, B6, B12, B20, B26, B29, B31, C2, C4, C10, C16, C22, C28, C30, D1, D8, D14, D18, D24, D29, D31, E2, E6, E12 E20, E26, E28, E30, F1, F4, F10, F16, F22, F29, F31, G2, G4, G6, G8, G24, G26, G28, G30, H1, H3, H5, H7, H9, H23, H25, H27, H29, H31, J2, J4, J6, J8, J24, J26 J28, J30, K1, K3, K5, K7, K9, K23, K25, K27, K29, K31, L2, L4, L6, L8, L24, L26, L28, L30, M1, M3, M5, M7, M9, M23, M25, M27, M29, M31, N1, N3, N5, N7, N9, N23 N25, N27, N29, N31, P2, P4, P6, P8, P24, P26, P28, P30, R1, R3, R5, R7, R9, R23, R25, R27, R29, R31, T2, T4, T6, T8, T24, T26, T28, T30, U1, U3, U5, U7, U9, U23 U25, U27, U29, U31, V2, V4, V6, V8, V24, V26, V28, V30, W1, W25, W27, W29, W31, Y2, Y10, Y16, Y22, Y30
82801DB (ICH4)	+3.3V(VCC3_CLK)	A5, AC8, AC17, B2, H6, H18, J1, J18, K6, M10, P6, P12, U1, V10, V16, V18
	GND	A1, A4, A16, A18, A20, A22, AA3, AA9, AA12, AA16, AA22, AB7, AB20, AC1, AC5, AC10, AC14, AC18, AC23, B9, B12, B16, B18, B20, B22, C6, C15, C17, C19, C21 C23, D1, D4, D8, D12, D15, D17, D19, D21, D22, D23, E10, E14, E16, E17, E18, E19, E21, E22, F8, G3, G6, G19, G21, H1, J6, K3, K11, K13, K19, K23, L10, L11 L12, L13, L14, L21, M1, M11, M12, M13, M20, M22, N5, N10, N11, N12, N13, N14, N19, N21, N23, P3, P11, P13, P20, P22, R5, R18, R21, T1, T19, T23, U20, V3 V15, V17, W5, W8, W22, Y7, Y19
	P1_5V_ICH4	C22, K10, K12, K18, K22, L23, M14, P10, P18, T18, T22, U19, V14
	SB1_5V	E12, E13, E20, F6, F7, F14, G18, R6, T6, U6
	SB5V	E15
	STANDBY3V	E9, E11, F9, F10, F15, F16, F17, F18, K14, V7, V8, V9
	VCC_CORE	AA23, P14, U18
82870P2 (P64H2)	+3.3V	AD24, G1, H8, H9, H16, H17, H18, J8, J9, J16, J17, J19, L6, L18, M7, M8, M9, M16, M17, M19, N8, N9, N16, N17, P6, P18, R7, R19, T8, T9, T12, T13, T16, T17, U6 U8, U9, U12, U13, U16, U17, U18, V7, V10, V13, V16, V19, W8, W11, W14, W17
	+1.8V	F8, F10, F12, F13, F15, F16, F17, G7, G9, G14, G15, G16, G17, H12, H13, J7, J12, J13, K10, K11, K14, K15, L10, L11, L14, L15, M12, M13, N12, N13, P10, P11 P14, P15, R10, R11, R14, R15, V9, V18
	GND	A7, A9, A13, A15, A17, AA1, AA4, AA7, AA10, AA13, AA16, AA19, AA22, AB2, AB5, AB8, AB11, AB14, AB17, AB20, AB23, AC3, AC6, AC9, AC12, AC15, AC18, AC21 AC24, AD1, AD4, AD7, AD10, AD16, AD19, AD22, B8, B10, B12, B14, B16, B20, C7, C9, C11, C13, C15, C17, D4, D8, D10, D12, D14, D16, D22, E7, E9, E11, E13, E15 E17, F14, F22, G5, G20, G23, H10, H11, H14, H15, H21, H24, J1, J4, J10, J11, J14, J15, J22, K2, K5, K8, K9, K12, K13, K15, K17, K20, K23, L3, L8, L9, L12, L13 L16, L17, L21, L24, M4, M10, M11, M14, M15, M22, N2, N5, N10, N11, N14, N15, N20, N23, P3, P8, P9, P12, P13, P15, P17, P21, P24, R1, R4, R8, R9, R12, R13, R16 R17, R22, T2, T5, T10, T11, T14, T15, T20, T23, U3, U10, U11, U14, U15, U21, U24, V1, V4, V22, W2, W5, W20, W23, Y3, Y6, Y9, Y12, Y15, Y18, Y21, Y24
CK408B	VCC3_CLK	1, 8, 14, 19, 32, 46, 50, 26, 37
	GND	4, 9, 15, 20, 27, 31, 36, 41, 47
82545EM (KENAI-64)	STANDBY3V	B8, B14, B19, C10, C16, D6, D11, E17, H4, H19 L17, M2, N19, R4, R17, U1, U3, U7, U11, U15 U19, W1, W5, W9, W13, W17, B4, F1
	SB2_5V	A19, G1, G2, G3, L2, L5, L18
	SB1_5V	G7, G8, G9, G12, G13, G14, H7, H8, H13, H14, J7 J14, M7, M14, N7, N8, N13, N14, P7, P8, P9, P12 P13, P14
	GND	A1, A2, A5, B11, B17, B3, B6, C3, D14, D3, D8 E19, F3, G10, G11, H10, H11, H12, H17, H2, H9 J10, J11, J12, J13, J8, J9, K10, K11, K12 K13, K14, K2, K7, K8, K9, L10, L11, L12, L13 L14, L19, L7, L8, L9, M10, M11, M12, M13, M4 M8, M9, N10, N11, N12, N17, N9, P10, P11, R19 R2, U13, U17, U5, U9, V2, W11, W15, W19, W3 W7, A10, K4, K5, E20
74HCT4051	+5V	16
	GND	7
HCT4052	+5V	16
	GND	8

SIO 47M102	+3.3V	53, 65, 93
	+5V	44
	STANDBY3V	18
	GND	7, 31, 40, 60, 76
AD1885	+3.3V	1, 9
	AUD_VCC	25, 38
	GND	4, 7, 26, 40, 44
GLUECHIP4	SB5V	2
	STANDBY3V	3
	GND	43 29 11
74HC682	+3.3V	20
	GND	10

HECETA 6	VCC_CORE	23
	GND	3
FWH	+3.3V	25, 27, 32
	GND	16, 26, 28
SC1405	+5V	8
	GND	10
SC1110	+12V	1
	GND	5
HIP6004E	+12V	18
	GND	11
HIP6311	+5V	20
	GND	9

74F08	+5V	14
	GND	7
AT24C01	+3.3V	8
	GND	4
74LVC00	+3.3V	14
	GND	7
74LVC03D	+3.3V	7
	GND	14

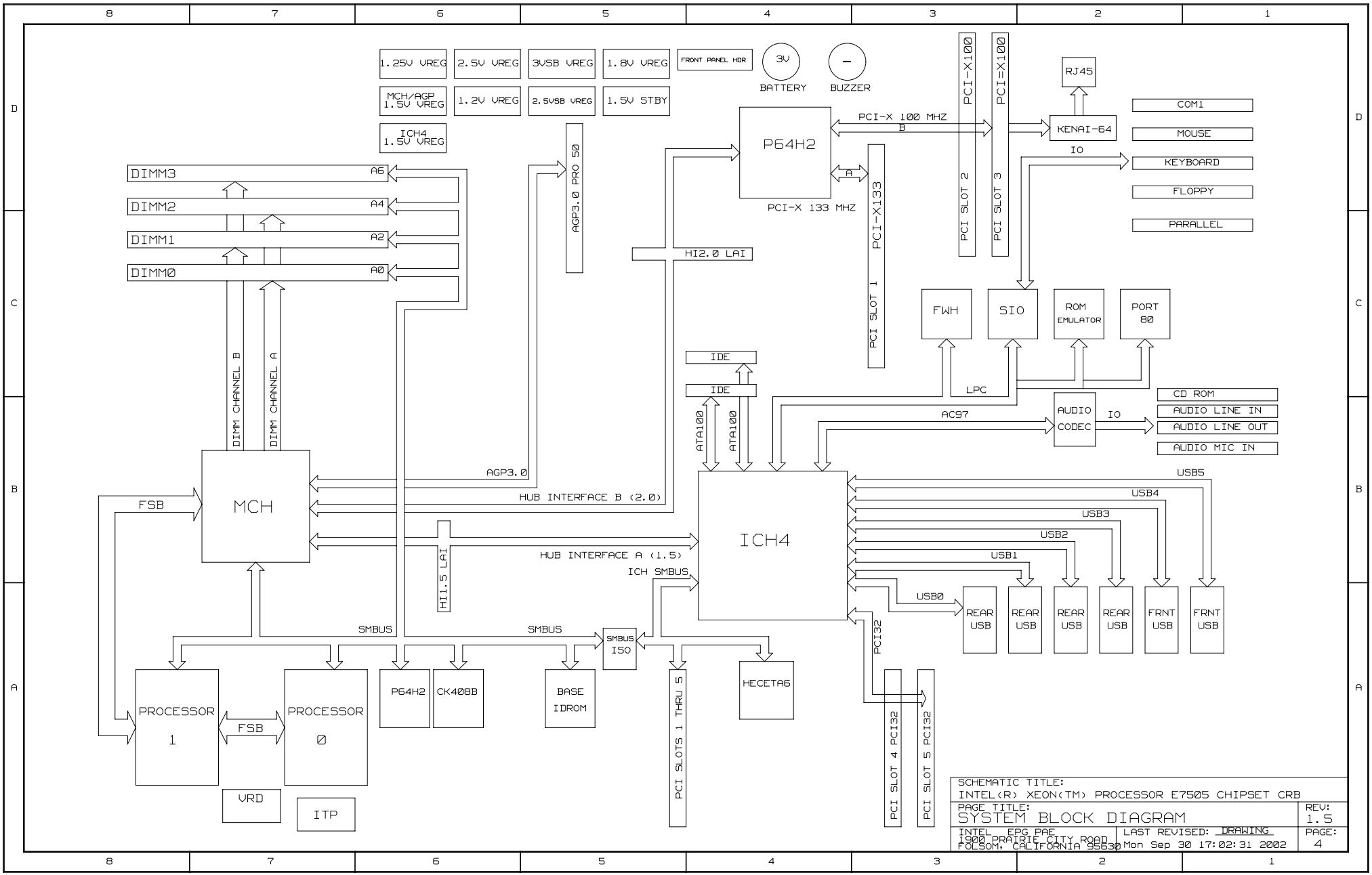
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

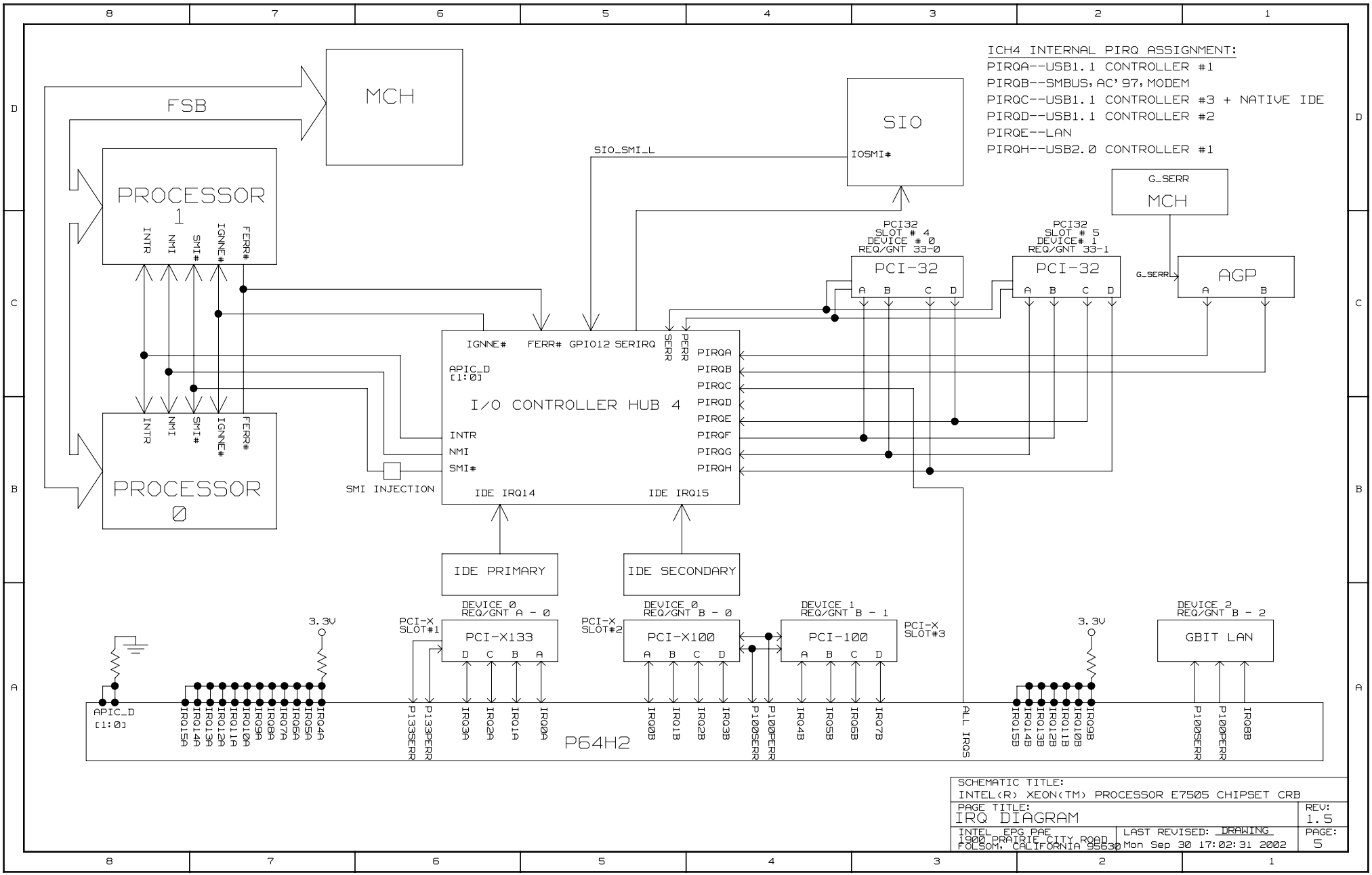
PAGE TITLE:
DEVICE TABLE

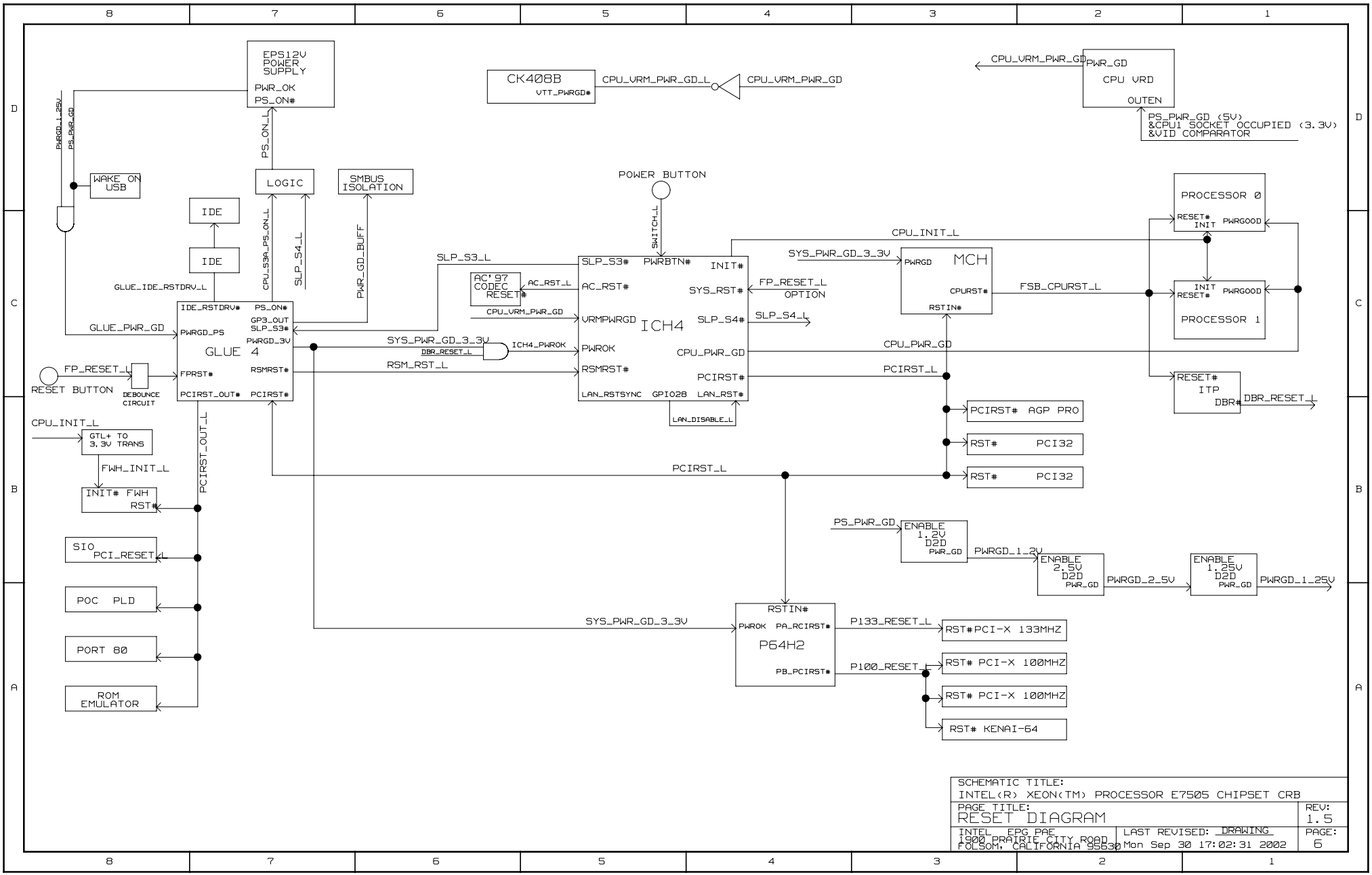
REV: 1.5

INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

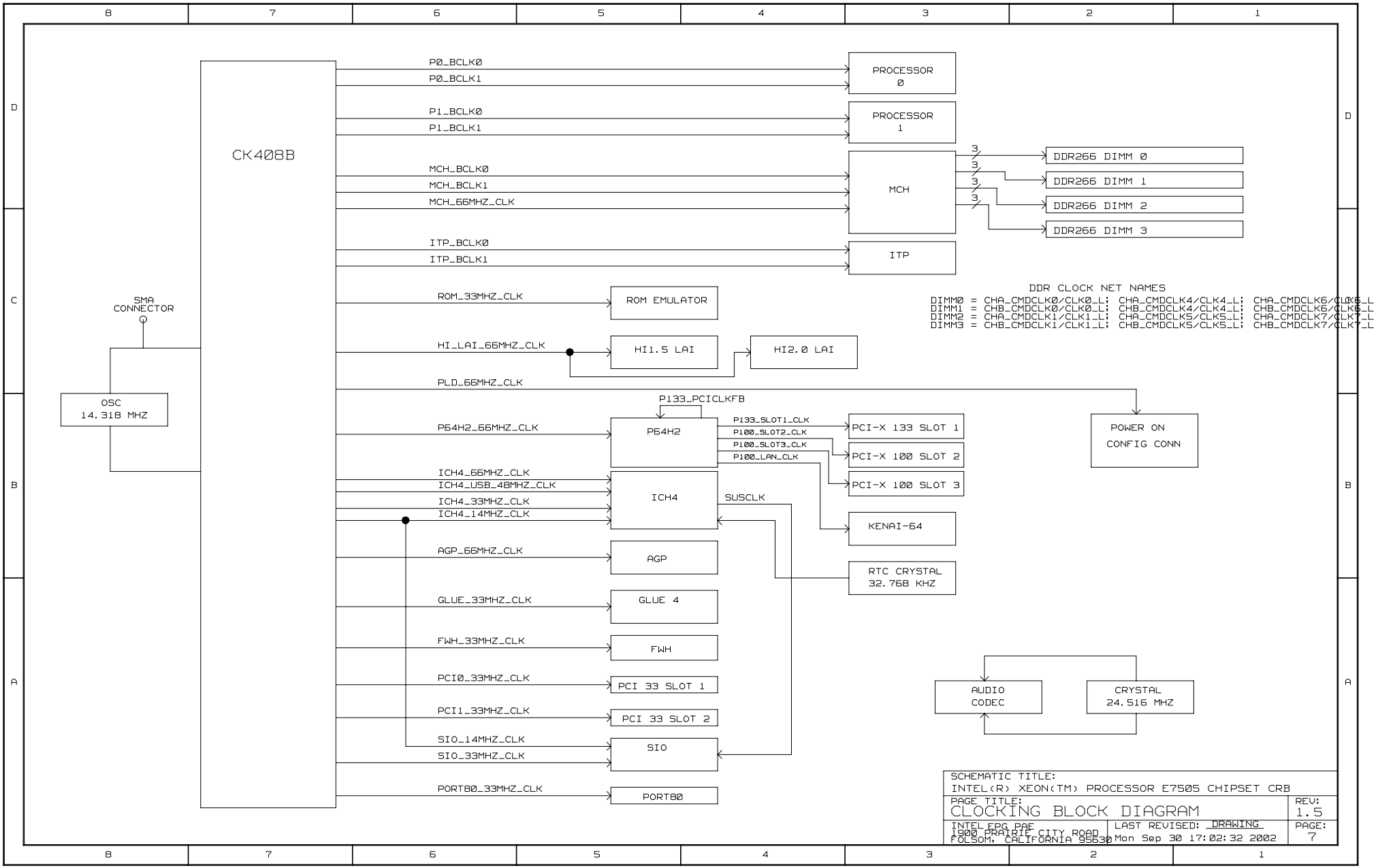
LAST REVISED: _DRAWING_
Mon Sep 30 17:02:30 2002

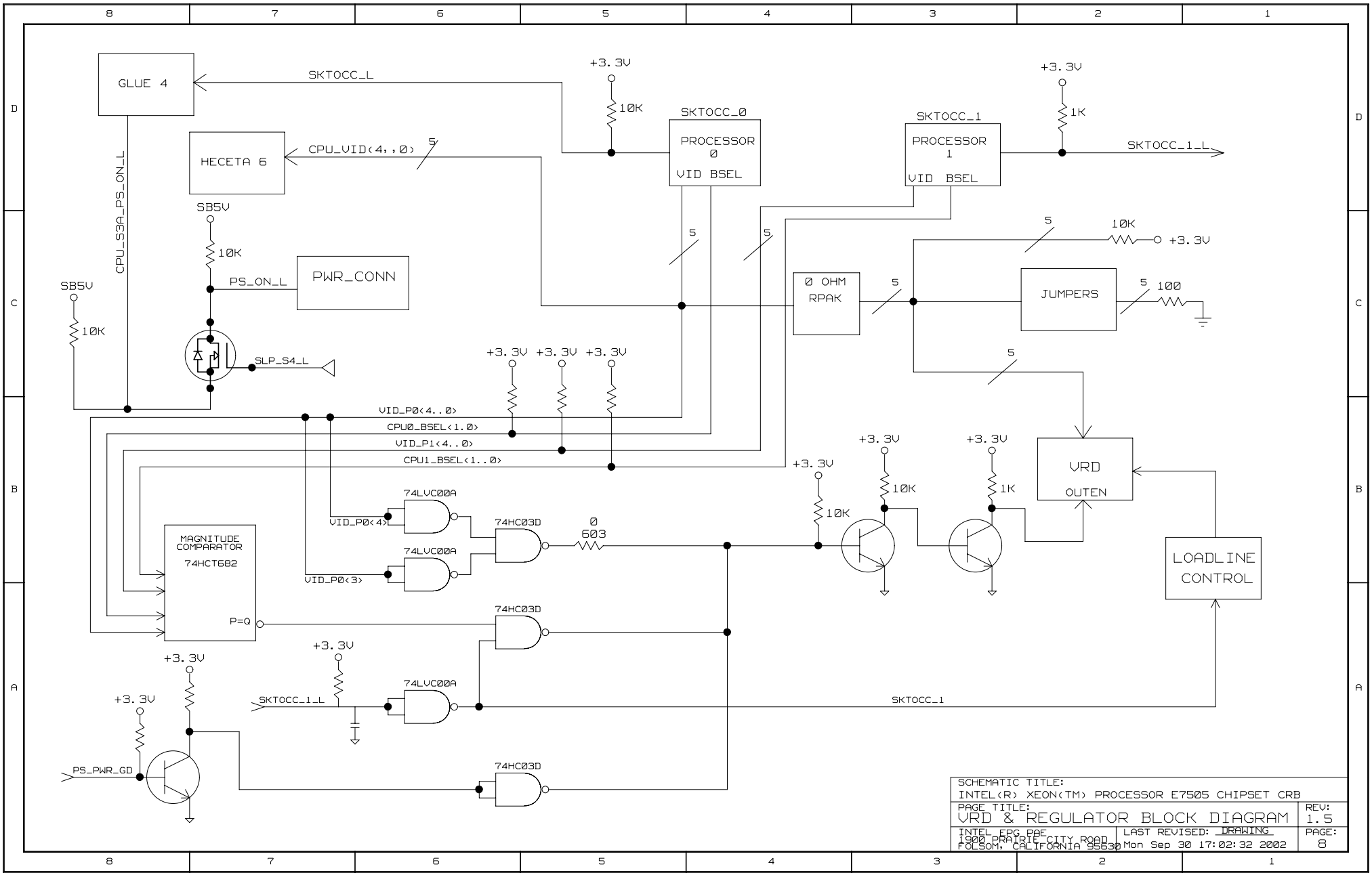

1.25V VREG
2.5V VREG
3VSB VREG
1.8V VREG
FRONT PANEL HDR
3V
BATTERY
BUZZER
MCH/AGP 1.5V VREG
1.2V VREG
2.5VSB VREG
1.5V STBY
ICH4 1.5V VREG
PCI-X100
PCI-X100
RJ45
P64H2
PCI-X 100 MHZ
B
A
PCI-X 133 MHZ
KENAI-64
IO
COM1
MOUSE
KEYBOARD
FLOPPY
PARALLEL
PCI SLOT 2
PCI SLOT 3
PCI SLOT 1
PCI-X133
AGP3.0 PRO 50
HI2.0 LAI
DIMM3
DIMM2
DIMM1
DIMM0
A6
A4
A2
A0
DIMM CHANNEL B
DIMM CHANNEL A
FWH
SIO
ROM EMULATOR
PORT 80
IDE
IDE
ATA100
ATA100
LPC
AC97
AUDIO CODEC
IO
CD ROM
AUDIO LINE IN
AUDIO LINE OUT
AUDIO MIC IN
AGP3.0
HUB INTERFACE B (2.0)
FSB
MCH
ICH4
USB5
USB4
USB3
USB2
USB1
USB0
HUB INTERFACE A (1.5)
HI1.5 LAI
ICH SMBUS
REAR USB
REAR USB
REAR USB
REAR USB
FRNT USB
FRNT USB
SMBUS
SMBUS
SMBUS ISO
PCI32
PROCESSOR 1
FSB
PROCESSOR 0
P64H2
CK408B
BASE IDROM
HECETA6
PCI SLOTS 1 THRU 5
PCI SLOT 4 PCI32
PCI SLOT 5 PCI32
VRD
ITP
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
SYSTEM BLOCK DIAGRAM
REV:
1.5
INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:31 2002
PAGE:
4


ICH4 INTERNAL PIRQ ASSIGNMENT:
PIRQA--USB1.1 CONTROLLER #1
PIRQB--SMBUS, AC'97, MODEM
PIRQC--USB1.1 CONTROLLER #3 + NATIVE IDE
PIRQD--USB1.1 CONTROLLER #2
PIRQE--LAN
PIRQH--USB2.0 CONTROLLER #1
MCH
FSB
SIO
IOSMI#
SIO_SMI_L
G_SERR
MCH
PROCESSOR 1
INTR
NMI
SMI#
IGNNE#
FERR#
PCI32 SLOT # 4 DEVICE # 0 REQ/GNT 33-0
PCI-32
PCI32 SLOT # 5 DEVICE# 1 REQ/GNT 33-1
PCI-32
G_SERR
AGP
A B C D
A B
IGNNE# FERR# GPIO12 SERIRQ SERR PERR
APIC_D [1:0]
I/O CONTROLLER HUB 4
PIRQA
PIRQB
PIRQC
PIRQD
PIRQE
PIRQF
PIRQG
PIRQH
INTR
NMI
SMI#
PROCESSOR 0
SMI INJECTION
IDE IRQ14
IDE IRQ15
IDE PRIMARY
IDE SECONDARY
DEVICE 0 REQ/GNT A - 0
DEVICE 0 REQ/GNT B - 0
DEVICE 1 REQ/GNT B - 1
DEVICE 2 REQ/GNT B - 2
PCI-X SLOT#1
PCI-X133
PCI-X SLOT#2
PCI-X100
PCI-100
PCI-X SLOT#3
GBIT LAN
3.3V
3.3V
D C B A
A B C D
APIC_D [1:0]
IRQ15A IRQ14A IRQ13A IRQ12A IRQ11A IRQ10A IRQ9A IRQ8A IRQ7A IRQ6A IRQ5A IRQ4A
P133SERR P133PERR IRQ3A IRQ2A IRQ1A IRQ0A
P64H2
IRQ0B IRQ1B IRQ2B IRQ3B P100SERR P100PERR IRQ4B IRQ5B IRQ6B IRQ7B
ALL IRQS
IRQ15B IRQ14B IRQ13B IRQ12B IRQ11B IRQ10B IRQ9B
P100SERR P100PERR IRQ8B
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
IRQ DIAGRAM
REV:
1.5
INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:31 2002
PAGE:
5

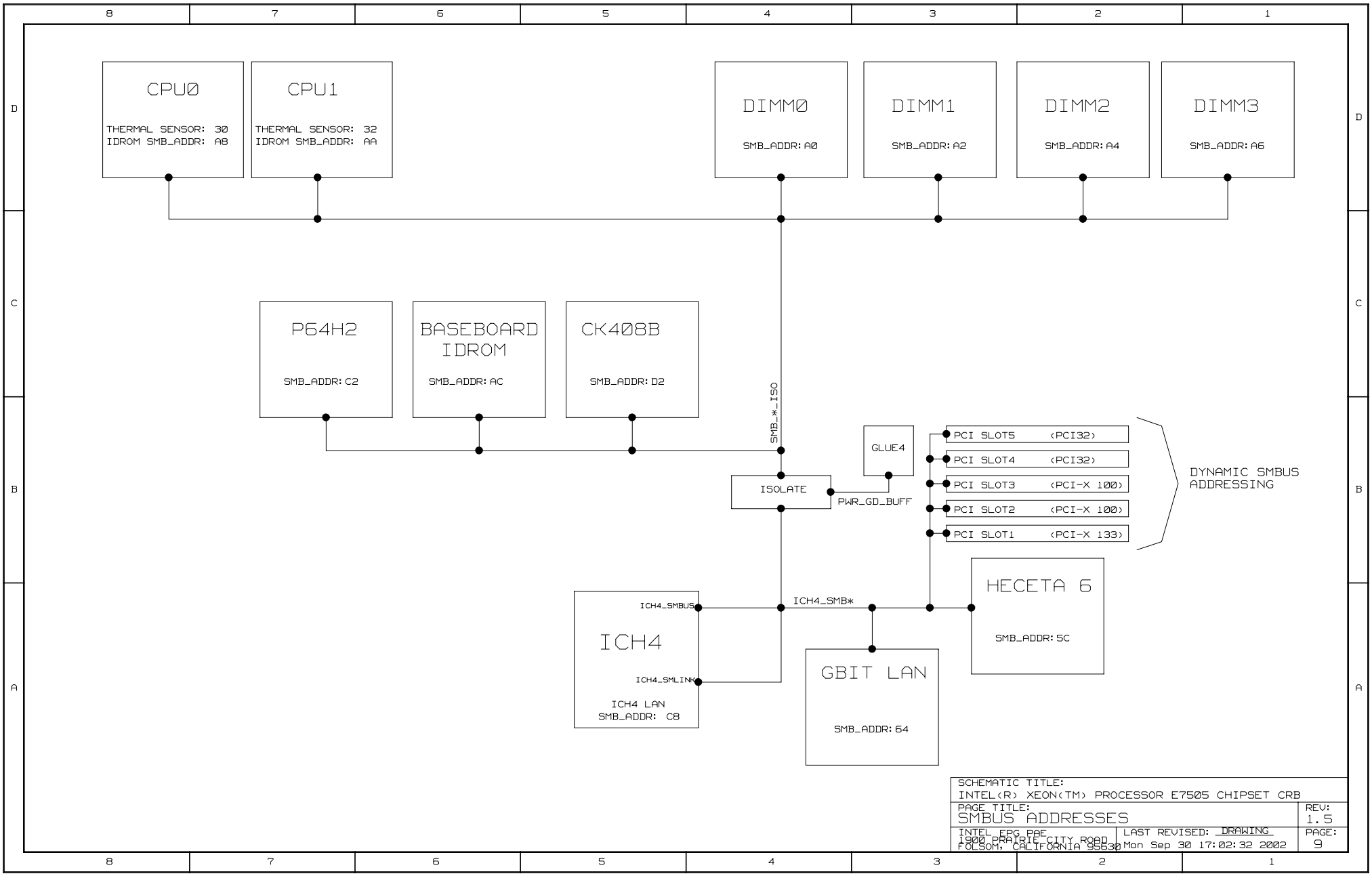


SCHEMATIC TITLE:	INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:	RESET DIAGRAM
REV:	1.5
INTEL EPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: _DRAWING_ Mon Sep 30 17:02:31 2002
PAGE:	6

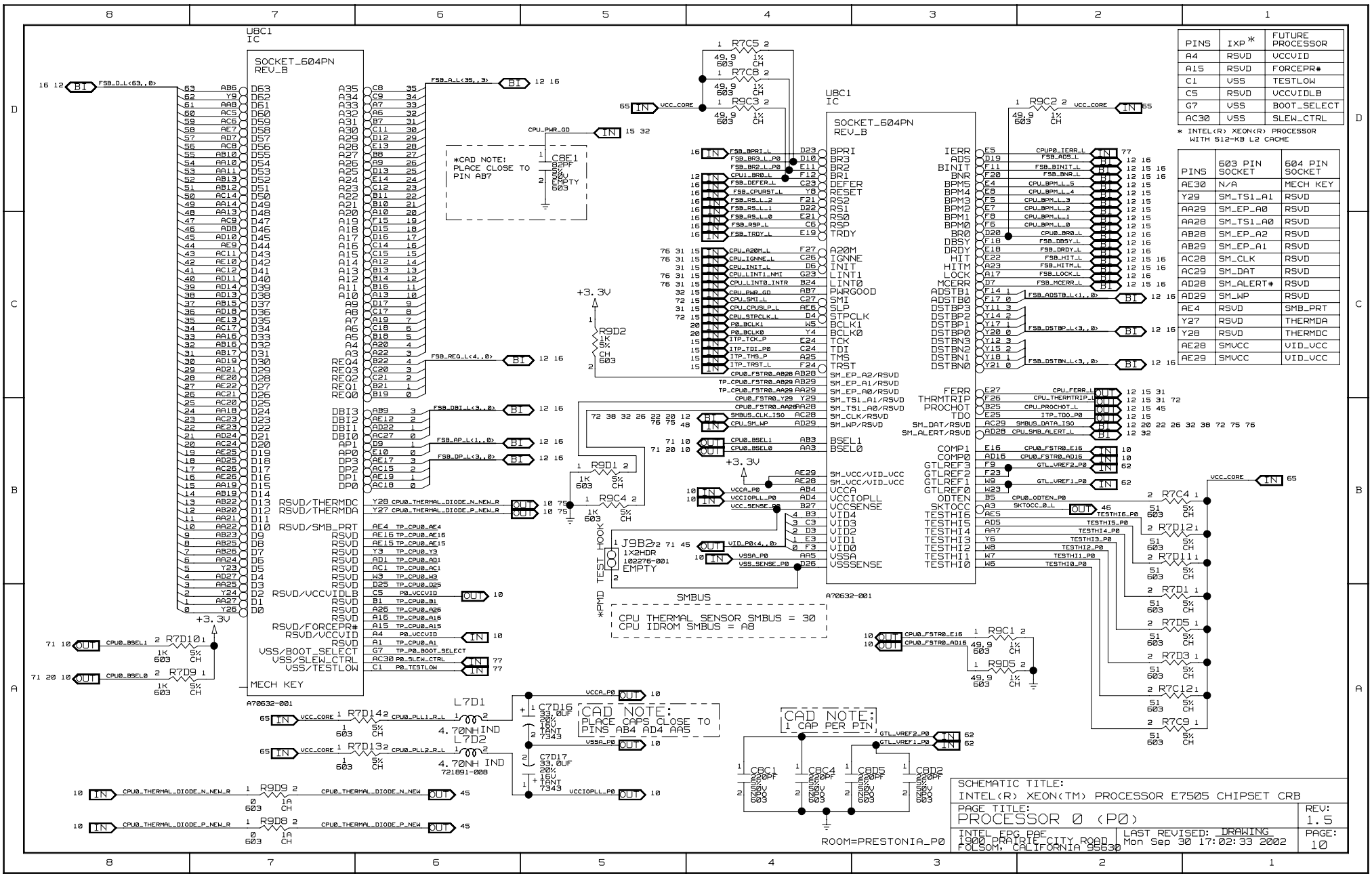

CK408B
P0_BCLK0
P0_BCLK1
P1_BCLK0
P1_BCLK1
MCH_BCLK0
MCH_BCLK1
MCH_66MHZ_CLK
ITP_BCLK0
ITP_BCLK1
ROM_33MHZ_CLK
HI_LAI_66MHZ_CLK
PLD_66MHZ_CLK
P64H2_66MHZ_CLK
ICH4_66MHZ_CLK
ICH4_USB_48MHZ_CLK
ICH4_33MHZ_CLK
ICH4_14MHZ_CLK
AGP_66MHZ_CLK
GLUE_33MHZ_CLK
FWH_33MHZ_CLK
PCI0_33MHZ_CLK
PCI1_33MHZ_CLK
SIO_14MHZ_CLK
SIO_33MHZ_CLK
PORT80_33MHZ_CLK
PROCESSOR 0
PROCESSOR 1
MCH
ITP
DDR266 DIMM 0
DDR266 DIMM 1
DDR266 DIMM 2
DDR266 DIMM 3
ROM EMULATOR
HI1.5 LAI
HI2.0 LAI
SMA CONNECTOR
OSC 14.318 MHZ
P64H2
P133_PCICLKFB
P133_SLOT1_CLK
P100_SLOT2_CLK
P100_SLOT3_CLK
P100_LAN_CLK
PCI-X 133 SLOT 1
PCI-X 100 SLOT 2
PCI-X 100 SLOT 3
POWER ON CONFIG CONN
ICH4
SUSCLK
KENAI-64
RTC CRYSTAL 32.768 KHZ
AGP
GLUE 4
FWH
PCI 33 SLOT 1
PCI 33 SLOT 2
SIO
PORT80
AUDIO CODEC
CRYSTAL 24.516 MHZ
DDR CLOCK NET NAMES
DIMM0 = CHA_CMDCLK0/CLK0_L; CHA_CMDCLK4/CLK4_L; CHA_CMDCLK6/CLK6_L
DIMM1 = CHB_CMDCLK0/CLK0_L; CHB_CMDCLK4/CLK4_L; CHB_CMDCLK6/CLK6_L
DIMM2 = CHA_CMDCLK1/CLK1_L; CHA_CMDCLK5/CLK5_L; CHA_CMDCLK7/CLK7_L
DIMM3 = CHB_CMDCLK1/CLK1_L; CHB_CMDCLK5/CLK5_L; CHB_CMDCLK7/CLK7_L
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
CLOCKING BLOCK DIAGRAM
REV:
1.5
INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:32 2002
PAGE:
7



SCHEMATIC TITLE:	
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB	
PAGE TITLE: VRD & REGULATOR BLOCK DIAGRAM	REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:32 2002
	PAGE: 8



SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB	
PAGE TITLE: SMBUS ADDRESSES	REV: 1.5
INTEL_FPG_PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: _DRAWING_ Mon Sep 30 17:02:32 2002
	PAGE: 9



PINS	IXP *	FUTURE PROCESSOR
A4	RSVD	VCCVID
A15	RSVD	FORCEPR#
C1	VSS	TESTLOW
C5	RSVD	VCCVIDLB
G7	VSS	BOOT_SELECT
AC30	VSS	SLEW_CTRL

* INTEL(R) XEON(R) PROCESSOR WITH 512-KB L2 CACHE

PINS	603 PIN SOCKET	604 PIN SOCKET
AE30	N/A	MECH KEY
Y29	SM_TS1_A1	RSVD
AA29	SM_EP_A0	RSVD
AA28	SM_TS1_A0	RSVD
AB28	SM_EP_A2	RSVD
AB29	SM_EP_A1	RSVD
AC28	SM_CLK	RSVD
AC29	SM_DAT	RSVD
AD28	SM_ALERT#	RSVD
AD29	SM_WP	RSVD
AE4	RSVD	SMB_PRT
Y27	RSVD	THERMDA
Y28	RSVD	THERMDC
AE28	SMVCC	VID_VCC
AE29	SMVCC	VID_VCC

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

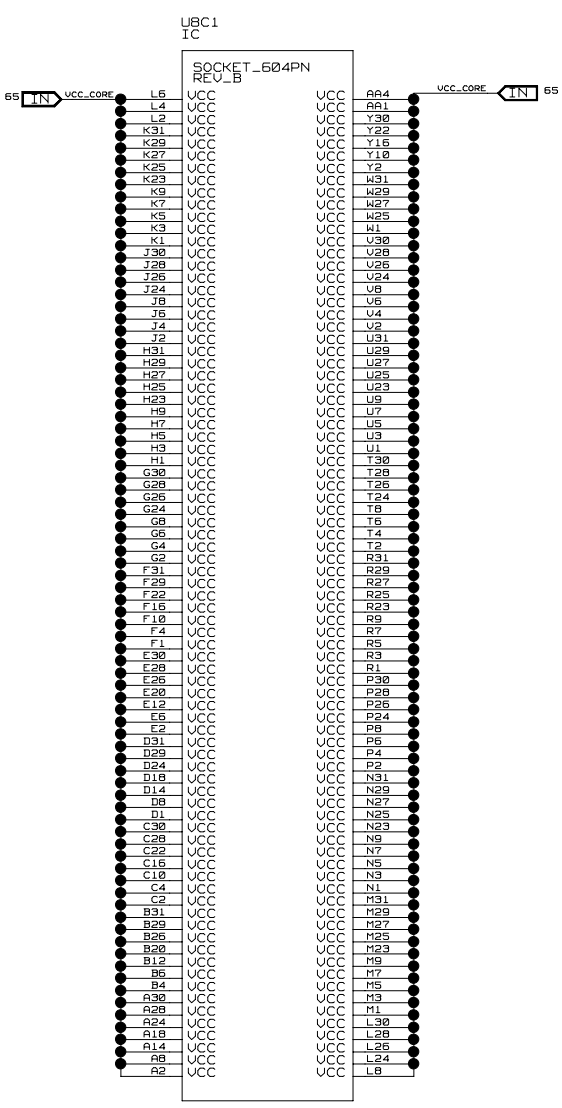
PAGE TITLE:
PROCESSOR 0 (P0)

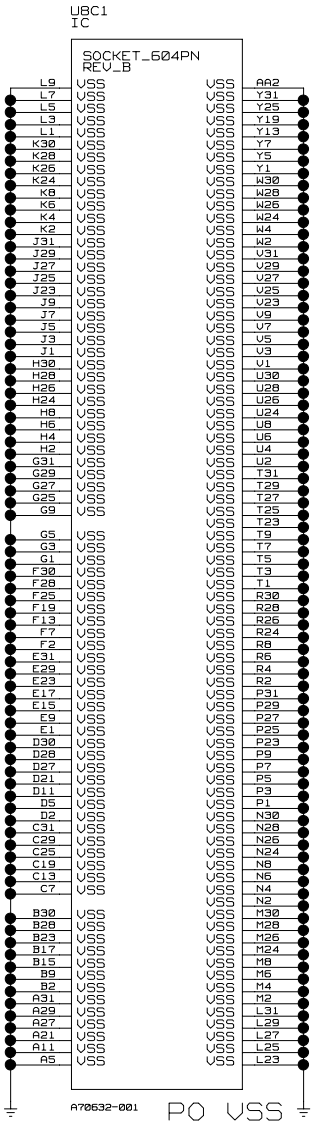
REV: 1.5

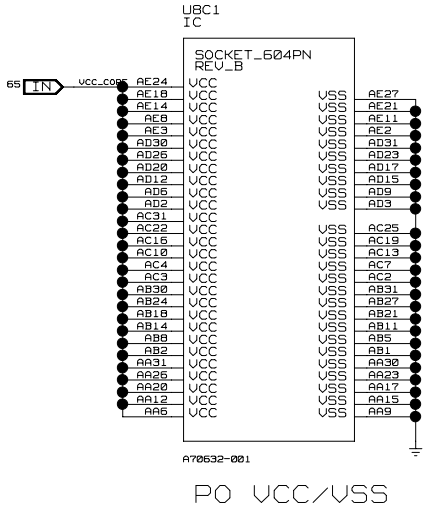
INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:02:33 2002

PAGE: 10

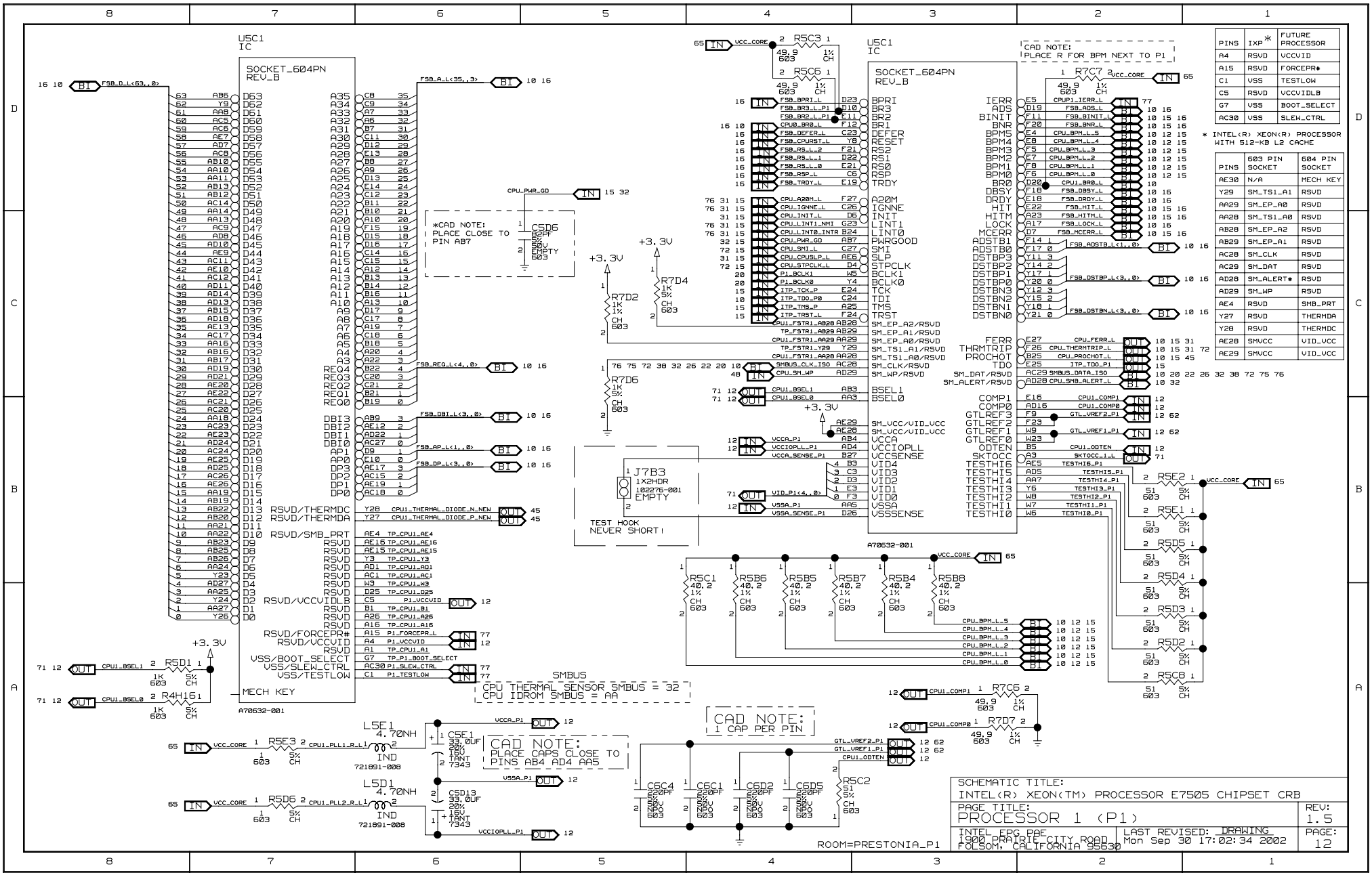


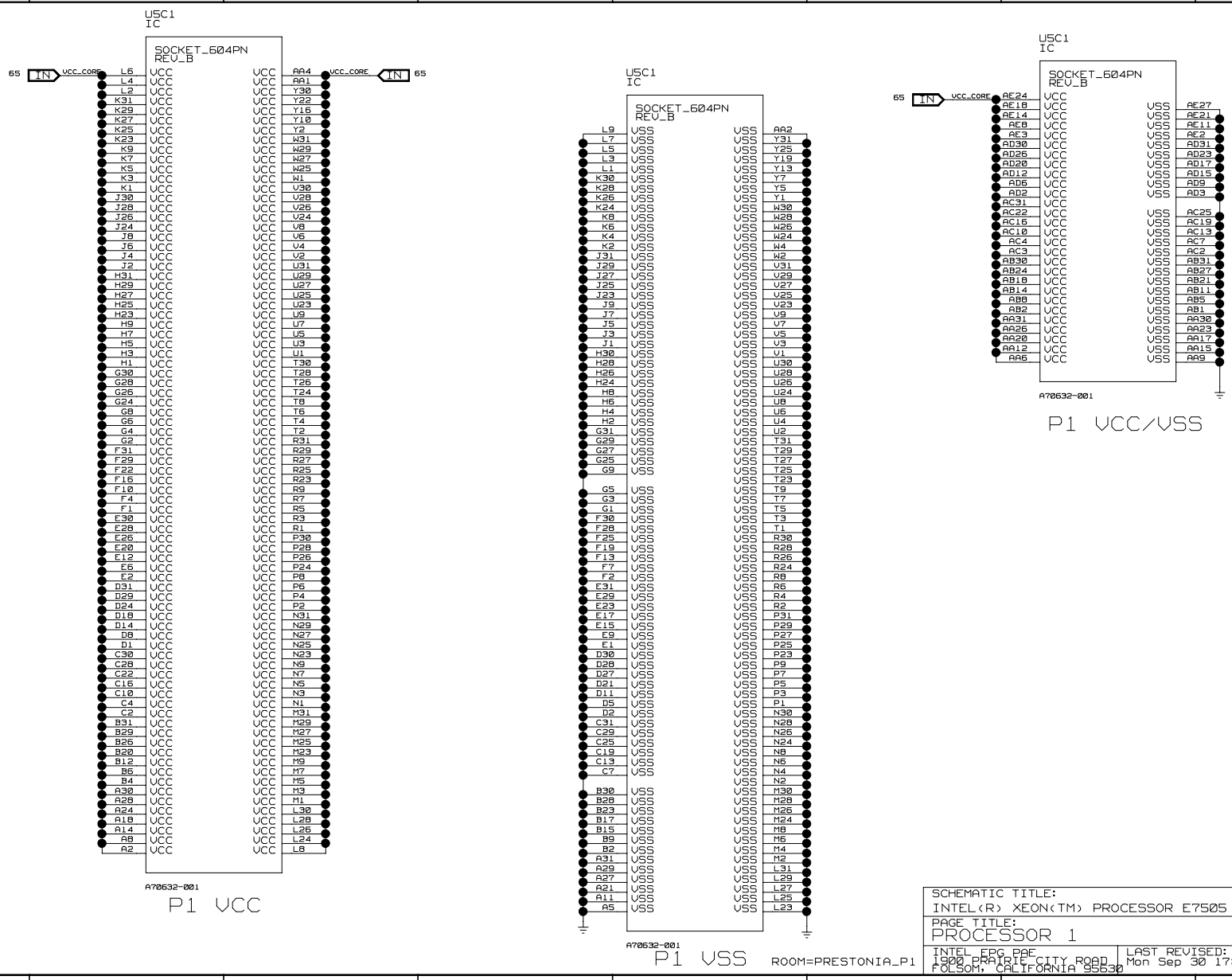




ROOM=PRESTONIA_P0

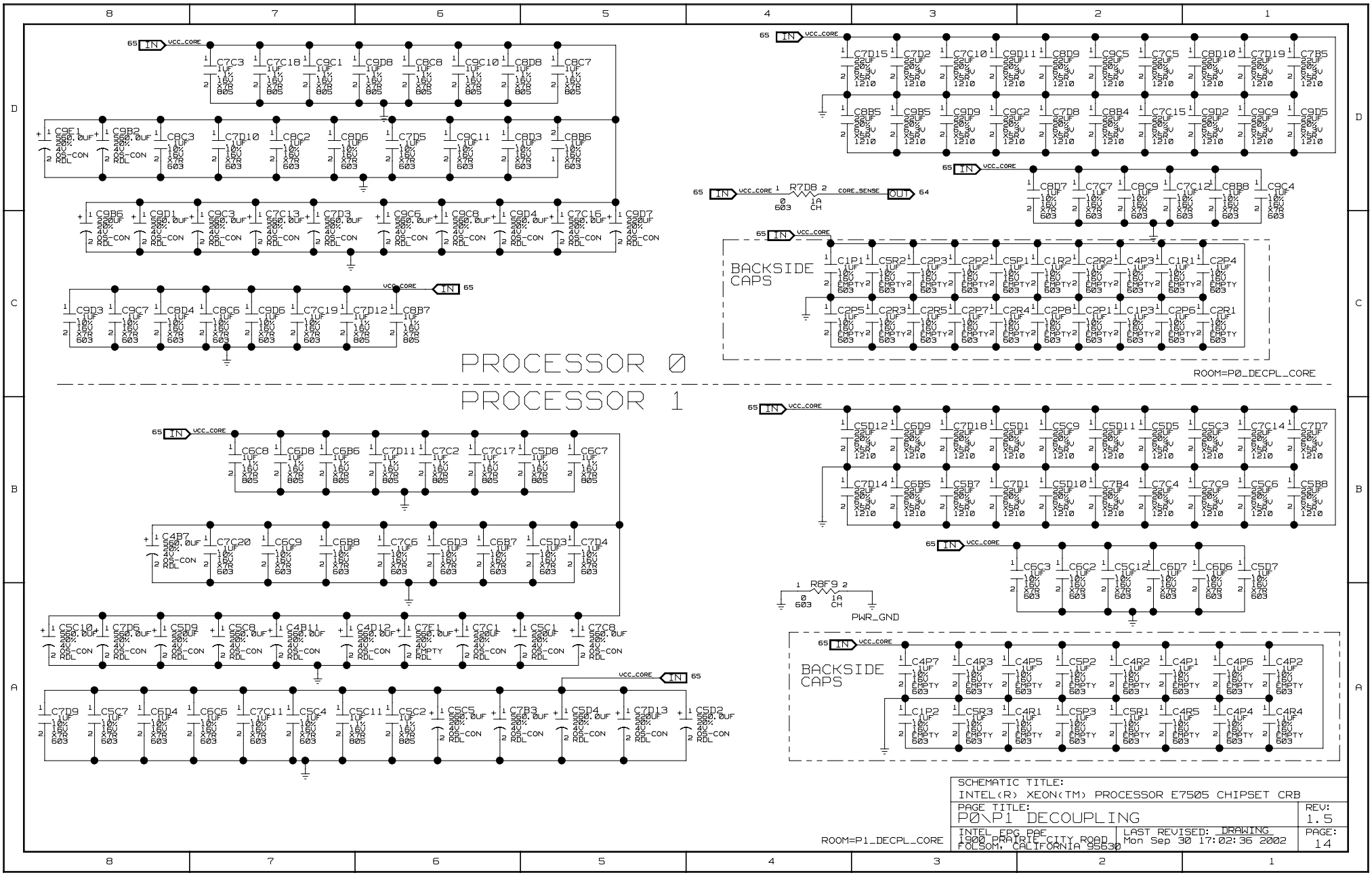
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB		
PAGE TITLE: PROCESSOR 0 / POWER		REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:34 2002	PAGE: 11


U5C1
IC
SOCKET_604PN
REV_B
MECH KEY
A70632-001
FSB_D_L<63,,0>
FSB_A_L<35,,3>
FSB_REQ_L<4,,0>
FSB_DBI_L<3,,0>
FSB_AP_L<1,,0>
FSB_DP_L<3,,0>
RSVD/THERMDC
RSVD/THERMDA
RSVD/SMB_PRT
RSVD/VCCVIDLB
RSVD/FORCEPR#
RSVD/VCCVID
VSS/BOOT_SELECT
VSS/SLEW_CTRL
VSS/TESTLOW
CPU_PWR_GD
*CAD NOTE:
PLACE CLOSE TO
PIN AB7
C5D6
68PF
50V
NPO
EMPTY
603
+3.3V
R5D1
R4H16
1K
5%
CH
603
SMBUS
CPU THERMAL SENSOR SMBUS = 32
CPU IDROM SMBUS = AA
R5C3
R5C6
49.9
1%
CH
603
BPRI
BR3
BR2
BR1
DEFER
RESET
RS2
RS1
RS0
RSP
TRDY
A20M
IGNNE
INIT
LINT1
LINT0
PWRGOOD
SMI
SLP
STPCLK
BCLK1
BCLK0
TCK
TDI
TMS
TRST
SM_EP_A2/RSVD
SM_EP_A1/RSVD
SM_EP_A0/RSVD
SM_TS1_A1/RSVD
SM_TS1_A0/RSVD
SM_CLK/RSVD
SM_WP/RSVD
BSEL1
BSEL0
VCCA
VCCIOPLL
VCCSENSE
VID4
VID3
VID2
VID1
VID0
VSSA
VSSSENSE
R7D2
R7D4
R7D6
1K
1%
CH
603
5%
J7B3
1X2HDR
102276-001
EMPTY
TEST HOOK
NEVER SHORT
CAD NOTE:
PLACE R FOR BPM NEXT TO P1
R7C7
IERR
ADS
BINIT
BNR
BPM5
BPM4
BPM3
BPM2
BPM1
BPM0
BR0
DBSY
DRDY
HIT
HITM
LOCK
MCERR
ADSTB1
ADSTB0
DSTBP3
DSTBP2
DSTBP1
DSTBP0
DSTBN3
DSTBN2
DSTBN1
DSTBN0
FERR
THRMTRIP
PROCHOT
TDO
SM_DAT/RSVD
SM_ALERT/RSVD
COMP1
COMP0
GTLREF3
GTLREF2
GTLREF1
GTLREF0
ODTEN
SKTOCC
TESTHI6
TESTHI5
TESTHI4
TESTHI3
TESTHI2
TESTHI1
TESTHI0
A70632-001
R5C1
R5B6
R5B5
R5B7
R5B4
R5B8
40.2
1%
R5E2
R5E1
R5D5
R5D4
R5D3
R5D2
R5C8
L5E1
4.70NH
IND
721891-008
L5D1
C5E1
33.0UF
20%
16V
TANT
7343
C5D13
R5E3
R5D6
CAD NOTE:
PLACE CAPS CLOSE TO
PINS AB4 AD4 AA5
CAD NOTE:
1 CAP PER PIN
C6C4
C6C1
C5D2
C5D5
220PF
10%
50V
X7R
603
R5C2
51
R7C6
R7D7
49.9
ROOM=PRESTONIA_P1
PINS | IXP* | FUTURE PROCESSOR
A4 | RSVD | VCCVID
A15 | RSVD | FORCEPR#
C1 | VSS | TESTLOW
C5 | RSVD | VCCVIDLB
G7 | VSS | BOOT_SELECT
AC30 | VSS | SLEW_CTRL
* INTEL(R) XEON(R) PROCESSOR WITH 512-KB L2 CACHE
PINS | 603 PIN SOCKET | 604 PIN SOCKET
AE30 | N/A | MECH KEY
Y29 | SM_TS1_A1 | RSVD
AA29 | SM_EP_A0 | RSVD
AA28 | SM_TS1_A0 | RSVD
AB28 | SM_EP_A2 | RSVD
AB29 | SM_EP_A1 | RSVD
AC28 | SM_CLK | RSVD
AC29 | SM_DAT | RSVD
AD28 | SM_ALERT# | RSVD
AD29 | SM_WP | RSVD
AE4 | RSVD | SMB_PRT
Y27 | RSVD | THERMDA
Y28 | RSVD | THERMDC
AE28 | SMVCC | VID_VCC
AE29 | SMVCC | VID_VCC
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
PROCESSOR 1 (P1)
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:34 2002
PAGE:
12

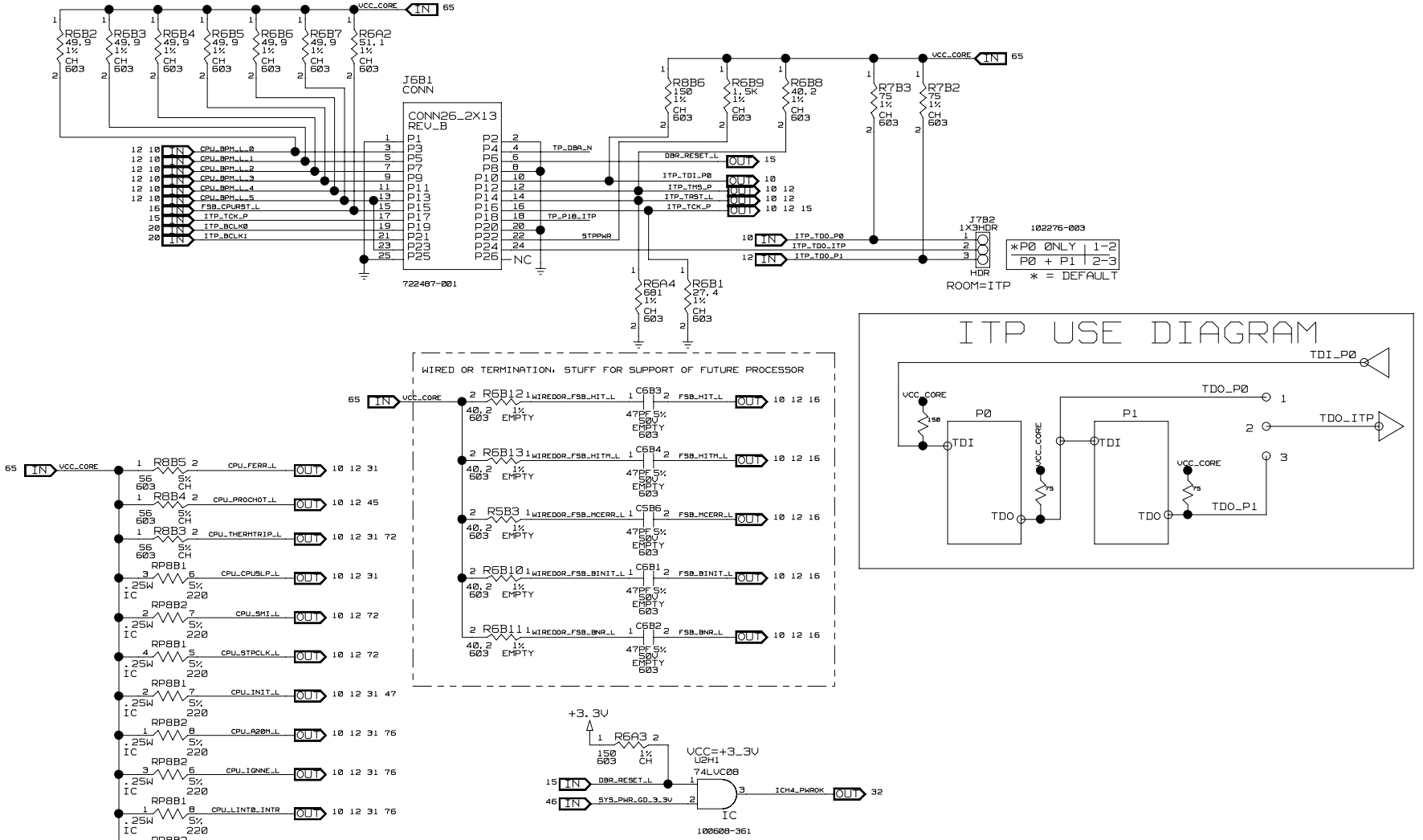


ROOM=PRESTONIA_P1

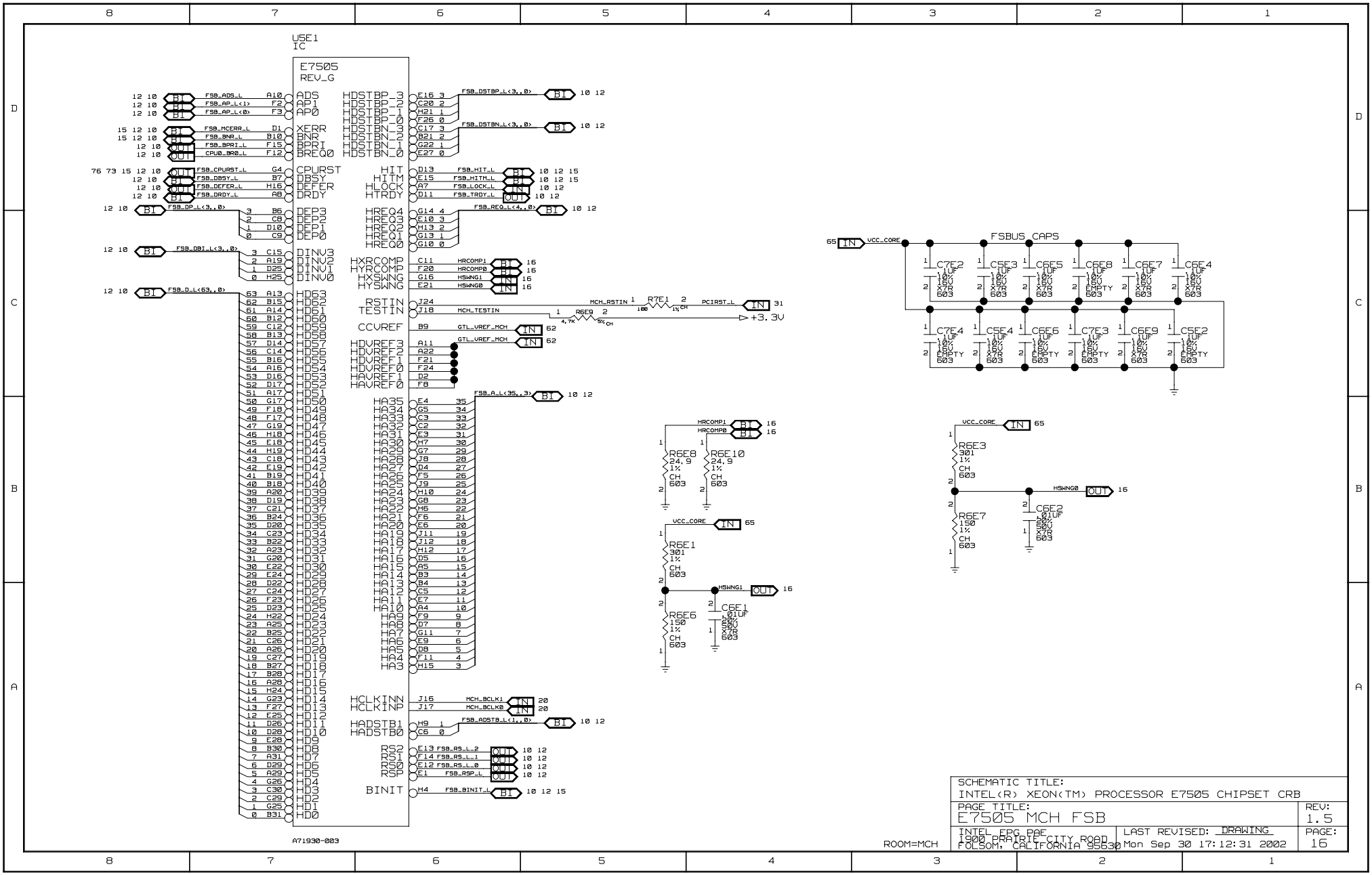
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB		
PAGE TITLE: PROCESSOR 1		REV: 1.5
INTEL_FPG_PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:35 2002	PAGE: 13

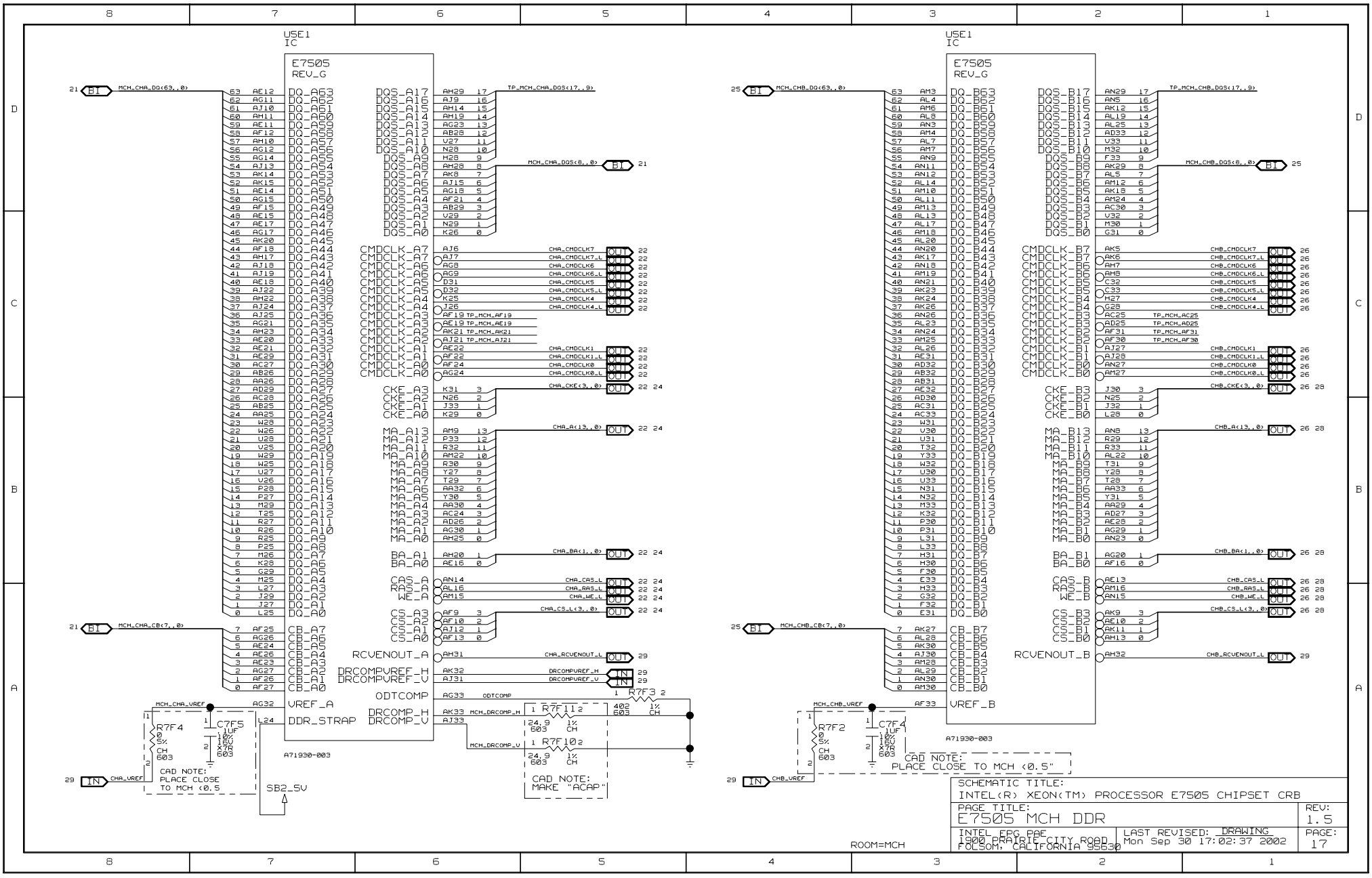


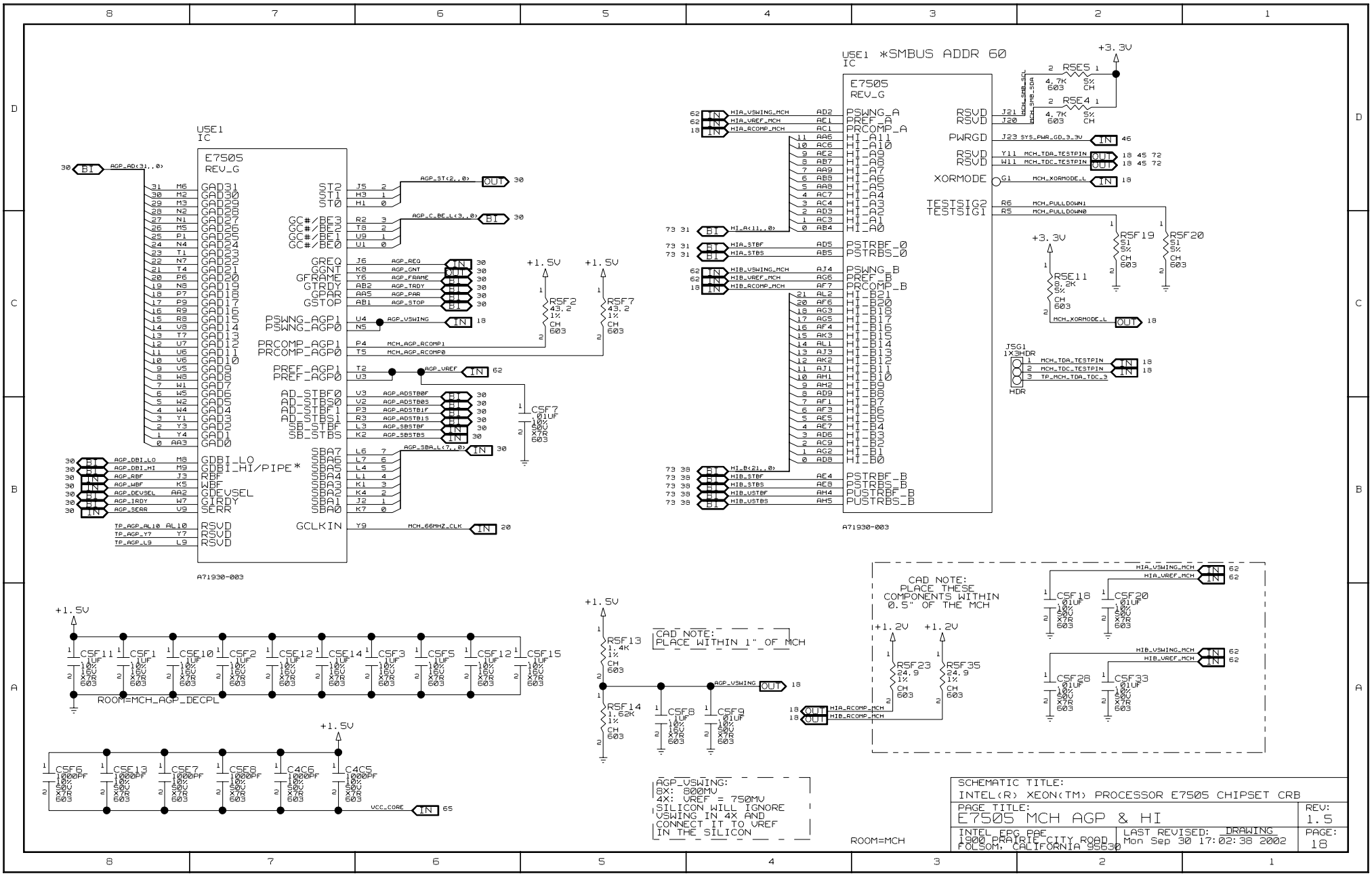
SCHEMATIC TITLE:	INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:	P0\P1 DECOUPLING
REV:	1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:36 2002
PAGE:	14

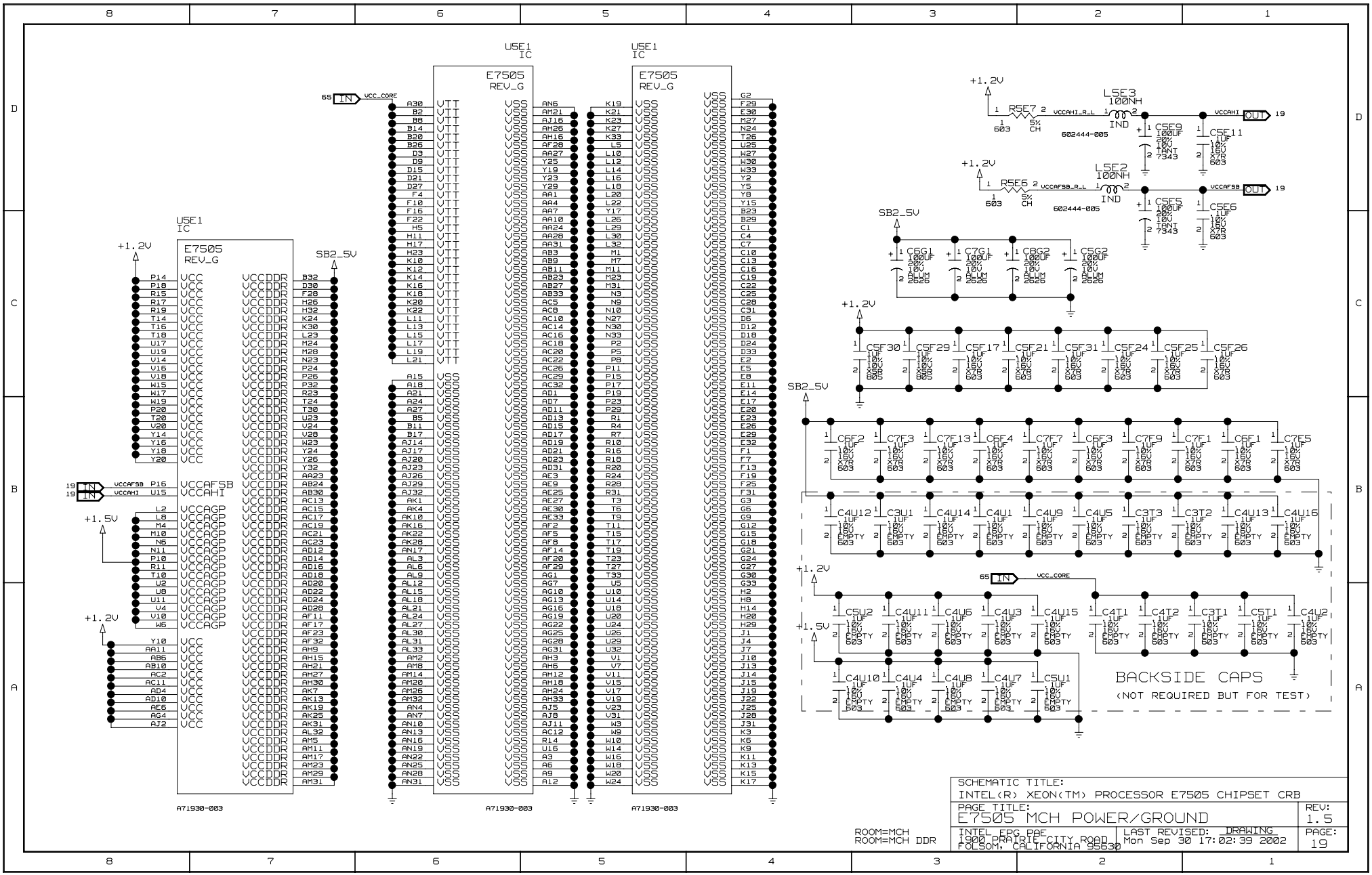


SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB		
PAGE TITLE: ITP, FUTURE PROCESSOR SUPPORT		REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:36 2002	PAGE: 15


USE1
IC
E7505
REV_G
FSB_ADS_L
FSB_AP_L<1>
FSB_AP_L<0>
FSB_MCERR_L
FSB_BNR_L
FSB_BPRI_L
CPU0_BR0_L
FSB_CPURST_L
FSB_DBSY_L
FSB_DEFER_L
FSB_DRDY_L
FSB_DP_L<3,,0>
FSB_DB1_L<3,,0>
FSB_D_L<63,,0>
FSB_DSTBP_L<3,,0>
FSB_DSTBN_L<3,,0>
FSB_HIT_L
FSB_HITM_L
FSB_LOCK_L
FSB_TRDY_L
FSB_REQ_L<4,,0>
HRCOMP1
HRCOMP0
HSWNG1
HSWNG0
MCH_RSTIN
PCIRST_L
MCH_TESTIN
+3.3V
GTL_VREF_MCH
FSB_A_L<35,,3>
MCH_BCLK1
MCH_BCLK0
FSB_ADSTB_L<1,,0>
FSB_RS_L_2
FSB_RS_L_1
FSB_RS_L_0
FSB_RSP_L
FSB_BINIT_L
FSBUS CAPS
VCC_CORE
R6E8
R6E10
R6E1
R6E6
R6E3
R6E7
C6E1
C6E2
C7F2
C5F3
C6F5
C6F8
C6F7
C6F4
C7F4
C5F4
C6F6
C7F3
C6F9
C5F2
A71930-003
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
E7505 MCH FSB
REV:
1.5
INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:12:31 2002
PAGE:
16
ROOM=MCH


USE1
IC
E7505
REV_G
MCH_CHA_DQ<63,,0>
DQ_A63
DQ_A62
DQ_A61
DQ_A60
DQ_A59
DQ_A58
DQ_A57
DQ_A56
DQ_A55
DQ_A54
DQ_A53
DQ_A52
DQ_A51
DQ_A50
DQ_A49
DQ_A48
DQ_A47
DQ_A46
DQ_A45
DQ_A44
DQ_A43
DQ_A42
DQ_A41
DQ_A40
DQ_A39
DQ_A38
DQ_A37
DQ_A36
DQ_A35
DQ_A34
DQ_A33
DQ_A32
DQ_A31
DQ_A30
DQ_A29
DQ_A28
DQ_A27
DQ_A26
DQ_A25
DQ_A24
DQ_A23
DQ_A22
DQ_A21
DQ_A20
DQ_A19
DQ_A18
DQ_A17
DQ_A16
DQ_A15
DQ_A14
DQ_A13
DQ_A12
DQ_A11
DQ_A10
DQ_A9
DQ_A8
DQ_A7
DQ_A6
DQ_A5
DQ_A4
DQ_A3
DQ_A2
DQ_A1
DQ_A0
MCH_CHA_CB<7,,0>
CB_A7
CB_A6
CB_A5
CB_A4
CB_A3
CB_A2
CB_A1
CB_A0
MCH_CHA_VREF
VREF_A
DDR_STRAP
R7F4
C7F5
CAD NOTE:
PLACE CLOSE
TO MCH <0.5
CHA_VREF
SB2_SV
A71930-003
DQS_A17
DQS_A16
DQS_A15
DQS_A14
DQS_A13
DQS_A12
DQS_A11
DQS_A10
DQS_A8
DQS_A7
DQS_A6
DQS_A5
DQS_A4
DQS_A3
DQS_A2
DQS_A1
DQS_A0
TP_MCH_CHA_DQS<17,,9>
MCH_CHA_DQS<8,,0>
CMDCLK_A7
CMDCLK_A7_L
CMDCLK_A6
CMDCLK_A6_L
CMDCLK_A5
CMDCLK_A5_L
CMDCLK_A4
CMDCLK_A4_L
CMDCLK_A3
CMDCLK_A3_L
CMDCLK_A2
CMDCLK_A2_L
CMDCLK_A1
CMDCLK_A1_L
CMDCLK_A0
CMDCLK_A0_L
CHA_CMDCLK7
CHA_CMDCLK7_L
CHA_CMDCLK6
CHA_CMDCLK6_L
CHA_CMDCLK5
CHA_CMDCLK5_L
CHA_CMDCLK4
CHA_CMDCLK4_L
TP_MCH_AF19
TP_MCH_AE19
TP_MCH_AK21
TP_MCH_AJ21
CHA_CMDCLK1
CHA_CMDCLK1_L
CHA_CMDCLK0
CHA_CMDCLK0_L
CKE_A3
CKE_A2
CKE_A1
CKE_A0
CHA_CKE<3,,0>
MA_A13
MA_A12
MA_A11
MA_A10
MA_A9
MA_A8
MA_A7
MA_A6
MA_A5
MA_A4
MA_A3
MA_A2
MA_A1
MA_A0
CHA_A<13,,0>
BA_A1
BA_A0
CHA_BA<1,,0>
CAS_A
RAS_A
WE_A
CHA_CAS_L
CHA_RAS_L
CHA_WE_L
CS_A3
CS_A2
CS_A1
CS_A0
CHA_CS_L<3,,0>
RCVENOUT_A
CHA_RCVENOUT_L
DRCOMPVREF_H
DRCOMPVREF_V
DRCOMPVREF_H
DRCOMPVREF_V
ODTCOMP
ODTCOMP
DRCOMP_H
DRCOMP_V
MCH_DRCOMP_H
MCH_DRCOMP_V
R7F11
R7F10
R7F3
24.9 1% 603
402 1% 603
CAD NOTE:
MAKE "ACAP"
MCH_CHB_DQ<63,,0>
DQ_B63
DQ_B62
DQ_B61
DQ_B60
DQ_B59
DQ_B58
DQ_B57
DQ_B56
DQ_B55
DQ_B54
DQ_B53
DQ_B52
DQ_B51
DQ_B50
DQ_B49
DQ_B48
DQ_B47
DQ_B46
DQ_B45
DQ_B44
DQ_B43
DQ_B42
DQ_B41
DQ_B40
DQ_B39
DQ_B38
DQ_B37
DQ_B36
DQ_B35
DQ_B34
DQ_B33
DQ_B32
DQ_B31
DQ_B30
DQ_B29
DQ_B28
DQ_B27
DQ_B26
DQ_B25
DQ_B24
DQ_B23
DQ_B22
DQ_B21
DQ_B20
DQ_B19
DQ_B18
DQ_B17
DQ_B16
DQ_B15
DQ_B14
DQ_B13
DQ_B12
DQ_B11
DQ_B10
DQ_B9
DQ_B8
DQ_B7
DQ_B6
DQ_B5
DQ_B4
DQ_B3
DQ_B2
DQ_B1
DQ_B0
MCH_CHB_CB<7,,0>
CB_B7
CB_B6
CB_B5
CB_B4
CB_B3
CB_B2
CB_B1
CB_B0
MCH_CHB_VREF
VREF_B
R7F2
C7F4
CAD NOTE:
PLACE CLOSE TO MCH <0.5"
CHB_VREF
A71930-003
DQS_B17
DQS_B16
DQS_B15
DQS_B14
DQS_B13
DQS_B12
DQS_B11
DQS_B10
DQS_B9
DQS_B8
DQS_B7
DQS_B6
DQS_B5
DQS_B4
DQS_B3
DQS_B2
DQS_B1
DQS_B0
TP_MCH_CHB_DQS<17,,9>
MCH_CHB_DQS<8,,0>
CMDCLK_B7
CMDCLK_B7_L
CMDCLK_B6
CMDCLK_B6_L
CMDCLK_B5
CMDCLK_B5_L
CMDCLK_B4
CMDCLK_B4_L
CMDCLK_B3
CMDCLK_B3_L
CMDCLK_B2
CMDCLK_B2_L
CMDCLK_B1
CMDCLK_B1_L
CMDCLK_B0
CMDCLK_B0_L
CHB_CMDCLK7
CHB_CMDCLK7_L
CHB_CMDCLK6
CHB_CMDCLK6_L
CHB_CMDCLK5
CHB_CMDCLK5_L
CHB_CMDCLK4
CHB_CMDCLK4_L
TP_MCH_AC25
TP_MCH_AD25
TP_MCH_AF31
TP_MCH_AF30
CHB_CMDCLK1
CHB_CMDCLK1_L
CHB_CMDCLK0
CHB_CMDCLK0_L
CKE_B3
CKE_B2
CKE_B1
CKE_B0
CHB_CKE<3,,0>
MA_B13
MA_B12
MA_B11
MA_B10
MA_B9
MA_B8
MA_B7
MA_B6
MA_B5
MA_B4
MA_B3
MA_B2
MA_B1
MA_B0
CHB_A<13,,0>
BA_B1
BA_B0
CHB_BA<1,,0>
CAS_B
RAS_B
WE_B
CHB_CAS_L
CHB_RAS_L
CHB_WE_L
CS_B3
CS_B2
CS_B1
CS_B0
CHB_CS_L<3,,0>
RCVENOUT_B
CHB_RCVENOUT_L
ROOM=MCH
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
E7505 MCH DDR
REV:
1.5
INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:37 2002
PAGE:
17


USE1
IC
E7505
REV_G
AGP_AD<31..0>
GAD31
GAD30
GAD29
GAD28
GAD27
GAD26
GAD25
GAD24
GAD23
GAD22
GAD21
GAD20
GAD19
GAD18
GAD17
GAD16
GAD15
GAD14
GAD13
GAD12
GAD11
GAD10
GAD9
GAD8
GAD7
GAD6
GAD5
GAD4
GAD3
GAD2
GAD1
GAD0
AGP_ST<2..0>
ST2
ST1
ST0
AGP_C_BE_L<3..0>
GC#/BE3
GC#/BE2
GC#/BE1
GC#/BE0
GREQ
GGNT
GFRAME
GTRDY
GSTOP
PSWNG_AGP1
PSWNG_AGP0
PRCOMP_AGP1
PRCOMP_AGP0
PREF_AGP1
PREF_AGP0
AD_STBF0
AD_STBS0
AD_STBF1
AD_STBS1
SB_STBF
SB_STBS
AGP_SBA_L<7..0>
SBA7
SBA6
SBA5
SBA4
SBA3
SBA2
SBA1
SBA0
GCLKIN
AGP_REQ
AGP_GNT
AGP_FRAME
AGP_TRDY
AGP_PAR
AGP_STOP
AGP_VSWING
MCH_AGP_RCOMP1
MCH_AGP_RCOMP0
AGP_VREF
AGP_ADSTB0F
AGP_ADSTB0S
AGP_ADSTB1F
AGP_ADSTB1S
AGP_SBSTBF
AGP_SBSTBS
MCH_66MHZ_CLK
AGP_DBI_LO
AGP_DBI_HI
AGP_RBF
AGP_WBF
AGP_DEVSEL
AGP_IRDY
AGP_SERR
GDBI_LO
GDBI_HI/PIPE*
RBF
WBF
GDEVSEL
GIRDY
SERR
TP_AGP_AL10
TP_AGP_Y7
TP_AGP_L9
RSVD
R5F2
R5F7
C5F7
A71930-003
USE1 *SMBUS ADDR 60
HIA_VSWING_MCH
HIA_VREF_MCH
HIA_RCOMP_MCH
HI_A<11..0>
HIA_STBF
HIA_STBS
HIB_VSWING_MCH
HIB_VREF_MCH
HIB_RCOMP_MCH
HI_B<21..0>
HIB_STBF
HIB_STBS
HIB_USTBF
HIB_USTBS
PSWNG_A
PREF_A
PRCOMP_A
PSTRBF_0
PSTRBS_0
PSWNG_B
PREF_B
PRCOMP_B
PSTRBF_B
PSTRBS_B
PUSTRBF_B
PUSTRBS_B
+3.3V
R5E5
R5E4
4.7K
603
5%
CH
MCH_SMB_SCL
MCH_SMB_SDA
RSVD
PWRGD
SYS_PWR_GD_3_3V
MCH_TDA_TESTPIN
MCH_TDC_TESTPIN
XORMODE
MCH_XORMODE_L
TESTSIG2
TESTSIG1
MCH_PULLDOWN1
MCH_PULLDOWN0
R5F19
R5F20
R5E11
8.2K
JSG1
1X3HDR
HDR
TP_MCH_TDA_TDC_3
A71930-003
+1.5V
C5F11
C5F1
C5F10
C5F2
C5F12
C5F14
C5F3
C5F5
C5F12
C5F15
1UF
10%
10V
X7R
603
ROOM=MCH_AGP_DECPL
C5F6
C5F13
C5F7
C5F8
C4C6
C4C5
1000PF
50V
VCC_CORE
R5F13
1.4K
1%
CH
603
CAD NOTE:
PLACE WITHIN 1" OF MCH
R5F14
1.62K
C5F8
C5F9
.01UF
AGP_VSWING
HIA_RCOMP_MCH
HIB_RCOMP_MCH
CAD NOTE:
PLACE THESE
COMPONENTS WITHIN
0.5" OF THE MCH
+1.2V
R5F23
R5F35
24.9
C5F18
C5F20
C5F28
C5F33
AGP_VSWING:
8X: 800MV
4X: VREF = 750MV
SILICON WILL IGNORE
VSWING IN 4X AND
CONNECT IT TO VREF
IN THE SILICON
ROOM=MCH
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
E7505 MCH AGP & HI
REV:
1.5
INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:38 2002
PAGE:
18



SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
E7505 MCH POWER/GROUND

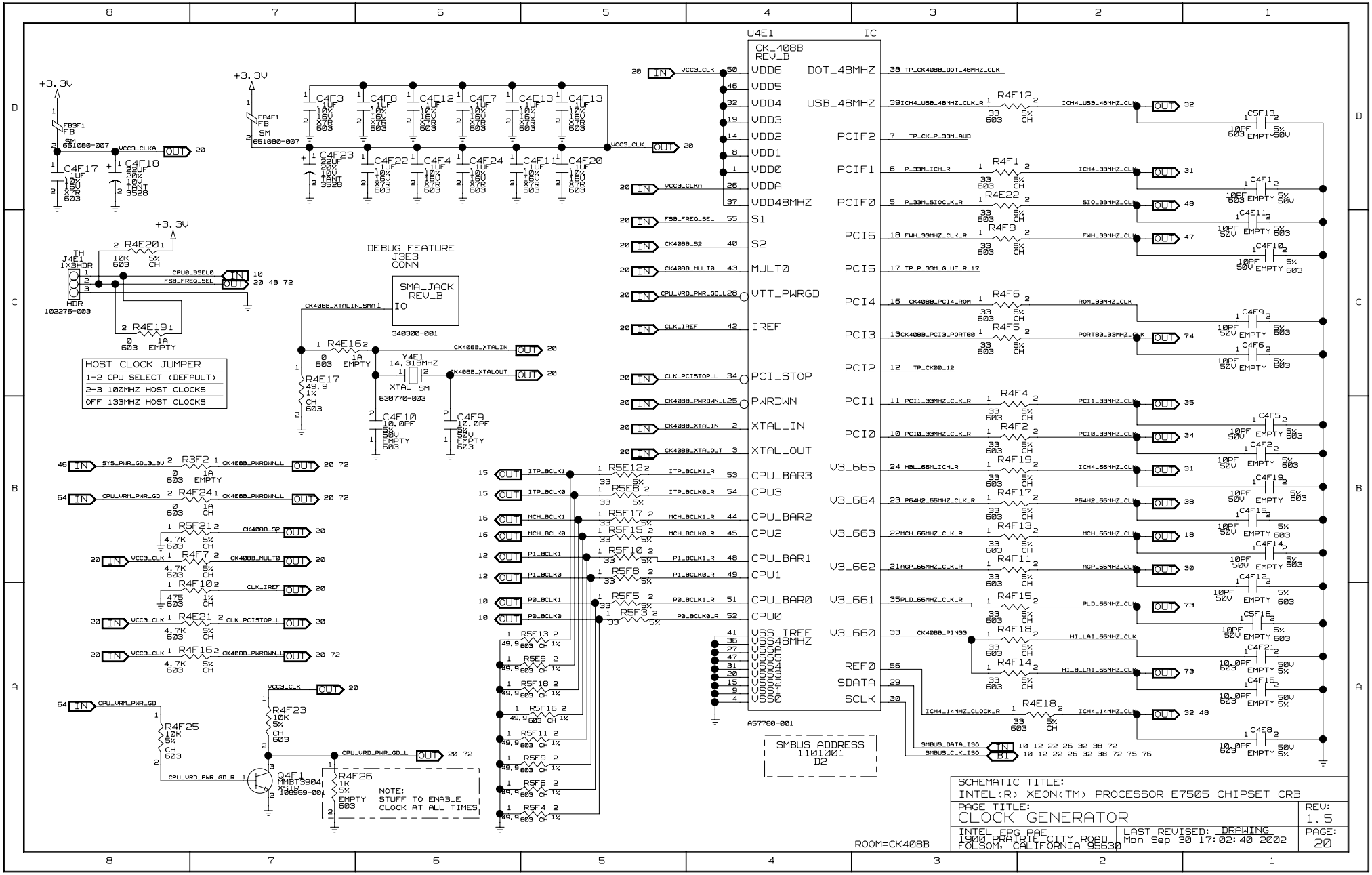
REV: 1.5

INTEL_FPG_PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

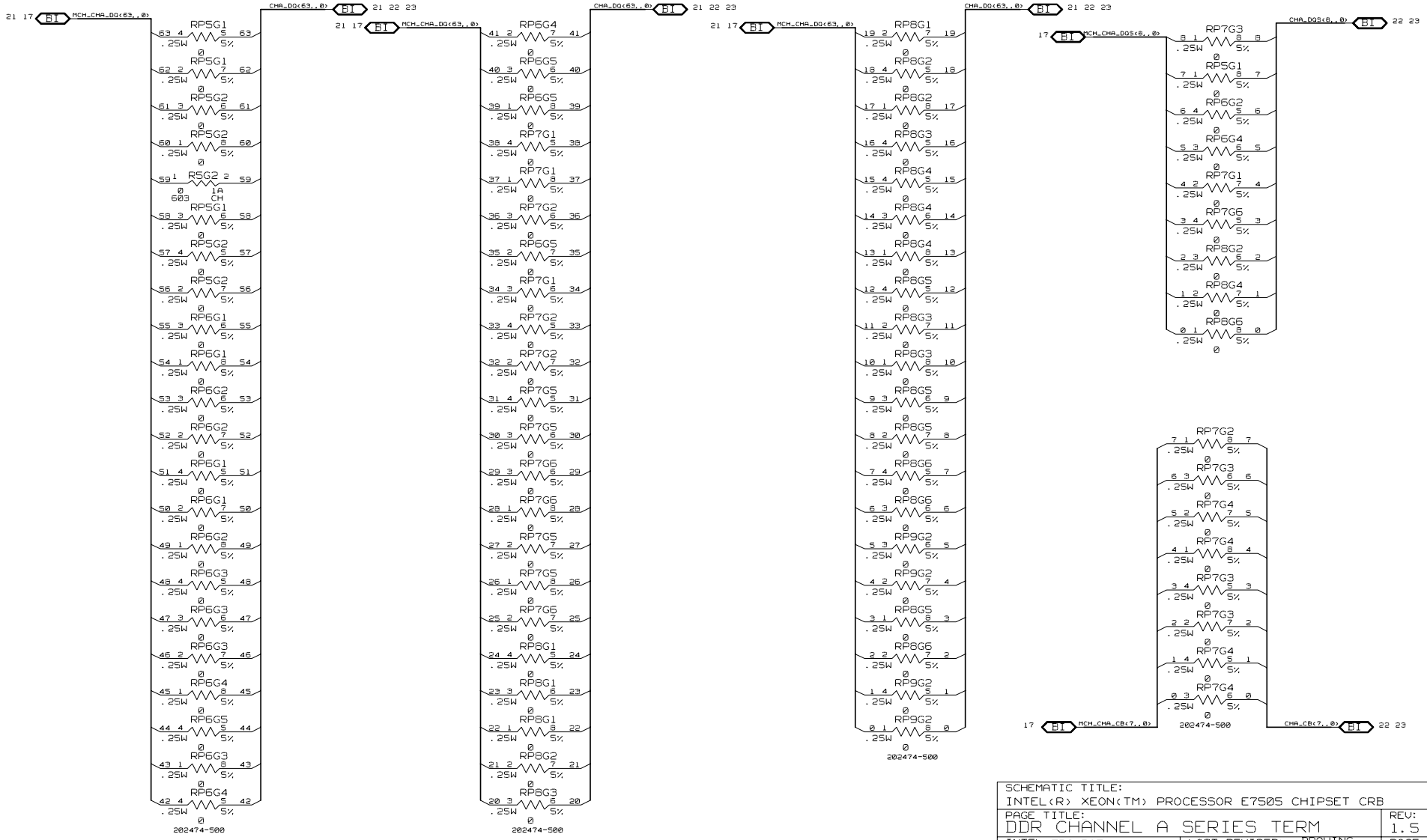
LAST REVISED: DRAWING
Mon Sep 30 17:02:39 2002

PAGE: 19

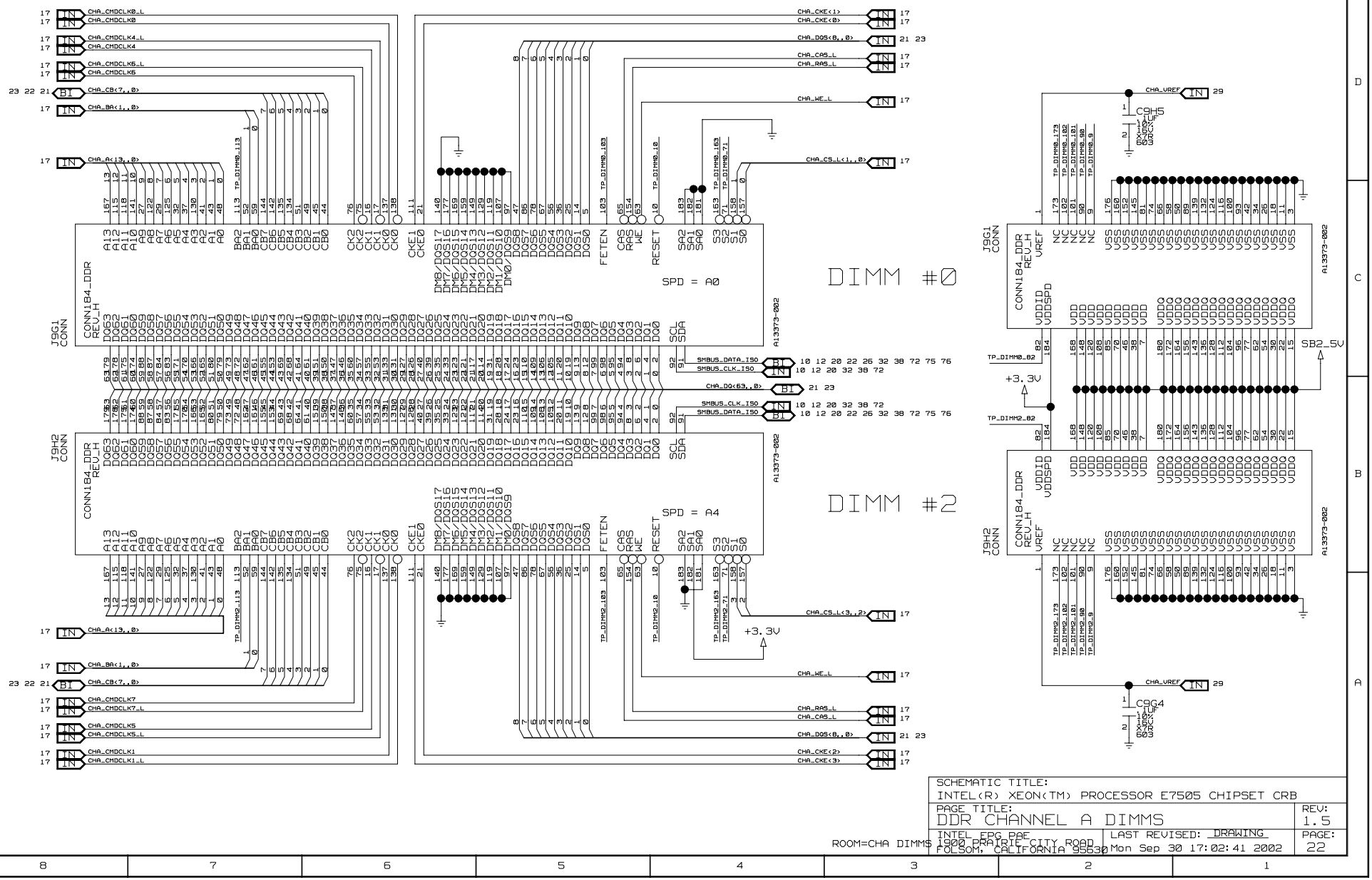
ROOM=MCH
ROOM=MCH DDR

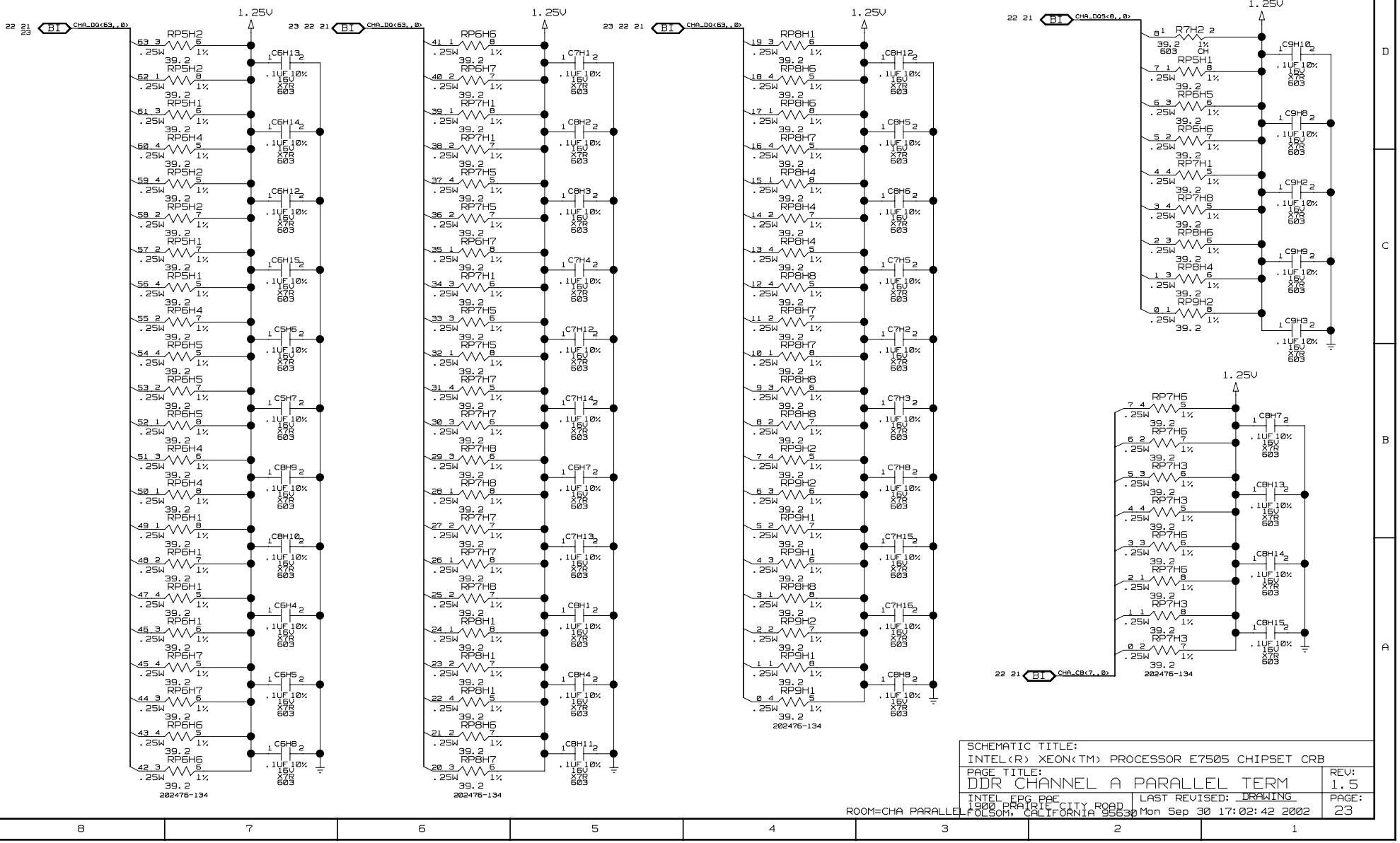

U4E1
IC
CK_408B
REV_B
VDD6
VDD5
VDD4
VDD3
VDD2
VDD1
VDD0
VDDA
VDD48MHZ
S1
S2
MULT0
VTT_PWRGD
IREF
PCI_STOP
PWRDWN
XTAL_IN
XTAL_OUT
CPU_BAR3
CPU3
CPU_BAR2
CPU2
CPU_BAR1
CPU1
CPU_BAR0
CPU0
VSS_IREF
VSS48MHZ
VSS5
VSS4
VSS3
VSS2
VSS1
VSS0
DOT_48MHZ
USB_48MHZ
PCIF2
PCIF1
PCIF0
PCI6
PCI5
PCI4
PCI3
PCI2
PCI1
PCI0
V3_665
V3_664
V3_663
V3_662
V3_661
V3_660
REF0
SDATA
SCLK
A57780-001
+3.3V
HOST CLOCK JUMPER
1-2 CPU SELECT (DEFAULT)
2-3 100MHZ HOST CLOCKS
OFF 133MHZ HOST CLOCKS
DEBUG FEATURE
J3E3
CONN
SMA_JACK
REV_B
340300-001
SMBUS ADDRESS
1101001
D2
ROOM=CK408B
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
CLOCK GENERATOR
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:40 2002
PAGE:
20

NOTE: ZERO OHM RESISTORS NOT REQUIRED (FOR TEST PURPOSES)



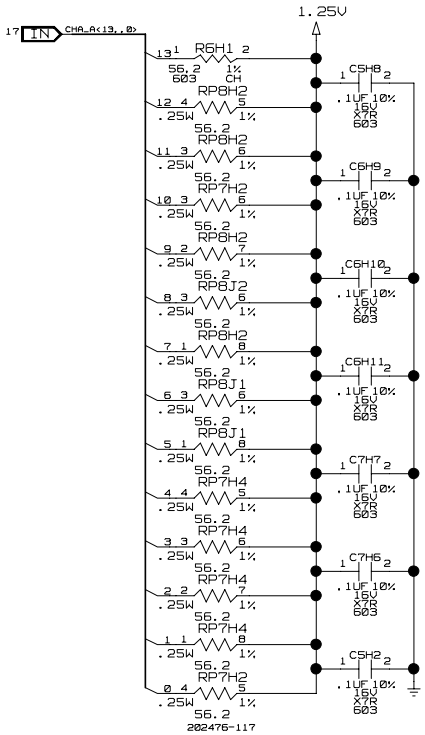
SCHEMATIC TITLE:	INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:	DDR CHANNEL A SERIES TERM
REV:	1.5
INTEL FPG PAE	ROOM=CHA SERIES
1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	
LAST REVISED: DRAWING	Mon Sep 30 17:02:40 2002
PAGE:	21

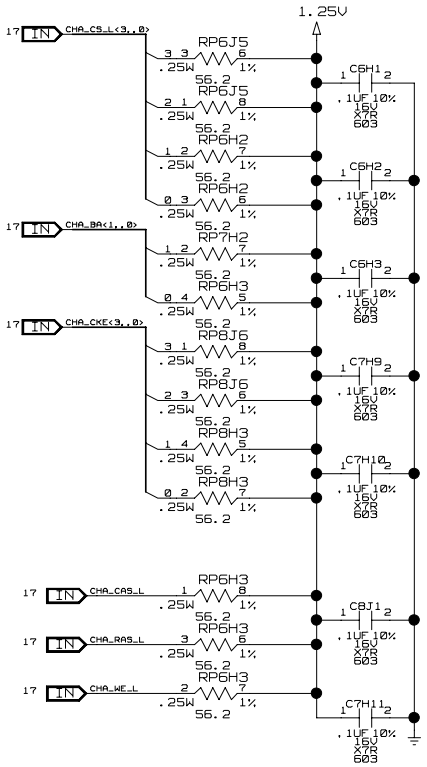

DIMM #0
DIMM #2
SPD = A0
SPD = A4
J9G1 CONN
J9H2 CONN
CONN184_DDR REV_H
A13373-002
CHA_CMDCLK0_L
CHA_CMDCLK0
CHA_CMDCLK4_L
CHA_CMDCLK4
CHA_CMDCLK6_L
CHA_CMDCLK6
CHA_CB<7,,0>
CHA_BA<1,,0>
CHA_A<13,,0>
CHA_CKE<1>
CHA_CKE<0>
CHA_DQS<8,,0>
CHA_CAS_L
CHA_RAS_L
CHA_WE_L
CHA_CS_L<1,,0>
CHA_CS_L<3,,2>
CHA_DQ<63,,0>
SMBUS_DATA_ISO
SMBUS_CLK_ISO
CHA_CMDCLK7
CHA_CMDCLK7_L
CHA_CMDCLK5
CHA_CMDCLK5_L
CHA_CMDCLK1
CHA_CMDCLK1_L
CHA_CKE<2>
CHA_CKE<3>
+3.3V
CHA_VREF
C9H5
C9G4
1uF
SB2_5V
ROOM=CHA DIMMS
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
DDR CHANNEL A DIMMS
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:41 2002
PAGE:
22



SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB		
PAGE TITLE: DDR CHANNEL A PARALLEL TERM		REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:42 2002	PAGE: 23

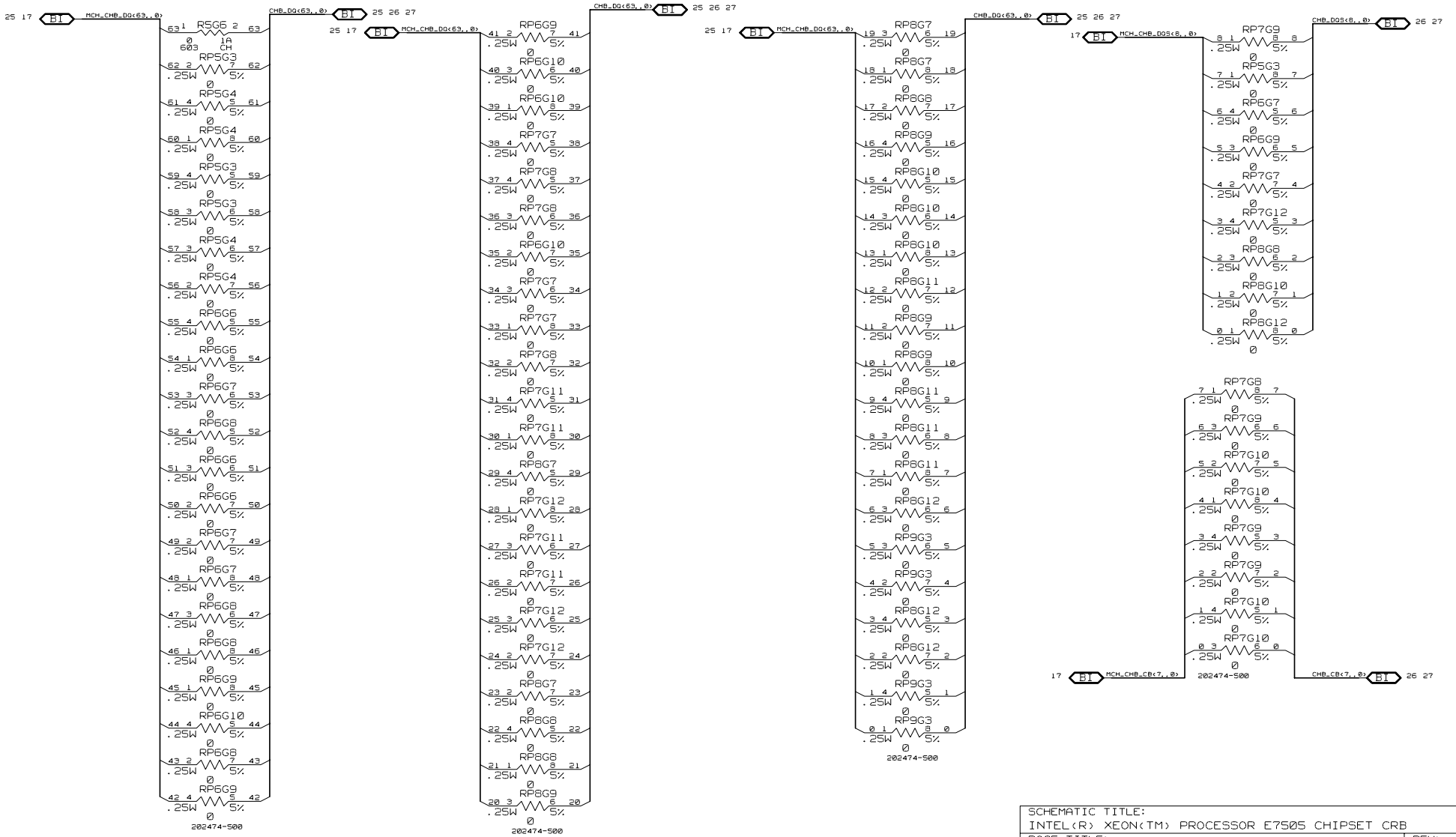
ROOM=CHA PARALLEL





SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB		
PAGE TITLE: DDR CHANNEL A PARALLEL TERM		REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:43 2002	PAGE: 24

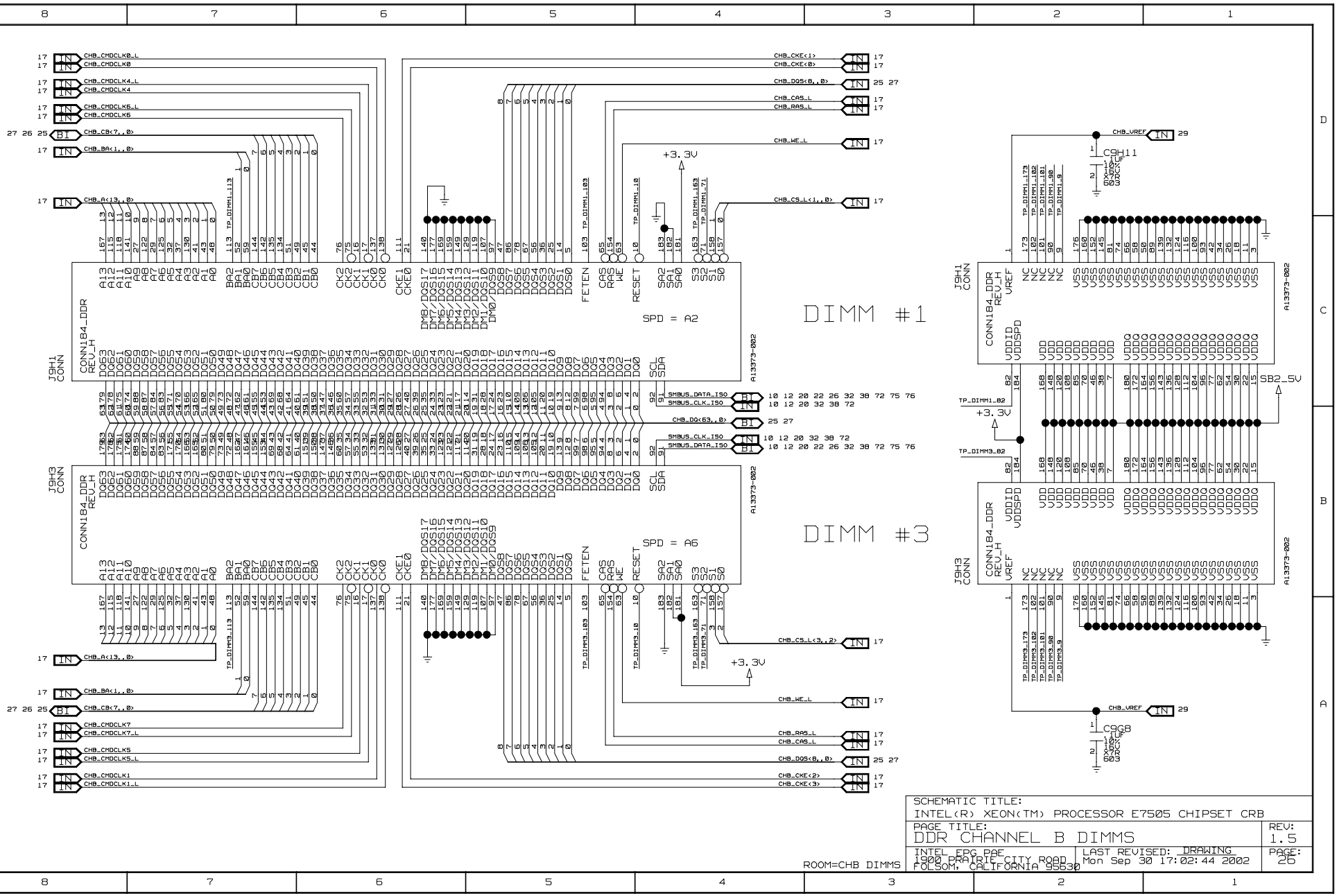
ROOM=CHA PARALLEL

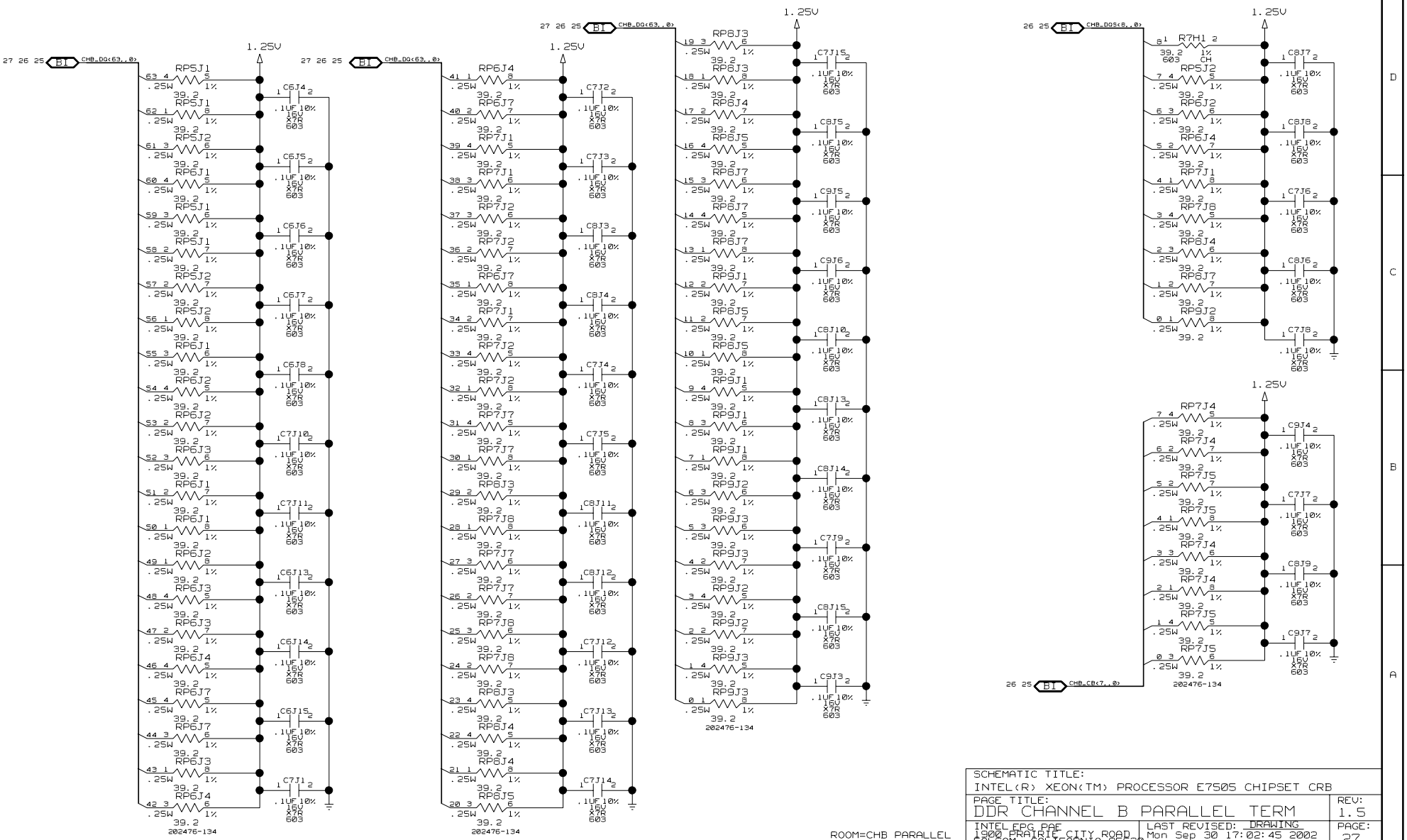


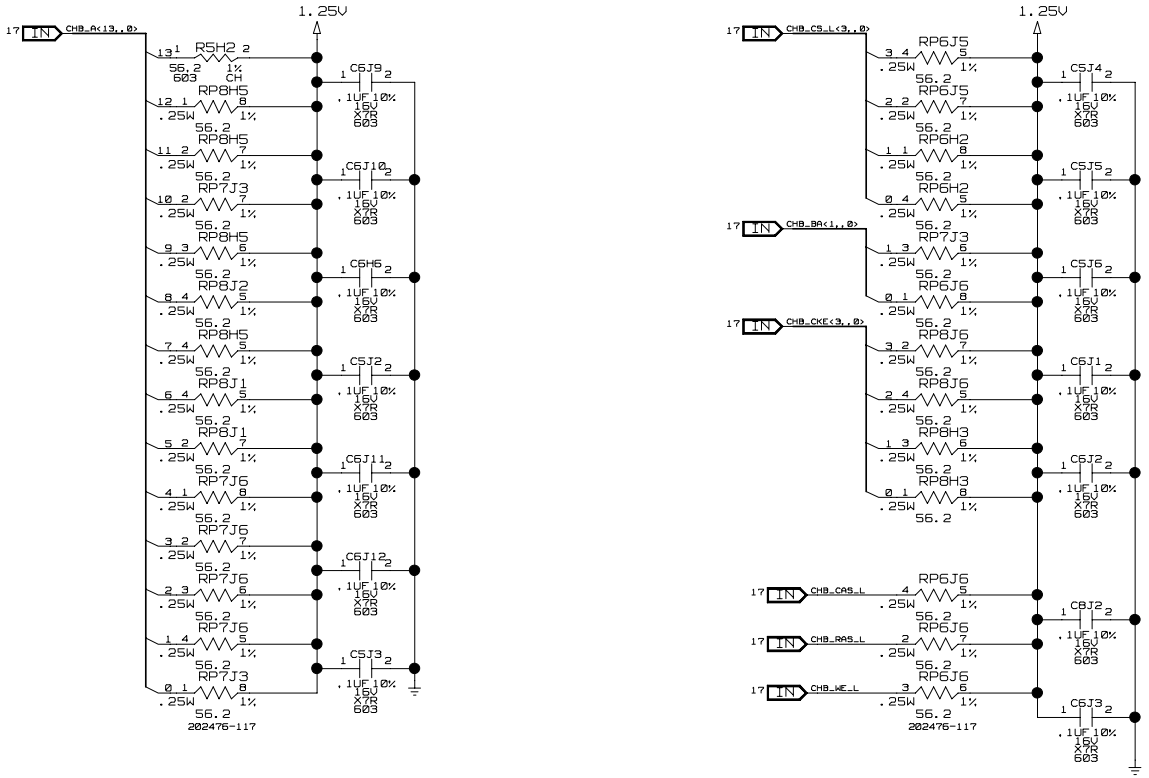
NOTE: ZERO OHM RESISTORS NOT REQUIRED (FOR TEST PURPOSES)

ROOM=CHB SERIES

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB		
PAGE TITLE: DDR CHANNEL B SERIES TERM		REV: 1.5
INTEL EPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:43 2002	PAGE: 25

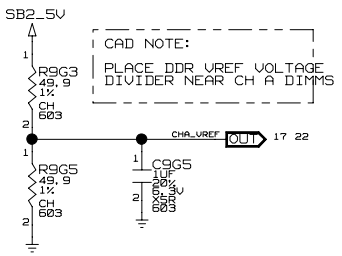

DIMM #1
DIMM #3
SPD = A2
SPD = A6
J9H1 CONN
J9H3 CONN
CONN184_DDR REV_H
CHB_CMDCLK0_L
CHB_CMDCLK0
CHB_CMDCLK4_L
CHB_CMDCLK4
CHB_CMDCLK6_L
CHB_CMDCLK6
CHB_CB<7,,0>
CHB_BA<1,,0>
CHB_A<13,,0>
CHB_CMDCLK7
CHB_CMDCLK7_L
CHB_CMDCLK5
CHB_CMDCLK5_L
CHB_CMDCLK1
CHB_CMDCLK1_L
CHB_CKE<1>
CHB_CKE<0>
CHB_DQS<8,,0>
CHB_CAS_L
CHB_RAS_L
CHB_WE_L
CHB_CS_L<1,,0>
CHB_CS_L<3,,2>
CHB_DQ<63,,0>
SMBUS_DATA_ISO
SMBUS_CLK_ISO
+3.3V
CHB_VREF
SB2_5V
A13373-002
ROOM=CHB DIMMS
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
DDR CHANNEL B DIMMS
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:44 2002
PAGE:
26

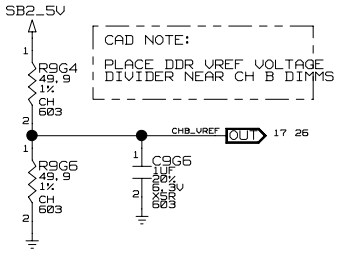

1.25V
CMB_DQ<63..0>
RP5J1
RP5J2
RP6J1
RP6J2
RP6J3
RP6J4
RP6J7
RP7J1
RP7J2
RP7J6
RP7J7
RP7J8
RP8J3
RP8J4
RP8J5
RP8J7
RP9J1
RP9J2
RP9J3
C6J4
C6J5
C6J6
C6J7
C6J8
C7J10
C7J11
C6J13
C6J14
C6J15
C7J1
C7J2
C7J3
C8J3
C8J4
C7J4
C7J5
C8J11
C8J12
C7J12
C7J13
C7J14
C7J15
C8J5
C9J5
C9J6
C8J10
C8J13
C8J14
C7J9
C8J15
C9J3
R7H1
CMB_DQS<8..0>
RP7J4
RP7J5
CMB_CB<7..0>
C8J7
C8J8
C7J6
C8J6
C7J8
C9J4
C7J7
C8J9
C9J7
202476-134
ROOM=CHB PARALLEL
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
DDR CHANNEL B PARALLEL TERM
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:45 2002
PAGE:
27



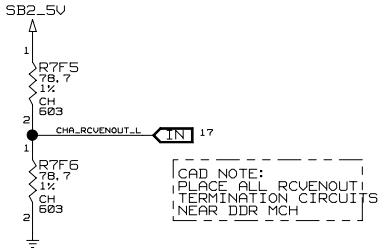
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB		
PAGE TITLE: DDR CHANNEL B PARALLEL TERM		REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:45 2002	PAGE: 28

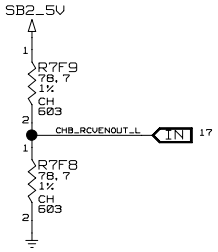
ROOM=CHB PARALLEL





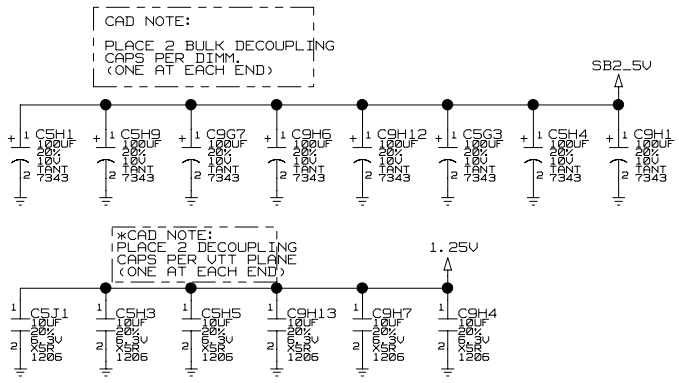
CHANNEL VREFS

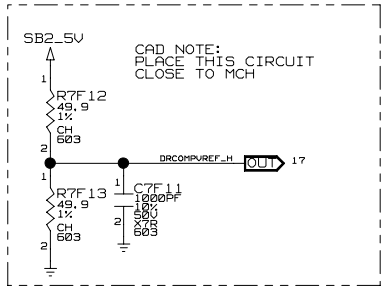




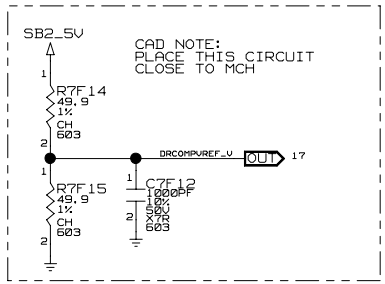
RCVENOUT TERMINATION

DDR DECOUPLING



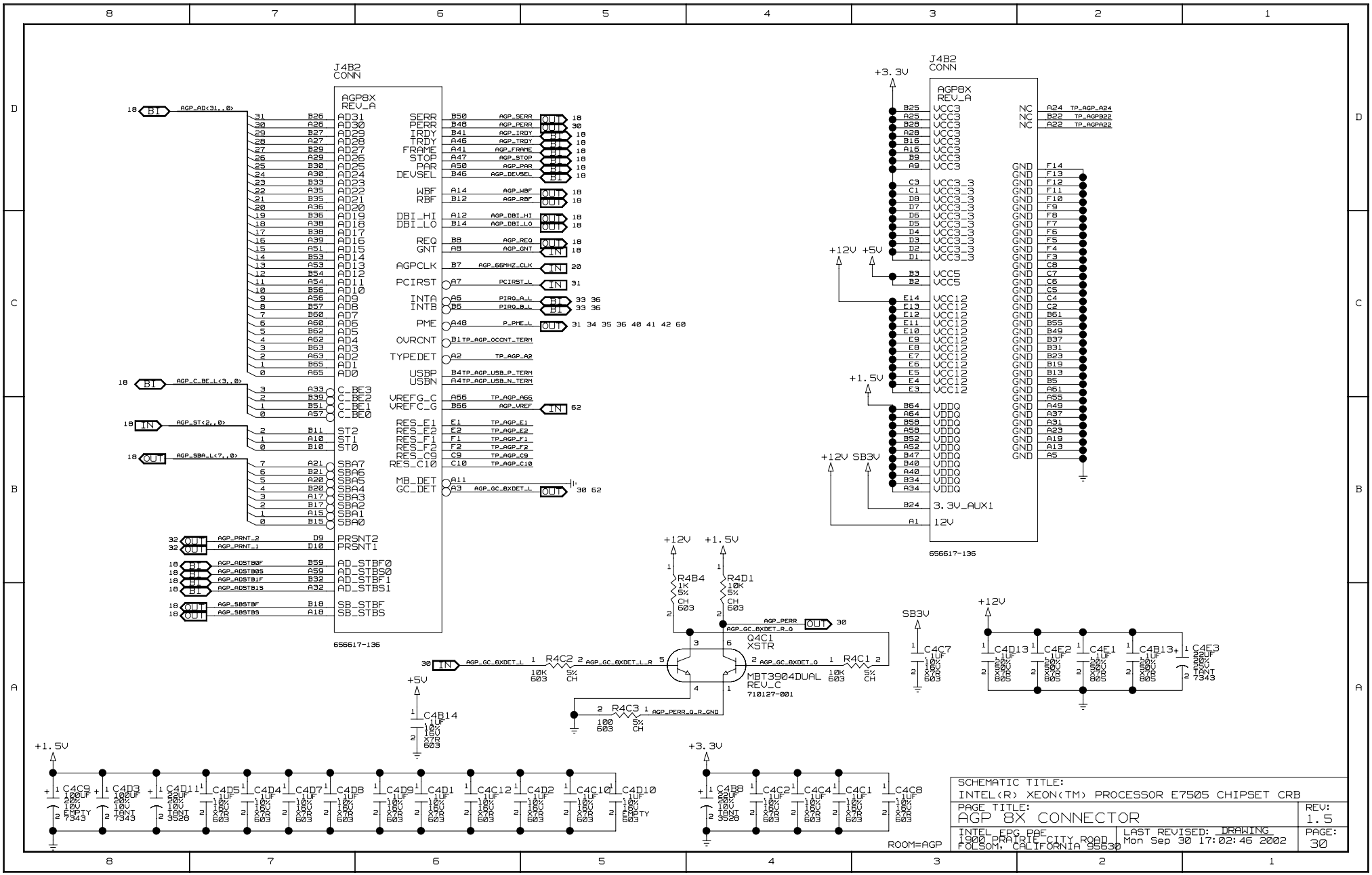


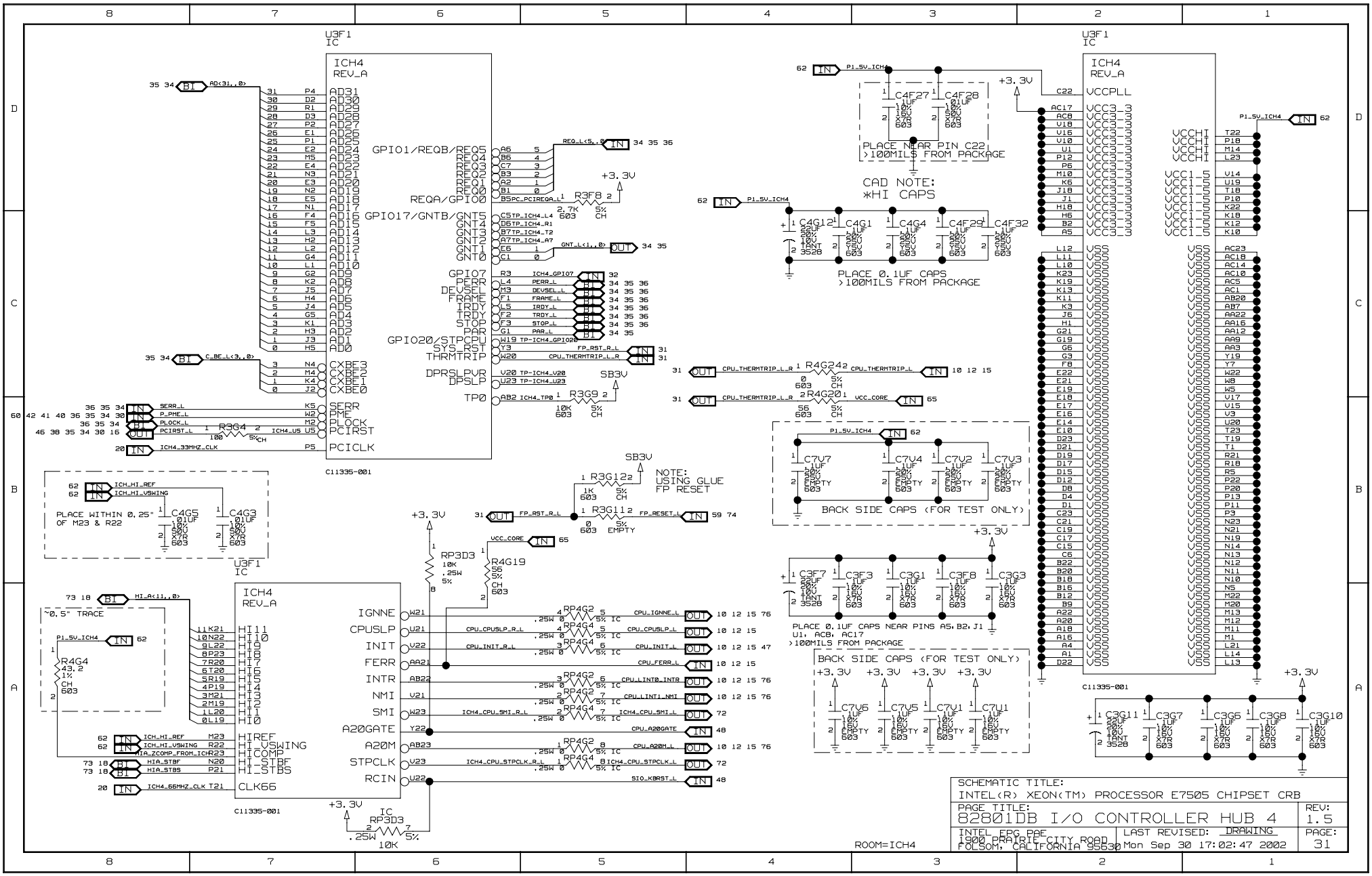
COMPENSATION VREFS

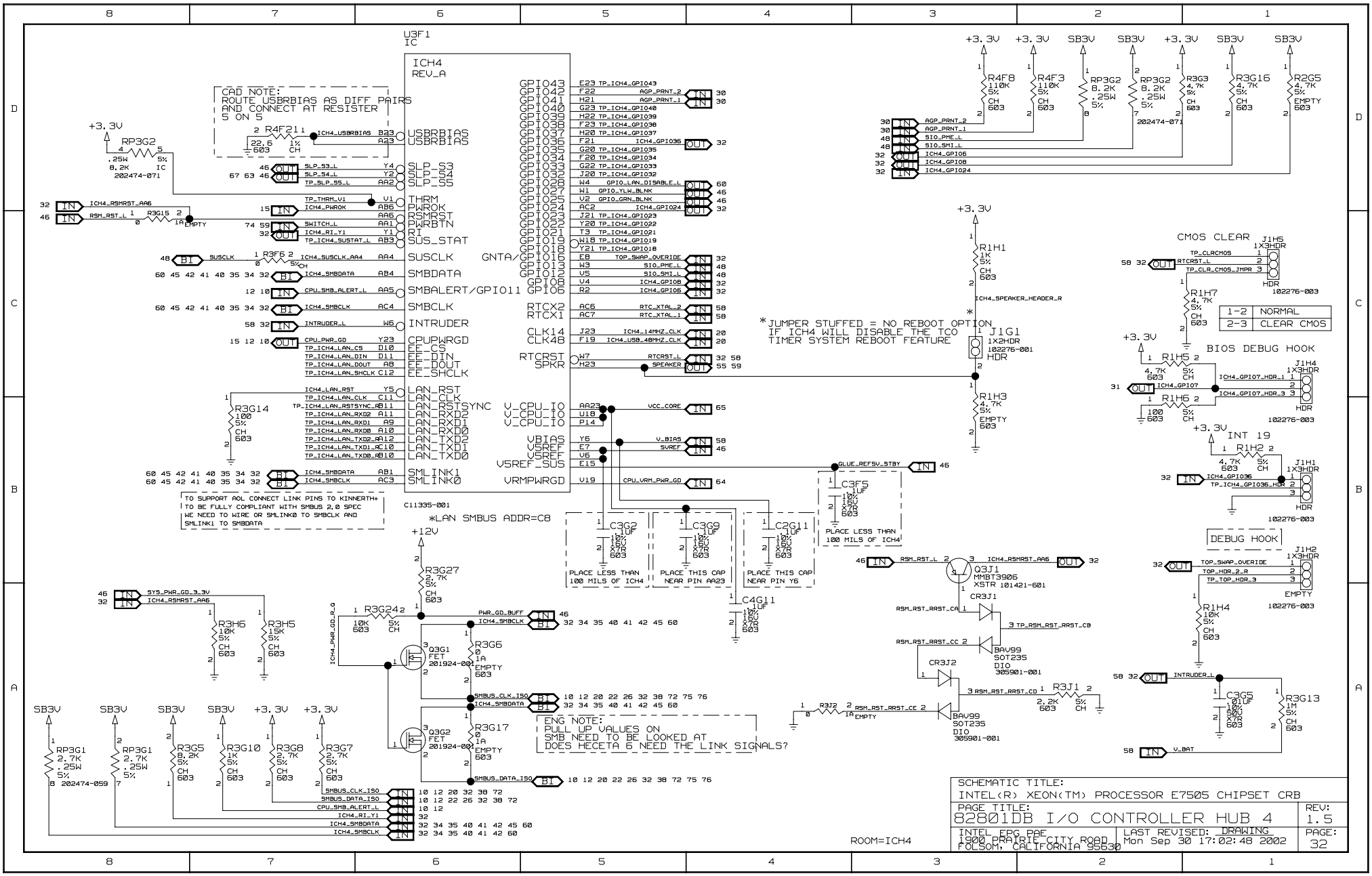


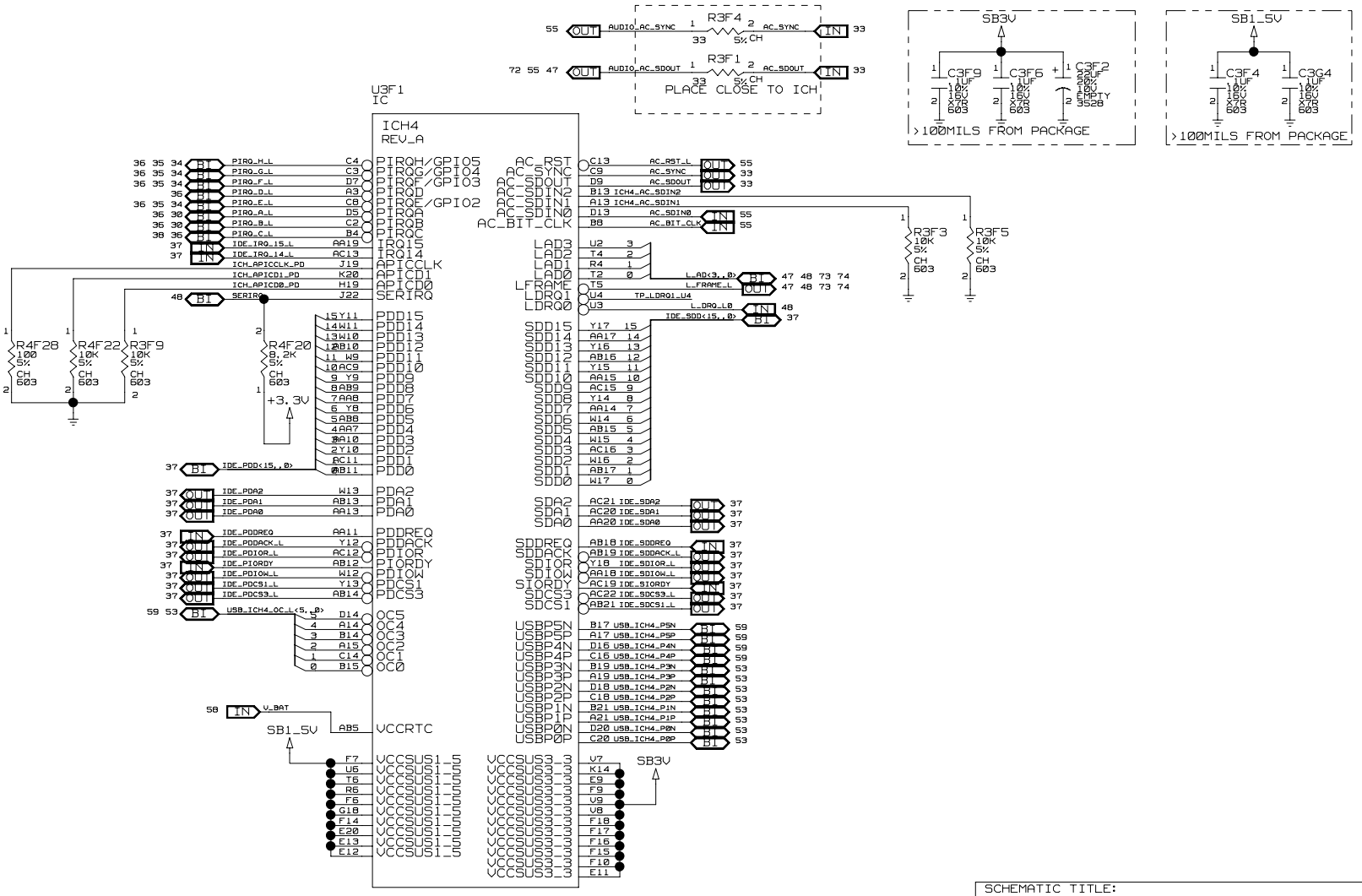
ROOM=CHA DIMMS
ROOM=CHB DIMMS
ROOM=MCH DDR

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB		
PAGE TITLE: DDR VREFS AND DECOUPLING		REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:46 2002	PAGE: 29


J4B2
CONN
AGP8X
REV_A
656617-136
R4B4
1K
5%
CH
603
R4D1
10K
5%
CH
603
Q4C1
XSTR
MBT3904DUAL
REV_C
7101127-001
R4C2
10K
603
5%
CH
R4C1
10K
603
5%
CH
R4C3
100
603
5%
CH
C4B14
1UF
10%
16V
X7R
603
C4C7
1UF
10%
16V
X7R
603
C4D13
1UF
10%
50V
X7R
805
C4E2
1UF
10%
50V
X7R
805
C4E1
1UF
10%
50V
X7R
805
C4B13
1UF
10%
50V
X7R
805
C4E3
22UF
20%
10V
TANT
7343
C4C9
100UF
20%
10V
ELTY
7343
C4D3
100UF
20%
10V
TANT
7343
C4D11
22UF
20%
10V
TANT
3528
C4D5
C4D4
C4D7
C4D8
C4D9
C4D1
C4C12
C4D2
C4C10
C4D10
C4B8
22UF
20%
10V
TANT
3528
C4C2
C4C4
C4C1
C4C8
ROOM=AGP
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
AGP 8X CONNECTOR
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:46 2002
PAGE:
30


U3F1
IC
ICH4
REV_A
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
GPIO1/REQB/REQ5
REQ4
REQ3
REQ2
REQ1
REQA/GPIO0
GPIO17/GNTB/GNT5
GNT4
GNT3
GNT2
GNT1
GNT0
GPIO7
PERR
DEVSEL
FRAME
IRDY
TRDY
STOP
PAR
GPIO20/STPCPU
SYS_RST
THRMTRIP
DPRSLPVR
DPSLP
TP0
CXBE3
CXBE2
CXBE1
CXBE0
SERR
PME
PLOCK
PCIRST
PCICLK
C11335-001
R3G64
R3F8
2.7K
R3G9
10K
SB3V
+3.3V
REQ_L<5,.0>
GNT_L<1,.0>
AD<31,.0>
C_BE_L<3,.0>
ICH4_33MHZ_CLK
NOTE:
USING GLUE
FP RESET
R3G122
R3G112
FP_RESET_L
FP_RST_R_L
VCC_CORE
RP3D3
R4G19
IC
RP3D3
10K
.25W
5%
HI_A<1,.0>
~0.5" TRACE
R4G4
43.2
1%
CH
603
HI11
HI10
HI9
HI8
HI7
HI6
HI5
HI4
HI3
HI2
HI1
HI0
HIREF
HI_VSWING
HICOMP
HI_STBF
HI_STBS
CLK66
ICH_HI_REF
ICH_HI_VSWING
HIA_ZCOMP_FROM_ICH
HIA_STBF
HIA_STBS
ICH4_66MHZ_CLK
C11335-001
IGNNE
CPUSLP
INIT
FERR
INTR
NMI
SMI
A20GATE
A20M
STPCLK
RCIN
CPU_IGNNE_L
CPU_CPUSLP_L
CPU_INIT_L
CPU_FERR_L
CPU_LINT0_INTR
CPU_LINT1_NMI
ICH4_CPU_SMI_L
CPU_A20GATE
CPU_A20M_L
ICH4_CPU_STPCLK_L
SIO_KBRST_L
PLACE WITHIN 0.25"
OF M23 & R22
C4G5
C4G3
.01UF
50V
X7R
603
P1_5V_ICH4
PLACE NEAR PIN C22
>100MILS FROM PACKAGE
CAD NOTE:
*HI CAPS
C4F27
C4F28
C4G12
C4G1
C4G4
C4F29
C4F32
PLACE 0.1UF CAPS
>100MILS FROM PACKAGE
R4G242
R4G201
CPU_THERMTRIP_L_R
CPU_THERMTRIP_L
VCC_CORE
BACK SIDE CAPS (FOR TEST ONLY)
C7V7
C7V4
C7V2
C7V3
C3F7
C3F3
C3G1
C3F8
C3G3
PLACE 0.1UF CAPS NEAR PINS A5, B2, J1
U1, AC8, AC17
>100MILS FROM PACKAGE
C7V6
C7V5
C7V1
C7U1
VCCPLL
VCC3_3
VCCHI
VCC1_5
VSS
C3G11
C3G7
C3G6
C3G8
C3G10
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
82801DB I/O CONTROLLER HUB 4
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:47 2002
PAGE:
31
ROOM=ICH4


U3F1
IC
ICH4
REV_A
CAD NOTE:
ROUTE USBRBIAS AS DIFF PAIRS
AND CONNECT AT RESISTER
5 ON 5
USBRBIAS
USBRBIAS
SLP_S3
SLP_S4
SLP_S5
THRM
PWROK
RSMRST
PWRBTN
RI
SUS_STAT
SUSCLK
SMBDATA
SMBALERT/GPIO11
SMBCLK
INTRUDER
CPUPWRGD
EE_CS
EE_DIN
EE_DOUT
EE_SHCLK
LAN_RST
LAN_CLK
LAN_RSTSYNC
LAN_RXD2
LAN_RXD1
LAN_RXD0
LAN_TXD2
LAN_TXD1
LAN_TXD0
SML_LINK1
SML_LINK0
GPIO43
GPIO42
GPIO41
GPIO40
GPIO39
GPIO38
GPIO37
GPIO36
GPIO35
GPIO34
GPIO33
GPIO32
GPIO28
GPIO27
GPIO25
GPIO24
GPIO23
GPIO22
GPIO21
GPIO19
GPIO18
GNTA/GPIO16
GPIO13
GPIO12
GPIO8
GPIO6
RTCX2
RTCX1
CLK14
CLK48
RTCRST
SPKR
V_CPU_IO
V_CPU_IO
V_CPU_IO
VBIAS
V5REF
V5REF
V5REF_SUS
VRMPWRGD
GLUE_REF5V_STBY
C11335-001
TO SUPPORT AOL CONNECT LINK PINS TO KINNERTH+
TO BE FULLY COMPLIANT WITH SMBUS 2.0 SPEC
WE NEED TO WIRE OR SMLINK0 TO SMBCLK AND
SMLINK1 TO SMBDATA
*LAN SMBUS ADDR=C8
PLACE LESS THAN
100 MILS OF ICH4
PLACE THIS CAP
NEAR PIN AA23
PLACE THIS CAP
NEAR PIN Y6
PLACE LESS THAN
100 MILS OF ICH4
ENG NOTE:
PULL UP VALUES ON
SMB NEED TO BE LOOKED AT
DOES HECETA 6 NEED THE LINK SIGNALS?
*JUMPER STUFFED = NO REBOOT OPTION
IF ICH4 WILL DISABLE THE TCO
TIMER SYSTEM REBOOT FEATURE
1-2 NORMAL
2-3 CLEAR CMOS
CMOS CLEAR
BIOS DEBUG HOOK
INT 19
DEBUG HOOK
Q3J1
MMBT3906
XSTR 101421-601
CR3J1
CR3J2
BAV99
SOT23S
DIO
305901-001
Q3G1
Q3G2
FET
201924-001
ROOM=ICH4
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
82801DB I/O CONTROLLER HUB 4
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:48 2002
PAGE:
32



SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
82801DB I/O CONTROLLER HUB 4

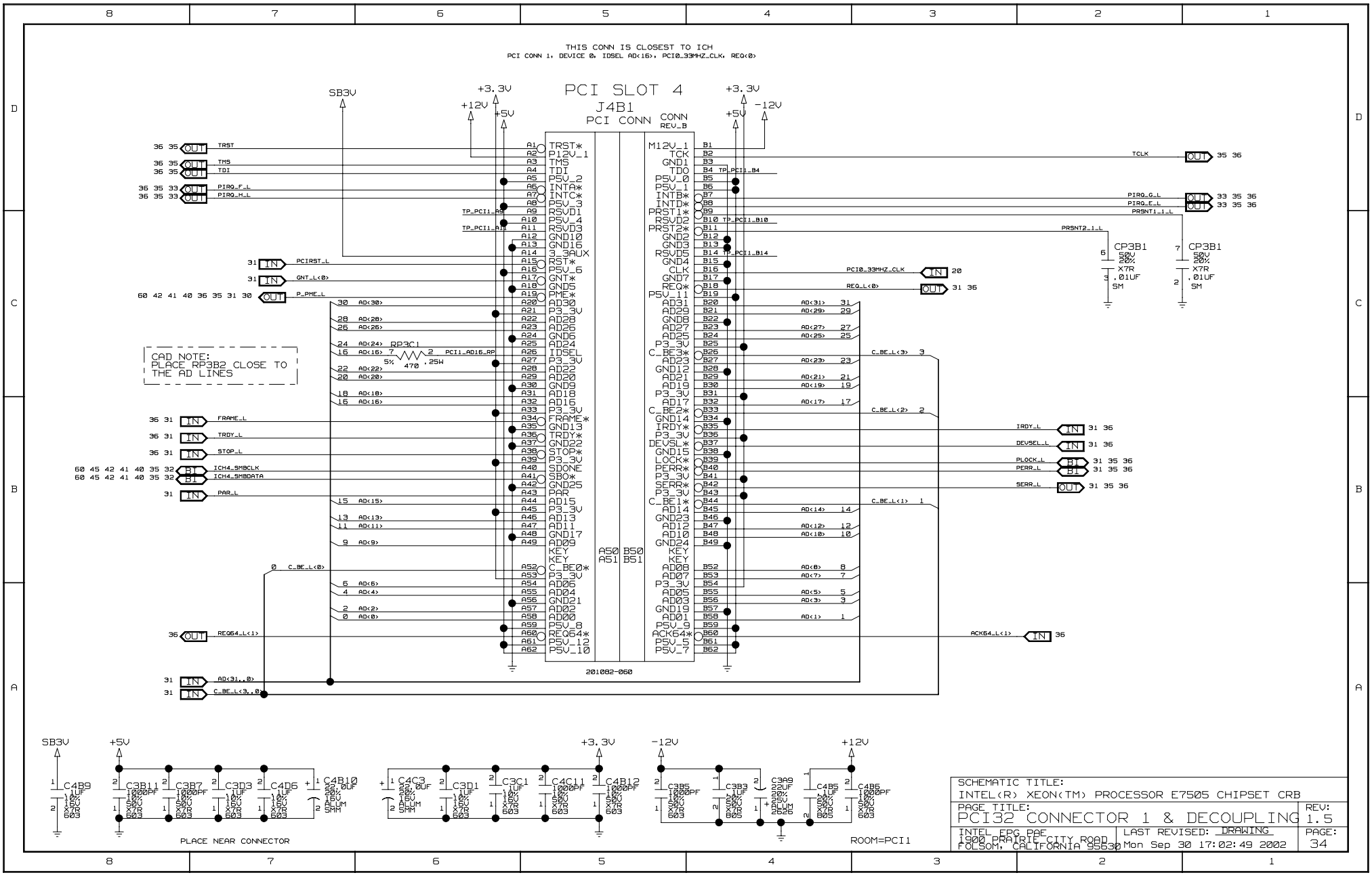
REV: 1.5

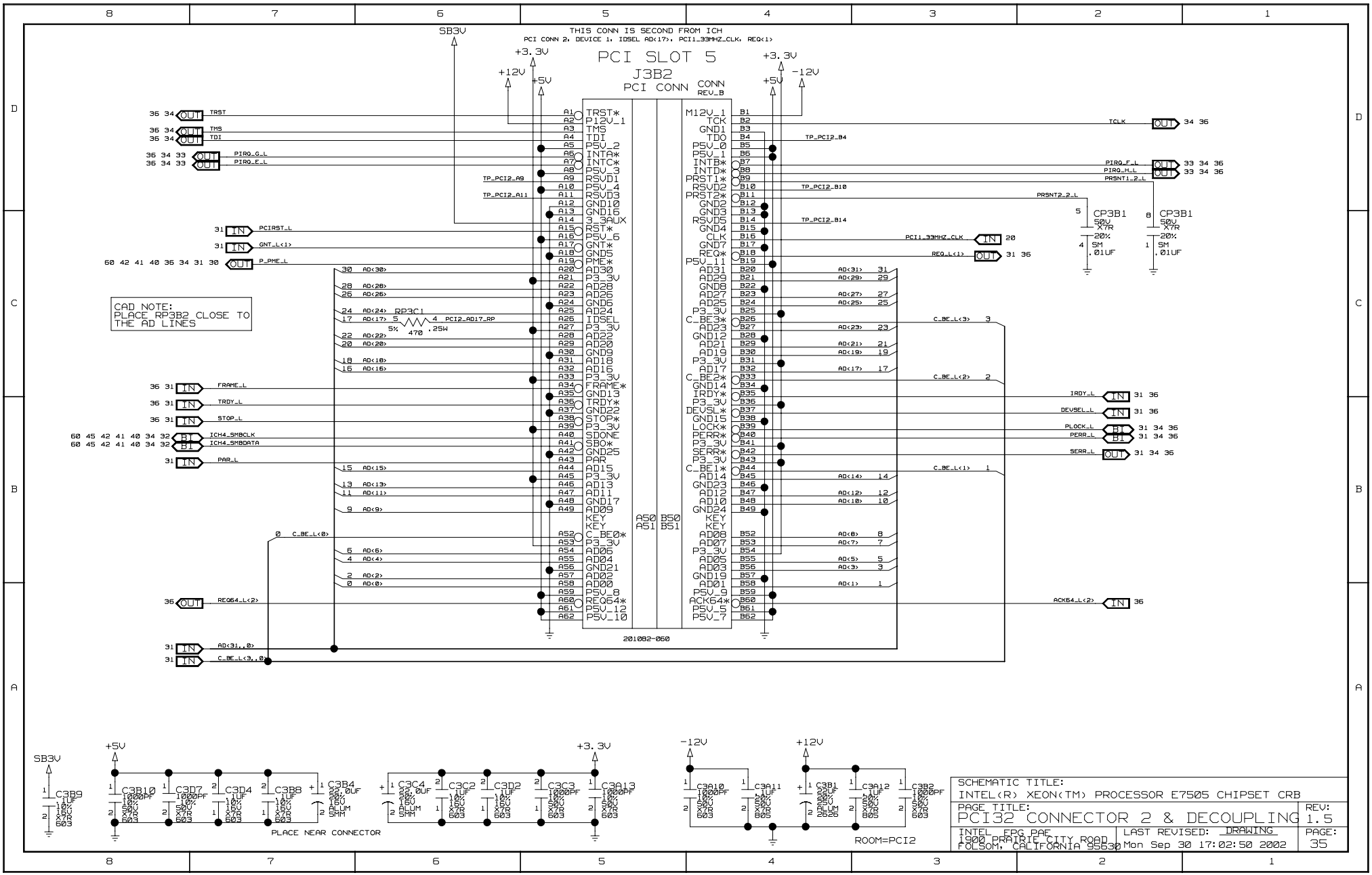
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

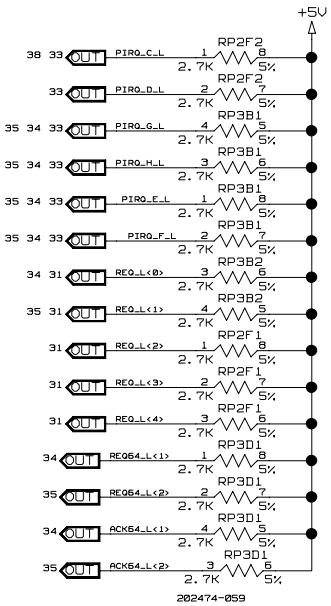
LAST REVISED: DRAWING
Mon Sep 30 17:02:48 2002

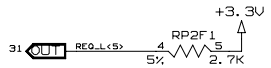
PAGE: 33

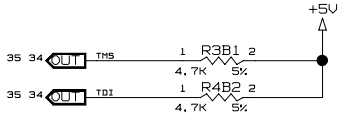
ROOM=ICH4

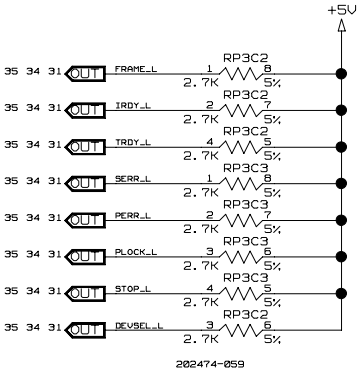

THIS CONN IS CLOSEST TO ICH
PCI CONN 1, DEVICE 0, IDSEL AD<16>, PCI0_33MHZ_CLK, REQ<0>
PCI SLOT 4
J4B1
PCI CONN
CONN REV_B
SB3V
+3.3V
+12V
+5V
-12V
TRST*
P12V_1
TMS
TDI
P5V_2
INTA*
INTC*
P5V_3
RSVD1
P5V_4
RSVD3
GND10
GND16
3_3AUX
RST*
P5V_6
GNT*
GND5
PME*
AD30
P3_3V
AD28
AD26
GND6
AD24
IDSEL
P3_3V
AD22
AD20
GND9
AD18
AD16
P3_3V
FRAME*
GND13
TRDY*
GND22
STOP*
P3_3V
SDONE
SB0*
GND25
PAR
AD15
P3_3V
AD13
AD11
GND17
AD09
KEY
KEY
C_BE0*
P3_3V
AD06
AD04
GND21
AD02
AD00
P5V_8
REQ64*
P5V_12
P5V_10
M12V_1
TCK
GND1
TDO
P5V_0
P5V_1
INTB*
INTD*
PRST1*
RSVD2
PRST2*
GND2
GND3
RSVD5
GND4
CLK
GND7
REQ*
P5V_11
AD31
AD29
GND8
AD27
AD25
P3_3V
C_BE3*
AD23
GND12
AD21
AD19
P3_3V
AD17
C_BE2*
GND14
IRDY*
P3_3V
DEVSEL*
GND15
LOCK*
PERR*
P3_3V
SERR*
P3_3V
C_BE1*
AD14
GND23
AD12
AD10
GND24
KEY
KEY
AD08
AD07
P3_3V
AD05
AD03
GND19
AD01
P5V_9
ACK64*
P5V_5
P5V_7
A50 B50
A51 B51
201082-060
CAD NOTE:
PLACE RP3B2 CLOSE TO
THE AD LINES
RP3C1
5% 470 .25W
PCI1_AD16_RP
TRST
TMS
TDI
PIRQ_F_L
PIRQ_H_L
PCIRST_L
GNT_L<0>
P_PME_L
FRAME_L
TRDY_L
STOP_L
ICH4_SMBCLK
ICH4_SMBDATA
PAR_L
REQ64_L<1>
AD<31..0>
C_BE_L<3..0>
TP_PCI1_A9
TP_PCI1_A11
TP_PCI1_B4
TP_PCI1_B10
TP_PCI1_B14
TCLK
PIRQ_G_L
PIRQ_E_L
PRSNT1_1_L
PRSNT2_1_L
PCI0_33MHZ_CLK
REQ_L<0>
IRDY_L
DEVSEL_L
PLOCK_L
PERR_L
SERR_L
ACK64_L<1>
C_BE_L<3>
C_BE_L<2>
C_BE_L<1>
CP3B1
50V
20%
X7R
.01UF
SM
C4B9 .1UF 10% 50V X7R 603
C3B11 1000PF 10% 50V X7R 603
C3B7 1000PF 10% 50V X7R 603
C3D3 .1UF 10% 50V X7R 603
C4D6 .1UF 10% 50V X7R 603
C4B10 22.0UF 20% 16V ALUM SMM
C4C3 22.0UF 20% 16V ALUM SMM
C3D1 .1UF 10% 50V X7R 603
C3C1 .1UF 10% 50V X7R 603
C4C11 1000PF 10% 50V X7R 603
C4B12 1000PF 10% 50V X7R 603
C3B5 1000PF 10% 50V X7R 603
C3B3 .1UF 20% 50V X7R 805
C3A9 22UF 20% 25V ALUM 2626
C4B5 .1UF 20% 50V X7R 805
C4B6 1000PF 10% 50V X7R 603
PLACE NEAR CONNECTOR
ROOM=PCI1
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
PCI32 CONNECTOR 1 & DECOUPLING
REV: 1.5
INTEL_FPG_PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:49 2002
PAGE: 34

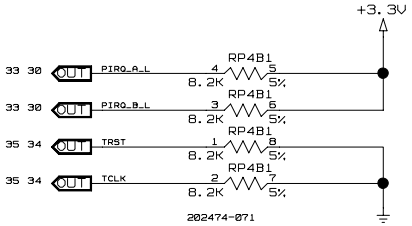

THIS CONN IS SECOND FROM ICH
PCI CONN 2, DEVICE 1, IDSEL AD<17>, PCI1_33MHZ_CLK, REQ<1>
PCI SLOT 5
J3B2
PCI CONN CONN
REV_B
SB3V
+3.3V
+12V
+5V
-12V
CAD NOTE:
PLACE RP3B2 CLOSE TO
THE AD LINES
RP3C1
470 .25W
5%
201082-060
PLACE NEAR CONNECTOR
ROOM=PCI2
SCHEMATIC TITLE:
INTEL<R> XEON<TM> PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
PCI32 CONNECTOR 2 & DECOUPLING
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:50 2002
PAGE:
35

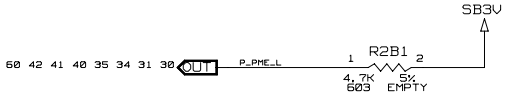






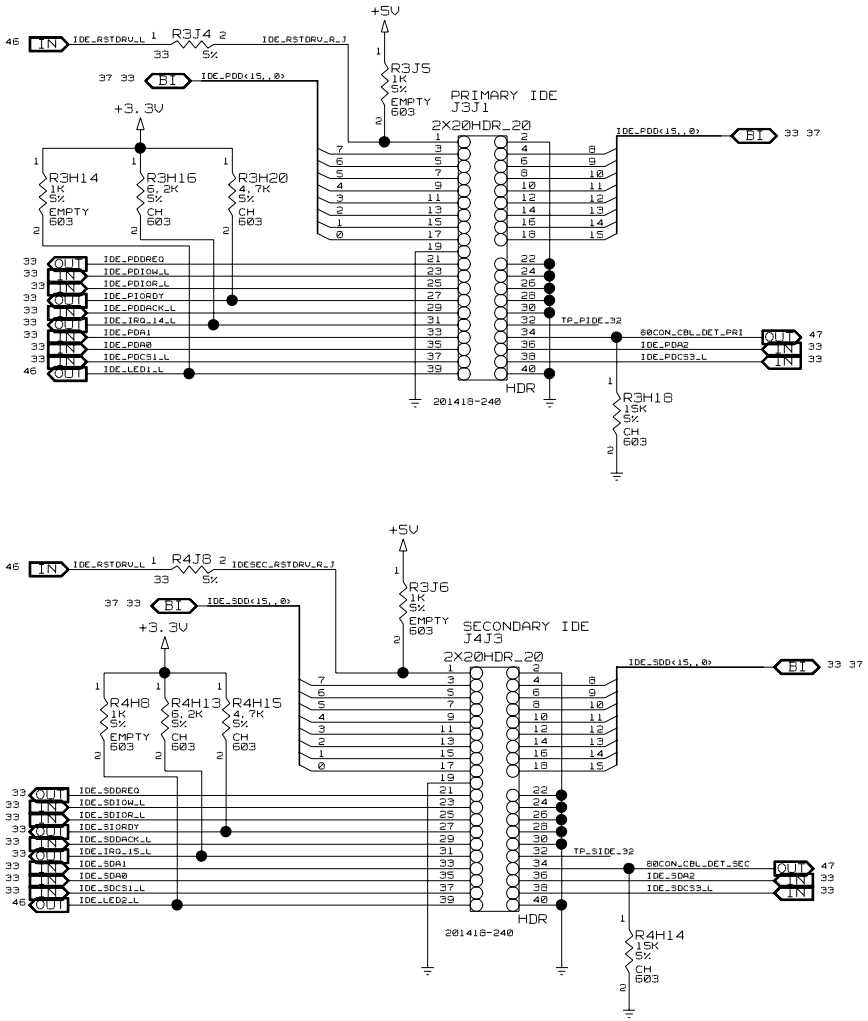






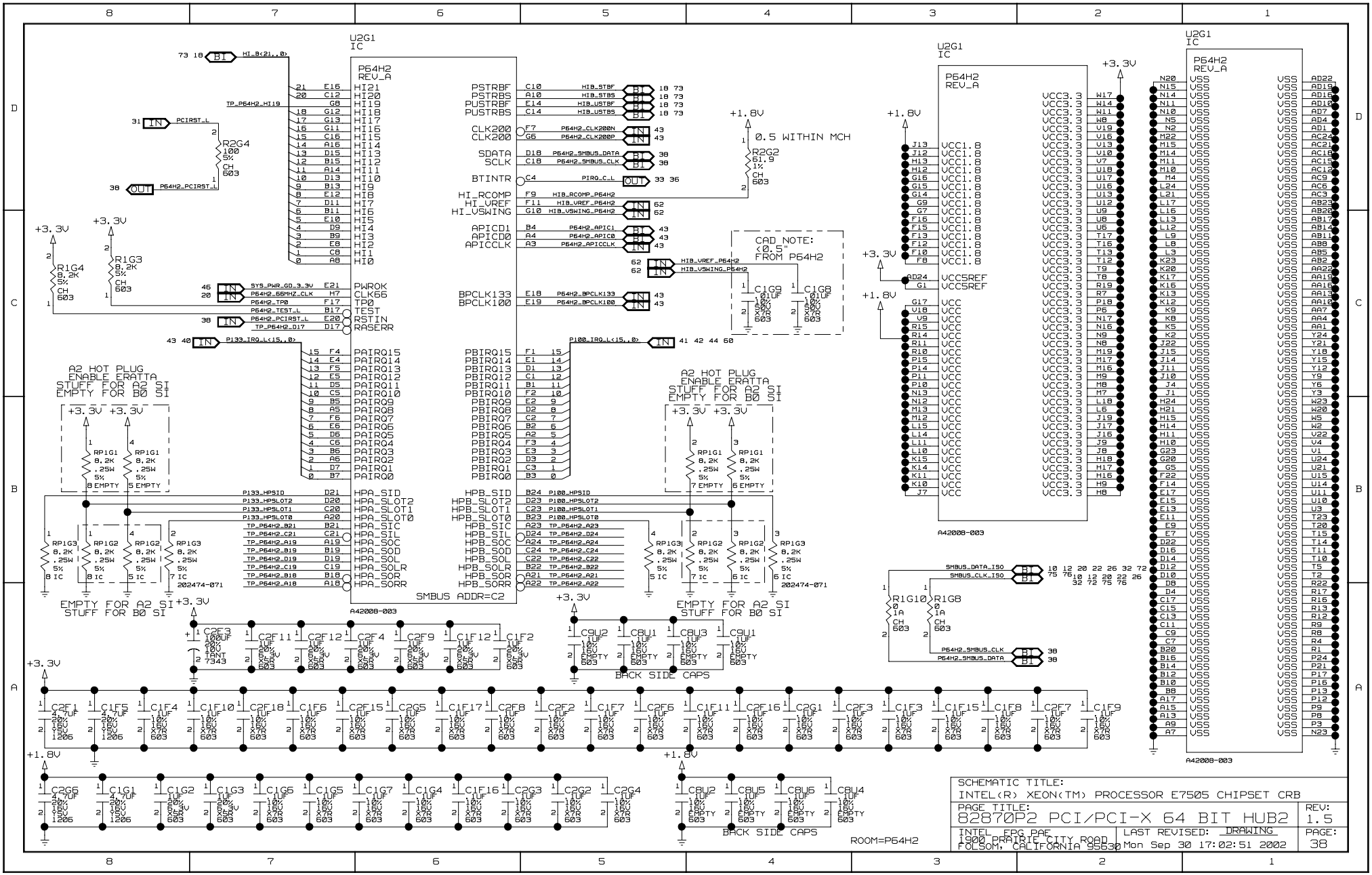
ROOM=PCI33_TERM

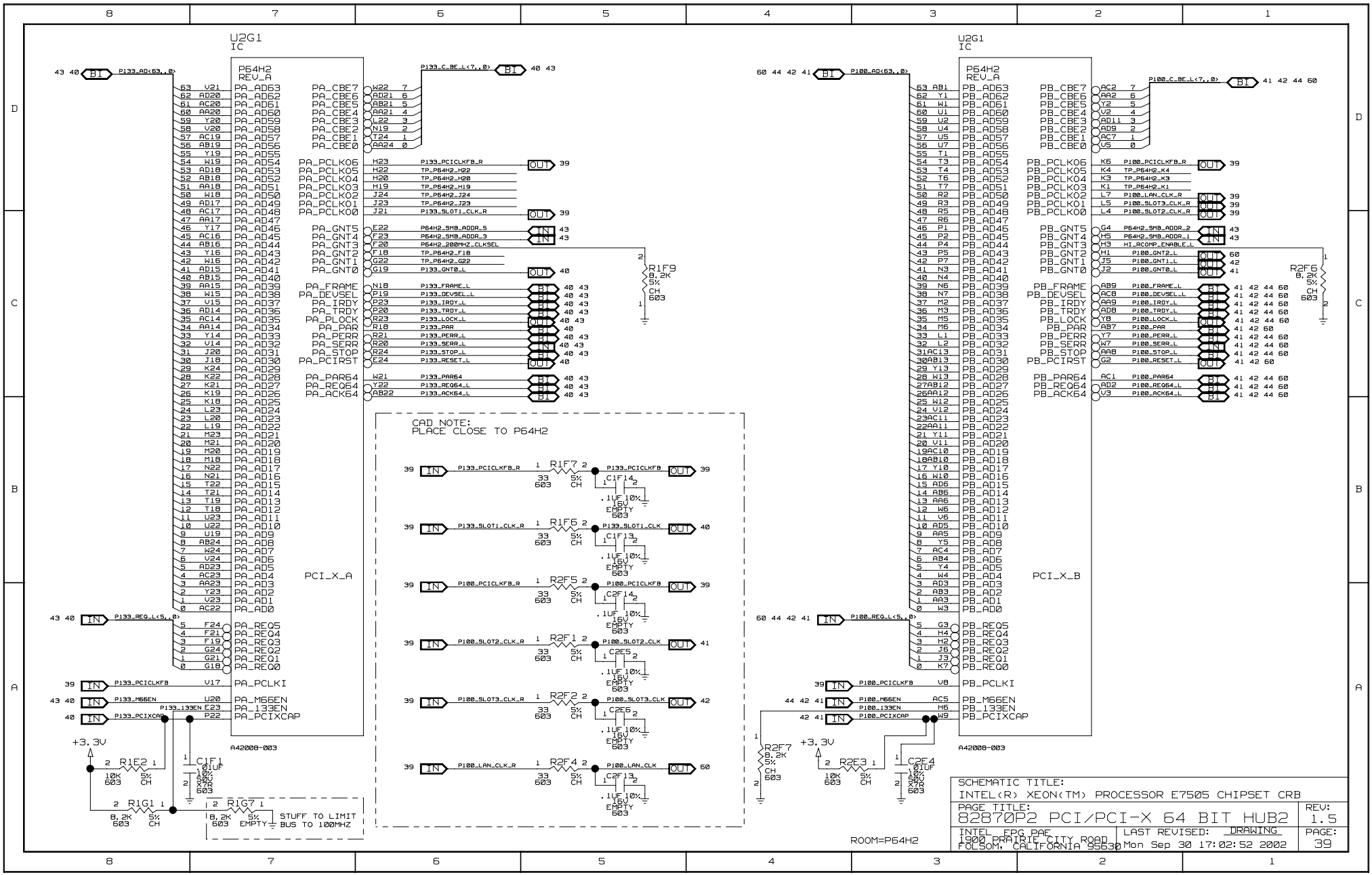
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB	
PAGE TITLE: PCI TERMINATION	REV: 1.5
INTEL EPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:50 2002
	PAGE: 36

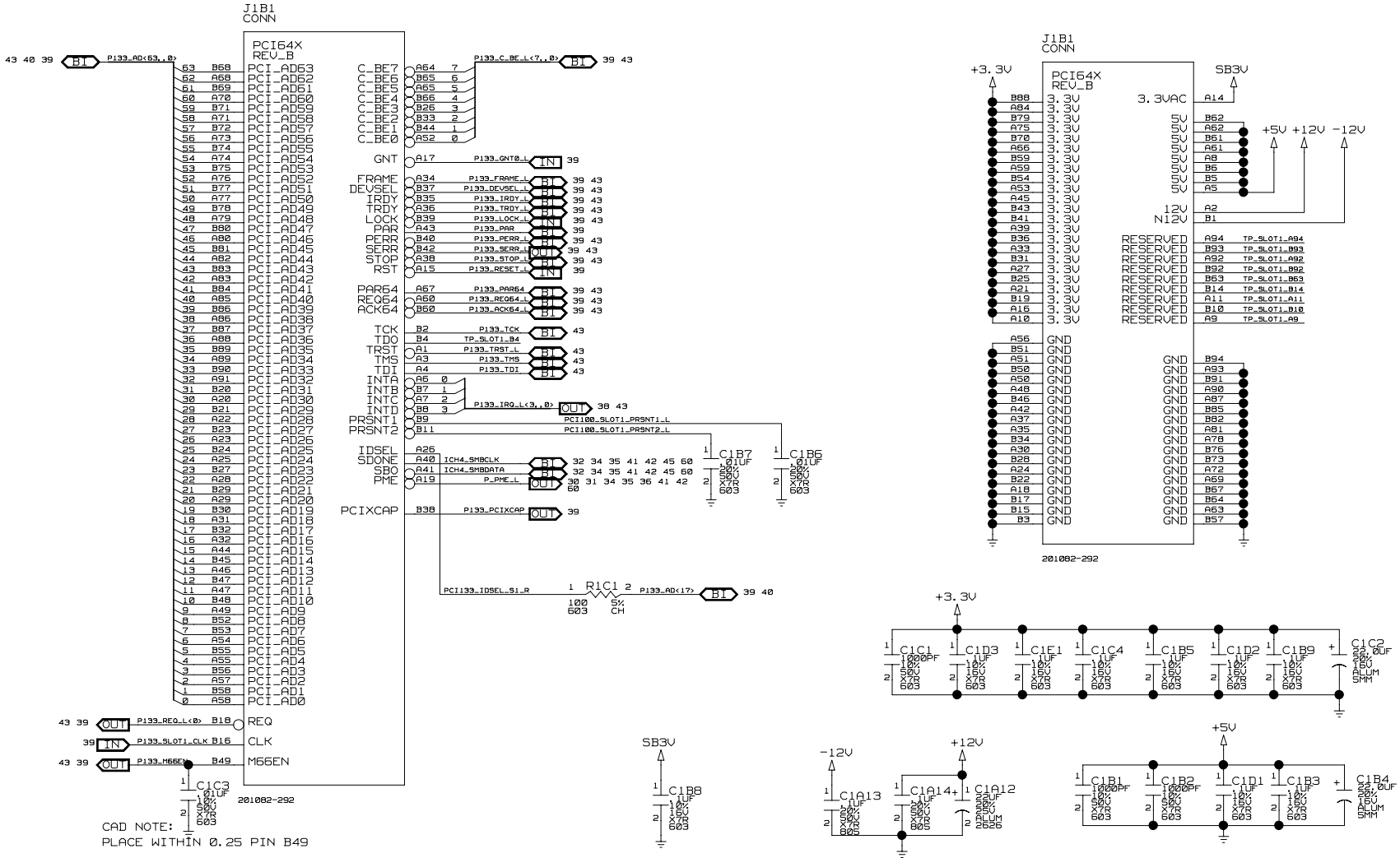


ROOM=IDESEC
ROOM=IDEPRI

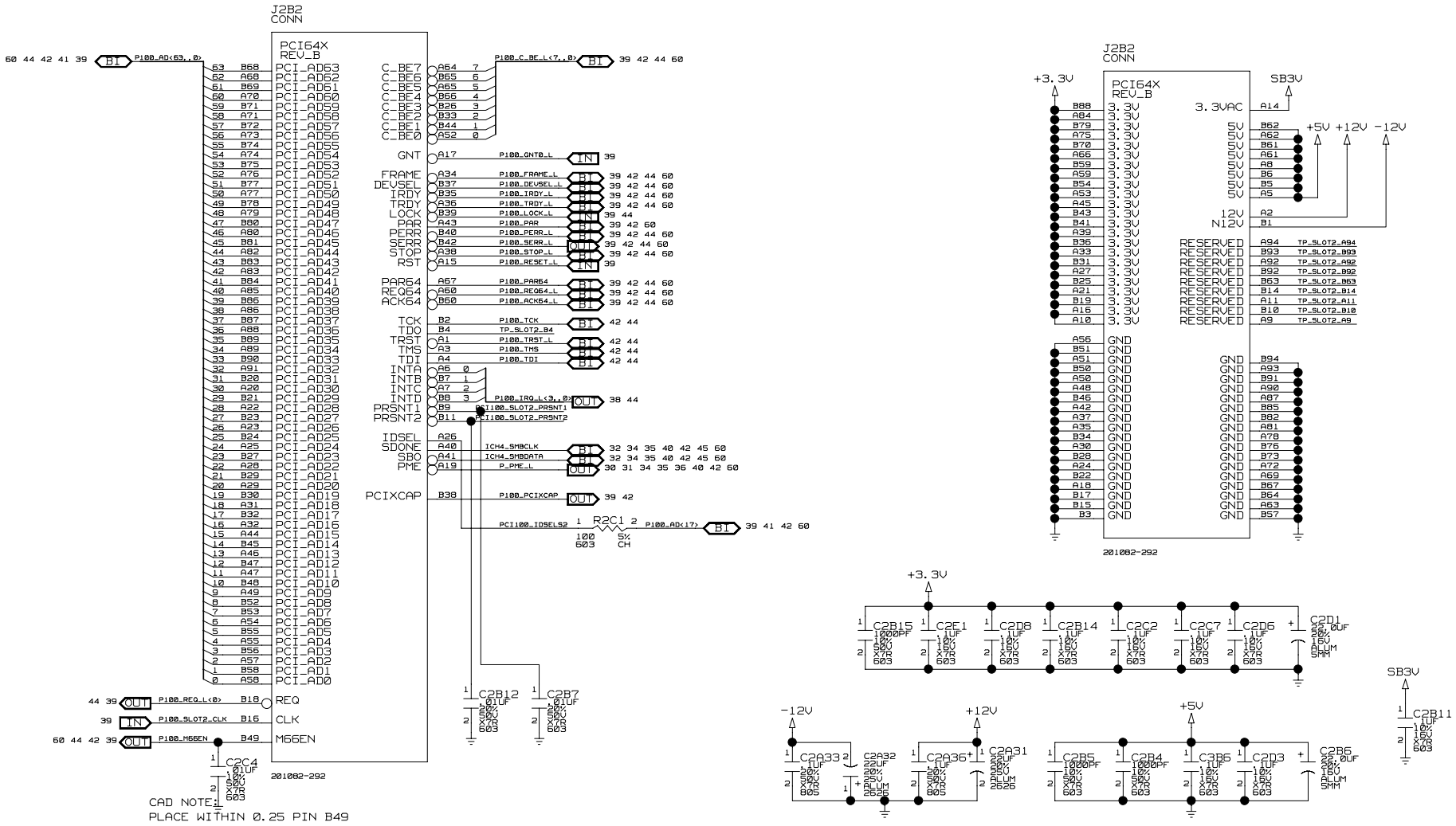
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB	
PAGE TITLE: IDE PRIMARY / SECONDARY	REV: 1.5
INTEL EPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:50 2002
	PAGE: 37

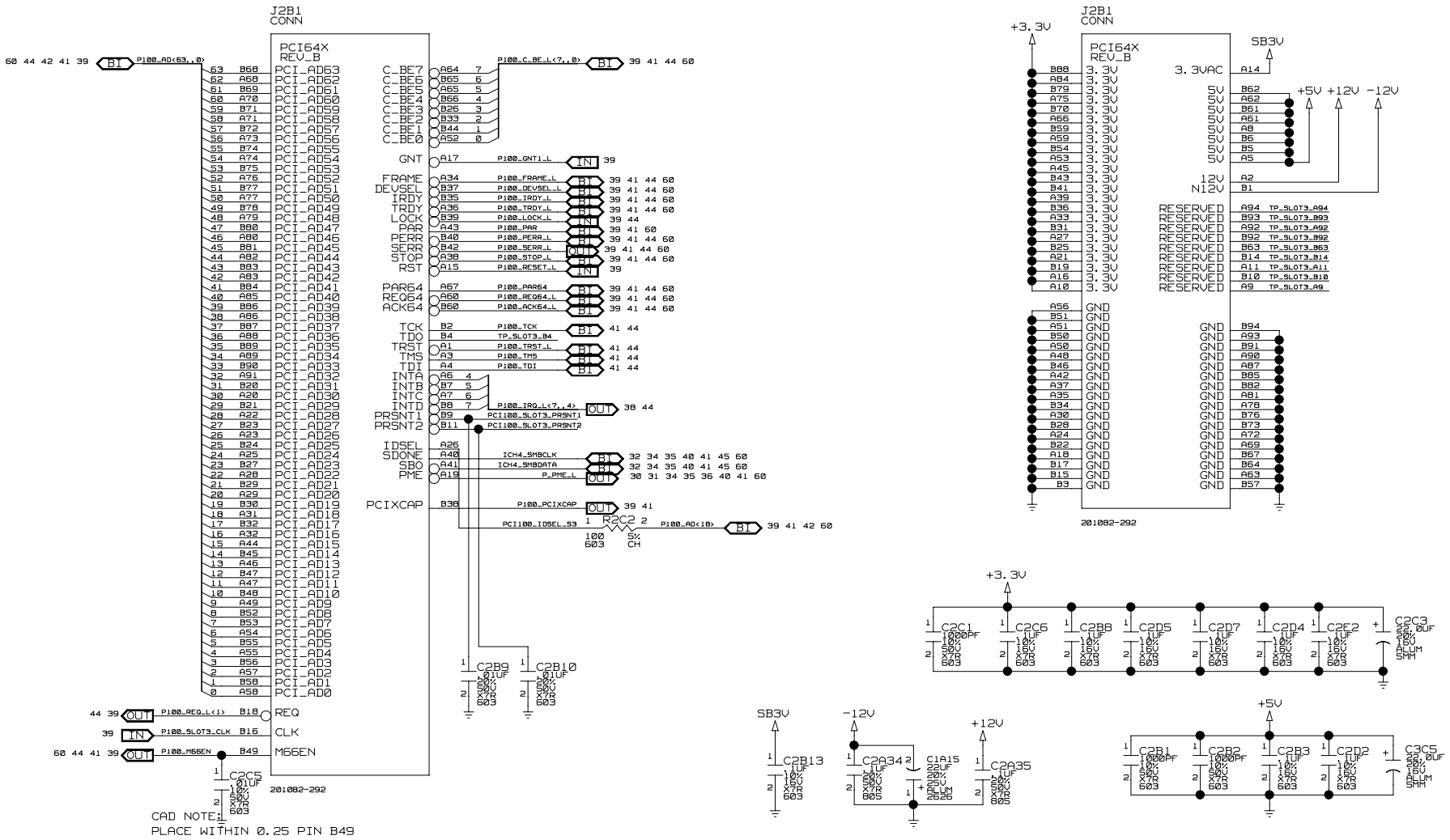

U2G1
IC
P64H2
REV_A
HI_B<21..0>
HI21 HI20 HI19 HI18 HI17 HI16 HI15 HI14 HI13 HI12 HI11 HI10 HI9 HI8 HI7 HI6 HI5 HI4 HI3 HI2 HI1 HI0
PSTRBF PSTRBS PUSTRBF PUSTRBS
HIB_STBF HIB_STBS HIB_USTBF HIB_USTBS
CLK200 CLK200
P64H2_CLK200N P64H2_CLK200P
SDATA SCLK
P64H2_SMBUS_DATA P64H2_SMBUS_CLK
BTINTR
PIRQ_C_L
HI_RCOMP HI_VREF HI_VSWING
HIB_RCOMP_P64H2 HIB_VREF_P64H2 HIB_VSWING_P64H2
APICD1 APICD0 APICCLK
P64H2_APIC1 P64H2_APIC0 P64H2_APICCLK
BPCLK133 BPCLK100
P64H2_BPCLK133 P64H2_BPCLK100
PCIRST_L
P64H2_PCIRST_L
SYS_PWR_GD_3.3V
P64H2_66MHZ_CLK
P64H2_TP0
P64H2_TEST_L
P64H2_PCIRST_L
TP_P64H2_DI7
PWROK CLK66 TP0 TEST RSTIN RASERR
P133_IRQ_L<15..0>
PAIRQ15 PAIRQ14 PAIRQ13 PAIRQ12 PAIRQ11 PAIRQ10 PAIRQ9 PAIRQ8 PAIRQ7 PAIRQ6 PAIRQ5 PAIRQ4 PAIRQ3 PAIRQ2 PAIRQ1 PAIRQ0
PBIRQ15 PBIRQ14 PBIRQ13 PBIRQ12 PBIRQ11 PBIRQ10 PBIRQ9 PBIRQ8 PBIRQ7 PBIRQ6 PBIRQ5 PBIRQ4 PBIRQ3 PBIRQ2 PBIRQ1 PBIRQ0
P100_IRQ_L<15..0>
P133_HPSID P133_HPSLOT2 P133_HPSLOT1 P133_HPSLOT0
HPA_SID HPA_SLOT2 HPA_SLOT1 HPA_SLOT0 HPA_SIC HPA_SIL HPA_SOC HPA_SOD HPA_SOL HPA_SOLR HPA_SOR HPA_SORR
HPB_SID HPB_SLOT2 HPB_SLOT1 HPB_SLOT0 HPB_SIC HPB_SIL HPB_SOC HPB_SOD HPB_SOL HPB_SOLR HPB_SOR HPB_SORR
P100_HPSID P100_HPSLOT2 P100_HPSLOT1 P100_HPSLOT0
TP_P64H2_A23 TP_P64H2_D24 TP_P64H2_A24 TP_P64H2_C24 TP_P64H2_C22 TP_P64H2_B22 TP_P64H2_A21 TP_P64H2_A22
SMBUS ADDR=C2
A42008-003
A2 HOT PLUG ENABLE ERATTA
STUFF FOR A2 SI
EMPTY FOR B0 SI
RP1G1 8.2K .25W 5%
RP1G2 8.2K .25W 5%
RP1G3 8.2K .25W 5%
202474-071
EMPTY FOR A2 SI
STUFF FOR B0 SI
R2G4 100 5% CH 603
R1G4 8.2K 5% CH 603
R1G3 8.2K 5% CH 603
R2G2 61.9 1% CH 603
0.5 WITHIN MCH
CAD NOTE: .0.5" FROM P64H2
C1G9 C1G8 10UF 10% 50V X7R 603
+3.3V
+1.8V
VCC3.3
VCC1.8
VCC5REF
VCC
VSS
SMBUS_DATA_ISO
SMBUS_CLK_ISO
R1G10 R1G8 0 1A CH 603
C2E3 100UF 20% 10V TANT 7343
C2F11 C2F12 C2F4 C2F9 C1F12 C1F2
C8V2 C8U1 C8U3 C8V1
BACK SIDE CAPS
C2F1 4.7UF 20% 10V 1206
C1F5 C1F4 C1F10 C2F18 C1F6 C2F15 C2G5 C1F17 C2F8 C2F2 C1F7 C2F5 C1F11 C2F16 C2G1 C2F3 C1F3 C1F15 C1F8 C2F7 C1F9
C2G6 C1G1 C1G2 C1G3 C1G6 C1G5 C1G7 C1G4 C1F16 C2G3 C2G2 C2G4
C8U2 C8U5 C8U6 C8U4
BACK SIDE CAPS
ROOM=P64H2
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
82870P2 PCI/PCI-X 64 BIT HUB2
REV: 1.5
INTEL FDG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:51 2002
PAGE: 38


U2G1
IC
P64H2
REV_A
PCI_X_A
A42008-003
U2G1
IC
P64H2
REV_A
PCI_X_B
A42008-003
CAD NOTE:
PLACE CLOSE TO P64H2
STUFF TO LIMIT BUS TO 100MHZ
ROOM=P64H2
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:
82870P2 PCI/PCI-X 64 BIT HUB2
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:52 2002
PAGE:
39

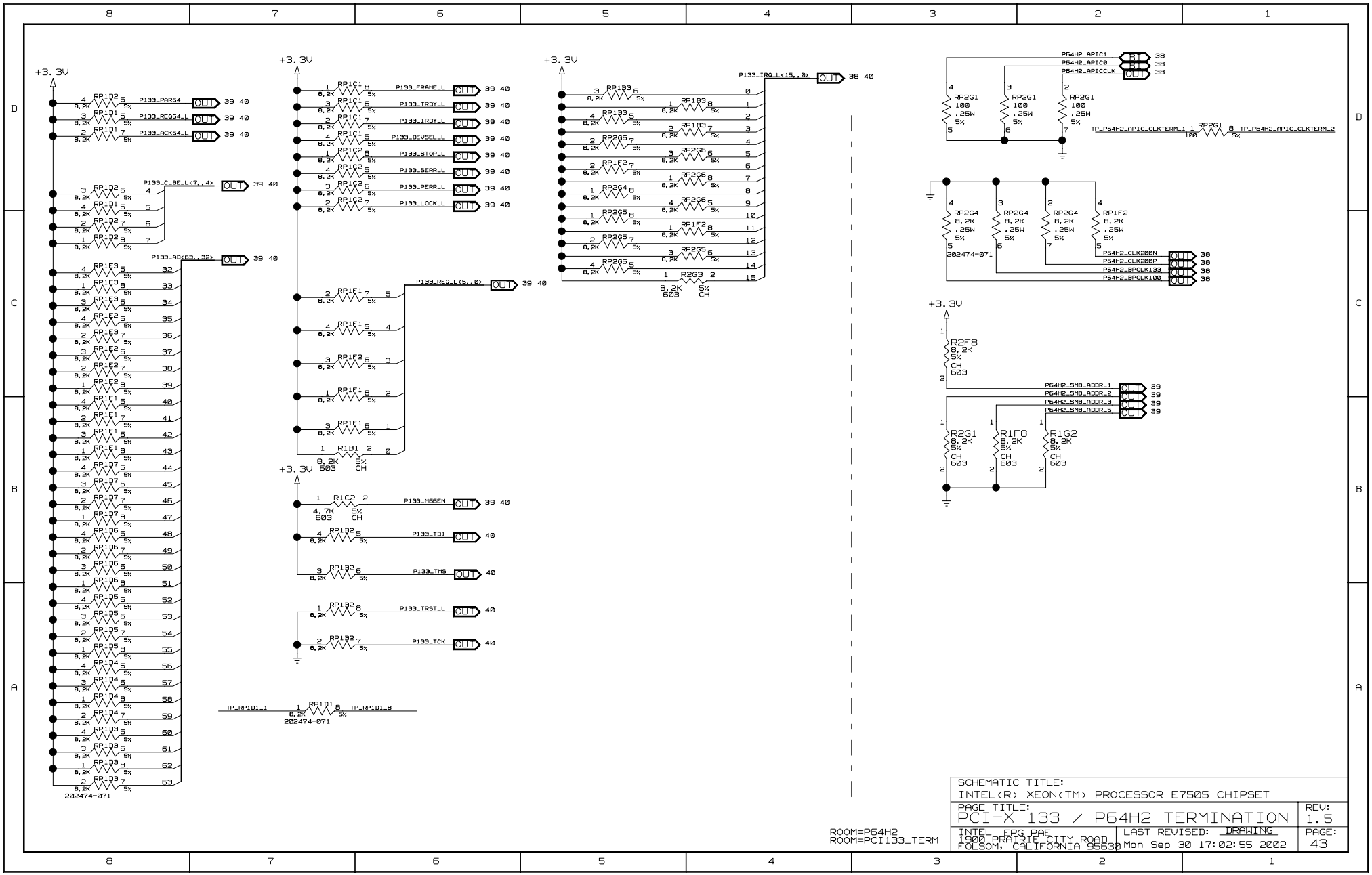


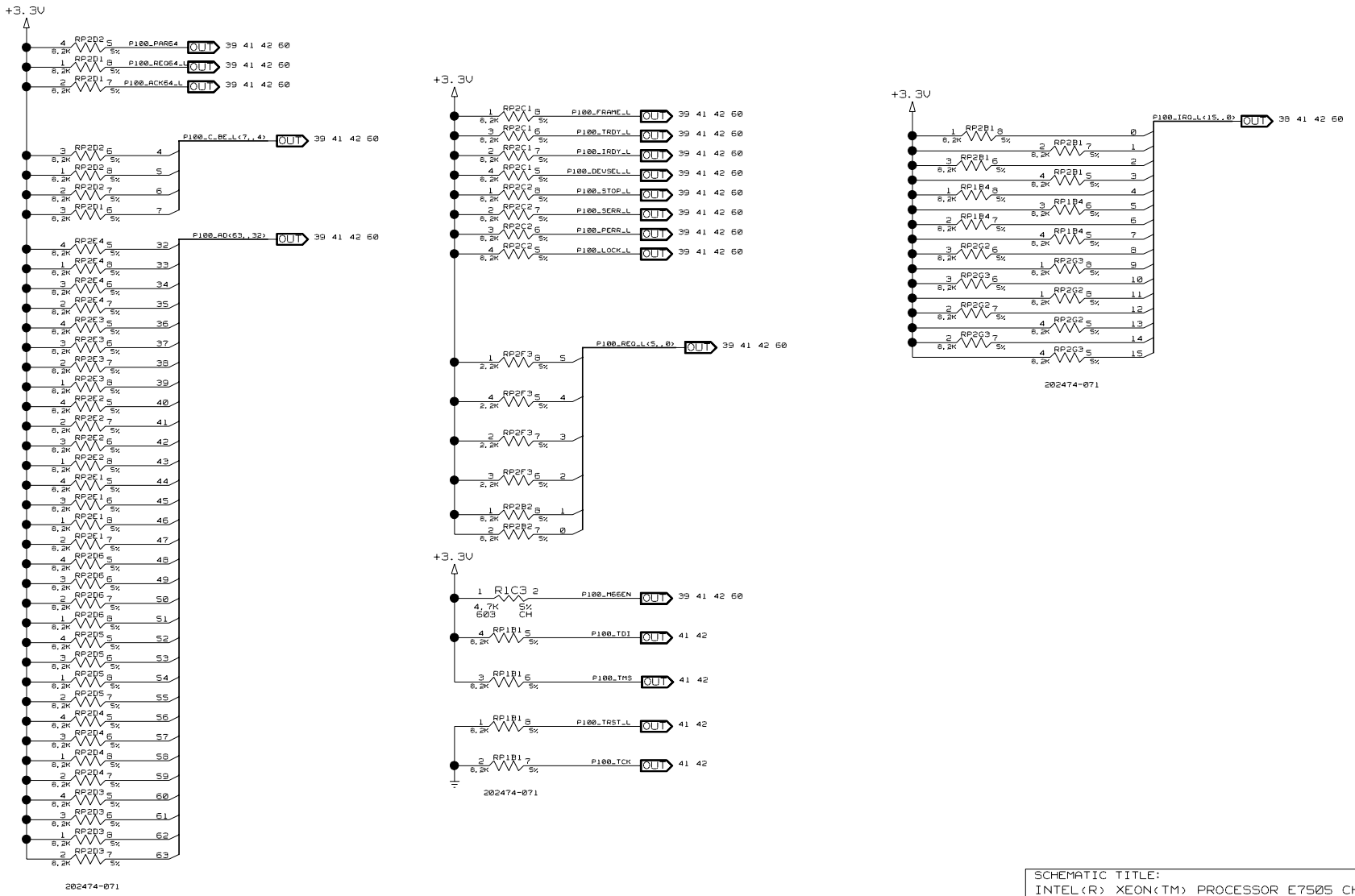
SCHEMATIC TITLE:	INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB
PAGE TITLE:	PCI-X 133 MHZ SLOT1
REV:	1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:53 2002
PAGE:	40


J2B2
CONN
PCI64X
REV_B
P100_AD<63..0>
PCI_AD63
PCI_AD62
PCI_AD61
PCI_AD60
PCI_AD59
PCI_AD58
PCI_AD57
PCI_AD56
PCI_AD55
PCI_AD54
PCI_AD53
PCI_AD52
PCI_AD51
PCI_AD50
PCI_AD49
PCI_AD48
PCI_AD47
PCI_AD46
PCI_AD45
PCI_AD44
PCI_AD43
PCI_AD42
PCI_AD41
PCI_AD40
PCI_AD39
PCI_AD38
PCI_AD37
PCI_AD36
PCI_AD35
PCI_AD34
PCI_AD33
PCI_AD32
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
C_BE7
C_BE6
C_BE5
C_BE4
C_BE3
C_BE2
C_BE1
C_BE0
P100_C_BE_L<7..0>
GNT
P100_GNT0_L
FRAME
DEVSEL
IRDY
TRDY
LOCK
PAR
PERR
SERR
STOP
RST
P100_FRAME_L
P100_DEVSEL_L
P100_IRDY_L
P100_TRDY_L
P100_LOCK_L
P100_PAR
P100_PERR_L
P100_SERR_L
P100_STOP_L
P100_RESET_L
PAR64
REQ64
ACK64
P100_PAR64
P100_REQ64_L
P100_ACK64_L
TCK
TDO
TRST
TMS
TDI
P100_TCK
TP_SLOT2_B4
P100_TRST_L
P100_TMS
P100_TDI
INTA
INTB
INTC
INTD
P100_IRQ_L<3..0>
PRSNT1
PRSNT2
PCI100_SLOT2_PRSNT1
PCI100_SLOT2_PRSNT2
IDSEL
SDONE
SBO
PME
ICH4_SMBCLK
ICH4_SMBDATA
P_PME_L
PCIXCAP
P100_PCIXCAP
PCI100_IDSELS2
R2C1
100
603
5%
CH
P100_AD<17>
REQ
CLK
M66EN
P100_REQ_L<0>
P100_SLOT2_CLK
P100_M66EN
C2C4
10UF
C2B12
C2B7
201082-292
CAD NOTE:
PLACE WITHIN 0.25 PIN B49
J2B2
CONN
PCI64X
REV_B
+3.3V
SB3V
3.3VAC
+5V
+12V
-12V
RESERVED
GND
201082-292
C2B15
1000PF
C2E1
C2D8
C2B14
C2C2
C2C7
C2D6
C2D1
330UF
C2B11
C2A33
C2A32
22UF
C2A36
C2A31
C2B5
C2B4
C3B6
C2D3
C2B6
ROOM=PCI100
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
PCI-X 100MHZ SLOT2
REV:
1.5
INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:54 2002
PAGE:
41



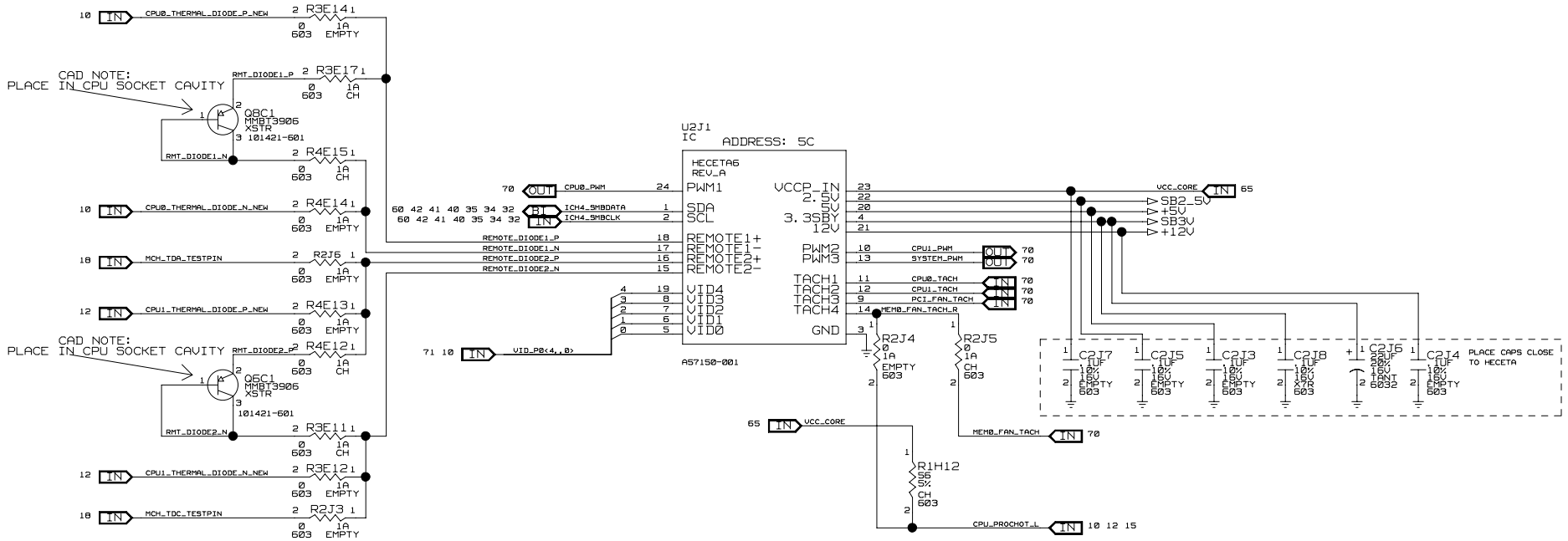
SCHEMATIC TITLE:	INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:	PCI-X 100MHZ SLOT3
REV:	1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:54 2002
PAGE:	42


+3.3V
RP1D2 8.2K 5%
P133_PAR64
RP1D1 8.2K 5%
P133_REQ64_L
RP1D1 8.2K 5%
P133_ACK64_L
OUT 39 40
P133_C_BE_L<7,,4>
RP1D2 8.2K 5%
RP1D1 8.2K 5%
RP1D2 8.2K 5%
RP1D2 8.2K 5%
P133_AD<63,,32>
RP1E3 8.2K 5%
RP1E3 8.2K 5%
RP1E3 8.2K 5%
RP1E2 8.2K 5%
RP1E3 8.2K 5%
RP1E2 8.2K 5%
RP1E2 8.2K 5%
RP1E1 8.2K 5%
RP1E1 8.2K 5%
RP1E1 8.2K 5%
RP1D7 8.2K 5%
RP1D7 8.2K 5%
RP1D7 8.2K 5%
RP1D6 8.2K 5%
RP1D6 8.2K 5%
RP1D6 8.2K 5%
RP1D5 8.2K 5%
RP1D5 8.2K 5%
RP1D5 8.2K 5%
RP1D4 8.2K 5%
RP1D4 8.2K 5%
RP1D4 8.2K 5%
RP1D3 8.2K 5%
RP1D3 8.2K 5%
RP1D3 8.2K 5%
202474-071
RP1C1 8.2K 5%
P133_FRAME_L
P133_TRDY_L
P133_IRDY_L
P133_DEVSEL_L
RP1C2 8.2K 5%
P133_STOP_L
P133_SERR_L
P133_PERR_L
P133_LOCK_L
RP1F1 8.2K 5%
P133_REQ_L<5,,0>
R1B1 8.2K 603 5% CH
R1C2 4.7K 603 5% CH
P133_M66EN
RP1B2 8.2K 5%
P133_TDI
P133_TMS
P133_TRST_L
P133_TCK
OUT 39 40
OUT 40
TP_RP1D1_1
RP1D1 8.2K 5%
TP_RP1D1_8
202474-071
RP1B3 8.2K 5%
RP2G6 8.2K 5%
RP1F2 8.2K 5%
RP2G4 8.2K 5%
RP2G5 8.2K 5%
P133_IRQ_L<15,,0>
R2G3 8.2K 603 5% CH
OUT 38 40
P64H2_APIC1
P64H2_APIC0
P64H2_APICCLK
OUT 38
RP2G1 100 .25W 5%
TP_P64H2_APIC_CLKTERM_1
TP_P64H2_APIC_CLKTERM_2
RP2G4 8.2K .25W 5%
RP1F2 8.2K .25W 5%
202474-071
P64H2_CLK200N
P64H2_CLK200P
P64H2_BPCLK133
P64H2_BPCLK100
OUT 38
R2F8 8.2K 5% CH 603
P64H2_SMB_ADDR_1
P64H2_SMB_ADDR_2
P64H2_SMB_ADDR_3
P64H2_SMB_ADDR_5
OUT 39
R2G1 8.2K 5% CH 603
R1F8 8.2K 5% CH 603
R1G2 8.2K 5% CH 603
ROOM=P64H2
ROOM=PCI133_TERM
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
PCI-X 133 / P64H2 TERMINATION
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:55 2002
PAGE:
43



ROOM=PCI100_TERM

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET	
PAGE TITLE: PCI-X 100 TERMINATION	REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:55 2002
	PAGE: 44

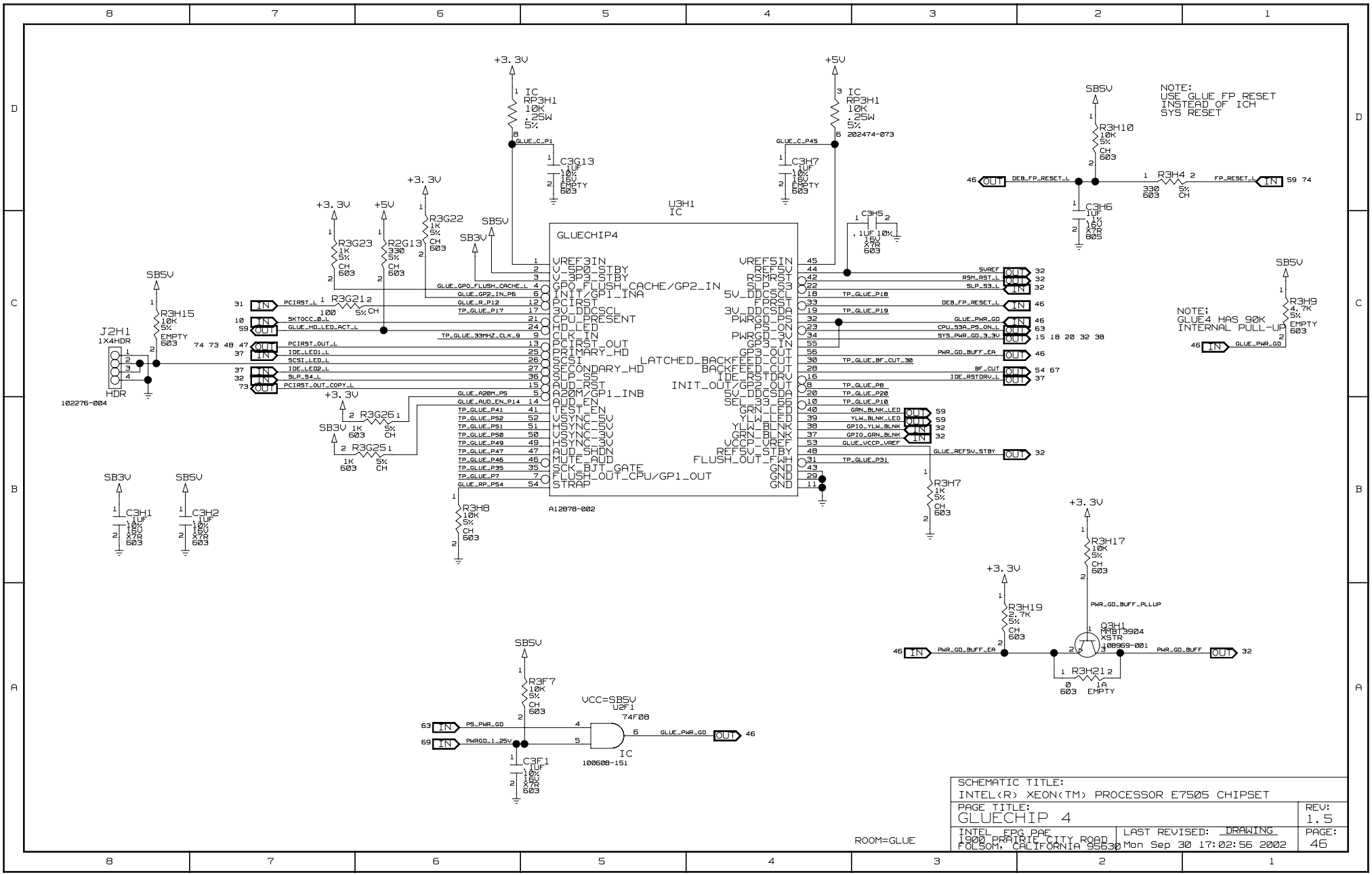


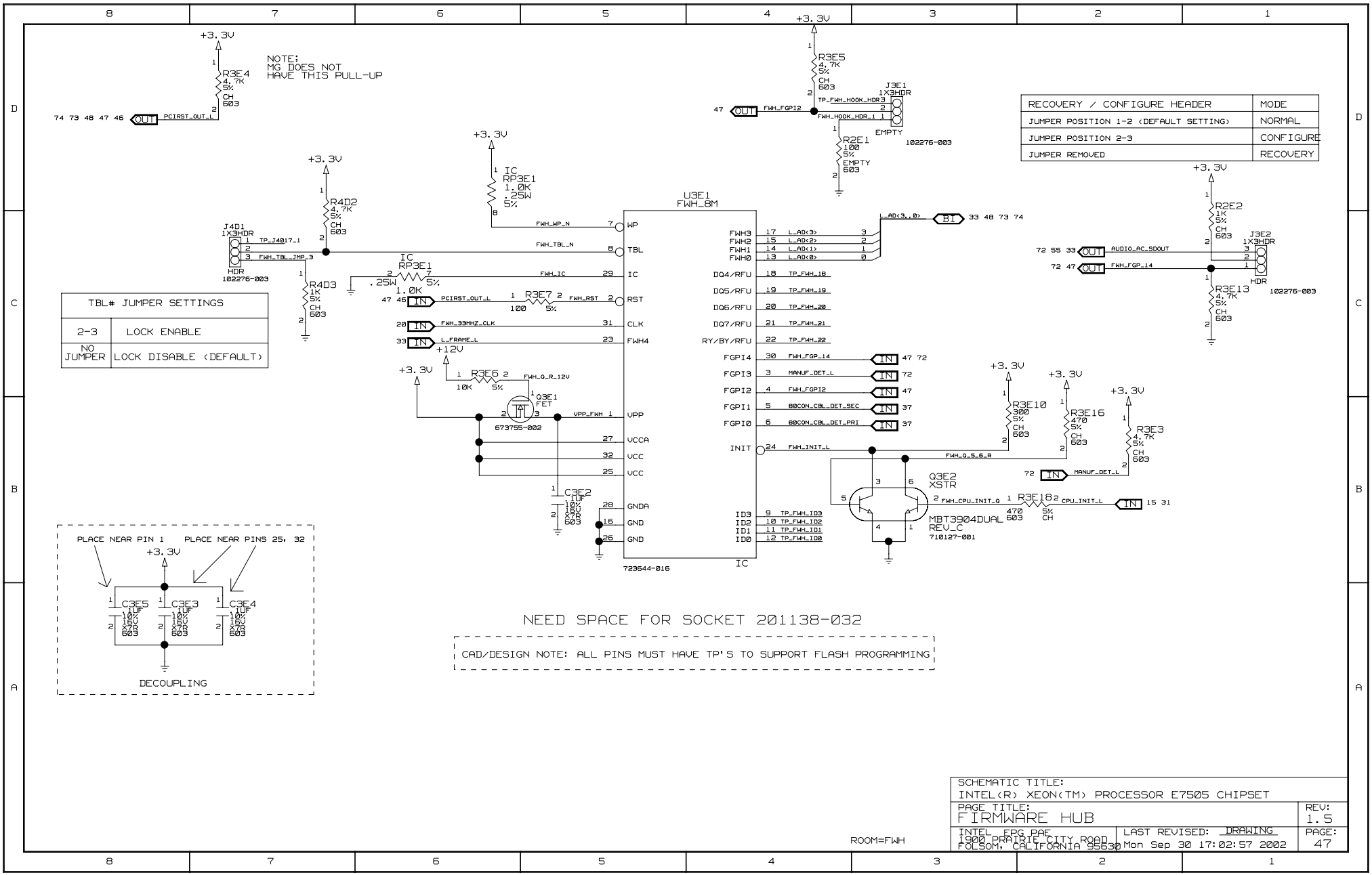
NOTES:

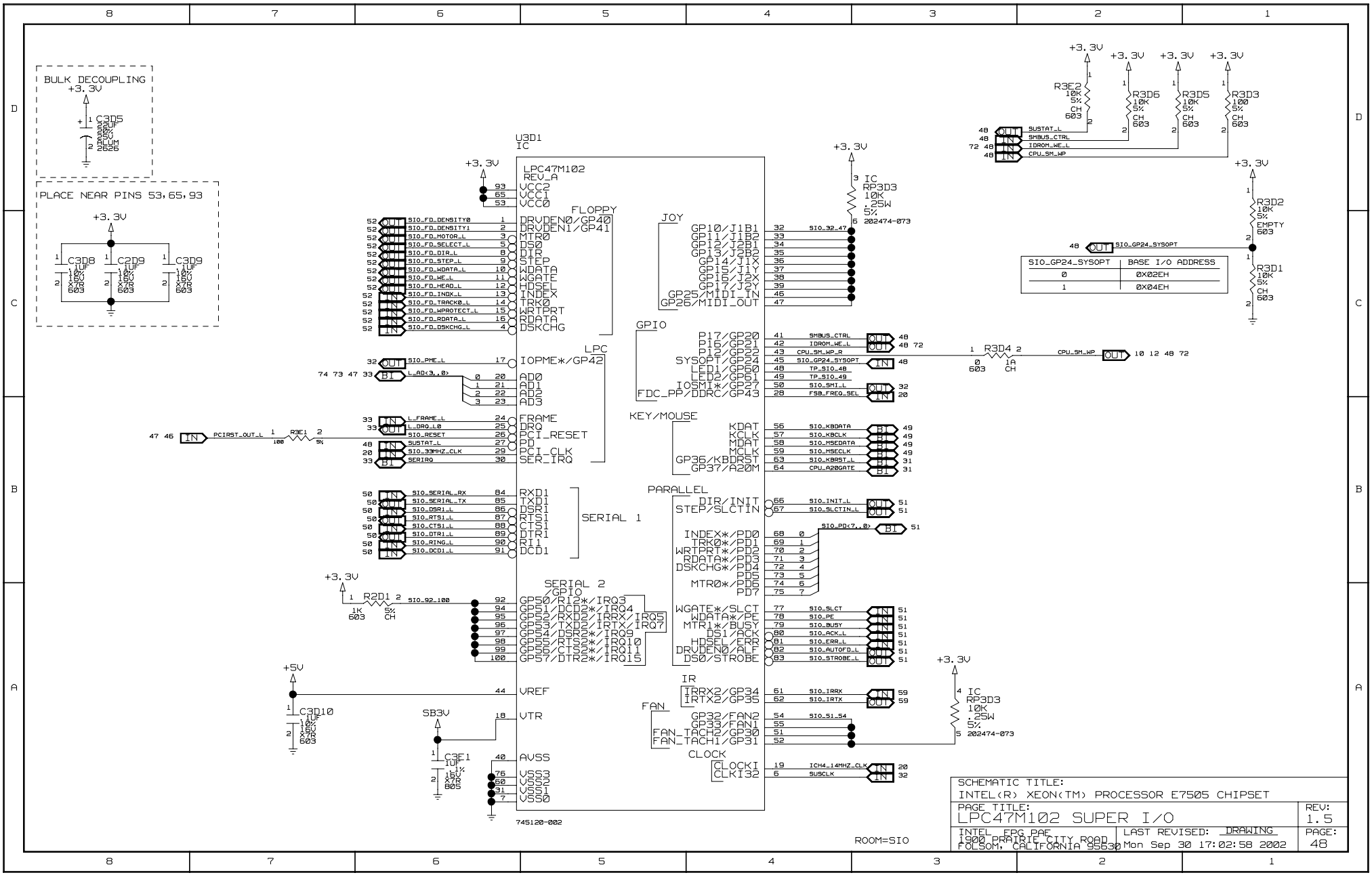
* PLACE 100PF CAP CLOSE TO HECETA
* DIFFERENTIAL PAIR 10 MIL TRACING WITH 10 MIL SPACING WITH GROUND GUARD TRACES ON EACH SIDE FOR THERMDP THERMDN
* HECETA VID[0..4] HAS INTERNAL WEAK PULL-UP (100K).

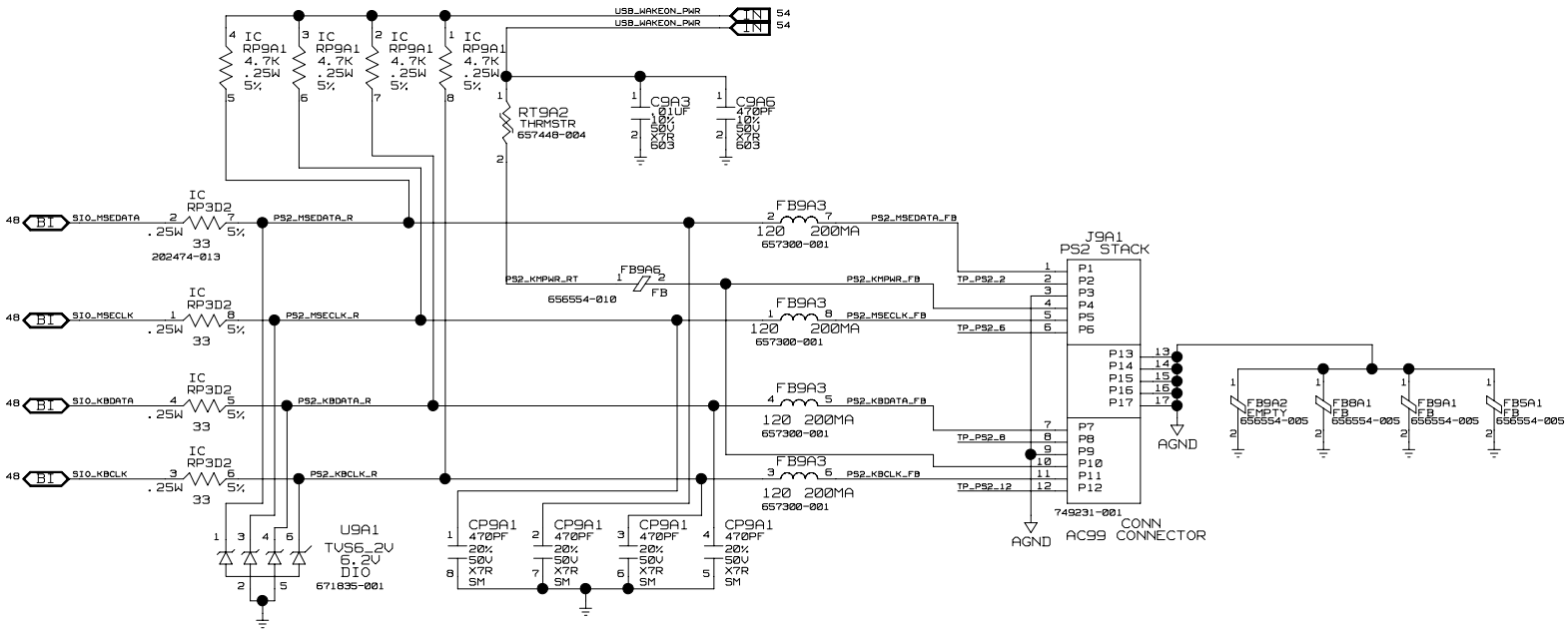
ROOM=HECETA

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET	
PAGE TITLE: HECETA 6	REV: 1.5
INTEL EPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:56 2002
	PAGE: 45


GLUECHIP4
U3H1
IC
A12078-002
NOTE:
USE GLUE FP RESET
INSTEAD OF ICH
SYS RESET
NOTE;
GLUE4 HAS 90K
INTERNAL PULL-UP
VCC=SB5V
U2F1
74F08
ROOM=GLUE
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
GLUECHIP 4
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:56 2002
PAGE:
46

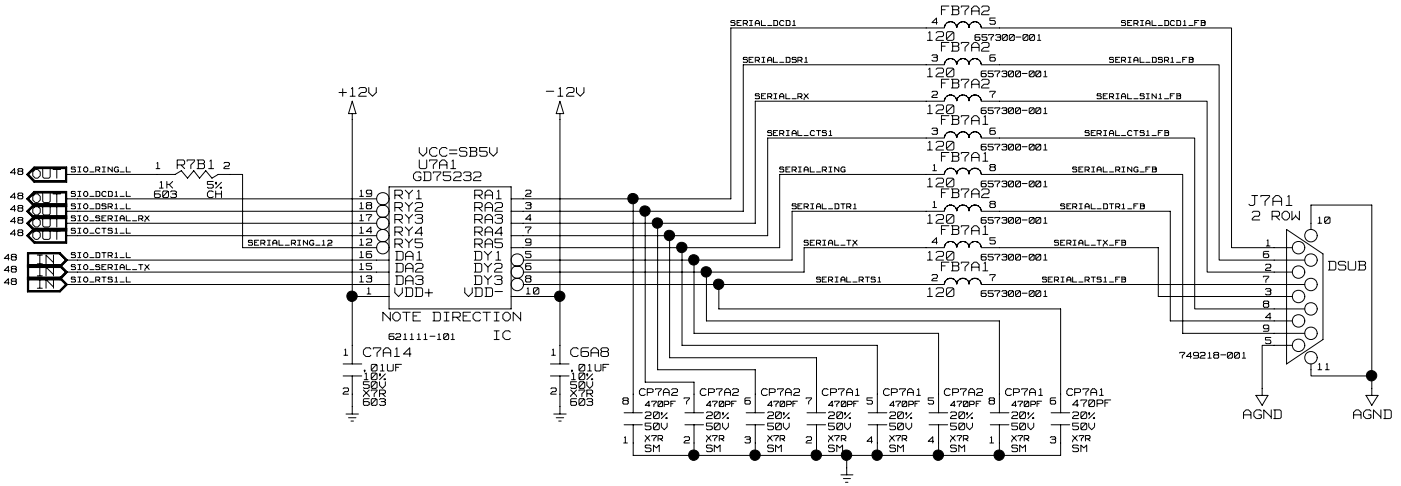

NOTE;
MG DOES NOT
HAVE THIS PULL-UP
RECOVERY / CONFIGURE HEADER | MODE
JUMPER POSITION 1-2 (DEFAULT SETTING) | NORMAL
JUMPER POSITION 2-3 | CONFIGURE
JUMPER REMOVED | RECOVERY
TBL# JUMPER SETTINGS
2-3 | LOCK ENABLE
NO JUMPER | LOCK DISABLE (DEFAULT)
U3E1
FWH_8M
723644-016
IC
NEED SPACE FOR SOCKET 201138-032
CAD/DESIGN NOTE: ALL PINS MUST HAVE TP'S TO SUPPORT FLASH PROGRAMMING
PLACE NEAR PIN 1
PLACE NEAR PINS 25, 32
DECOUPLING
ROOM=FWH
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
FIRMWARE HUB
REV:
1.5
INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:57 2002
PAGE:
47


BULK DECOUPLING
+3.3V
C3D5
PLACE NEAR PINS 53,65,93
C3D8
C2D9
C3D9
U3D1
IC
LPC47M102
REV_A
VCC2
VCC1
VCC0
FLOPPY
DRVDEN0/GP40
DRVDEN1/GP41
MTR0
DS0
DIR
STEP
WDATA
WGATE
HDSEL
INDEX
TRK0
WRTPRT
RDATA
DSKCHG
LPC
IOPME*/GP42
AD0
AD1
AD2
AD3
FRAME
DRQ
PCI_RESET
PD
PCI_CLK
SER_IRQ
SERIAL 1
RXD1
TXD1
DSR1
RTS1
CTS1
DTR1
RI1
DCD1
SERIAL 2
GPIO
GP50/RI2*/IRQ3
GP51/DCD2*/IRQ4
GP52/RXD2/IRRX/IRQ5
GP53/TXD2/IRTX/IRQ7
GP54/DSR2*/IRQ9
GP55/RTS2*/IRQ10
GP56/CTS2*/IRQ11
GP57/DTR2*/IRQ15
VREF
VTR
AVSS
VSS3
VSS2
VSS1
VSS0
745120-002
JOY
GP10/J1B1
GP11/J1B2
GP12/J2B1
GP13/J2B2
GP14/J1X
GP15/J1Y
GP16/J2X
GP17/J2Y
GP25/MIDI_IN
GP26/MIDI_OUT
GPIO
P17/GP20
P16/GP21
P12/GP22
SYSOPT/GP24
LED1/GP60
LED2/GP61
IOSMI*/GP27
FDC_PP/DDRC/GP43
KEY/MOUSE
KDAT
KCLK
MDAT
MCLK
GP36/KBDRST
GP37/A20M
PARALLEL
DIR/INIT
STEP/SLCTIN
INDEX*/PD0
TRK0*/PD1
WRTPRT*/PD2
RDATA*/PD3
DSKCHG*/PD4
PD5
MTR0*/PD6
PD7
WGATE*/SLCT
WDATA*/PE
MTR1*/BUSY
DS1/ACK
HDSEL/ERR
DRVDEN0/ALF
DS0/STROBE
IR
IRRX2/GP34
IRTX2/GP35
FAN
GP32/FAN2
GP33/FAN1
FAN_TACH2/GP30
FAN_TACH1/GP31
CLOCK
CLKI
CLKI32
ROOM=SIO
R3E2
R3D6
R3D5
R3D3
R3D2
R3D1
R3D4
R2D1
R3E1
C3D10
C3E1
SB3V
SUSTAT_L
SMBUS_CTRL
IDROM_WE_L
CPU_SM_WP
SIO_GP24_SYSOPT
SIO_GP24_SYSOPT | BASE I/O ADDRESS
0 | 0X02EH
1 | 0X04EH
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
LPC47M102 SUPER I/O
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:02:58 2002
PAGE:
48

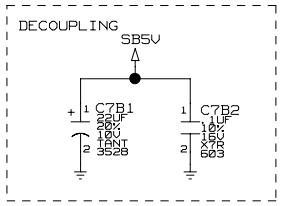


ROOM=PS2_MOUSE

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET		
PAGE TITLE: PS2 KEYBOARD AND MOUSE		REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:58 2002	PAGE: 49

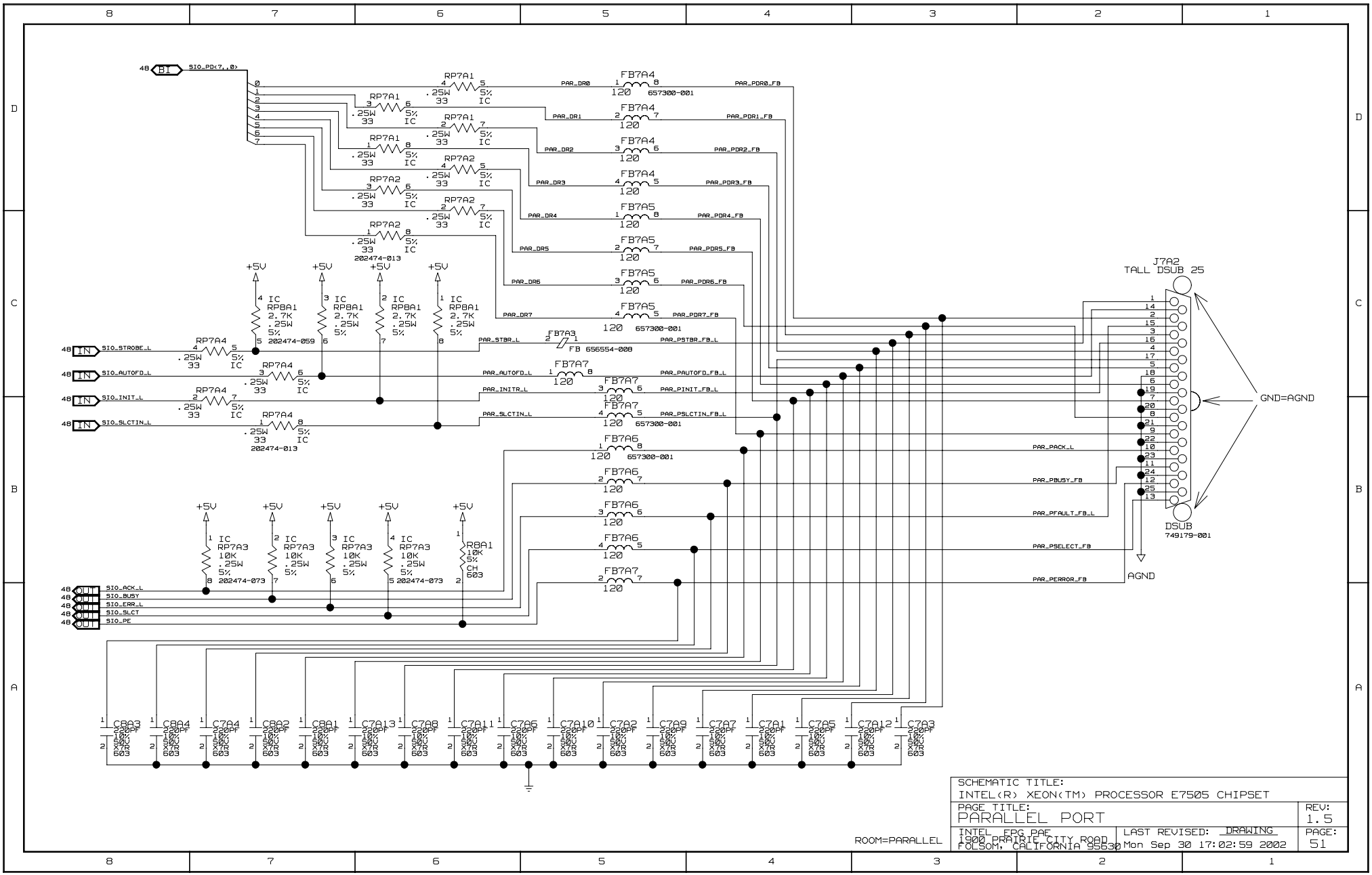


DECOUPLING

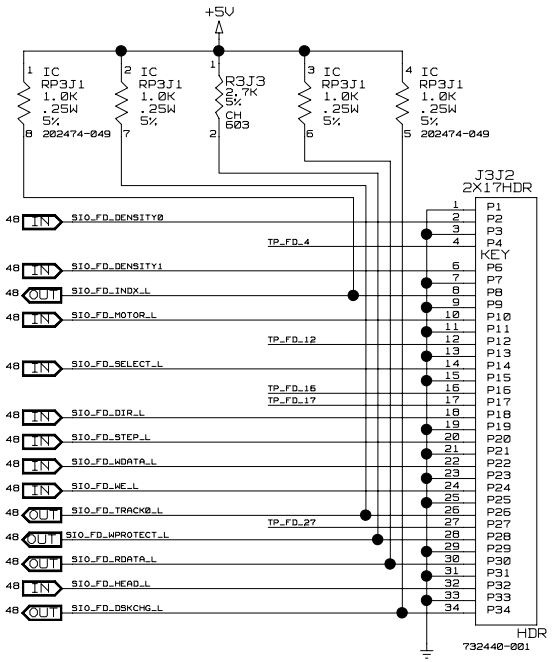


ROOM=SERIAL

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET		
PAGE TITLE: SERIAL PORTS		REV: 1.5
INTEL EPS PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:58 2002	PAGE: 50

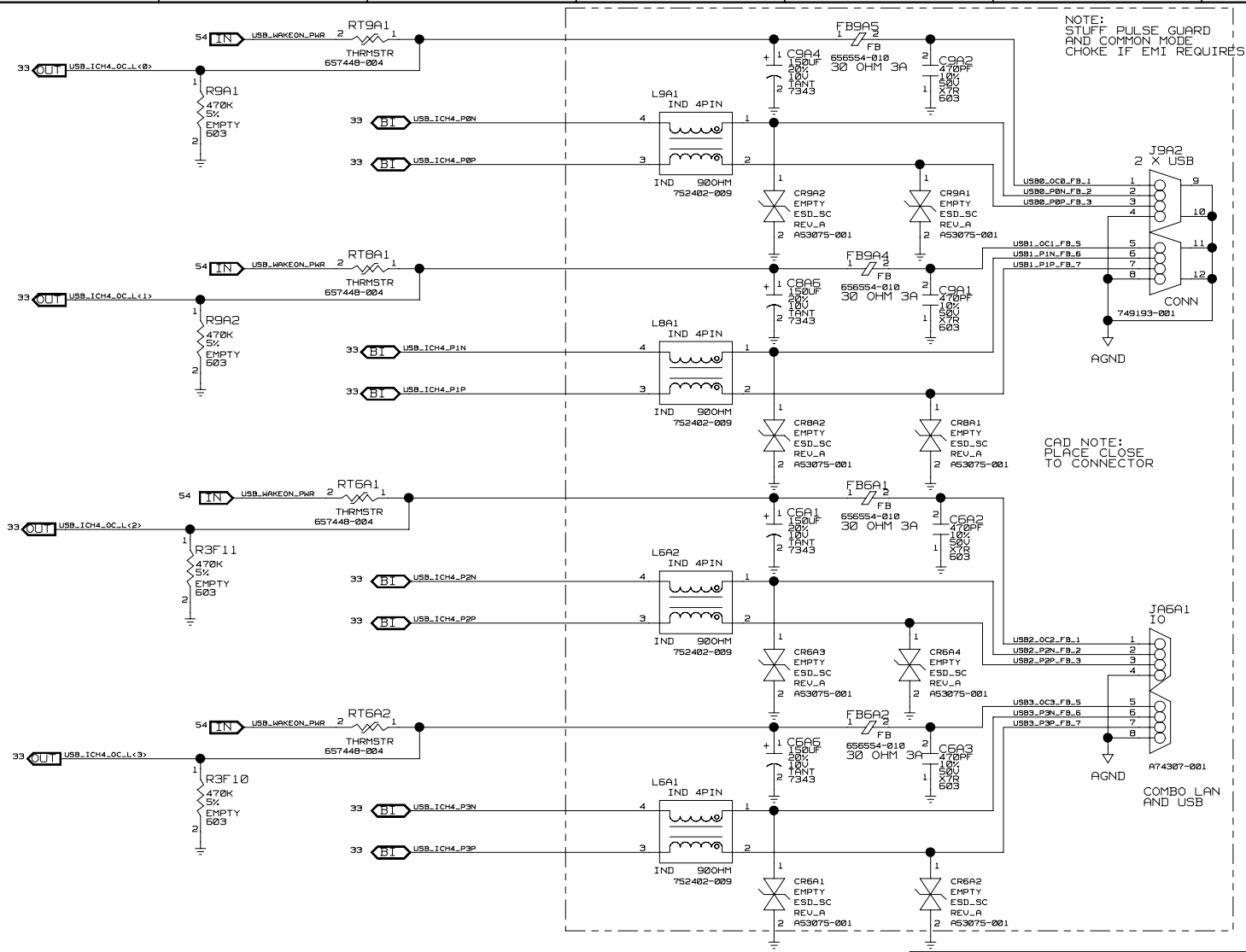


SCHEMATIC TITLE:	
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET	
PAGE TITLE: PARALLEL PORT	REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:59 2002
ROOM=PARALLEL	PAGE: 51



ROOM=FLOPPY

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET		
PAGE TITLE: FLOPPY DRIVE PORT		REV: 1.5
INTEL EPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:02:59 2002	PAGE: 52



SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET

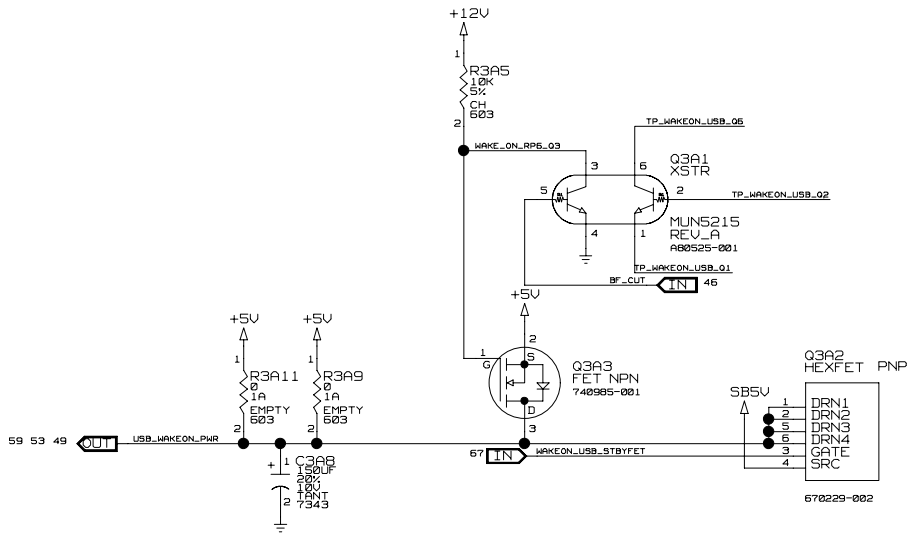
PAGE TITLE:
USB CONNECTORS

REV:
1.5

INTEL FDG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:00 2002

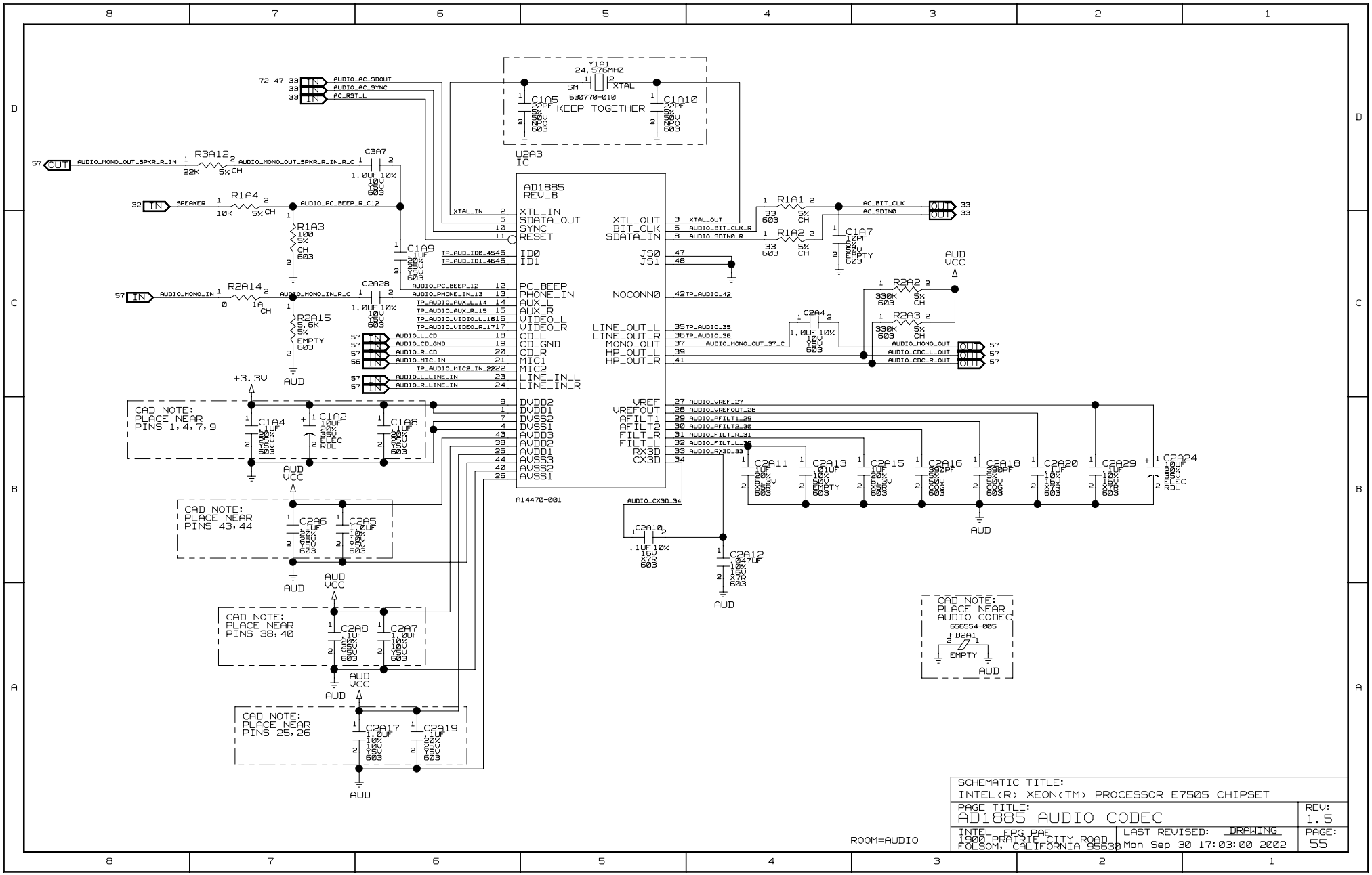
PAGE:
53

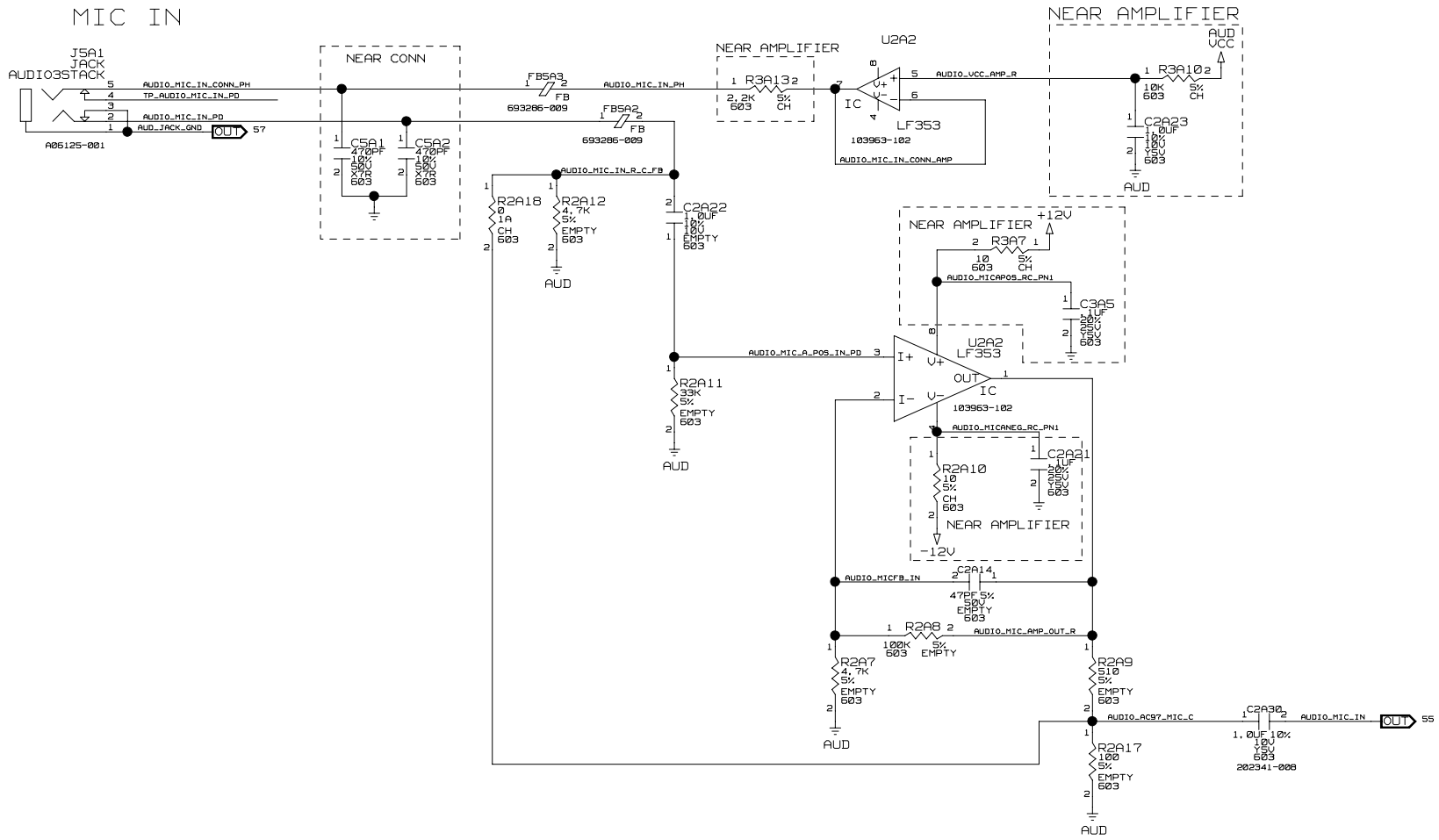


PNP FET	NPN FET	STATE
1	1	HW ON
0	0	S3

ROOM=USB_WAKE

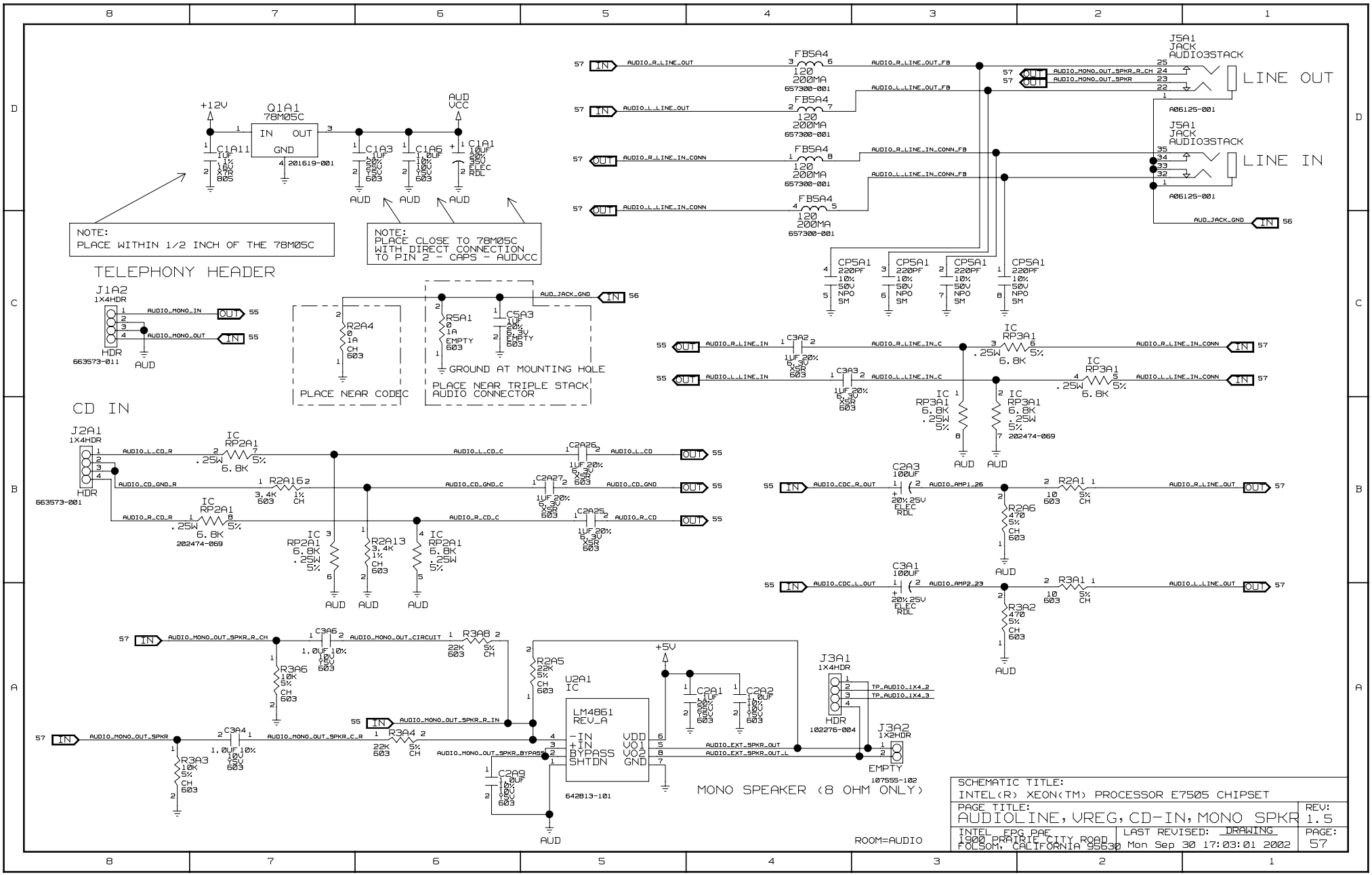
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET		
PAGE TITLE: WAKE ON USB		REV: 1.5
INTEL EPS PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:00 2002	PAGE: 54

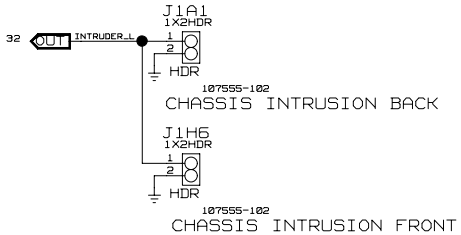

U2A3
IC
AD1885
REV_B
A14470-001
Y1A1
24.576MHZ
XTAL
SM
630770-010
KEEP TOGETHER
AUDIO_AC_SDOUT
AUDIO_AC_SYNC
AC_RST_L
AUDIO_MONO_OUT_SPKR_R_IN
AUDIO_MONO_OUT_SPKR_R_IN_R_C
SPEAKER
AUDIO_PC_BEEP_R_C12
AUDIO_MONO_IN
AUDIO_MONO_IN_R_C
AUDIO_PC_BEEP_12
AUDIO_PHONE_IN_13
TP_AUDIO_AUX_L_14
TP_AUDIO_AUX_R_15
TP_AUDIO_VIDIO_L_16
TP_AUDIO_VIDEO_R_17
AUDIO_L_CD
AUDIO_CD_GND
AUDIO_R_CD
AUDIO_MIC_IN
TP_AUDIO_MIC2_IN_22
AUDIO_L_LINE_IN
AUDIO_R_LINE_IN
XTL_IN
SDATA_OUT
SYNC
RESET
ID0
ID1
PC_BEEP
PHONE_IN
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_GND
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
DVDD2
DVDD1
DVSS2
DVSS1
AVDD3
AVDD2
AVDD1
AVSS3
AVSS2
AVSS1
XTL_OUT
BIT_CLK
SDATA_IN
JS0
JS1
NOCONN0
LINE_OUT_L
LINE_OUT_R
MONO_OUT
HP_OUT_L
HP_OUT_R
VREF
VREFOUT
AFILT1
AFILT2
FILT_R
FILT_L
RX3D
CX3D
AUDIO_CX3D_34
AUDIO_BIT_CLK_R
AUDIO_SDIN0_R
AUDIO_MONO_OUT_37_C
TP_AUDIO_35
TP_AUDIO_36
TP_AUDIO_42
AUDIO_VREF_27
AUDIO_VREFOUT_28
AUDIO_AFILT1_29
AUDIO_AFILT2_30
AUDIO_FILT_R_31
AUDIO_FILT_L_32
AUDIO_RX3D_33
AC_BIT_CLK
AC_SDIN0
AUDIO_MONO_OUT
AUDIO_CDC_L_OUT
AUDIO_CDC_R_OUT
+3.3V
AUD
VCC
CAD NOTE:
PLACE NEAR
PINS 1,4,7,9
CAD NOTE:
PLACE NEAR
PINS 43,44
CAD NOTE:
PLACE NEAR
PINS 38,40
CAD NOTE:
PLACE NEAR
PINS 25,26
CAD NOTE:
PLACE NEAR
AUDIO CODEC
656554-005
FB2A1
EMPTY
ROOM=AUDIO
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
AD1885 AUDIO CODEC
REV:
1.5
INTEL FDG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:03:00 2002
PAGE:
55



ROOM=AUDIO

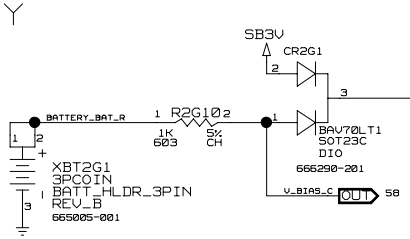
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET		
PAGE TITLE: MICROPHONE IN		REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:01 2002	PAGE: 56


NOTE:
PLACE WITHIN 1/2 INCH OF THE 78M05C
NOTE:
PLACE CLOSE TO 78M05C
WITH DIRECT CONNECTION
TO PIN 2 - CAPS - AUDVCC
TELEPHONY HEADER
CD IN
PLACE NEAR CODEC
PLACE NEAR TRIPLE STACK
AUDIO CONNECTOR
GROUND AT MOUNTING HOLE
LINE OUT
LINE IN
MONO SPEAKER (8 OHM ONLY)
LM4861
REV_A
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
AUDIOLINE, VREG, CD-IN, MONO SPKR
REV: 1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:03:01 2002
PAGE: 57
ROOM=AUDIO



CHASSIS INTRUSION

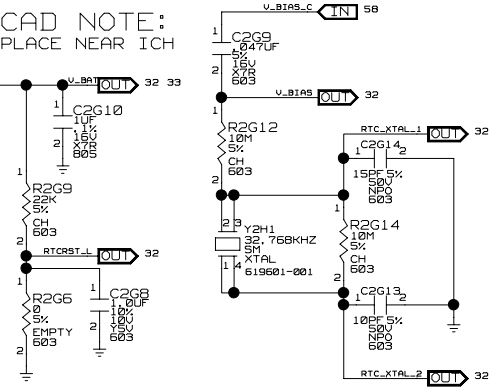
BATTERY



CAD NOTE: DO NOT PLACE BATTERY NEAR MOUNTING HOLES, GROUND OR VIAS

ROOM=BATTERY

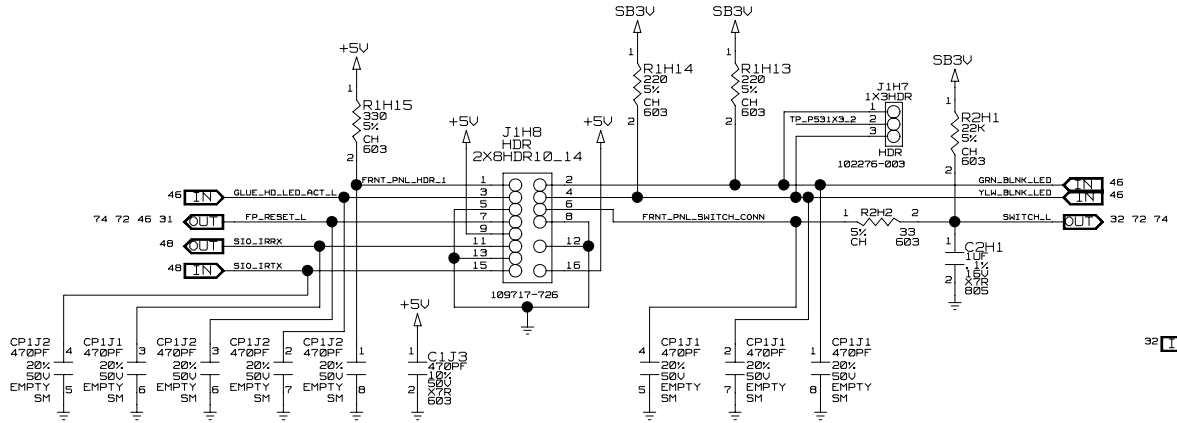
CAD NOTE:
PLACE NEAR ICH



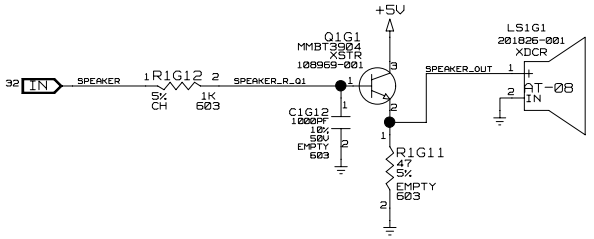
ROOM=INTRUSION
ROOM=BATTERY

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET		
PAGE TITLE: CHASSIS INTRUSION AND BATTERY		REV: 1.5
INTEL_FPG_PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:02 2002	PAGE: 58

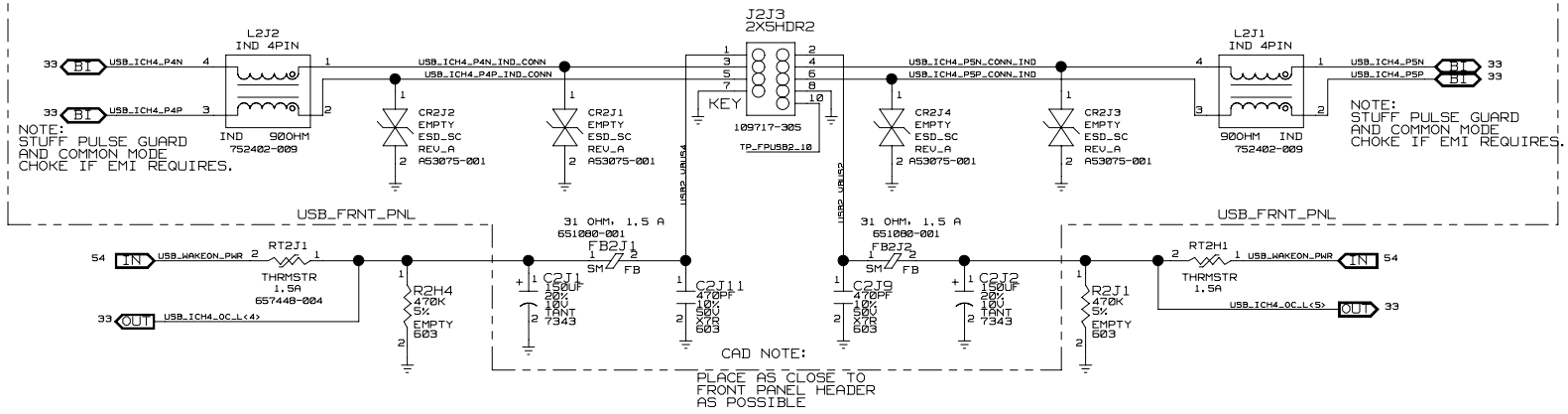
POWER AND LED FRONT PANEL HEADER



SPEAKER

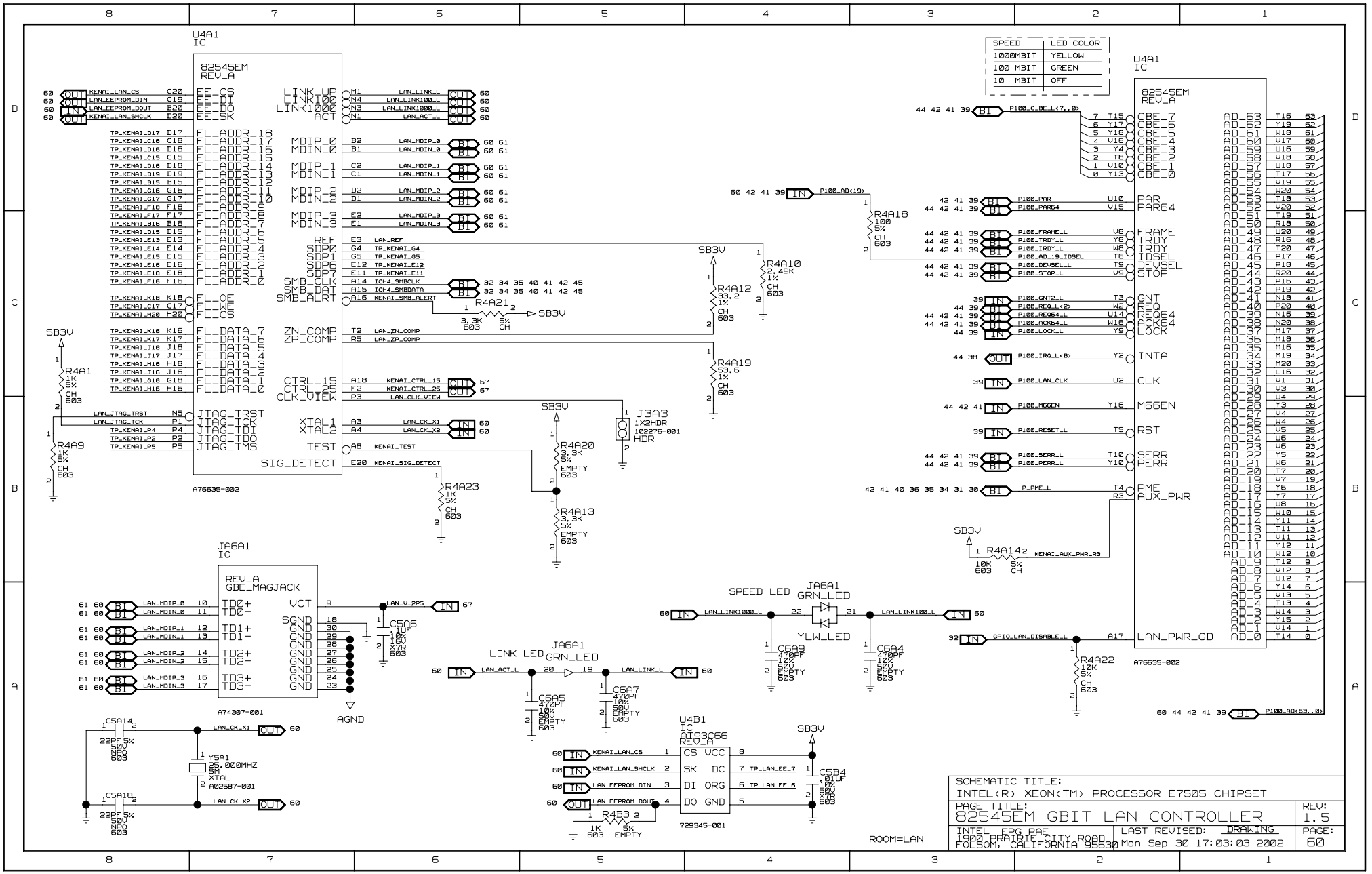


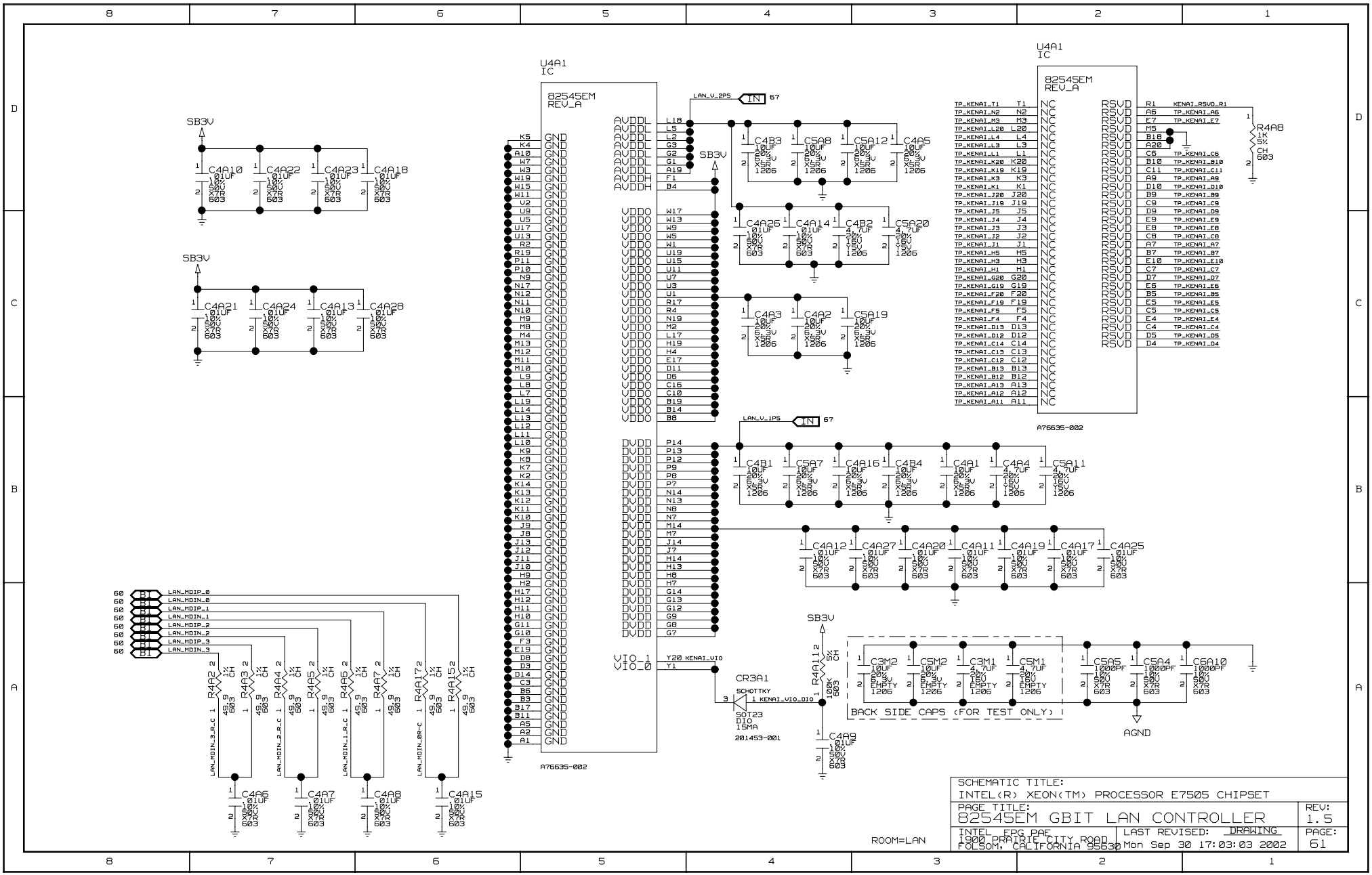
USB 2.0 FRONT PANEL HEADER

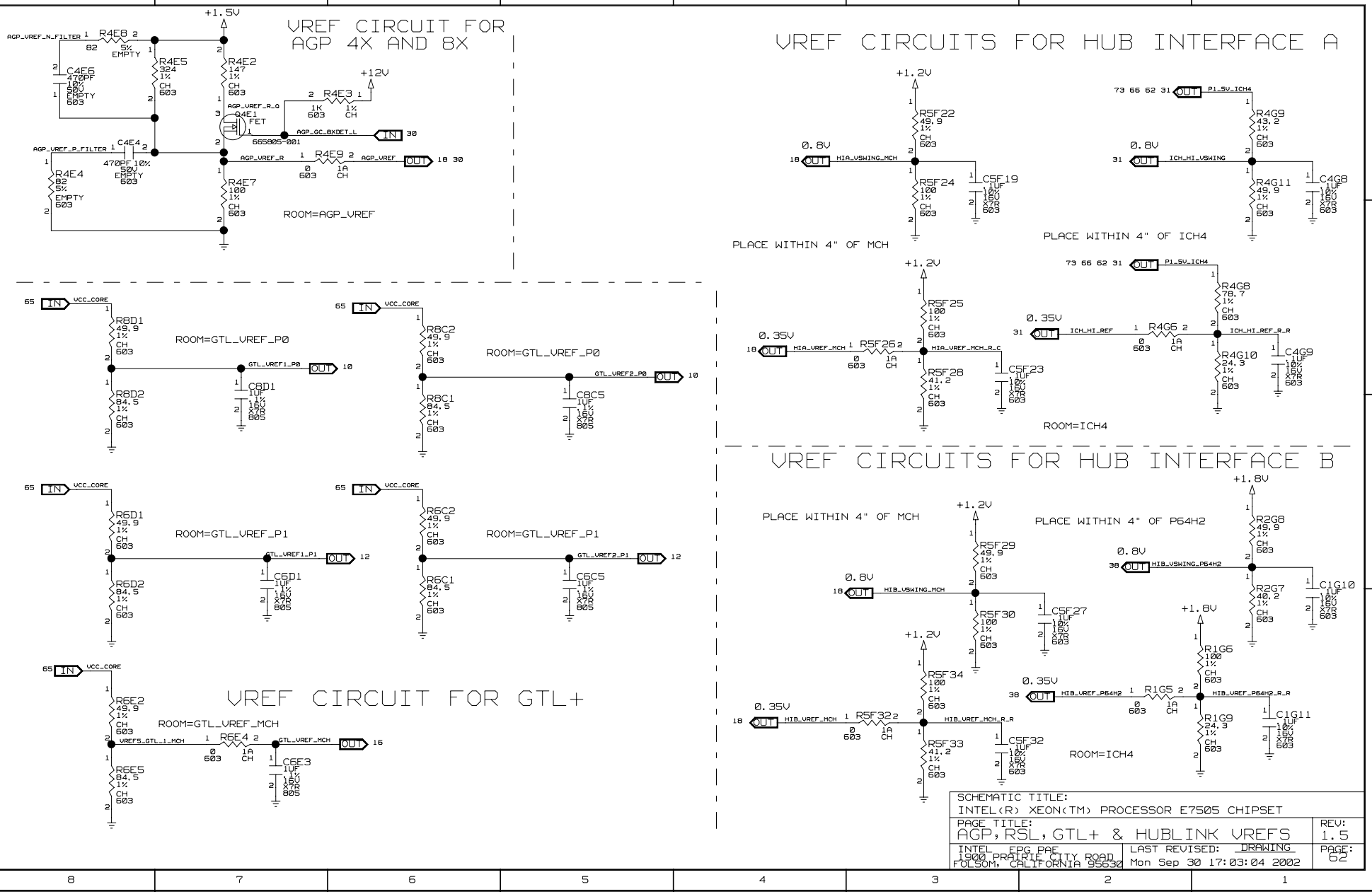


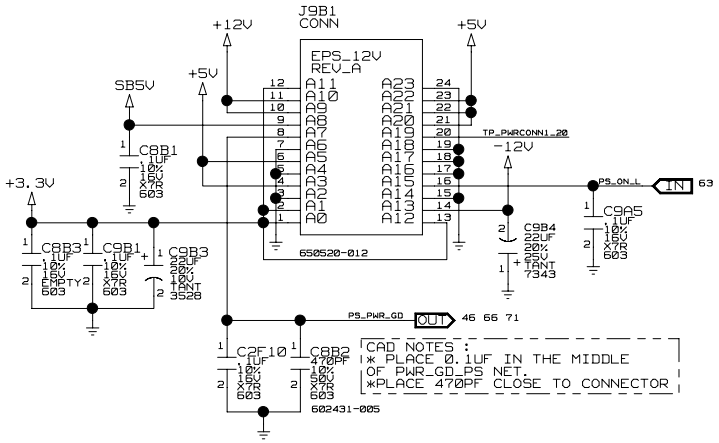
ROOM=USB_FRNT_PNL
ROOM=INTRUSION
ROOM=FRNT_PNL
ROOM=SPEAKER

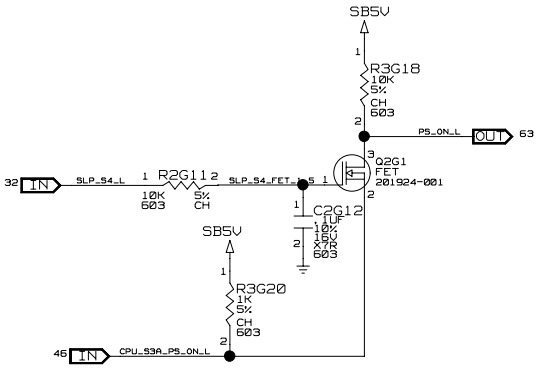
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET	
PAGE TITLE: FRONT PANEL HEADERS & SPEAKER	REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:02 2002
	PAGE: 59

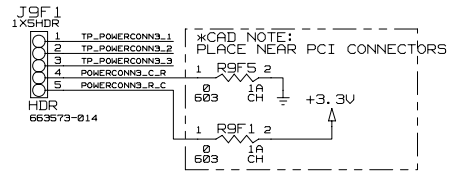

U4A1
IC
82545EM
REV_A
SPEED | LED COLOR
1000MBIT | YELLOW
100 MBIT | GREEN
10 MBIT | OFF
JA6A1
IO
REV_A
GBE_MAGJACK
A76635-002
A74307-001
A02587-001
U4B1
IC
AT93C66
REV_A
729345-001
SB3V
AGND
YSA1
25.000MHZ
XTAL
J3A3
1X2HDR
102276-001
HDR
SPEED LED
LINK LED
GRN_LED
YLW_LED
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
82545EM GBIT LAN CONTROLLER
REV:
1.5
INTEL FDG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:03:03 2002
PAGE:
60
ROOM=LAN

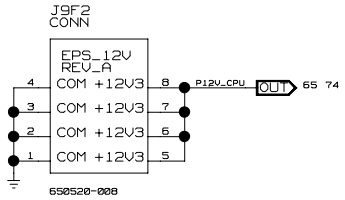

U4A1
IC
82545EM
REV_A
A76535-002
SB3V
LAN_V_2P5
LAN_V_1P5
IN 67
AVDDL
AVDDH
VDDO
DVDD
VIO_1
VIO_0
Y20 KENAI_VIO
Y1
CR3A1
SCHOTTKY
SOT23
DIO
15MA
201453-001
1 KENAI_VIO_DIO
BACK SIDE CAPS (FOR TEST ONLY)
AGND
ROOM=LAN
LAN_MDIP_0
LAN_MDIN_0
LAN_MDIP_1
LAN_MDIN_1
LAN_MDIP_2
LAN_MDIN_2
LAN_MDIP_3
LAN_MDIN_3
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
82545EM GBIT LAN CONTROLLER
REV:
1.5
INTEL FDG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:03:03 2002
PAGE:
61

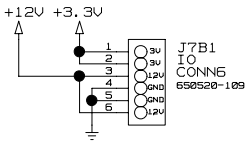

VREF CIRCUIT FOR AGP 4X AND 8X
+1.5V
+12V
AGP_VREF_N_FILTER
R4E8 82 5% EMPTY 603
R4E5 324 1% CH 603
R4E2 147 1% CH 603
R4E3 1K 1% CH 603
C4E6 470PF 10% 50V EMPTY 603
Q4E1 FET 665805-001
AGP_VREF_R_Q
AGP_GC_8XDET_L
IN 30
C4E4 470PF 10% 50V EMPTY 603
AGP_VREF_P_FILTER
AGP_VREF_R
R4E9 0 603 1A CH
AGP_VREF
OUT 18 30
R4E4 82 5% EMPTY 603
R4E7 100 1% CH 603
ROOM=AGP_VREF
VREF CIRCUITS FOR HUB INTERFACE A
+1.2V
0.8V
R5F22 49.9 1% CH 603
R5F24 100 1% CH 603
C5F19 1UF 10% 16V X7R 603
HIA_VSWING_MCH
OUT 18
PLACE WITHIN 4" OF MCH
73 66 62 31
P1_5V_ICH4
R4G9 43.2 1% CH 603
R4G11 49.9 1% CH 603
C4G8 1UF 10% 16V X7R 603
ICH_HI_VSWING
OUT 31
PLACE WITHIN 4" OF ICH4
0.35V
R5F25 100 1% CH 603
R5F28 41.2 1% CH 603
R5F26 0 603 1A CH
HIA_VREF_MCH
HIA_VREF_MCH_R_C
C5F23 1UF 10% 16V X7R 603
R4G8 78.7 1% CH 603
R4G6 0 603 1A CH
ICH_HI_REF
ICH_HI_REF_R_R
R4G10 24.3 1% CH 603
C4G9 1UF 10% 16V X7R 603
ROOM=ICH4
VREF CIRCUITS FOR HUB INTERFACE B
PLACE WITHIN 4" OF MCH
PLACE WITHIN 4" OF P64H2
+1.8V
R5F29 49.9 1% CH 603
R5F30 100 1% CH 603
C5F27 1UF 10% 16V X7R 603
HIB_VSWING_MCH
R2G8 49.9 1% CH 603
R2G7 40.2 1% CH 603
C1G10 1UF 10% 16V X7R 603
HIB_VSWING_P64H2
R5F34 100 1% CH 603
R5F33 41.2 1% CH 603
R5F32 0 603 1A CH
HIB_VREF_MCH
HIB_VREF_MCH_R_R
C5F32 1UF 10% 16V X7R 603
R1G6 100 1% CH 603
R1G5 0 603 1A CH
HIB_VREF_P64H2
HIB_VREF_P64H2_R_R
R1G9 24.3 1% CH 603
C1G11 1UF 10% 16V X7R 603
ROOM=ICH4
R8D1 49.9 1% CH 603
R8D2 84.5 1% CH 603
C8D1 1UF 1% 16V X7R 805
GTL_VREF1_P0
ROOM=GTL_VREF_P0
R8C2 49.9 1% CH 603
R8C1 84.5 1% CH 603
C8C5 1UF 1% 16V X7R 805
GTL_VREF2_P0
R6D1 49.9 1% CH 603
R6D2 84.5 1% CH 603
C6D1 1UF 1% 16V X7R 805
GTL_VREF1_P1
ROOM=GTL_VREF_P1
R6C2 49.9 1% CH 603
R6C1 84.5 1% CH 603
C6C5 1UF 1% 16V X7R 805
GTL_VREF2_P1
VREF CIRCUIT FOR GTL+
R6E2 49.9 1% CH 603
R6E5 84.5 1% CH 603
R6E4 0 603 1A CH
VREFS_GTL_1_MCH
C6E3 1UF 1% 16V X7R 805
GTL_VREF_MCH
ROOM=GTL_VREF_MCH
VCC_CORE
IN 65
OUT 10 12 16
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
AGP, RSL, GTL+ & HUBLINK VREFS
REV:
1.5
INTEL FPS PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:03:04 2002
PAGE:
62





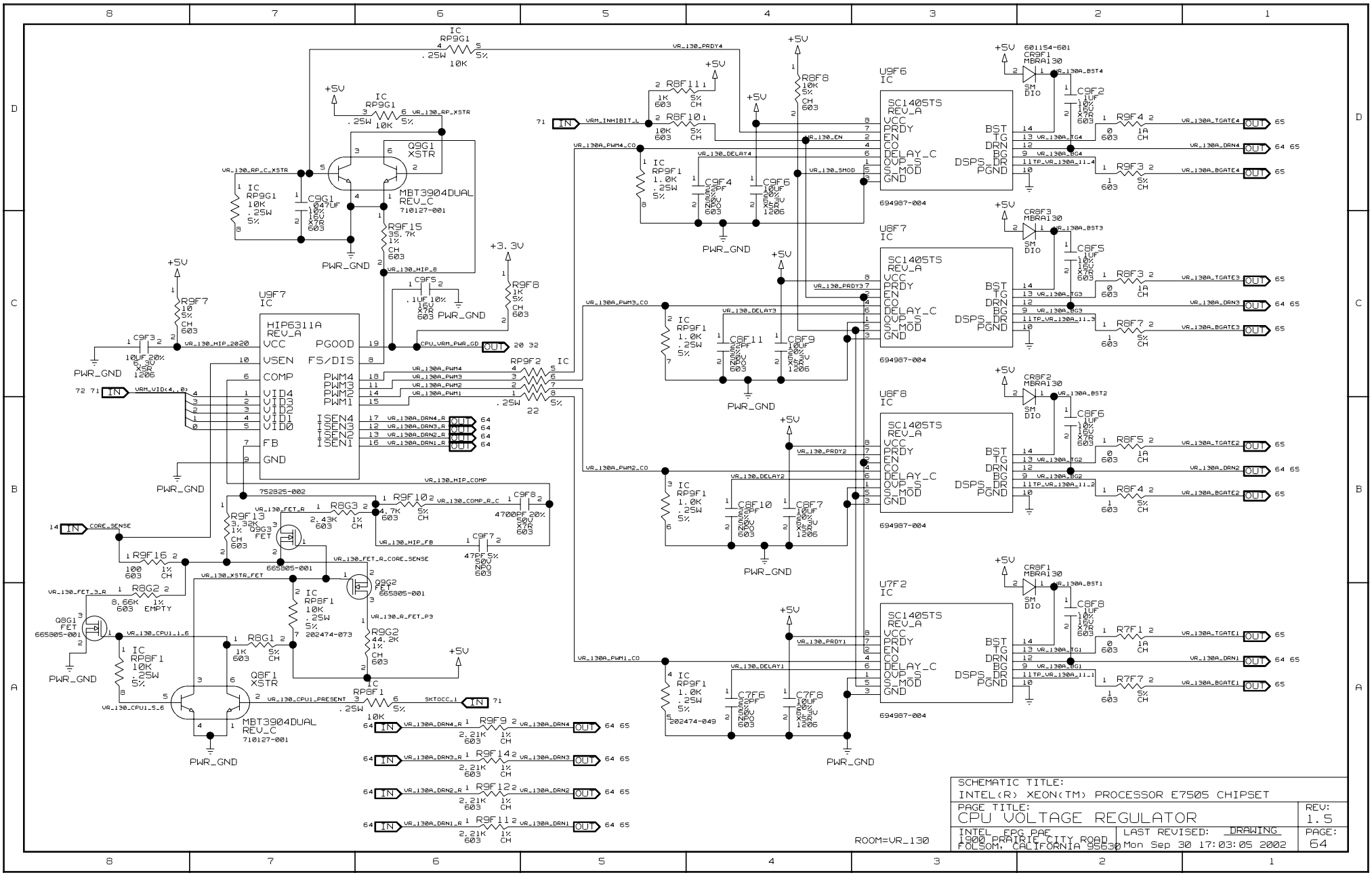


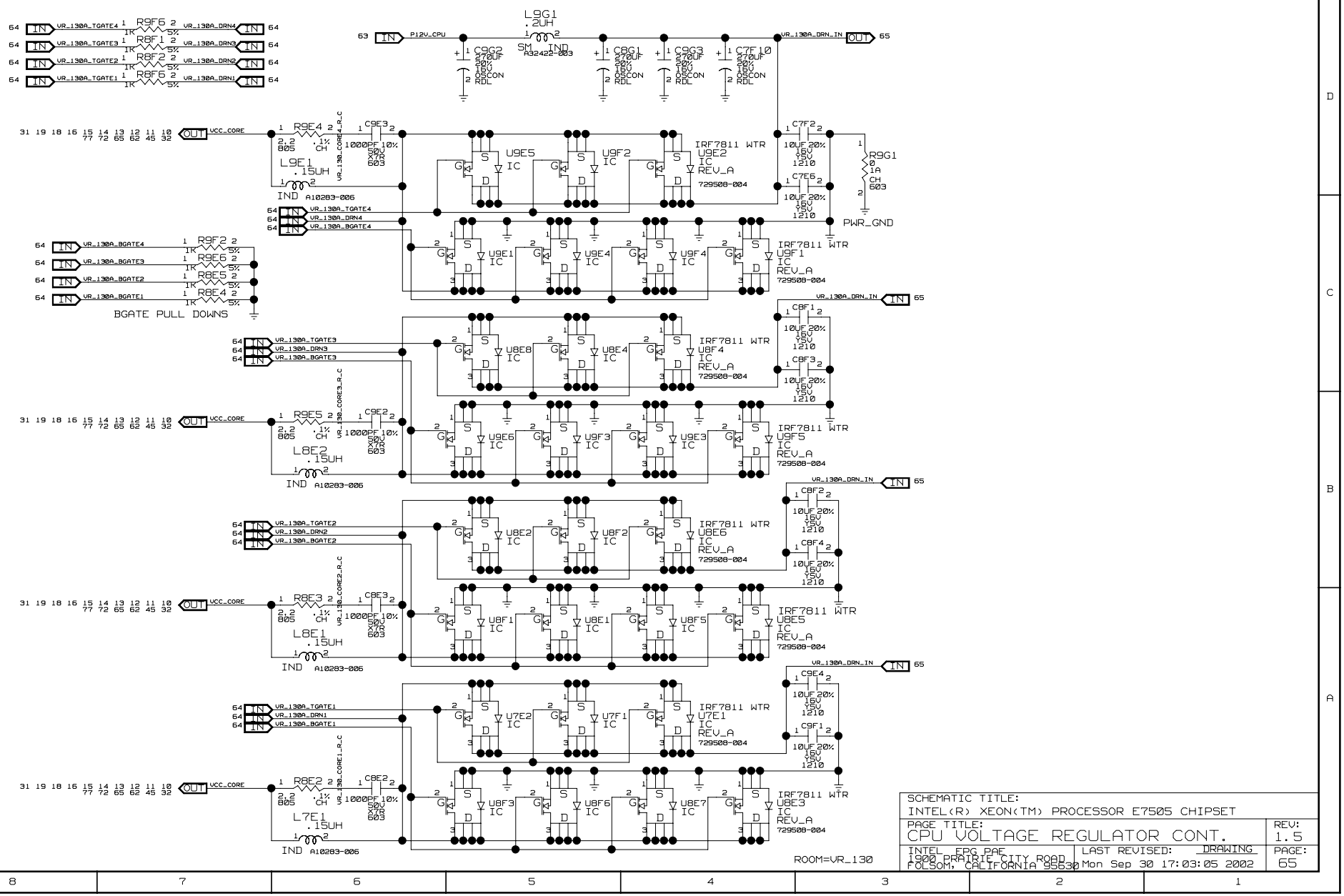




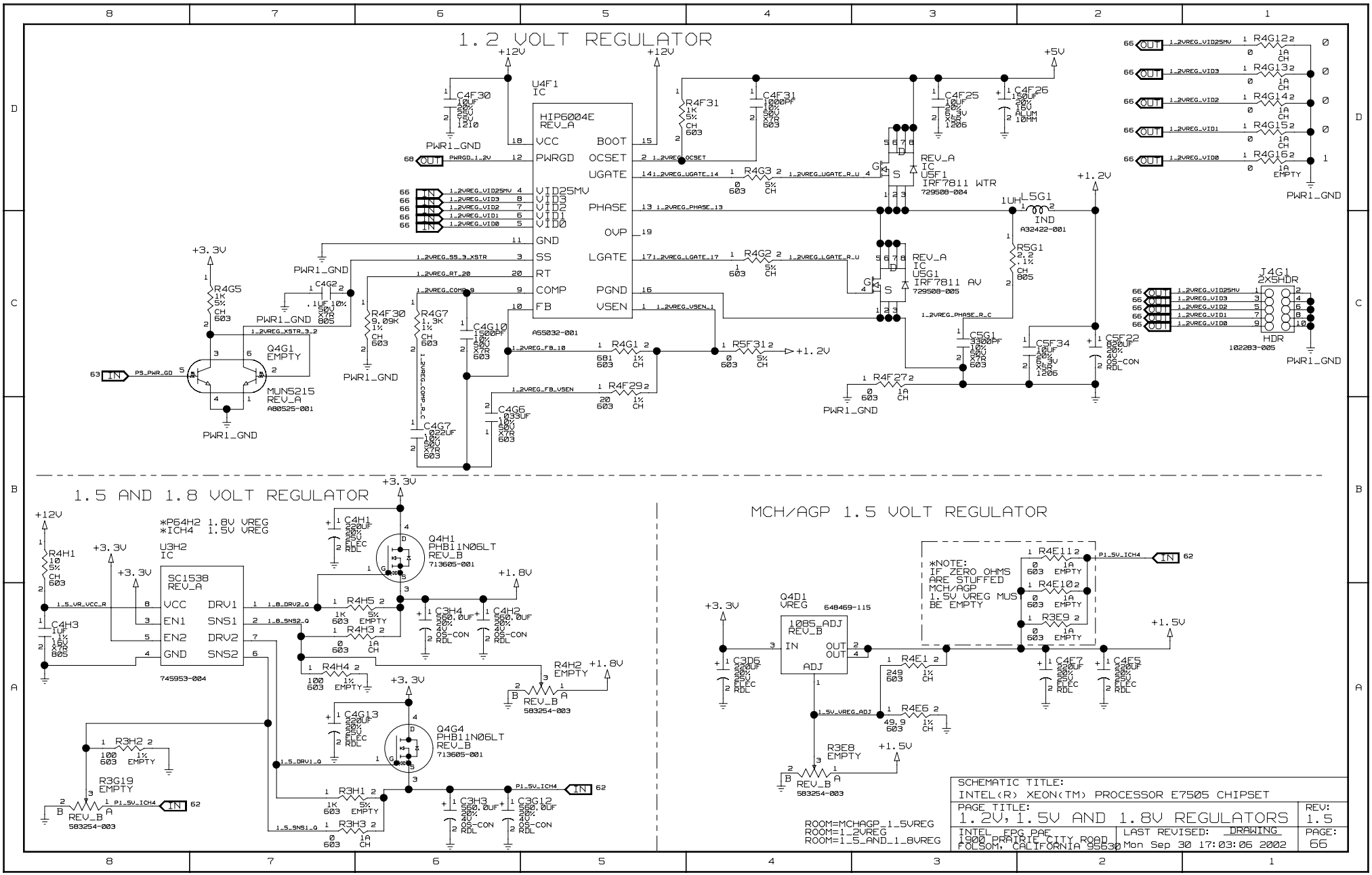
ROOM=PWRCONN_BASE

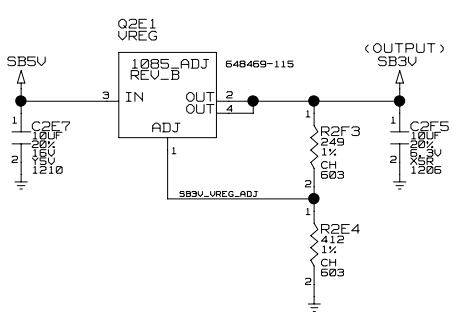
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET		
PAGE TITLE: POWER SUPPLY CONNECTORS		REV: 1.5
INTEL EPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:04 2002	PAGE: 63


SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
CPU VOLTAGE REGULATOR
REV:
1.5
INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:03:05 2002
PAGE:
64
ROOM=VR_130
HIP6311A
REV_A
SC1405TS
REV_A
MBT3904DUAL
REV_C
710127-001
PWR_GND
+5V
+3.3V

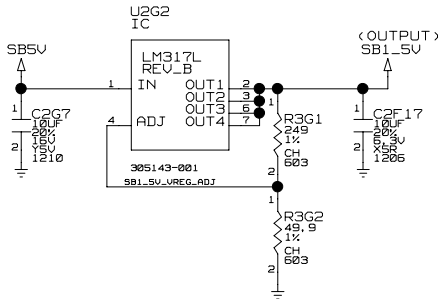


SCHEMATIC TITLE:	
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET	
PAGE TITLE: CPU VOLTAGE REGULATOR CONT.	REV: 1.5
INTEL FDG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:05 2002
	PAGE: 65

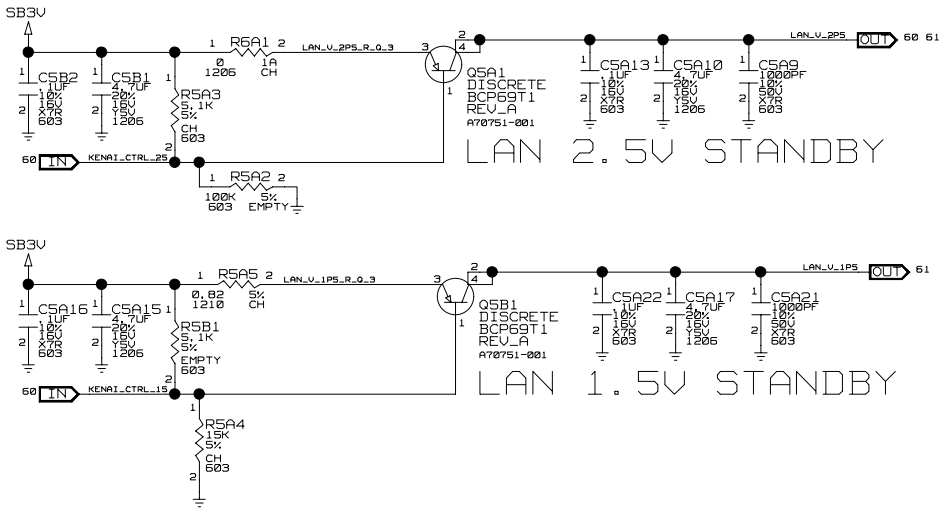

1.2 VOLT REGULATOR
1.5 AND 1.8 VOLT REGULATOR
MCH/AGP 1.5 VOLT REGULATOR
HIP6004E
REV_A
SC1538
REV_A
1085_ADJ
REV_B
MUN5215
REV_A
IRF7811 WTR
IRF7811 AV
PHB11N06LT
REV_B
HDR
2X5HDR
*NOTE:
IF ZERO OHMS
ARE STUFFED
MCH/AGP
1.5V VREG MUST
BE EMPTY
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
1.2V, 1.5V AND 1.8V REGULATORS
REV:
1.5
INTEL FDG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:03:06 2002
PAGE:
66



3V STANDBY



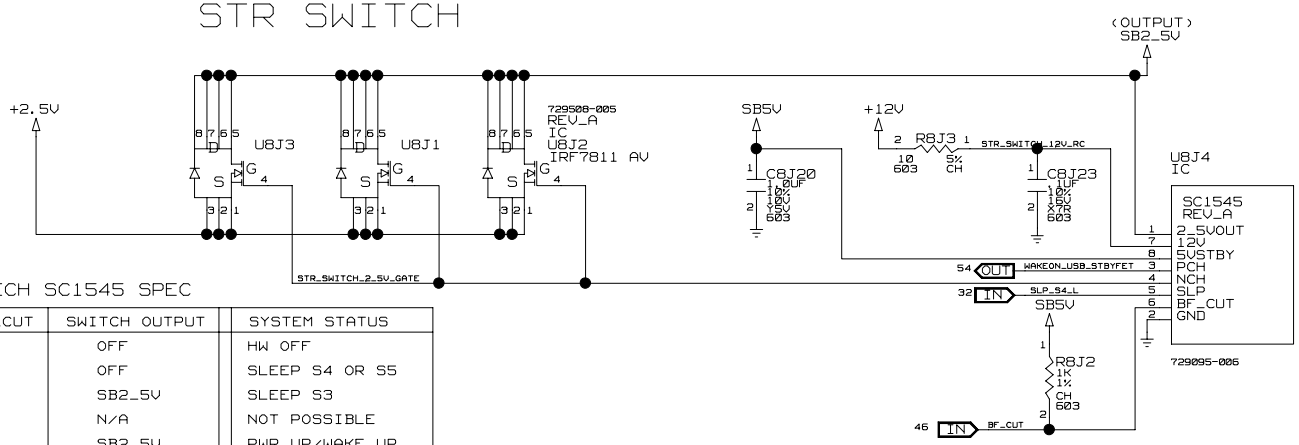
1.5V STANDBY



LAN 2.5V STANDBY

LAN 1.5V STANDBY

STR SWITCH



FROM GLUE 4 SPEC / FROM SEMTECH SC1545 SPEC

PWRGD_PS	SLP_S3_L	BF_CUT_OUT	SLP_S4_L	BF_CUT	SWITCH OUTPUT	SYSTEM STATUS
0	0	HIGH-Z	0	0	OFF	HW OFF
0	0	HIGH-Z	0	1	OFF	SLEEP S4 OR S5
0	0	HIGH-Z	1	1	SB2_5V	SLEEP S3
0	1	HIGH-Z	0	X	N/A	NOT POSSIBLE
0	1	HIGH-Z	1	1	SB2_5V	PWR UP/WAKE UP
1	0	HIGH-Z	0	1	+2_5V	ENTERING S4 OR S5
1	0	HIGH-Z	1	1	SB2_5V	ENTERING S3
1	1	0	0	X	N/A	NOT POSSIBLE
1	1	0	1	0	+2_5V	HW ON

ROOM=3V_STANDBY
ROOM=2_5V_STANDBY
ROOM=1_5V_STANDBY
ROOM=STR_SWITCH

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET

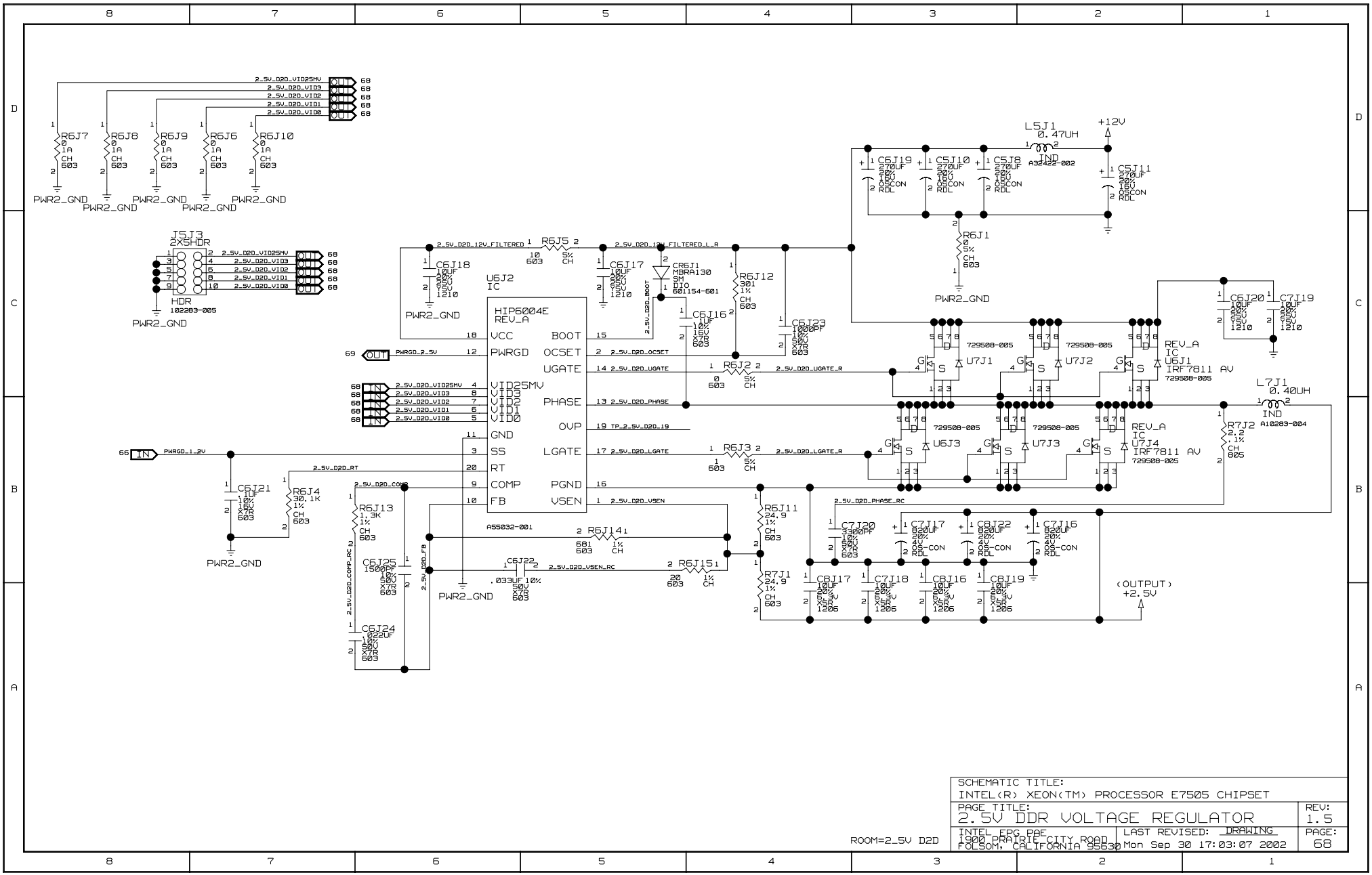
PAGE TITLE:
STANDBY VREGS AND STR SWITCH

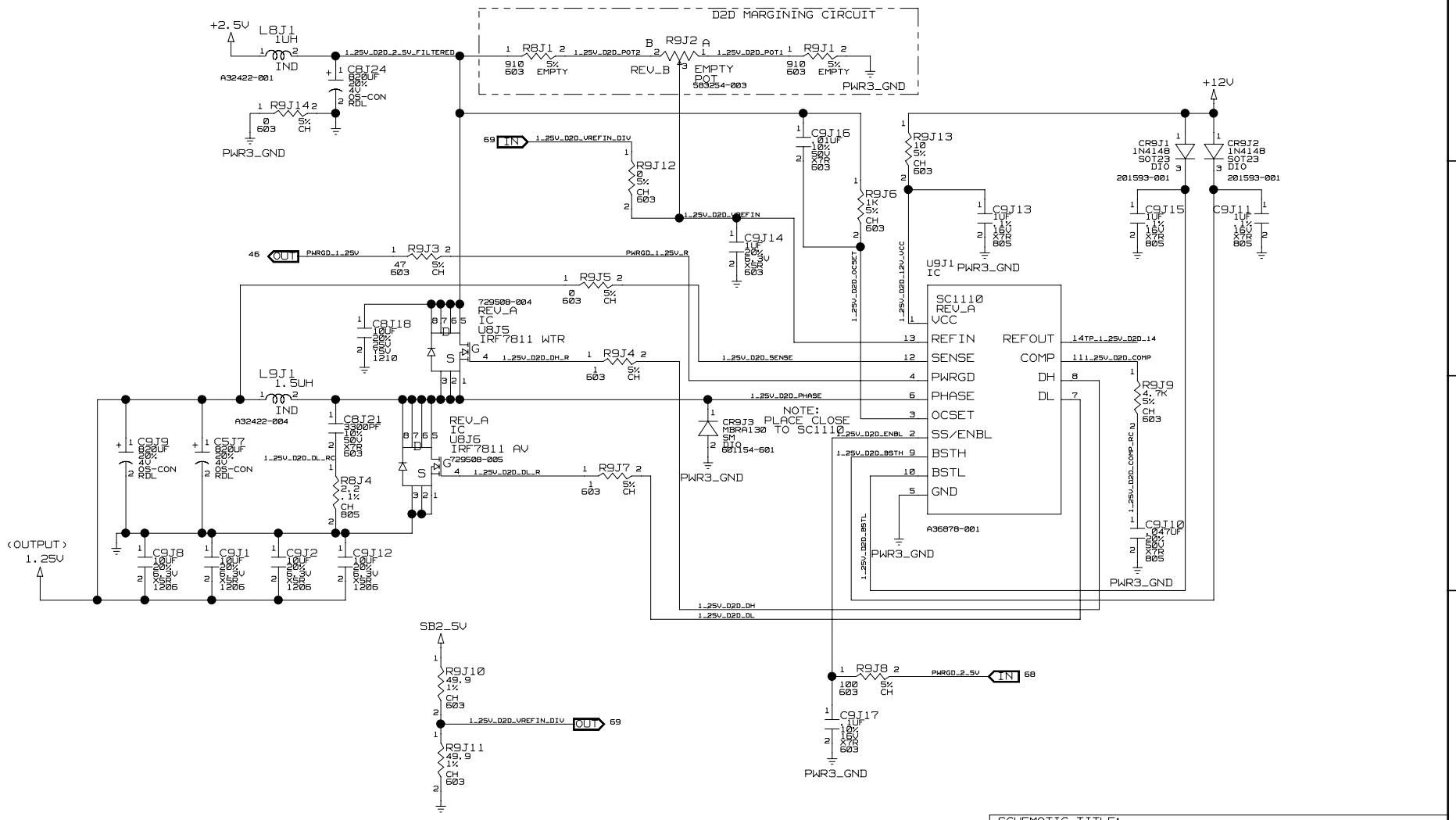
REV: 1.5

INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:06 2002

PAGE: 67


2_5V_D2D_VID25MV
2_5V_D2D_VID3
2_5V_D2D_VID2
2_5V_D2D_VID1
2_5V_D2D_VID0
R6J7
R6J8
R6J9
R6J6
R6J10
PWR2_GND
J5J3
2X5HDR
HDR
102283-005
U6J2
IC
HIP6004E
REV_A
VCC
PWRGD
VID25MV
VID3
VID2
VID1
VID0
GND
SS
RT
COMP
FB
BOOT
OCSET
UGATE
PHASE
OVP
LGATE
PGND
VSEN
2_5V_D2D_12V_FILTERED
2_5V_D2D_12V_FILTERED_L_R
R6J5
C6J18
C6J17
CR6J1
MBRA130
SM
DIO
601154-601
C6J16
R6J12
C6J23
2_5V_D2D_BOOT
2_5V_D2D_OCSET
2_5V_D2D_UGATE
2_5V_D2D_UGATE_R
R6J2
2_5V_D2D_PHASE
TP_2_5V_D2D_19
2_5V_D2D_LGATE
2_5V_D2D_LGATE_R
R6J3
PWRGD_1_2V
2_5V_D2D_RT
C6J21
R6J4
2_5V_D2D_COMP
R6J13
C6J25
C6J24
2_5V_D2D_COMP_RC
2_5V_D2D_FB
A55032-001
R6J14
C6J22
2_5V_D2D_VSEN_RC
R6J15
2_5V_D2D_VSEN
R6J11
R7J1
2_5V_D2D_PHASE_RC
C7J20
C7J17
C8J22
C7J16
C8J17
C7J18
C8J16
C8J19
L5J1
0.47UH
IND
A32428-002
+12V
C5J19
C5J10
C5J18
C5J11
270UF
20%
16V
OSCON
RDL
R6J1
C5J20
C7J19
10UF
20%
6.3V
X5R
1210
U7J1
U7J2
U6J3
U7J3
729508-005
REV_A
IC
U6J1
IRF7811 AV
U7J4
L7J1
0.40UH
A10283-004
R7J2
2.2
1%
805
(OUTPUT)
+2.5V
ROOM=2_5V D2D
SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:
2.5V DDR VOLTAGE REGULATOR
REV:
1.5
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: DRAWING
Mon Sep 30 17:03:07 2002
PAGE:
68

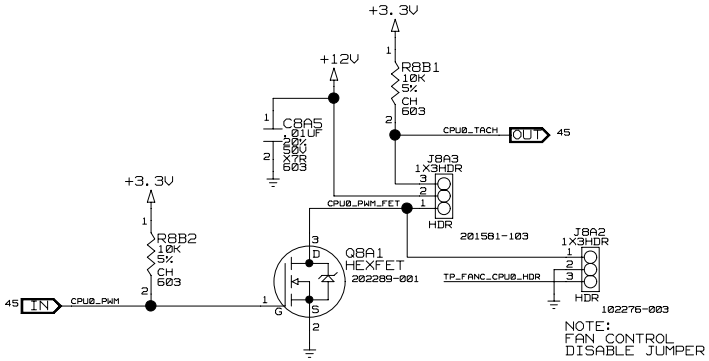


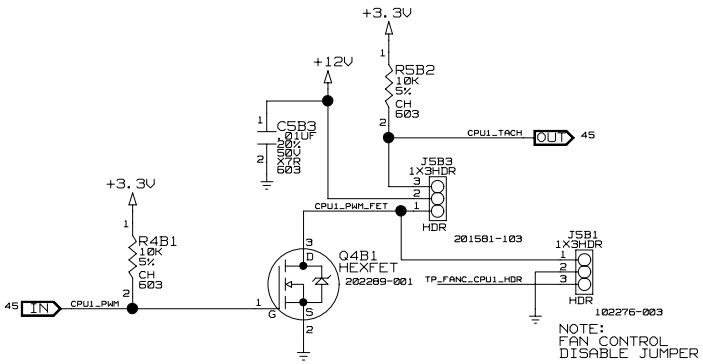
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET		
PAGE TITLE: 1.25V VTT VOLTAGE REGULATOR		REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:07 2002	PAGE: 69

ROOM=1_25V D2D

CAD NOTES:
+12V TRACE TO PNP = 100MILS
12 VOLT TRACE TO FAN HEADERS = 100MILS
BUTTERFLY PLANE 1 ON Q12
LOCATE ON BOARD EDGE NEAR AIR FLOW

CPU FAN HEADERS

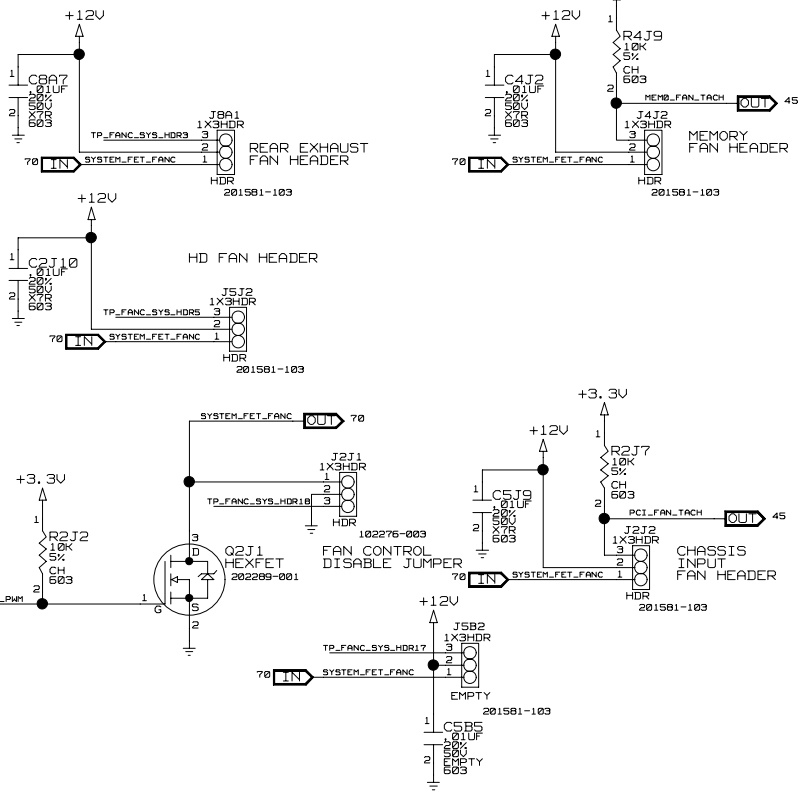




FAN CONTROL DISABLE JUMPER TABLE	
1-2	FANS FULL SPEED
NO JUMPER	FAN SPEED CONTROLLED BY HECETA

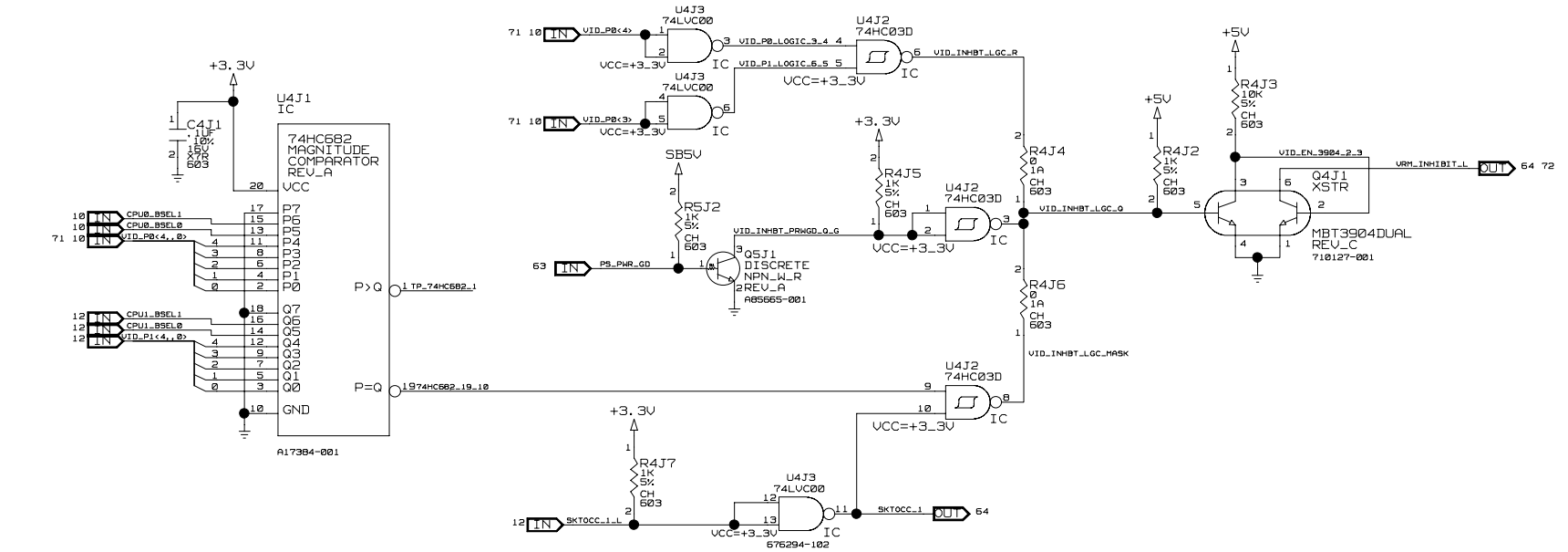
ROOM=FANC_CPU1

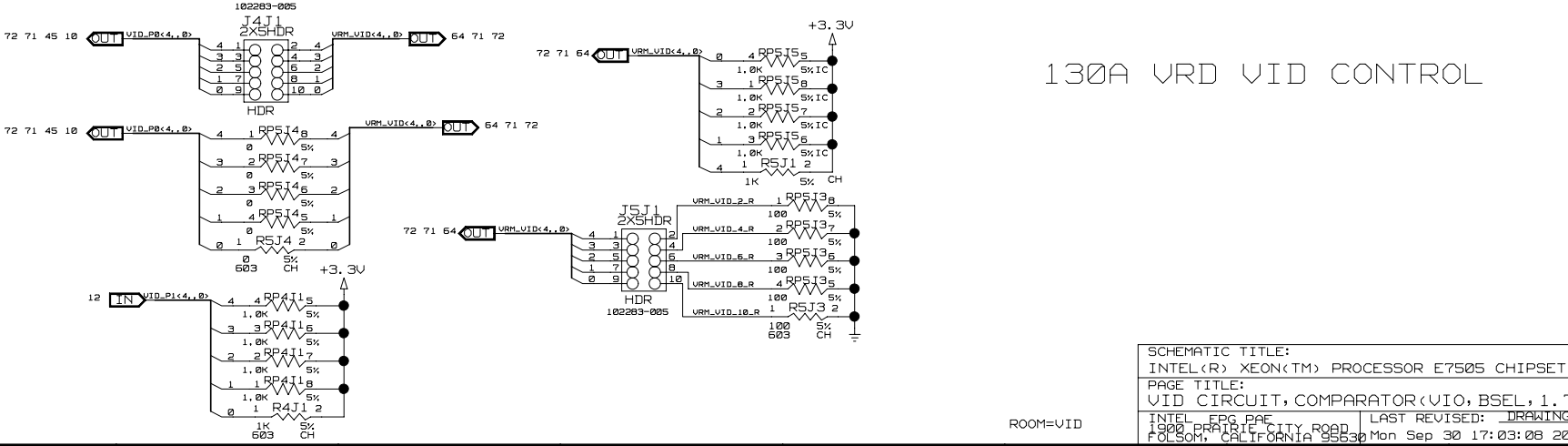
NOTE:
* D-PACK NEEDS 1 SQ PLANE ON TOPSIDE WITH VIA TO GROUND PLANE.
* LOCATE RT3H1 AWAY FROM Q3H3 1-2.



ROOM=FANC_SYSTEM

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET		
PAGE TITLE: FAN CONTROL		REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:08 2002	PAGE: 70



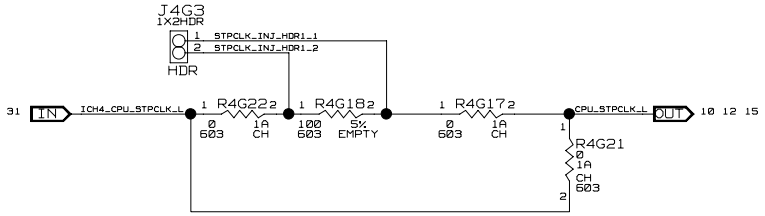


130A VRD VID CONTROL

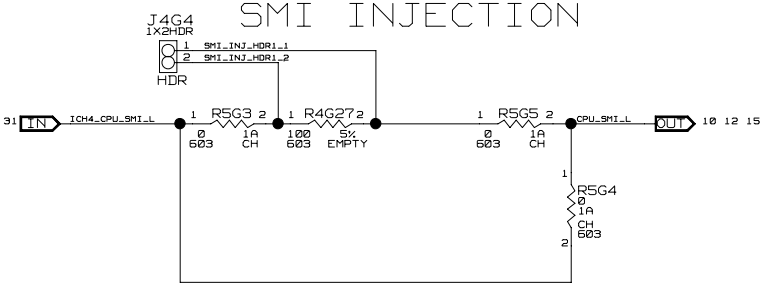
ROOM=VID

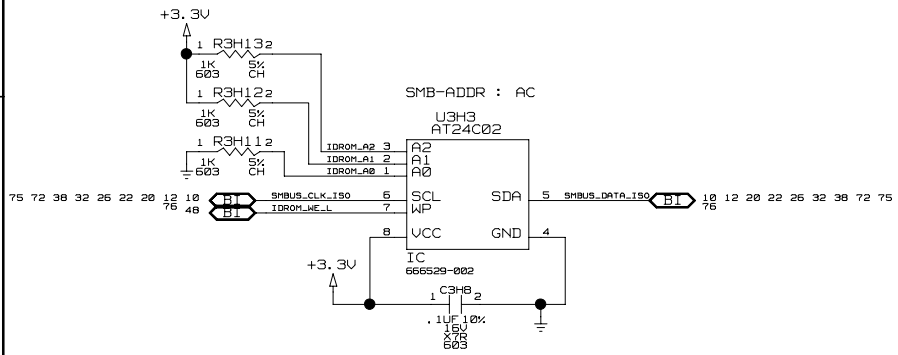
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET	
PAGE TITLE: VID CIRCUIT, COMPARATOR(VIO, BSEL, 1.7V)	REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:08 2002
	PAGE: 71

STPCLK INJECTION



SMI INJECTION





IDROM

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET

PAGE TITLE:
STPCLK, SMI INJ, IDROM

REV:
1.5

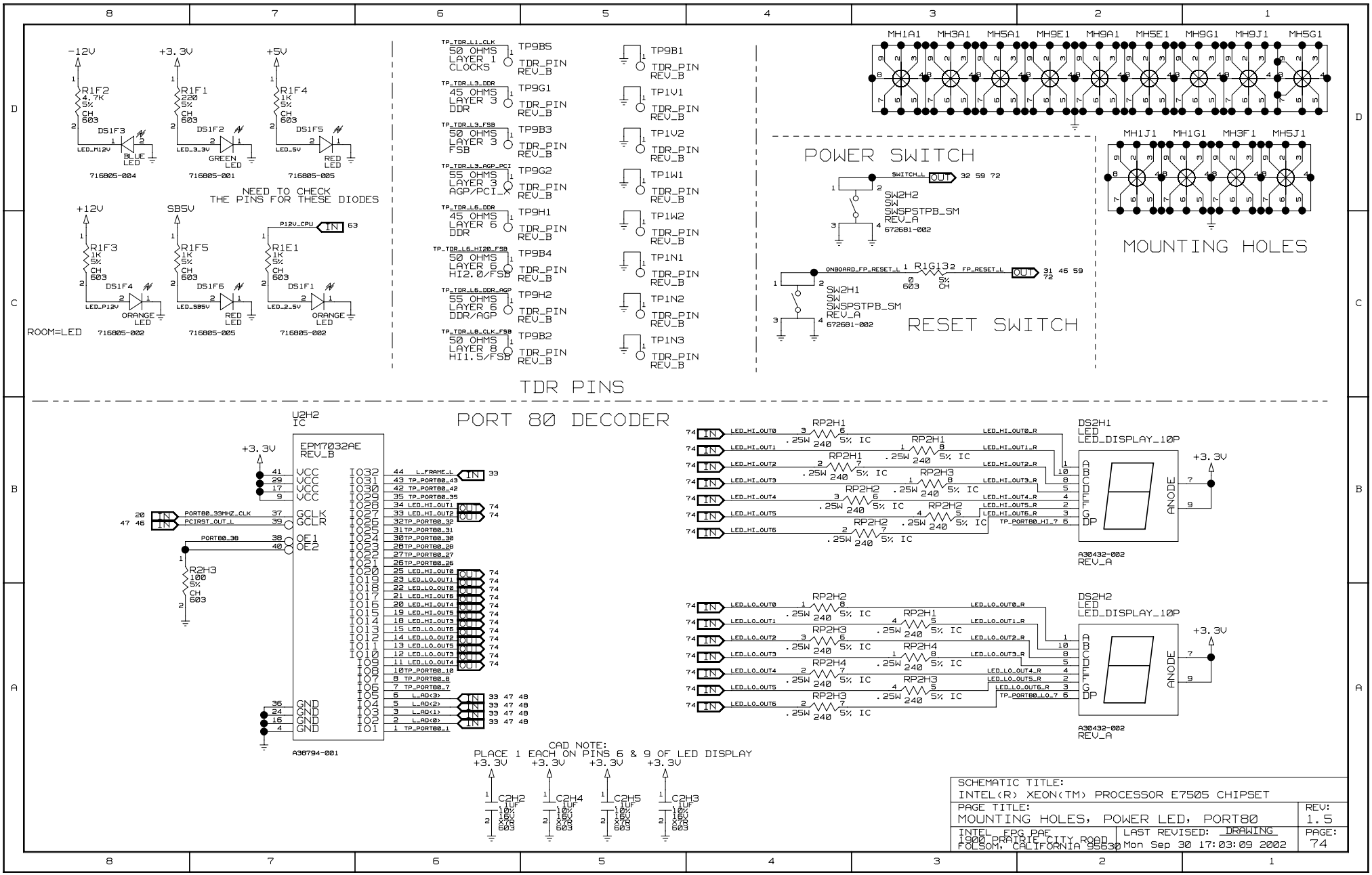
INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:09 2002

PAGE:
72

PAGE INTENTIONALLY BLANK

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET	
PAGE TITLE:	REV: 1.5
INTEL EPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:09 2002
	PAGE: 73



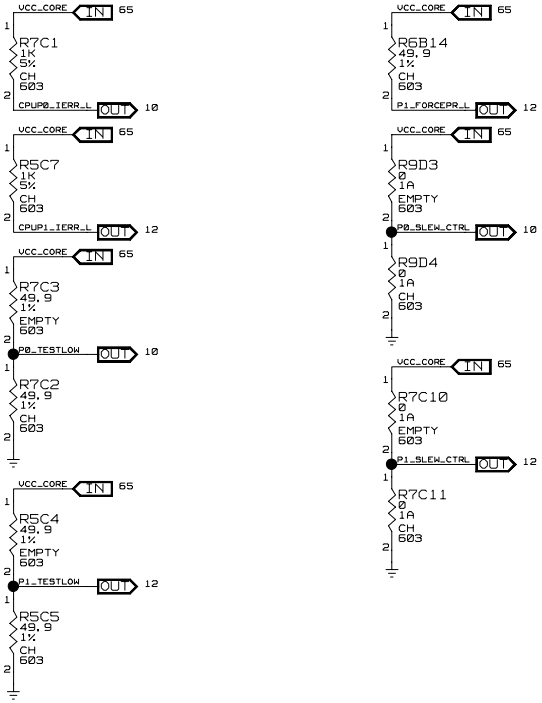
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET	
PAGE TITLE: MOUNTING HOLES, POWER LED, PORT80	REV: 1.5
INTEL FDG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:09 2002
	PAGE: 74

PAGE INTENTIONALLY BLANK

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET	
PAGE TITLE:	REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:10 2002
	PAGE: 75

PAGE INTENTIONALLY BLANK

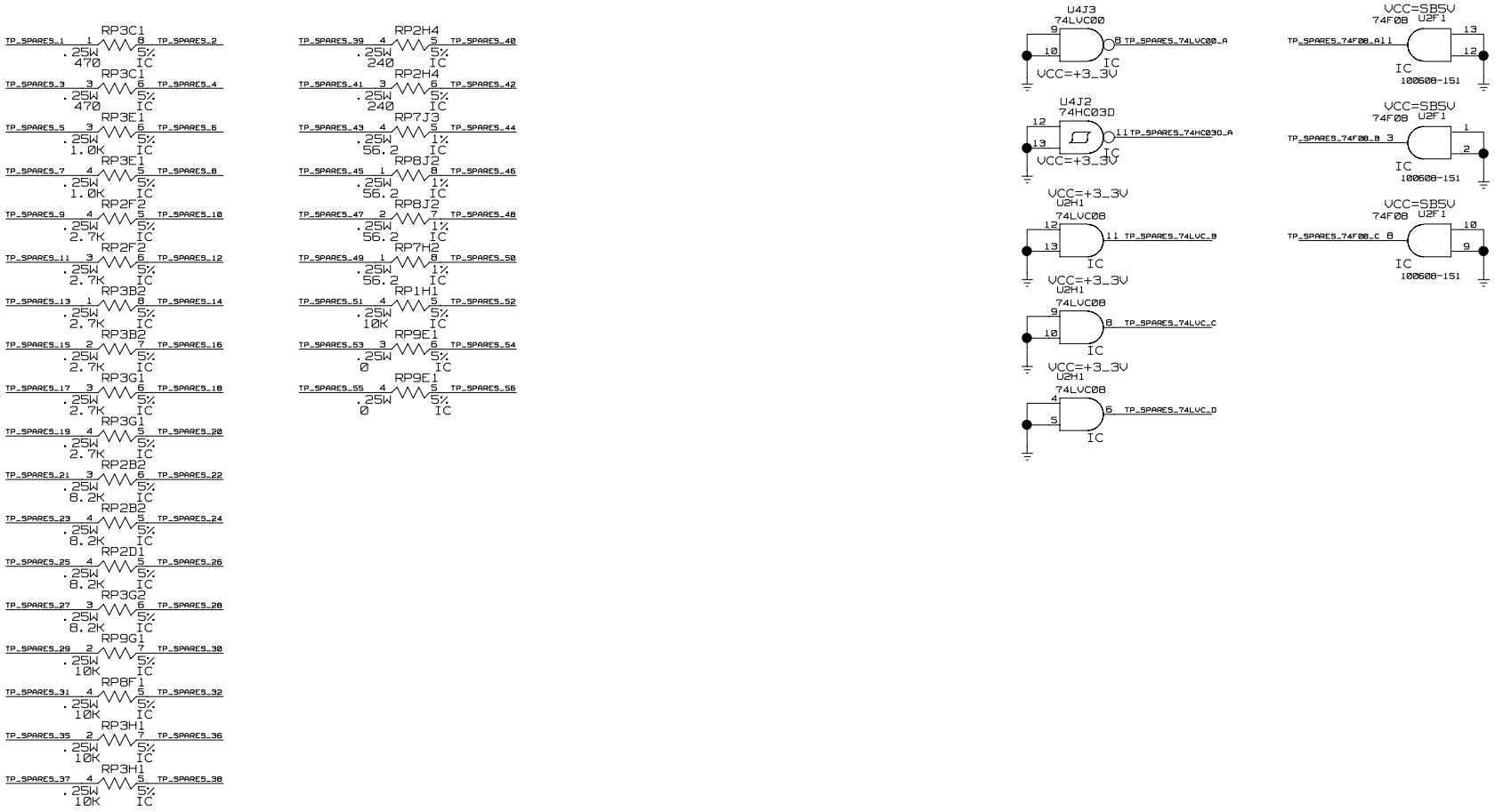
SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET	
PAGE TITLE:	REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:10 2002
	PAGE: 76



SCHEMATIC TITLE:	INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET
PAGE TITLE:	FUTURE PROCESSOR SUPPORT
REV:	1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:10 2002
PAGE:	77

PAGE INTENTIONALLY BLANK

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET	
PAGE TITLE:	REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:10 2002
	PAGE: 78



SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET

PAGE TITLE:
SPARE COMPONENTS

REV: 1.5

INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:11 2002

PAGE: 79

PAGE INTENTIONALLY BLANK

SCHEMATIC TITLE: INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB	
PAGE TITLE:	REV: 1.5
INTEL FPG PAE 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: DRAWING Mon Sep 30 17:03:11 2002
	PAGE: 80

*** Signal Cross-Reference for the entire design ***

1_2VREG_VID0	66
1_2VREG_VID1	66
1_2VREG_VID2	66
1_2VREG_VID3	66
1_2VREG_VID25MV	66
1_25V_D2D_VREFIN_DIV	69
2_5V_D2D_VID0	68
2_5V_D2D_VID1	68
2_5V_D2D_VID2	68
2_5V_D2D_VID3	68
2_5V_D2D_VID25MV	68
5VREF	32 46
80CON_CBL_DET_PRI	37 47
80CON_CBL_DET_SEC	37 47
ACK64_L<1>	34 36
ACK64_L<2>	35 36
AC_BIT_CLK	33 55
AC_RST_L	33 55
AC_SDIN0	33 55
AC_SDOUT	33
AC_SYNC	33
AD<0>	31 34 35
AD<31,,0>	31 34 35
AD<1>	31 34 35
AD<2>	31 34 35
AD<3>	31 34 35
AD<4>	31 34 35
AD<5>	31 34 35
AD<6>	31 34 35
AD<7>	31 34 35
AD<8>	31 34 35
AD<9>	31 34 35
AD<10>	31 34 35
AD<11>	31 34 35
AD<12>	31 34 35
AD<13>	31 34 35
AD<14>	31 34 35
AD<15>	31 34 35
AD<16>	31 34 35
AD<17>	31 34 35
AD<18>	31 34 35
AD<19>	31 34 35
AD<20>	31 34 35
AD<21>	31 34 35
AD<22>	31 34 35
AD<23>	31 34 35
AD<24>	31 34 35
AD<25>	31 34 35
AD<26>	31 34 35
AD<27>	31 34 35
AD<28>	31 34 35
AD<29>	31 34 35
AD<30>	31 34 35
AD<31>	31 34 35
AGP_66MHZ_CLK	20 30
AGP_AD<31,,0>	18 30
AGP_ADSTB0F	18 30
AGP_ADSTB0S	18 30
AGP_ADSTB1F	18 30
AGP_ADSTB1S	18 30
AGP_C_BE_L<3,,0>	18 30
AGP_DBI_HI	18 30
AGP_DBI_LO	18 30
AGP_DEVSEL	18 30
AGP_FRAME	18 30
AGP_GC_8XDET_L	30 62
AGP_GNT	18 30
AGP_IRDY	18 30
AGP_PAR	18 30
AGP_PERR	30
AGP_PRNT_1	30 32
AGP_PRNT_2	30 32
AGP_RBF	18 30
AGP_REQ	18 30
AGP_SBA_L<7,,0>	18 30
AGP_SBSTBF	18 30
AGP_SBSTBS	18 30
AGP_SERR	18 30
AGP_ST<2,,0>	18 30
AGP_STOP	18 30
AGP_TRDY	18 30
AGP_VREF	18 30 62
AGP_VSWING	18
AGP_WBF	18 30
AUDIO_AC_SDOUT	33 47 55 72
AUDIO_AC_SYNC	33 55
AUDIO_CDC_L_OUT	55 57
AUDIO_CDC_R_OUT	55 57
AUDIO_CD_GND	55 57
AUDIO_L_CD	55 57
AUDIO_L_LINE_IN	55 57
AUDIO_L_LINE_IN_CONN	57
AUDIO_L_LINE_OUT	57
AUDIO_MIC_IN	55 56
AUDIO_MONO_IN	55 57
AUDIO_MONO_OUT	55 57
AUDIO_MONO_OUT_SPKR	57
AUDIO_MONO_OUT_SPKR_R_CH	57
AUDIO_MONO_OUT_SPKR_R_IN	55 57
AUDIO_R_CD	55 57
AUDIO_R_LINE_IN	55 57
AUDIO_R_LINE_IN_CONN	57
AUDIO_R_LINE_OUT	57
AUD_JACK_GND	56 57
BF_CUT	46 54 67
CHA_A<13,,0>	17 22 24
CHA_BA<1,,0>	17 22 24
CHA_CAS_L	17 22 24
CHA_CB<7,,0>	21 22 23
CHA_CKE<0>	17 22 24
CHA_CKE<3,,0>	17 22 24
CHA_CKE<1>	17 22 24
CHA_CKE<2>	17 22 24
CHA_CKE<3>	17 22 24
CHA_CMDCLK0	17 22
CHA_CMDCLK0_L	17 22
CHA_CMDCLK1	17 22
CHA_CMDCLK1_L	17 22
CHA_CMDCLK4	17 22
CHA_CMDCLK4_L	17 22
CHA_CMDCLK5	17 22
CHA_CMDCLK5_L	17 22
CHA_CMDCLK6	17 22
CHA_CMDCLK6_L	17 22
CHA_CMDCLK7	17 22
CHA_CMDCLK7_L	17 22
CHA_CS_L<1,,0>	17 22 24
CHA_CS_L<3,,0>	17 22 24
CHA_CS_L<3,,2>	17 22 24
CHA_DQ<63,,0>	21 22 23
CHA_DQS<8,,0>	21 22 23
CHA_RAS_L	17 22 24
CHA_RCVENOUT_L	17 29
CHA_VREF	17 22 29
CHA_WE_L	17 22 24
CHB_A<13,,0>	17 26 28
CHB_BA<1,,0>	17 26 28
CHB_CAS_L	17 26 28
CHB_CB<7,,0>	25 26 27
CHB_CKE<0>	17 26 28
CHB_CKE<3,,0>	17 26 28
CHB_CKE<1>	17 26 28
CHB_CKE<2>	17 26 28
CHB_CKE<3>	17 26 28
CHB_CMDCLK0	17 26
CHB_CMDCLK0_L	17 26
CHB_CMDCLK1	17 26
CHB_CMDCLK1_L	17 26
CHB_CMDCLK4	17 26
CHB_CMDCLK4_L	17 26
CHB_CMDCLK5	17 26
CHB_CMDCLK5_L	17 26
CHB_CMDCLK6	17 26
CHB_CMDCLK6_L	17 26
CHB_CMDCLK7	17 26
CHB_CMDCLK7_L	17 26
CHB_CS_L<1,,0>	17 26 28
CHB_CS_L<3,,0>	17 26 28
CHB_CS_L<3,,2>	17 26 28
CHB_DQ<63,,0>	25 26 27
CHB_DQS<8,,0>	25 26 27
CHB_RAS_L	17 26 28
CHB_RCVENOUT_L	17 29
CHB_VREF	17 26 29
CHB_WE_L	17 26 28
CK408B_MULT0	20
CK408B_PWRDWN_L	20 72
CK408B_S2	20
CK408B_XTALIN	20
CK408B_XTALOUT	20
CLK_IREF	20
CLK_PCISTOP_L	20
CORE_SENSE	14 64
CPU0_BR0_L	10 12 15
CPU0_BSEL0	10 20 71
CPU0_BSEL1	10 71
CPU0_FSTR0_AD16	10
CPU0_FSTR0_E16	10
CPU0_PWM	45 70
CPU0_TACH	45 70
CPU0_THERMAL_DIODE_N_NEW	10 45
CPU0_THERMAL_DIODE_N_NEW_R	10 75
CPU0_THERMAL_DIODE_P_NEW	10 45
CPU0_THERMAL_DIODE_P_NEW_R	10 75
CPU1_BR0_L	10 12
CPU1_BSEL0	12 71
CPU1_BSEL1	12 71
CPU1_COMP0	12
CPU1_COMP1	12
CPU1_ODTEN	12
CPU1_PWM	45 70
CPU1_TACH	45 70
CPU1_THERMAL_DIODE_N_NEW	12 45
CPU1_THERMAL_DIODE_P_NEW	12 45
CPUP0_IERR_L	10 77
CPUP1_IERR_L	12 77
CPU_A20GATE	31 48
CPU_A20M_L	10 12 15 31 76
CPU_A20M_R_L	31 76
CPU_BPM_L_0	10 12 15
CPU_BPM_L_1	10 12 15
CPU_BPM_L_2	10 12 15
CPU_BPM_L_3	10 12 15
CPU_BPM_L_4	10 12 15
CPU_BPM_L_5	10 12 15
CPU_CPUSLP_L	10 12 15 31
CPU_FERR_L	10 12 15 31
CPU_IGNNE_L	10 12 15 31 76
CPU_IGNNE_R_L	31 76
CPU_INIT_L	10 12 15 31 47
CPU_LINT0_INTR	10 12 15 31 76
CPU_LINT0_INTR_R	31 76
CPU_LINT1_NMI	10 12 15 31 76
CPU_LINT1_NMI_R	31 76
CPU_PROCHOT_L	10 12 15 45
CPU_PWR_GD	10 12 15 32
CPU_S3A_PS_ON_L	46 63
CPU_SMB_ALERT_L	10 12 32
CPU_SMI_L	10 12 15 72
CPU_SM_WP	10 12 48 72
CPU_STPCLK_L	10 12 15 72
CPU_THERMTRIP_L	10 12 15 31 72
CPU_THERMTRIP_L_ITTO	72
CPU_THERMTRIP_L_R	31
CPU_VRD_PWR_GD_L	20 72
CPU_VRM_PWR_GD	20 32 64
CRESET	76
C_BE_L<0>	31 34 35
C_BE_L<3,,0>	31 34 35
C_BE_L<1>	31 34 35
C_BE_L<2>	31 34 35
C_BE_L<3>	31 34 35
DBR_RESET_L	15
DEB_FP_RESET_L	46
DEVSEL_L	31 34 35 36
DRCOMPVREF_H	17 29
DRCOMPVREF_V	17 29
FP_RESET_L	31 46 59 72 74
FP_RST_R_L	31
FRAME_L	31 34 35 36
FSB_ADSTB_L<1,,0>	10 12 16
FSB_ADS_L	10 12 16
FSB_AP_L<0>	10 12 16
FSB_AP_L<1,,0>	10 12 16
FSB_AP_L<1>	10 12 16
FSB_A_L<35,,3>	10 12 16
FSB_BINIT_L	10 12 15 16
FSB_BNR_L	10 12 15 16
FSB_BPRI_L	10 12 16
FSB_CPURST_L	10 12 15 16 73 76
FSB_DBI_L<3,,0>	10 12 16
FSB_DBSY_L	10 12 16
FSB_DEFER_L	10 12 16
FSB_DP_L<3,,0>	10 12 16
FSB_DRDY_L	10 12 16
FSB_DSTBN_L<3,,0>	10 12 16
FSB_DSTBP_L<3,,0>	10 12 16
FSB_D_L<63,,0>	10 12 16
FSB_FREQ_SEL	20 48 72
FSB_HITM_L	10 12 15 16
FSB_HIT_L	10 12 15 16
FSB_LOCK_L	10 12 16
FSB_MCERR_L	10 12 15 16
FSB_REQ_L<4,,0>	10 12 16
FSB_RSP_L	10 12 16
FSB_RS_L_0	10 12 16
FSB_RS_L_1	10 12 16
FSB_RS_L_2	10 12 16
FSB_TRDY_L	10 12 16
FWH_33MHZ_CLK	20 47
FWH_FGPI2	47
FWH_FGP_14	47 72
GLUE_HD_LED_ACT_L	46 59
GLUE_PWR_GD	46
GLUE_REF5V_STBY	32 46
GNT_L<0>	31 34
GNT_L<1,,0>	31 34 35
GNT_L<1>	31 35

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
NETS BY PAGE

REV:
1.5

INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:11 2002

PAGE:
81

```
GPIO_GRN_BLNK    32 46
GPIO_LAN_DISABLE_L 32 60
GPIO_YLW_BLNK    32 46
GRN_BLNK_LED     46 59
GTL_VREF1_P0     10 62
GTL_VREF1_P1     12 62
GTL_VREF2_P0     10 62
GTL_VREF2_P1     12 62
GTL_VREF_MCH     16 62
HIA_RCOMP_MCH    18
HIA_STBF         18 31 73
HIA_STBS         18 31 73
HIA_VREF_LAI     73
HIA_VREF_MCH     18 62
HIA_VSWING_MCH   18 62
HIB_RCOMP_MCH    18
HIB_STBF         18 38 73
HIB_STBS         18 38 73
HIB_USTBF        18 38 73
HIB_USTBS        18 38 73
HIB_VREF_LAI     73
HIB_VREF_MCH     18 62
HIB_VREF_P64H2   38 62
HIB_VSWING_MCH   18 62
HIB_VSWING_P64H2 38 62
HI_A<0>          18 31 73
HI_A<11,,0>      18 31 73
HI_A<1>          18 31 73
HI_A<2>          18 31 73
HI_A<3>          18 31 73
HI_A<4>          18 31 73
HI_A<5>          18 31 73
HI_A<6>          18 31 73
HI_A<7>          18 31 73
HI_A<8>          18 31 73
HI_A<9>          18 31 73
HI_A<10>         18 31 73
HI_B<0>          18 38 73
HI_B<21,,0>      18 38 73
HI_B<1>          18 38 73
HI_B<2>          18 38 73
HI_B<3>          18 38 73
HI_B<4>          18 38 73
HI_B<5>          18 38 73
HI_B<6>          18 38 73
HI_B<7>          18 38 73
HI_B<8>          18 38 73
HI_B<9>          18 38 73
HI_B<10>         18 38 73
HI_B<11>         18 38 73
HI_B<12>         18 38 73
HI_B<13>         18 38 73
HI_B<14>         18 38 73
HI_B<15>         18 38 73
HI_B<16>         18 38 73
HI_B<17>         18 38 73
HI_B<18>         18 38 73
HI_B<20>         18 38 73
HI_B<21>         18 38 73
HI_B_LAI_66MHZ_CLK 20 73
HI_LAI_66MHZ_CLK 20 73
HRCOMP0          16
HRCOMP1          16
HSWNG0           16
HSWNG1           16
ICH4_14MHZ_CLK   20 32 48
ICH4_33MHZ_CLK   20 31
ICH4_66MHZ_CLK   20 31
ICH4_CPU_SMI_L   31 72
ICH4_CPU_STPCLK_L 31 72
```

```
ICH4_GPIO6       32
ICH4_GPIO7       31 32
ICH4_GPIO8       32
ICH4_GPIO24      32
ICH4_GPIO36      32
ICH4_PWROK       15 32
ICH4_RI_Y1       32
ICH4_RSMRST_AA6  32
ICH4_SMBCLK      32 34 35 40 41 42 45 60
ICH4_SMBDATA     32 34 35 40 41 42 45 60
ICH4_USB_48MHZ_CLK 20 32
ICH_HI_REF       31 62
ICH_HI_VSWING    31 62
IDE_IRQ_14_L     33 37
IDE_IRQ_15_L     33 37
IDE_LED1_L       37 46
IDE_LED2_L       37 46
IDE_PDA0         33 37
IDE_PDA1         33 37
IDE_PDA2         33 37
IDE_PDCS1_L      33 37
IDE_PDCS3_L      33 37
IDE_PDD<15,,0>   33 37
IDE_PDDACK_L     33 37
IDE_PDDREQ       33 37
IDE_PDIOR_L      33 37
IDE_PDIOW_L      33 37
IDE_PIORDY       33 37
IDE_RSTDRV_L     37 46
IDE_SDA0         33 37
IDE_SDA1         33 37
IDE_SDA2         33 37
IDE_SDCS1_L      33 37
IDE_SDCS3_L      33 37
IDE_SDD<15,,0>   33 37
IDE_SDDACK_L     33 37
IDE_SDDREQ       33 37
IDE_SDIOR_L      33 37
IDE_SDIOW_L      33 37
IDE_SIORDY       33 37
IDROM_WE_L       48 72
INTRUDER_L       32 58
IRDY_L           31 34 35 36
ITP_BCLK0        15 20
ITP_BCLK1        15 20
ITP_TCK_P        10 12 15
ITP_TDI_P0       10 15
ITP_TDO_P0       10 12 15
ITP_TDO_P1       12 15
ITP_TMS_P        10 12 15
ITP_TRST_L       10 12 15
KENAI_CTRL_15    60 67
KENAI_CTRL_25    60 67
KENAI_LAN_CS     60
KENAI_LAN_SHCLK  60
LAN_ACT_L        60
LAN_CK_X1        60
LAN_CK_X2        60
LAN_EEPROM_DIN   60
LAN_EEPROM_DOUT  60
LAN_LINK100_L    60
LAN_LINK1000_L   60
LAN_LINK_L       60
LAN_MDIN_0       60 61
LAN_MDIN_1       60 61
LAN_MDIN_2       60 61
LAN_MDIN_3       60 61
LAN_MDIP_0       60 61
LAN_MDIP_1       60 61
LAN_MDIP_2       60 61
```

```
LAN_MDIP_3       60 61
LAN_V_1P5        61 67
LAN_V_2P5        60 61 67
LED_HI_OUT0      74
LED_HI_OUT1      74
LED_HI_OUT2      74
LED_HI_OUT3      74
LED_HI_OUT4      74
LED_HI_OUT5      74
LED_HI_OUT6      74
LED_LO_OUT0      74
LED_LO_OUT1      74
LED_LO_OUT2      74
LED_LO_OUT3      74
LED_LO_OUT4      74
LED_LO_OUT5      74
LED_LO_OUT6      74
L_AD<0>          33 47 48 73 74
L_AD<3,,0>       33 47 48 73 74
L_AD<1>          33 47 48 73 74
L_AD<2>          33 47 48 73 74
L_AD<3>          33 47 48 73 74
L_DRQ_L0         33 48
L_FRAME_L        33 47 48 73 74
MANUF_DET_L      47 72
MCH_66MHZ_CLK    18 20
MCH_BCLK0        16 20
MCH_BCLK1        16 20
MCH_CHA_CB<7,,0> 17 21
MCH_CHA_DQ<63,,0> 17 21
MCH_CHA_DQS<8,,0> 17 21
MCH_CHB_CB<7,,0> 17 25
MCH_CHB_DQ<63,,0> 17 25
MCH_CHB_DQS<8,,0> 17 25
MCH_SSI_ST       19 73
MCH_TDA_TESTPIN  18 45 72
MCH_TDC_TESTPIN  18 45 72
MCH_XORMODE_L    18
MEM0_FAN_TACH    45 70
P0_BCLK0         10 20
P0_BCLK1         10 20
P0_SLEW_CTRL     10 77
P0_TESTLOW       10 77
P0_VCCVID        10
P1_5V_ICH4       31 62 66 73
P1_BCLK0         12 20
P1_BCLK1         12 20
P1_FORCEPR_L     12 77
P1_SLEW_CTRL     12 77
P1_TESTLOW       12 77
P1_VCCVID        12
P12V_CPU         63 65 74
P64H2_66MHZ_CLK  20 38
P64H2_APIC0      38 43
P64H2_APIC1      38 43
P64H2_APICCLK    38 43
P64H2_BPCLK100   38 43
P64H2_BPCLK133   38 43
P64H2_CLK200N    38 43
P64H2_CLK200P    38 43
P64H2_PCIRST_L   38
P64H2_SMBUS_CLK  38
P64H2_SMBUS_DATA 38
P64H2_SMB_ADDR_1 39 43
P64H2_SMB_ADDR_2 39 43
P64H2_SMB_ADDR_3 39 43
P64H2_SMB_ADDR_5 39 43
P100_ACK64_L     39 41 42 44 60
P100_AD<63,,0>   39 41 42 44 60
P100_AD<17>      39 41 42 60
```

```
P100_AD<18>      39 41 42 60
P100_AD<19>      39 41 42 60
P100_AD<63,,32>  39 41 42 44 60
P100_C_BE_L<7,,0> 39 41 42 44 60
P100_C_BE_L<7,,4> 39 41 42 44 60
P100_DEVSEL_L    39 41 42 44 60
P100_FRAME_L     39 41 42 44 60
P100_GNT0_L      39 41
P100_GNT1_L      39 42
P100_GNT2_L      39 60
P100_IRDY_L      39 41 42 44 60
P100_IRQ_L<3,,0> 38 41 44
P100_IRQ_L<15,,0> 38 41 42 44 60
P100_IRQ_L<7,,4> 38 42 44
P100_IRQ_L<8>    38 44 60
P100_LAN_CLK     39 60
P100_LAN_CLK_R   39
P100_LOCK_L      39 41 42 44 60
P100_M66EN       39 41 42 44 60
P100_PAR         39 41 42 60
P100_PAR64       39 41 42 44 60
P100_PCICLKFB    39
P100_PCICLKFB_R  39
P100_PCIXCAP     39 41 42
P100_PERR_L      39 41 42 44 60
P100_REQ64_L     39 41 42 44 60
P100_REQ_L<0>    39 41 44
P100_REQ_L<5,,0> 39 41 42 44 60
P100_REQ_L<1>    39 42 44
P100_REQ_L<2>    39 44 60
P100_RESET_L     39 41 42 60
P100_SERR_L      39 41 42 44 60
P100_SLOT2_CLK   39 41
P100_SLOT2_CLK_R 39
P100_SLOT3_CLK   39 42
P100_SLOT3_CLK_R 39
P100_STOP_L      39 41 42 44 60
P100_TCK         41 42 44
P100_TDI         41 42 44
P100_TMS         41 42 44
P100_TRDY_L      39 41 42 44 60
P100_TRST_L      41 42 44
P133_ACK64_L     39 40 43
P133_AD<63,,0>   39 40 43
P133_AD<17>      39 40
P133_AD<63,,32>  39 40 43
P133_C_BE_L<7,,0> 39 40 43
P133_C_BE_L<7,,4> 39 40 43
P133_DEVSEL_L    39 40 43
P133_FRAME_L     39 40 43
P133_GNT0_L      39 40
P133_IRDY_L      39 40 43
P133_IRQ_L<3,,0> 38 40 43
P133_IRQ_L<15,,0> 38 40 43
P133_LOCK_L      39 40 43
P133_M66EN       39 40 43
P133_PAR         39 40
P133_PAR64       39 40 43
P133_PCICLKFB    39
P133_PCICLKFB_R  39
P133_PCIXCAP     39 40
P133_PERR_L      39 40 43
P133_REQ64_L     39 40 43
P133_REQ_L<0>    39 40 43
P133_REQ_L<5,,0> 39 40 43
P133_RESET_L     39 40
P133_SERR_L      39 40 43
P133_SLOT1_CLK   39 40
P133_SLOT1_CLK_R 39
P133_STOP_L      39 40 43
```

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
NETS BY PAGE

REV:
1.5

INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:11 2002

PAGE:
82

8	7	6	5	4	3	2	1

D C B A

```
P133_TCK          40 43
P133_TDI          40 43
P133_TMS          40 43
P133_TRDY_L       39 40 43
P133_TRST_L       40 43
PAR_L             31 34 35
PCI0_33MHZ_CLK    20 34
PCI1_33MHZ_CLK    20 35
PCIRST_L          16 30 31 34 35 38 46
PCIRST_OUT_COPY_L 46 73
PCIRST_OUT_L      46 47 48 73 74
PCI_FAN_TACH      45 70
PERR_L            31 34 35 36
PIRQ_A_L          30 33 36
PIRQ_B_L          30 33 36
PIRQ_C_L          33 36 38
PIRQ_D_L          33 36
PIRQ_E_L          33 34 35 36
PIRQ_F_L          33 34 35 36
PIRQ_G_L          33 34 35 36
PIRQ_H_L          33 34 35 36
PLD_66MHZ_CLK     20 73
PLOCK_L           31 34 35 36
PORT80_33MHZ_CLK 20 74
PROCHOT_3_3V_L    45 72
PS_ON_L           63
PS_PWR_GD         46 63 66 71
PWRGD_1_2V        66 68
PWRGD_1_25V       46 69
PWRGD_2_5V        68 69
PWR_GD_BUFF       32 46
PWR_GD_BUFF_EA    46
P_PME_L           30 31 34 35 36 40 41 42 60
RECOVERY_CONFIGURE 47 72
REQ64_L<1>        34 36
REQ64_L<2>        35 36
REQ_L<0>          31 34 36
REQ_L<5,,0>       31 34 35 36
REQ_L<1>          31 35 36
REQ_L<2>          31 36
REQ_L<3>          31 36
REQ_L<4>          31 36
REQ_L<5>          31 36
ROM_33MHZ_CLK     20 73
RSM_RST_L         32 46
RTCRST_L          32 58
RTC_XTAL_1        32 58
RTC_XTAL_2        32 58
SERIRQ            33 48
SERR_L            31 34 35 36
SIO_33MHZ_CLK     20 48
SIO_ACK_L         48 51
SIO_AUTOFD_L      48 51
SIO_BUSY          48 51
SIO_CTS1_L        48 50
SIO_DCD1_L        48 50
SIO_DSR1_L        48 50
SIO_DTR1_L        48 50
SIO_ERR_L         48 51
SIO_FD_DENSITY0 48 52
SIO_FD_DENSITY1 48 52
SIO_FD_DIR_L      48 52
SIO_FD_DSKCHG_L 48 52
SIO_FD_HEAD_L     48 52
SIO_FD_INDX_L     48 52
SIO_FD_MOTOR_L  48 52
SIO_FD_RDATA_L  48 52
SIO_FD_SELECT_L 48 52
SIO_FD_STEP_L   48 52
SIO_FD_TRACK0_L 48 52
```

```
SIO_FD_WDATA_L  48 52
SIO_FD_WE_L     48 52
SIO_FD_WPROTECT_L 48 52
SIO_GP24_SYSOPT 48
SIO_INIT_L        48 51
SIO_IRRX          48 59
SIO_IRTX          48 59
SIO_KBCLK         48 49
SIO_KBDATA        48 49
SIO_KBRST_L       31 48
SIO_MSECLK        48 49
SIO_MSEDATA       48 49
SIO_PD<7,,0>      48 51
SIO_PE            48 51
SIO_PME_L         32 48
SIO_RING_L        48 50
SIO_RTS1_L        48 50
SIO_SERIAL_RX     48 50
SIO_SERIAL_TX     48 50
SIO_SLCT          48 51
SIO_SLCTIN_L      48 51
SIO_SMI_L         32 48
SIO_STROBE_L      48 51
SKTOCC_0_L        10 46
SKTOCC_1          64 71
SKTOCC_1_L        12 71
SLP_S3_L          32 46
SLP_S4_L          32 46 63 67
SMBUS_CLK_ISO     10 12 20 22 26 32 38 72 75 76
SMBUS_CTRL        48
SMBUS_DATA_ISO    10 12 20 22 26 32 38 72 75 76
SPEAKER           32 55 59
STOP_L            31 34 35 36
STPCLK_INJ_HDR2_1 72
SUSCLK            32 48
SUSTAT_L          48
SWITCH_L          32 59 72 74
SYSTEM_FET_FANC 70
SYSTEM_PWM        45 70
SYS_PWR_GD_3_3V 15 18 20 32 38 46
TCLK              34 35 36
TDI               34 35 36
TMS               34 35 36
TOP_SWAP_OVERIDE 32
TRDY_L            31 34 35 36
TRST              34 35 36
USB_ICH4_OC_L<0> 33 53
USB_ICH4_OC_L<5,,0> 33 53 59
USB_ICH4_OC_L<1> 33 53
USB_ICH4_OC_L<2> 33 53
USB_ICH4_OC_L<3> 33 53
USB_ICH4_OC_L<4> 33 59
USB_ICH4_OC_L<5> 33 59
USB_ICH4_P0N      33 53
USB_ICH4_P0P      33 53
USB_ICH4_P1N      33 53
USB_ICH4_P1P      33 53
USB_ICH4_P2N      33 53
USB_ICH4_P2P      33 53
USB_ICH4_P3N      33 53
USB_ICH4_P3P      33 53
USB_ICH4_P4N      33 59
USB_ICH4_P4P      33 59
USB_ICH4_P5N      33 59
USB_ICH4_P5P      33 59
USB_WAKEON_PWR  49 53 54 59
VCC3_CLK          20
VCC3_CLKA         20
VCCAFSB           19
VCCAHI            19
```

```
VCCA_P0           10
VCCA_P1           12
VCCIOPLL_P0       10
VCCIOPLL_P1       12
VCC_CORE          10 11 12 13 14 15 16 18 19 31 32 45
                  62 65 72 77
VCC_SENSE_P0      10 72
VID_P0<4,,0>      10 45 71 72
VID_P0<3>         10 45 71 72
VID_P0<4>         10 45 71 72
VID_P1<4,,0>      12 71
VRM_INHIBIT_L     64 71 72
VRM_VID<4,,0>     64 71 72
VR_130A_BGATE1    64 65
VR_130A_BGATE2    64 65
VR_130A_BGATE3    64 65
VR_130A_BGATE4    64 65
VR_130A_DRN1      64 65
VR_130A_DRN1_R    64
VR_130A_DRN2      64 65
VR_130A_DRN2_R    64
VR_130A_DRN3      64 65
VR_130A_DRN3_R    64
VR_130A_DRN4      64 65
VR_130A_DRN4_R    64
VR_130A_DRN_IN    65
VR_130A_TGATE1    64 65
VR_130A_TGATE2    64 65
VR_130A_TGATE3    64 65
VR_130A_TGATE4    64 65
VSSA_P0           10
VSSA_P1           12
VSS_SENSE_P0      10 72
V_BAT             32 33 58
V_BIAS            32 58
V_BIAS_C          58
WAKEON_USB_STBYFET 54 67
YLW_BLNK_LED      46 59
```

8	7	6	5	4	3	2	1

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
NETS BY PAGE

REV: 1.5

INTEL FPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:12 2002

PAGE: 83

*** Part Cross-Reference for the entire design ***

C1A1	CAP-P	57
C1A2	CAP-P	55
C1A3	CAP	57
C1A4	CAP	55
C1A5	CAP	55
C1A6	CAP	57
C1A7	CAP	55
C1A8	CAP	55
C1A9	CAP	55
C1A10	CAP	55
C1A11	CAP	57
C1A12	CAP-P	40
C1A13	CAP	40
C1A14	CAP	40
C1A15	CAP-P	42
C1B1	CAP	40
C1B2	CAP	40
C1B3	CAP	40
C1B4	CAP-P	40
C1B5	CAP	40
C1B6	CAP	40
C1B7	CAP	40
C1B8	CAP	40
C1B9	CAP	40
C1C1	CAP	40
C1C2	CAP-P	40
C1C3	CAP	40
C1C4	CAP	40
C1D1	CAP	40
C1D2	CAP	40
C1D3	CAP	40
C1E1	CAP	40
C1F1	CAP	39
C1F2	CAP	38
C1F3	CAP	38
C1F4	CAP	38
C1F5	CAP	38
C1F6	CAP	38
C1F7	CAP	38
C1F8	CAP	38
C1F9	CAP	38
C1F10	CAP	38
C1F11	CAP	38
C1F12	CAP	38
C1F13	CAP	39
C1F14	CAP	39
C1F15	CAP	38
C1F16	CAP	38
C1F17	CAP	38
C1G1	CAP	38
C1G2	CAP	38
C1G3	CAP	38
C1G4	CAP	38
C1G5	CAP	38
C1G6	CAP	38
C1G7	CAP	38
C1G8	CAP	38
C1G9	CAP	38
C1G10	CAP	62
C1G11	CAP	62
C1G12	CAP	59
C1H1	CAP	76
C1J1	CAP	76
C1J2	CAP	76
C1J3	CAP	59
C1J4	CAP	72
C1J5	CAP	72
C1J6	CAP	72
C1J7	CAP	72
C1P1	CAP	14
C1P2	CAP	14
C1P3	CAP	14
C1R1	CAP	14
C1R2	CAP	14
C2A1	CAP	57
C2A2	CAP	57
C2A3	CAP-P	57
C2A4	CAP	55
C2A5	CAP	55
C2A6	CAP	55
C2A7	CAP	55
C2A8	CAP	55
C2A9	CAP	57
C2A10	CAP	55
C2A11	CAP	55
C2A12	CAP	55
C2A13	CAP	55
C2A14	CAP	56
C2A15	CAP	55
C2A16	CAP	55
C2A17	CAP	55
C2A18	CAP	55
C2A19	CAP	55
C2A20	CAP	55
C2A21	CAP	56
C2A22	CAP	56
C2A23	CAP	56
C2A24	CAP-P	55
C2A25	CAP	57
C2A26	CAP	57
C2A27	CAP	57
C2A28	CAP	55
C2A29	CAP	55
C2A30	CAP	56
C2A31	CAP-P	41
C2A32	CAP-P	41
C2A33	CAP	41
C2A34	CAP	42
C2A35	CAP	42
C2A36	CAP	41
C2B1	CAP	42
C2B2	CAP	42
C2B3	CAP	42
C2B4	CAP	41
C2B5	CAP	41
C2B6	CAP-P	41
C2B7	CAP	41
C2B8	CAP	42
C2B9	CAP	42
C2B10	CAP	42
C2B11	CAP	41
C2B12	CAP	41
C2B13	CAP	42
C2B14	CAP	41
C2B15	CAP	41
C2C1	CAP	42
C2C2	CAP	41
C2C3	CAP-P	42
C2C4	CAP	41
C2C5	CAP	42
C2C6	CAP	42
C2C7	CAP	41
C2D1	CAP-P	41
C2D2	CAP	42
C2D3	CAP	41
C2D4	CAP	42
C2D5	CAP	42
C2D6	CAP	41
C2D7	CAP	42
C2D8	CAP	41
C2D9	CAP	48
C2E1	CAP	41
C2E2	CAP	42
C2E3	CAP-P	38
C2E4	CAP	39
C2E5	CAP	39
C2E6	CAP	39
C2E7	CAP	67
C2F1	CAP	38
C2F2	CAP	38
C2F3	CAP	38
C2F4	CAP	38
C2F5	CAP	67
C2F6	CAP	38
C2F7	CAP	38
C2F8	CAP	38
C2F9	CAP	38
C2F10	CAP	63
C2F11	CAP	38
C2F12	CAP	38
C2F13	CAP	39
C2F14	CAP	39
C2F15	CAP	38
C2F16	CAP	38
C2F17	CAP	67
C2F18	CAP	38
C2G1	CAP	38
C2G2	CAP	38
C2G3	CAP	38
C2G4	CAP	38
C2G5	CAP	38
C2G6	CAP	38
C2G7	CAP	67
C2G8	CAP	58
C2G9	CAP	58
C2G10	CAP	58
C2G11	CAP	32
C2G12	CAP	63
C2G13	CAP	58
C2G14	CAP	58
C2H1	CAP	59
C2H2	CAP	74
C2H3	CAP	74
C2H4	CAP	74
C2H5	CAP	74
C2J1	CAP-P	59
C2J2	CAP-P	59
C2J3	CAP	45
C2J4	CAP	45
C2J5	CAP	45
C2J6	CAP-P	45
C2J7	CAP	45
C2J8	CAP	45
C2J9	CAP	59
C2J10	CAP	70
C2J11	CAP	59
C2P1	CAP	14
C2P2	CAP	14
C2P3	CAP	14
C2P4	CAP	14
C2P5	CAP	14
C2P6	CAP	14
C2P7	CAP	14
C2P8	CAP	14
C2R1	CAP	14
C2R2	CAP	14
C2R3	CAP	14
C2R4	CAP	14
C2R5	CAP	14
C3A1	CAP-P	57
C3A2	CAP	57
C3A3	CAP	57
C3A4	CAP	57
C3A5	CAP	56
C3A6	CAP	57
C3A7	CAP	55
C3A8	CAP-P	54
C3A9	CAP-P	34
C3A10	CAP	35
C3A11	CAP	35
C3A12	CAP	35
C3A13	CAP	35
C3B1	CAP-P	35
C3B2	CAP	35
C3B3	CAP	34
C3B4	CAP-P	35
C3B5	CAP	34
C3B6	CAP	41
C3B7	CAP	34
C3B8	CAP	35
C3B9	CAP	35
C3B10	CAP	35
C3B11	CAP	34
C3C1	CAP	34
C3C2	CAP	35
C3C3	CAP	35
C3C4	CAP-P	35
C3C5	CAP-P	42
C3D1	CAP	34
C3D2	CAP	35
C3D3	CAP	34
C3D4	CAP	35
C3D5	CAP-P	48
C3D6	CAP-P	66
C3D7	CAP	35
C3D8	CAP	48
C3D9	CAP	48
C3D10	CAP	48
C3E1	CAP	48
C3E2	CAP	47
C3E3	CAP	47
C3E4	CAP	47
C3E5	CAP	47
C3F1	CAP	46
C3F2	CAP-P	33
C3F3	CAP	31
C3F4	CAP	33
C3F5	CAP	32
C3F6	CAP	33
C3F7	CAP-P	31
C3F8	CAP	31
C3F9	CAP	33
C3G1	CAP	31
C3G2	CAP	32
C3G3	CAP	31
C3G4	CAP	33
C3G5	CAP	32
C3G6	CAP	31
C3G7	CAP	31
C3G8	CAP	31
C3G9	CAP	32
C3G10	CAP	31
C3G11	CAP-P	31
C3G12	CAP-P	66
C3G13	CAP	46
C3H1	CAP	46
C3H2	CAP	46
C3H3	CAP-P	66

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
REF'S BY PAGE

REV:
1.5

INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:12 2002

PAGE:
84

C3H4	CAP-P	66
C3H5	CAP	46
C3H6	CAP	46
C3H7	CAP	46
C3H8	CAP	72
C3M1	CAP	61
C3M2	CAP	61
C3T1	CAP	19
C3T2	CAP	19
C3T3	CAP	19
C3U1	CAP	19
C4A1	CAP	61
C4A2	CAP	61
C4A3	CAP	61
C4A4	CAP	61
C4A5	CAP	61
C4A6	CAP	61
C4A7	CAP	61
C4A8	CAP	61
C4A9	CAP	61
C4A10	CAP	61
C4A11	CAP	61
C4A12	CAP	61
C4A13	CAP	61
C4A14	CAP	61
C4A15	CAP	61
C4A16	CAP	61
C4A17	CAP	61
C4A18	CAP	61
C4A19	CAP	61
C4A20	CAP	61
C4A21	CAP	61
C4A22	CAP	61
C4A23	CAP	61
C4A24	CAP	61
C4A25	CAP	61
C4A26	CAP	61
C4A27	CAP	61
C4A28	CAP	61
C4B1	CAP	61
C4B2	CAP	61
C4B3	CAP	61
C4B4	CAP	61
C4B5	CAP	34
C4B6	CAP	34
C4B7	CAP-P	14
C4B8	CAP-P	30
C4B9	CAP	34
C4B10	CAP-P	34
C4B11	CAP-P	14
C4B12	CAP	34
C4B13	CAP	30
C4B14	CAP	30
C4C1	CAP	30
C4C2	CAP	30
C4C3	CAP-P	34
C4C4	CAP	30
C4C5	CAP	18
C4C6	CAP	18
C4C7	CAP	30
C4C8	CAP	30
C4C9	CAP-P	30
C4C10	CAP	30
C4C11	CAP	34
C4C12	CAP	30
C4D1	CAP	30
C4D2	CAP	30
C4D3	CAP-P	30
C4D4	CAP	30
C4D5	CAP	30
C4D6	CAP	34
C4D7	CAP	30
C4D8	CAP	30
C4D9	CAP	30
C4D10	CAP	30
C4D11	CAP-P	30
C4D12	CAP-P	14
C4D13	CAP	30
C4E1	CAP	30
C4E2	CAP	30
C4E3	CAP-P	30
C4E4	CAP	62
C4E5	CAP-P	66
C4E6	CAP	62
C4E7	CAP-P	66
C4E8	CAP	20
C4E9	CAP	20
C4E10	CAP	20
C4E11	CAP	20
C4E12	CAP	20
C4E13	CAP	20
C4F1	CAP	20
C4F2	CAP	20
C4F3	CAP	20
C4F4	CAP	20
C4F5	CAP	20
C4F6	CAP	20
C4F7	CAP	20
C4F8	CAP	20
C4F9	CAP	20
C4F10	CAP	20
C4F11	CAP	20
C4F12	CAP	20
C4F13	CAP	20
C4F14	CAP	20
C4F15	CAP	20
C4F16	CAP	20
C4F17	CAP	20
C4F18	CAP-P	20
C4F19	CAP	20
C4F20	CAP	20
C4F21	CAP	20
C4F22	CAP	20
C4F23	CAP-P	20
C4F24	CAP	20
C4F25	CAP	66
C4F26	CAP-P	66
C4F27	CAP	31
C4F28	CAP	31
C4F29	CAP	31
C4F30	CAP	66
C4F31	CAP	66
C4F32	CAP	31
C4G1	CAP	31
C4G2	CAP	66
C4G3	CAP	31
C4G4	CAP	31
C4G5	CAP	31
C4G6	CAP	66
C4G7	CAP	66
C4G8	CAP	62
C4G9	CAP	62
C4G10	CAP	66
C4G11	CAP	32
C4G12	CAP-P	31
C4G13	CAP-P	66
C4H1	CAP-P	66
C4H2	CAP-P	66
C4H3	CAP	66
C4J1	CAP	71
C4J2	CAP	70
C4P1	CAP	14
C4P2	CAP	14
C4P3	CAP	14
C4P4	CAP	14
C4P5	CAP	14
C4P6	CAP	14
C4P7	CAP	14
C4R1	CAP	14
C4R2	CAP	14
C4R3	CAP	14
C4R4	CAP	14
C4R5	CAP	14
C4T1	CAP	19
C4T2	CAP	19
C4U1	CAP	19
C4U2	CAP	19
C4U3	CAP	19
C4U4	CAP	19
C4U5	CAP	19
C4U6	CAP	19
C4U7	CAP	19
C4U8	CAP	19
C4U9	CAP	19
C4U10	CAP	19
C4U11	CAP	19
C4U12	CAP	19
C4U13	CAP	19
C4U14	CAP	19
C4U15	CAP	19
C4U16	CAP	19
C5A1	CAP	56
C5A2	CAP	56
C5A3	CAP	57
C5A4	CAP	61
C5A5	CAP	61
C5A6	CAP	60
C5A7	CAP	61
C5A8	CAP	61
C5A9	CAP	67
C5A10	CAP	67
C5A11	CAP	61
C5A12	CAP	61
C5A13	CAP	67
C5A14	CAP	60
C5A15	CAP	67
C5A16	CAP	67
C5A17	CAP	67
C5A18	CAP	60
C5A19	CAP	61
C5A20	CAP	61
C5A21	CAP	67
C5A22	CAP	67
C5B1	CAP	67
C5B2	CAP	67
C5B3	CAP	70
C5B4	CAP	60
C5B5	CAP	70
C5B6	CAP	15
C5B7	CAP	14
C5B8	CAP	14
C5C1	CAP-P	14
C5C2	CAP	14
C5C3	CAP	14
C5C4	CAP	14
C5C5	CAP-P	14
C5C6	CAP	14
C5C7	CAP	14
C5C8	CAP-P	14
C5C9	CAP	14
C5C10	CAP-P	14
C5C11	CAP	14
C5C12	CAP	14
C5D1	CAP	14
C5D2	CAP-P	14
C5D3	CAP	14
C5D4	CAP-P	14
C5D5	CAP	14
C5D6	CAP	12
C5D7	CAP	14
C5D8	CAP	14
C5D9	CAP-P	14
C5D10	CAP	14
C5D11	CAP	14
C5D12	CAP	14
C5D13	CAP-P	12
C5E1	CAP-P	12
C5E2	CAP	16
C5E3	CAP	16
C5E4	CAP	16
C5E5	CAP-P	19
C5E6	CAP	19
C5E7	CAP	18
C5E8	CAP	18
C5E9	CAP-P	19
C5E10	CAP	18
C5E11	CAP	19
C5E12	CAP	18
C5E13	CAP	18
C5E14	CAP	18
C5F1	CAP	18
C5F2	CAP	18
C5F3	CAP	18
C5F4	CAP	73
C5F5	CAP	18
C5F6	CAP	18
C5F7	CAP	18
C5F8	CAP	18
C5F9	CAP	18
C5F10	CAP	73
C5F11	CAP	18
C5F12	CAP	18
C5F13	CAP	20
C5F14	CAP	73
C5F15	CAP	18
C5F16	CAP	20
C5F17	CAP	19
C5F18	CAP	18
C5F19	CAP	62
C5F20	CAP	18
C5F21	CAP	19
C5F22	CAP-P	66
C5F23	CAP	62
C5F24	CAP	19
C5F25	CAP	19
C5F26	CAP	19
C5F27	CAP	62
C5F28	CAP	18
C5F29	CAP	19
C5F30	CAP	19
C5F31	CAP	19
C5F32	CAP	62
C5F33	CAP	18
C5F34	CAP	66
C5G1	CAP	66
C5G2	CAP-P	19
C5G3	CAP-P	29
C5H1	CAP-P	29
C5H2	CAP	24
C5H3	CAP	29

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
REF'S BY PAGE

REV:
1.5

INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:12 2002

PAGE:
85

C5H4	CAP-P	29
C5H5	CAP	29
C5H6	CAP	23
C5H7	CAP	23
C5H8	CAP	24
C5H9	CAP-P	29
C5H10	CAP	76
C5J1	CAP	29
C5J2	CAP	28
C5J3	CAP	28
C5J4	CAP	28
C5J5	CAP	28
C5J6	CAP	28
C5J7	CAP-P	69
C5J8	CAP-P	68
C5J9	CAP	70
C5J10	CAP-P	68
C5J11	CAP-P	68
C5M1	CAP	61
C5M2	CAP	61
C5P1	CAP	14
C5P2	CAP	14
C5P3	CAP	14
C5R1	CAP	14
C5R2	CAP	14
C5R3	CAP	14
C5T1	CAP	19
C5U1	CAP	19
C5U2	CAP	19
C6A1	CAP-P	53
C6A2	CAP	53
C6A3	CAP	53
C6A4	CAP	60
C6A5	CAP	60
C6A6	CAP-P	53
C6A7	CAP	60
C6A8	CAP	50
C6A9	CAP	60
C6A10	CAP	61
C6B1	CAP	15
C6B2	CAP	15
C6B3	CAP	15
C6B4	CAP	15
C6B5	CAP	14
C6B6	CAP	14
C6B7	CAP	14
C6B8	CAP	14
C6C1	CAP	12
C6C2	CAP	14
C6C3	CAP	14
C6C4	CAP	12
C6C5	CAP	62
C6C6	CAP	14
C6C7	CAP	14
C6C8	CAP	14
C6C9	CAP	14
C6D1	CAP	62
C6D2	CAP	12
C6D3	CAP	14
C6D4	CAP	14
C6D5	CAP	12
C6D6	CAP	14
C6D7	CAP	14
C6D8	CAP	14
C6D9	CAP	14
C6E1	CAP	16
C6E2	CAP	16
C6E3	CAP	62
C6E4	CAP	16
C6E5	CAP	16

C6E6	CAP	16
C6E7	CAP	16
C6E8	CAP	16
C6E9	CAP	16
C6F1	CAP	19
C6F2	CAP	19
C6F3	CAP	19
C6F4	CAP	19
C6G1	CAP-P	19
C6H1	CAP	24
C6H2	CAP	24
C6H3	CAP	24
C6H4	CAP	23
C6H5	CAP	23
C6H6	CAP	28
C6H7	CAP	23
C6H8	CAP	23
C6H9	CAP	24
C6H10	CAP	24
C6H11	CAP	24
C6H12	CAP	23
C6H13	CAP	23
C6H14	CAP	23
C6H15	CAP	23
C6J1	CAP	28
C6J2	CAP	28
C6J3	CAP	28
C6J4	CAP	27
C6J5	CAP	27
C6J6	CAP	27
C6J7	CAP	27
C6J8	CAP	27
C6J9	CAP	28
C6J10	CAP	28
C6J11	CAP	28
C6J12	CAP	28
C6J13	CAP	27
C6J14	CAP	27
C6J15	CAP	27
C6J16	CAP	68
C6J17	CAP	68
C6J18	CAP	68
C6J19	CAP-P	68
C6J20	CAP	68
C6J21	CAP	68
C6J22	CAP	68
C6J23	CAP	68
C6J24	CAP	68
C6J25	CAP	68
C6U1	CAP	73
C7A1	CAP	51
C7A2	CAP	51
C7A3	CAP	51
C7A4	CAP	51
C7A5	CAP	51
C7A6	CAP	51
C7A7	CAP	51
C7A8	CAP	51
C7A9	CAP	51
C7A10	CAP	51
C7A11	CAP	51
C7A12	CAP	51
C7A13	CAP	51
C7A14	CAP	50
C7B1	CAP-P	50
C7B2	CAP	50
C7B3	CAP-P	14
C7B4	CAP	14
C7B5	CAP	14
C7C1	CAP-P	14

C7C2	CAP	14
C7C3	CAP	14
C7C4	CAP	14
C7C5	CAP	14
C7C6	CAP	14
C7C7	CAP	14
C7C8	CAP-P	14
C7C9	CAP	14
C7C10	CAP	14
C7C11	CAP	14
C7C12	CAP	14
C7C13	CAP-P	14
C7C14	CAP	14
C7C15	CAP	14
C7C16	CAP-P	14
C7C17	CAP	14
C7C18	CAP	14
C7C19	CAP	14
C7C20	CAP	14
C7D1	CAP	14
C7D2	CAP	14
C7D3	CAP-P	14
C7D4	CAP	14
C7D5	CAP	14
C7D6	CAP-P	14
C7D7	CAP	14
C7D8	CAP	14
C7D9	CAP	14
C7D10	CAP	14
C7D11	CAP	14
C7D12	CAP	14
C7D13	CAP-P	14
C7D14	CAP	14
C7D15	CAP	14
C7D16	CAP-P	10
C7D17	CAP-P	10
C7D18	CAP	14
C7D19	CAP	14
C7E1	CAP-P	14
C7E2	CAP	16
C7E3	CAP	16
C7E4	CAP	16
C7E5	CAP	19
C7E6	CAP	65
C7F1	CAP	19
C7F2	CAP	65
C7F3	CAP	19
C7F4	CAP	17
C7F5	CAP	17
C7F6	CAP	64
C7F7	CAP	19
C7F8	CAP	64
C7F9	CAP	19
C7F10	CAP-P	65
C7F11	CAP	29
C7F12	CAP	29
C7F13	CAP	19
C7G1	CAP-P	19
C7H1	CAP	23
C7H2	CAP	23
C7H3	CAP	23
C7H4	CAP	23
C7H5	CAP	23
C7H6	CAP	24
C7H7	CAP	24
C7H8	CAP	23
C7H9	CAP	24
C7H10	CAP	24
C7H11	CAP	24
C7H12	CAP	23

C7H13	CAP	23
C7H14	CAP	23
C7H15	CAP	23
C7H16	CAP	23
C7J1	CAP	27
C7J2	CAP	27
C7J3	CAP	27
C7J4	CAP	27
C7J5	CAP	27
C7J6	CAP	27
C7J7	CAP	27
C7J8	CAP	27
C7J9	CAP	27
C7J10	CAP	27
C7J11	CAP	27
C7J12	CAP	27
C7J13	CAP	27
C7J14	CAP	27
C7J15	CAP	27
C7J16	CAP-P	68
C7J17	CAP-P	68
C7J18	CAP	68
C7J19	CAP	68
C7J20	CAP	68
C7U1	CAP	31
C7V1	CAP	31
C7V2	CAP	31
C7V3	CAP	31
C7V4	CAP	31
C7V5	CAP	31
C7V6	CAP	31
C7V7	CAP	31
C8A1	CAP	51
C8A2	CAP	51
C8A3	CAP	51
C8A4	CAP	51
C8A5	CAP	70
C8A6	CAP-P	53
C8A7	CAP	70
C8B1	CAP	63
C8B2	CAP	63
C8B3	CAP	63
C8B4	CAP	14
C8B5	CAP	14
C8B6	CAP	14
C8B7	CAP	14
C8B8	CAP	14
C8C1	CAP	10
C8C2	CAP	14
C8C3	CAP	14
C8C4	CAP	10
C8C5	CAP	62
C8C6	CAP	14
C8C7	CAP	14
C8C8	CAP	14
C8C9	CAP	14
C8D1	CAP	62
C8D2	CAP	10
C8D3	CAP	14
C8D4	CAP	14
C8D5	CAP	10
C8D6	CAP	14
C8D7	CAP	14
C8D8	CAP	14
C8D9	CAP	14
C8D10	CAP	14
C8E1	CAP	10
C8E2	CAP	65
C8E3	CAP	65
C8F1	CAP	65

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
REF'S BY PAGE

REV:
1.5

INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:13 2002

PAGE:
86

C8F2 CAP 65
C8F3 CAP 65
C8F4 CAP 65
C8F5 CAP 64
C8F6 CAP 64
C8F7 CAP 64
C8F8 CAP 64
C8F9 CAP 64
C8F10 CAP 64
C8F11 CAP 64
C8G1 CAP-P 65
C8G2 CAP-P 19
C8H1 CAP 23
C8H2 CAP 23
C8H3 CAP 23
C8H4 CAP 23
C8H5 CAP 23
C8H6 CAP 23
C8H7 CAP 23
C8H8 CAP 23
C8H9 CAP 23
C8H10 CAP 23
C8H11 CAP 23
C8H12 CAP 23
C8H13 CAP 23
C8H14 CAP 23
C8H15 CAP 23
C8J1 CAP 24
C8J2 CAP 28
C8J3 CAP 27
C8J4 CAP 27
C8J5 CAP 27
C8J6 CAP 27
C8J7 CAP 27
C8J8 CAP 27
C8J9 CAP 27
C8J10 CAP 27
C8J11 CAP 27
C8J12 CAP 27
C8J13 CAP 27
C8J14 CAP 27
C8J15 CAP 27
C8J16 CAP 68
C8J17 CAP 68
C8J18 CAP 69
C8J19 CAP 68
C8J20 CAP 67
C8J21 CAP 69
C8J22 CAP-P 68
C8J23 CAP 67
C8J24 CAP-P 69
C8U1 CAP 38
C8U2 CAP 38
C8U3 CAP 38
C8U4 CAP 38
C8U5 CAP 38
C8U6 CAP 38
C8V1 CAP 73
C9A1 CAP 53
C9A2 CAP 53
C9A3 CAP 49
C9A4 CAP-P 53
C9A5 CAP 63
C9A6 CAP 49
C9B1 CAP 63
C9B2 CAP-P 14
C9B3 CAP-P 63
C9B4 CAP-P 63
C9B5 CAP 14
C9B6 CAP-P 14

C9C1 CAP 14
C9C2 CAP 14
C9C3 CAP-P 14
C9C4 CAP 14
C9C5 CAP 14
C9C6 CAP-P 14
C9C7 CAP 14
C9C8 CAP-P 14
C9C9 CAP 14
C9C10 CAP 14
C9C11 CAP 14
C9D1 CAP-P 14
C9D2 CAP 14
C9D3 CAP 14
C9D4 CAP-P 14
C9D5 CAP 14
C9D6 CAP 14
C9D7 CAP-P 14
C9D8 CAP 14
C9D9 CAP 14
C9D10 CAP 75
C9D11 CAP 14
C9D12 CAP 75
C9E1 CAP-P 14
C9E2 CAP 65
C9E3 CAP 65
C9E4 CAP 65
C9F1 CAP 65
C9F2 CAP 64
C9F3 CAP 64
C9F4 CAP 64
C9F5 CAP 64
C9F6 CAP 64
C9F7 CAP 64
C9F8 CAP 64
C9G1 CAP 64
C9G2 CAP-P 65
C9G3 CAP-P 65
C9G4 CAP 22
C9G5 CAP 29
C9G6 CAP 29
C9G7 CAP-P 29
C9G8 CAP 26
C9H1 CAP-P 29
C9H2 CAP 23
C9H3 CAP 23
C9H4 CAP 29
C9H5 CAP 22
C9H6 CAP-P 29
C9H7 CAP 29
C9H8 CAP 23
C9H9 CAP 23
C9H10 CAP 23
C9H11 CAP 26
C9H12 CAP-P 29
C9H13 CAP 29
C9J1 CAP 69
C9J2 CAP 69
C9J3 CAP 27
C9J4 CAP 27
C9J5 CAP 27
C9J6 CAP 27
C9J7 CAP 27
C9J8 CAP 69
C9J9 CAP-P 69
C9J10 CAP 69
C9J11 CAP 69
C9J12 CAP 69
C9J13 CAP 69
C9J14 CAP 69

C9J15 CAP 69
C9J16 CAP 69
C9J17 CAP 69
C9U1 CAP 38
C9U2 CAP 38
CP1J1 CPAK4C4C 59
CP1J2 CPAK4C4C 59
CP3B1 CPAK4C4C 34 35
CP5A1 CPAK4C4C 57
CP7A1 CPAK4C4C 50
CP7A2 CPAK4C4C 50
CP9A1 CPAK4C4C 49
CR2G1 DIOSOT23C 58
CR2J1 ESD_SC 59
CR2J2 ESD_SC 59
CR2J3 ESD_SC 59
CR2J4 ESD_SC 59
CR3A1 SCHOTTKY 61
CR3J1 DIOSOT23S 32
CR3J2 DIOSOT23S 32
CR6A1 ESD_SC 53
CR6A2 ESD_SC 53
CR6A3 ESD_SC 53
CR6A4 ESD_SC 53
CR6J1 DIODE 68
CR8A1 ESD_SC 53
CR8A2 ESD_SC 53
CR8F1 DIODE 64
CR8F2 DIODE 64
CR8F3 DIODE 64
CR9A1 ESD_SC 53
CR9A2 ESD_SC 53
CR9F1 DIODE 64
CR9J1 DIODE 69
CR9J2 DIODE 69
CR9J3 DIODE 69
DS1F1 LED 74
DS1F2 LED 74
DS1F3 LED 74
DS1F4 LED 74
DS1F5 LED 74
DS1F6 LED 74
DS2H1 LED_DISPLAY_10P 74
DS2H2 LED_DISPLAY_10P 74
FB2A1 FERRITE 55
FB2J1 FERRITE 59
FB2J2 FERRITE 59
FB3F1 FERRITE 20
FB4F1 FERRITE 20
FB5A1 FERRITE 49
FB5A2 FERRITE 56
FB5A3 FERRITE 56
FB5A4 LPAK4L 57
FB6A1 FERRITE 53
FB6A2 FERRITE 53
FB7A1 LPAK4L 50
FB7A2 LPAK4L 50
FB7A3 FERRITE 51
FB7A4 LPAK4L 51
FB7A5 LPAK4L 51
FB7A6 LPAK4L 51
FB7A7 LPAK4L 51
FB8A1 FERRITE 49
FB9A1 FERRITE 49
FB9A2 FERRITE 49
FB9A3 LPAK4L 49
FB9A4 FERRITE 53
FB9A5 FERRITE 53
FB9A6 FERRITE 49
J1A1 1X2HDR 58

J1A2 1X4HDR 57
J1B1 PCI64X 40
J1G1 1X2HDR 32
J1H1 1X3HDR 32
J1H2 1X3HDR 32
J1H3 CONN_2PIN_MFRCONN 72
J1H4 1X3HDR 32
J1H5 1X3HDR 32
J1H6 1X2HDR 58
J1H7 1X3HDR 59
J1H8 2X8HDR10_14 59
J1J1 1X2HDR 76
J1J2 2X25HDR50 72
J2A1 1X4HDR 57
J2B1 PCI64X 42
J2B2 PCI64X 41
J2H1 1X4HDR 46
J2J1 1X3HDR 70
J2J2 1X3HDR 70
J2J3 2X5HDR2 59
J3A1 1X4HDR 57
J3A2 1X2HDR 57
J3A3 1X2HDR 60
J3B1 2X30HDR 73
J3B2 CONPCI 35
J3E1 1X3HDR 47
J3E2 1X3HDR 47
J3E3 SMA_JACK 20
J3J1 2X20HDR20 37
J3J2 2X17HDR5 52
J4B1 CONPCI 34
J4B2 AGP8X 30
J4D1 1X3HDR 47
J4E1 1X3HDR 20
J4G1 2X5HDR 66
J4G2 1X2HDR 72
J4G3 1X2HDR 72
J4G4 1X2HDR 72
J4J1 2X5HDR 71
J4J2 1X3HDR 70
J4J3 2X20HDR20 37
J5A1 AUDIO3STACK 56 57
J5B1 1X3HDR 70
J5B2 1X3HDR 70
J5B3 1X3HDR 70
J5F1 POCTOOL_CONN 73
J5G1 1X3HDR 18
J5G2 1X2HDR 72
J5J1 2X5HDR 71
J5J2 1X3HDR 70
J5J3 2X5HDR 68
J6B1 CONN26_2X13 15
J6U1 2X25HDR 73
J7A1 DSUB9 50
J7A2 DSUB25TALL 51
J7B1 CONN6 63
J7B2 1X3HDR 15
J7B3 1X2HDR 12
J8A1 1X3HDR 70
J8A2 1X3HDR 70
J8A3 1X3HDR 70
J8V1 2X40HDR 73
J9A1 PS2STACK 49
J9A2 CON2XUSB 53
J9B1 CONN24 63
J9B2 1X2HDR 10
J9E1 1X4HDR 75
J9F1 1X5HDR 63
J9F2 CONN8 63
J9G1 CONN184_DDR 22

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
REF'S BY PAGE

REV:
1.5

INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:13 2002

PAGE:
87

8	7	6	5	4	3	2	1

J9H1 CONN184_DDR 26
J9H2 CONN184_DDR 22
J9H3 CONN184_DDR 26
JA6A1 GBE_MAGJACK 53 60
L2J1 IND_4PIN 59
L2J2 IND_4PIN 59
L5D1 INDUCTOR 12
L5E1 INDUCTOR 12
L5E2 INDUCTOR 19
L5E3 INDUCTOR 19
L5G1 INDUCTOR 66
L5J1 INDUCTOR 68
L6A1 IND_4PIN 53
L6A2 IND_4PIN 53
L7D1 INDUCTOR 10
L7D2 INDUCTOR 10
L7E1 INDUCTOR 65
L7J1 INDUCTOR 68
L8A1 IND_4PIN 53
L8E1 INDUCTOR 65
L8E2 INDUCTOR 65
L8J1 INDUCTOR 69
L9A1 IND_4PIN 53
L9E1 INDUCTOR 65
L9G1 INDUCTOR 65
L9J1 INDUCTOR 69
LS1G1 SPKR 59
MH1A1 MTG_HOLE 74
MH1G1 MTG_HOLE 74
MH1J1 MTG_HOLE 74
MH3A1 MTG_HOLE 74
MH3F1 MTG_HOLE 74
MH5A1 MTG_HOLE 74
MH5E1 MTG_HOLE 74
MH5G1 MTG_HOLE 74
MH5J1 MTG_HOLE 74
MH9A1 MTG_HOLE 74
MH9E1 MTG_HOLE 74
MH9G1 MTG_HOLE 74
MH9J1 MTG_HOLE 74
Q1A1 78M05C 57
Q1G1 NPN 59
Q1H1 MBT3904DUAL 72
Q1H2 MBT3904DUAL 45
Q2E1 VREG 67
Q2G1 FET 63
Q2J1 HEXFET 70
Q3A1 MUN5215 54
Q3A2 HEXFET 54
Q3A3 MOSFET 54
Q3E1 FET 47
Q3E2 MBT3904DUAL 47
Q3G1 FET 32
Q3G2 FET 32
Q3H1 NPN 46
Q3J1 PNP 32
Q4B1 HEXFET 70
Q4C1 MBT3904DUAL 30
Q4D1 VREG 66
Q4E1 FET 62
Q4F1 NPN 20
Q4G1 MUN5215 66
Q4G2 NPN 72
Q4G3 NPN 72
Q4G4 PHB11N06LT 66
Q4H1 PHB11N06LT 66
Q4H2 MBT3904DUAL 76
Q4H3 MBT3904DUAL 76
Q4H4 MBT3904DUAL 76
Q4H5 MBT3904DUAL 76

Q4J1 MBT3904DUAL 71
Q5A1 PZT2907A 67
Q5B1 PZT2907A 67
Q5F1 NPN 76
Q5J1 NPN_W_R 71
Q6C1 PNP 45
Q8A1 HEXFET 70
Q8C1 PNP 45
Q8F1 MBT3904DUAL 64
Q8G1 FET 64
Q9G1 MBT3904DUAL 64
Q9G2 FET 64
Q9G3 FET 64
R1A1 RES 55
R1A2 RES 55
R1A3 RES 55
R1A4 RES 55
R1B1 RES 43
R1C1 RES 40
R1C2 RES 43
R1C3 RES 44
R1E1 RES 74
R1E2 RES 39
R1F1 RES 74
R1F2 RES 74
R1F3 RES 74
R1F4 RES 74
R1F5 RES 74
R1F6 RES 39
R1F7 RES 39
R1F8 RES 43
R1F9 RES 39
R1G1 RES 39
R1G2 RES 43
R1G3 RES 38
R1G4 RES 38
R1G5 RES 62
R1G6 RES 62
R1G7 RES 39
R1G8 RES 38
R1G9 RES 62
R1G10 RES 38
R1G11 RES 59
R1G12 RES 59
R1G13 RES 74
R1H1 RES 32
R1H2 RES 32
R1H3 RES 32
R1H4 RES 32
R1H5 RES 32
R1H6 RES 32
R1H7 RES 32
R1H8 RES 72
R1H9 RES 72
R1H10 RES 72
R1H11 RES 72
R1H12 RES 45
R1H13 RES 59
R1H14 RES 59
R1H15 RES 59
R1J1 RES 76
R1J2 RES 76
R2A1 RES 57
R2A2 RES 55
R2A3 RES 55
R2A4 RES 57
R2A5 RES 57
R2A6 RES 57
R2A7 RES 56
R2A8 RES 56

R2A9 RES 56
R2A10 RES 56
R2A11 RES 56
R2A12 RES 56
R2A13 RES 57
R2A14 RES 55
R2A15 RES 55
R2A16 RES 57
R2A17 RES 56
R2B1 RES 36
R2C1 RES 41
R2C2 RES 42
R2D1 RES 48
R2E1 RES 47
R2E2 RES 47
R2E3 RES 39
R2E4 RES 67
R2F1 RES 39
R2F2 RES 39
R2F3 RES 67
R2F4 RES 39
R2F5 RES 39
R2F6 RES 39
R2F7 RES 39
R2F8 RES 43
R2G1 RES 43
R2G2 RES 38
R2G3 RES 43
R2G4 RES 38
R2G5 RES 32
R2G6 RES 58
R2G7 RES 62
R2G8 RES 62
R2G9 RES 58
R2G10 RES 58
R2G11 RES 63
R2G12 RES 58
R2G13 RES 46
R2G14 RES 58
R2H1 RES 59
R2H2 RES 59
R2H3 RES 74
R2H4 RES 59
R2J1 RES 59
R2J2 RES 70
R2J3 RES 45
R2J4 RES 45
R2J5 RES 45
R2J6 RES 45
R2J7 RES 70
R3A1 RES 57
R3A2 RES 57
R3A3 RES 57
R3A4 RES 57
R3A5 RES 54
R3A6 RES 57
R3A7 RES 56
R3A8 RES 57
R3A9 RES 54
R3A10 RES 56
R3A11 RES 54
R3A12 RES 55
R3A13 RES 56
R3B1 RES 36
R3D1 RES 48
R3D2 RES 48
R3D3 RES 48
R3D4 RES 48
R3D5 RES 48
R3D6 RES 48

R3E1 RES 48
R3E2 RES 48
R3E3 RES 47
R3E4 RES 47
R3E5 RES 47
R3E6 RES 47
R3E7 RES 47
R3E8 POT 66
R3E9 RES 66
R3E10 RES 47
R3E11 RES 45
R3E12 RES 45
R3E13 RES 47
R3E14 RES 45
R3E15 RES 72
R3E16 RES 47
R3E17 RES 45
R3E18 RES 47
R3F1 RES 33
R3F2 RES 20
R3F3 RES 33
R3F4 RES 33
R3F5 RES 33
R3F6 RES 32
R3F7 RES 46
R3F8 RES 31
R3F9 RES 33
R3F10 RES 53
R3F11 RES 53
R3G1 RES 67
R3G2 RES 67
R3G3 RES 32
R3G4 RES 31
R3G5 RES 32
R3G6 RES 32
R3G7 RES 32
R3G8 RES 32
R3G9 RES 31
R3G10 RES 32
R3G11 RES 31
R3G12 RES 31
R3G13 RES 32
R3G14 RES 32
R3G15 RES 32
R3G16 RES 32
R3G17 RES 32
R3G18 RES 63
R3G19 POT 66
R3G20 RES 63
R3G21 RES 46
R3G22 RES 46
R3G23 RES 46
R3G24 RES 32
R3G25 RES 46
R3G26 RES 46
R3G27 RES 32
R3H1 RES 66
R3H2 RES 66
R3H3 RES 66
R3H4 RES 46
R3H5 RES 32
R3H6 RES 32
R3H7 RES 46
R3H8 RES 46
R3H9 RES 46
R3H10 RES 46
R3H11 RES 72
R3H12 RES 72
R3H13 RES 72
R3H14 RES 37

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
REF'S BY PAGE

REV:
1.5

INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:13 2002

PAGE:
88

8	7	6	5	4	3	2	1

R3H15	RES	46
R3H16	RES	37
R3H17	RES	46
R3H18	RES	37
R3H19	RES	46
R3H20	RES	37
R3H21	RES	46
R3J1	RES	32
R3J2	RES	32
R3J3	RES	52
R3J4	RES	37
R3J5	RES	37
R3J6	RES	37
R4A1	RES	60
R4A2	RES	61
R4A3	RES	61
R4A4	RES	61
R4A5	RES	61
R4A6	RES	61
R4A7	RES	61
R4A8	RES	61
R4A9	RES	60
R4A10	RES	60
R4A11	RES	61
R4A12	RES	60
R4A13	RES	60
R4A14	RES	60
R4A15	RES	61
R4A17	RES	61
R4A18	RES	60
R4A19	RES	60
R4A20	RES	60
R4A21	RES	60
R4A22	RES	60
R4A23	RES	60
R4B1	RES	70
R4B2	RES	36
R4B3	RES	60
R4B4	RES	30
R4C1	RES	30
R4C2	RES	30
R4C3	RES	30
R4D1	RES	30
R4D2	RES	47
R4D3	RES	47
R4E1	RES	66
R4E2	RES	62
R4E3	RES	62
R4E4	RES	62
R4E5	RES	62
R4E6	RES	66
R4E7	RES	62
R4E8	RES	62
R4E9	RES	62
R4E10	RES	66
R4E11	RES	66
R4E12	RES	45
R4E13	RES	45
R4E14	RES	45
R4E15	RES	45
R4E16	RES	20
R4E17	RES	20
R4E18	RES	20
R4E19	RES	20
R4E20	RES	20
R4E21	RES	20
R4E22	RES	20
R4F1	RES	20
R4F2	RES	20
R4F3	RES	32

R4F4	RES	20
R4F5	RES	20
R4F6	RES	20
R4F7	RES	20
R4F8	RES	32
R4F9	RES	20
R4F10	RES	20
R4F11	RES	20
R4F12	RES	20
R4F13	RES	20
R4F14	RES	20
R4F15	RES	20
R4F16	RES	20
R4F17	RES	20
R4F18	RES	20
R4F19	RES	20
R4F20	RES	33
R4F21	RES	32
R4F22	RES	33
R4F23	RES	20
R4F24	RES	20
R4F25	RES	20
R4F26	RES	20
R4F27	RES	66
R4F28	RES	33
R4F29	RES	66
R4F30	RES	66
R4F31	RES	66
R4G1	RES	66
R4G2	RES	66
R4G3	RES	66
R4G4	RES	31
R4G5	RES	66
R4G6	RES	62
R4G7	RES	66
R4G8	RES	62
R4G9	RES	62
R4G10	RES	62
R4G11	RES	62
R4G12	RES	66
R4G13	RES	66
R4G14	RES	66
R4G15	RES	66
R4G16	RES	66
R4G17	RES	72
R4G18	RES	72
R4G19	RES	31
R4G20	RES	31
R4G21	RES	72
R4G22	RES	72
R4G23	RES	72
R4G24	RES	31
R4G25	RES	72
R4G26	RES	72
R4G27	RES	72
R4H1	RES	66
R4H2	POT	66
R4H3	RES	66
R4H4	RES	66
R4H5	RES	66
R4H6	RES	76
R4H7	RES	76
R4H8	RES	37
R4H9	RES	76
R4H10	RES	76
R4H11	RES	76
R4H12	RES	76
R4H13	RES	37
R4H14	RES	37
R4H15	RES	37

R4H16	RES	12
R4J1	RES	71
R4J2	RES	71
R4J3	RES	71
R4J4	RES	71
R4J5	RES	71
R4J6	RES	71
R4J7	RES	71
R4J8	RES	37
R4J9	RES	70
R5A1	RES	57
R5A2	RES	67
R5A3	RES	67
R5A4	RES	67
R5A5	RES	67
R5B1	RES	67
R5B2	RES	70
R5B3	RES	15
R5B4	RES	12
R5B5	RES	12
R5B6	RES	12
R5B7	RES	12
R5B8	RES	12
R5C1	RES	12
R5C2	RES	12
R5C3	RES	12
R5C4	RES	77
R5C5	RES	77
R5C6	RES	12
R5C7	RES	77
R5C8	RES	12
R5D1	RES	12
R5D2	RES	12
R5D3	RES	12
R5D4	RES	12
R5D5	RES	12
R5D6	RES	12
R5E1	RES	12
R5E2	RES	12
R5E3	RES	12
R5E4	RES	18
R5E5	RES	18
R5E6	RES	19
R5E7	RES	19
R5E8	RES	20
R5E9	RES	20
R5E10	RES	73
R5E11	RES	18
R5E12	RES	20
R5E13	RES	20
R5F1	RES	73
R5F2	RES	18
R5F3	RES	20
R5F4	RES	20
R5F5	RES	20
R5F6	RES	20
R5F7	RES	18
R5F8	RES	20
R5F9	RES	20
R5F10	RES	20
R5F11	RES	20
R5F12	RES	73
R5F13	RES	18
R5F14	RES	18
R5F15	RES	20
R5F16	RES	20
R5F17	RES	20
R5F18	RES	20
R5F19	RES	18
R5F20	RES	18

R5F21	RES	20
R5F22	RES	62
R5F23	RES	18
R5F24	RES	62
R5F25	RES	62
R5F26	RES	62
R5F27	RES	76
R5F28	RES	62
R5F29	RES	62
R5F30	RES	62
R5F31	RES	66
R5F32	RES	62
R5F33	RES	62
R5F34	RES	62
R5F35	RES	18
R5G1	RES	66
R5G2	RES	21
R5G3	RES	72
R5G4	RES	72
R5G5	RES	72
R5G6	RES	25
R5H1	RES	76
R5H2	RES	28
R5J1	RES	71
R5J2	RES	71
R5J3	RES	71
R5J4	RES	71
R5U1	RES	73
R6A1	RES	67
R6A2	RES	15
R6A3	RES	15
R6A4	RES	15
R6B1	RES	15
R6B2	RES	15
R6B3	RES	15
R6B4	RES	15
R6B5	RES	15
R6B6	RES	15
R6B7	RES	15
R6B8	RES	15
R6B9	RES	15
R6B10	RES	15
R6B11	RES	15
R6B12	RES	15
R6B13	RES	15
R6B14	RES	77
R6C1	RES	62
R6C2	RES	62
R6D1	RES	62
R6D2	RES	62
R6E1	RES	16
R6E2	RES	62
R6E3	RES	16
R6E4	RES	62
R6E5	RES	62
R6E6	RES	16
R6E7	RES	16
R6E8	RES	16
R6E9	RES	16
R6E10	RES	16
R6H1	RES	24
R6J1	RES	68
R6J2	RES	68
R6J3	RES	68
R6J4	RES	68
R6J5	RES	68
R6J6	RES	68
R6J7	RES	68
R6J8	RES	68
R6J9	RES	68

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
REF'S BY PAGE

REV:
1.5

INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:13 2002

PAGE:
89

R6J10 RES 60
R6J11 RES 60
R6J12 RES 60
R6J13 RES 60
R6J14 RES 60
R6J15 RES 60
R6U1 RES 73
R6U2 RES 73
R7B1 RES 50
R7B2 RES 15
R7B3 RES 15
R7C1 RES 77
R7C2 RES 77
R7C3 RES 77
R7C4 RES 10
R7C5 RES 10
R7C6 RES 12
R7C7 RES 12
R7C8 RES 10
R7C9 RES 10
R7C10 RES 77
R7C11 RES 77
R7C12 RES 10
R7D1 RES 10
R7D2 RES 12
R7D3 RES 10
R7D4 RES 12
R7D5 RES 10
R7D6 RES 12
R7D7 RES 12
R7D8 RES 14
R7D9 RES 10
R7D10 RES 10
R7D11 RES 10
R7D12 RES 10
R7D13 RES 10
R7D14 RES 10
R7E1 RES 16
R7F1 RES 64
R7F2 RES 17
R7F3 RES 17
R7F4 RES 17
R7F5 RES 29
R7F6 RES 29
R7F7 RES 64
R7F8 RES 29
R7F9 RES 29
R7F10 RES 17
R7F11 RES 17
R7F12 RES 29
R7F13 RES 29
R7F14 RES 29
R7F15 RES 29
R7H1 RES 27
R7H2 RES 23
R7J1 RES 60
R7J2 RES 60
R8A1 RES 51
R8B1 RES 70
R8B2 RES 70
R8B3 RES 15
R8B4 RES 15
R8B5 RES 15
R8B6 RES 15
R8C1 RES 62
R8C2 RES 62
R8D1 RES 62
R8D2 RES 62
R8E1 RES 15
R8E2 RES 65

R8E3 RES 65
R8E4 RES 65
R8E5 RES 65
R8F1 RES 65
R8F2 RES 65
R8F3 RES 64
R8F4 RES 64
R8F5 RES 64
R8F6 RES 65
R8F7 RES 64
R8F8 RES 64
R8F9 RES 14
R8F10 RES 64
R8F11 RES 64
R8G1 RES 64
R8G2 RES 64
R8G3 RES 64
R8J1 RES 69
R8J2 RES 67
R8J3 RES 67
R8J4 RES 69
R8V1 RES 73
R8V2 RES 73
R8V3 RES 73
R8V4 RES 73
R8V5 RES 73
R8V6 RES 73
R8V7 RES 73
R8V8 RES 73
R8V9 RES 73
R8V10 RES 73
R8V11 RES 73
R8V12 RES 73
R8V13 RES 73
R8V14 RES 73
R8V15 RES 73
R8V16 RES 73
R8V17 RES 73
R8V18 RES 73
R8V19 RES 73
R8V20 RES 73
R8W1 RES 73
R8W2 RES 73
R8W3 RES 73
R8W4 RES 73
R8W5 RES 73
R8W6 RES 73
R8W7 RES 73
R8W8 RES 73
R9A1 RES 53
R9A2 RES 53
R9C1 RES 10
R9C2 RES 10
R9C3 RES 10
R9C4 RES 10
R9D1 RES 10
R9D2 RES 10
R9D3 RES 77
R9D4 RES 77
R9D5 RES 10
R9D6 RES 75
R9D7 RES 75
R9D8 RES 10
R9D9 RES 10
R9E1 RES 75
R9E2 RES 75
R9E3 RES 75
R9E4 RES 65
R9E5 RES 65
R9E6 RES 65

R9F1 RES 63
R9F2 RES 65
R9F3 RES 64
R9F4 RES 64
R9F5 RES 63
R9F6 RES 65
R9F7 RES 64
R9F8 RES 64
R9F9 RES 64
R9F10 RES 64
R9F11 RES 64
R9F12 RES 64
R9F13 RES 64
R9F14 RES 64
R9F15 RES 64
R9F16 RES 64
R9G1 RES 65
R9G2 RES 64
R9G3 RES 29
R9G4 RES 29
R9G5 RES 29
R9G6 RES 29
R9J1 RES 69
R9J2 POT 69
R9J3 RES 69
R9J4 RES 69
R9J5 RES 69
R9J6 RES 69
R9J7 RES 69
R9J8 RES 69
R9J9 RES 69
R9J10 RES 69
R9J11 RES 69
R9J12 RES 69
R9J13 RES 69
R9J14 RES 69
RP1B1 RPAK4C4R 44
RP1B2 RPAK4C4R 43
RP1B3 RPAK4C4R 43
RP1B4 RPAK4C4R 44
RP1C1 RPAK4C4R 43
RP1C2 RPAK4C4R 43
RP1D1 RPAK4C4R 43
RP1D2 RPAK4C4R 43
RP1D3 RPAK4C4R 43
RP1D4 RPAK4C4R 43
RP1D5 RPAK4C4R 43
RP1D6 RPAK4C4R 43
RP1D7 RPAK4C4R 43
RP1E1 RPAK4C4R 43
RP1E2 RPAK4C4R 43
RP1E3 RPAK4C4R 43
RP1F1 RPAK4C4R 43
RP1F2 RPAK4C4R 43
RP1G1 RPAK4C4R 38
RP1G2 RPAK4C4R 38
RP1G3 RPAK4C4R 38
RP1H1 RPAK4C4R 45 79
RP2A1 RPAK4C4R 57
RP2B1 RPAK4C4R 44
RP2B2 RPAK4C4R 44 79
RP2C1 RPAK4C4R 44
RP2C2 RPAK4C4R 44
RP2D1 RPAK4C4R 44 79
RP2D2 RPAK4C4R 44
RP2D3 RPAK4C4R 44
RP2D4 RPAK4C4R 44
RP2D5 RPAK4C4R 44
RP2D6 RPAK4C4R 44
RP2E1 RPAK4C4R 44

RP2E2 RPAK4C4R 44
RP2E3 RPAK4C4R 44
RP2E4 RPAK4C4R 44
RP2F1 RPAK4C4R 36
RP2F2 RPAK4C4R 36 79
RP2F3 RPAK4C4R 44
RP2G1 RPAK4C4R 43
RP2G2 RPAK4C4R 44
RP2G3 RPAK4C4R 44
RP2G4 RPAK4C4R 43
RP2G5 RPAK4C4R 43
RP2G6 RPAK4C4R 43
RP2H1 RPAK4C4R 74
RP2H2 RPAK4C4R 74
RP2H3 RPAK4C4R 74
RP2H4 RPAK4C4R 74 79
RP3A1 RPAK4C4R 57
RP3B1 RPAK4C4R 36
RP3B2 RPAK4C4R 36 79
RP3C1 RPAK4C4R 34 35 79
RP3C2 RPAK4C4R 36
RP3C3 RPAK4C4R 36
RP3D1 RPAK4C4R 36
RP3D2 RPAK4C4R 49
RP3D3 RPAK4C4R 31 48
RP3E1 RPAK4C4R 47 79
RP3G1 RPAK4C4R 32 79
RP3G2 RPAK4C4R 32 79
RP3H1 RPAK4C4R 46 79
RP3J1 RPAK4C4R 52
RP4B1 RPAK4C4R 36
RP4G1 RPAK4C4R 76
RP4G2 RPAK4C4R 31
RP4G3 RPAK4C4R 76
RP4G4 RPAK4C4R 31
RP4H1 RPAK4C4R 76
RP4H2 RPAK4C4R 76
RP4J1 RPAK4C4R 71
RP5G1 RPAK4C4R 21
RP5G2 RPAK4C4R 21
RP5G3 RPAK4C4R 25
RP5G4 RPAK4C4R 25
RP5H1 RPAK4C4R 23
RP5H2 RPAK4C4R 23
RP5J1 RPAK4C4R 27
RP5J2 RPAK4C4R 27
RP5J3 RPAK4C4R 71
RP5J4 RPAK4C4R 71
RP5J5 RPAK4C4R 71
RP6G1 RPAK4C4R 21
RP6G2 RPAK4C4R 21
RP6G3 RPAK4C4R 21
RP6G4 RPAK4C4R 21
RP6G5 RPAK4C4R 21
RP6G6 RPAK4C4R 25
RP6G7 RPAK4C4R 25
RP6G8 RPAK4C4R 25
RP6G9 RPAK4C4R 25
RP6G10 RPAK4C4R 25
RP6H1 RPAK4C4R 23
RP6H2 RPAK4C4R 24 28
RP6H3 RPAK4C4R 24
RP6H4 RPAK4C4R 23
RP6H5 RPAK4C4R 23
RP6H6 RPAK4C4R 23
RP6H7 RPAK4C4R 23
RP6J1 RPAK4C4R 27
RP6J2 RPAK4C4R 27
RP6J3 RPAK4C4R 27
RP6J4 RPAK4C4R 27

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
REF'S BY PAGE

REV:
1.5

INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:14 2002

PAGE:
90

RP6J5 RPAK4C4R 24 28
RP6J6 RPAK4C4R 28
RP6J7 RPAK4C4R 27
RP7A1 RPAK4C4R 51
RP7A2 RPAK4C4R 51
RP7A3 RPAK4C4R 51
RP7A4 RPAK4C4R 51
RP7G1 RPAK4C4R 21
RP7G2 RPAK4C4R 21
RP7G3 RPAK4C4R 21
RP7G4 RPAK4C4R 21
RP7G5 RPAK4C4R 21
RP7G6 RPAK4C4R 21
RP7G7 RPAK4C4R 25
RP7G8 RPAK4C4R 25
RP7G9 RPAK4C4R 25
RP7G10 RPAK4C4R 25
RP7G11 RPAK4C4R 25
RP7G12 RPAK4C4R 25
RP7H1 RPAK4C4R 23
RP7H2 RPAK4C4R 24 79
RP7H3 RPAK4C4R 23
RP7H4 RPAK4C4R 24
RP7H5 RPAK4C4R 23
RP7H6 RPAK4C4R 23
RP7H7 RPAK4C4R 23
RP7H8 RPAK4C4R 23
RP7J1 RPAK4C4R 27
RP7J2 RPAK4C4R 27
RP7J3 RPAK4C4R 28 79
RP7J4 RPAK4C4R 27
RP7J5 RPAK4C4R 27
RP7J6 RPAK4C4R 28
RP7J7 RPAK4C4R 27
RP7J8 RPAK4C4R 27
RP8A1 RPAK4C4R 51
RP8B1 RPAK4C4R 15
RP8B2 RPAK4C4R 15
RP8F1 RPAK4C4R 64 79
RP8G1 RPAK4C4R 21
RP8G2 RPAK4C4R 21
RP8G3 RPAK4C4R 21
RP8G4 RPAK4C4R 21
RP8G5 RPAK4C4R 21
RP8G6 RPAK4C4R 21
RP8G7 RPAK4C4R 25
RP8G8 RPAK4C4R 25
RP8G9 RPAK4C4R 25
RP8G10 RPAK4C4R 25
RP8G11 RPAK4C4R 25
RP8G12 RPAK4C4R 25
RP8H1 RPAK4C4R 23
RP8H2 RPAK4C4R 24
RP8H3 RPAK4C4R 24 28
RP8H4 RPAK4C4R 23
RP8H5 RPAK4C4R 28
RP8H6 RPAK4C4R 23
RP8H7 RPAK4C4R 23
RP8H8 RPAK4C4R 23
RP8J1 RPAK4C4R 24 28
RP8J2 RPAK4C4R 24 28 79
RP8J3 RPAK4C4R 27
RP8J4 RPAK4C4R 27
RP8J5 RPAK4C4R 27
RP8J6 RPAK4C4R 24 28
RP8J7 RPAK4C4R 27
RP9A1 RPAK4C4R 49
RP9E1 RPAK4C4R 75 79
RP9F1 RPAK4C4R 64
RP9F2 RPAK4C4R 64

RP9G1 RPAK4C4R 64 79
RP9G2 RPAK4C4R 21
RP9G3 RPAK4C4R 25
RP9H1 RPAK4C4R 23
RP9H2 RPAK4C4R 23
RP9J1 RPAK4C4R 27
RP9J2 RPAK4C4R 27
RP9J3 RPAK4C4R 27
RT2H1 THERMISTOR 59
RT2J1 THERMISTOR 59
RT6A1 THERMISTOR 53
RT6A2 THERMISTOR 53
RT8A1 THERMISTOR 53
RT9A1 THERMISTOR 53
RT9A2 THERMISTOR 49
SW2H1 SWSPSTPB_5M 74
SW2H2 SWSPSTPB_5M 74
TP1N1 TDR_PIN 74
TP1N2 TDR_PIN 74
TP1N3 TDR_PIN 74
TP1V1 TDR_PIN 74
TP1V2 TDR_PIN 74
TP1W1 TDR_PIN 74
TP1W2 TDR_PIN 74
TP9B1 TDR_PIN 74
TP9B2 TDR_PIN 74
TP9B3 TDR_PIN 74
TP9B4 TDR_PIN 74
TP9B5 TDR_PIN 74
TP9G1 TDR_PIN 74
TP9G2 TDR_PIN 74
TP9H1 TDR_PIN 74
TP9H2 TDR_PIN 74
U1J1 74F74 76
U2A1 LM4861 57
U2A2 LF353 56
U2A3 AD1885 55
U2F1 74F08 46 79
U2G1 P64H2 38 39
U2G2 LM317L 67
U2H1 74LVC08 15 79
U2H2 EPM7032AE 74
U2J1 HECETA6 45
U3D1 LPC47M102 48
U3E1 FWH_8M 47
U3F1 ICH4 31 32 33
U3H1 GLUECHIP4 46
U3H2 SC1538 66
U3H3 AT24C02 72
U4A1 KENAI64 60 61
U4B1 AT93C56 60
U4E1 CK_408 20
U4F1 HIP6004E 66
U4H1 PCA9559 76
U4J1 74HC682 71
U4J2 74HC03 71 79
U4J3 74LVC00 71 79
U5C1 SOCKET_604PN 12 13
U5E1 PLACER_MCH 16 17 18 19
U5F1 IRF7811 66
U5G1 IRF7811 66
U6J1 IRF7811 68
U6J2 HIP6004E 68
U6J3 IRF7811 68
U7A1 GD75232 50
U7E1 IRF7811 65
U7E2 IRF7811 65
U7F1 IRF7811 65
U7F2 SC1405 64
U7J1 IRF7811 68

U7J2 IRF7811 68
U7J3 IRF7811 68
U7J4 IRF7811 68
U8C1 SOCKET_604PN 10 11
U8E1 IRF7811 65
U8E2 IRF7811 65
U8E3 IRF7811 65
U8E4 IRF7811 65
U8E5 IRF7811 65
U8E6 IRF7811 65
U8E7 IRF7811 65
U8E8 IRF7811 65
U8F1 IRF7811 65
U8F2 IRF7811 65
U8F3 IRF7811 65
U8F4 IRF7811 65
U8F5 IRF7811 65
U8F6 IRF7811 65
U8F7 SC1405 64
U8F8 SC1405 64
U8J1 IRF7811 67
U8J2 IRF7811 67
U8J3 IRF7811 67
U8J4 SC1545 67
U8J5 IRF7811 69
U8J6 IRF7811 69
U9A1 TVS6_2V 49
U9D1 TEMP_MONITOR 75
U9E1 IRF7811 65
U9E2 IRF7811 65
U9E3 IRF7811 65
U9E4 IRF7811 65
U9E5 IRF7811 65
U9E6 IRF7811 65
U9F1 IRF7811 65
U9F2 IRF7811 65
U9F3 IRF7811 65
U9F4 IRF7811 65
U9F5 IRF7811 65
U9F6 SC1405 64
U9F7 HIP6311A 64
U9J1 SC1110 69
XBT2G1 BATT_HLDR_3PIN 58
Y1A1 CRYSTAL 55
Y1J1 OSC_PWR 76
Y2H1 XTAL4P 58
Y4E1 CRYSTAL 20
Y5A1 CRYSTAL 60

SCHEMATIC TITLE:
INTEL(R) XEON(TM) PROCESSOR E7505 CHIPSET CRB

PAGE TITLE:
REF'S BY PAGE

REV:
1.5

INTEL EPG PAE
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: DRAWING
Mon Sep 30 17:03:14 2002

PAGE:
91