Intel® 5 Series Chipset and Intel® 3400 Series Chipset

Specification Update

October 2010

Contents

§

Revision History

Revision	Description	Date
-001	• Initial Release	September 2009

-002	• Updated
	  — Identification Information Markings
	  — PCH Device and Revision Identification
	  — 6-Errata: Intel® 5 Series Chipset and Intel® 3400 Series Chipset Full-Speed USB Isochronous Packet Truncation
	• Added
	  — Errata: 7-Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Port Stall with Bulk and Control Traffic, 8-Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA SYNC Escape Erratum
		January 7, 2010

-003	• Added — Errata: 9 - Intel® P55, PM55, 3400, and 3420 Chipsets May Not Fully Initialize Intel® ME, 10 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB End of Frame When Retrying Packets Issue, 11 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Transaction Priority Issue, 12 - Intel® H55 Express Chipset and Intel® 3420 Chipset May Report Incorrect Number of USB Ports, 13 - Intel® HM55 Express Chipset May Report Incorrect Number of USB Ports	January 13, 2010
-004	• Added — Errata: 14 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset HPET Writing Timing Issue, 15 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Full-Speed Port Staggering	February 13, 2010

-005	• Added
	  — Errata: 16 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Device May Slow or Hang, 17- Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Low Speed Bulk/Control Transactions, 18- Intel® 5 Series Chipset and Intel® 3400 Series Chipset May Not Detect Unsolicited SATA COMIINITs, 19- Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Hot Unplug.
	
	  — Specification Clarification: 1. GP_RST_SEL[95:0] Description Updated
	
	• Updated:
	  — Intel®QS57 Chipset High Definition Audio Device ID Updated
		March 10, 2010

-006	Added • Documentation Changes: 1. Correct Figure 8-2 S5 to S0 Timing Diagram • Updated Errata 17 Removed Bulk Transtion	April 14, 2010
-007	Added • Documentation Changes: 2. Update Table 3-1 to include SPI_CS0#. 3. Add Tj Mobile Thermal Junction Operating Temperature limits in Table 8-1. 4. Add sections 5.27.2.9 through 5.27.2.15 to section 5.27 PCH DisPlay Interface. 5. Remove Unit Interval DMI from Table 8-14	May 12, 2010
-008	Edited • Corrected typographical error in Documentation Changes, item #4.	May 17, 2010

-009	• Added
	  — Errata: 20- Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Missing ACK
	• Updated:
	  — Errata: 11- Intel® 5 / 3400 Series Chipset Family USB Classic Device Removal Issue
	• Removed
	  — Specification Clarification: 1; Documentation Changes: 1~5 that went into the updated datasheet 003
		June 9, 2010

Revision	Description	Date
-010	• Added — Errata: 21 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset Serial ATA Revision 3.0 (SATA 6Gb/s) Device Detection , 22 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset PCI Express* Link Disable Bit. • Updated: — Specification Clarification: 1- Host WOL Behavior Clarification. — Documentation Changes: 1- Correct Table 5-58 PCH supported Audio formats over HDMI and DisplayPort*.	July 14, 2010
-011	• Updated: — Documentation Changes: 2 - Correct Table 8-8 DC Output Characteristics and Notes 1; 3 - Correct 21.1.2 HSFS-Hardware Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers) ; 4 - Correct 21.4.2 HSFS—Hardware Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)	August 11, 2010
-012	• Added — Errata: 23 - Pixel Corruption Over Integrated LVDS Interface of Intel® 5 Series Chipset. • Updated: — Specification Clarification: 2 - Display Port Clarification	September 8, 2010
-013	• Updated: — Errata: 21 - Pixel Corruption Over Integrated LVDS Interface of Intel® 5 Series Chipset	October 10, 2010

§ §

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel ® 5 Series Chipset and Intel ® 3400 Series Chipset Datasheet	322169

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

§

Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the PCH product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata (Sheet 1 of 2)

Erratum Number	Stepping		Status	ERRATA
	B2	B3		
1	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset High-Speed USB Test J/Test K Output Drive Level
2	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset High-Speed USB 2.0 Vhsoh
3	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset 1.5 Gb/s & 3.0 Gb/s SATA Signal Voltage Level
4	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Low Power Device Detection

Errata (Sheet 2 of 2)

Erratum Number	Stepping		Status	ERRATA
	B2	B3		
5	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset Intel® HD Audio Interface Intermittently Does Not Play Sound
6	X		Fixed	Intel® 5 Series Chipset and Intel® 3400 Series Chipset Full-Speed USB Isochronous Packet Truncation
7	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Port Stall with Bulk and Control Traffic
8	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA SYNC Escape Erratum.
9	X		Fixed	Intel® P55, PM55, 3400, and 3420 Chipsets May Not Fully Initialize Intel® Management Engine
10	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB End of Frame When Retrying Packets Issue
11	X	X	No Fix	Intel® 5 / 3400 Series Chipset Family USB Classic Device Removal Issue
12	X	X	No Fix	Intel® H55 Express Chipset and Intel® 3420 Chipset May Report Incorrect Number of USB Ports
13	X	X	No Fix	Intel® HM55 Express Chipset May Report Incorrect Number of USB Ports
14	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset HPET Writing Timing Issue
15	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Full-Speed Port Staggering
16	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Devices May Slow or Hang
17	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Low Speed Control Transactions
18	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset May Not Detect Unsolicited SATA COMINITs
19	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Hot Unplug
20	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Missing ACK
21	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset Serial ATA Revision 3.0 (SATA 6Gb/s) Device Detection
22	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset PCI Express* Link Disable Bit
23	X	X	No Fix	Pixel Corruption Over Integrated LVDS Interface of Intel® 5 Series Chipset

Specification Changes

Spec Change Number	Stepping		SPECIFICATION CHANGES
	B2	B3	
			There are no specification changes in this revision of the specification update

Specification Clarification

No.	Document Revision	SPECIFICATION CLARIFICATIONS
1	003	Host WOL Behavior Clarification
2	003	Display Port Clarification

Documentation Changes

No.	Document Revision	DOCUMENTATION CHANGES
1	003	Correct Table 5-58 PCH supported Audio formats over HDMI and DisplayPort*
2	003	Correct Table 8-8 DC Output Characteristics and Note 1
3	003	Correct 21.1.2 HSFS-Hardware Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers)
4	003	Correct 21.4.2 HSFS—Hardware Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)

§

Identification Information

Markings

PCH Stepping	S-Spec	Top Marking	Notes
B2	SLGWN	82PM55	Intel® PM55 Chipset
B2	SLGWV	82P55	Intel® P55 Chipset
B2	SLGWX	3400	Intel® 3400 Chipset
B2	SLGWW	3420	Intel® 3420 Chipset
B3	SLGZQ	82QM57	Intel® QM57 Chipset
B3	SLGZR	82HM57	Intel® H57 Chipset
B3	SLGZS	82HM55	Intel® HM55 Chipset
B3	SLGZW	82Q57	Intel® Q57 Chipset
B3	SLGZL	82H57	Intel® H57 Chipset
B3	SLGZX	82H55	Intel® H55 Chipset
B3	SLH25	3520	Intel® 3420 Chipset
B3	SLGZY	3450	Intel® 3450 Chipset
B3	SLGZV	82QS57	Intel® QS57 Chipset
B3	SLH23	82PM55	Intel® PM55 Chipset
B3	SLH24	82P55	Intel® P55 Chipset

PCH Device and Revision Identification

The Revision ID (RID) is traditionally an 8-bit register located at the offset 08h in the PCI header of every PCI device and function. The assigned value is based on the product's stepping.

Intel ® 5 Series Chipset and Intel ® 3400 Series Chipset Device and Revision ID Table (Sheet 1 of 2)

Device Function	Description	Dev ID[1]	B2 Rev ID	B3 Rev ID	Comments
D31:F0	LPC	3B02h	05h	06h	Intel® P55 Chipset
		3B03h	05h	06h	Intel® PM55 Chipset
		3B06h	n/a	06h	Intel® H55 Chipset
		3B07h	n/a	06h	Intel® QM57 Chipset
		3B08h	n/a	06h	Intel® H57 Chipset
		3B09h	n/a	06h	Intel® HM55 Chipset
		3B0Ah	n/a	06h	Intel® Q57 Chipset
		3B0Bh	n/a	06h	Intel® HM57 Chipset
		3B0Fh	n/a	06h	Intel® QS57 Chipset
		3B12h	05h	n/a	Intel® 3400 Chipset
		3B14h	05h	06h	Intel® 3420 Chipset
		3B16h	n/a	06h	Intel® 3450 Chipset
D31:F2	SATA	3B20h	05h	06h	Desktop: Non-AHCI and Non-RAID Mode (Ports 0, 1, 2, 3)
		3B21h	05h	06h	Desktop: Non-AHCI and Non-RAID Mode (Ports 0 and 1)
		3B22h	05h	06h	Desktop: AHCI (Ports 0-5)
		3B23h	05h	06h	Desktop: AHCI (Ports 0, 1, 4 and 5)
		3B25h	05h	06h	Desktop RAID: 0/1/5/10
		3B28h	05h	06h	Mobile: Non-AHCI and Non-RAID Mode (Ports 0, 1, 4 and 5)
		3B29h	05h	06h	Mobile: AHCI (Ports 0, 1, 4 and 5)
		3B2Ch	05h	06h	Mobile: RAID: 0/1/5/10
		3B2Eh	05h	06h	Mobile: Non-AHCI and Non-RAID Mode (Ports 0, 1, 2, 3)
		3B2Fh	05h	06h	Mobile: AHCI (Ports 0-5)

Intel® 5 Series Chipset and Intel® 3400 Series Chipset Device and Revision ID Table (Sheet 2 of 2)

Device Function	Description	Dev ID[1]	B2 Rev ID	B3 Rev ID	Comments
D31:F5	SATA	3B26h	05h	06h	Desktop: Non-AHCI and Non-RAID Mode (Ports 4 and 5)
		3B2Dh	05h	06h	Mobile: Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	3B30h	05h	06h	
D31:F6	Thermal	3B32h	05h	06h	
D30:F0	DMI to PCI Bridge	244Eh	A5h	A6h	Desktop
D30:F0	DMI to PCI Bridge	2448h	A5h	A6h	Mobile
D29:F0	USB EHCI #1	3B34h	05h	06h	
D26:F0	USB EHCI #2	3B3Ch	05h	06h	
D27:F0	Intel High Definition Audio	3B56h	05h	06h	
D27:F0	Intel® High Definition Audio	3B57h	05h	06h	Intel® QS57 Chipset Only
D28:F0	PCI Express* Port 1	3B42h	05h	06h	
D28:F1	PCI Express Port 2	3B44h	05h	06h	
D28:F2	PCI Express Port 3	3B46h	05h	06h	
D28:F3	PCI Express Port 4	3B48h	05h	06h	
D28:F4	PCI Express Port 5	3B4Ah	05h	06h	
D28:F5	PCI Express Port 6	3B4Ch	05h	06h	
D28:F6	PCI Express Port 7	3B4Eh	05h	06h	
D28:F7	PCI Express Port 8	3B50h	05h	06h	
D25:F0	LAN[3]	3B41h	05h	06h	
D22:F0	Intel MEI #1	3B64h	05h	06h	
D22:F1	Intel MEI #2	3B65h	05h	06h	
D22:F2	IDE-R	3B66h	05h	06h	
D22:F3	KT	3B67h	05h	06h	

NOTES:
1. The PCH contains two SATA controllers. The SATA Device ID is dependant upon which SATA mode is selected by BIOS and what RAID capabilities exist in the SKU.
2. The SATA RAID Controller Device ID may reflect a different value based on Bit 7 of D31:F2:Offset 9Ch.

3. LAN Device ID is loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the Device ID location, then 3B41h is used. Refer to the appropriate Intel GbE Physical Layer Transceiver (PHY) Datasheet for LAN Device IDs.
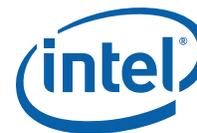
Errata

1.   Intel® 5 Series Chipset and Intel® 3400 Series Chipset High-Speed USB Test J/Test K Output Drive Level

Problem: Pre-emphasis is not disabled on high-speed USB ports during Test J/Test K.

Implication: J and K DC voltage levels may exceed USB 2.0 V_{HSOH}-MAX and V_{HSOL}-MAX during Test J/Test K testing and may not meet the USB 2.0 specification.

Workaround: Clear bit 1 of the USB Initialization Registers [0-13] prior to enabling Test J/Test K mode using a memory editing tool. This bit must be set back to 1 for each port after Test J/Test K testing is complete.

Port	Offset: RCBA + Offset:
0	3500h
1	3504h
2	3508h
3	350Ch
4	3510h
5	3514h
6	3518h
7	351Ch
8	3520h
9	3524h
10	3528h
11	352Ch
12	3530h
13	3534h

Status: No Fix. For steppings affected, see the Summary Table of Changes.

2.   Intel® 5 Series Chipset and Intel® 3400 Series Chipset High-Speed USB 2.0 V$_{hsoh}$

Problem: High-Speed USB 2.0 V_{hsoh} may not meet the USB 2.0 Specification.

               • The maximum expected V_{hsoh} is 495 mV.

Implication: Some motherboards may exceed specification limits during USB-IF compliance testing.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

3. Intel® 5 Series Chipset and Intel® 3400 Series Chipset 1.5 Gb/s & 3.0 Gb/s SATA Signal Voltage Level

Problem: The Intel® 5 Series Chipset and Intel® 3400 Series Chipset 1.5 Gb/s & 3.0 Gb/s SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA 1.5 Gb/s & 3.0 Gb/s (Gen1i, Gen1m, Gen2i, and Gen2m) transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications (section 7.2.1 of the Serial ATA Specification, rev 2.5).

Implication: None Known.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

4. Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Low Power Device Detection

Problem: Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Low Power Device Detection (SLPD) may not recognize, or may falsely detect, a SATA hot-plug event during a Partial or Slumber Link Power Management (LPM) state.

Implication: On Systems which enable LPM, when a SATA device attached to the Intel® 5 Series Chipset and Intel® 3400 Series Chipset is configured as External or hot-plug capable, one of the following symptoms may occur:

- Symptom #1: A hot-plug or External SATA device removal which is not detected results in the OS and Intel® Matrix Storage Manager/Intel® Rapid Storage Technology console falsely reporting the device present, or incorrectly identifying an eSATA device.

- Symptom#2: A false hot-plug removal detection may occur resulting in OS boot hang or ODD media playback hang

Workaround: A driver workaround is available.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

5. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Intel® HD Audio Interface Intermittently Does Not Play Sound

Problem: The Intel® 5 Series Chipset and Intel® 3400 Series Chipset Intel® HD Audio controller logic may not be gated by DMI L1 entry.

Implication: Systems may intermittently not play sound on the Intel HD Audio interface Following a DMI L1 exit.

Workaround: BIOS workaround available.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

6. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Full-Speed USB Isochronous Packet Truncation

Problem: Full-Speed isochronous-out transactions with multi-frame packets may be truncated, in the presence of Full or Low-Speed USB asynchronous transactions.

- For this to occur, two devices, one performing Full-Speed isochronous-out transactions and one performing asynchronous transactions must be connected to the same USB controller (Ports 0-7 and 8-13).

Implication: In the case of a USB audio device this issue may result in no audible impact or audible artifacts such as pops and clicks.

Note:

- High-Speed and Low-Speed USB devices are not impacted by this issue.
- Only devices supporting Full-Speed isochronous-out transactions that Intel is aware of are audio devices, such as sound adapters, speakers, and headphones.
- Intel has only observed the issue when a Full-Speed audio devices and Full-Speed USB web camera are connected to the same USB controller.

Workaround: None.

Status: Fixed For steppings affected, see the Summary Table of Changes.

7. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Port Stall with Bulk and Control Traffic

Problem: When a single USB bulk device is active on an EHCI controller, and the device has pending control and bulk traffic the PCH may not be able to resolve which traffic type is a priority and the associated with the device may stall.

- The processor must be in C0 for an extended period of time such as when Cx states are disabled, or if system traffic prevents the system from leaving C0.

Implication: The USB device may appear unresponsive. If Cx states are enabled the device may recover a short time later.

Note: Intel has only observed this failure on a limited number of devices. Failure only occurs if software associated with a USB device programs the Nak Count Reload bits defined in the EHCI Specification for USB Rev 1.0 to 0.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

8. Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA SYNC Escape Erratum

Problem: When SYNC Escape by a SATA device occurs on a D2H FIS, the PCH does not set the PxIS.IFS bit to '1.' This deviates from section 6.1.9 of the Rev 1.3 Serial ATA Advanced Host Controller Interface (AHCI).

Implication: There is no known observable impact. Instead of detecting the IFS bit, software will detect a timeout error caused by the SYNC escape and then respond.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

9. Intel® P55, PM55, 3400, and 3420 Chipsets May Not Fully Initialize Intel® ME

Problem: Some Intel P55, PM55, 3400, and 3420 based systems with Intel ME Ignition 6.0.0.1126 PV firmware may fail to correctly initialize the Intel ME subsystem during boot at colder temperatures.

Implication: Failures may occur during BIOS update. Systems fans may run continuously at full speed and the system may have increased power consumption.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: Fixed. For steppings affected, see the Summary Table of Changes.

10. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB End of Frame When Retrying Packets Issue

Problem: If the PCH encounters a Full-Speed or Low-Speed USB transaction with errors, the PCH may retry the transaction without considering if the transaction can finish before the end of the current frame.

Implication: The implication is dependant on the USB device. The PCH will attempt to recover per error handling specified in Section 4.5.2 of the USB Specification 2.0. The device may hang and require cycle to resume normal functionality.

Note: Intel has only observed this behavior on a limited number of USB devices. The implication only occurs if a USB device does not correctly respond to error handling as specified Section 4.5.2 of the USB Specification 2.0.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

11. Intel® 5 / 3400 Series Chipset Family USB Classic Device Removal Issue

Problem: If two or more USB Full-Speed / Low-Speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependant. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Workaround: None

Status: No Fix. For steppings affected, see the Summary Table of Changes.

12. Intel® H55 Express Chipset and Intel® 3420 Chipset May Report Incorrect Number of USB Ports

Problem: The Intel H55 Express Chipset and Intel 3420 Chipset support 6 ports on RMH #1 and may incorrectly report 8 USB ports in the bNbrPorts field of the RMH hub descriptor.

Implication: If AC power is removed while the system is in hibernate, when the system resumes new USB devices may not be detected, and all devices on RMH #1 may not function.

Note: AC power removal while a system is in S4 is not a common occurrence.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

13. Intel® HM55 Express Chipset May Report Incorrect Number of USB Ports

Problem: The Intel HM55 Express Chipset supports 6 ports on RMH #1 and will incorrectly report 8 USB ports in the bNbrPorts field of the RMH hub descriptor.

Implication: There are no known functional implications due to this issue on production Intel HM55 chipsets.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

14. Intel® 5 Series Chipset and Intel® 3400 Series Chipset HPET Writing Timing Issue

Problem: A read transaction that immediately follows a write transaction to the HPET TIMn_COMP Timer 0 (108h), HPET MAIN_CNT (0F0h), or TIMn_CONF.bit 6 (100h) may return an incorrect value.

Implication: There are no known functional implications with known software and operating systems.

- For the HPET TIMn_COMP Timer 0 Comparator Value Register and HPET MAIN_CNT - Main Counter Value Register the issue could result in the software receiving stale data. This may result in undetermined system behavior.

    Note: Timers [1:7] are not affected by this issue.

- For TIMERn_VAL_SET_CNF bit 6 in the TIMn_CONF-Timer n Configuration there is no known usage model for reading this bit and there are no known functional implications.

Workaround: A workaround is available.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

15. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Full-Speed Port Staggering

Problem: When USB full-speed/low-speed port staggering is enabled, the PCH may not wait for the bus to return to an idle state after an End of Packet (EOP) and may incorrectly acknowledge bus noise as a data packet.

Implication: Some full-speed/low-speed devices may fail to enumerate and function.

Note: This issue has been seen with a minimum number of devices on some motherboard ports with certain cable and trace lengths.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

16. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Devices May Slow or Hang

Problem: When the processor is in C0, and a single bulk High-Speed USB device is active the port associated with the active device may hang.

Implication: The implication is device driver dependant. Intel has observed some USB devices may have decreased performance, or the device may hang.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

17. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Low Speed Control Transactions

Problem: If the USB control buffers in the PCH Rate Matching Hub(s) are saturated with pending transactions the buffers may not be serviced in round robin order.

Implication: Some low-speed endpoints may not receive their pending control transactions.

Note: This issue has only been observed in synthetic test environment. The implication will be Device, driver and operating system specific.

Workaround: None

Status: No Fix. For steppings affected, see the Summary Table of Changes.

18. Intel® 5 Series Chipset and Intel® 3400 Series Chipset May Not Detect Unsolicited SATA COMINITs

Problem: Intel® 5 Series Chipset and Intel® 3400 Series Chipset may not detect an unsolicited COMINIT from a SATA device

Implication: The SATA device may not be properly detected and configured resulting in the device Not functioning as expected.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

19. Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Hot Unplug

Problem: Intel 5® Series Chipset and Intel® 3400 Series Chipset may not detect the unplug of a SATA 3.0 Gb/s device on a hot-plug enabled SATA port.

Implication: Unplugged SATA device may temporarily appear to be available.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

20. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Missing ACK

Problem: Following system power cycling or S3-S5 resume, if both HS and LS/FS devices are attached to the same controller, the host controller may not respond to a HS device ACK during a Get Descriptor request from the host SW to a USB HS port.

Implication: USB high-speed devices may not be detected after a power cycling or S3-S5 resume.

- Intel has only observed this failure on a limited number of platforms. On a failing platform, the issue occurs infrequently.
- Full-speed and low-speed USB devices are not impacted by this issue.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

21. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Serial ATA Revision 3.0 (SATA 6Gb/s) Device Detection

Problem: Intel 5® Series Chipset and Intel® 3400 Series Chipset may not be able to complete SATA Out Of Band (OOB) signaling with SATA 6Gb/s devices and down-shift to SATA 3Gb/s speed.

Implication: Intel 5® Series Chipset and Intel® 3400 Series Chipset may not detect a SATA 6Gb/s device upon power up or resume form S3, S4 or S5 State, resulting in indeterminate system behavior.

Workaround: None

Status: No Fix. For steppings affected, see the Summary Table of Changes.

22. Intel® 5 Series Chipset and Intel® 3400 Series Chipset PCI Express* Link Disable Bit

Problem: Intel 5® Series Chipset and Intel® 3400 Series Chipset PCI Express Ports may not exit the disable state when the Link Control Register "Link Disable" bit is set and PCIe Device Electrical Idle Exit is detected.

Implication: Port Specific Software Directed Hot Plug or Power Management support using the "Link Disable" bit may cause an Intel 5® Series Chipset and Intel® 3400 Series Chipset PCI Express Port to be stuck in the "Link Disable state" until a Host Reset with Power Cycling occurs.

Workaround: For Intel 5® Series Chipset and Intel® 3400 Series Chipset PCI Express Port Specific Software Directed Hot Plug or Power Management support, use PCI Power Management Control register D3$_{HOT}$ bits instead of Link Disable bit.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

23. Pixel Corruption Over Integrated LVDS Interface of Intel® 5 Series Chipset

Problem: Pixel corruption may be observed over integrated LVDS interface on Mobile Intel® 5 Series Platforms.

Implication: Display artifacts may be seen upon mode sets (resolution changes, screen rotation) and/or system boot on the platforms that use integrated LVDS.

Note: Visual artifacts observed in LVDS dual channel mode with panels supporting maximum native resolution of 1920 x1080 and higher.

Workaround: VBIOS and Intel® Graphics Media Accelerator driver change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

Specification Changes

There are no specification changes in this revision of the specification update.

Specification Clarification

1. Host WOL Behavior Clarification

The following note add to Section 5.3.4.1.1 and 5.3.4.1.2

5.3.4.1.1 Advanced Power Management Wake Up

Note: APM wake up settings will be restored to NVM default by the PCH when LAN connected Device (PHY) power is turned off and subsequently restored. Some example host WOL flows are:

When system transitions to G3 after WOL is disabled from the BIOS, APM host WOL would get enabled.

Anytime power to the LAN Connected Device (PHY) is cycled while in S4/S5 after WOL is disabled from the BIOS, APM host WOL would get enabled. Anytime power to the LAN Connected Device (PHY) is cycled while in S3, APM host WOL configuration is lost.

5.3.4.1.2 ACPI Power Management Wake Up

Note: ACPI wake up settings are not preserved when the LAN Connected Device (PHY) power is turned off and subsequently restored. Some example host WOL flows are:

Anytime power to the LAN Connected Device (PHY) is cycled while in S3 or S4, ACPI host WOL configuration is lost.

2. DisplayPort Clarification

The following note add to Section 5.27.2.8

5.27.2.8 Display Port

Note: DisplayPort includes support for Dual-Mode operation, refer to the Platform Design Guide for more details on Dual-mode implementation.

Documentation Changes

1. **Correct Table 5-58 PCH supported Audio formats over HDMI and DisplayPort***

The following changes applies to Table 5-58

Table 5-58 PCH supported Audio formats over HDMI and DisplayPort*

Audio Formats	HDMI	DisplayPort
AC-3 - Dolby Digital	Yes	No
Dolby* Digital Plus	Yes	No
DTS-HD*	Yes	No
LPCM, 192 KHz/24 bit, 8 Channel	Yes	Yes (two channel - upto 96 KHz 24 bit)
Dolby True HD, DTS HD Master Audio (Losses Blu-Ray Audio Format)	Yes	No

2. **Correct Table 8-8 DC Output Characteristics and NOTES 1.**

The following changes applies to Table 8-8

Symbol	Parameter	Min	Max	Unit	I_{OL} / I_{OH}	Notes
V_{OL3}	Output Low Voltage	0	0.4	V	4 mA	
V_{OH3}	Output High Voltage	3.3 V - 0.5	—	V	-2 mA	Note 1, 7

NOTES:

1. The SERR#, PIRQ[H:A], SMBDATA, SMBCLK, SML[1:0]CLK, SML[1:0]DATA, SML[1:0] ALERT# and PWM[3:0] signal has an open-drain driver and SATALED# has an open-collector driver, and the V_{OH} / I_{OH} specification does not apply. This signal must have external pull up resistor.

3. **Correct 21.1.2 HSFS-Hardware Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers)**

Bit	Description
13	**Flash Descriptor Override Pin Strap Status (FDOPSS)—** RO. This bit reflects the value the Flash Descriptor Override Pin-Strap. 0 = The Flash Descriptor Override strap is set 1 = No override

4. Correct 21.4.2 HSFS—Hardware Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)

Bit	Description
13	**Flash Descriptor Override Pin Strap Status (FDOPSS)—** RO. This bit reflects the value the Flash Descriptor Override Pin-Strap. 0 = The Flash Descriptor Override strap is set 1 = No override