Intel® 815EM Chipset Platform

Design Guide

October 2000

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Revision History

Rev.	Description	Date
-001	• Initial Release	October 2000

1. Introduction

This document provides design recommendations for mobile Intel® Pentium® This document provides design recommendations for Intel® mobile Pentium® III processor systems with 100-MHz SDRAM memory subsystems based on the Intel 815EM chipset. The design recommendations provided include simulation methodologies for post-layout validation of the design, debug recommendations, a system checklist, and board schematics. The schematics can be used as a reference for board designers. The core schematics will remain the same for most 815EM chipset platforms, while peripherals may change from one platform to another based on the market segments they are targeted for.

The recommendations ensure maximum flexibility for board designers while minimizing the risk of board related issues.

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2. System Overview

The Intel® 815EM chipset platform consists of the mobile Intel® Pentium® III processor, the mobile Graphics Memory Controller Hub 2 (GMCH2-M), the Video Controller Hub (VCH), and the mobile I/O Controller Hub 2 (82801BAM). The GMCH2-M provides the SDRAM memory interface support at 100 MHz. The *AGP Specification 2.0* with AGP4X is also supported by the GMCH2-M. The VCH component allows notebook PC internal TFT LCD displays (or TFT like interface panels) to support TV-out displays with an external TV encoder, and to support DVI monitor displays with an external DVI transmitter.

The memory controller hub connects to the I/O controller hub through the point-to-point Hub Interface that provides 266 MB/s maximum throughput. The mobile I/O controller Hub 2 (82801BAM) supports mobile power management, TCO management, AC'97 link, integrated Intel® SpeedStep™ Technology support, I/O APIC, USB, ATA66/100, SMBus Interface, PCI interface, LPC (Low-Pin Count) Interface, and Firmware Hub (FWH) Interface. The Firmware Hub Interface will support 4-MB BIOS, with a hardware Random Number Generator, Monotonic Counter, Protected Storage, and Protected Processing.

The AGP 4X and the Hub Interface provide a balanced system architecture for the mobile Intel® Pentium® III processor by minimizing bottlenecks and increasing system performance. Increasing graphics bandwidth through the use of AGP 4X, allows the Intel® 815EM chipset to deliver the necessary data throughput provided by the powerful mobile Intel® Pentium® III processor.

In addition, the Intel® 815EM chipset architecture enables a new security and manageability infrastructure through the Firmware Hub component.

The ACPI 1.0b-compliant Intel 815EM chipset platform can support Full-on, Autohalt, Quick Start, Deep Sleep, Power-On-Suspend, Suspend-To-RAM, Suspend-To-Disk, and Soft-off power management states. Through the use of an appropriate LAN device, the Intel 815EM chipset also supports *Wake-on-LAN*** and *Alert-on-LAN** for remote administration and troubleshooting.

2.1. Processor

The mobile Intel® Pentium® III processor will support a processor system bus (PSB) speed of 100 MHz as shown in Table 1. The processor will be able to obtain optimal performance while using Intel SpeedStep™ technology, which enables the processor to switch bus ratios and core speeds without being reset. The mobile Intel® Pentium® III processor includes on-die L2, integrated GTL+ termination, low-power state support, and thermal diode for measuring processor temperature.

2.2. Chipset Components

2.2.1. Mobile Graphics Memory Controller Hub 2 (82815EM)

The 82815EM contains the processor interface, DRAM controller, AGP interface, and arbiter logic. The I/O Controller Hub interfaces with the 82815EM through the proprietary Hub Interface.

The 82815EM supports a single ended GTL+ interface to the processor in a uni-processor system. Other support includes 32-bit host addressing, decoding up to 4 GB of the processor's memory address space, and a selectable 6-deep-in-order queue to support outstanding pipelined address requests on the host bus.

The DRAM controller supports 64-bit wide SO-DIMMS using 16-Mb, 64-Mb, 128-Mb, and 256-Mb technology. The DRAM controller also has six SCS# lines enabling the support of up to six 64-bit rows of DRAM. The six 64-bit rows of DRAM populate up to three, double-sided SO-DIMMs. The 82815EM supports up to 512 MB of memory. The speed configurations of the PSB and memory bus in Table 1 are also supported.

Table 1: Speed Configurations of PSB/SDRAM

PSB Frequency	SDRAM Frequency
100 MHz	100 MHz

The AGP graphics port supports a single AGP or PCI 66 device. The *AGP Specification Rev 2.0* is supported including up to 4X AGP transfers with 1.5-V signaling or 1X, 2X AGP transfers at 1.5V or 3.3V. The 82815EM supports a 66-MHz AGP bus with both PIPE# or SBA[7:0] AGP address mechanisms, as well as a 32 deep AGP request queue. The AGP graphics controller signals are multiplexed with the display cache signals. When internal graphics are used, these signals can be used to interface with an optional display cache.

The 82815EM interfaces to the 82801BAM via the 8-bit hub point-to-point interface. The bus runs at 66 MHz and the interface provides a 266 MB/s maximum throughput.

Additionally, the 82815EM provides arbitration for the processor, PCI, SDRAM, AGP, and Hub interfaces. The 82815EM also supports the mobile power management. It is *ACPI 1.0b* compliant, *APM Rev 1.2* compliant, and supports Quick Start (C2), Deep Sleep (C3), S1, S3, S4, and S5 transitions.

2.2.1.1. 82815EM Interface Summary

Table 2 provides the bus frequencies and operating voltages that the 82815EM supports.

Table 2: 82815EM Interface

Interface	Bus/Clk Frequency	Interface Voltage
CPU [GTL+]	100 MHz	1.5V
AGP	66 MHz	1.5V or 3.3V [1]
SDRAM	100 MHz	3.3V
Hub Interface	66 MHz	1.8V

NOTE: 4x AGP transfers only operate at 1.5V.

2.2.2. Video Controller Hub – (VCH)

The VCH receives display images in RGB pixel format from the 82815EM through the DVO port. The display images are converted to LCD panel interface formats via an LVDS interface or a CMOS interface when the LCD display is enabled and DVO bypassing is disabled.

The VCH is capable of passing the display image from the DVO port to an external TV encoder for TV displaying, or to an external DVI transmitter for DVI monitor displaying when DVO bypassing is enabled and the LCD display is disabled.

2.2.3. Mobile I/O Controller Hub 2 (82801BAM)

The I/O Controller Hub 2-Mobile (82801BAM) supports the PCI 2.2 interface at 33 MHz (which supports up to six master devices) and the Low-Pin Count (LPC) interface at 33 MHz for Super I/O, KBC, SMC, and other peripheral ASICs. The 82801BAM provides support for a total of four IDE devices with ATA66/100 support.

The 82801BAM includes the following:

- Two USB host controllers, supporting up to four USB ports, one of which can be used for Bluetooth* wireless technology
- An integrated D110 LAN MAC controller with a link to the LAN PHY through the Jordan interface
- An interrupt controller
- APIC
- A DMA controller
- AC’97 2.1 link
- GPIOs
- System TCO support
- An SMBus interface
- Mobile power management
- Intel® SpeedStep™ technology support.

The 82801BAM interfaces to FWH through a proprietary firmware Hub Interface.

2.2.3.1. 82801BAM Interface Summary

Table 3 summarizes the interfaces that the 82801BAM supports.

Table 3: 82801BAM Interfaces

Interface	Bus/Clk Frequency	Interface Voltage
Processor (sideband)	N/A	1.5V
Hub Interface	66 MHz	1.8V
PCI	33 MHz	3.3V
LPC	33 MHz	3.3V
FWH	33 MHz	3.3V
USB	48 MHz	3.3V
IDE	[ATA66]	3.3V
AC'97	12.288 MHz	3.3V
LAN-D110 MAC	Up to 50 MHz	3.3V I/O 1.8V Core
SMBus	N/A	3.3V
Interrupt	N/A	3.3V
RTC	N/A	3.3V
Resume Well	N/A	3.3V I/O 1.8V Core
GPIO	N/A	3.3V

2.2.3.2. Bandwidth Summary

Table 4: 82801BAM Bandwidth Summary

Interface	Clock Speed (MHz)	Samples Per Clock	Data Rate (Mega-samples/s)	Data Width (Bytes)	Bandwidth (MB/s)
Hub Interface	66	4	266	1	266
PCI 2.2	33	1	33	4	133

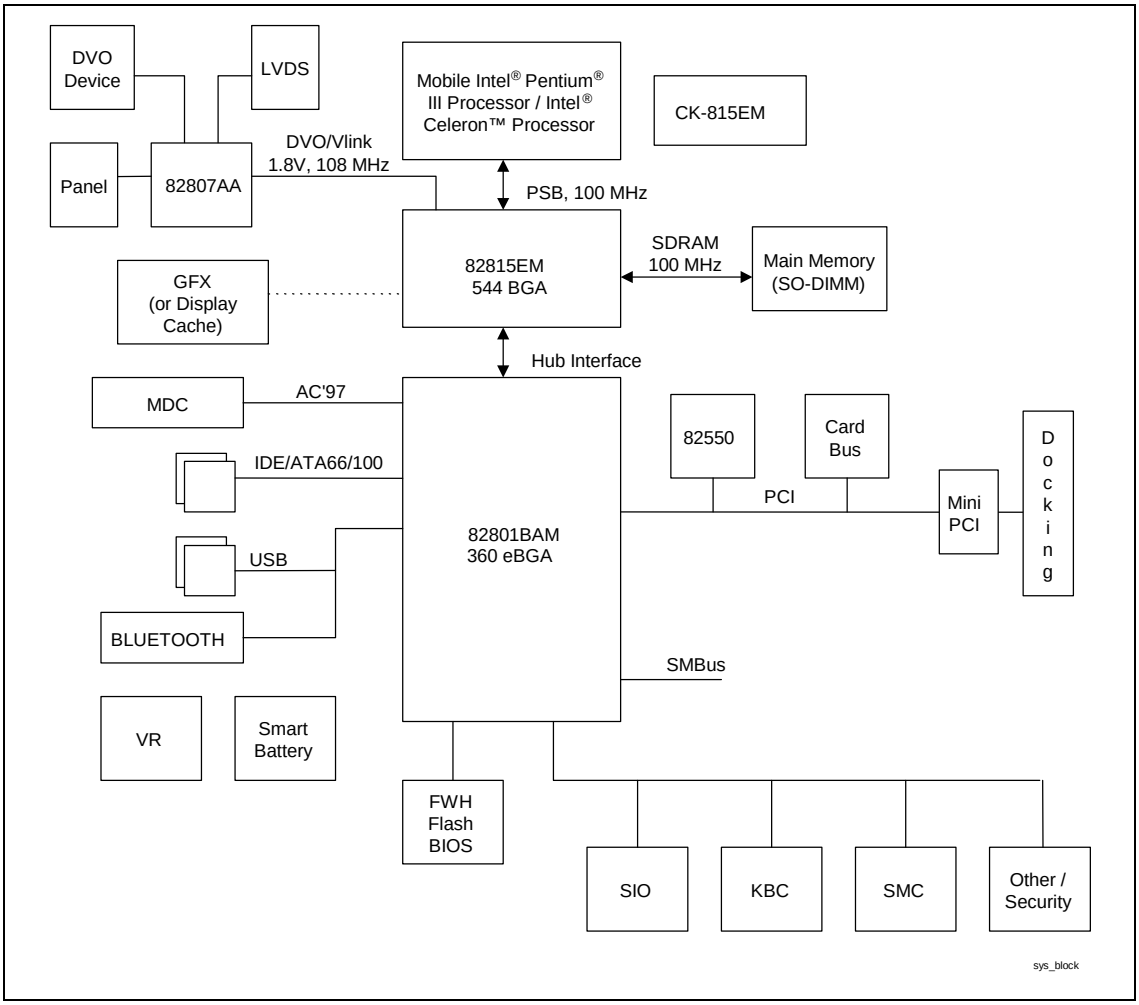
2.2.4. Firmware Hub (FWH)

The FWH component is an important element for enabling a new security and manageability infrastructure for the PC platform. The device operates under the FWH interface and protocol. The hardware features of this device include a unique Random Number Generator (RNG), register-based locking, and hardware-based locking.

2.3. System Configurations

Figure 1 shows a possible system configuration.

Figure 1: System Configuration



2.4. New Platform Initiatives

2.4.1. Hub Interface

The Intel proprietary Hub Interface connects the 82815EM to 82801BAM, providing 266 MB/S bandwidth with a 66-MHz clock. The Hub Interface is a narrow, low pin, low latency, and low power interface used to connect the memory and I/O control subsystems. Placing the I/O bridge on the Hub Interface instead of on the PCI bus ensures that adequate bandwidth is provided for I/O transactions as well as for PCI transactions.

2.4.2. Low-Pin Count (LPC) Interface

The Low Pin Count Interface replaces the X-bus/ISA bus for legacy I/O components, such as the SIO and keyboard controller. The LPC Interface reduces pin count for easier, more cost-effective and space-efficient designs. Unlike ISA, which runs at 8 MHz, the LPC interface will use the PCI 33-MHz clock. The LPC interface is software transparent for I/O functions and is compatible with existing peripheral devices and applications.

2.4.3. AC ’97

The *Audio Codec ’97* (AC’97) *Specification* defines a digital link that can be used to attach an audio codec (AC), a modem codec (MC), an audio/modem codec (AMC), or both an AC and an MC. The *AC’97 Specification* defines the interface between the system logic and the audio or modem codec known as the *AC’97 Digital Link*.

Adding cost-effective audio and modem solutions as the platform migrates away from ISA is important. In addition, the AC’97 audio and modem components are software configurable, which reduces configuration errors. The Intel® 815EM chipset’s AC’97 (with the appropriate codecs) not only replace ISA audio and modem functionality, but also improve overall platform integration by incorporating the AC’97 digital link. Using the Intel® 815EM chipset’s integrated AC’97 digital link also reduces cost and eases migration from ISA.

By using an audio codec, the AC’97 digital link allows for cost-effective, high-quality, integrated audio on the Intel® 815EM chipset platform. In addition, an AC’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC’97. The Intel® 815EM chipset’s integrated digital link allows two external codecs to be connected to the 82801BAM. The system designer can provide audio with an audio codec or a modem with a modem codec. For systems requiring both audio and a modem, there are two solutions. The audio codec and the modem codec can be integrated into an AMC, or separate audio and modem codecs can be connected to the ICH-M.

Modem implementation for different countries must be considered as telephone systems may vary. By using a split design, the audio codec can be on-board and the modem codec can be placed on a riser. Intel is developing an AC’97 digital link connector. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

The digital link in the 82801BAM is AC’97 Rev. 2.1 compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake-On-Ring from suspend is also supported with an appropriate modem codec.

Manageability

The Intel® 815EM chipset platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external micro-controller.

TCO Timer

The 82801BAM integrates a programmable TCO Timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI#, which the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

CPU Present Indicator

The 82801BAM looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the 82801BAM will reboot the system at the Safe Mode frequency multiplier.

ECC Error Reporting

Upon detecting an ECC error, the 82815EM has the ability to send one of several messages to the 82801BAM. The 82815EM can tell the 82801BAM to generate either an SMI#, NMI#, SERR#, or TCO interrupt.

Function Disable

The 82801BAM provides the ability to independently disable any or all of the following functions: AC'97 Modem, AC'97 Audio, IDE, USB, or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.

SMBus

The 82801BAM integrates an SMBus controller. The SMBus provides an interface to manage peripherals, such as serial presence detection (SPD) on SO-DIMMs, thermal sensors and clock generators.

Alert-On-LAN 2 (AOL2)

The 82801BAM supports Alert-On-LAN 2 (AOL2) by using Intel's 82550 PCI Ethernet controller. In AOL1, in response to a TCO event (intruder detect, thermal event, processor not booting) the 82801BAM will send a message over the SMBus. A LAN controller can decode this SMBus message and send a message over the network to alert the network manager. In AOL2, in addition to the AOL1, the central management servers can send the commands or messages to manage or correct the console (clients) in response to the alerting message sent by the clients.

2.5. General Recommendations

2.5.1. Layout and Routing Guidelines

The impedance tolerance is specified to be ± 10%, and the nominal impedance value is specified to 55Ω for all interfaces including the SDRAM interface, 100-MHz PSB, Hub Interface, and 2x/4x AGP interface. This is the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace that is based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

Note: All recommendations given in these guidelines are developed on pre-layout simulations. Designers are expected to review and fully analyze their requirements and to run simulations after their board design is complete to validate their design.

2.5.2. Simulations

The current systems have very high-performance busses and most have the source synchronous strobing data transfer mechanism. A source synchronous strobed interface uses strobe signals (instead of clock) to indicate that the data is valid, for example AGP 4x and Hub Interfaces. Refer to

Figure 2 for an example of strobing. As busses get faster and cycle times get shorter, the propagation delay becomes a limiting factor in bus speed. Source synchronous strobing is used to minimize the impact of propagation delay on maximum bus frequency. The primary benefit of the source synchronous strobing is that the data and the strobe arrive at the receiver simultaneously. Thus, a strobe and its associated data signals have very strict trace length mismatch requirements. With well-matched trace lengths (even under loaded conditions) as well as matched impedance, the propagation delay for the strobe and the propagation delay for the data will be very similar.

In addition to matched lengths, for a source strobed interface it is very important that the strobed signals are routed carefully. The signals must be very clean (free of noise). Data signals are latched on the rising or falling edge of the strobe signal (or both). If there is noise on these signals, it could cause an extra “edge” to be detected, thus latching incorrect data as shown in Figure 3 and Figure 4.

Manufacturing tolerance is very important in high-speed bus analysis. Additionally, electrical events that are not obvious at lower frequencies start affecting the performance of the design. For example, even and odd mode propagation velocity change creates skew between the clock and data, or the Inter-Symbol Interface phenomenon can impact timing of a signal.

High-performance bus designs must be analyzed for all these issues and validated after the layout is completed to ensure that the design still meets the system requirements.

Figure 2: Data Strobing Example

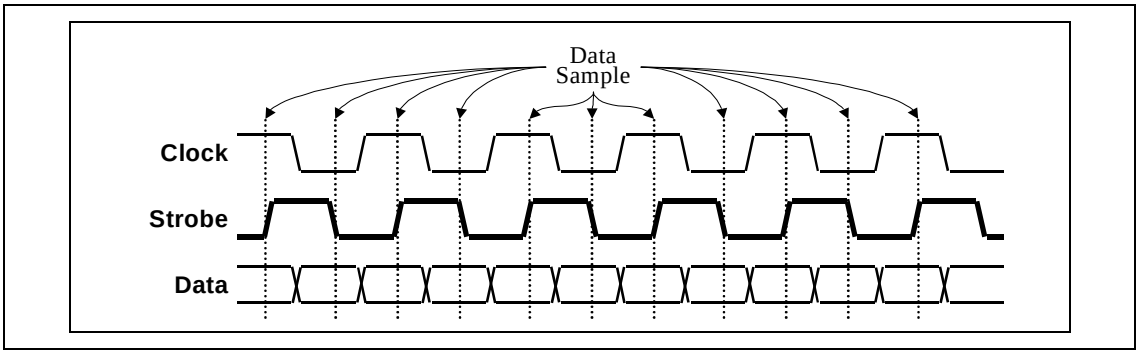


Figure 3: Correct Strobing Example (No Noise)

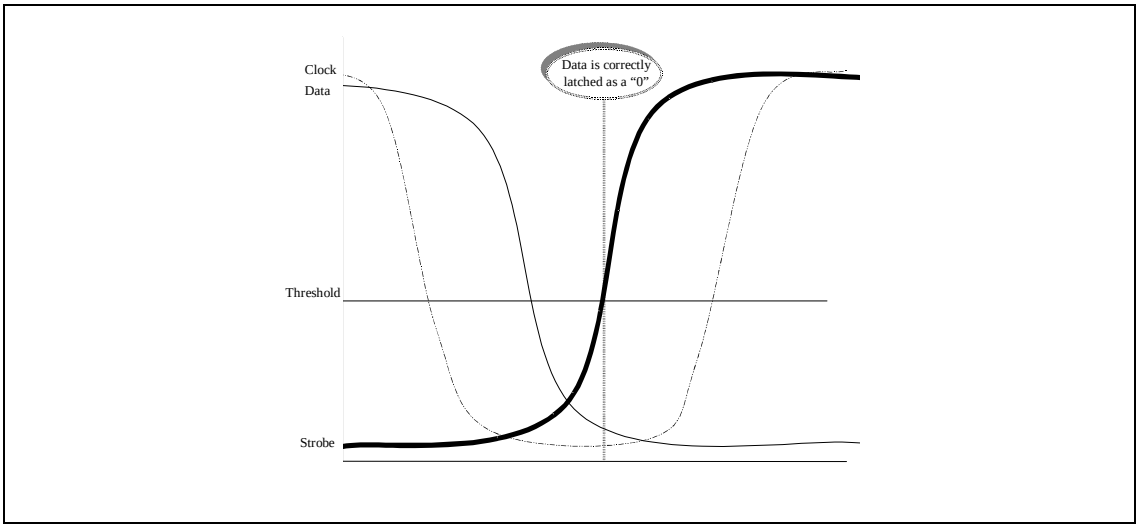
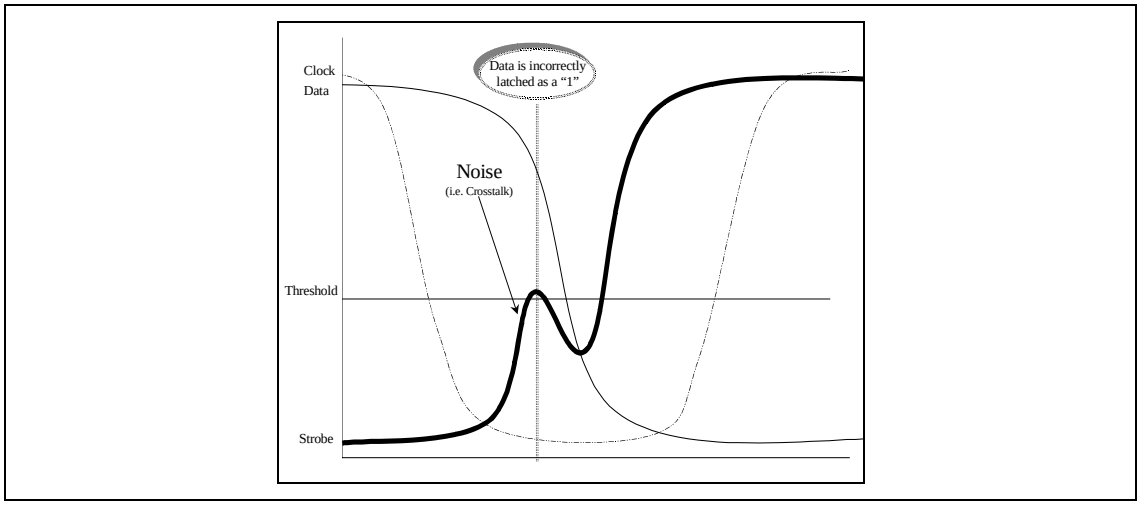


Figure 4: Effect of Crosstalk on Strobe Signal



For general signal integrity concepts and simulation methodologies, OEMs can request the *Signal Integrity Concepts* document.

Even though Intel provides layout and routing guidelines for high-speed interfaces, Intel strongly recommends that designers validate their board design through post-layout simulations.

Figure 5 shows the entire simulations-driven design development methodology. Simulations are performed before the layout of the PCB is completed. Trace lengths, loading conditions, and manufacturing tolerances are extensively analyzed. Based on the results of the simulations routing guidelines are generated.

Manufacturers are expected to follow the guidelines to design their boards. The post-layout simulation methodologies are developed with this assumption in mind. A typical post-layout simulation methodology requires very minimal simulations that would just validate the layout, based on the parameters that pre-layout analysis determined to be most sensitive. Otherwise, the designer must perform all the pre-layout analyses that need to be normally performed.

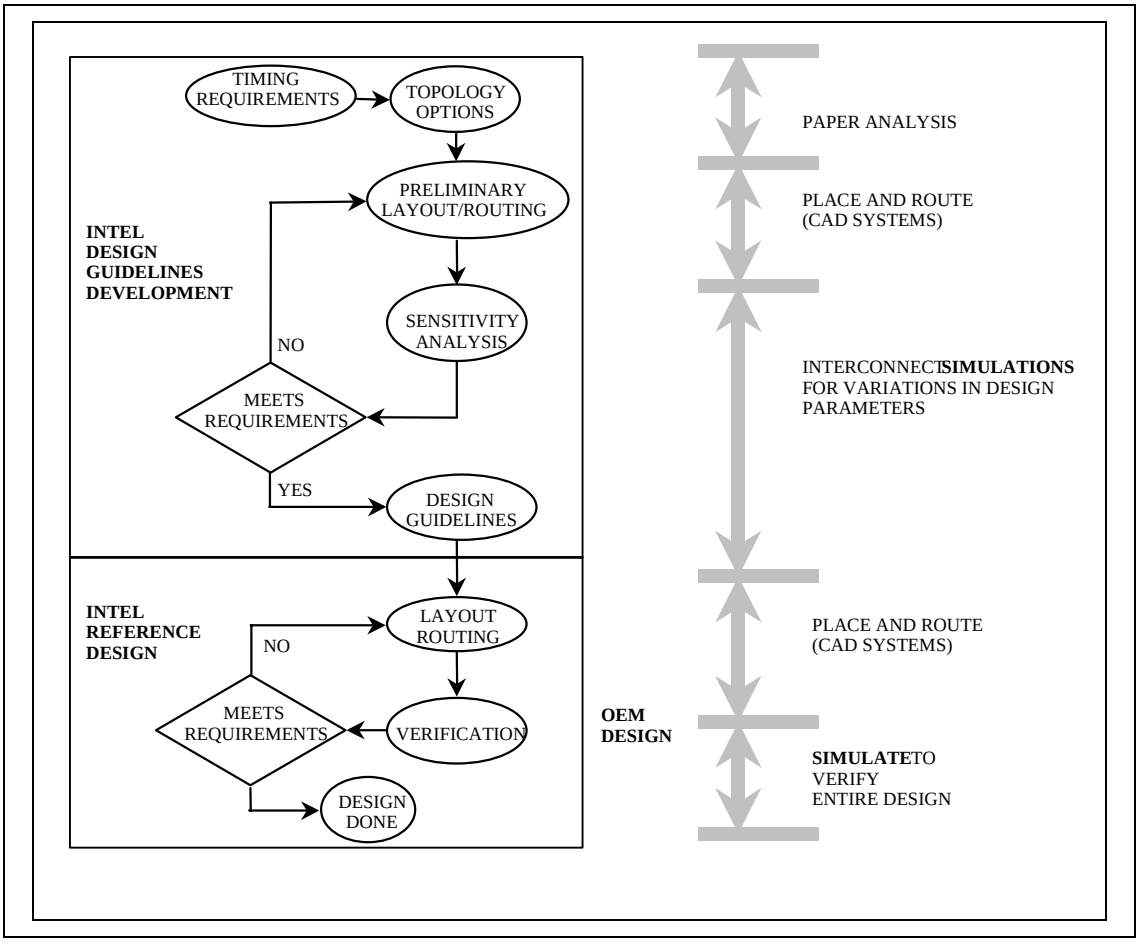
Following layout, the interconnect information is extracted for the board from the CAD layout tools. Simulations are run to verify that the layout meets timing and noise requirements. A small amount of "tuning" may be required. Sensitivity analysis dramatically reduces the amount of tuning required. The post- layout simulations should take into account the expected variation for all interconnect parameters.

The simulation methodologies Intel provides are geared towards finding violations in signal integrity and timing area. For signal integrity, designers should look for the following:

- Reflections (Undershoot/overshoot) and Ringing
- Crosstalk
- Non-monotonic edges

By measuring flight times, the designer must determine if there are any timing (setup and hold) violations. Therefore, the designer must estimate allowable flight times first. Flight time estimations are covered in various presentations on signal integrity and specific simulation methodologies. Additionally, an example of flight time measurement for hold time violations is described in Figure 5.

Figure 5: Simulation Driven Design Methodology



Intel specifies signal integrity at the device pads. Therefore, Intel recommends running simulations at the device pads for signal quality. However, Intel specifies core timings at the device pins, so simulation results at the device pins should be used later to correlate simulation performance against actual system measurements.

As the performance of the interfaces increases, more complex electrical phenomena should be considered, specifically crosstalk, ISI, and AC losses.

2.5.2.1. Crosstalk Analysis

For relatively low-frequency interfaces like PSB, designers performing crosstalk simulations may consider the package and connectors as non-coupled.

2.5.2.2. Inter-Symbol Interference

Inter-Symbol Interference (ISI) refers to the distortion or change in the waveform shape caused by the voltage and transient energy on the network when the driver begins its next transition.

ISI occurs when transitions in the current cycle interfere with transitions in subsequent cycles. ISI can also occur when the line is driven high, low, and then high in consecutive cycles (the opposite case is also valid). When the driver drives high on the first cycle and low on the second cycle, the signal may not settle to the minimum V_{OL} before driving the next rising edge, which results in improved flight times in the third cycle. Intel performed ISI simulations for the topology given in this section by comparing flight times for the first and third cycle. ISI effects do not necessarily span only three cycles so it may be necessary to simulate beyond three cycles for certain designs. After simulating and quantifying ISI effects, adjust the timing budget accordingly to take these conditions into consideration.

2.5.2.3. Losses

Losses are due to DC resistance of the traces (which are negligible for lengths on typical PCBs) and AC Losses comprised of skin effect and dielectric loss. AC losses are a function of the frequency, geometry of the traces, bulk resistivity, and dielectric material properties. Losses affect the signal by attenuating the amplitude and degrading the waveform edges. More discussion on group simulations-related concepts is provided in subsequent sections.

2.5.2.4. Flight Time Measurement

Flight time is the time difference between a signal crossing V_{REF} at the input pin of the receiver and the output pin of the driver crossing V_{REF} were it driving a *test load*.

Figure 6 shows the different configurations for T_{CO} testing and flight time simulation. The flip-flop represents the logic input and driver stage of a typical I/O buffer. T_{CO} timings are specified at the driver pin output.

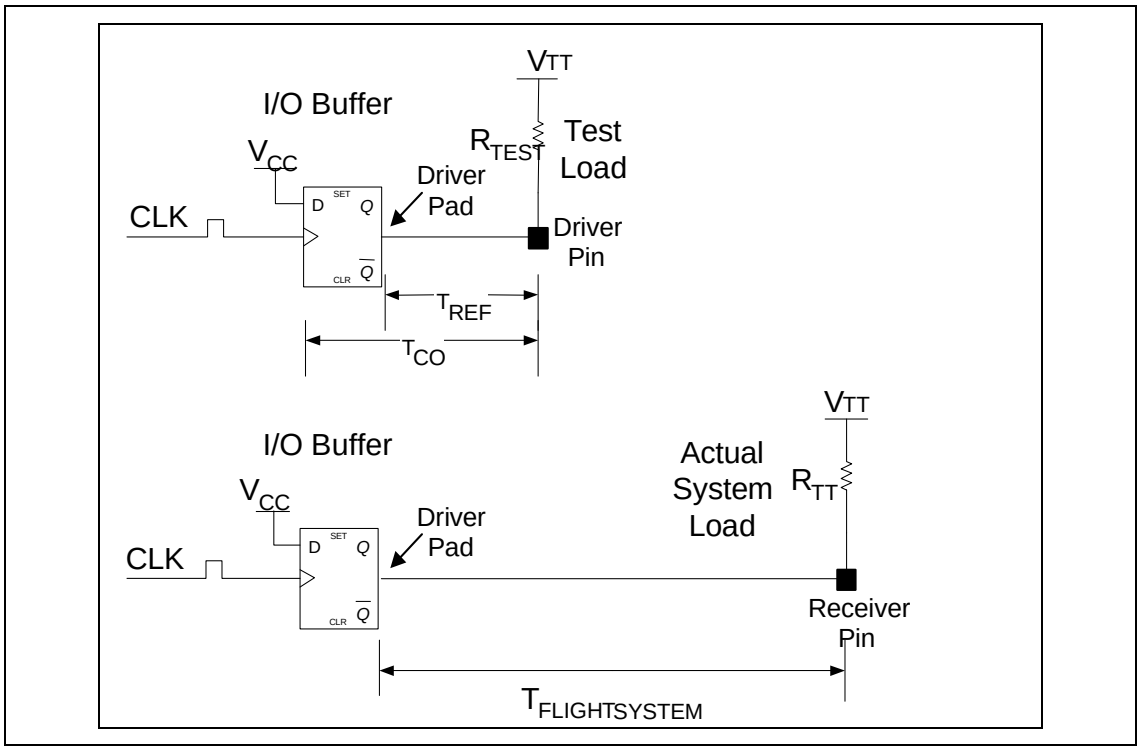
Sometimes Tco is presented in specification sheets into different test loads. Additional information is provided below.

2.5.2.5. Test Load

A test load is a circuit that is attached (as shown in

Figure 7) either in simulation or actual practice, to a driver to specify its AC timings. The test load parameters are included in the IBIS model of the device.

Figure 6: Test Load vs. Actual System Load



2.5.2.6. Origin of the Tco Number

The Tco comes from the manufacturer. The manufacturer attaches (either in simulation or actual practice) a test load to the output of a device, and then measures from a particular point on the clock to a particular point (Vmeas) on the output waveform.

2.5.2.7. Test Waveform

A test waveform is a waveform that is produced when a test load is connected to the output of a device. For proper measurement of flight times in a simulation tool, the test load used by the tool (and specified in the IBIS model) is the same test load that is used for the measurement of Tco.

Intel uses the simulation tool ICX from Mentor Graphics*, which automatically produces a test waveform by looking into the IBIS model for values of Cref, Rref, and Vref. The ICX tool produces a test waveform based on these values. The test waveform produced by the tool assumes no other loading but the test load. Therefore, this waveform is identical to the waveform produced at the output of a device when a manufacturer tests for and specifies Tco.

2.5.2.8. Flight Time

Flight time is defined as the additional delay between the driver and receiver as shown in

Figure 8. Flight time is introduced by the PCB interconnects and the component loading effects as compared to the datasheet specification load. For waveforms in a simulation tool, flight time is the difference (in time) between when a signal at the input pin of a receiver crosses some valid threshold, and the time that the driver crosses Vmeas were it driving the test load used to specify that driver's AC timings.

Warning: Flight Time is not measured from the driver pin to the receiver pin!

2.5.2.9. Example Using a Hypothetical Simulation Scenario

This section will show how to perform the following:

- Calculate minimum flight time
- How to use Tco in the equation for minimum flight time
- Measure the flight time in a simulation and compare it to the calculated minimum flight time
- How the selection of Tco doesn't matter, as long as you make your measurements from an appropriate test waveform

The simulation strategy is comprised of two steps:

- Budget for minimum flight time
- Comparison of actual flight time to budgeted flight time

2.5.2.10. Equation for Minimum Flight Time

Equation 1.

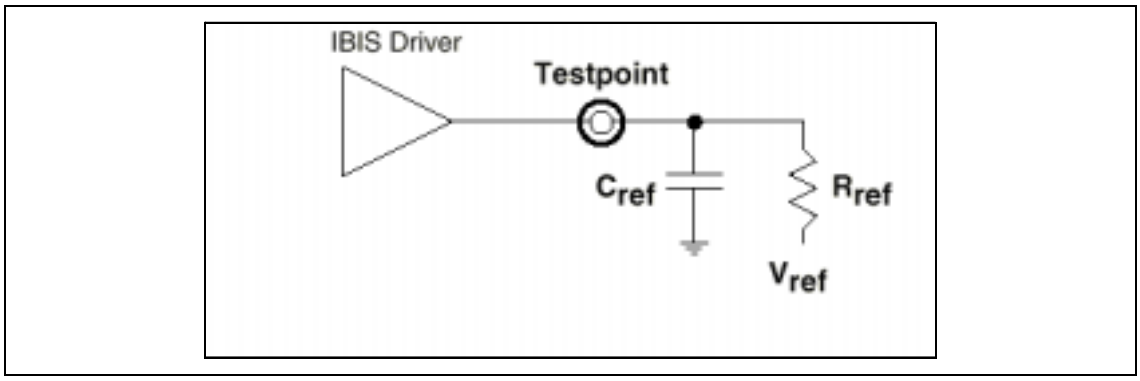
$$Tco(\min) + Tflight(\min) \geq Thold + Tskew$$

For example, arbitrarily assume that (Thold +Tskew) is 5 ns. Budget for minimum flight time when Tco (min)= 1.8 ns (Cref = 0 pF), Tflight(min) = 5 ns – 1.8 ns, and Tflight(min) = 3.2 ns.

Perform the following steps:

- Assume a particular net has one driver and one receiver with a transmission line between them. Further assume that from any particular clock edge to the receiver waveform, exactly 6 ns elapses.
- Next, the layout information is imported into our simulation tool. The IBIS models are loaded for the driver and receiver. Before loading the IBIS model for the driver, ensure that the value of Cref is 0 pF so that our simulation tool produces the correct test waveform.
- Run the simulation. The output of the simulation produces three waveforms. Two of them are of interest. One is the test waveform, which is the waveform produced by driving into a test load only, and the other waveform is the receiver waveform, which is the waveform that is produced when driving into a transmission line and the receiver. The third waveform of the unloaded output of the driver. Here is the critical point. Since Tco is already accounted for in the budget, the flight time must be measured from the point in time that corresponds to the Tco, which is thus accounted for. Measure from the test waveform at Vmeas to the appropriate threshold crossing of the receiver.

Figure 7: A Test Load



2.5.2.11. Comparison of Actual Flight Time to Budgeted Flight Time

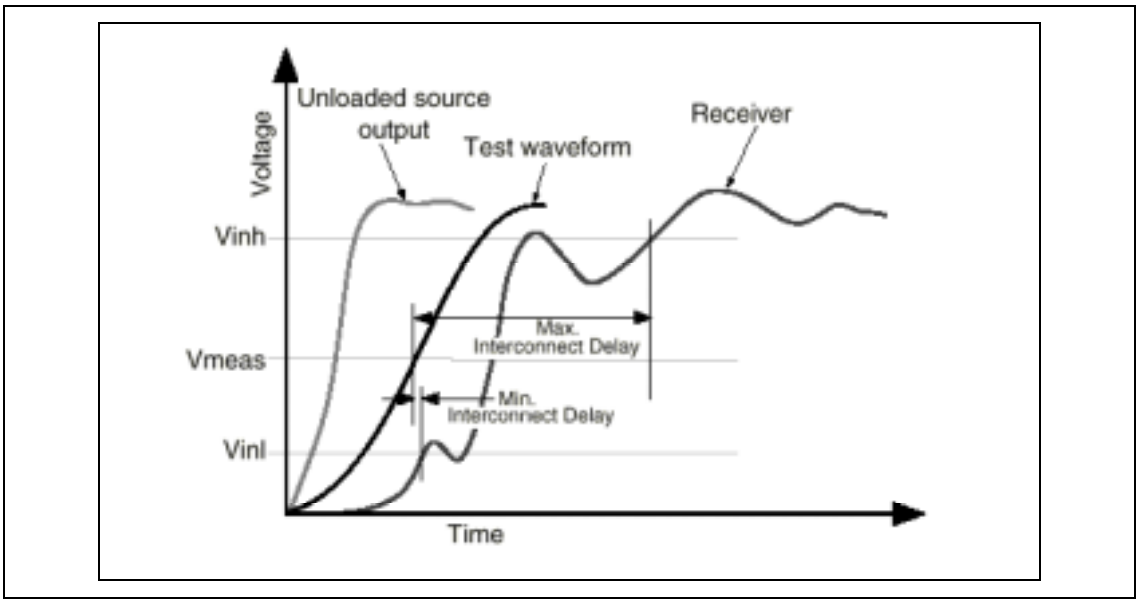
In the example measuring from test waveform to the receiver waveform (6 ns - 1.8 ns) = 4.2 ns. Our margin is therefore, (4.2 ns – 3.2 ns) = 1 ns of margin.

Budget for minimum flight time when Tco (min) = 3.0 ns (Cref = 50 pF), Tflight(min) = 5.0 ns – 3.0 ns, and Tflight(min) = 2.0 ns

In this case, follow the previous procedures with the following modifications.

- This time, when checking the IBIS model for the driver, ensure that the value of Cref = 50 pF so that the simulation tool produces the correct test waveform.
- Now, when "running" the simulation, note that the receiver waveform is exactly as in the previous case. (It has to be, since the VI and VT characteristics of the IBIS model are exactly as before. The only different information in the IBIS model is the value of Cref, which has nothing to do with the VT and VI curves.) However, *the test waveform is now shifted with respect to the receiver waveform*. In the previous example, the test waveform was simulated/produced into a 0-pF load. Therefore, on a set of coordinate axes, it "shows up" before the test waveform simulated/produced into a 50-pF load.

Figure 8: Flight Time Measurement



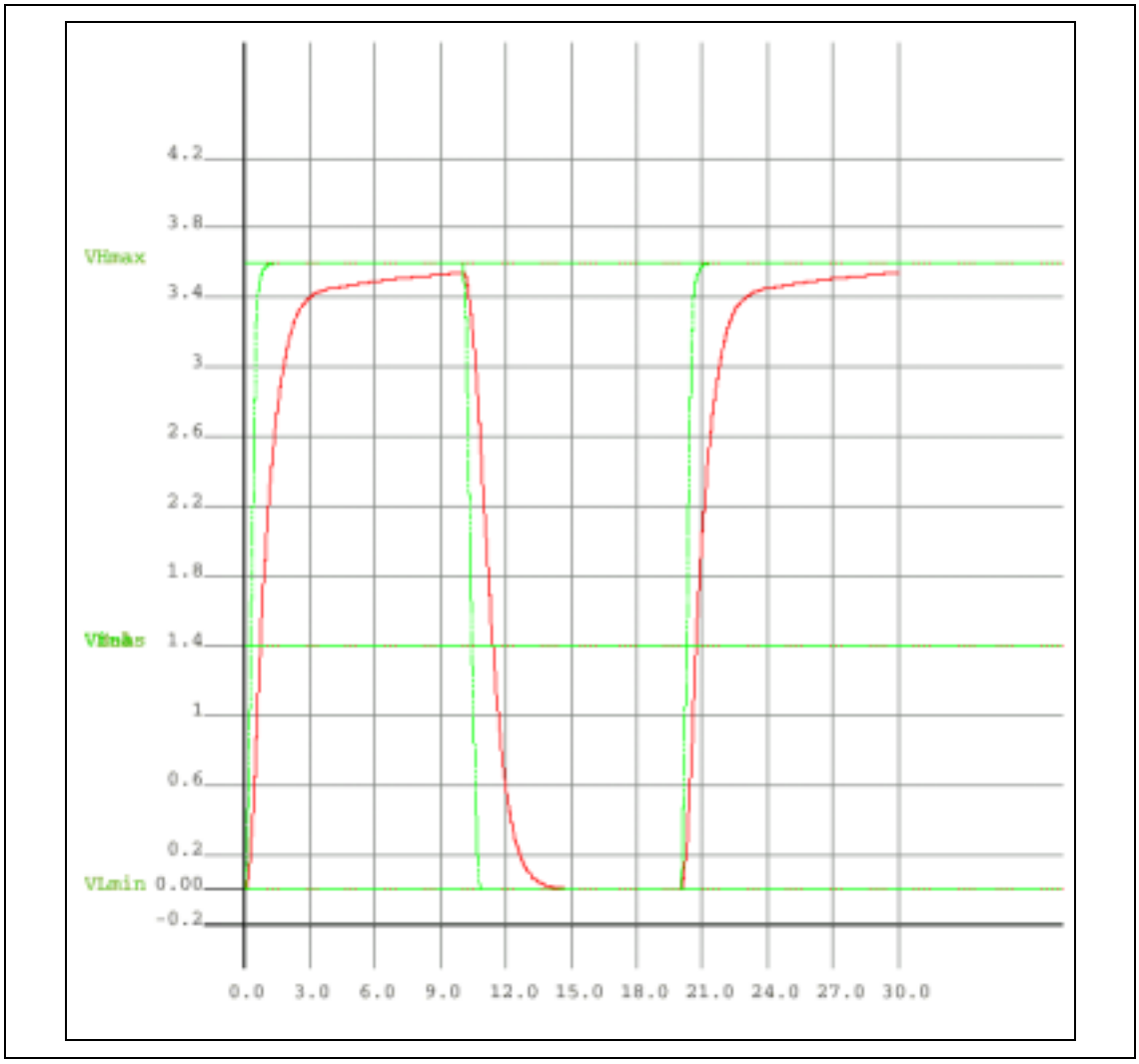
Note: The receiver waveform is in exactly the same place, and only the test waveform has shifted. Therefore, the flight time will be different as well since it is measured from a different relative position in time.

2.5.2.12. Comparison of Actual Flight Time to Budgeted Flight Time

In the example, measuring from the 50-pF test waveform to the receiver waveform, 3 ns are measured (6 ns – 3 ns). Thus the margin is (3 ns –2 ns) = 1 ns, just as before. Therefore, which specification of Tco is used does not matter, as long as the IBIS model test load information corresponds to the Tco used in budgeting the minimum flight time.

Figure 9 shows an illustration of test waveforms with different test loads.

Figure 9: Test Waveform Comparisons for Cref=0 pF (Green) and Cref= 50 pF (Red)



3. Clocking

The clock generator component required in a 815EM system is CK-815EM. The CK-815EM generates the clocks shown in Table 5.

Table 5: 815EM System Clocks

Amount	Name on Clk Driver	Used for	Routed to	Name on Receiver	Frequency	Volt
2	CPUCLK[0-1]	System Bus Clock	Processor	CLK	100 MHz	2.5V
			82815EM	HCLKIN		
2	APIC[0-1]	APIC Bus Clock	Processor	PICCLK	33 MHz	2.5V
			82801BAM	APICCLK		
8	PCICLK[1-7,F]	PCI Bus Clock	5 PCI Devices	CLK	33 MHz	3.3V
		PCI, LPC, FWH Bus Clock	82801BAM	PCICLK		
		FWH I/F Clock	FWH	CLK		
		LPC I/F Clock	LPC	CLK		
3	3V66[0-1], 3V66AGP	Hub link/AGP Bus Clock	82815EM	HLCLK	66 MHz	3.3V
		Hub link Clock	82801BAM	HLCLK		
		AGP Bus Clock	AGP device	CLK		
7	SDRAM[0-5], DCLK	Memory Interface Clocks	SDRAMs and 82815EM	SCLK on GMCH	100 MHz	3.3V
2	REF	Internal 82801BAM Logic	82801BAM	CLK14	14.318 MHz	3.3V
		Internal Super I/O Logic	Super I/O	Vendor Specific		
1	USB 48 MHz	USB	82801BAM	CLK48	48 MHz	3.3V
1	DOT	GFX Dot Clock	82815EM	DOTCLK	48 MHz	3.3V
1	VCH_CLK	VCH Clock	VCH	CLK	48/66 MHz	3.3V
1	CPU-ITP	ITP clock	ITP logic		100 MHz	2.5V

3.1. Description of Interface

The CK-815EM clock generator is a mixed voltage component. Some of the output clocks are 3.3V and some of the output clocks are 2.5V. As a result, the clock driver requires both 3.3V and 2.5V. These power supplies should be as clean as possible. Noise in the power delivery system for the clock driver can cause noise on the clock lines.

Figure 10 shows the clock distribution for the 815EM platform, and the system's clock skew timing requirements are listed in Table 7.

3.1.1. 815EM Clock Skew Relationship

- HCLK on the Processor and HCLK on the 82815EM
- HCLK and SCLK on the 82815EM
- SCLK on the 82815EM and the SDRAM clocks
- HCLK on the 82815EM and HLCLK on the 82815EM
- SCLK on the 82815EM and HLCLK on the 82815EM
- HLCLK on the 82815EM and HLCLK on the 82801BAM
- HLCLK on the 82801BAM and PCICLK on the 82801BAM

Figure 10: Clock Distribution on the 815EM Platform

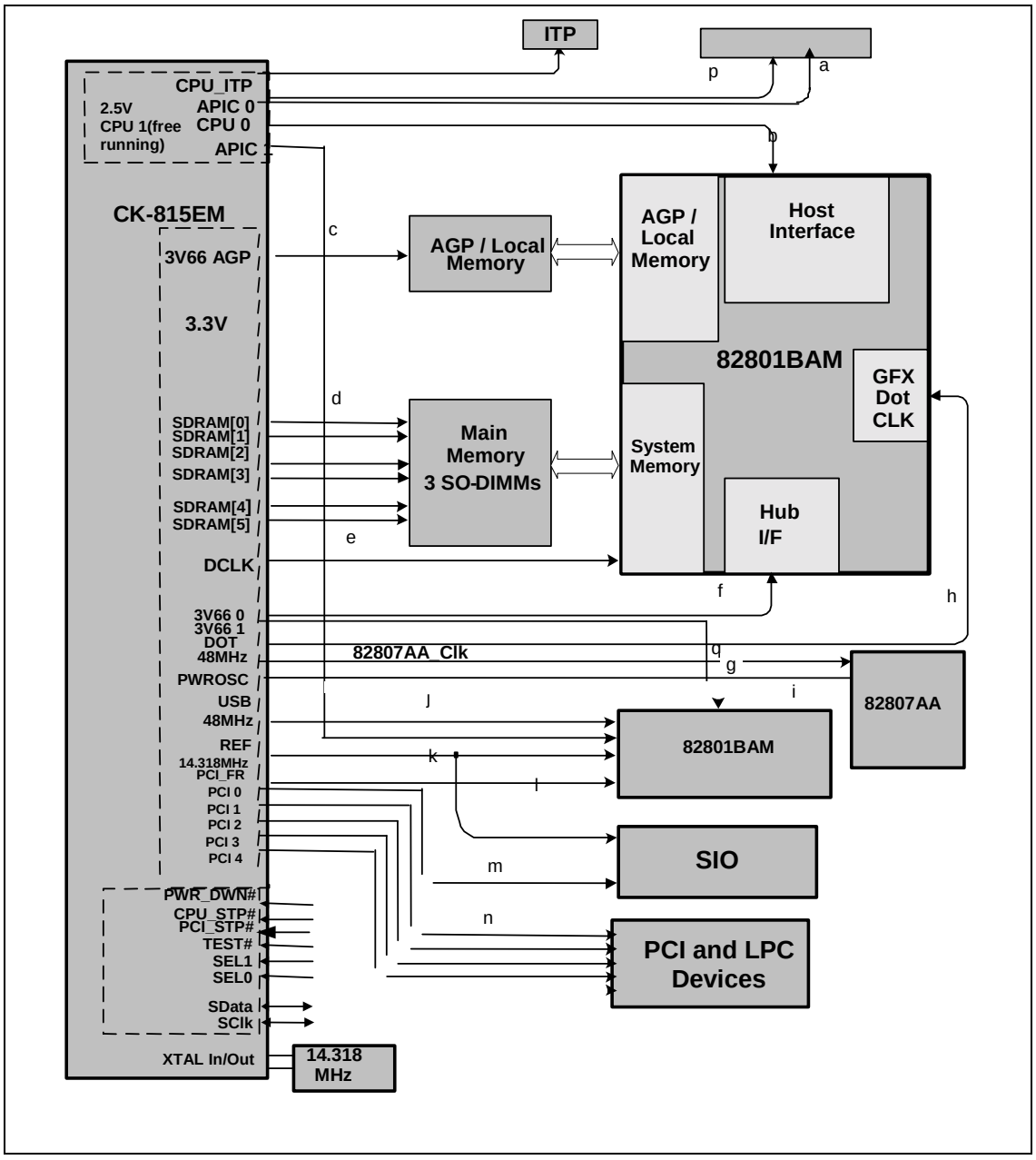


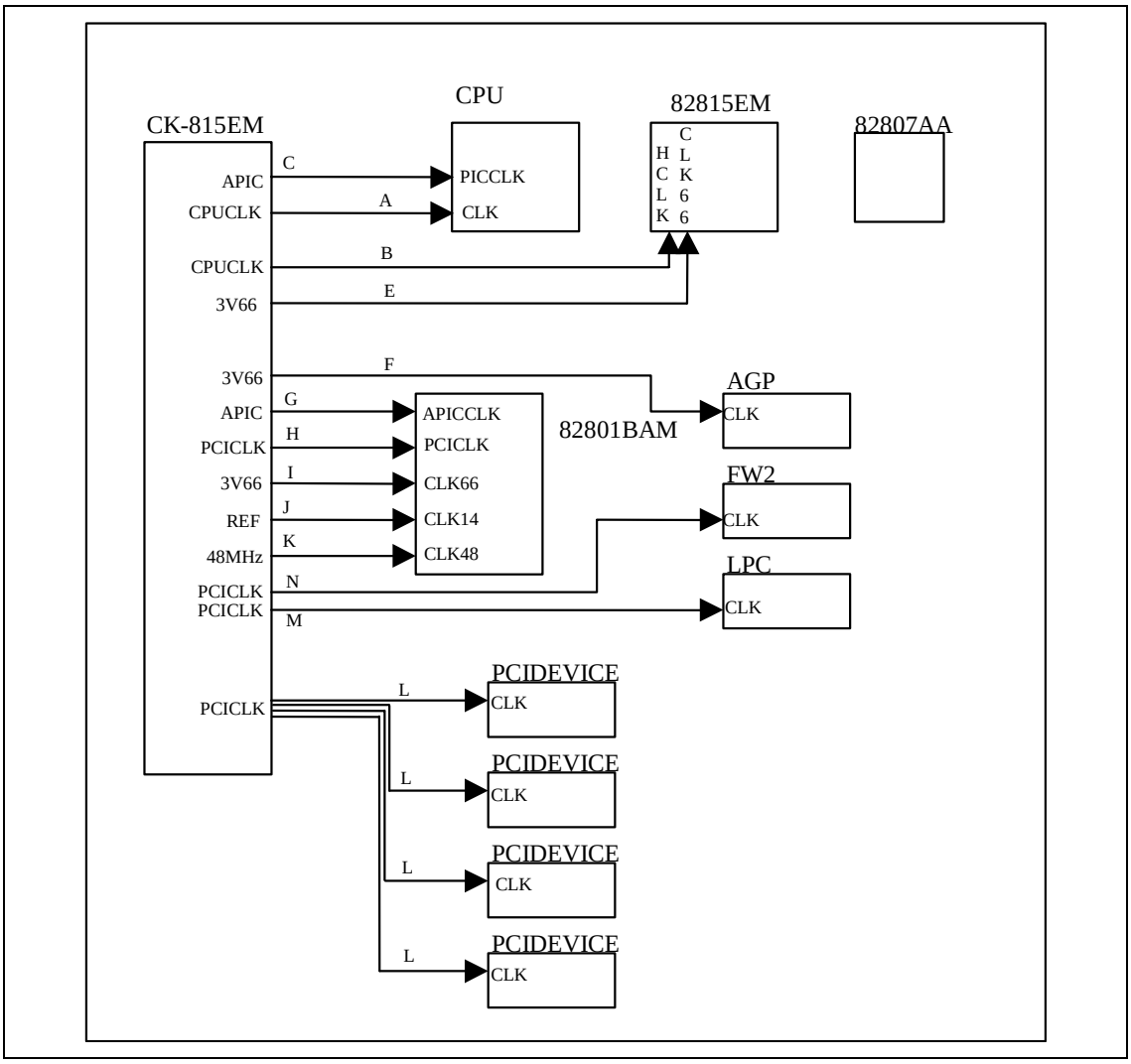
Table 6 lists the pin names from driver to clock inputs of the receivers on the platform.

Figure 11 and Table 8 show the clock trace lengths.

Table 6: Clock Driver and Receiver Pin Names

CK-815EM Pin	Component	Pin Name
PCICLK	PCI Device	CLK
	PCI Device	CLK
	PCI Device	CLK
	PCI Device	CLK
	PCI Device	CLK
	82801BAM (free running)	PCICLK
	LPC Super I/O	CLK
	FWH	CLK
3V66	82815EM	CLK66
	82801BAM	CLK66
48 MHz	82801BAM	CLK48
CPUCLK	CPU	BCLK
	ITP Logic	BCLK
	82815EM	HCLKIN
APIC	CPU	PICCLK
	82801BAM	APICCLK
PclkM	82815EM	HCLKOUT
SynclkN	82815EM	RCLKOUT

Figure 11: Clock Trace Lengths



3.2. Routing Guidelines

The rules for the routing of the 815EM platform clocks are shown in Table 7.

Table 7: System Clock Skew Requirements

Clock Symbols See Figure 10	Relationship	Skews (Allowed)						Note
		Clock Driver Pin-to-Pin (ps)		Board (ps)		Total (ps)		
		Min	Max	Min	Max	Min	Max	
a and b	CPU HCLK to 82815EM HCLKin	-175	+175	NA	NA	-290	+290	1
b and c	HCLK on 82815EM and 3V66AGP	-175	+175	-325	+325	-500	+500	
b and e	HCLK on 82815EM and SCLK on 82815EM	-500	+500	-100	+100	-600	+600	
d and e	SDRAM clocks and SCLK on 82815EM	-250	+250	-(380-x)	+(380-x)	-630	+630	2
b and f	HCLK on 82815EM and HLCLK on 82815EM	-500	+500	-400	+400	-900	+900	
e and f	SCLK on 82815EM and HLCLK on 82815EM	-500	+500	-400	+400	-900	+900	
f and g	HLCLK on 82815EM and HLCLK on 82801BAM	-175	+175	-325	+325	-500	+500	
g and l	HLCLK on 82801BAM and PCICLK on 82801BAM	-500	+500	-400	+400	-900	+900	
l and m	PCICLK on 82801BAM and PCI devices	-500	+500	-1500	+1500	-2000	+2000	
l and n	PCICLK on 82801BAM and PCI slots	-500	+500					3
I	CLCK onVCHm	NA	NA					4
H	DOTCLK on 82815EM	NA	NA					4
K	REFCLK on 82801BAM	NA	NA					4
P	APIC CLK on Processor	NA	NA					4

Board skew is included in the pin-to-pin skew of the driver by definition. Total skew includes a 115 ps adjustment factor for the unknowns. Total skew for (a and b) is best achievable for the PSB routing described in Chapter 4 of Rev 1.0.

Total skew for other clock is the amount tolerable by the 82815EM component.

Board skew for (a and b) includes skew due to input loading (packaging and die capacitance). Board skew for another clock is the amount that is allowed based on pin-to-pin skew on the clock driver and the skew that is tolerable at the clock inputs of the respective components.

"x" is the electrical length of the clock trace on the SO-DIMMs.

3.3. Trace Length Guidelines

Based on simulations, clock length is 8 inches maximum to avoid signal integrity issues. Recommended trace length information is given in Table 8.

Table 8: System Clocks Routing Details

Clock signal (See Figure 11)	Series R Value	Length (inches)	Comments
A	33 Ohms	t + 4	
B	33 Ohms	t + 4	
C	33 Ohms	t + 4	
D	33 Ohms	t	(not pictured)
E	33 Ohms	t + 4	22 pF at receiver after 33 ohm series resistor
F	33 Ohms	t + 4	
G	33 Ohms	t + 4	
H	33 Ohms	t + 4	
I	33 Ohms	t + 4	
J	33 Ohms	t + 4	
K	33 Ohms	t + 4	
L	33 Ohms	t + 4	
M	33 Ohms	t + 4	
N	33 Ohms	t + 4	

NOTE: Length "t" is to the SO-DIMM's connector. It has been simulated up to 4 inches. Length "t" trace spacing from driver to series termination resistor is 0.5 inches max and from series termination resistor to 22-pF capacitor is 0.1 inches.

For other clocks, trace length between driver to series termination resistor is 0.5 inches max.

All clocks should be routed 5mils wide with 15 mils spacing to any other signals.

Clocks must be routed on the same layer, internally to contain EMI. Intel strongly recommends that clock series resistors not be placed in R-packs to allow individually tunability if necessary. Vias should be minimized on all clock traces. Clock traces should not be allowed to cross a split plane.

3.4. Simulation Assumptions and Estimations

For clock distribution simulations, the following assumptions are made:

- PCB vendors control impedance tolerance to be ± 10% for Intel® 815EM chipset platforms.
- All clock traces will be inner traces. The microstrip stub from the via will be as short as possible.
- Package parasitics are included in the IBIS model.
- Although the clock driver is connected to many receivers, simulations will be performed only on the following:

The processor (100 MHz)

82815EM (100 MHz and 66 MHz)

AGP 2.0 (66 MHz)

Other clocks are not seen as critical, and if the routing guidelines are followed, there should not be any need for simulations to verify the design.

3.5. Post-layout Validation Methodology

The simulation methodology outlined here is for post-layout validation of the clock distribution circuit.

In order to produce a routing guideline for the clock distribution on the platform, a Monte Carlo analysis was performed on the topology shown in

Figure 10. Variations in board impedance, driver strength, dielectric constant, trace lengths, package parasitics, and series resistor values were accounted for to come up with the proper solution space in terms of meeting the skew requirements.

However, the OEM may wish to do their own post-layout simulation to ensure that they meet skew requirements between the processor and 815EM. Taking the extracted layout, the OEM can do a simulation analysis by varying resistors, buffer strength, board impedance, and the dielectric constant within their specified ranges. Resistor tolerance (± 5%) was found to have no impact in simulation results.

3.5.1. Define Simulation Cases Explicitly

Simulation cases must be defined first. Consider the following parameters:

- Velocity of signals , Er:
  Low Er:4.0 – High Er:4.4 Typ Er: 4.2
- Characteristic impedance of boards, Zo : 55Ω nominal ± 10%
- Weak, typical and strong output and slow, typical, fast input buffers

Perform the following steps.

1. Prepare simulation boards for different combinations of the variables listed above. Table 9 shows simulation boards for processor and 815EM clock distribution.

Table 9: Clock Distribution Simulation Boards

Boards	Clock Driver	PCB	Processor	815EM
Board1	Weak Buffer Ibis	High Er and Low Zo	Slow Buffer Ibis	Fast Buffer Ibis
Board2	Strong Buffer ibis	Low Er and High Zo	Fast Buffer Ibis	Slow Buffer Ibis
Board3	…….			
…….	……..			
Boardn	…….			

- Perform simulations for each board.
- The skew must be measured at the receivers' pads, not the pins.
- Ensure that signal quality (overshoot, undershoot, and ringback) and rise and fall time requirements are met on the receivers.
- Report violations to improve routing.

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4. Processor System Bus (PSB)

4.1. Description of Interface

The bus is a GTL+ interface with 64-bit data bus operating at 100 MHz. The mobile Intel® Pentium® III processor has an integrated termination on the PSB. The termination resistors for the bus are internal to the silicon and are 65Ω - 50Ω.

The mobile Intel® Pentium® III processor system bus uses a variation of the low-voltage swing GTL signaling technology. The mobile Intel® Pentium® III processor bus specification is similar to the mobile Intel® Pentium® II processor system bus specification, which itself is a version of GTL with enhanced noise margin and less ringing.

The GTL+ system bus depends on incident wave switching and uses flight time for timing calculations of the GTL+ signals, as opposed to capacitive derating. Intel recommends analog simulation of the system bus including trace lengths. Contact your Intel sales representative to receive the IBIS models for the mobile Intel® Pentium® III processor.

The GTL+ system bus of the mobile Intel® Pentium® II processor was designed to support high-speed data transfers with multiple loads on a long bus that behaves like a transmission line. However, in mobile systems the system bus has only two loads, the processor and the chipset; and the bus traces are short. In mobile systems, the GTL+ system bus is terminated at one end only. This termination is provided on the processor core.

All GTL+ signals shown in Table 10 are synchronous with the BCLK signal.

Table 10: PSB Signals

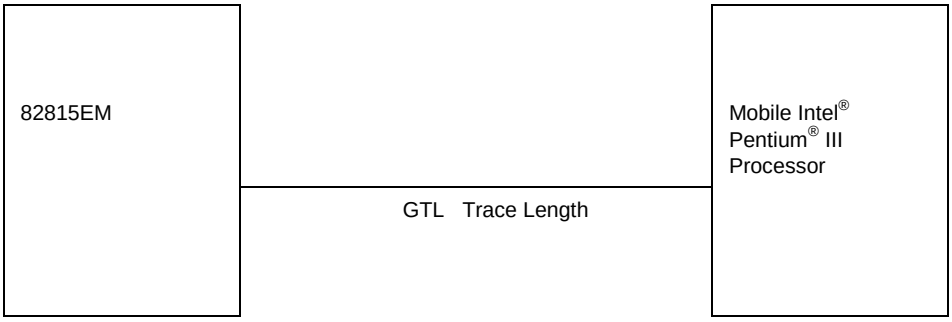
Signal Group Name	Signals
GTL+ Input	BPRI#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
GTL+ Output	PRDY#
GTL+ I/O	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BREQ0#, D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK# REQ[4:0]#, RP#

For more information on the processor system bus GTL+ signal, refer to the *Mobile Intel® Pentium® III Processor Electrical, Mechanical, and Thermal Specification.*

4.2. Routing Guidelines

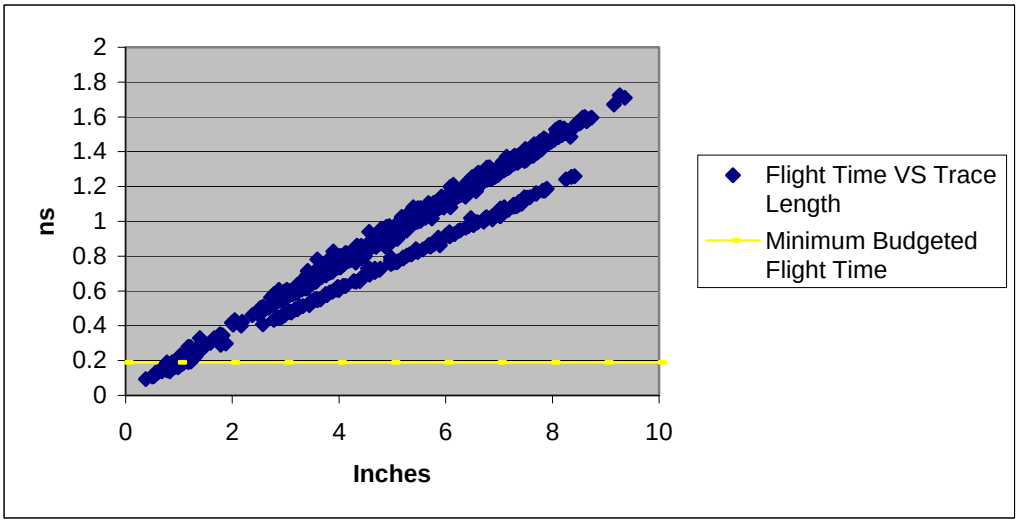
The mobile Intel® Pentium® III processor and the 815EM chipset configuration are shown in Figure 12.

Figure 12: PSB Traces



Through extensive pre-layout simulations, the trace lengths vs. flight times plots were obtained. A representative graph for fast corners is shown in Figure 13.

Figure 13: Trace Length vs. Flight Times (Processor Driving – Fast Corner Board Conditions)



On the graph, the solution space that satisfies the minimum trace length design requirements can be seen. The minimum trace length information is derived from this graph.

Segment lengths are defined at the component pins. Table 11 shows the length for the PSB trace.

Table 11: GTL Signal Trace Lengths

Segment	Min Length	Max Length
L	2.0 inches	4.0 inches

Perform the following steps:

1. Use 1:2 trace signal width/space ratio.
2. Avoid parallelism between signals on adjacent layers.
3. Since GTL+ is a low swing signal technology, it is important to isolate GTL+ signals from other signals by at least 0.025 inches. This will avoid coupling from signals that have larger voltage swings, such as 3-V PCI.
4. Route GTL+ address, data, and control signals in separate groups to minimize crosstalk between groups.

4.3. Simulation Assumptions and Estimates

For processor system bus simulations, the following assumptions are made:

- PCB impedance tolerance is ± 10%.
- All PSB traces will be inner, single stripline traces. The microstrip stub from the via to the mobile Intel® Pentium® III processor or the 82815EM will not exceed 75 mils.
- Triple and quadruple striplines are not supported.
- Microstrip traces are not supported.
- A fast board is defined as low Er and Strong buffer.
- A slow board is defined a high Er and weak buffer.
- Variations of Vtt are accounted for in the IBIS model.
- Package parasitics are included in the IBIS model.
- The clock skew between the Intel® 815EM chipset and the processor as seen in Table 7.

4.3.1. Timing Analysis

Allowable flight times are calculated using the equations below.

Equation 2.

$$T_{flightMax} \leq T_{cycle} - T_{coMax} - T_{su} - T_{clkSkew} - T_{jit} - T_{adj}$$

Equation 3.

$$T_{flightMin} \geq T_{ho} - T_{coMin} + T_{clkSkew} + T_{adj}$$

where:

$T_{flightMax}$: Maximum System Flight Time
$T_{flightMin}$: Minimum System Flight Time
T_{cycle} : System Cycle Time
T_{coMax} : Driver Maximum Clock-to-Out Delay
T_{su} : Receiver Setup Time
$T_{clkSkew}$: Hclk Skew
T_{jit} : Clock Generator Jitter, Maximum Edge to Edge Variation
T_{adj} : Adjustment Factor for SSO
T_{ho} : Receiver Hold Time
T_{coMin} : Driver minimum Clock-to-Out Delay

Using Equation 2 and Equation 3, the allowable flight times for signals are generated based on the processor and 82815EM timing specification as shown in Table 12.

Table 12: Allowable Flight Times

	Driver Tco		Receiver			Flight Limits	
	Min (ns)	Max (ns)	Setup (ns)	Hold (ns)		Max (ns)	Min (ns)
Mobile Intel® Pentium® III Processor Drvng	0.20	2.70	3.50	0.10	815EM Rcvng	1.63	0.19
815EM Drvng	1.05	4.10	1.20	0.80	Mobile Intel® Pentium® III Processor Rcvng	1.68	0.40

In Table 12 the flight times are calculated with the following data gathered from the specification documents and experimental values (T_{adj}).

T_{cycle} = 10.0 ns

$T_{clkSkew}$ = Clock pin-to-pin skew of 0.175 ns including routing and loading skew

T_{jit} = 0.250 ns

T_{adj} = 0.115 ns

4.4. Simulation Methodology

The simulation methodology outlined below is for post-layout validation of the PSB.

Simulation cases must be defined first. Consider the following parameters:

- Velocity of signals , Er:
  Low Er:4.0 – High Er:4.4
- Characteristic impedance of boards, Zo : 55Ω ±10%
- Weak, typical, and strong output and slow, typical, and fast input buffers

Perform the following steps:

1. Prepare the processor and 82815EM GTL models and boards as shown in the example below:

Table 13: System Processor Bus Simulation Boards

Boards	Processor	PCB	MCHm IBIS
Board1	Weak Buffer IBIS high Rtt	High Er and Low Zo	Slow Buffer IBIS
Board2	Weak Buffer IBIS low Rtt	High Er and Low Zo	Slow Buffer IBIS
Board3	Weak Buffer IBIS high Rtt	High Er and High Zo	Slow Buffer IBIS
Board4	Weak Buffer IBIS low Rtt	High Er and High Zo	Slow Buffer IBIS
Board5	Strong Buffer IBIS high Rtt	Low Er and High Zo	Fast Buffer IBIS
Board6	Strong Buffer IBIS low Rtt	Low Er and High Zo	Fast Buffer IBIS
Board7	Strong Buffer IBIS high Rtt	Low Er and Low Zo	Fast Buffer IBIS
Board8	Strong Buffer IBIS low Rtt	Low Er and Low Zo	Fast Buffer IBIS
Board9	Strong Buffer IBIS high Rtt	High Er and High Zo	Fast Buffer IBIS
Board10	Strong Buffer IBIS low Rtt	High Er and High Zo	Fast Buffer IBIS

- Perform simulations for each board.
  - Enable coupled line simulations with even and odd mode crosstalk on a board with high Er and strong driver (boards 9 and 10).
- Measure Flight Times from Vmeas on the driver to V_{IH} and V_{IL} on the receiver and compare with allowable flight times.
- Make sure that signal quality (overshoot, undershoot and ringback) and rise/fall time requirements are met on the receivers.
  - Flag all overshoot values above 2.0V
  - Flag all undershoot values below 0.350V
- Report violations to improve routing.

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5. SDRAM Memory Interface–82815EM

This section lists guidelines for routing the signal traces of the board design. The order of which signals are routed first and last will vary as some designers prefer routing all of the clock signals first, while others prefer routing all of the high-speed bus signals first. Either order can be used, as long as the guidelines listed below are followed. Intel recommends simulating the signals for proper signal integrity, flight time, and crosstalk.

5.1. Description of Interface

The 82815EM integrates a main memory DRAM controller with a 64-bit wide interface. The DRAM type supported is Synchronous (SDRAM). The 82815EM generates the CS#, DQM, CAS#, RAS#, WE#, CKE, and MA (multiplexed addresses) to control the SDRAM devices. The 82815EM DRAM interface operates in its own clock domain. The DRAM controller interface is fully configurable through a set of control registers.

The 82815EM supports industry standard 64-bit wide SO-DIMM modules with SDRAM devices (unregistered only). The two bank select lines SBS[1:0] and the 13 Address lines SMA[12:0] allow the 82815EM to support 64-bit wide SO-DIMMs using 16-Mb, 64-Mb, 128-Mb, and 256-Mb technology SDRAMs. The 82815EM has six SCS# lines, enabling the support of up to six 64-bit rows of DRAM, populated on up to three double-sided SO-DIMM modules. For write operations of less than a QWord, the 82815EM will perform a byte-wise write. The 82815EM targets SDRAM with CL2 and CL3 and supports both single and double-sided SO-DIMMs. 815EM provides refresh functionality with programmable rate (normal DRAM rate is 1 refresh/15.6 µs). Additionally 815EM provides a 1024-deep refresh queue. 815EM can be configured via the Page Closing Policy Bit in the 815EM Configuration Register to keep multiple pages open within the memory array. Pages can be kept open in any one row of memory. Up to four pages can be kept open within that row (815EM supports both two and four bank SDRAM). 815EM supports System Memory running at 100 MHz.

Note: The proper operating frequency must be selected during system bootup and cannot be changed during normal operation.

5.1.1. SDRAM Interface Signals

815EM supports 64-bit DRAM configurations. In the following discussion the term *row* refers to a set of memory devices that are simultaneously selected by a CS# signal. 815EM will support a maximum of six rows of memory when using SDRAM in a mobile configuration. Both single-sided and double-sided SO-DIMMs are supported. For the purposes of this discussion, a "side" of a SO-DIMM is equivalent to a "row" of SDRAM devices. 815EM has multiple copies of four of the address signals interfacing to memory. The copies reduce the loading on these signals as they are required to change in consecutive clocks, where the rest of the "command" signals are given two clocks to setup before the command is latched by the SDRAM devices (signaled by the assertion of CS#).

The interface consists of the following pins:

- SMD[63:0]
- SDQM[7:0]#
- SBS[1:0]#
- SMAA[12:0], SMAB[7:4]#, SMAC[7:4]#
- SCSA[5:0]#
- SCKE[5:0]#
- SCAS#
- SRAS#
- SWE#

815EM does not support Registered SO-DIMMs or SO-DIMMs populated with 4-bit wide or 32-bit wide SDRAM devices. Furthermore, only 3.3-V standard SDRAMs are supported. There is a table in the ICD that describes the possible SO-DIMM configuration supported by 815EM, along with the corresponding Register Codes used to identify them.

5.2. Mobile DRAM Layout Guidelines

The following list provides the mobile DRAM layout guidelines.

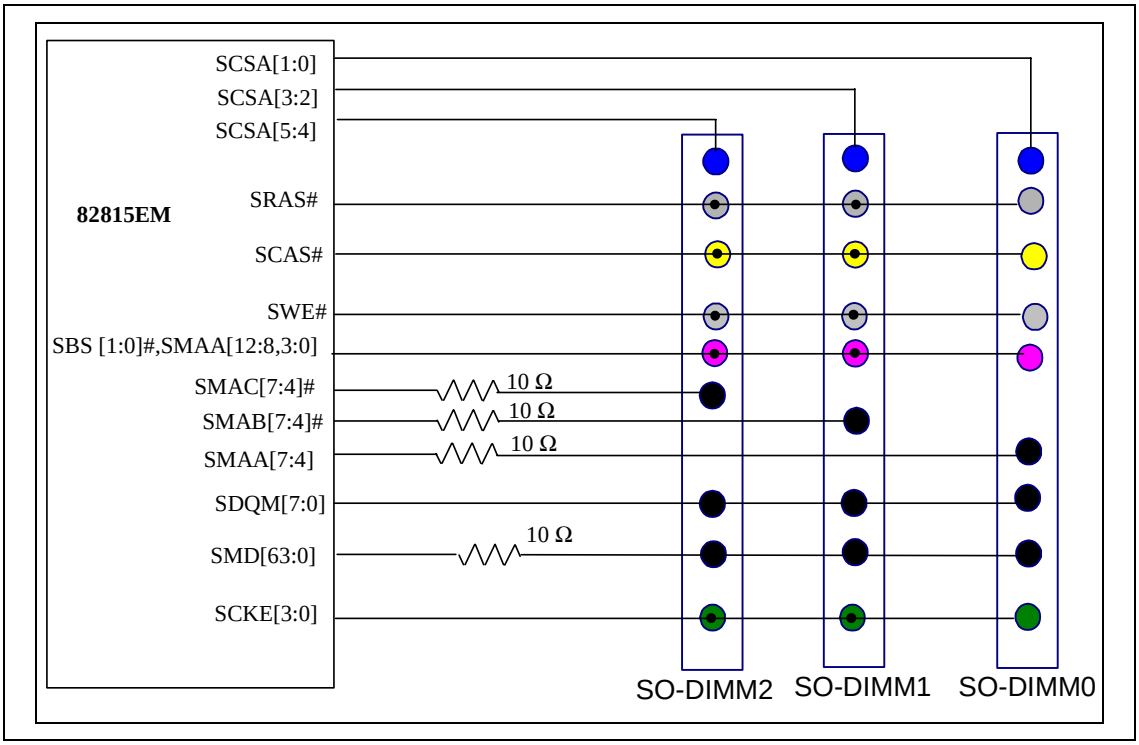
- The DRAM expansion socket for mobile is the 144-pin SO-DIMM.
- MAB[11]# should be connected to pin 106 of the SO-DIMM connector.
- MAB[12]# should be connected to pin 70 and pin 110 of the SO-DIMM connector.
- MAB[13] should be connected to pin 72 and pin 112 of the SO-DIMM connector.
- For onboard 64-Mbit SDRAM devices on the motherboard, MAB[11]# should be connected to A13/BA0 on the SDRAM device, and MAB[13] should be connected to A11 on the SDRAM device.
- The memory data bit traces may be byte swapped to simplify board routing and minimize trace lengths. This should also be done for the data bits within the byte channel.
- Board impedance should be 55Ω ±10%.
- All resistors should be maximum 5% tolerance.

- Populate furthest SO-DIMM first to avoid stub reflections.
- Any onboard memory should replace the furthest SO-DIMM socket.
- Place on-board DRAM and SO-DIMM connectors as near as possible to each other and the 82815EM.

5.2.1. SO-DIMM Connection - SDRAM

The guidelines cover the configurations where there are three SO-DIMM sockets present and running at 100 MHz. The socket farthest from the 82815EM component can be replaced with on-board memory. For memory configurations with on-board memory devices, the third SO-DIMM connector can be treated as a "phantom" connector on the board. The designer should follow the routing guidelines from the *100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin UNBUFFERED SO-DIMM SPECIFICATION Rev.* for the memory signals from the "phantom" connector to the on-board memory devices. Therefore, route the memory channel to the position that SO-DIMM0 would occupy in your design while following constraints in this routing guideline, and route from that point onwards according to the *100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin UNBUFFERED SO-DIMM Specification.*

Figure 14: SDRAM - Three SO-DIMMs at 100 MHz



5.2.2. Trace Lengths for Three SO-DIMM Designs

The figures and tables below show the topology for a three or two SO-DIMM design and provide the minimum and maximum trace lengths to the SO-DIMM connector pads for each signal group.

5.2.2.1. Data - SMD[63:0]

Figure 15: MD[63:0] Topology, Three SO-DIMM Sockets

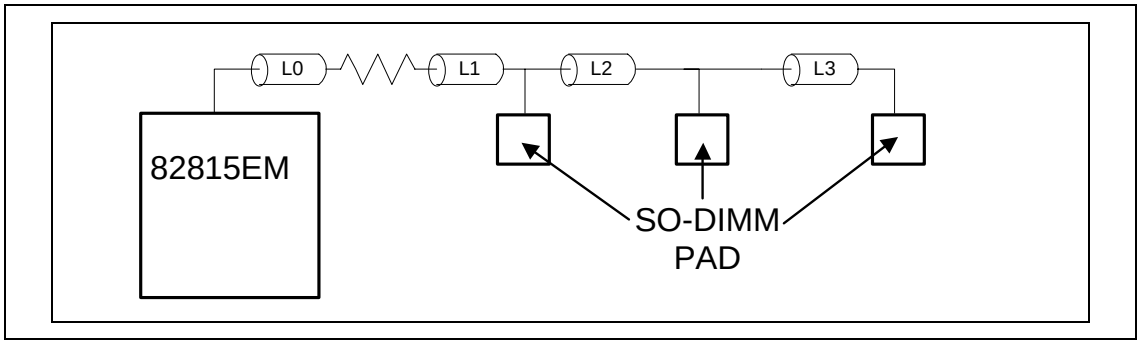


Table 14: Trace Lengths SMD[63:0], Three SO-DIMM Sockets

Section	Minimum	Maximum
L0	N/A	1.0 in
L0+L1	1.1 in	N/A
L2+L3	N/A	2.75 in
L0+L1+L2+L3	N/A	4.25 in
Series R	N/A	10 Ω

5.2.2.2. Data Mask - SDQM[7:0]

Figure 16: SDQM[7:0] Topology, Three SO-DIMMs

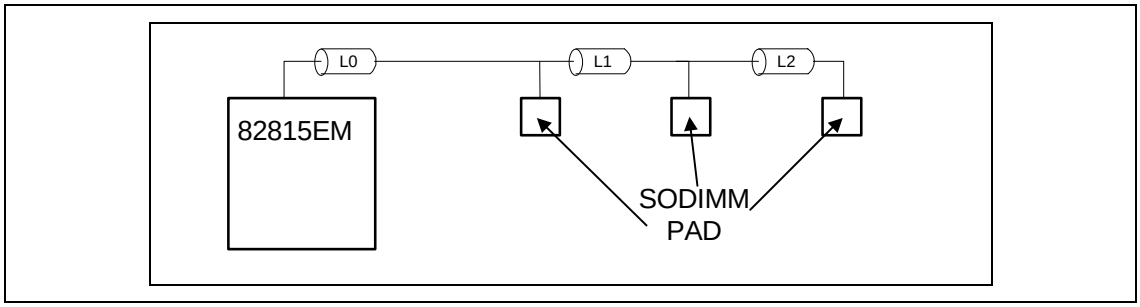


Table 15: Trace Lengths for SDQM[7:0], Three SO-DIMMs

Section	Minimum	Maximum
L0	1.0 in	N/A
L0+L1+L2	N/A	4.0 in

5.2.2.3. Chip Select - SCSA[5:0]

Figure 17: SCSA[5:0] Topology

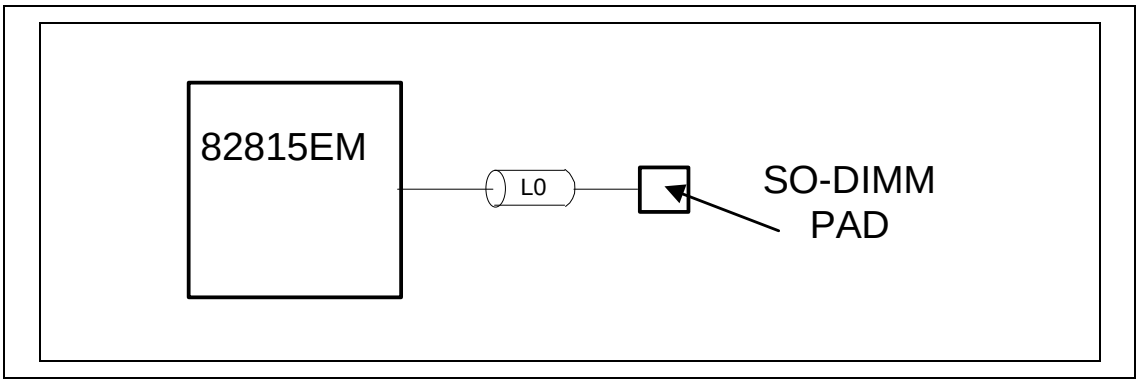


Table 16: Trace Lengths for SCSA[5:0]

Section	Minimum	Maximum
L0	1.0 in	6.0 in

5.2.2.4. Clock Enable -SCKE[5:0]

Figure 18: SCKE[5:0] Topology

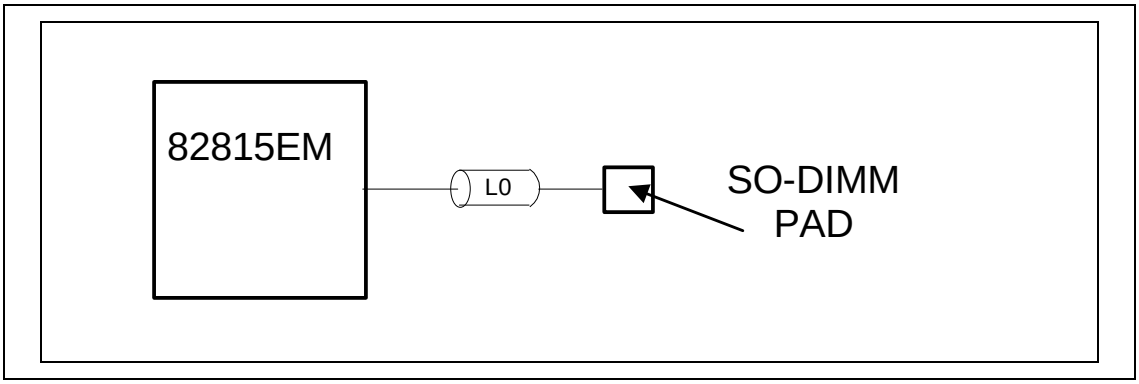


Table 17: Trace Lengths for SCKE[5:0]

Section	Minimum	Maximum
L0	1.0 in	6.0 in

5.2.2.5. Command - SMAX[13:0]#, SWE#, SRAS#, SCAS#

Figure 19: SMAX[13:0], SWE#, SRAS#, SCAS# Topology, Three SO-DIMMs

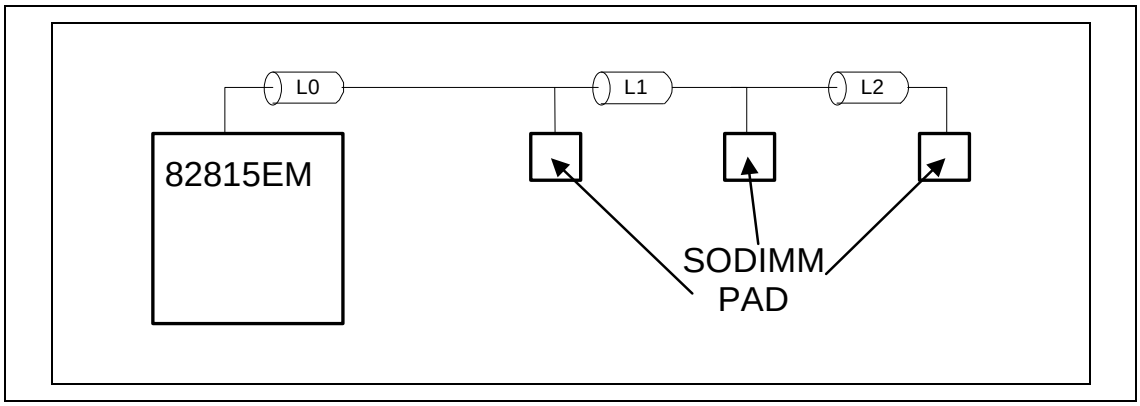


Table 18: Trace Lengths for SMAX[13:0], SWE#, SRAS#, SCAS#, Three SO-DIMMs

Section	Minimum	Maximum
L0	1.0	N/A
L0+L1+L2	N/A	6.0

5.2.3. SO-DIMM Placement Options

There are many ways to place the three SO-DIMMs on the system electronics. The following diagrams illustrate a few of the possibilities. The dotted outline indicates the SO-DIMM socket is on the other side of the board. In all the configurations, the last SO-DIMM (SO-DIMM0) slot can be replaced by on-board memory (please see Section 5.2.1). Three SO-DIMM designs will support only 100-MHz SDRAM.

Figure 20: All Three SO-DIMM Slots on One Side With First Two Back-to-Back

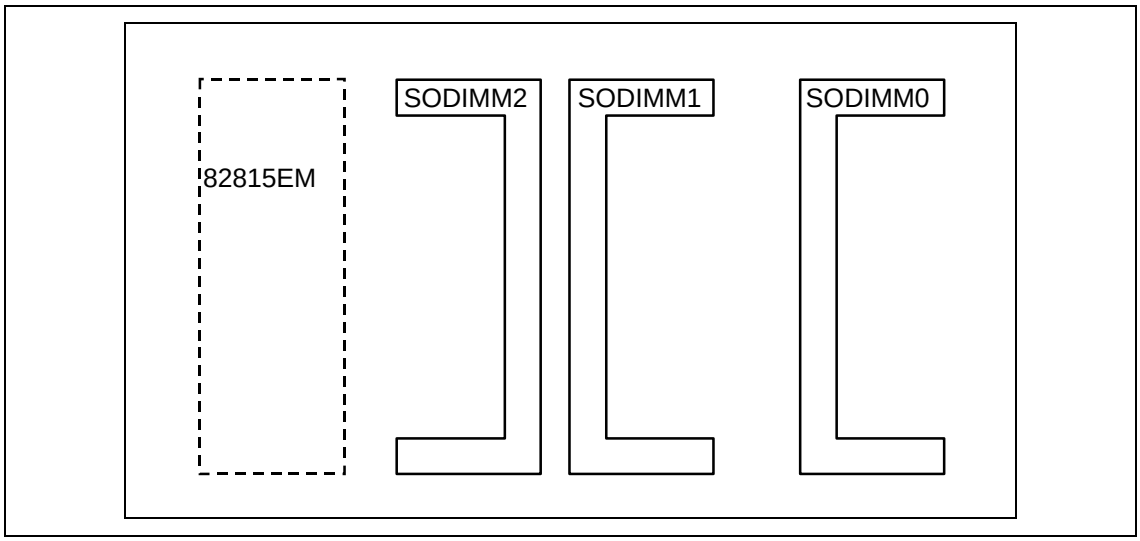


Figure 21: Two SO-DIMM Slots Back-to-Back and Third Slot on the Other Side

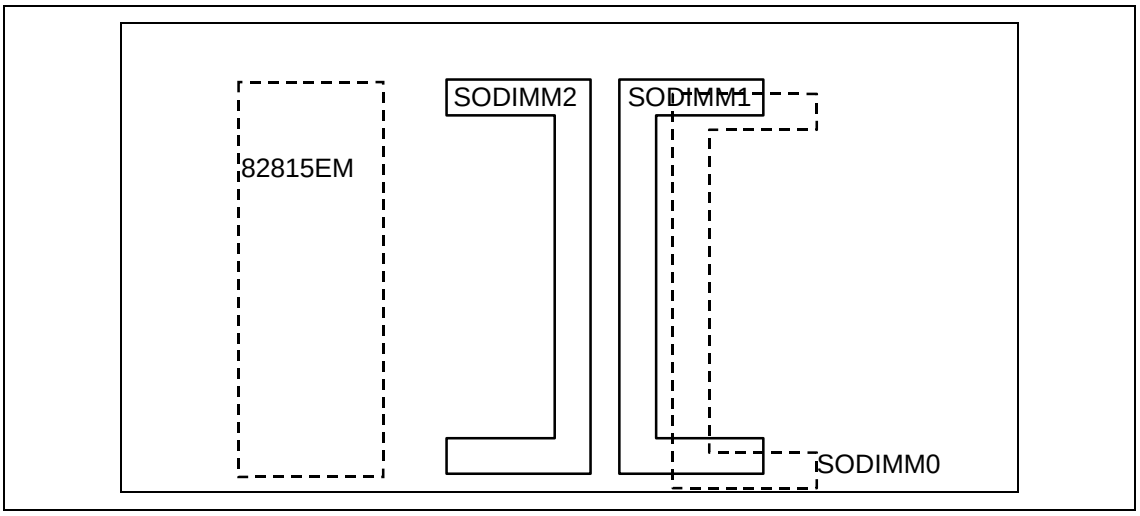


Figure 22: Two SO-DIMMs on One Side and One on the Other Side (1)

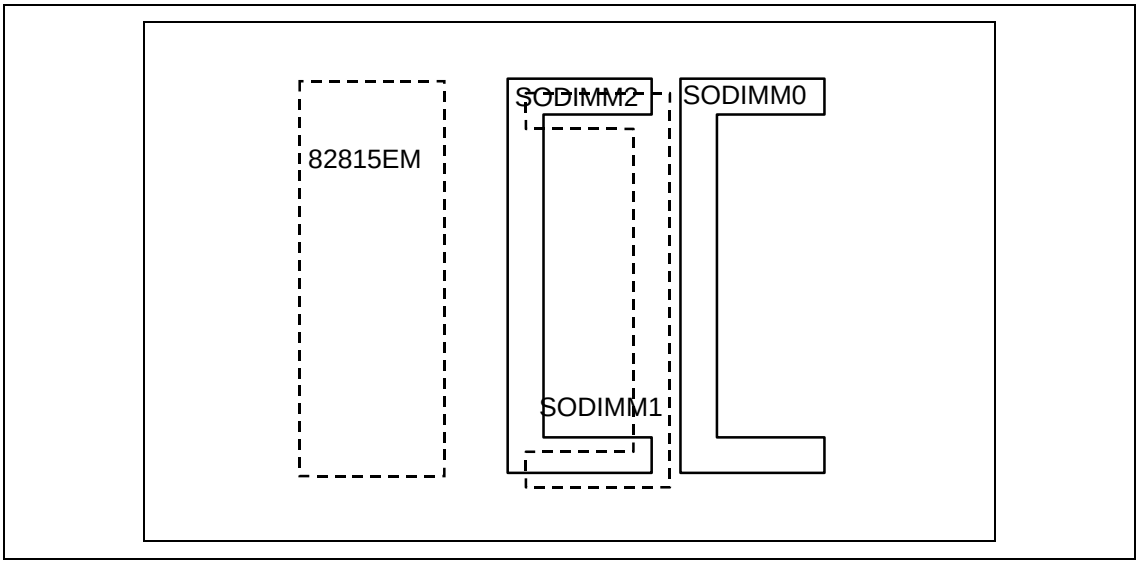
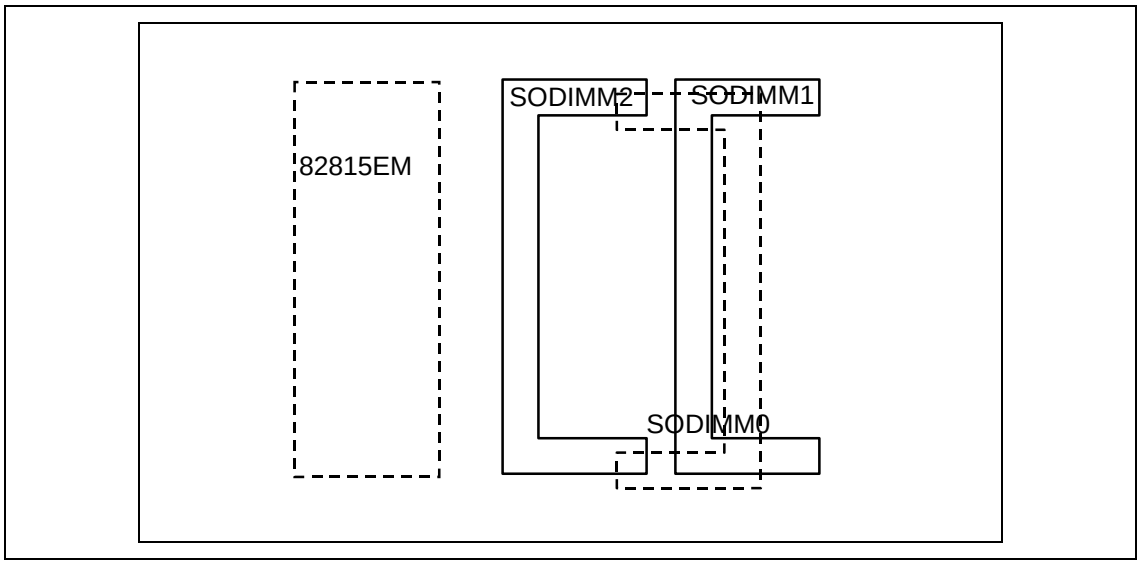


Figure 23: Two SO-DIMMs on One Side and One on the Other Side (2)



6. External Graphics Subsystem Interface

6.1. Description of Interface

The functionality of the AGP Interface is enhanced by allowing 4X data transfers (four data samples per clock) and 1.5-V operation. Additional performance enhancement and clarifications, such as *fast write* capability, are included. For detailed AGP Interface functionality (protocols, rules and signaling mechanisms, etc.) refer to the latest *AGP Interface Specification Revision 2.0*, which can be obtained from http://www.agpforum.org.

The 4X operation of the AGP interface provides for "quad-sampling" of the AGP AD (Address/Data) and SBA (Sideband Addressing) buses so that the data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of a 15 ns (66-MHz clock) or 3.75 ns. It is important to note that 3.75 ns is the data cycle time; not the clock cycle time. During 2X operation, the data is sampled twice during a 66-MHz clock cycle, therefore, the data cycle time is 7.5 ns.

In order to allow these high-speed data transfers, the 2X mode of AGP operation uses source synchronous data strobing. During 4X operation, the AGP interface uses differential source synchronous strobing.

With data cycle times as small as 3.75 ns, and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great, or there is noise on the interface, incorrect data will be sampled.

The low-voltage operation on AGP (1.5V) requires even more noise immunity. For example, during 1.5-V operation, V_{ilmax} is 570 mV. Without proper isolation, crosstalk could create signal integrity issues.

6.1.1. AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: 1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals. Each group has different routing requirements. In addition, within the 2X/4X timing domain signals, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. However, trace length matching requirements only need to be met within each set of 2X/4X timing domain signals.

The signal groups are documented in Table 19 and Table 20.

Table 19: AGP 2.0 Signal Groups

1X Timing Domain	
	CLK
	RBF#
	WBF#
	ST[2:0]
	PIPE#
	REQ#
	GNT#
	PAR
	FRAME#
	IRDY#
	TRDY#
	STOP#
	DEVSEL#
2X/4X Timing Domain	
Set #1	AD[15:0]
	C/BE[1:0]#
	AD_STB0
	AD_STB0#[1]
Set #2	AD[31:16]
	C/BE[3:2]#
	AD_STB1
	AD_STB1#[1]
Set #3	SBA[7:0]
	SB_STB
	SB_STB#[1]
Miscellaneous, Async	
	USB+
	USB-
	OVRCNT#
	PME#
	TYPDET#
	PERR#
	SERR#
	INTA#
	INTB#

These signals are used in 4X mode ONLY.

Table 20: AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

Throughout this section, the term *data* refers to AD[31:0], C/BE[3:0]# and SBA[7:0]. The term *strobe* refers to AD_STB[1:0], AD_STB#[1:0], SB_STB, and SB_STB# (see Table 19). The term *strobe* refers to one of the strobes as it relates to the data in its associated group.

6.2. AGP Routing Guidelines

This section contains information on the timing domain routing guidelines.

6.2.1. Trace Length Requirements for the AGP 1X

The AGP 1X timing domain signals (refer to Table 19) have maximum trace lengths of 9.5 inches. This maximum applies to *all* of the signals listed as 1X timing domain signals in Table 19. In addition to this maximum trace length requirement, these signals must meet the trace spacing and trace length mismatch requirements in Section 6.2.3.2.

AGP 1X timing domain signals (refer to Table 19) can be routed with 5-mil minimum trace separation.

6.2.2. Trace Length Mismatch

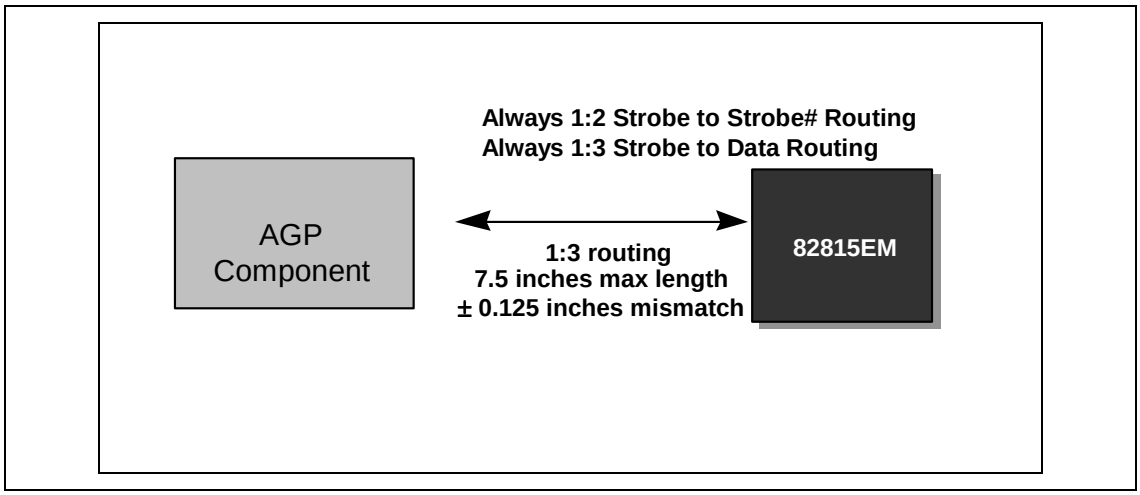
There are no trace length mismatch requirements for 1X timing domain signals. These signals must meet minimum and maximum trace length requirements.

6.2.3. Trace Length Requirements for AGP 2X/4X

These trace length guidelines apply to ALL of the signals listed as 2X/4X timing domain signals in Table 19. In addition to these maximum trace length requirements, these signals must meet the trace spacing and trace length mismatch requirements in Section 6.2.3.2.

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. These routing rules are divided by trace spacing. In 1:2 spacing, the distance between the traces is two times the width of traces. Simulations in a mobile environment support this rule.

Figure 24: AGP Layout Guidelines



If the AGP interface is less than 6 inches, a 1:2 trace spacing is required for 2X/4X lines. These 2X/4X signals must be matched to their associated strobes within ±0.5 inches for designs that require less than 6 inches between the graphics device and the 82815EM.

Longer lines have more crosstalk; therefore, in order to maintain skew longer line lengths require a greater amount of spacing between traces. For line lengths greater than 6 inches and less than 7.5 inches, 1:3 routing is required for all data lines and strobes. For these designs, the line length mismatch must be less than ± 0.125 inches within each signal group.

Reduce line length mismatch to ensure added margin. In order to reduce trace to trace coupling (crosstalk), separate the traces as much as possible.

6.2.3.1. Trace Spacing Requirements

AGP 2X/4X timing domain signals (refer to Table 19) must be routed as documented in Table 21. They should be routed using 5-mil traces. Additionally, the signals can be routed with 5-mil spacing when breaking out of the 82815EM. The routing must widen to the requirement in Table 21 within 0.3 inches of the 82815EM package.

Since the strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB , and SB_STB#) act as clocks on the source synchronous AGP interface, special care should be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g. AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5-mil traces with 10 mils of space (1:2) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 15 mils (1:3). The strobe pair must be length matched to less than ± 0.1 inches (that is, a strobe and its compliment must be the same length within ± 0.1 inches).

6.2.3.2. Trace Length Mismatch Requirements

The length-matching requirement depends on the maximum AGP trace length. If the longest AGP 2X/4X trace is greater than 6.0 inches (and less than 7.5 inches), then signals must be matched with ± 0.125 inches. If there are no AGP 2X/4X traces longer than 6.0 inches, then signals must be matched within ± 0.5 inches.

Table 21: AGP 2.0 Data Lengths Relative to Strobe Length

Max Trace Length	Trace Spacing	Strobe Length	Minimum Trace Length (inches)	Maximum Trace Length (inches)
< 7.25	1:3	X	X – 0.125	X + 0.125
< 6.0 in	1:2	X	X – 0.5	X + 0.5

The trace length minimum and maximum (relative to strobe length) should be applied to each set of 2X/4X timing domain signals **independently**. That is, if AD_STB0 and ADSTB0# are 5 inches, then AD[15:0] and C/BE[1:0] must be between 4.5 inches and 5.5 inches. However AD_STB1 and ADSTB1# can be 3.5 inches (and therefore AD[31:0] and C/BE#[3:2] must be between 3 inches and 4 inches). In addition, all 2X/4X timing domain signals must meet the maximum trace length requirements.

To avoid additional signal mismatch all of the lines within a group need to be the same type (either microstrip or stripline). This is because microstrip (surface traces) and stripline (buried traces) have different trace velocities, and mixing these can increase the flight time mismatch beyond acceptable limits.

All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to 0 inches as possible to provide timing margin. Table 22 shows AGP 2.0 routing summary.

Table 22: AGP 2.0 Routing Guideline Summary

Signal	Maximum Length (inches)	Trace Spacing (5 mil traces)	Length Mismatch (inches)	Relative To	Notes
1X Timing Domain	9.5	5 mils	No Requirement	N/A	
2X/4X Timing Domain Set#1	7.5	15 mils	± 0.125	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	7.5	15 mils	± 0.125	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	7.5	15 mils	± 0.125	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length
2X/4X Timing Domain Set#1	6.0	10 mils	± 0.5	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	6.0	10 mils	± 0.5	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	6.0	10 mils	± 0.5	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length

NOTE: Each strobe pair must be separated from other signals by at least 15 mils.

6.2.3.3. AGP Clock Skew

The maximum total AGP clock skew, between the 82815EM and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter, which originates on the motherboard, add-in card (if used), and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but at all points on the clock edge that falls in the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew (the motherboard designer shall determine how the 0.9 ns are allocated between the board and the synthesizer).

6.2.3.4. Pull-ups

AGP control signals require pull-up resistors to VDDQ (refer to Section 10.2) on the motherboard to ensure they contain stable values when no agent is actively driving the bus. The signals requiring pull-up resistors are **1X Timing Domain Signals. See below.**

- FRAME#
- TRDY#
- IRDY#
- DEVSEL#
- STOP#
- SERR#
- PERR#
- RBF#
- INTA#
- INTB#
- PIPE#
- REQ#

It is critical that these signals are pulled up to VDDQ– not 3.3V.

The trace stub to the pull-up resistor on 1X timing domain signals should be kept to less than 0.5 inch to avoid signal reflections from the stub.

The strobe signals require pull-up/pull-downs on the motherboard to ensure they contain stable values when no agent is driving the bus. The 2X/4X Timing Domain signals are shown below.

- AD_STB[1:0] (pull-up to VDDQ)
- SB_STB (pull-up to VDDQ)
- AD_STB[1:0]# (pull-down to ground)
- SB_STB# (pull-down to ground)

The trace stub to the pull-up/pull-down resistor on 2X/4X timing domain signals should be kept to less than 0.1 inch to avoid signal reflections from the stub.

The pull-up/pull-down resistor value requirements are shown in Table 23.

Table 23: AGP 2.0 Pull-up Resistor Values

Rmin	Rmax
4 kΩ	16 kΩ

The recommended AGP pull-up/pull-down resistor value is 8.2 kΩ.

Note: These signals must be terminated as suggested above when using the internal graphics engine and the local memory interface.

6.2.3.5. Impedance

The motherboard impedance should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. Intel strongly recommends an impedance of 55Ω ±10%; otherwise, signal integrity requirements may be violated. Refer to 7.5 for an example stackup.

6.2.3.6. Termination

The AGP Interface does not require external *termination*.

6.3. Simulation Assumptions and Estimates

The simulation methodology described below is for a post-layout design validation. It is provided for OEMs that have a post-layout simulation tool, such as ICX (Mentor Graphics*), ISIS (Viewlogic*), etc.

While layout guidelines have been developed based on a comprehensive pre-layout analysis of the technologies and simulations, OEMs are still encouraged to simulate their designs to make sure design timing and signal integrity requirements are met.

6.3.1. Assumptions, Definitions, and Specifications

The source synchronous solution space consists of all designs in which the flight time mismatch between a strobe and its associated data is less than the total allowable skew. See Equation 4 below.

Equation 4.

$$T_{skew} = T_{flightdata} - T_{flightstrobe}$$

Where $T_{flightdata}$ and $T_{flightstrobe}$ are the driver-pad-to-receiver-pad flight times of the data and the strobe respectively.

- The AGP physical interface is a point-to-point topology using 1.5V or 3.3V signaling. The baseline performance level for AGP uses a 66-MHz clock to provide a peak bandwidth of 266 MB/S. A double-clocking data technique is used to achieve twice the baseline width. Thus, the AGP 2X mode provides a peak bandwidth of 533 MB/S. AGP 2X mode is a superset of the 1X mode. The AGP 4X mode clock provides high-performance levels with a peak bandwidth of 1066 MB/S. This bandwidth is achieved by using a quad clocked data transfer methodology, which allows four times

as much data to be transferred every 66-MHz clock cycle. AGP 4X mode is a superset of the 1X and 2X modes. Thus, all components supporting 4X must also support 1X and 2X modes.

- The flight time skew simulations simulate all parameters that could cause a skew between two signals, including motherboard and add-in card line lengths, effective capacitance in the buffer models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and ISI induced skews.

6.3.1.1. Simulation Model

A model for simulation purposes is shown in Figure 25.

Figure 25: AGP Simulations Model

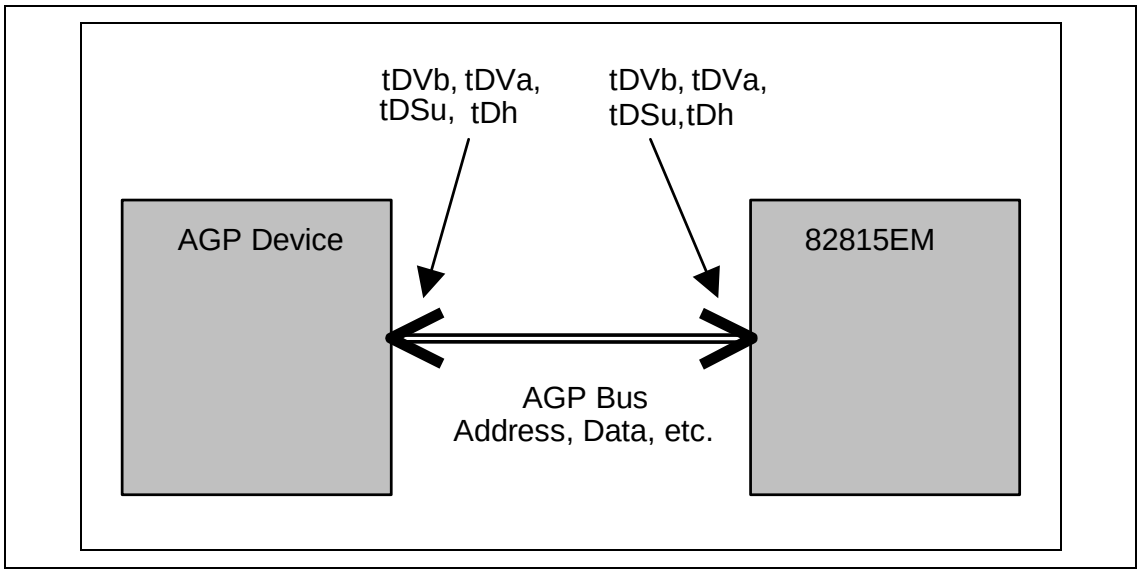
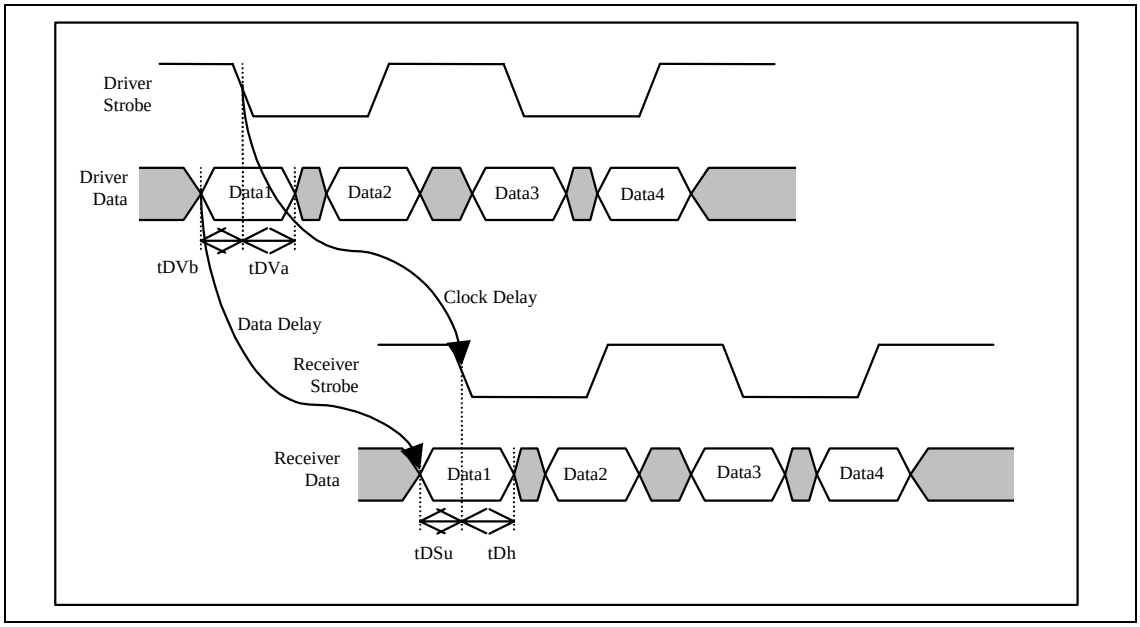


Figure 26: 4X Driver- Receiver Waveforms Relationship Specification



As shown in Figure 26, the setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides. However, note that available margins are not absolute values. Any skew due to routing and loading differences, any coupling differences in the parallel traces, and any effects of SSO (ISI, ground bounce, etc.) should be accounted for in the timing budget as they will reduce the total available margin for the design.

As an example here, the timing budget that was used for mobile 4x simulations is listed in Table 24.

Table 24: Allowable Interconnect Skew Calculation

Component	Skew Element	Symbol	Setup	Hold	Units
Driver	Data Valid before Strobe	tDVb	950		ps
	Data Valid after Strobe	tDVa		1150	ps
Interconnect	Allowable Skew		550	-450	ps
Receiver	Data Setup to Strobe	tDSu	400		ps
	Data Hold from Strobe	tDh		700	ps

All numbers in the table are from the MCM-m specification documents. As seen in the table, total amount of skew is only 1000 ps. This skew includes allocations for SSO, crosstalk, and routing and loading introduced skew.

6.4. Post-layout Validation Methodology

The simulation methodology outlined here is for post-layout validation of the AGP only and does not apply to pre-layout analysis of the design. Although the methodology was developed using the ICX simulation tool, the goal is to make the methodology applicable to other post layout tools as much as possible.

6.4.1. Define Simulation Cases Explicitly

Simulation cases must be defined first, considering the following parameters:

- Velocity of signals, Er: Low Er:4.0 – High Er:4.4
- Characteristic impedance of boards:
- Zo: 55Ω ± 10%
- Weak, typical and strong output and slow, typical and fast input buffers

Prepare the models and boards as shown below.

Table 25: AGP Interface Simulation Boards

Boards	82815EMm	PCB	AGP Device
Board1	Weak Buffer IBIS	High Er and Low Zo	Slow Buffer IBIS
Board2	Weak Buffer IBIS	High Er and High Zo	Slow Buffer IBIS
Board3	Strong Buffer IBIS	Low Er and High Zo	Fast Buffer IBIS
Board4	Strong Buffer IBIS	Low Er and Low Zo	Fast Buffer IBIS
Board5	Strong Buffer IBIS	High Er and High Zo	Fast Buffer IBIS

1. Perform both READ and WRITE simulations.
   - Enable coupled EVEN/ODD crosstalk (Board 5).
   - Patterns with buffers switching high to low or low to high (0000 to FFFF or FFFF to 0000) or 0000 to 1110 or 1111 to 0001 or 1110 to 0001 or 0001 to 1110.
   - Use ISI patterns (e.g., 000001 at 266 MHz), Otherwise, allow ~ 150 ps for ISI in timing spreadsheet.
2. For each board's specific Er, change dielectric thickness to meet Zo specified.
3. Run simulations on each board for strobe lines and also the data lines.
4. Measure flight times of all signals from Vmeas on the driver to Vmeas on the receiver.
5. Also make sure signal quality requirements are met.
6. Calculate skews between the strobe and data signals.
7. Report violations to improve routing

6.5. AGP Power Requirements

6.5.1. AGP VDDQ

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller. This voltage is ALWAYS 3.3V. VDDQ is the interface voltage. In AGP 1.0 implementations, VDDQ was also 3.3V. For the designer developing an AGP 1.0 motherboard, there is no distinction between VCC and VDDQ as both are tied to the 3.3-V power plane on the motherboard.

AGP 2.0 requires that these power planes are separate. In conjunction with the 4X data rate, the AGP 2.0 Interface Specification provides for low-voltage (1.5V) operation. The VCC and VDQ power supplies are such that the VDDQ voltage level is never more than 0.5V above the VCC voltage level.

6.5.2. Vref Generation for AGP 2.0 (2X and 4X)

6.5.2.1. 3.3-V AGP Interface (AGP 2x)

The 3.3-V AGP interfaces will use only one Vref. Therefore, there is only one resistor divider on the AGP controller that will divide VDDQ down to Vref for the 815EM and AGP controller. See following figure.

6.5.2.2. 1.5-V AGP Interface (AGP 2x and 4x)

In order to account for potential differences between VDDQ and GND at the 815EM and graphics controller, both devices use *source generated Vref*. That is, the Vref signal is generated at the graphics controller and *sent* to the 815EM, and another Vref is generated at the 815EM and *sent* to the graphics controller (refer to

Figure 28).

Both the graphics controller and the 815EM are required to generate Vref. The voltage divider networks consist of AC and DC elements as shown in

Figure 28.

The Vref divider network should be placed as close to the *AGP* interface as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the Vref signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity.

All resistors used in above reference generation schemes should have ± 1% tolerance.

6.5.3. Compensation

The 815EM AGP interface supports resistive buffer compensation (RCOMP). For Printed Circuit Boards with characteristic impedances of 55Ω, tie the GRCOMP pin to a 36.5-Ω, 1% pull-down resistor (to ground) via a 10-mil wide, very short (≈0.5 inches) trace.

Figure 27: AGP 2.0 Vref Generation and Distribution for 3.3-V Interface

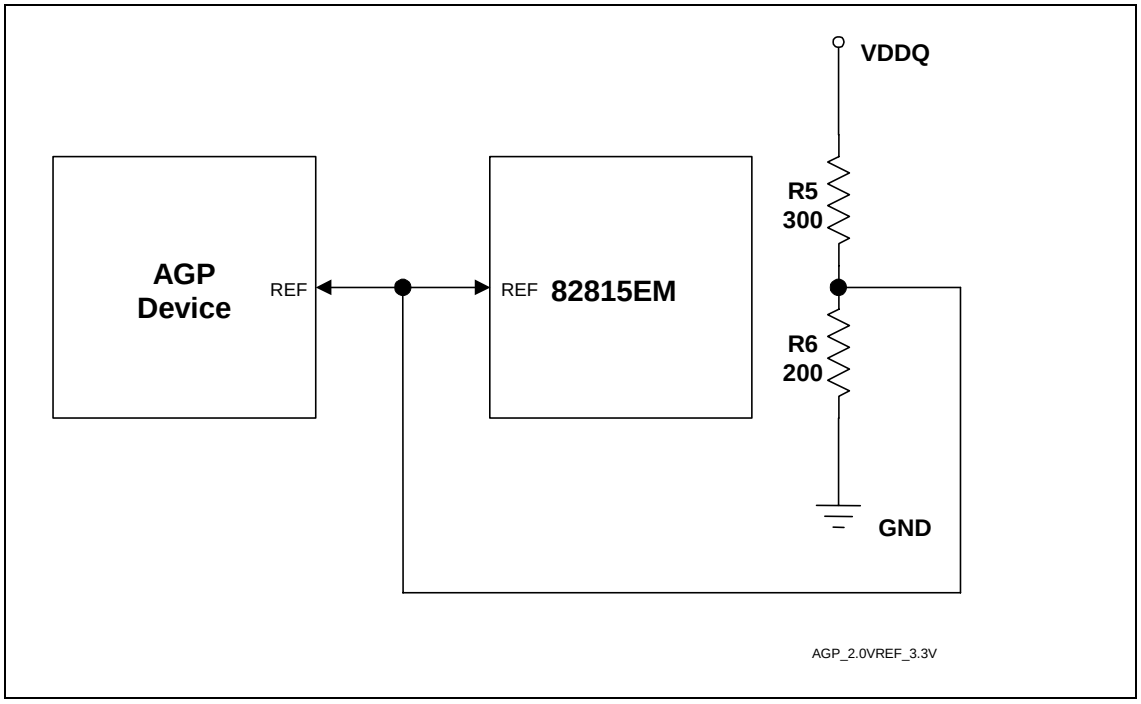
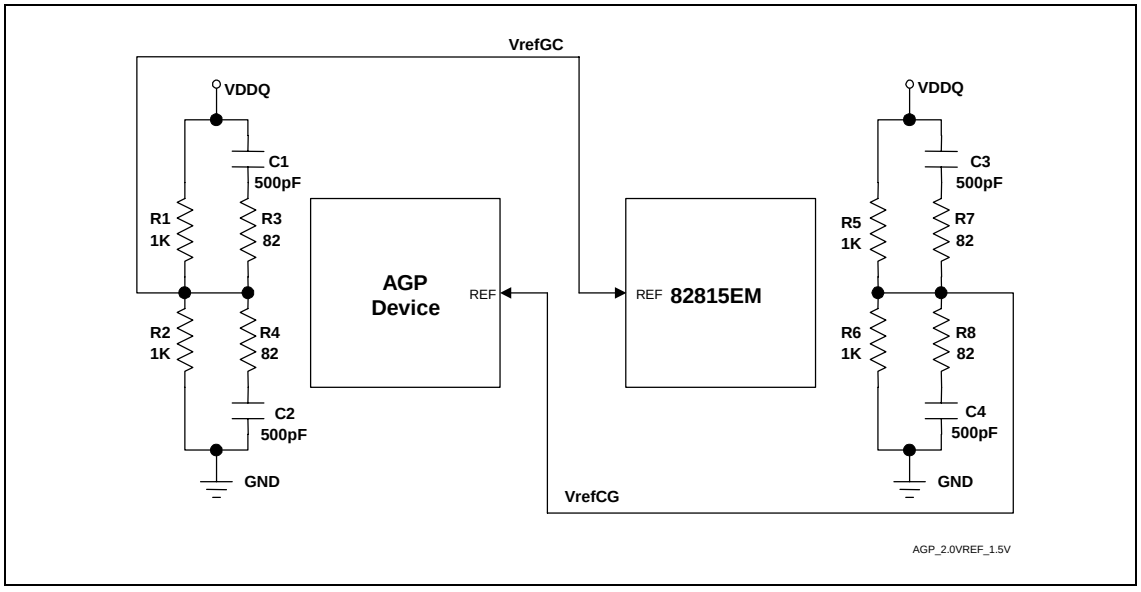


Figure 28: AGP 2.0 Vref Generation and Distribution for 1.5-V Interface



7. Internal Graphics Subsystem Interface

The Intel Digital Video Out (DVO) port is a scaleable, low-voltage interface that ranges from 1.1V to 1.8V. The Intel DVO port interfaces with a discrete TV encoder to enable platform support for TV Out, discrete TMDS transmitter to enable platform support for DVI compliant digital displays, or integrated TV encoder and TMDS transmitter.

The 82815EM DVO port controls the video front-end devices via an I^2C interface, by using the LTVDA and LTVCK pins. I2C is a two-wire communications bus/protocol. The protocol and bus are used to collect EDID from a digital display panel, and to detect and configure registers in the TV encoder or TMDS transmitter chips.

7.1. DVO I2C Interface Considerations

LTVDA and LTVCK should be connected up to the TMDS transmitter, TV encoder, or integrated TMDS transmitter/TV encoder device as required by the specifications for those devices. LTVDA and LTVCK should also be connected to the DVI connector as specified by the DVI specification. On LTVDA and LTVCK, 10 KΩ pull-ups are recommended.

7.2. Leaving the 815EM DVO port Unconnected

If the motherboard does not implement any of the possible video devices with the 815EM DVO port, Intel recommends the following on the motherboard.

- Pull-up LTVDA and LTVCK with 4.7-KΩ resistors at the 82815EM. This will prevent the 82815EM DVO controller from confusing noise on these lines for false I2C cycles.
- Route LTVDATA[11:0] and LTVCLKOUT[1:0] out of BGA to test points for use by automated test equipment (if required). These signals are part of one of the 82815EM XOR chains.

7.3. DVO Interface Signal Groups

The VLINK interface signals include:

- LCD Panel Mode (Signal Name)
  - LTVDATA[11:0]
  - CLKIN[1:0]
  - BLANK#
  - FPVSYNC
  - FPHSYNC
  - LCD_VREF
  - CLKOUT
- TV Out Mode (Signal Name)

  - LTVDATA[11:0]
  - CLKIN[1:0]
  - BLANK#
  - FPVSYNC
  - FPHSYNC
  - LCD_VREF
  - CLKOUT

- FPDM Mode (Signal Name)
  - LTVDATA[11:0]
  - CLKIN[1:0]
  - BLANK#
  - FPVSYNC
  - FPHSYNC
  - LCD_VREF
  - CLKOUT

7.4. DVO Interface Routing Guidelines

7.4.1. Trace Spacing and Trace Length Mismatch Requirements

Route data signals (LTVDATA[11:0]) with a trace width of 5 mils and a trace spacing of 10 mils. These signals can also be routed with a trace width of 5 mils, and a trace spacing of 10 mils for navigation around components or mounting holes. In order to break-out of the 82815EM, the DVO data signals can be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals should be separated to a trace width of 5 mils and a trace spacing of 10 mils within 0.3 inches of the 82815EM component. The maximum trace length for the DVO data signals is 7 inches. These signals should each be matched within ± 0.1 inch of the LTVCLKOUT[1] and LTVCLKOUT[0] signals.

Route the LTVCLKOUT[1:0] signals 5 mils wide and routed 10 mils apart. This signal pair should be a minimum of 10 mils from any adjacent signals. The maximum length for LTVCLKOUT[1:0] is 7 inches and the two signals should be the same length.

7.4.2. Impedance

The motherboard impedance should be controlled to minimize the impact of any mismatch. Intel recommends an impedance of 55 Ω ± 10 %; otherwise, signal integrity requirements may be violated.

7.4.3. Termination

The DVO interface does not require external termination.

7.5. Display Cache Interface

As described earlier, the AGP and display cache interfaces of the Intel® 815EM chipset are multiplexed or shared. In other words, the same component pins (balls) are used for both interfaces, although obviously only one interface can be supported at any given time. As a result, almost all display cache

interface signals are mapped onto the new AGP interface. The Intel® 815EM chipset can be configured in either AGP mode or Graphics mode. In the AGP mode, the interface supports a full AGP 4X interface. In the Graphics mode, the interface becomes a display cache.

Note: In the Graphics mode, the display cache is optional. There do not have to be any SDRAM devices connected to the interface. The only dedicated display cache signals are OCLK and RCLK, which need not connect directly to the SDRAM devices. These are not mapped onto existing AGP signals.

7.5.1. AIMM Card Considerations

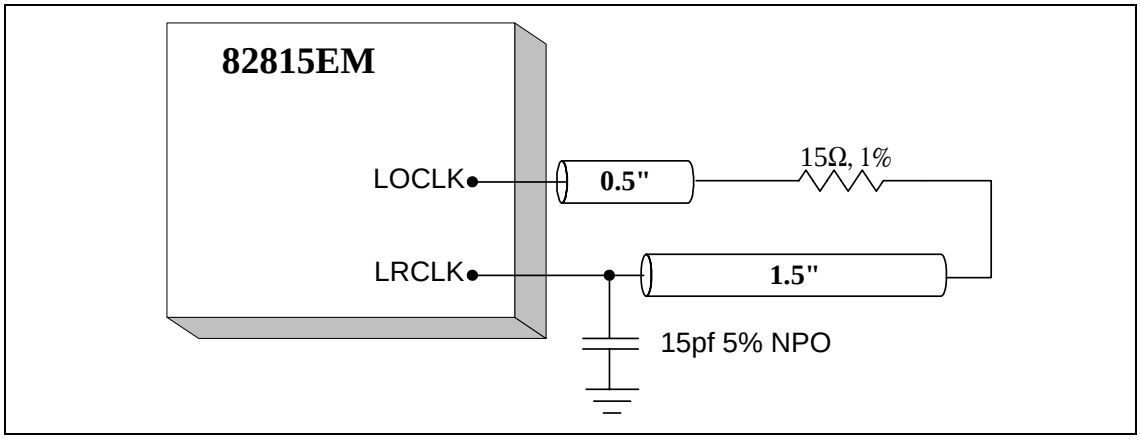
To support the fullest flexibility, the display cache exists on an add-in card (AGP In-Line Memory Module, or AIMM) that complies with the AGP connector form factor. Motherboard manufacturers can choose to populate the AGP slot in an Intel® 815EM chipset-based system with either an AGP graphics card, with an AIMM card to enable the highest-possible internal graphics performance, or with nothing to get the lowest-cost internal graphics solution. Some of the AIMM/Intel® 815EM chipset interfacing implications are as follows. For a complete description of the AIMM card design, refer to the *Intel® 815 Chipset Inline Memory Module External Design Specification* available from Intel.

- A strap is required to determine which frequency to select for display cache operation. This is the L_FSEL pin of the Intel® 815EM chipset's GMCH. The AIMM card will pull this signal up or down as appropriate to communicate to the Intel® 815E chipset the appropriate operating frequency. The Intel® 815EM chipset will sample this pin on the deasserting edge of reset.
- Since current SDRAM technology is always 3.3 V rather than the 1.5-V option also supported by AGP, the AIMM card should set the TYPEDET# signal correctly to indicate that it requires a 3.3-V power supply. Furthermore, the AIMM card should have only the 3.3-V key and not the 1.5-V key, thereby preventing it from being inserted into a 1.5-V-only connector.
- The pad buffers on the chip will be the normal AGP buffers and will work for both interfaces.
- In internal graphics mode, the AGPREF signal, which is required for the AGP mode, should remain functional as a reference voltage for sampling 3.3-V LMD inputs. The voltage level on AGPREF should remain exactly the same as in the AGP mode, as opposed to the VCC/2 used for previous products.
- The AGP control and strobe signals must be terminated as suggested in Section 6.2.3.4 when using the local memory interface.

7.5.2. Display Cache Clocking

The display cache is clocked source-synchronously from a clock generated by the Intel® 815EM chipset's 82815EM. The display cache clocking scheme uses three clock signals. LTCLK clocks the SDRAM devices, is muxed with an AGP signal, and should be routed according to the flexible AGP guidelines. LOCLK and LRCLK clock the input buffers of the Intel® 815EM chipset. LOCLK is an output of the 82815EM and is a buffered copy of LTCLK. LOCLK should be connected to LRCLK at the 82815EM, with a length of PCB trace to create the appropriate clock skew relationship between the Intel® 815EM chipset's clock input (LRCLK) and the SDRAM capacitor clock input(s). The guidelines are illustrated in the following figure:

Figure 29: Intel® 815EM Chipset's Display Cache Input Clocking



7.6. LVDS Interface

The Intel LVDS (Low Voltage Differential Signaling) Transmitter serializer converts up to 24 bits of parallel digital RGB data, (8 bits per RGB), along with up to 4 bits for control (shfclk, hsync, vsync, enable data) into 2, 4 channel serial bit streams, for output by the LVDS Transmitter.

The transmitter is fully differential and utilizes a current mode drive with a high impedance output. The drive current develops a differential swing in the range of 250mv to 450mv across a 100 Ohm termination load.

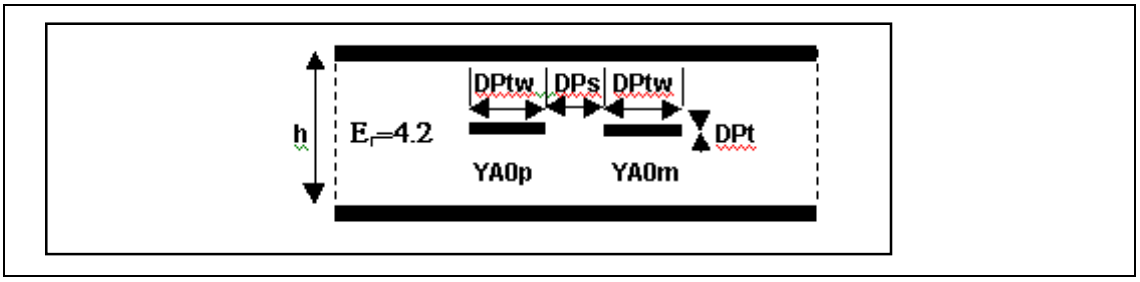
The parallel digital data is serially converted to a 7 bit serial bit stream that is transmitted over the 8 channel LVDS interface at 7x the input clock. The differential output clock channel transmits the output clock at the input clock frequency. While the differential output channels transmit the data at the 7x clock rate (1bit time is 7x the input clock). The 7x serializer will synchronize and regenerate and input clock from 35Mhz to 112Mhz. Typical operation is at 65Mhz (15.4ns), therefore, at a 7x clock rate, 1bit time would be 2.2ns. This corresponding bit time for a 112 Mhz clock rate is a mere 2.2ns. With data cycle times as small as 2.2 ns, propagation delay mismatch is critical, such that intra-channel skew (skew between the inverting and non-inverting output) must be kept minimal.

7.6.1. LVDS Routing Guidelines

The traces associated with the LVDS Transmitter timing domain signals are differential traces terminated across 100 ohms +/- 10 ohms and should be routed as:

- Microstrip or stripline both work well, however, stripline offers better shielding between signals.
- It is necessary to maintain the differential impedance, Zdiff = 100 ohms +/-10 ohms. This can be achieved, for example, by routing the traces as stripline traces as shown in Fig. 30.
- Isolate all other signals from the LVDS signals to prevent coupling from other sources onto the LVDS lines.
- Use controlled impedance traces that match the differential impedance of your transmission medium (i.e. cable) and termination resistor (Note: the transmission medium's Zdiff should be maintained to 100 ohms +/-15%). Run the differential pair trace lines as close together as possible as soon as they leave the IC, not greater that 40 mils (stubs should be <400 mils long). This will help eliminate reflections and ensure noise is coupled as common mode. Plus, noise induced on the differential lines is much more likely to appear as common mode, which is rejected by the receiver.
- Breakout from VCH 5 mils within .03 inches of the package

Figure 30: Stripline Stackup Example



Where:

h = 16 mils DPs = 8 mils

DPtw = 5 mils DPtw = 0.7 mils

$$Z_{diff} = 2*Z_0 (1 - 0.347e^{-2.9(DPs/h)})$$

Note: For Z_0 = 58.6 ohms, Z_{diff} = 101 ohms

7.6.1.1. Trace Length Requirements

The LVDS Transmitter timing domain signals have a maximum trace length of 7.0 inches. This maximum applies to ALL of the LVDS Transmitter signals. In addition to this maximum trace length requirement, these signals must meet the trace spacing and trace length mismatch requirements in Section 1.2.1.1 and 1.2.1.2.

7.6.1.2. Trace Space (Ts) Requirements

Figure 30 is an example stackup with differential pair spacing that provides sufficient common mode coupling to reject common mode noise. A practice that needs to be maintained to ensure common mode rejection of common mode noise, and maintain the differential impedance of 100 ohms +/- 10 ohms which matches the termination resistor and therefore minimizes noises from reflections. Where Figure 30 is not applicable, and given that Zdiff must equal R(term)=100 Ohms and differential pair spacing (DPs) must be close for common mode noise rejection, follow the rules below.

- Differential Pair Spacing(DPs) is less than Differential pair trace width (DPtw)
- DPs is less than the distance between the power or ground plane pair (h)

7.6.1.3. Trace Width Requirements

Trace width (Tw):

$$Tw > Ts/2$$

Spacing between Diff pairs (Tdps):

$$Tdps \geq 2Tw$$

7.6.1.4. Trace Characteristic Impedence

The side by side differential pair shown in Figure 30 is designed by targeting the uncoupled trace impedance to be 5 or 10 ohms greater than one half of the differential impedance. For Zdiff = 100 ohms, Z0= 50 +(5 or 10) or 55 to 60 Ohms. Adjust the spacing between the traces as described in 1.2.1.1, and compute the Zdiff. If the trace to trace spacing is as close as the manufacturing rule allows, adjust the trace width and re-compute the Zdiff.

Table 26: LVDS Transmitter Routing Summary

Signal	Maximum Length	Trace Spacing (5 mil traces)	Length Mismatch
7X Timing Domain	7.0 in	8 mils	+/- 0.1in

Note: The differential pairs must be separated from other signals by at least 2*Tdps or 2*Tw.

7.6.1.5. Termination

The LVDS Interface is terminated in 100 ohms only at the input to the receiver.

7.6.2. Simulation Assumptions/Estimates

The simulation methodology described below is for a post-layout design validation. It is provided for OEMs that have a post-layout simulation tool, such as ICX (Mentor Graphics), ISIS (Viewlogic), Cadence(SigXp), etc.

While layout guidelines have been developed based on a comprehensive pre-layout analysis of the technologies and simulations, OEMs are still encouraged to simulate their designs to make sure design timing and signal integrity requirements are met.

7.6.2.1. Assumptions/Definitions/Specifications

The LVDS timing interface is source synchronous to the extent that data and clock are both simultaneously transmitted down the LVDS channel. However, the data sampling at the receiver is a function of an accurate strobe generated from the LVDS clock. The first strobe is generated from the output clock from the transmitter and the remaining 6(total of 7 strobes) are generated from each previous strobe. Each strobe at the receiver samples one data bit ($^1/_f$*7). Jitter from the transmitter is passed on to the receiver and decreases the available margin (sampling window) to the receiver. The receiver has inherit margin (setup and hold time). The transmitter also introduces clock to data skew (output skew), the variation of transmitter pulse position from the ideal position. The routing skew(due to pair to pair length mismatch + intra-channel trace length mismatch), cable skew, and any ISI). These five items will determine the available LVDS system skew margin(skm) as follows

$$T_{skm} = T_{rskm} - T_{xcsk}$$

Where $\mathbf{T_{skm}}$ is the remaining system skew timing margin. $\mathbf{T_{rskm}}$ a function of LVDS receiver skew margin and the transmitter output skew margin, or, the allowable skew margin. $\mathbf{T_{xcsk}}$ is the transmit channel skew margin:

1. routing skew (Trsk)---worst case from simulations: 90ps
2. cable skew (Tcsk)-----using the Foxconn Microcoax: 0ps
3. ISI----------measured from simulations: 0ps
4. clock jitter (Tclkj)------from the LVDS spec: 225ps

Example: Using the National Semiconductor 65Mhz receiver and the allowable skew calculated from Table 3.

$$\mathbf{T_{skm}} = \mathbf{T_{rskm}} - 315ps$$

Note:

1. The LVDS physical interface is a point-to-point topology using differential signaling, where the single ended voltage swings nominally from 1.0v(Vol) to 1.4v(Voh), for a nominal 400mv differential output (Vod).
2. The baseline performance level for the LVDS transmitter uses a 65 MHz(1/T is 15.4 ns) clock, where the data rate is 7xT or 475Mb/s, and 1 bit time is 2.2ns
3. The flight time skew simulations simulate all parameters that could cause a skew between two signals, including motherboard trace capacitance due to long trace length, effective capacitance in the buffer models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and ISI induced skews. The simulated ISI contribution is approximately 0 ps.
4. Routing channel to channel skew maximum is 0.095ns.
5. Maximum cycle to cycle jitter is 225ps.
6. Cable skew is approximately 0ps due to use of a coax based cable model in the simulation model.

7.6.2.1.1.Simulation Model

A model for simulation purposes is shown below.

Figure 31: LVDS Simulations Model

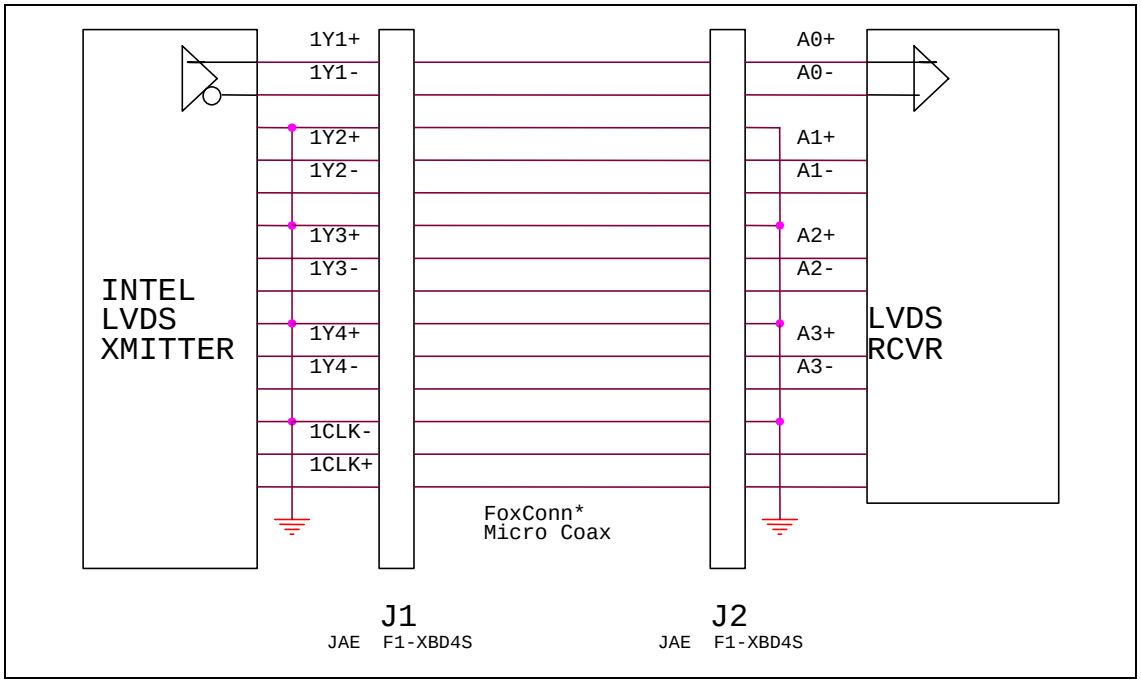
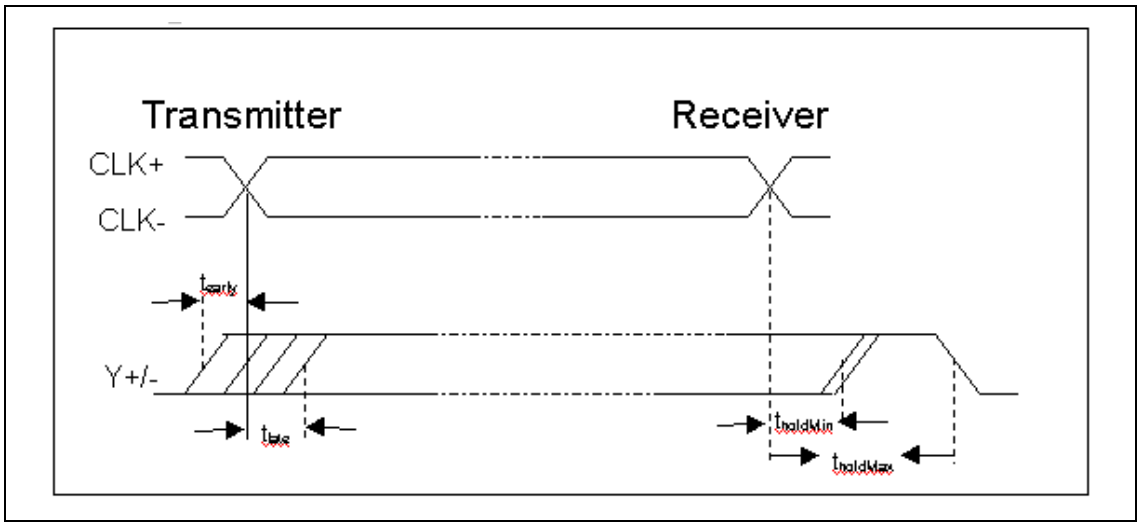


Figure 32: LVDS Driver- Receiver Waveforms Relationship Specification



The timing budget from the LVDS simulations is listed in the following table.

Table 27: Allowable Interconnect Skew Calcuation

Component	Skew Element	Symbol	Units
Driver	Data Valid before Strobe	Tearly	TBD
	Data Valid after Strobe	Tlate	TBD
Interconnect	**Allowable Skew**		0.4 nS
Receiver	Minimum hold time	TholdMin	0.7 nS
	Maximum hold time	TholdMax	1.4 nS

All numbers in the table are from the LVDS specification documents, and the National Semiconductor data sheets.

7.6.3. Post-layout Validation Methodology

The simulation methodology outlined here is for post-layout validation of the LVDS transmitter only. It does not apply to pre-layout analysis of the design. Although the methodology was developed using the ICX simulation tool, it was in general the goal to make the methodology applicable to other post layout tools as much as possible.

7.6.3.1. Define Simulation Cases Explicitly

Simulation cases must be defined first, considering the following parameters:

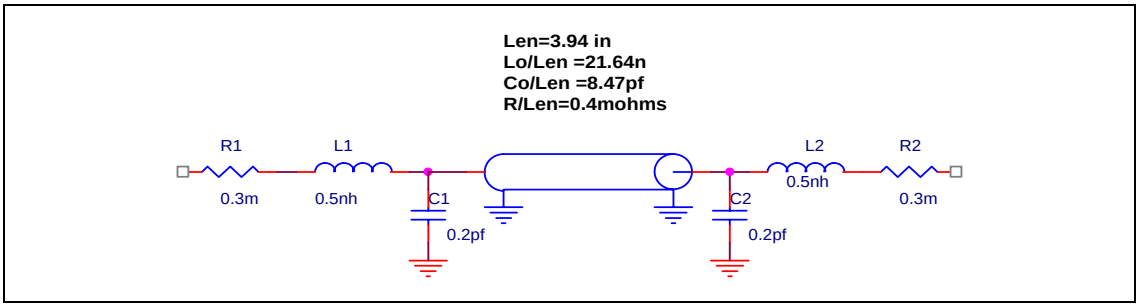
- Velocity of signals , Er: Low Er:4.0 – High Er:4.4, nominal Er:4.1
- Characteristic impedance of boards:
- Common mode Z0 = 58.6ohms +/- 15%
- Differential Z0 = 101ohms +/- 15%
- Weak, typical and strong output and slow, typical and fast input buffers

Prepare models and boards as follows:

Table 28: LVDS Interface Simulation Boards

Boards	MVCHx	LVDS Transmitter PCB	Interconnect Connector/Cable	LVDS Receiver Board
Board1	Typical Buffer IBIS	nominal Er(4.1) and nominal Zdiff(101.2 ohms	Low to 0 ps skew. Connector/cable model (Length =4.0 inches.) Note 1	Typ Receiver, nominal Board(Er=4.1) Note 2
Board2	Weak Buffer IBIS	High Er and Low Zo	Low to 0 ps skew. Connector/cable model (Length =4.0 inches.) Note 1	Typ Receiver, nominal Board(Er=4.1) Note 2
Board3	Weak Buffer IBIS	High Er and High Zo	Low to 0 ps skew. Connector/cable model (Length =4.0 inches.) Note 1	Typ Receiver, nominal Board(Er=4.1) Note 2
Board4	Strong Buffer IBIS	Low Er and High Zo	Low to 0 ps skew. Connector/cable model (Length =4.0 inches.) Note 1	Typ Receiver, nominal Board(Er=4.1) Note 2
Board5	Strong Buffer IBIS	Low Er and Low Zo	Low to 0 ps skew. Connector/cable model (Length =4.0 inches.) Note 1	Typ Receiver, nominal Board(Er=4.1) Note 2

Note1: The Interconnect Connector/Cable Model is defined as follows. This is an uncoupled model.



Note2: The Receiver board model is based on lab measurements(typ.) from several LVDS based flat panel displays.

Simulations are as follows:

- Output only simulations with respect to the LVDS Transmitter.
  - Enable coupled EVEN/ODD crosstalk (Board 1).
  - Use ISI patterns (eg: 0111101… at 455Mhz, and 1111110 at 455Mhz), ISI measured from simulations was found to be approximately equal to 0 ps,
  - For each board's specific Er, change dielectric thickness to meet Zo specified.
- Run simulations on each board for the differential clock lines and also the differential data lines.
- Measure flight times of all signals from Vmeas on the driver to Vmeas on the receiver.
- Also make sure signal quality requirements are met.
- Calculate skews on a differential channel to channel basis.
- Report violations to improve routing.

7.7. CRT Routing

Intel recommends a 20-mil spacing between any video (RGB) route and any other routes. Match the RGB routes. The termination resistor can be placed anywhere along the video route from the RAMDAC output to the VGA connector. Each DAC output is doubly terminated with a 75 Ω resistance from the DAC output to the board ground. Place the reference resistor in close proximity to the IREF pin. Place LC filter components and high -frequency de-coupling capacitors as close to the power pins as possible. Intel recommends that the LC filter be designed for a cut-off frequency of 100 kHz.

7.8. DVOr Interface

The VCH DVOr port is a low-voltage, 1.8-V interface. This Intel DVOr port interfaces with a discrete TV encoder to enable platform support for TV Out, discrete TMDS transmitter to enable platform support for DVI compliant digital displays, or integrated TV encoder and TMDS transmitter.

7.8.1. Signal Groups

Input signals: DVOr Interface Signal Groups

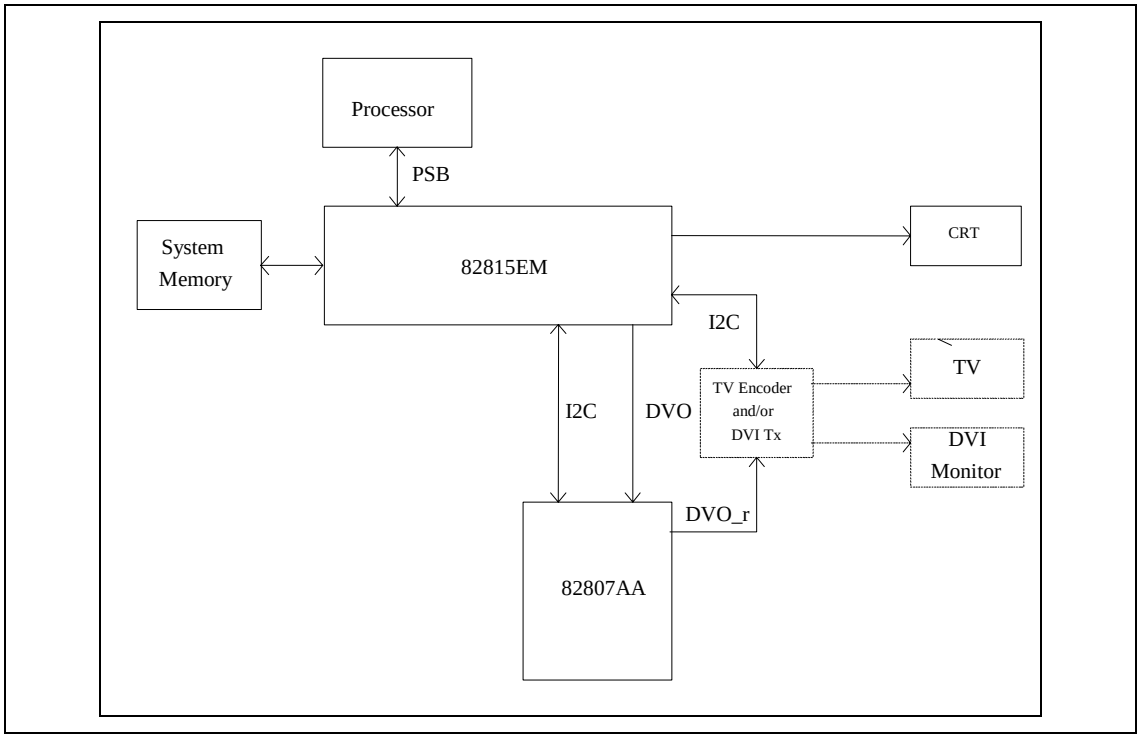
Output Data Signals: DVOrHSYNC, DVOrVSYNC, DVOrBLANK#

DVOrDATA[11:0]

Output Strobe Signals: DVOrCLKOUT[1:0]

7.8.2. DVOr Interface Routing Guidelines for Discrete TV Encoder

Figure 33: DVO Interface



7.8.2.1. Trace Spacing and Trace Length Mismatch

Route data signals (DVOrDATA[11:0]) with a trace width of 5 mils and a trace spacing of 10 mils. These signals can be routed with a trace width of 5 mils and a trace spacing of 10 mils for navigation around components or mounting holes. In order to break-out of the VCH, the DVOr data signals can be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals should be separated to a trace width of 5 mils and a trace spacing of 10 mils within 0.3 inches of the VCH component. The maximum trace length for the DVOr data signals is 7 inches. These signals should each be matched within ± 0.2 inches of the DVOrCLKOUT[1] and DVOrCLKOUT[0] signals.

Route the DVOrCLKOUT[1:0] signals 5 mils wide and routed 10 mils apart. This signal pair should be a minimum of 10 mils from any adjacent signals. The maximum length for DVOrCLKOUT[1:0] is 7

inches and the two signals should be the same length. The maximum frequency simulated for discrete TV Out is 50 MHz.

7.8.3. DVOr Interface Routing Guidelines for Discrete TMDS Transmitter or Integrated TMDS Transmitter/TV Encoder

7.8.3.1. Trace Spacing and Trace Length Mismatch Requirements

Route data signals (DVOrDATA[11:0]) with a trace width of 5 mils and a trace spacing of 10 mils. These signals can be routed with a trace width of 5 mils and a trace spacing of 10 mils for navigation around components or mounting holes. In order to break-out of the VCH, the DVO data signals can be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals should be separated to a trace width of 5 mils and a trace spacing of 10 mils within 0.3 inches of the VCH component. The maximum trace length for the DVOr data signals is 7 inches. These signals should each be matched within ± 0.1 inches of the DVOrCLKOUT[1] and DVOrCLKOUT[0] signals.

Route the DVOrCLKOUT[1:0] signals 5 mils wide and routed 10 mils apart. This signal pair should be a minimum of 10 mils from any adjacent signals. The maximum length for DVOrCLKOUT[1:0] is 7 inches and the two signals should be the same length. The maximum frequency is 112 MHz.

7.8.4. Impedance

The motherboard impedance should be controlled to minimize the impact of any mismatch. An impedance of 55 Ω $\pm$ 10 % is strongly recommended; otherwise, signal integrity requirements may be violated.

7.8.5. Termination

The DVOr interface does not require external termination.

7.9. Assumptions, Definitions, and Specifications

The source synchronous solution space consists of all designs in which the flight time mismatch between a strobe and its associated data is less than the total allowable skew. See Equation 5 below.

Equation 5.

$$T_{skew} = T_{flightdata} - T_{flightstrobe}$$

Where $T_{flightdata}$ and $T_{flightstrobe}$ are the driver-pad-to-receiver-pad flight times of the data and the strobe respectively.

- The DVO physical interface is a point-to-point topology using 1.8V signaling. The DVOrCLKOUT[0:1] Maximum frequency is 112 MHz.
- The flight time skew simulations simulate all parameters that could cause a skew between two signals, including motherboard and add-in card line lengths, effective capacitance in the buffer

models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and ISI induced skews.

7.9.1. Design Margin Calculations

Setup Margin = Tvb - Tsu

Hold Margin = Tva - Th

The setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides. However, note that available margins are not absolute values. Any skew DUT to routing and loading differences, and coupling differences in the parallel traces, and any effects of SSO (ISI, ground bounce, etc.) should be accounted for in the timing budget as they will reduce the total available margin for the design. Therefore, Intel strongly recommends that OEMs simulate their designs. For the values of Tvb, Tsu, Tva, and Th, refer to the product specification.

7.9.2. Simulation Method

A model for simulation purposes is shown in Figure 34.

Figure 34: DVO Simulations Model

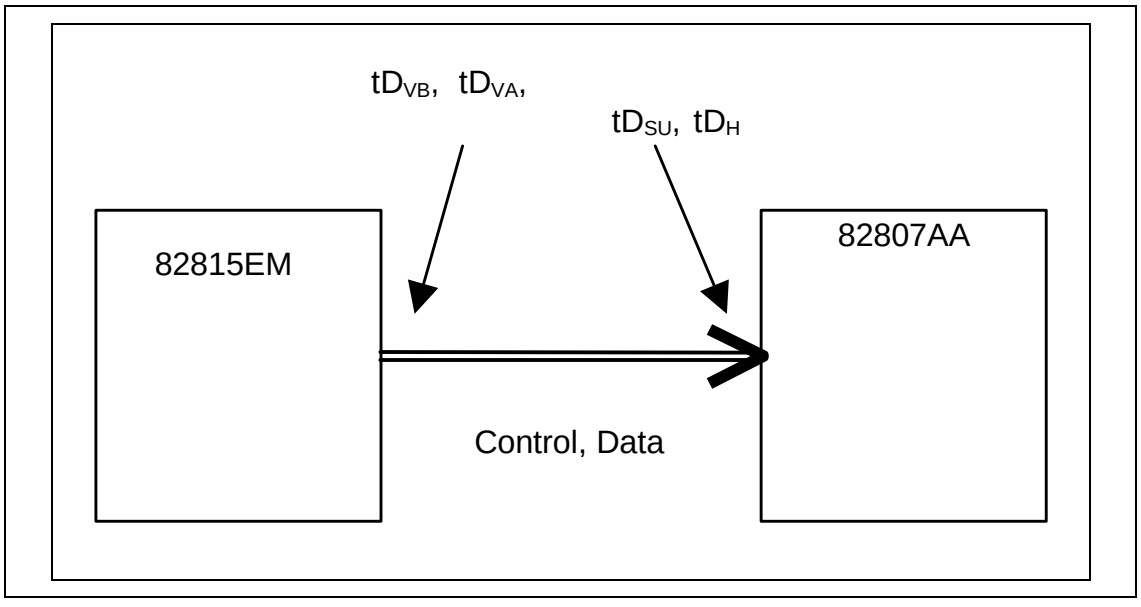
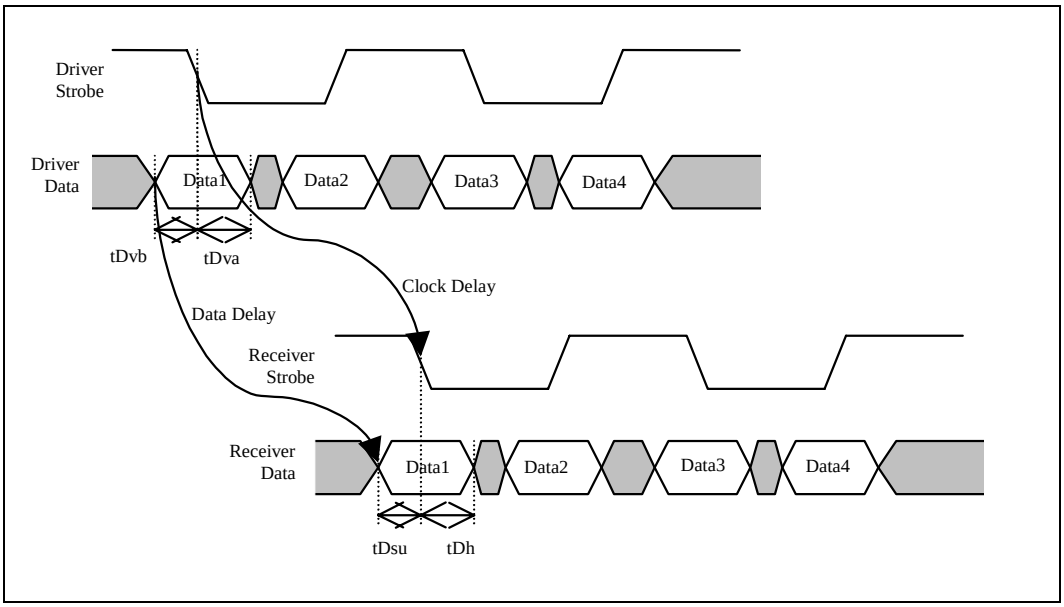


Figure 35: Driver-Receiver Waveforms Relationship Specification



The setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides.

Warning: The available margins are not absolute values. Any skew due to routing and loading differences, any coupling differences in the parallel traces, and any effects of SSO (ISI, ground bounce, etc.) should be accounted for in the timing budget as they will reduce the total available margin for the design.

Table 29: Allowable Interconnect Skew Calculation

Component	Skew Element	Symbol	Value	Units
Driver	Data Valid before Strobe	tDvb	-750	psec
	Data Valid after Strobe	tDva	1000	psec
Receiver	Data Setup to Strobe	tDsu	250	psec
	Data Hold from Strobe	tDh	500	psec

All numbers in Table 29 above are from the Hub Interface specification documents, which are applicable for this interface.

7.10. Post-layout Validation Methodology

The simulation methodology in this section is for post-layout validation of the DVO only, and does not apply to pre-layout analysis of the design. Although the methodology was developed using the ICX simulation tool, it was in general the goal to make the methodology applicable to other post layout tools as much as possible.

7.10.1. Define Simulation Cases Explicitly

Simulation cases must be defined first, considering the following parameters:

- Velocity of signals , Er: Low Er:4.0 – High Er:4.4
- Characteristic impedance of boards: Zo: 55Ω ± 10%
- Weak, typical and strong output and slow, typical and fast input buffers

Prepare the models and boards as shown below.

Table 30: DVO Interface Simulation Boards

Boards	82815EM	PCB	DVO Device
Board1	Weak Buffer IBIS	High Er and Low Zo	Slow Buffer IBIS
Board2	Weak Buffer IBIS	High Er and High Zo	Slow Buffer IBIS
Board3	Strong Buffer IBIS	Low Er and High Zo	Fast Buffer IBIS
Board4	Strong Buffer IBIS	Low Er and Low Zo	Fast Buffer IBIS
Board5	Strong Buffer IBIS	High Er and High Zo	Fast Buffer IBIS

Perform both READ and WRITE simulations.

1. Enable coupled EVEN/ODD crosstalk (Board 5).
2. Patterns with buffers switching high to low or low to high (0000 to FFFF or FFFF to 0000) or 0000 to 1110 or 1111 to 0001 or 1110 to 0001 or 0001 to 1110.
3. Use ISI patterns, otherwise, allow ~ 150 ps for ISI in timing spreadsheet.
4. For each board's specific Er, change dielectric thickness to meet Zo specified.
   - Run simulations on each board for strobe lines and also the data lines.
   - Measure flight times of all signals from Vmeas on the driver to Vmeas on the receiver.
   - Also make sure signal quality requirements are met.
   - Calculate skews between the strobe and data signals.
   - Report violations to improve routing.

8. Hub Interface

8.1. Description of Interface

The 82815EM ball assignment and 82801BAM ball assignment have been optimized to simplify hub routing. Intel recommends that the Hub Interface signals be routed directly from the 82815EM to the 82801BAM on an inner signal layer (they do not need to be run through vias).

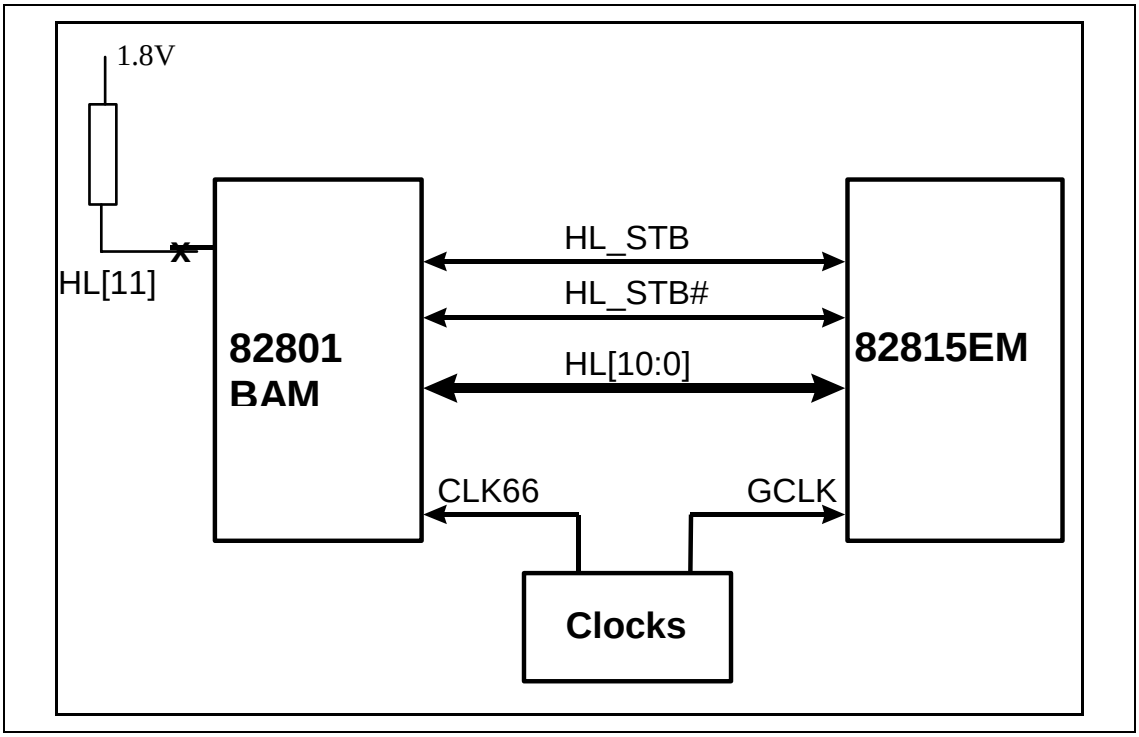
The Hub Interface is broken into two signal groups: data signals and strobe signals (See Figure 36.) The data signals consist of HL[10:0], and the strobe signals consist of HL_STB and HL_STB#.

Warning: HL_STB/HL_STB# is a differential strobe pair.

8.2. Routing Guidelines

Each signal must be routed so that it meets the guidelines documented for the signal group to which it belongs.

Figure 36: Hub Interface Signal Routing



8.2.1. Data Signals

Hub Interface data signals should be routed *5 on 10 mils*. These signals can also be routed *5 on 10 mils* for navigation around components or mounting holes. In order to breakout of the 82815EM BGA and the 82801BAM eBGA, the Hub Interface data signals can be routed *5 on 5* mils. The signals must be separated to *5 on 10 mils* within 30 mils of the BGA package.

The maximum trace length for the Hub Interface data signals is 7 inches. These signals must each be matched within ± 0.1 inches of the HL_STB and HL_STB# signals.

8.2.2. Strobe Signals

Due to their differential nature, the Hub Interface strobe signals should be 5 mils wide and routed 10 mils apart. This strobe pair should be a minimum of 10 mils from any adjacent signals. The maximum length for the strobe signals is 7 inches and the two strobes must be the same length ± 0.1 inches. Additionally, the trace length for each data signal must be matched to the trace length of the strobes with ± 0.1 inches.

With the exception of HL[11] on the 82801BAM (which should be pulled up to 1.8V through a 10-kΩ resistor), there are no pull-ups or pull-downs required on the Hub Interface.

8.2.2.1. Routing Summary

- Max Trace Length: 7 inches
- Strobe Signals Traces:
  - 5 mils wide, 10 mils apart from each other, 10 mils apart from other signals
  - Routed as differential pair
  - Match length within ± 0.1 inches
- Data Signal Traces:
  - 5 mils wide, 10 mils apart from each other
  - Breakout from 82815EM or 82801BAM 10 mils within 0.03 inches of the package
  - Match length within ± 0.1 inches

8.3. Simulation Assumptions and Estimates

The simulation methodology described below is for a post-layout design validation and is provided for OEMs who have a post-layout simulation tool, such as ICX* (Mentor Graphics) and ISIS* (Viewlogic).

While layout guidelines have been developed based on a comprehensive pre-layout analysis of the technologies and simulations, OEMs are still encouraged to simulate their designs to make sure design timing and signal integrity requirements are met.

8.3.1. Assumptions, Definitions, and Specifications

The following list provides the simulation assumptions, definitions, and specifications.

- The source synchronous solution space consists of all designs in which the flight time mismatch between a strobe and its associated data is less than the total allowable skew. See Equation 6 below.

Equation 6.

$$T_{skew} = T_{flightdata} - T_{flightstrobe}$$

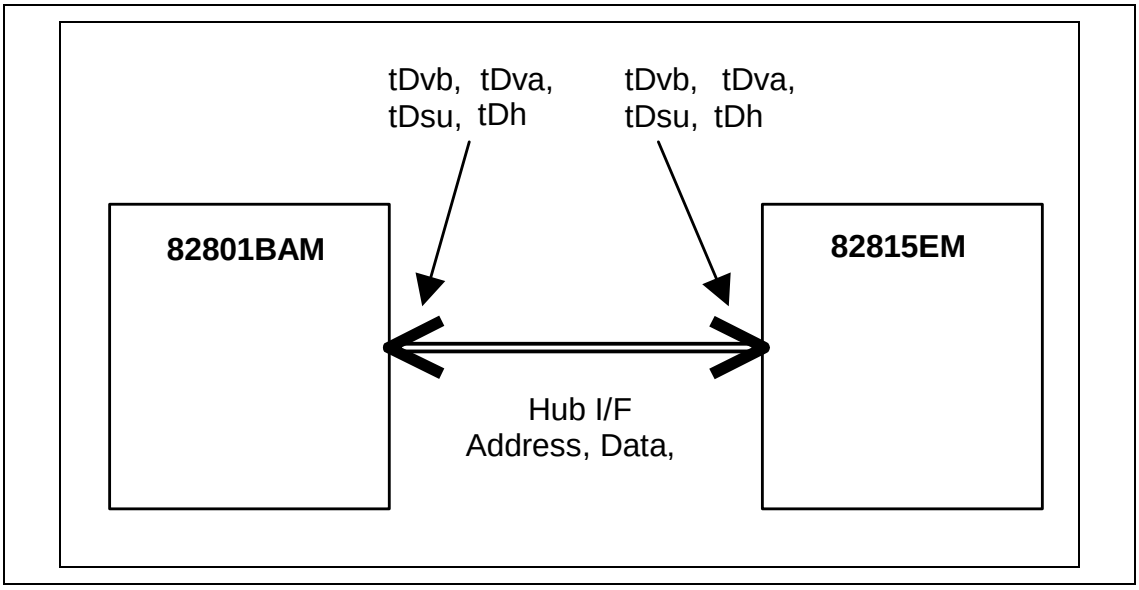
Where $T_{flightdata}$ and $T_{flightstrobe}$ are the driver-pad-to-receiver-pad flight times of the data and the strobe respectively.

- The Hub physical interface is a point-to-point topology using 1.5-V signaling. The baseline performance level for Hub Interface uses a 66-MHz clock to provide a peak bandwidth of 266 MB/s.
- The flight time skew simulations simulate all parameters that could cause a skew between two signals, including motherboard and add-in card line lengths, effective capacitance in the buffer models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and ISI induced skews.

8.3.1.1. Simulation Model

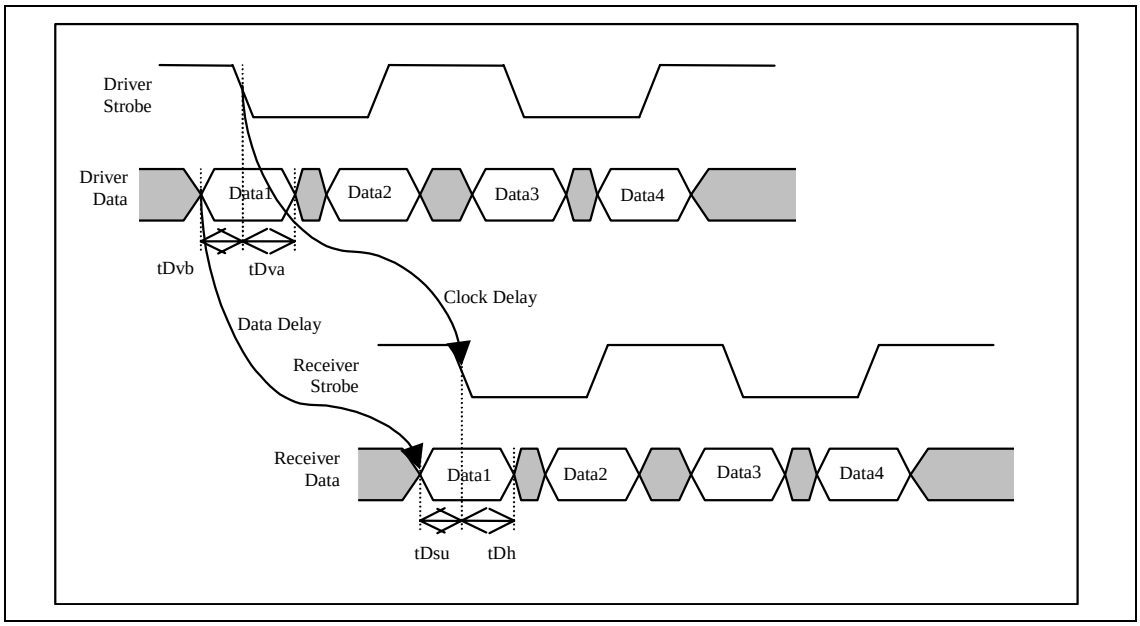
A model for simulation purposes is shown in Figure 37.

Figure 37: Hub Interface Simulations Model



8.3.1.2. Timing

Figure 38: Driver- Receiver Waveforms Relationship Specification



As shown in Figure 38 the setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides.

Note: The available margins are not absolute values. Any skew due to routing and loading differences, any coupling differences in the parallel traces, and any effects of SSO (ISI, ground bounce, etc.) should be accounted for in the timing budget as they will reduce the total available margin for the design.

As an example here, the timing budget that was used for mobile simulations is listed Table 31.

Table 31: Allowable Interconnect Skew Calculation

Component	Skew Element	Symbol	Setup	Hold	Units
Driver	Data Valid before Strobe	tDvb	800		ps
	Data Valid after Strobe	tDva		1100	ps
Interconnect	Allowable Skew		550	600	ps
Receiver	Data Setup to Strobe	tDsu	350		ps
	Data Hold from Strobe	tDh		500	ps

All numbers in the table are from the 82815EM specification documents. As seen in the table, total amount of skew is only 1000 ps. This skew includes allocations for SSO, crosstalk, and routing and loading introduced skew.

8.4. Post-layout Validation Methodology

The simulation methodology outlined here is for post-layout validation of the Hub Interface only. It does not apply to pre-layout analysis of the design. Although the methodology was developed using the ICX simulation tool, it was in general the goal to make the methodology applicable to other post layout tools as much as possible.

8.4.1. Define Simulation Cases Explicitly

Simulation cases must be defined first. Considering the following parameters.

- Velocity of signals, Er: Low Er:4.0 – High Er:4.4
- Characteristic impedance of boards: Zo: 55Ω ± 10%
- Weak, typical, and strong output and slow, typical, and fast input buffers

Perform the following steps to prepare the models and boards.

Table 32: Hub Interface Simulation Boards

Boards	82815EM	PCB	82801BAM
Board1	Weak Buffer IBIS	High Er and Low Zo	Slow Buffer IBIS
Board2	Weak Buffer IBIS	High Er and High Zo	Slow Buffer IBIS
Board3	Strong Buffer IBIS	Low Er and High Zo	Fast Buffer IBIS
Board4	Strong Buffer IBIS	Low Er and Low Zo	Fast Buffer IBIS
Board5	Strong Buffer IBIS	High Er and High Zo	Fast Buffer IBIS

Perform both READ and WRITE simulations.

- Enable coupled EVEN/ODD crosstalk (Board 5).
- Patterns with buffers switching high to low or low to high (0000 to FFFF or FFFF to 0000) or 0000 to 1110 or 1111 to 0001 or 1110 to 0001 or 0001 to 1110.
- Use ISI patterns (e.g., 000001 at 266 MHz). Otherwise allow ~150 ps for ISI in the timing spreadsheet.
- For each board's specific Er, change the dielectric thickness to meet Zo specified.
  - Run simulations on each board for strobe lines and also the data lines.
  - Measure flight times of all signals from Vmeas on the driver to Vmeas on the receiver.
  - Also make sure signal quality requirements are met.
  - Calculate skews between the strobe and data signals.
  - Report violations to improve routing.

8.5. Hub Interface Power Requirements

8.5.1. HREF Generation and Distribution

HREF is the Hub Interface reference voltage and is 0.5 * 1.8V = 0.9V ± 2%. HREF can be generated using a single HREF divider or locally generated dividers (as shown in Figure 39 and

Figure 40). Each divider consists of a DC element and an AC element. The resistors in the DC element should be equal in value and rated at a 1-% tolerance (to maintain 2% tolerance on 0.9V). The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The recommended range for resistor value is from minimum 100Ω to maximum 1 kΩ (300Ω shown in example). The resistors in the AC element of the resistor divider should be no greater and 80Ω and the capacitors should be 500 pF. Additionally, the reference voltage should be bypassed to ground at each component with a 0.1-uF capacitor.

The single HREF divider should not be located more than 4 inches away from either 815EM or 82801BAM. If the single HREF divider will be located more than 4 inches away, then the locally generated Hub Interface reference voltage dividers should be used.

Figure 39: Single Hub Interface Reference Divider Circuit

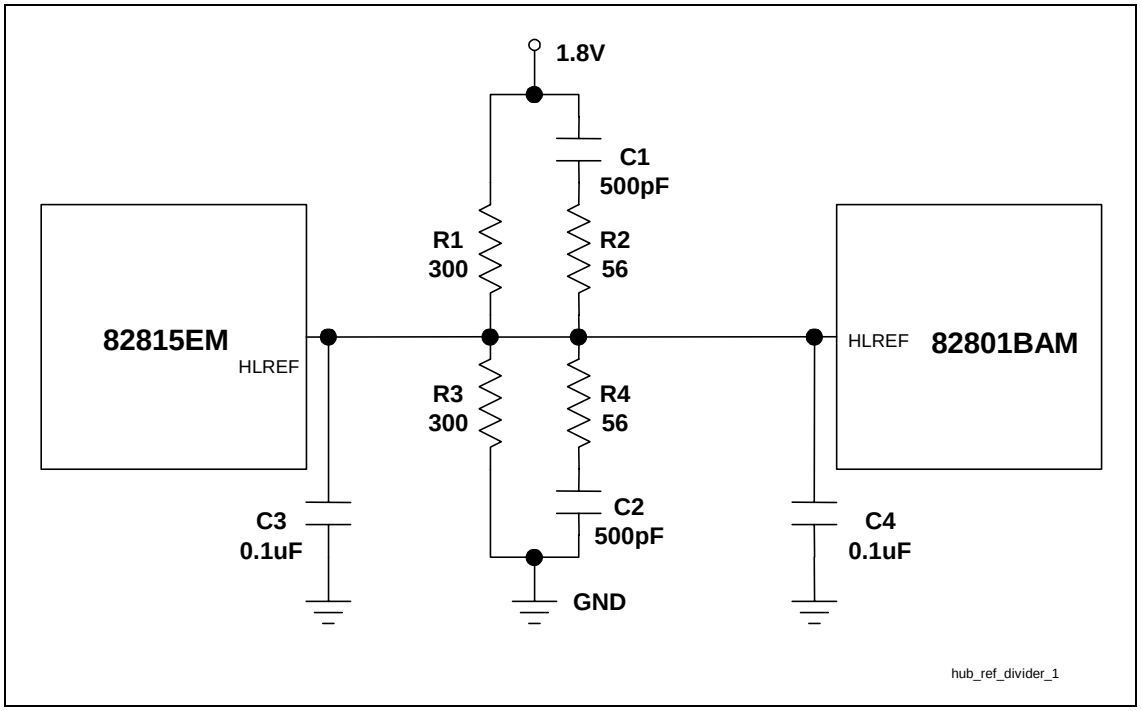
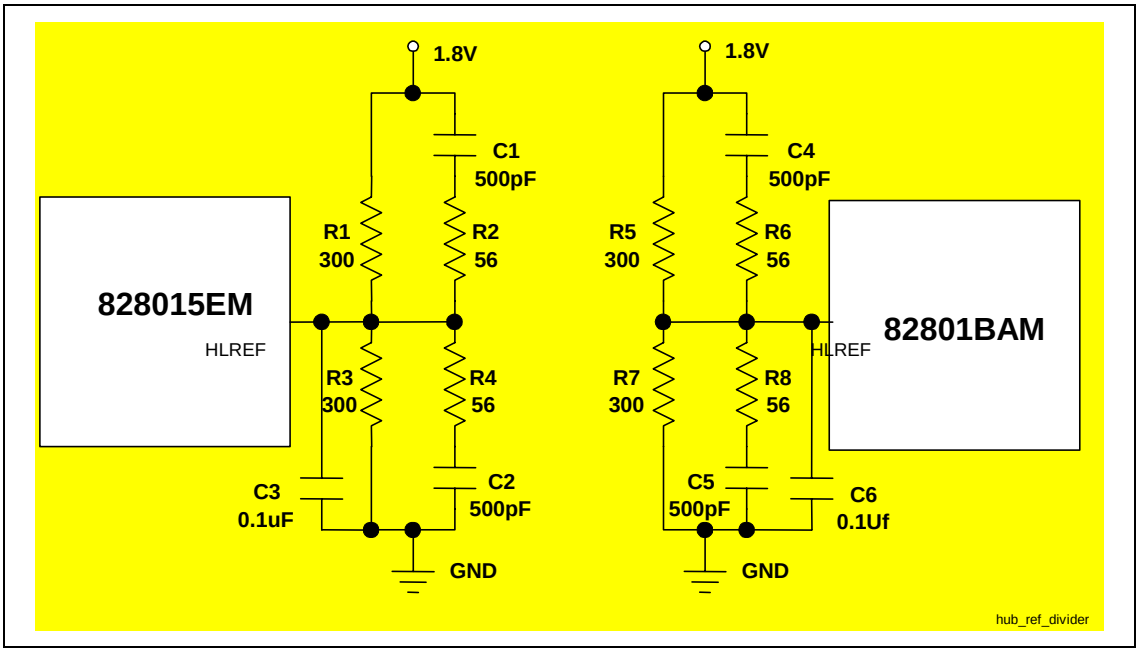


Figure 40: Locally Generated Hub Interface Reference Divider Circuits



8.5.2. Compensation

The 82801BAM Hub Interface supports resistive buffer compensation (RCOMP). Pin HLCOMP is used by the 82801BAM to adjust buffer characteristics. Refer to the Intel® 815EM Chipset: 82815EM Graphics and Memory Controller Hub (GMCH2-M) Datasheet, Document Reference Number: 290687 for details on compensation. The design guidelines are below.

- **RCOMP:** Tie the COMP pin to a 36.5Ω 1% pull-up resistor (to 1.8V) via a 10-mil wide, very short (≈0.5-inch) trace.
- The 815EM also has a hub compensation pin. This signal (HLCOMP) can be routed using the RCOMP method described for the 82801BAM.

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9. 82801BAM Design Considerations

9.1. IDE Interface

9.1.1. ATA66

This section contains guidelines for connecting and routing the 82801BAM IDE interface as shown in Figure 41 and Figure 42. The 82801BAM has two independent IDE channels. This section provides guidelines for design, including component and resistor placement and signal termination for both IDE channels. The 82801BAM has integrated the 33-Ω series resistors that have been typically required on the IDE data signals running to the two ATA connectors.

The IDE interface can be routed with 5-mil traces on 5-mil spaces, and must be less than 12 inches long (from 82801BAM to IDE connector). Additionally, all IDE signals must be length matched to within ± 0.5 inches.

Note: Primary and secondary channels can be length-matched independently.

9.1.1.1. Grounding

Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

9.1.1.2. 82801BAM Placement

The 82801BAM should be placed as close as possible to the ATA connector(s).

- 22-Ω to 47-Ω series resistors are required on SDDACK#, PDDACK#, IRQ14, IRQ15, and RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- A 10-kΩ pull-down resistor is required on PDD7 and SDD7 (as required by the ATA-4 specification).
- A 5.6-kΩ pull-down resistor is required on PDDREQ# and SDDREQ# (as required by the ATA-4 specification).
- A 4.7-kΩ pull-up resistor is required on PIORDY and SIORDY

Figure 41: Resistor Placement for Primary IDE Connectors

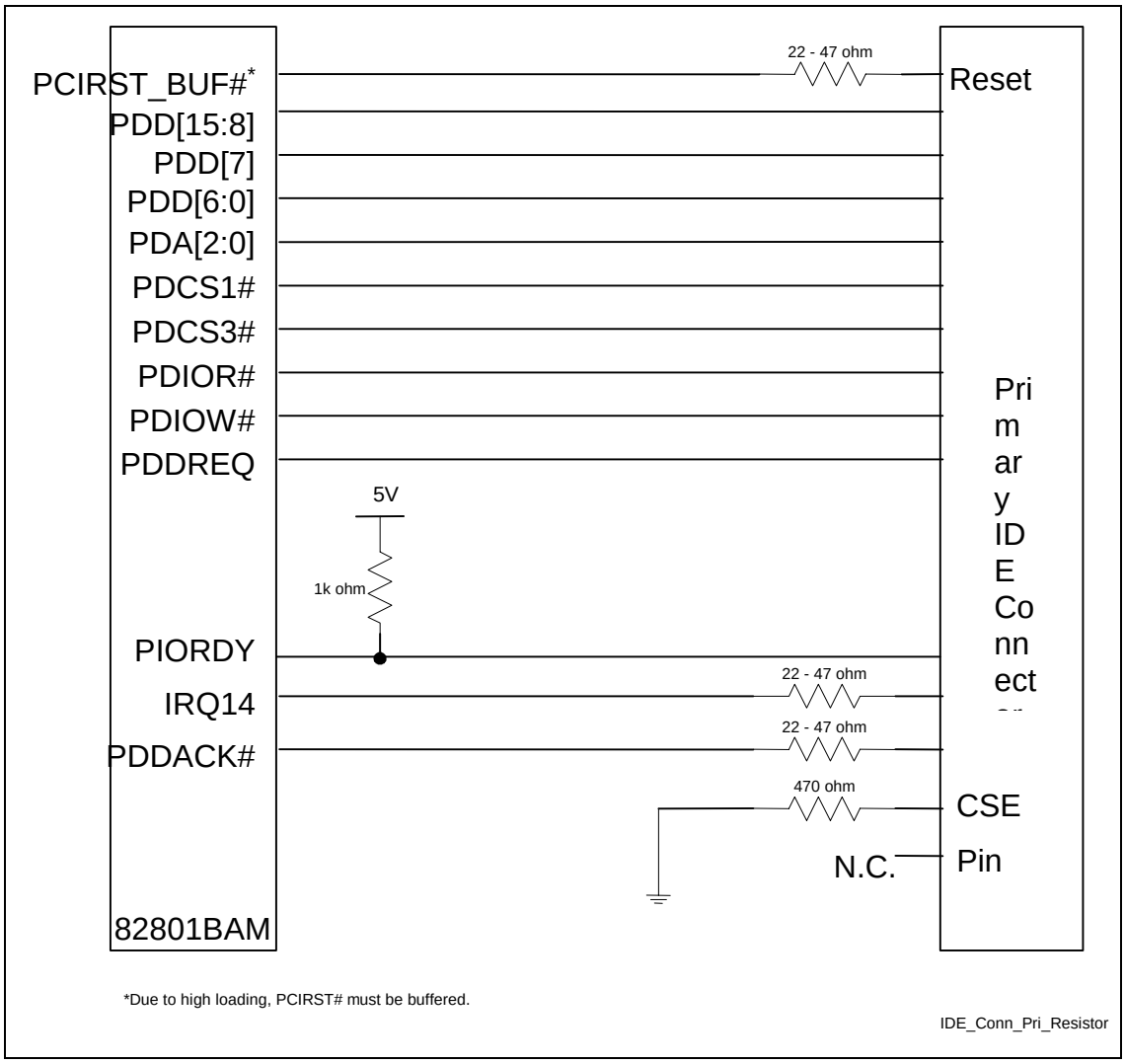
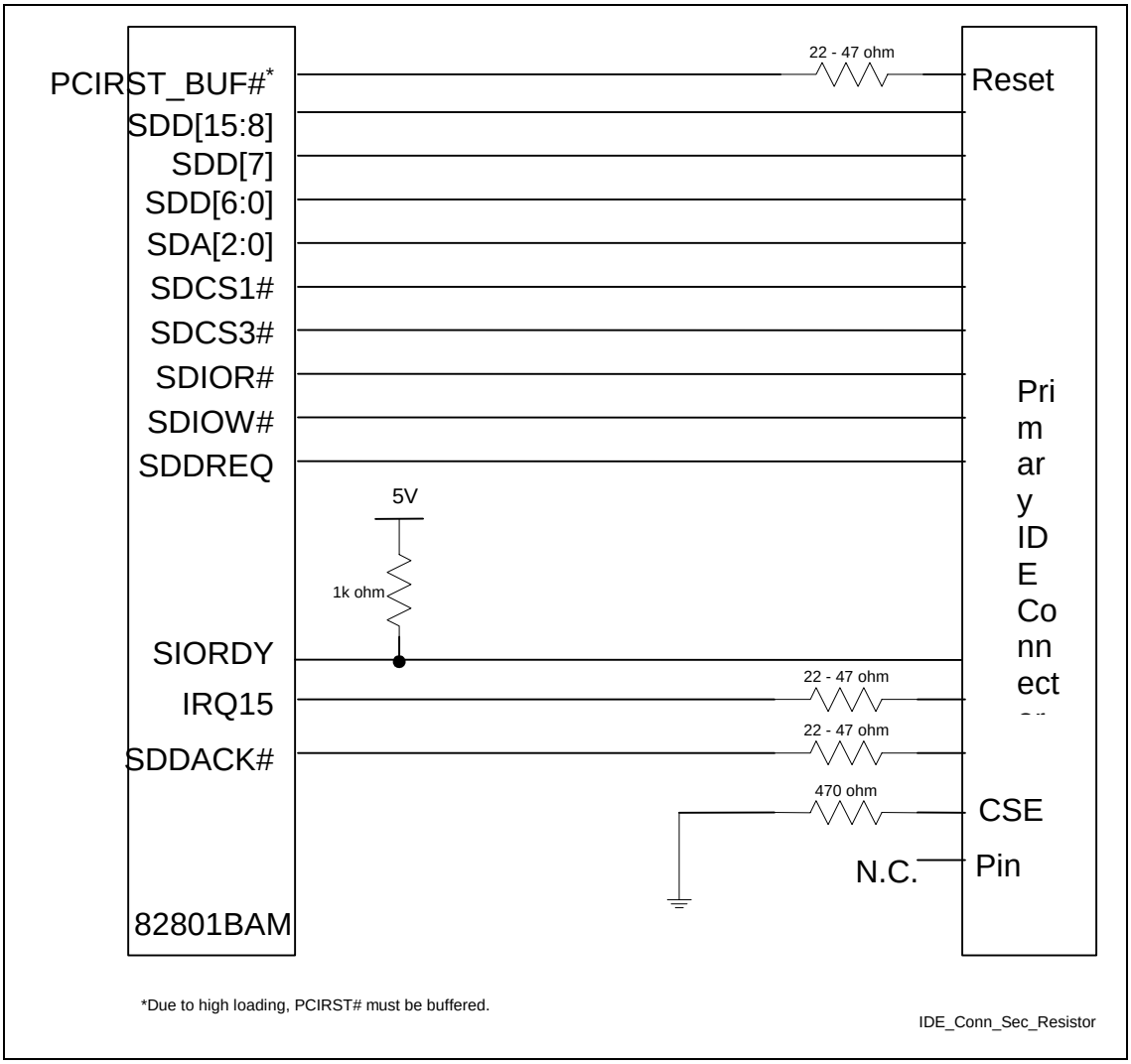


Figure 42: Resistor Placement for Secondary IDE Connectors

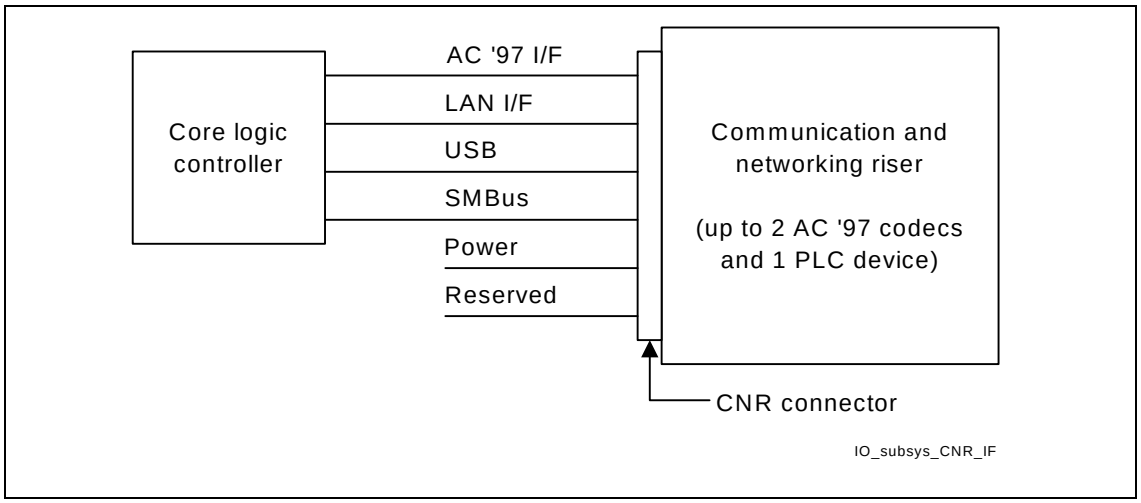


9.2. CNR Interface

The *Communication and Networking Riser (CNR) Specification* defines a hardware scalable OEM motherboard riser and interface. CNR is a desktop specification. A similar concept can be used on mobile platforms, but there is no actual mobile specification. This interface supports multi-channel audio, V.90 analog modem, phone-line based networking, and 10/100 Ethernet based networking. The CNR specification defines the interface that should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot. Unlike the AMR, the system designer will not sacrifice a PCI slot if they decide not to include a CNR in a particular build.

Figure 43 indicates the interface for the CNR connector. The Platform LAN Connection (PLC) can either be a 82562EH* or 82562ET* component. Refer to the *Communication and Networking Riser CNR specification* for additional information.

Figure 43: CNR Interface



9.3. USB Interface

The following are general guidelines for the USB interface:

- **Unused** USB ports should be terminated with 15-K pulldown resistors on both P+/P- data lines. Series resistors of 15Ω should be placed as close as possible to the 82801BAM (<1 inch). These series resistors are for source termination of the reflected signal.
- Caps of 47-pF must be placed as close to the 82801BAM as possible, and on the 82801BAM side of the series resistors on the USB data lines (P0+/-, P1+/-). These caps are for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15-K ±5% pulldown resistors should be placed on the USB side of the series resistors on the USB data lines (P0+/-, P1+/-), and are REQUIRED for signal termination by USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0+/-, P1+/- signals should be 45Ω (to ground) for each USB signal P+ or P-. Trace width should be determined based on the specific stackup. The impedance is 90Ω between the differential signal pairs P+ and P- to match the 90-Ω USB twisted pair cable impedance. Note that the twisted pair characteristic impedance of 90Ω is the series impedance of both wires, resulting in an individual wire presenting a 45-Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as “critical signals” (for example, hand routing is preferred). The P+/P- signal pair must be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI.

Figure 44 illustrates the recommended USB schematic.

Figure 44: USB Data Signals

9.3.1. Recommended USB Trace Characteristics

- Impedance Z0 = 45.4Ω
- Line Delay = 160.2 ps
- Capacitance = 3.5 pF
- Inductance = 7.3 nH
- Res at 20° C = 53.9 mΩ

9.4. AC '97

The 82801BAM implements an AC'97 2.1 compliant digital controller as in Figure 45 and Figure 46. Any codec attached to the 82801BAM AC-link must be AC'97 2.1 compliant as well. Please contact your codec IHV for information on 2.1 compliant products. The *AC'97 2.1 Specification* can be found online at http://developer.intel.com/pc-supp/platform/ac97/index.htm.

The 82801BAM supports the combinations of codecs, which are listed in Table 33.

Table 33: Codec Combinations

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio (AC)	Modem (MC)

Primary	Secondary
Audio/Modem (AMC)	None

As shown in Figure 46, the 82801BAM does not support two codecs of the same type on the link. For example, if an AMC is on the link, it must be the only codec. If an AC is on the link, another AC cannot be present.

For increased part placement flexibility, there are two routing methods for the AC'97 interface: the *tee* topology and the *daisy-chain* topology. The AC'97 interface can be routed using 5-mil traces with 5-mil space between the traces.

Figure 45: T Topology for AC'97 Trace Length Requirements

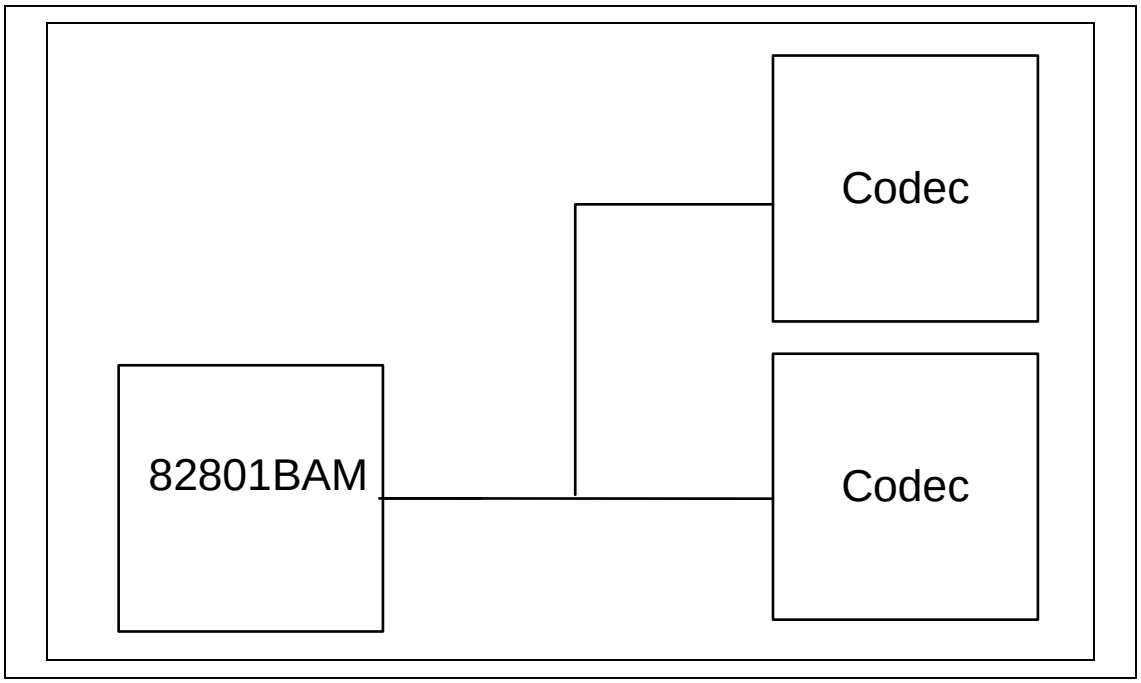
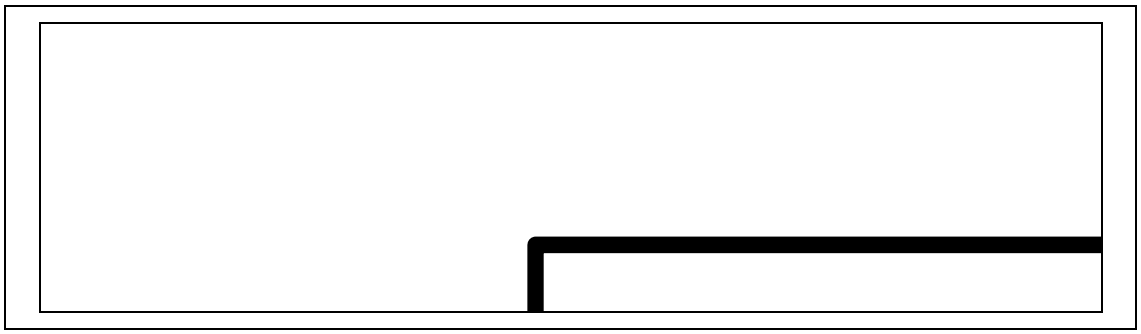


Figure 46: Daisy Chain Topology for AC'97 Trace Length Requirements



Clocking is provided from the primary codec on the link via BITCLK and is derived from a 24.576-MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288-MHz clock driven by the primary codec to the digital controller (82801BAM) and any other codec present. That clock is used as the timebase for latching and driving data.

The 82801BAM supports wake-on-ring from S1-S4 via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

If there is not a codec that is attached to the link, internal pull-downs will prevent the inputs from floating; therefore, external resistors are not required.

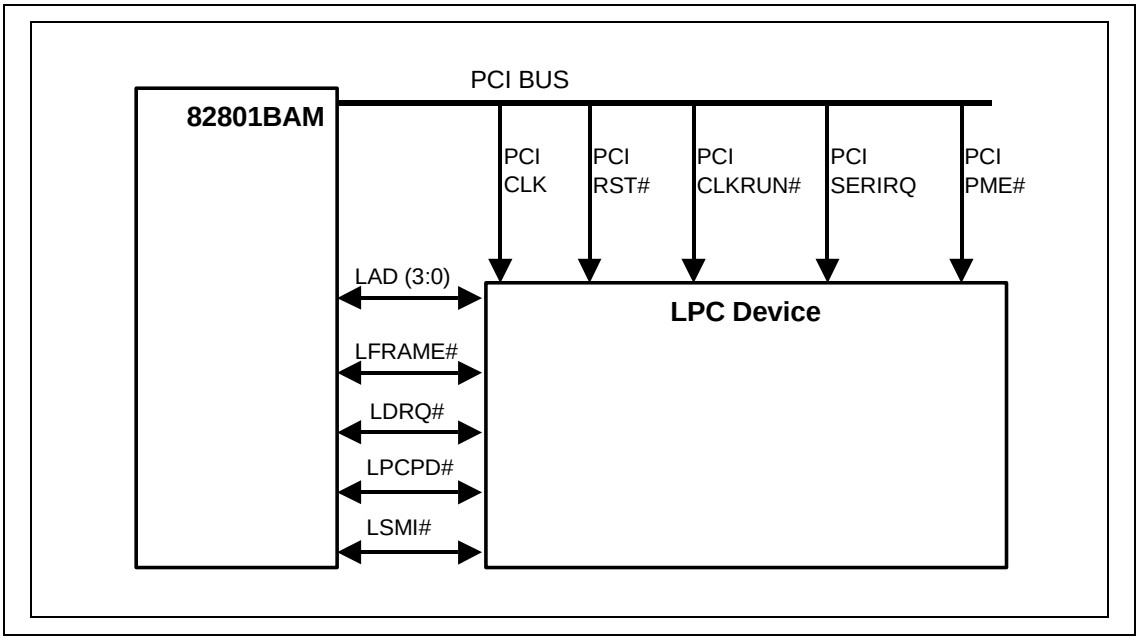
9.5. LPC Interface

The systems based on 82815EM and 82801BAM will require the super I/O component conforming to LPC specifications. Migration to the LPC component allows low-cost super I/O designs. The LPC super I/O component requires the same features as the traditional super I/O components. In addition, a game port may be included, as the AC '97 interface does not support a game port. Consult your super I/O vendor for a complete list of devices offered and features supported.

The 82801BAM implements an LPC I/F per the LPC specification. The LPC specifications are available at, http://developer.intel.com/design/chipsets/industry/lpc_100.pdf.

The LPC interface to the 82801BAM is shown in Figure 47. 82801BAM implements all the optional signals listed in the *LPC I/F Specifications*.

Figure 47: LPC Interface



The 82801BAM also supports two separate bus masters on the LPC I/F.

9.6. PCI Interface

The 82801BAM provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high-performance data streaming when the 82801BAM is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, please refer to the *PCI Local Bus Specification Revision 2.2*.

The 82801BAM supports six PCI Bus masters (excluding the 82801BAM), by providing six REQ#/GNT# pairs. In addition, the 82801BAM supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

9.7. SMBus

The 82801BAM provides an SMBus host controller, including an SMBus Master Interface. The SMBus host controller provides a mechanism for the processor to communicate with SMBus peripherals (slaves). The 82801BAM is also capable of operating in a mode that can communicate with I^2C-compatible devices.

9.8. ISA

Implementations that require ISA support can benefit from the enhancements of the Intel 82801BAM, while “ISA-less” designs are not burdened with the complexity and cost of the ISA subsystem. For implementation of an ISA design, contact external suppliers.

9.9. IOAPIC

Mobile systems not using the IOAPIC should follow these recommendations.

When on the 82801BAM:

- Tie PICCLK directly to ground.
- Tie PICD0, PICD1 to ground through a 10-kΩ resistor.

When on the processor:

- PICCLK must be connected from the clock generator to the PICCLK pin on the processor.
- Tie PICD0 to 1.5V through 150-Ω resistors.
- Tie PICD1 to 1.5V through 150-Ω resistors.

9.10. Networking

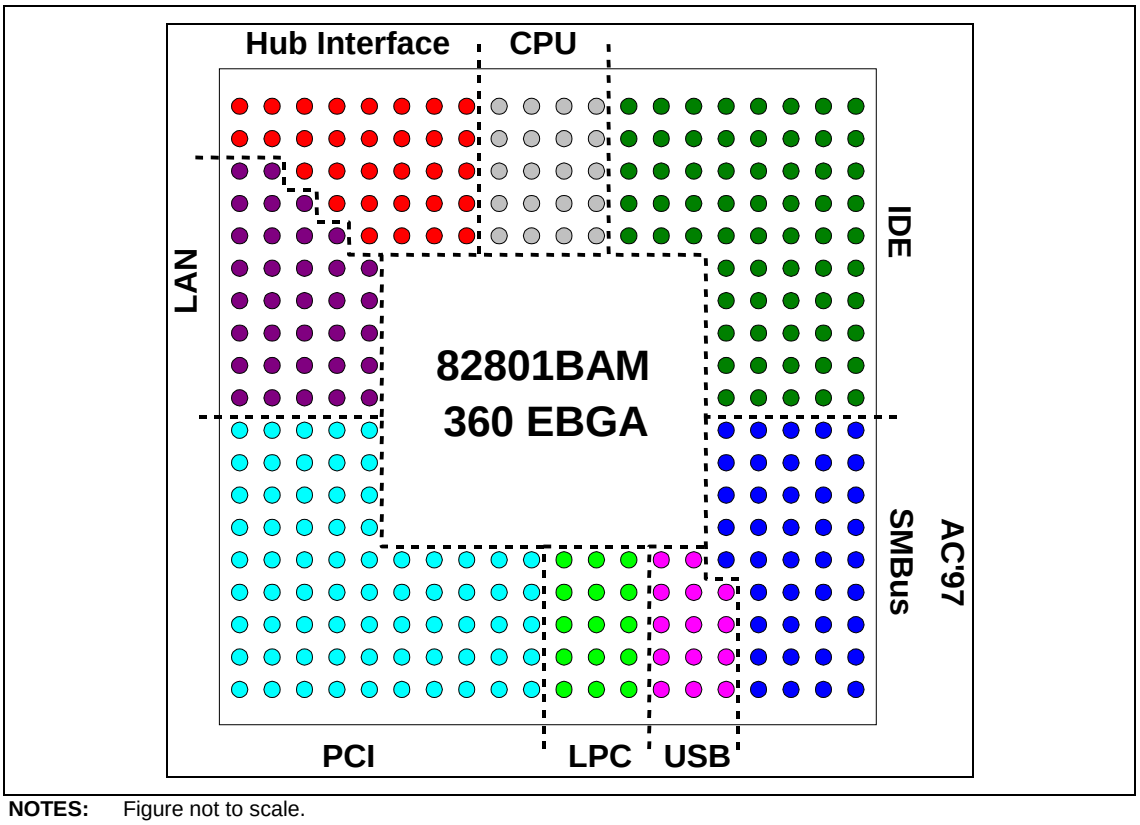
Refer to section 10.1 for LAN information.

9.11. Routing and Layout Considerations

9.11.1. Component Quadrant Layout

The quadrant layouts shown in Figure 48 are approximate, and the exact ball assignments should be used to conduct routing analysis. These quadrant layouts are designed for use during component placement.

Figure 48: 82801BAM Quadrant Layout (Top View)



NOTES: Figure not to scale.

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10. System Design Considerations

10.1. Network – LAN

The 82801BAM provides several options for integrated LAN capability. The platform supports several components depending on the target market. See Table 34 below.

Table 34. LAN Connect Components

LAN Connect Component	Connection	Features
82562EM	Advanced 10/100 Ethernet	AOL* & Ethernet 10/100 Connection
82562ET	10/100 Ethernet	Ethernet 10/100 Connection
82562EH	1Mb HomePNA* LAN	1Mb HomePNA connection

Intel developed a dual footprint for the 82562ET and 82562EH to minimize the required number of board builds. A single layout with the specified dual footprint will allow the installation of the appropriate LAN connect component to meet the market need. Design guidelines are provided for each required interface and connection. Refer to Table 35 for the corresponding section of the design guide.

Figure 49: 82801BAM /LAN Connect Section

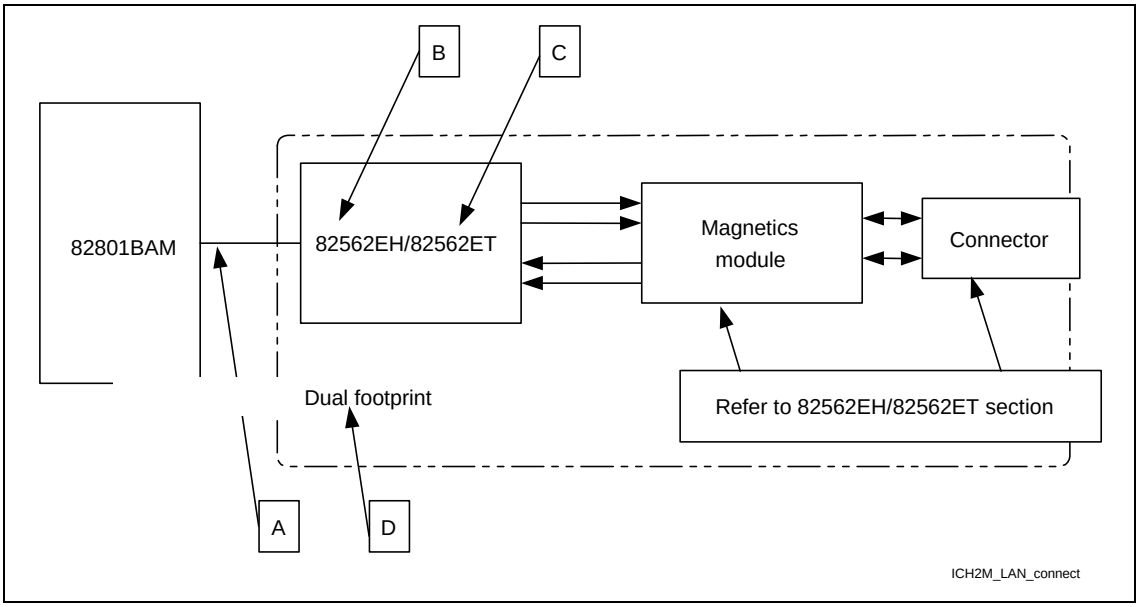


Table 35: LAN Design Guide Section Reference

Layout Section	Figure 49 Reference	Design Guide Section
82801BAM – LAN Interconnect	A	10.1.1 82801BAM – LAN Interconnect Guidelines

Layout Section	Figure 49 Reference	Design Guide Section
General Routing Guidelines	B,C,D	10.1.2 General LAN Routing Guidelines and Considerations
82562EH	B	10.1.3 82562EH Home/PNA* Guidelines
82562ET /82562EM	C	10.1.4 82562ET/82562EM and 82562ET/82562 EH Guidelines
Dual Layout Footprint	D	10.1.4.7 82562ET/82562EH Dual Footprint Guidelines

10.1.1. 82801BAM – LAN Interconnect Guidelines

This section contains guidelines for designing motherboards and riser cards to comply with a LAN connect. The system designer must ensure that the system meets the specified timings through simulations or other techniques. Special care must be given to matching the **LAN_CLK** traces to other signal traces. The following are guidelines for the 82801BAM to LAN component interface.

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

The interface supports both the 82562EH and 82562ET/82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by both components. Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected when 82562EH is installed. The AC characteristics for this interface are found in the Dual footprint guidelines of the Intel® 815EM Chipset: 82815EM Graphics and Memory Controller Hub (GMCH2-M) Datasheet; Document Reference Number: 290687.

10.1.1.1. Bus Topologies

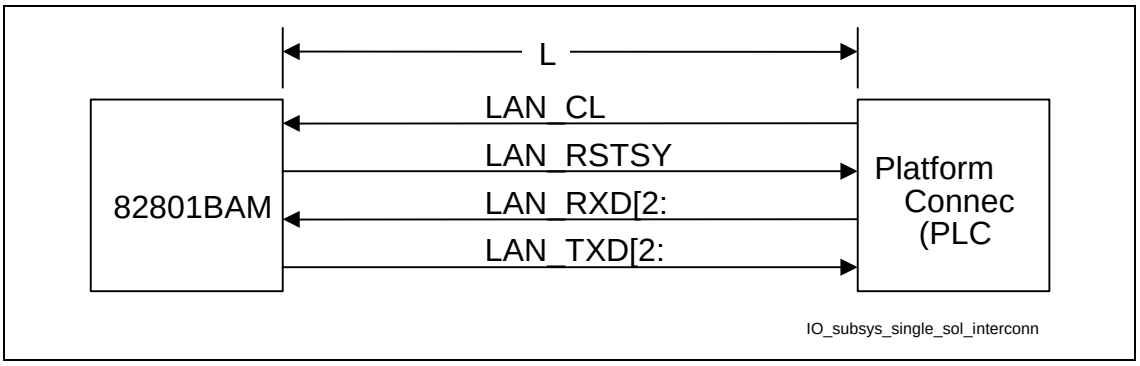
The LAN Connect interface can be configured in several topologies and a few are provided below.

- Direct point-to-point connection between the 82801BAM and the LAN component
- Dual Footprint (See Section 10.1.4.7)
- LOM/CNR Implementation

10.1.1.2. Point-to-point Interconnect

The following guidelines are for a single solution motherboard. Either 82562EH, 82562ET, or CNR are installed.

Figure 50: Single Solution Interconnect



The following are length requirements for Figure 50.

- 82562EH: L = 1.5 inches to 7.0 inches (Signal Lines LAN_RXD[2:1] and LAN_TXD[2:1] not connected)
- 82562ET: L = 0.5 inches to 4.5 inches
- CNR: L = 0.5 inches to 4 inches

10.1.1.3. LOM/CNR Interconnect

The following guidelines allow for an all inclusive motherboard solution. This layout combines LOM, dual footprint, and the CNR solutions. The resistor pack ensures that either a CNR option or a LAN on a motherboard option can be implemented at one time. A model of this is found in Figure 51. The recommended trace routing lengths are shown below.

Figure 51: LOM/CNR Interconnect

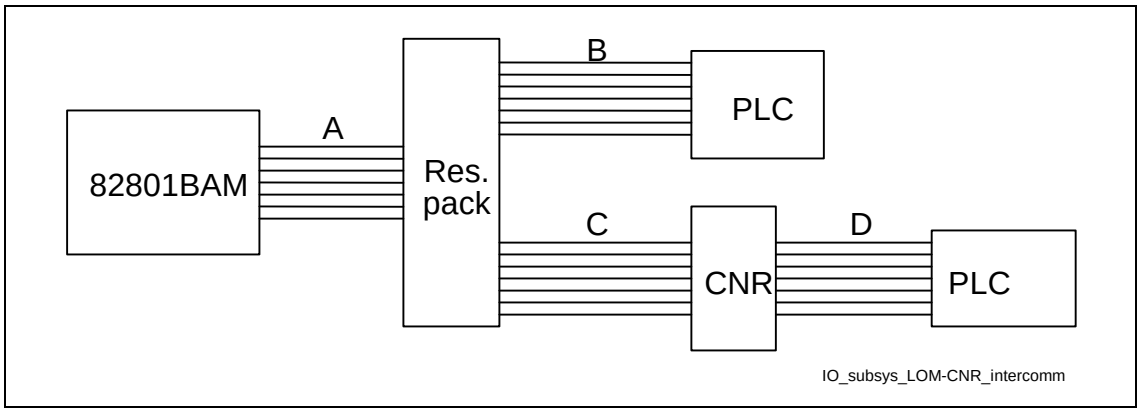


Table 36 provides the length requirements for Figure 51.

Table 36. Length Requirements

Configuration	A (inches)	B (inches)	C (inches)	D (inches)
82562EH	1.5 to 2.0	2.5 to 5.0		
82562EH Card	0.5 to 3.5		0.5 to (4.0 – A)	1.0 to 3.0
82562ET	0.5 to 2.0	0.5 to 2.5		
82562ET Card	0.5 to (4.5 – D)		0.5 to (4.0 – A)	1.0 to 3.0

Additional guidelines for this configuration are provided below.

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0Ω or 22Ω.
- LAN on motherboard PLC can be a dual footprint configuration.

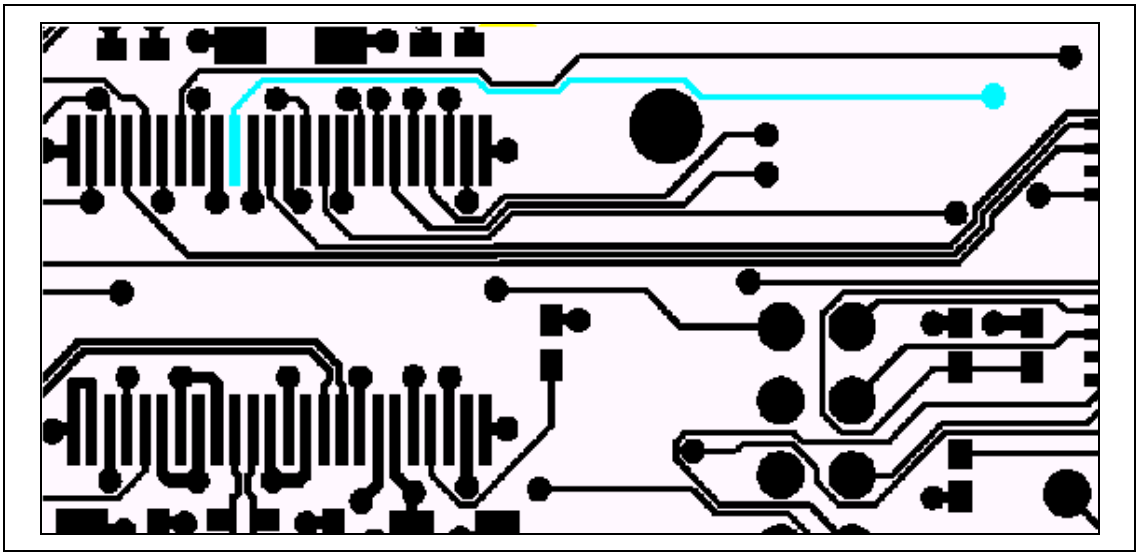
10.1.1.4. Signal Routing and Layout

LAN Connect signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed.

- Intel recommends that the designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk.

- On the motherboard, the length of each data trace is either equal in length to the **LAN_CLK** trace or up to 0.5 inches shorter than the **LAN_CLK** trace. (**LAN_CLK** should always be the longest motherboard trace in each group.)

Figure 52: LAN_CLK Routing Example



10.1.1.5. Crosstalk Considerations

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter.

10.1.1.6. Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. Intel recommends an impedance of 55Ω ±10%; otherwise, signal integrity requirements may be violated.

10.1.1.7. Line Termination

Line termination mechanisms are not specified for the LAN Connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 33.0-Ω series resistor can be installed at the driver side of the interface should there be concerns about overshoot and undershoot.

Note: The receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

10.1.2. General LAN Routing Guidelines and Considerations

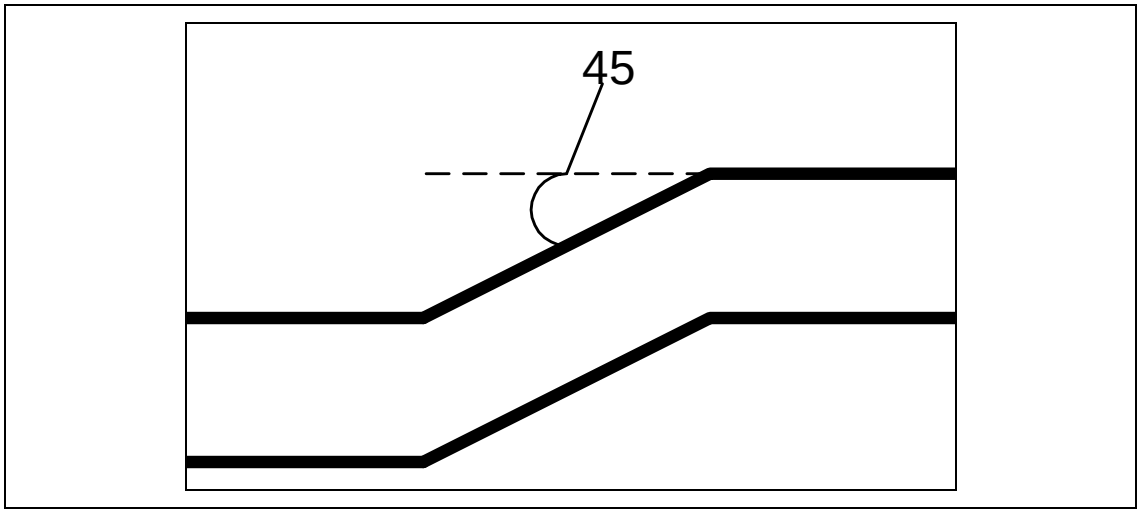
10.1.2.1. General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

To optimize board performance, consider the following suggestions.

- Maximum mismatch between the length of the clock trace and the length of any data trace is 0.5 inches.
- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. (Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and degraded receive BER.)
- Do not route the transmit differential traces closer than 70 mils to the receive differential traces.
- Do not route any other signal traces parallel to the differential traces and closer than 70 mils to the differential traces.
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, Intel recommends using two 45° bends instead. Refer to Figure 53.
- Traces should be routed away from the board edges by a distance greater than the trace height above the ground plane. Routing away from the board edges allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. As a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 53: Trace Routing



10.1.2.1.1. Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be approximately100Ω. It is necessary to compensate for trace-to-trace edge coupling (which can lower the differential impedance by 10Ω) when the traces within a pair are closer than 0.030 inches (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance.

10.1.2.1.2. Signal Isolation

Follow the rules below for signal isolation.

- Separate and group signals by function on separate layers if possible. Maintain a gap of 70 mils between all differential pairs (Phoneline and Ethernet) and other nets, but group associated differential pairs together.

Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk that can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, processor, or other similar devices.

10.1.2.2. Power and Ground Connections

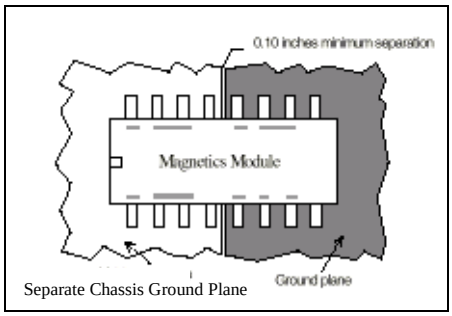
Follow the guidelines below for power and ground connections.

- All VCC pins should be connected to the same power supply.
- All VSS pins should be connected to the same ground plane.
- Use one decoupling capacitor per power pin for optimized performance.
- Place decoupling as close as possible to power pins.

10.1.2.2.1. General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 54: Ground Plane Separation



Grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return. Grounding will significantly reduce EMI radiation.

The guidelines below will help reduce circuit inductance in both backplanes and motherboards.

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling.
- Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.
- Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1.5 mm (59.0 mil). This is a ***critical*** requirement needed to pass FCC part 68 testing for phoneline connection.

10.1.2.3. Network Physical Layout Issues

Below is a list of common physical layer design and layout mistakes in LAN on motherboard designs.

- Unequal length of the two traces within a differential pair. Inequalities create common Mode noise, and they will distort the transmit or receive waveforms.
- Lack of symmetry between the two traces within a differential pair. (Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise, and distort the waveforms.
- Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector. Designing a spec-compliant LAN product beyond a total distance of approximately 4 inches can be difficult. Traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals if they are long. Also, any impedance mismatch in the traces will be aggravated if they are longer (see bullet 9 below).
- Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
- Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace. The transmit trace can also greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. In the vicinities where the traces enter or exit the magnetics, the RJ-45/11 , and the PLC are the only possible exceptions.
- Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no autotransformer in the transmit channel.)
- Another common mistake is using an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different, and there are also differences in the receive circuit. Please follow the appropriate reference schematic or Application Notes.
- Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45/11 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to the chassis ground via the proper value resistor and a capacitance or termplane. If the unused RJ pins are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
- Incorrect differential trace impedances. It is important to have approximately 100Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75Ω and 85Ω, even when designed for 100Ω. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge to edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close (see note) to each other, the edge coupling can lower the effective differential impedance by 5Ω to 20Ω. (A 10-Ω to 15-Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.
- Another common problem is that too large a capacitor is used between the transmit traces and/or too much capacitance from the magnetics's transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mb/s rise and fall time so that the capacitors fail the IEEE rise time and fall time specifications. Consequently, the return loss will fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used,

it should be less than 22 pF (6 pF to 12 pF values have been used on past designs with reasonably good success). Unless there is some overshoot in 100 Mb/s mode, these caps are not necessary.

Note: It is important to keep the two traces within a differential pair close to each other. Keeping the two traces close makes them more immune to crosstalk and other sources of common-mode noise, lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces. Close is defined as less than 0.030 inches between the two traces within a differential pair. Intel recommends 0.008-inch to 0.012-inch trace-to-trace spacing.

10.1.3. 82562EH Home/PNA* Guidelines

10.1.3.1. Related Documents

- *82562EH HomePNA 1 Mb/s Physical Layer Interface Datasheet*, order number: 278313-001. Available on Intel's website for developers is at http://developer.intel.com.
- *82562EH HomePNA 1 Mb/s Physical Layer Interface Brief Datasheet*, order number: 278314-001. Available on Intel's website for developers is at http://developer.intel.com.
- *RS-82562EH 1Mb/s Home PNA LAN Connect Option Application Note*: Order number OR-2065. Available on Intel's website for developers is at http://developer.intel.com.

For correct LAN performance, designers must follow the general guidelines outlined in Section 10.1.2. Additional guidelines for implementing an 82562EH Home/PNA* LAN connect component are provided in the subsequent section.

10.1.3.2. Power and Ground Connections

Follow the rules below for power and ground connections.

- For the best performance, place decoupling capacitors on the backside of the PCB, directly under the 82562EH, and with equal distance from both pins of the capacitor to power and ground.
- The analog power supply pins for 82562EH (VCCA, VSSA) should be isolated from the digital VCC and VSS through the use of ferrite beads. In addition, adequate filtering and decoupling capacitors should be provided between VCC and VSS, and VCCA and VSSA power supplies.

10.1.3.3. Guidelines for 82562EH Component Placement

Component placement can affect the signal quality, emissions, and temperature of a board design. The guidelines below are for component placement, which can perform the following:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.
- Minimizing the amount of space needed for the HomePNA LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA LAN circuits need to be as close as possible to the connector. Thus, all designs must fit in a very small space.

10.1.3.4. Crystals and Oscillators

Guidelines for Crystals and Oscillators are provided below.

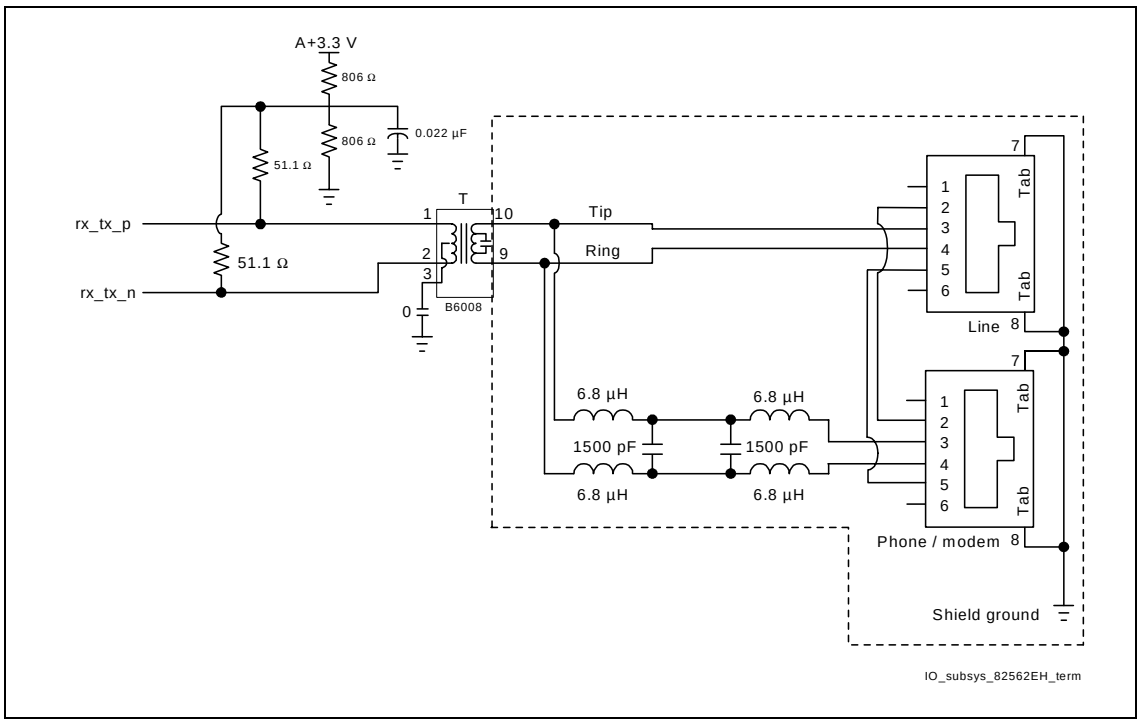
- To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis.
- Crystals should be kept away from the HomePNA magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case.
- The crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.
- For a noise-free and stable operation, place the crystal and associated discretes as close as possible to 82562EH, keeping the length as short as possible and do not route any noisy signals in this area.

10.1.3.5. Phone Line HPNA Termination

Guidelines for phone line HPNA termination are provided below.

- The transmit/receive differential signal pair is terminated with a pair of 51.1-Ω (1%) resistors. This parallel termination should be placed close to the 82562EH. The center, common point between the 51.1-Ω resistors is connected to a voltage divider network. The termination is shown in Figure 55.
- The filter and magnetics component T1, integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA LAN interface.
- One RJ-11 jack (labeled “LINE” in Figure 55) allows the node to be connected to the phone line, and the second jack (labeled “PHONE” in Figure 55) allows other downline devices to be connected at the same time. The HomePNA does not require this second connector.
- A low-pass filter, setup in-line with the second RJ-11 jack is also recommended by the HomePNA to minimize interference between the HomeRun connection and a POTs voice or modem connection on the second jack. This places a restriction of the type of devices connected to the second jack as the pass-band of this filter is set approximately at 1.1MHz. Please refer to the HomePNA website: www.homepna.org for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA certifications.

Figure 55: 82562EH Termination



10.1.3.6. Critical Dimensions

There are three dimensions to consider during layout. Distance “B” from the line RJ11 connector to the magnetics module, distance “C” from the phone RJ11 to the LPF (if implemented), and distance “A” from 82562EH to the magnetics module (See Figure 56).

Figure 56: Critical Dimensions for Component Placement

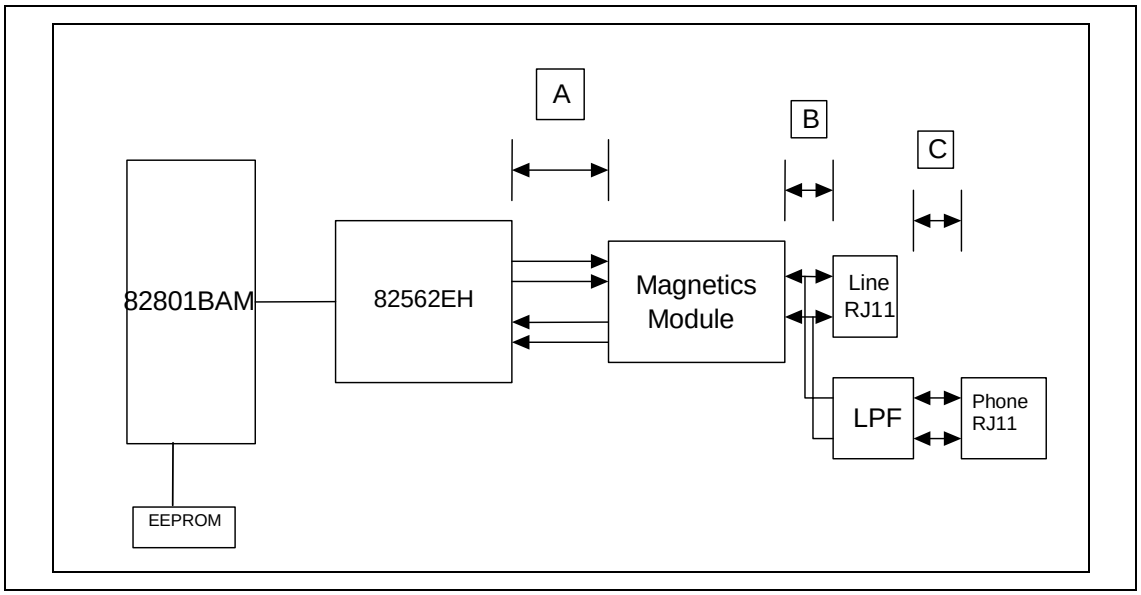


Table 37: Critical Dimension Definition

Distance	Priority	Guideline
B	1	< 1 inch
A	2	< 1 inch
C	3	< 1 inch

10.1.3.6.1. Distance from Magnetics Module to Line RJ11

The distance “B” should be given highest priority and should be less than 1 inch. For trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contributes to common mode noise, which can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

10.1.3.6.2. Distance from 82562EH to Magnetics Module

Due to the high-speed of signals present, distance “A” between the 82562EH and the magnetics should also be less than 1 inch, but should be second priority relative to distance form connects to the magnetics module.

In general, any section of trace that is intended for use with high-speed signals should observe proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between device and traces route. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself.

10.1.3.6.3. Distance from LPF to Phone RJ11

This distance “C” should be less then 1 inch. For trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

10.1.4. 82562ET/82562EM and 82562ET/82562 EH Guidelines

10.1.4.1. Related Documents

- *82562ET Platform LAN Connect (PLC) Datasheet*
- *PCB Design for the 82562 ET/EM Platform LAN Connect*
- *ICH2 Integrated LAN Controller Function Disable and Power Control Application Note (AP-417, Order# OR-2218)*

For correct LAN performance, designers must follow the general guidelines outlined in Section 10.1.2. Additional guidelines for implementing an 82562ET or 82562EM LAN connect component are provided below.

10.1.4.2. Guidelines for 82562ET/82562EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can do the following:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces. Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, all designs must fit in a very small space.

10.1.4.3. Crystals and Oscillators

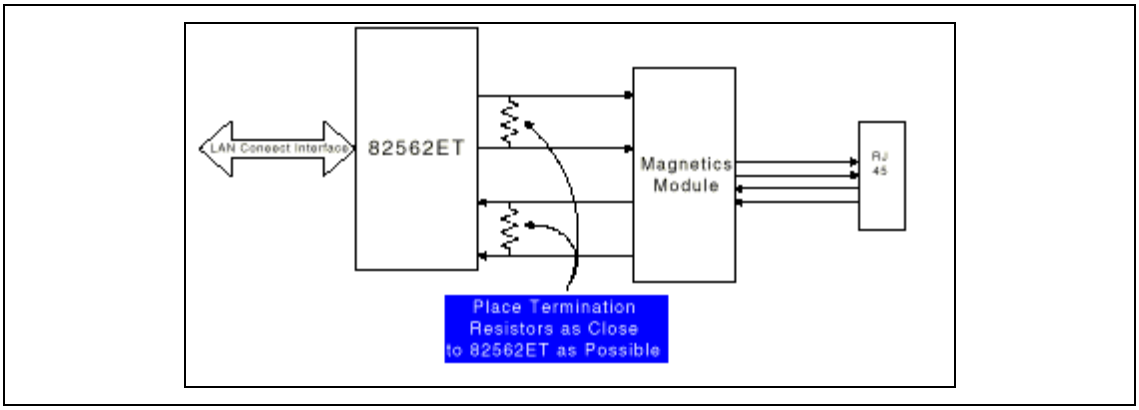
Below are guidelines for the crystals and oscillators.

- To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis.
- Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case.
- The crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.
- For a noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562ET or 82562EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

10.1.4.4. 82562ET/82562EM Termination Resistors

The 100-Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 100-Ω (1%) receive differential pairs (RDP/RDN) should be placed as close to the LAN connect component (82562ET or 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer. See Figure 57 below.

Figure 57: 82562ET/82562EM Termination



10.1.4.5. Critical Dimensions

There are two dimensions to consider during layout. Distance “B” from the line RJ45 connector to the magnetics module and distance “A” from the 82562ET or 82562EM to the magnetics module (see Figure 58).

Figure 58: Critical Dimensions for Component Placement

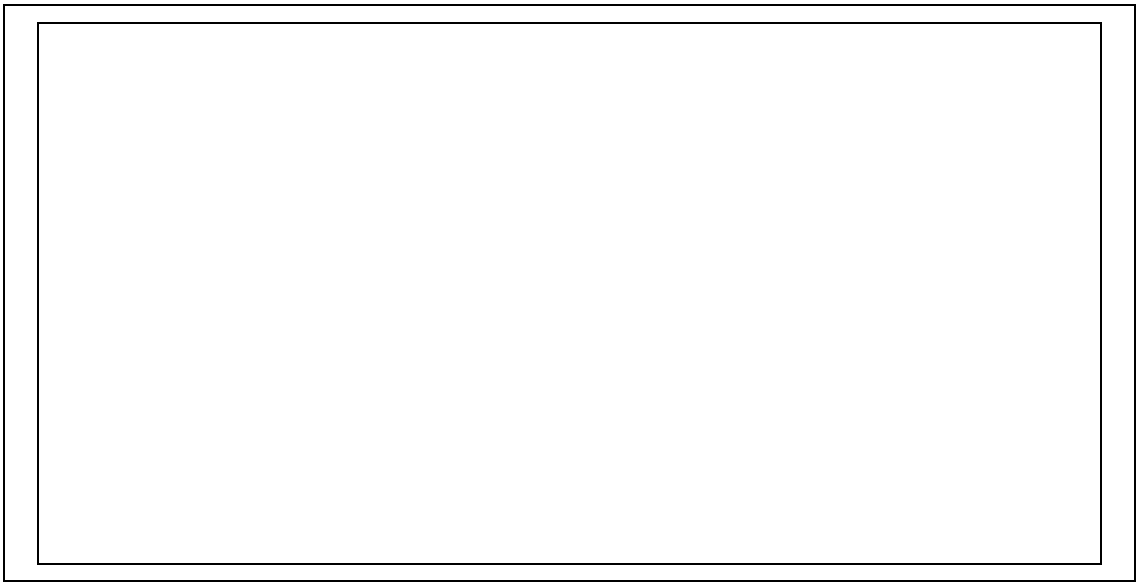


Table 38: Critical Dimensions Component Definition

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

10.1.4.5.1. Distance From Magnetics Module to RJ45

The distance A in Figure 58 above should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- Differential impedance should be 100Ω. The single ended trace impedance will be approximately 50Ω; however, the differential impedance can also be affected by the spacing between the traces.
- For trace symmetry, differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562ET must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562ET and RJ-45 will as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105Ω–110Ω should compensate for second order effects.

10.1.4.5.2. Distance From 82562ET to Magnetics Module

Distance B should also be designed less than 1 inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100-Ω differential value. These traces should also be symmetric and equal length within each differential pair.

10.1.4.6. Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards.

- Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels.
- Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc.
- All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential, which helps reduce circuit inductance.
- Physically locate grounds to minimize the loop area between a signal path and its return path.
- Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high-frequency harmonics that can radiate significantly, the most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk.

- The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

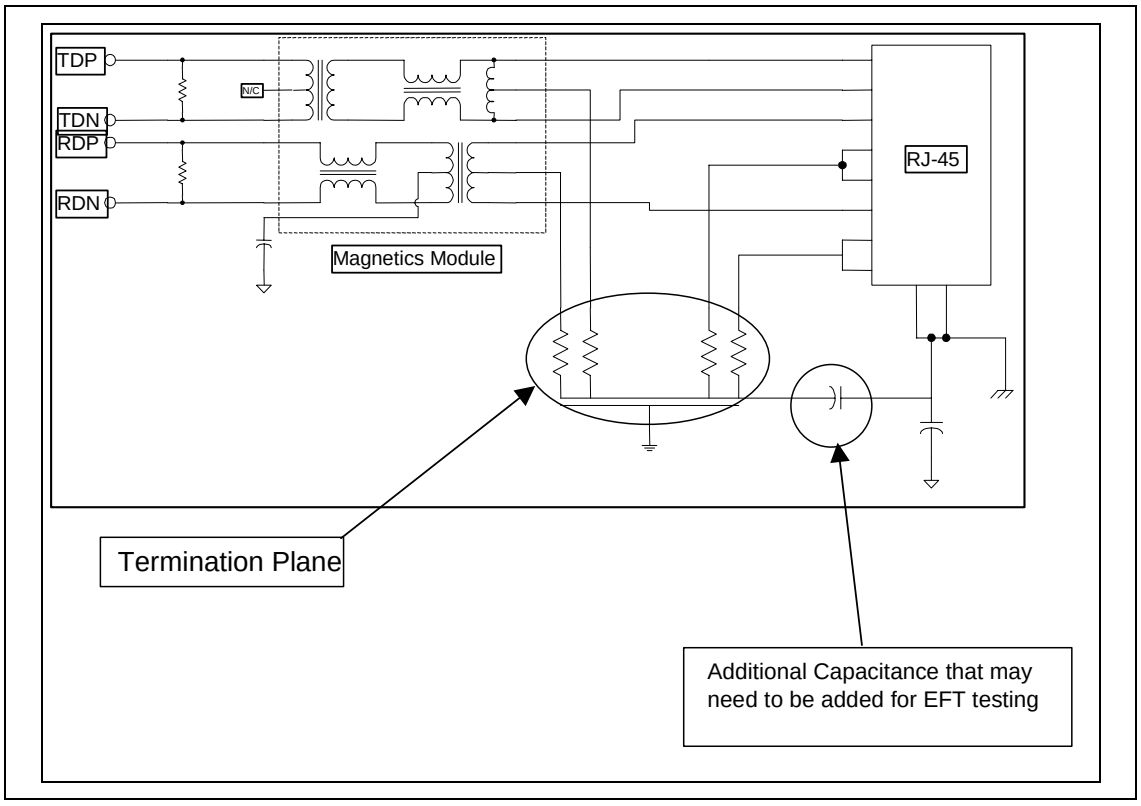
10.1.4.6.1. Terminating Unused Connections

In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to ensure that emission requirements are met. The method most often implemented is called the "Bob Smith" Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75-Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

10.1.4.6.2. Termination Plane Capacitance

Intel recommends that the termination plane capacitance equal a minimum value of 1500 pF, which helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used to meet the EFT requirements, it should be rated for at least 1000 Vac.

Figure 59: Termination Plane



10.1.4.7. 82562ET/82562EH Dual Footprint Guidelines

The guidelines in this section characterize the proper layout for a dual footprint solution. This configuration enables the developer to install either the 82562EH or the 82562ET/82562EM components while having only one motherboard design. The guidelines called out in Section 10.1.1 apply to this configuration. The dual footprint for this particular solution uses an SSOP footprint for 82562ET and a TQFP footprint for 82562EH. The combined footprint for this configuration is shown in Figure 60 and Figure 61 below.

Figure 60: Dual Footprint LAN Connect Interface

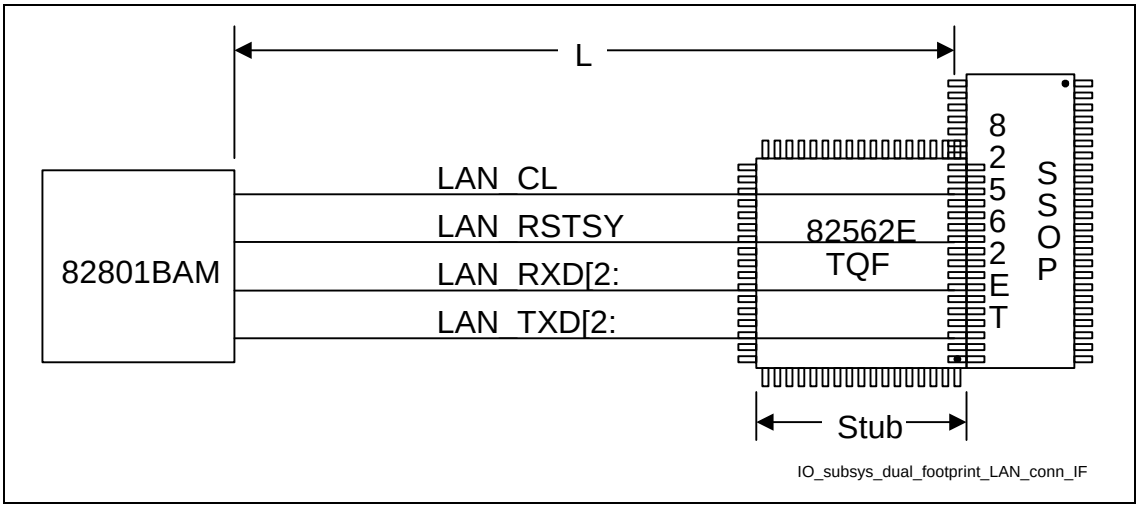
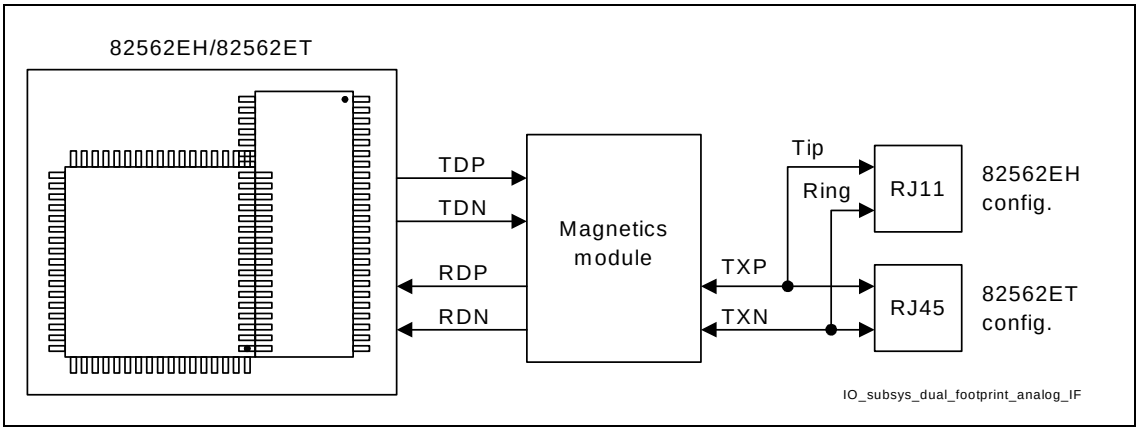


Figure 61: Dual Footprint Analog Interface



Additional guidelines for this configuration are provided below.

- L = 1.5 inches to 4.5 inches
- Stub < 0.5 inches
- Either 82562EH or 82562ET/82562EM can be installed. Not both.
- 82562ET pins 28,29, and 30 overlap with 82562EH pins 17,18, and 19.
- Overlapping pins are tied to ground.
- No other signal pads should overlap or touch.

- Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], LAN_TXD[0], RDP, RDN, RXP/Ring, and RXN/Tip are shared by the 82562EH and 82562ET configurations.
- No stubs should be present when 82562ET is installed.
- Packages used for the Dual Footprint are TQFP for 82562EH and SSOP for 82562ET.
- A 22-Ω resistor can be placed at the driving side of the signal line to improve signal quality on the LAN connect interface.
- The resistor should be placed as close as possible to the component.
- Use components that can satisfy both the 82562ET and 82562EH configurations (i.e., magnetics module).
- Install components for either the 82562ET or the 82562EH configuration. Only one configuration can be installed at a time.
- Route shared signal lines so that stubs are not present or are kept to a minimum.
- Stubs may occur on shared signal lines (i.e., RDP and RDN). These stubs are due to traces routed to an uninstalled component.
- Use 0.0-Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.
- Refer to Camino 2 CRB layout for routing examples.

10.1.5. 82550

Recommended practices for 82550 should be identical to those of the 82562EH, Section 10.1.4. Exceptions are as follows: the 82550 module requires that the Isolate pin is connected to PCI reset and that they both are connected to a pull up line. The 82550 module also requires that Alt reset is connected to a pull up line.

10.2. Other Subsystems

10.2.1. Super I/O

A Super I/O (SIO) with a LPC host interface can be used with 82801BAM. The SIO's host interface will connect to 82801BAM LPC interface. The SIO's reset input should be derived from 82801BAM PCIRST#. The SIO should have a Serial IRQ (SERIRQ) output, and this output should be connected to 82801BAM SERIRQ. The SIO should use one of the PCICLK to clock its LPC interface. The SIO's LDRQ# signal (for supporting legacy DMA) can be connected to either LDRQ0# or LDRQ1# from 82801BAM.

If additional system GPIOs are required in the design (beyond what is provided by 82801BAM), GPIOs from the SIO can be used.

10.2.2. RTC

The 82801BAM contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The RTC incorporates not only the features for keeping the time and date but also CMOS memory used by the BIOS, and a backup battery that keeps the clock running and the CMOS updated when the PC is switched off.

This section will present the recommended hookup for the RTC circuit for the 82801BAM. This circuit is not the same as the circuit used for the PIIX4.

10.2.2.1. RTC Crystal

The 82801BAM RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 pins. Figure 62 represents the external circuitry that comprises the oscillator of the 82801BAM RTC.

10.2.2.2. External Capacitors

To maintain the RTC accuracy, the external capacitor C1 must be set to 2.2 nF. The external capacitor values (C2 and C3) should also be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when the crystal is combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate the RTC will be.

Equation 7 can be used to choose the external capacitance values (C2 and C3).

Equation 7.

$$Cload = (C2^* C3)/(C2+C3) + Cparasitic$$

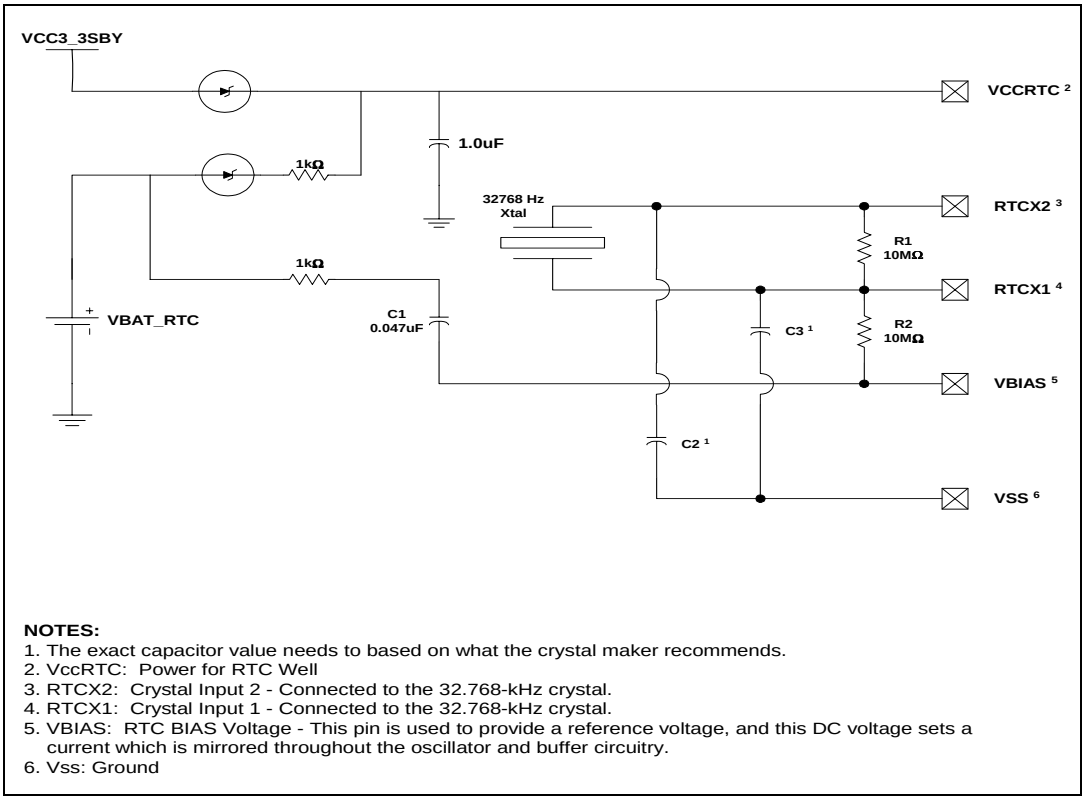
C3 can be chosen such that C3 is greater than C2. Then C2 can be trimmed to obtain the 32.768 kHz.

10.2.2.3. RTC Layout Considerations

RTC layout considerations are provided below.

- Keep the lead lengths as short as possible; around ¼ inch is sufficient.
- Minimize the capacitance between Xin and Xout in the routing.
- Put a ground plane under the XTAL components.
- Do not route any switching signals under the external component (unless separated by a ground plane).
- The oscillator VCC should be clean; use a filter, such as an RC low pass or a ferrite inductor.

Figure 62: External Circuitry for the 82801BAM RTC



NOTES:
1. The exact capacitor value needs to based on what the crystal maker recommends.
2. VccRTC: Power for RTC Well
3. RTCX2: Crystal Input 2 - Connected to the 32.768-kHz crystal.
4. RTCX1: Crystal Input 1 - Connected to the 32.768-kHz crystal.
5. VBIAS: RTC BIAS Voltage - This pin is used to provide a reference voltage, and this DC voltage sets a current which is mirrored throughout the oscillator and buffer circuitry.
6. Vss: Ground

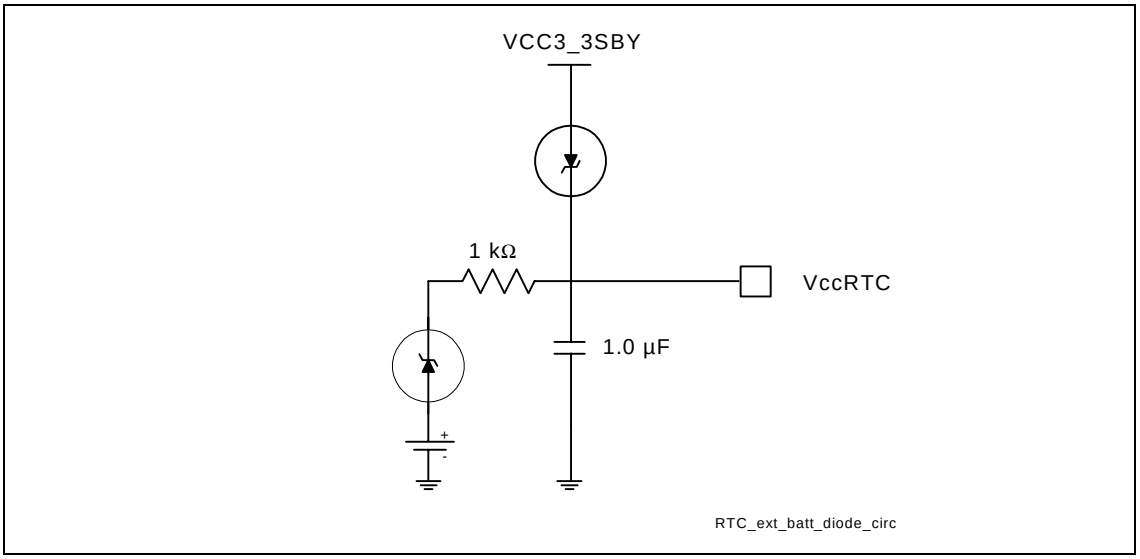
10.2.2.4. RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH is not powered by the system. Some example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 uA, the battery life will be at least 170,000 µAh/3 µA = 56,666 h = 6.4 years.

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0V to 3.3V.

The battery must be connected to the ICH via an isolation diode circuit. The diode circuit allows the ICH RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 63 is an example of a diode circuitry that is used.

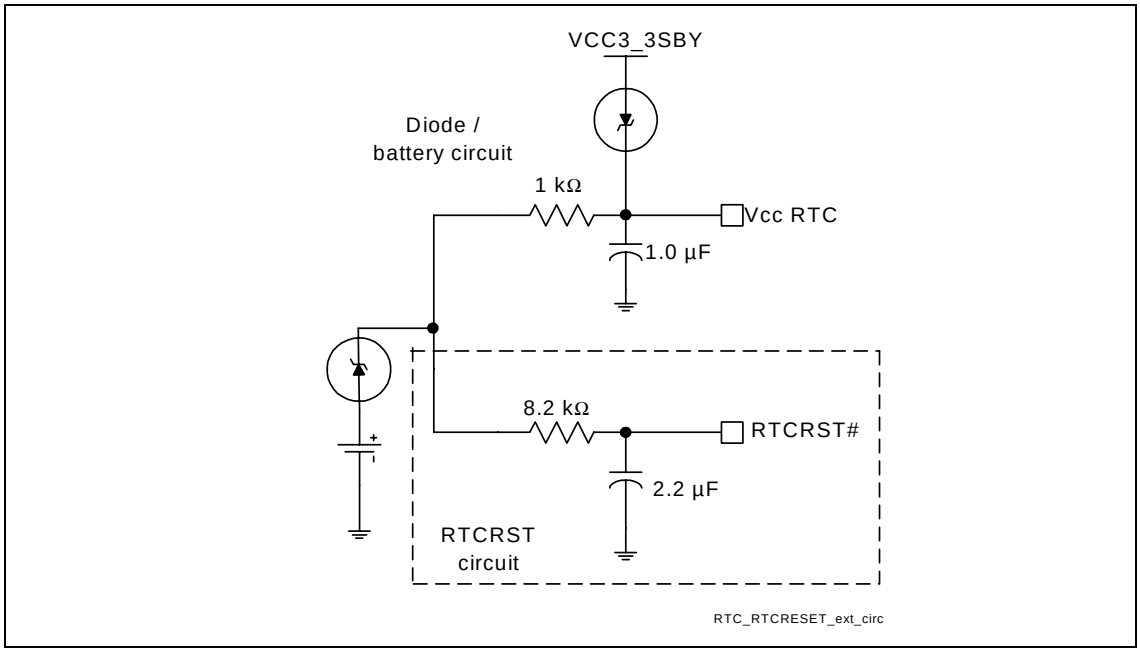
Figure 63: A Diode Circuit to Connect the RTC External Battery



A standby power supply should be used in desktop and mobile systems to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

10.2.2.5. RTC External RTEST Circuit

Figure 64: RTEST External Circuit for the ICH RTC



The 82801BAM RTC requires some additional external circuitry. The RTEST# (RTC Well Test) signal is used to reset the RTC Well. The external capacitor (2.2 µF) and the external resistor (8.2 KΩ) between RTEST# and the RTC battery (Vbat) were selected to create an RC time delay, such that RTEST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10 mS-20 mS. When RTEST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result, when the system boots, the BIOS knows that the RTC battery has been removed.

The RTEST circuit is combined with the diode circuit (Figure 63), which allows RTC-well to be powered by the battery when the system power is not available. Figure 64 is an example of this circuitry that is used, in conjunction with the external diode circuit.

Note: RTEST# will be renamed to RTCRESET# in a future revision of the Intel® 815EM Chipset: 82815EM Graphics and Memory Controller Hub (GMCH2-M) Datasheet.

10.2.2.6. RTC Routing Guidelines

The RTC routing guidelines are provided below.

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1 inch, the shorter the better.
- Minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them).
- Put a ground plane under all of the external RTC circuitry.

- Do not route any switching signals under the external components (unless on the other side of a ground plane).

10.2.2.7. VBIAS DC Voltage and Noise Measurements

The following list provides the VBIAS DC voltage and noise measurements.

- Steady state VBIAS will be a DC voltage of about 0.38V ± .06V.
- VBIAS will be "kicked" when the battery is inserted to about 0.7V-1.0V, but it will come back to its DC value within a few mS.
- Noise on VBIAS must be kept to a minimum, 200 mV or less.
- VBIAS is very sensitive and cannot be directly probed, it can be probed through a .01-uF capacitor.
- Excess noise on VBIAS can cause the 82801BAM internal oscillator to misbehave or even stop completely.
- To minimize noise of VBIAS, implement the routing guidelines described above and the required external RTC circuitry as described in the *Intel® 815EM Chipset: 82815EM Graphics and Memory Controller Hub (GMCH2-M) Datasheet*.

10.2.3. System Management Controller

An embedded controller can be used in the design to enhance system management capability. If an embedded controller is used, it should be an LPC-based micro-controller.

The embedded controller's host interface should be connected to 82801BAM LPC interface. Its host interface should be clocked by one of the PCICLKs.

The embedded controller should have three system interrupt outputs for supporting system management functions: EXT_SMI#, runtime SCI, and wake SCI. These three system interrupts need to be routed to 82801BAM GPIs.

10.2.4. Keyboard Controller

The Keyboard Controller should have an LPC host interface, and the keyboard controller's reset should be derived from the 82801BAM PCIRST#. The keyboard controller's host interface clock should be obtained from one of the PCICLKs, and its SERIRQ output should be connected to 82801BAM SERIRQ. Finally, the keyboard controller's A20GATE output and RCIN# output should be connected to the corresponding 82801BAM inputs.

10.2.5. FWH

The Firmware hub is a part of the chipset and is the key to enable future security and manageability infrastructure for a system. The device operates under FWH interface/protocol. The hardware features of this device include up to 8-Mbit, non-volatile flash memory core, a Random Number Generator (RNG), protected storage, five general purpose inputs (GPIs), register-based block locking, and hardware-based block locking.

An integrated combination of logic feature and non-volatile memory enables better protection for storage and update for platform code, and data adds platform flexibility through additional GPIs and allows quicker introduction of new security/manageability features.

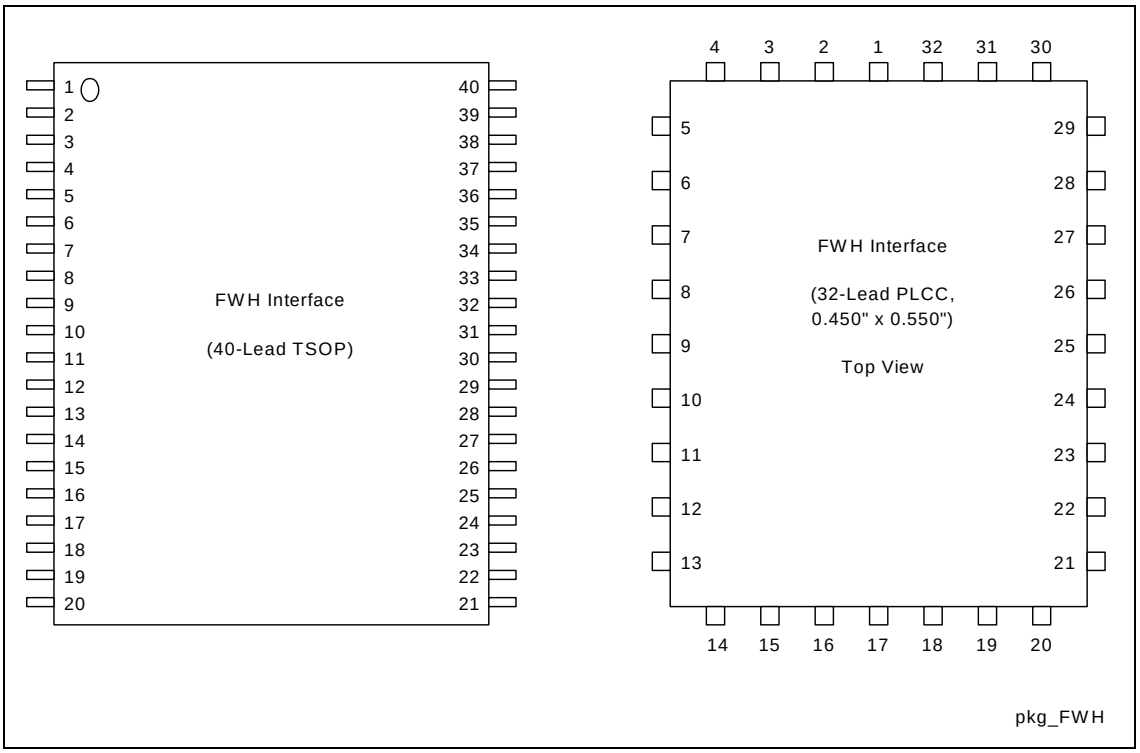
10.2.5.1. FWH Overview

The FWH is equipped with two configurable interfaces, the FWH and A/A Mux. The IC, interface configuration pin of the device provides control between these two interfaces. The FWH interface is designed to work with 82801BAM during platform operation. The A/A interface is designed as a programming interface for OEMs.

The FWH interface consists primarily of a five-signal interface, and the buffers are designed to be PCI compliant. The FWH interface operates at 33 MHz, which is synchronous with PCI interface.

The A/A Mux refers to multiplexed row and column addresses in this interface. This approach is used to provide quick programming/testing in OEMs manufacturing flow. This also allows for an efficient programming interface fitting into small pin count device. For more information on this interface, consult the *Intel® Firm Ware Hub PROM Programmer Architecture Specification*.

Figure 65: FWH Packages



10.2.5.2. FWH Programming

A feature of the FWH component is a non-volatile memory core based on Intel Flash Technology. This technology enables fast factory programming and low-power designs. The FWH component supports read operations at 3.3-V Vcc and block erase and program operations at 3.3V and 12V Vpp. Programming at 12.0-V Vpp is faster and increases factory throughput. However, this method is not recommended for in-system operation in the platform due to an 80-hour limit on 12.0V on Vpp pin over the lifetime of the device (programming or not). With a 3.3-V Vpp option, Vcc and Vpp should be tied together for a simple 3.0-V design. Full programming current may be drawn from either pin Vpp or Vcc, and care should be taken while connecting these pins to the 3.3V.

10.2.5.3. In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The 82801BAM Hub Interface to PCI Bridge will put all processor boot cycles out on PCI (before sending them out on the FWH interface). If the 82801BAM is set for subtractive decode, these boot cycles can be accepted by a positive decode agent out on PCI, which enables the ability to boot from a PCI card that positively decodes these memory cycles. In order to boot off a PCI card, it is necessary to keep the 82801BAM in subtractive decode mode. If a PCI boot card is inserted and the 82801BAM is programmed for positive decode, there will be two devices positively decoding the same cycle.

10.3. Power Management

- A power button is required by the ACPI specification.
- PWRBTN# is connected to the front panel on/off power button. The 82801BAM integrates 16-ms debouncing logic on this pin.
- AC power loss circuitry has been integrated into the 82801BAM to detect power failure.
- It is recommended that the PS_POK signal from the power supply connector be routed through a Schmitt trigger to square-off and maintain its signal integrity. It should not be connected directly to logic on the board.
- PS_POK logic from the power supply connector can be powered from the core voltage supply.
- RSMRST# logic should be powered by a standby supply, while making sure that the input to the ICH0/ICH is at the 3-V level. The RSMST# signal requires a minimum time delay of 1 ms from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1-ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20-ms delay at the input of the Schmitt trigger to ensure that the Schmitt trigger inverters have sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed VCC(RTC).
- It is recommended that 3.3-V logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from VCC5.
- The PWROK signal to the chipset is a 3-V signal.
- The core well power valid to PWROK asserted at the chipset is a minimum of 1 ms.
- PWROK to the chipset must be deasserted after RSMRST#.
- PWRGOOD signal to processor is driven with an open-collector buffer pulled up to 2.5 V, using a 330-Ω resistor.
- RI# can be connected to the serial port is this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the 82801BAM suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shutdown feature.
- SLP_S3# from the 82801BAM must be inverted and then connected to PSON of the power supply connector to control the state of the core well during sleep states.
- The circuitry checks for both processor VRM powered up and the PS_POK signal from the ATX power supply connector, before asserting PWRGOOD and PWROK to the processor and 82801BAM.

10.3.1. General Description of ACPI Power States

Power States	Description
G0/S0/C0	Full on: CPU is fully operating. Individual devices may be shut to save power. Different CPU operating levels are described in system level state transition table below. Within the C0 state, the 82801BAM can throttle the STPCLK# signal to further reduce power consumption.
G0/S0/C1	Auto-Halt: CPU has executed an AutoHalt instruction and is not executing code. The CPU snoops the bus and maintains cache coherency.
G0/S0/C2	Quick-start: The STPCLK# signal goes active to the CPU. There are restrictions on what interrupt signals can go active while STPCLK# is active.
G0/S0/C3	Stop-Clock: The STPCLK# signal goes active to the CPU. The CPU performs a Stop-Grant cycle and halts its instruction stream. This is used in the mobile system for Intel® SpeedStep™ Technology support.
G1/S1	Power-On Suspend (POS): In this state, all clocks are stopped except the 32.768 KHz clock. The system context is maintained in the system memory. Power is on to CPU, PCI, memory controller, memory, and all other critical circuits.
G1/S3	Suspend-to-RAM (STR): The system context is maintained in system memory, but power is shut to non-critical circuits. Memory is retained and refreshes continue. All clocks are shut except RTC.
G1/S4	Suspend-to-Disk (STD): The system context is maintained on the disk. All power is shut except for the logic required to resume. Externally appears same as S5, but may have different wake events.
G2/S5	Soft Off (SOFF): System context not maintained. All power is shut except for logic required to restart. A full boot is required when waking.
G3	Mechanical Off (MOFF): System context not maintained. All power is shut except for the RTC. No wake events are possible. When system power returns, transition will depend on the state just prior to the entry to G3.

10.3.2. Power State Transition Rules

Present State	TRANSITION TRIGGER	Next State
G0/S0/C0	CPU halt instruction	G0/S0/C1
	ACPI defined Level 2 Read	G0/S0/C2
	ACPI defined Level 3 Read	G0/S0/C3
	SLP_EN bit set	G1/Sx or G2/S5
	Power Button Override	G2/S5
	Mechanical Off/Power Failure	G3

Present State	TRANSITION TRIGGER	Next State
G0/S0/C1	Any Enabled Break Event	G0/S0/C0
	STPCLK# goes asserted	G0/S0/C2
	Power Button Override	G2/S5
	Power Failure	G3
G0/S0/C2	Any Enabled Break Event	G0/S0/C0
	STPCLK# goes inactive and was in C1	G0/S0/C1
	Power Button Override	G2/S5
	Power Failure	G3
G0/S0/C3	Any Enabled Break Event	G0/S0/C0
	Power Button Override	G2/S5
	Power Failure	G3
G1/S1,G1/S3, G1/S4	Any Enabled Break Event	G0/S0/C0
	Power Button Override	G2/S5
	Power Failure	G3
G2/S5	Any Enabled Break Event	G0/S0/C0
	Power Failure	G3
G3	Power Returns	G0/S0/C0 reboot or G2/S5 till power button pressed / other wake event.

10.3.3. ACPI Support

The Intel® 815EM chipset supports the minimum requirements for ACPI support. 815EM not only supports the minimum requirements for both system logic and for graphics controllers, but is also capable of controlling monitor's minimum functions.

10.3.4. 1.8V/3.3V Power Sequencing

The 82801BAM has two pairs of associated 1.8V and 3.3V supplies. These are {Vcc1_8, Vcc3_3} and {VccSus1_8, VccSus3_3}. These pairs are assumed to power up and power down together. **The difference between the two associated supplies must never be greater than 2.0V**. The 1.8V supply may come up before the 3.3V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.8V supply is typically derived from the 3.3V supply by means of a linear regulator).

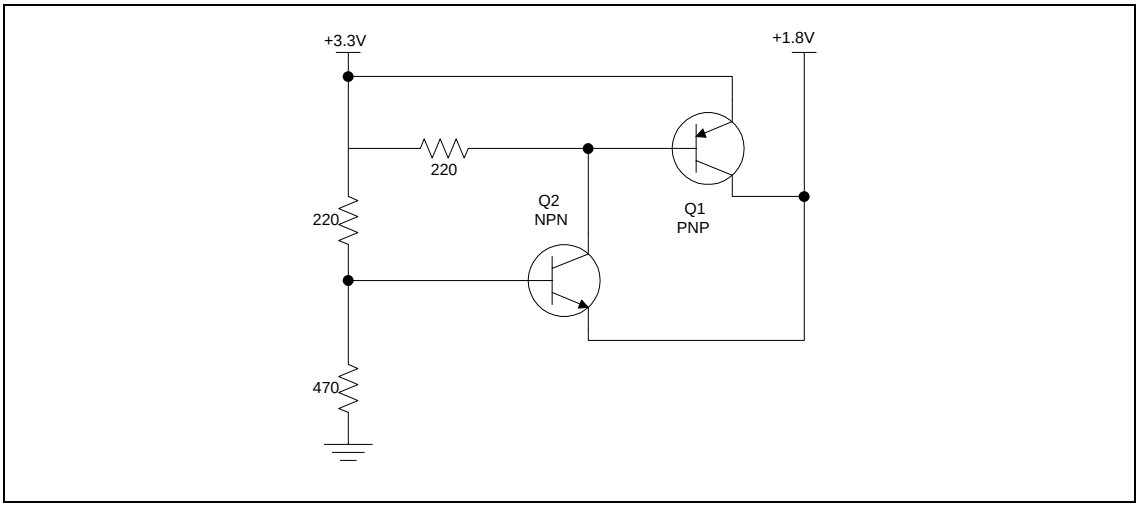
One serious consequence of violation of this "2V Rule" is electrical overstress of oxide layers, resulting in component damage.

The majority of the 82801BAM I/O buffers are driven by the 3.3V supplies, but are controlled by logic that is powered by the 1.8V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3V supply comes up first. In this case the I/O buffers will be in an undefined state until the 1.8V logic

is powered up. Some signals that are defined as "Input-only" actually have output buffers that are normally disabled, and the 82801BAM may unexpectedly drive these signals if the 3.3V supply is active while the 1.8V supply is not.

The figure below shows an example power-on sequencing circuit that ensures the “2V Rule” is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.8V supply tracks the 3.3V supply. The NPN transistor controls the current through PNP from the 3.3V supply into the 1.8V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8V plane, current will not flow from the 3.3V supply into 1.8V plane when the 1.8V plane reaches 1.8V.

Figure 66: Example 1.8V/3.3V Power Sequencing Circuit



When analyzing systems that may be "marginally compliant" to the 2V Rule, please pay close attention to the behavior of the 82801BAM RSMRST# and PWROK signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the Resume wells.
- PWROK controls isolation between the Resume wells and Main wells

If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

10.4. Capacitor Decoupling

10.4.1. Processor

The amount of bulk decoupling required on the V_{CC} and V_{CCT} planes to meet the voltage tolerance requirements for the mobile Intel® Pentium® III processor are a strong function of the power supply design. *Contact your Intel Field Sales Representative for tools to help determine how much bulk decoupling is required.*

10.4.1.1. High Speed Processors

For a processor with maximum performance mode at 700 MHz and above, the following decoupling is recommended. The processor core power plane (V_{CC}) should have fifteen 0.68 µF 0603 ceramic capacitors (using X74 dielectric for thermal reasons) placed directly under the package using two vias for power and two vias for ground to reduce the trace inductance. Also to minimize inductance, traces to those vias should be 22mils (in width) from the capacitor pads to match the via-pad size (assuming 22-mil pad size). Twenty-four 2.2 µF 0805 mid frequency decoupling capacitors should be placed around the die as close to the die as flex solution allows. The system bus buffer power plane (V_{CCT}) should have twenty 0.1-µF high frequency decoupling capacitors around the die.

10.4.1.2. Low Speed Processors

For a processor with maximum performance mode at 650MHz and below, the following decoupling is recommended. The processor core power plan (V_{CC}) should have twelve 0.1-µF high frequency decoupling capacitors placed underneath the die and twenty-seven 0.1-µF mid frequency decoupling capacitors placed around the die as close to the die (< 0.8” away) as flex solution allows. The system bus buffer power plane (V_{CCT}) should have fifteen 0.1-µF high frequency decoupling capacitors no further than 0.25 inches away from the V_{CCT} vias (balls).

10.4.2. Chipset

The placement of sufficient bulk capacitance on the system board is critical to the operation of the chipset and to ensure that the system design can accommodate various processors at various frequencies. In order to achieve proper filtering and in-rush current protection, it is imperative that additional filtering be provided on the system board. Table 39 below outlines the bulk capacitance requirements for the 815EM chipset platform.

Note: For more information, consult the Intel® Mobile Voltage Positioning Design Guide rev1.0.

Table 39: Bulk Capacitance Requirements per Power Plane

Power Plane	Bulk Capacitance Requirements			High-Frequency Capacitance Requirements	Notes
	Total Capacitance	ESR	RMS Ripple Current		
V_DC	100 µF 4 x 10 µF	20 mΩ	3A ~ 5A	0.1 µF, 0.01 µF	1, 3, 4, 5, 6, 7
V_5	100 µF	100 mΩ	1A	0.1 µF, 0.01 µF	4, 5, 6, 7
V_3	470 µF	100 mΩ	1A	0.1 µF, 0.01 µF	4, 5, 6, 7
VCCT	150 µF 14 x 1 µF 2.2 µF	N/A	N/A	8200 pF	5, 6, 7, 8
VCLK	10 µF, 1 µF	N/A	N/A	8200 pF	2, 5, 6, 7

NOTE:

1. Placement of the above capacitors should be located near the power Mosfets
2. The 10µF V_CLK filtering should be located next to the system clock synthesizer. The 1µF should be placed at the regulator V_CLK output
3. The RMS ripple current specification depends on V_DC input
4. If Tantalum Capacitors are used, a 50% voltage derating practice must be observed. For Example, a 5.0V rail requires a 10V rated capacitor
5. In order to reduce ESR, Intel recommends the use of multiple bulk capacitors rather than a single large capacitor
6. Intel strongly recommends that system designers pay close attention to capacitor design recommendations. Specifically, the “Capacitance vs. Temperature De-rating Curve”, the “Capacitance vs. Applied DC Voltage De-rating Curve”, and the “Capacitance vs. Frequency De-rating Curve”. Some capacitor dielectrics are particularly susceptible to these conditions.
7. Specifications marked as N/A are not available
8. The 150µF and 14x1µF capacitors should be placed near the regulator circuit. The 2.2µF should be placed near the 82801BAM VCCT input

10.5. System Management Signals

Checklist Items	Recommendations
SMBCLK, SMBDATA	Requires external pull-up resistors. See SMBus Architecture and Design Considerations section to determine the appropriate power well to use to tie the pullup resistors (Core well, Suspend well or a combination). Typical value of pullup resistors is 8.2 KΩ
SMBALERT#/GPIO[11]	See GPIO section if SMBALERT# not implemented.
SMLINK[1:0]	An external pull-up resistor to 3.3V is required. Typical value of pullup resistors is 8.2 KΩ
INTRUDER#	If signal is not used, connect the signal to VCCRTC (Vbat).

10.6. Manageability Devices

The Intel® 815EM chipset platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. The platform supports all features in the Intel® 815EM chipset, in addition to the following features. These system management functions are designed to report errors, diagnose the system, and recover from system lockups, without the aid of an external microcontroller.

10.6.1. SMBus

The 82801BAM integrates a SMBus controller. The SMBus provides an interface for managing peripherals such as serial presence detection (SPD) and thermal sensors. The slave interface allows an external microcontroller to access system resources.

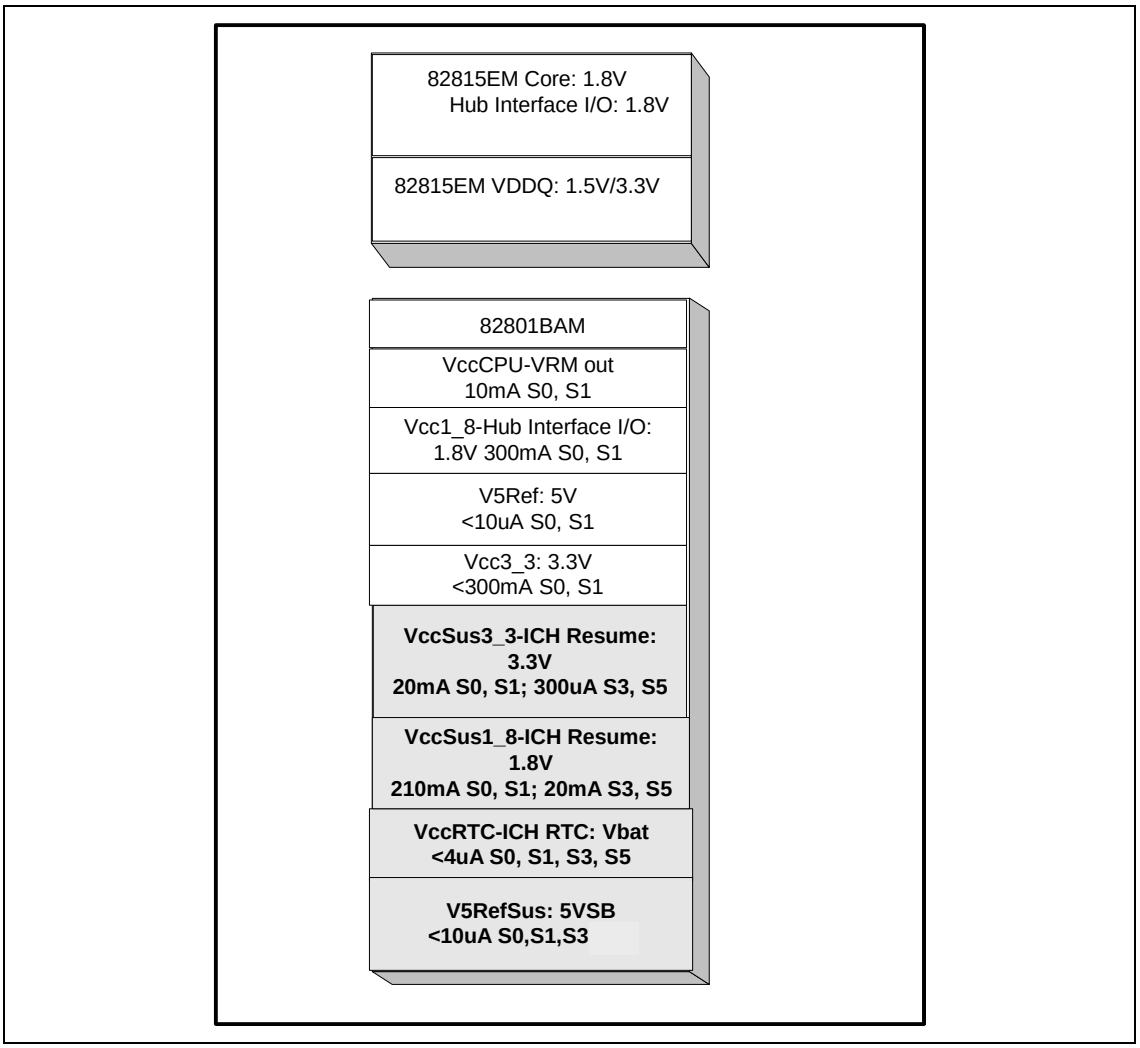
10.6.2. Interrupt Controller

The interrupt capabilities of the Intel® 815EM chipset platform expand support for up to 8 PCI interrupt pins and PCI 2.2 message-based interrupts. In addition, the 82801BAM supports system bus interrupt delivery.

10.7. Power Delivery

The following table provides the power requirements for Intel® 815EM chipset Platforms.

Figure 67: 815EM Power Requirements



10.8. Thermal Design Power

The thermal design power (TDP) is the estimated maximum possible power generated in a component by a realistic application. The TDP is based on extrapolations in both hardware and software technology over the life of the product and does not represent the expected power generated by a power hungry application.

The thermal design power numbers for the 82801BAM are listed in Table 40.

Table 40: 82801BAM Thermal Design Power

Device	Power
82801BAM	1.5W ±15%

10.9. Miscellaneous Board Considerations

Item	Recommendation
SPKR	82801BAM has an integrated pull-up resistor between 18 and 42KΩ. The integrated pull-up resistor is enabled only at boot/reset for strapping functions. At other times, the pull-up resistor is disabled. The effective impedance from the speaker and CODEC circuitry must be greater than 50KΩ. Alternatively, a means to isolate the resistive load from the signal could be used, such as a pass transistor.
FS[0]	82801BAM has an integrated weak pull-down resistor. No external pull-down resistors are required.

11. Debug

11.1. In-Target Probe (ITP)

An In-Target Probe (ITP) is a debug tool that allows access to on-chip debug features via a small port on the system board called the debug port. The ITP communicates to the processor through the debug port using a combination of hardware and software.

The debug port connector is connected to the signals that make up the processor's debug interface. Due to the nature of the ITP, the processor may be controlled without affecting any high-speed signals, which ensures that the system can operate at full speed with the ITP attached. Intel will use an ITP for internal debug and system validation and recommends that all system designs include a debug port.

The ITP port signals remain the same as in previous processors. However, a new connector has been defined. The new connector will help safeguard against using a 2.5-V or 3.3-V ITP with a 1.5-V tolerant processor.

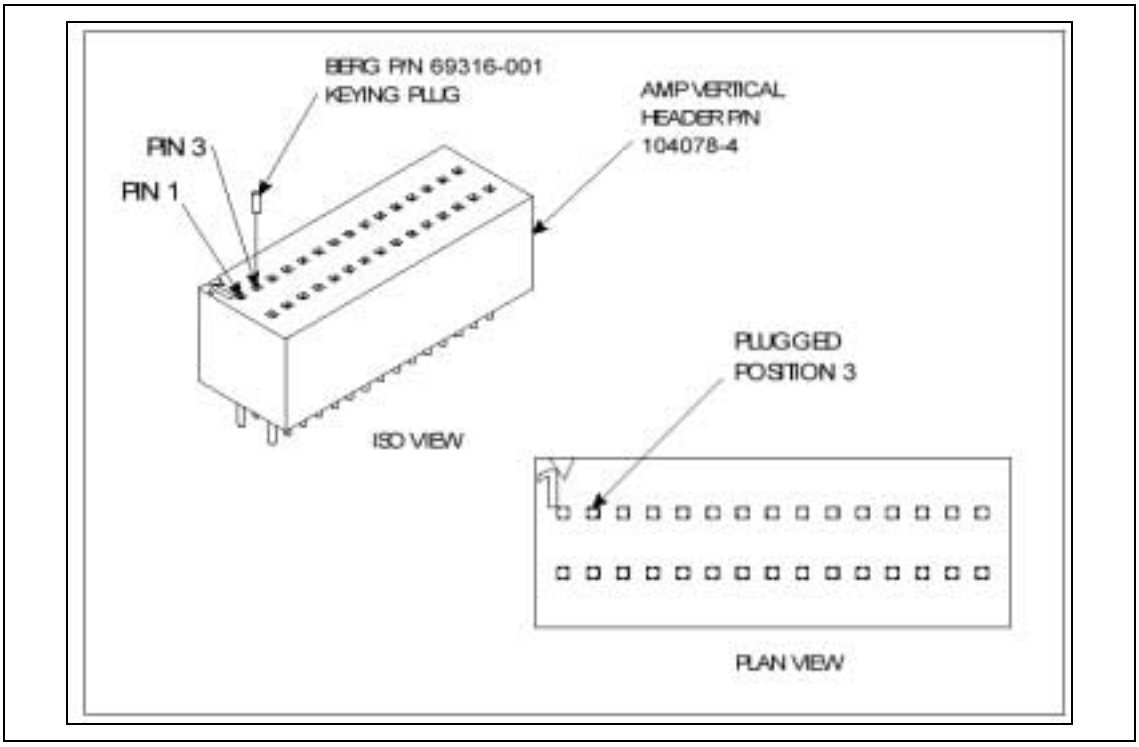
The following sections describe the mechanical and electrical design of the debug port.

11.2. Debug Port Connector Description

The ITP will connect to the system through the debug port. The recommended debug port connector is AMP* #104078-4. This connector is a 30-position, through-hole mount vertical receptacle (as shown in Figure 68 and

Figure 69). There is also a keying (polarizing) plug that needs to be inserted into position 3. The keying plug for this connector is BERG #69316-001. Full specifications for the AMP connector (including PCB layout guidelines) are available through AMP*, Incorporated. Information regarding the keying plug can be obtained through Berg Electronics*.

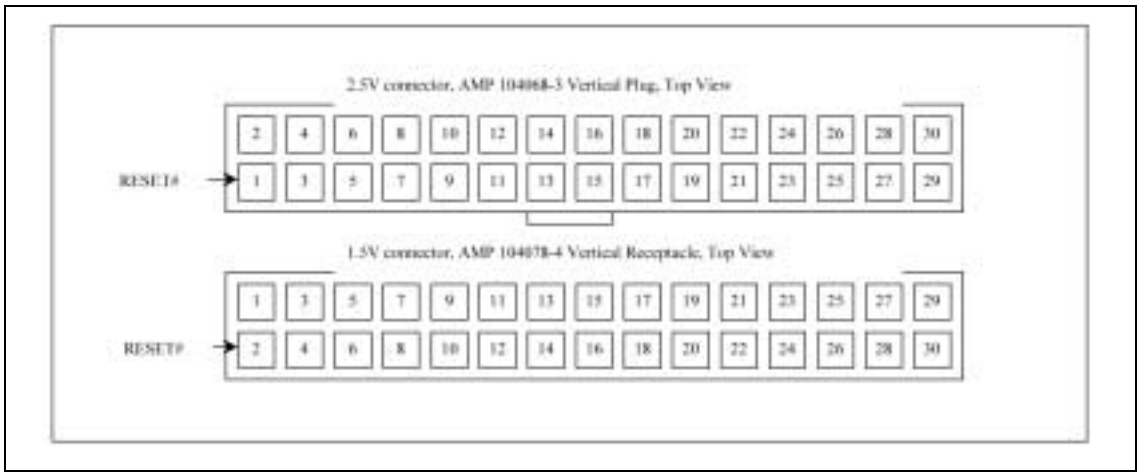
Figure 68: Debug Port Vertical Connector Example



Caution: This connector is different than previously specified for other Intel IA-32 processors, and the new connector receptacle counterpart is for use with processors utilizing 1.5-V CMOS TAP I/O signals. The connectors are high-density, through-hole connectors with pins on 0.050 inches by 0.100 inches centers. Do not confuse these with the more common 0.100 inches by 0.100 inches center headers. The debug port must be mounted on the system motherboard as the processor does not contain a debug port.

Caution: The mobile Intel® Pentium® III processor requires an ITP with a 1.5-V tolerant buffer board. Previous ITPs are designed to work with higher voltages and may damage the processor if they are connected to a mobile Intel® Pentium® III processor.

Figure 69: ITP Connector Comparison



The new 1.5-V connector resembles the old 2.5-V connector. Either connector will fit into the same Printed Circuit Board (PCB) layout. Just the pin numbers have changed, as seen in

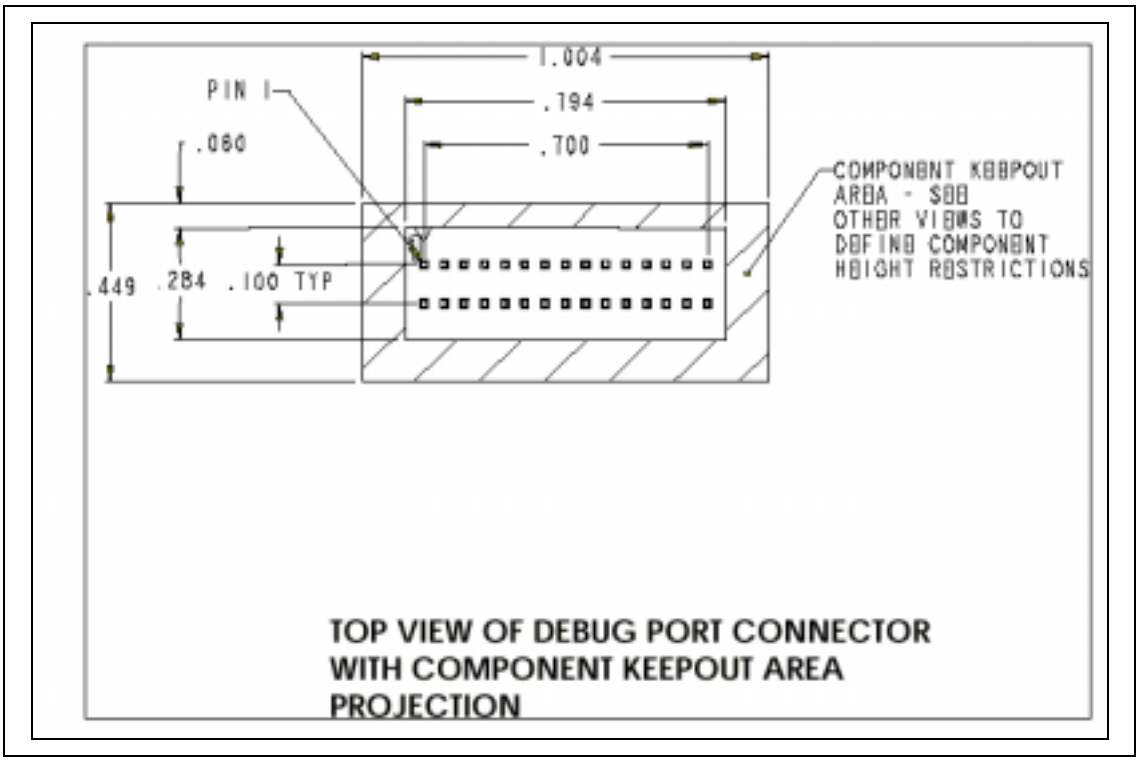
Figure 69 above.

11.2.1. Keep-out Concerns

There are two keep-out concerns to consider when designing a system that will support an ITP. First, in order for the ITP cabling to egress the system under test, a designer must either remove the “skins” of the system under test, or when this is not possible, design an aperture into the system.

Figure 70 details the second keep-out concern, the keep-out region that is required around the debug port connector.

Figure 70: Connector Keep-out Region



11.3. Debug Port Signal Notes

In general, all open-drain GTL+ outputs from the system must be retained at proper logic levels, whether or not the debug port is installed. GTL+ signals, RESET#, and PRDY# should be terminated at the debug port as shown in Figure 71.

Figure 71: GTL+ Signal Termination

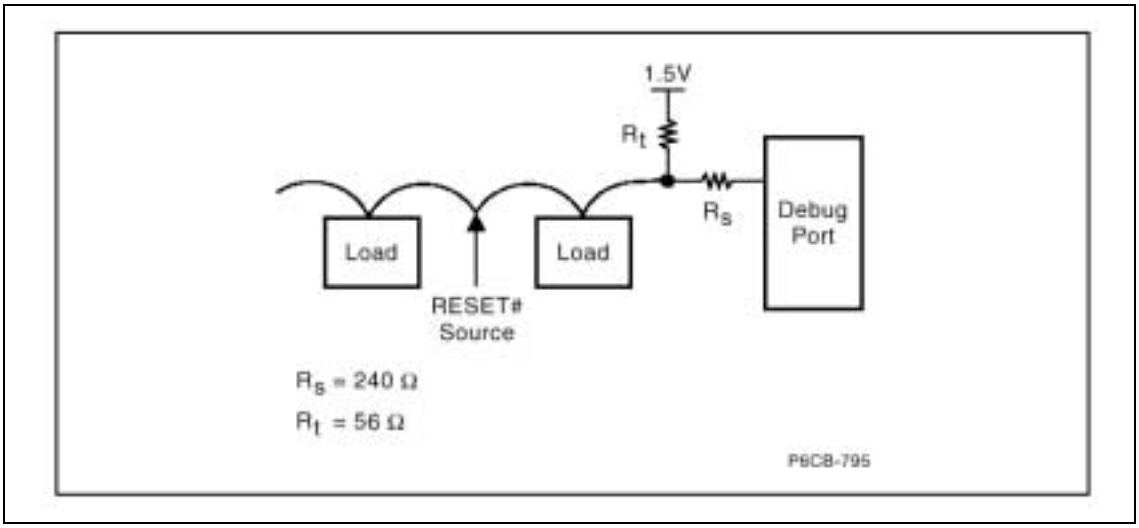


Table 41 lists the connector pins.

Table 41: Connector Pin Assignments

Name	Pin	Description	Specification Requirement	Notes
RESET#	2	Reset signal from target system to ITP	Terminate signal properly at the debug Port using 240-Ω series termination resistor and 56-Ω pullup to VCCT Debug port must be at the end of the signal trace	Note 1
DBRESET#	4	Allows ITP to reset entire target system	Tie signal to target system reset (Recommendation: PWRGOOD signal on the chipset as an Ored input). This is an open-drain output from the ITP to the target system and should be pulled up properly.	
TCK	6	TAP clock from ITP	Use 47-Ω series termination resistor with 1-K pullup to 1.5V near driver.	Note 2
TMS	8	Test mode select signal from ITP; Controls the TAP finite state machine	Use 47-Ω series termination resistor with 1-K pullup to 1.5 V near driver.	

Name	Pin	Description	Specification Requirement	Notes
TDI	7	Test data input signal from ITP to first component in boundary scan chain. Inputs test instructions and data serially	150-Ω pullup to 1.5V	
POWERON	10	Used by ITP to determine when target system power is on and once target system is on, enables all debug port electrical activity.	1.5-K pullup to 1.5V	
TDO	9	Test data output signal from last component in the boundary scan chain to the ITP. Test output is read serially	150-Ω pullup to 1.5V	
DBINST#	12	Indicates to target system that the ITP is installed	10-K pullup to 1.5V (optional)	
TRST#	11	Test reset signal from ITP; Used to reset TAP logic	680Ω– 1K pulldown to GND	
BSEN#	13	Informs target system that ITP is using boundary scan	NC	
PREQ#0	15	Probe ready signal, driven by processor 0, informs ITP that it is ready for debug mode.	1.5K pullup to 1.5V	
PRDY#0	17	Probe ready signal, driven by processor, informs ITP that it is ready for debug mode.	Terminate signal properly at the debug Port using 240-Ω series termination resistor and 56-Ω pullup to VCCT	
PREQ1#	19	Signal not used	NC	
PRDY1#	21	Signal not used	NC	
PREQ2#	23	Signal not used	NC	
PRDY2#	25	Signal not used	NC	
PREQ3#	27	Signal not used	NC	
PRDY3#	29	Signal not used	NC	
BCLK	30	Bus clock from target system (used in synchronous systems)	Must be connected to GND if not connected to BCLK	
GND	1,3,5,14, 16,18,20 ,22,24,2 6,28			

- For mobile Intel® Pentium® III processor systems, VCCT is the 1.5V GTL termination pull-up voltage.
- For legacy systems, terminating resistor value may be 0Ω to 47Ω.

Appendix A – Pullups and Pulldowns for Signals

Table 42: Pull-up and Pull-down Resistors

Signal	Pull-up/Pull-down	Ω	Notes
82815EM			
FRAME#	Pull-up to VDDQ	8.2 kΩ	
TRDY#	Pull-up to VDDQ	8.2 kΩ	
IRDY#	Pull-up to VDDQ	8.2 kΩ	
DEVSEL#	Pull-up to VDDQ	8.2 kΩ	
STOP#	Pull-up to VDDQ	8.2 kΩ	
SERR#	Pull-up to VDDQ	8.2 kΩ	
PERR#	Pull-up to VDDQ	8.2 kΩ	
RBF#	Pull-up to VDDQ	8.2 kΩ	
INTA#	Pull-up to VDDQ	8.2 kΩ	
INTB#	Pull-up to VDDQ	8.2 kΩ	
PIPE#	Pull-up to VDDQ	8.2 kΩ	
REQ#	Pull-up to VDDQ	8.2 kΩ	
WBF#	Pull-up to VDDQ	8.2 kΩ	
GNT#	Pull-up to VDDQ	8.2 kΩ	
AD_STB[1:0]	Pull-up to VDDQ	8.2 kΩ	
SB_STB	Pull-up to VDDQ	8.2 kΩ	
AD_STB[1:0]#	Pull-down to GND	8.2 kΩ	
SB_STB#	Pull-down to GND	8.2 kΩ	
GRCMP	Pull-down to GND	40Ω ± 2%	
HLZCOMP	Pull-up to 1.8V	36.5Ω ± 2%	
LTVDA	Pull-up to 3.3V	10 kΩ	If DVO unconnected, pullup 4.7 kΩ
LTCLK	Pull-up to 3.3V	10 kΩ	If DVO unconnected, pullup 4.7 kΩ
DCLKREF	Pull-down to VDDQ	4.7 kΩ	If internal gfx not used
LOCLK	Short stub connect to LRCLK		If internal gfx not used
LRCLK	Short stub connect to LOCLK		If internal gfx not used
82801BAM			
HL[11]	Pull-up to 1.8V	10 kΩ	

Signal	Pull-up/Pull-down	Ω	Notes
HL_RCOMP	Pull-up to 1.8V	36.5Ω ± 2%	
IRQ_14	Pull-up to VCC3	8.2 kΩ	
IRQ_15	Pull-up to VCC3	8.2 kΩ	
PIORDY	Pull-up to VCC3	4.7 kΩ	
SIORDY	Pull-up to VCC3	4.7 kΩ	
PDDREQ	Pull-down to GND	5.6 kΩ	
SDDREQ	Pull-down to GND	5.6 kΩ	
PDD7	Pull-down to GND	10 kΩ	
SDD7	Pull-down to GND	10 kΩ	
SMBALERT#/GPI11	Pull-up to 3.3V	4.7 kΩ	Not Used or as Alert on LAN ; if used for GPIO Pull-up depends on loading of GPIO signal
SC_SDATA_IN0	Pull-down to GND	10 kΩ	If not connected to codec
SC_SDATA_IN1	Pull-down to GND	10 kΩ	If not connected to codec
USBP0+	Pull-down to GND	15 kΩ	If unused; if used place on USB side of 15Ω series resistor
USBP0-	Pull-down to GND	15 kΩ	If unused; if used place on USB side of 15Ω series resistor
USBP1+	Pull-down to GND	15 kΩ	If unused; if used place on USB side of 15Ω series resistor
USBP1-	Pull-down to GND	15 kΩ	If unused; if used place on USB side of 15Ω series resistor
USBP2+	Pull-down to GND	15 kΩ	If unused; if used place on USB side of 15Ω series resistor
USBP2-	Pull-down to GND	15 kΩ	If unused; if used place on USB side of 15Ω series resistor
USBP3+	Pull-down to GND	15 kΩ	If unused; if used place on USB side of 15Ω series resistor
USBP3-	Pull-down to GND	15 kΩ	If unused; if used place on USB side of 15Ω series resistor
APICCLK	Pull-down to GND	0	If APIC not used
APICD0	Pull-down to GND	10 kΩ	If APIC not used
APICD1	Pull-down to GND	10 kΩ	If APIC not used
Processor			
BREQ0#	Pull-down to GND	10Ω	
PICD[1:0]	Pull-up to VCCT	150Ω	
TDI	Pull-up to VCCT	150Ω	If ITP/TAP unused pull-down with 1.5 kΩ
TDO	Pull-up to VCCT	150Ω	If ITP/TAP unused leave unconnected

Signal	Pull-up/Pull-down	Ω	Notes
TMS	Pull-up to VCCT	1 kΩ	If ITP/TAP unused pull-down with 1.5 kΩ
TCK	Pull-up to VCCT	1 kΩ	If ITP/TAP unused pull-down with 1.5 kΩ
TRST#	Pull-down to GND	1 kΩ	If ITP/TAP unused pull-down with 1.5 kΩ
PREQ#	Pull-up to VCCT	1.5 kΩ	If unused tie to VCCT
IERR#	Pull-up to VCCT	1.5 kΩ	
INIT#	Pull-up to VCCT	1 kΩ	
PWRGOOD	Pull-up to VCCT	1.5 kΩ	
A20M#	Pull-up to VCCT		Internal to 82801BAM (1.5 kΩ)
IGNNE#	Pull-up to VCCT		Internal to 82801BAM (1.5 kΩ)
FLUSH#	Pull-up to VCCT		Internal to 82801BAM (1.5 kΩ)
FERR#	Pull-up to VCCT		Internal to 82801BAM (1.5 kΩ)
LINT0/INTR	Pull-up to VCCT		Internal to 82801BAM (1.5 kΩ)
LINT1/SMI	Pull-up to VCCT		Internal to 82801BAM (1.5 kΩ)
SLP#	Pull-up to VCCT		Internal to 82801BAM (1.5 kΩ)

Appendix B – 815EM Platform Design Checklist

B.1. Checklist Summary

The following checklist provides design recommendations and guidance for the Intel® Pentium® III processor and Intel® Celeron™ processor systems with 100-MHz SDRAM memory subsystems based on the 815EM chipset. The checklist can be used to ensure all design recommendations in the RDDP (Recommended Design and Debug Practices) have been followed during schematic and layout design reviews.

Please note, unless otherwise specified the default tolerance on resistors is +/-5%. Also note that the (S) reference after power rails such as **VCC3_3 (S)** indicates a switched rail - one that is powered off during S3-S5.

Checklist Sections

- Processor
- 82815EM
- VCH
- 82801BAM
- FWH

B.2. Voltage Rails

Fill in Schematic Name of Voltage Rails on Mark Boxes of when Rails are powered on

Name of Rail	On S0-S1	On S3	On S4	On S5

Note: *Default tolerance for resistors is +/-5% unless otherwise specified

Table 43. Mobile Intel® Pentium® III Processor (B-step)

Signal	System Pull-up/Pull-down	Ω	Series Damping	Notes	✓
Ball P1	Tie to VCC			Recommend Ball P1 be tied to VCC	
BREQ0#	Pull-down to GND	10Ω	N/A		
CPURST#	Pull-up to VCCT	56.2Ω 1 %	N/A		
PICD[1:0]	Pull-up to VCCT	150Ω	N/A		
IERR#	Pull-up to VCCT	1.5 KΩ	N/A	Can be left as NC if not used	
FLUSH#	Pull-up to VCCT	1.5 KΩ	N/A		
FERR#	Pull-up to VCCT	1.5 KΩ	N/A		
PWRGOOD	Pull-up to 2.5V	1.5 KΩ	N/A		
INIT#	None	N/A	N/A	Pull-up internal to 82801BAM	
A20M#	None	N/A	N/A	Pull-up internal to 82801BAM	
IGNNE#	None	N/A	N/A	Pull-up internal to 82801BAM	
LINT0/INTR	None	N/A	N/A	Pull-up internal to 82801BAM	
LINT1/NMI	None	N/A	N/A	Pull-up internal to 82801BAM	
SMI#	None	N/A	N/A	Pull-up internal to 82801BAM	
STPCLK#	None	N/A	N/A	Pull-up internal to 82801BAM	
SLP#	Pull-up to VCCT	1.5 KΩ	N/A	Not used for mobile S1 state	
RTTIMPEDP	Pull-down to GND	56.2Ω 1 %	N/A		
EDGECTRLP	Pull-down to GND	110Ω 1%	N/A		
TESTHI	Pull-up to VCCT	1.5 KΩ	N/A		
TESTLO[2:1]	Pull-down to GND	1 KΩ	N/A		
BSEL1*	TIE to GND	N/A	N/A	100MHz Support Only; 3.3V tolerant	
BSEL0*	Pull-up to VCCT or 3.3V	1.5 KΩ	N/A	100MHz Support Only; 3.3V tolerant	

*BSEL[1:0] can be routed to clock generator for frequency selection, potentially saving jumper/glue logic

Table 44. Mobile Intel® Pentium® III Processor (B-step) ITP – In Target Probe

Signal	System Pull-up/Pull-down	Ω	Series Damping	Notes	✓
TDI	Pull-up to VCCT	150Ω	N/A	If ITP/TAP unused pull-down with 1.5 KΩ	
TDO	Pull-up to VCCT	150Ω	N/A	If ITP/TAP unused leave unconnected	
TMS	Pull-up to VCCT	1 KΩ	47Ω at ITP	If ITP/TAP unused pull-down with 1.5 KΩ	
TCK	Pull-up to VCCT	1 KΩ	47Ω at ITP	If ITP/TAP unused pull-down with 1.5 KΩ	
TRST#	Pull-down to GND	1 KΩ	N/A	If ITP/TAP unused pull-down with 1.5 KΩ	
PREQ#	Pull-up to VCCT	1.5 KΩ	N/A	If unused tie to VCCT	
PRDY#	Pull-up to VCCT	56.2 Ω	240 Ω	Pullup is optional if trace from processor to ITP port is >8”	
RESET#	Pull-up to VCCT	56.2 Ω	240 Ω	Pullup is optional if trace from processor to ITP port is >8”	

Table 45. Mobile Intel® Pentium® III Processor (B-step) PLL RLC Filter

Signal	Value	Notes	✓
R	1 Ω	(optional depending on LC choice) Refer to latest Mobile Intel® Pentium® III Processor EMTS for more details	
L	4.7 uH	Refer to latest Mobile Intel® Pentium® III Processor EMTS for more details	
C	33 uF	Refer to latest Mobile Intel® Pentium® III Processor EMTS for more details	

Table 46. Mobile Intel® Pentium® III ProcessorHigh Frequency Decoupling Recommendations (750Mhz and above frequencies)*

Signal	Capactior Value	QTY	Placement	Notes	✓
VCC	0.68uF_0603 X74	15	Directly under die	Use 2 vias per pwr & gnd pads for reduced inductance during layout	
	2.2uF_0805 X74	24	Place within 800 mils of CPU package		
VCCT	0.1uF_0603	20	Place around die close to VCCT balls		

*All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution.

Table 47. Other Decoupling*

Signal	Capactior Value	QTY	Placement	Notes	✓
VGTLREF	0.1uF	4	Close to processor	(2/3)*VCCT	
		2	Close to 82815EM		
VCLKREF	0.1uF	1	Close to processor	(1/2)*V2_5	
VCMOSREF	0.1uF	2	Close to processor	1.00V	

*All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout & PCB board design into consideration when deciding on their overall decoupling solution.

B.3. CK-815EM Clocking

Table 48. CK-815EM Damping Resistor Recommendations

Signal	Damping Resistor	Notes	✓
CPU[2:0]	33 Ω	18 pF EMI capacitor placed at the processor (For EMI) Route CPU[0] to processor Route CPU[1] to 82815EM Route CPU[2] to ITP if needed	
APIC[1:0]	33 Ω		
3V66[2:0]	33 Ω		
SDRAM[5:0], DCLK	33 Ω		
PCI_FR. PCI[6:1]	33 Ω	PCI_FR must be routed to 82801BAM	
USB	33 Ω		
14MHz REF	33 Ω		
48MHz DOT CLK	33 Ω		
VCH CLK	33 Ω		

B.4. 82815EM

Table 49. 82815EM System Memory Interface

Signal	Series termination	Notes	✓
SMD[63:0]	10 Ω	Place series termination resistor closest to 82815EM	
SMAA[7:4]	10 Ω	Place series termination resistor closest to 82815EM	
SMAB[7:4]#	10 Ω	Place series termination resistor closest to 82815EM	
SMAC[7:4]#	10 Ω	Place series termination resistor closest to 82815EM	

Table 50. 82815EM (External AGP Graphics / Internal Graphics controller)

Signal	System Pull-up/Pull-down	Ω	Notes	✓
PIPE#	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
G_FRAME#	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
G_TRDY#	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
G_IRDY#	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
G_DEVSEL#	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
G_STOP#	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
G_RBF#	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
G_WBF#	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
G_REQ#	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
G_GNT#	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
AD_STB[1:0]	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
SB_STB	Pull-up to VDDQ	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
AD_STB[1:0]#	Pull-down to GND	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
SB_STB#	Pull-down to GND	8.2 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	
G_PAR	Pull-down to GND	100 KΩ	No pull-up or pull down is needed If internal graphic controller is enabled	

Signal	System Pull-up/Pull-down	Ω	Notes	✓
GRCOMP	Pull-down to ground	40 Ω 1%	2/3 of PCB impedance, assuming the PCB impedance is 60 Ω	
AGPREF			0.5 VDDQ if VDDQ is 1.5V. See CRB schematics	
AGP_BUSY#	Pull-up to VCC3_3 (S)	10 KΩ	3.3V tolerant Open Drain Output from 82815EM	

Table 51. 82815EM – GMBUS

Signal	System Pull-up/Pull-down	Ω	Notes	✓
GMCK (Mux'd with WBF#)	Pullup to VCC3_3 (S)	4.7-10 KΩ	Internal Graphics Only. GMBUS is used to interface to VCH only If using external graphics, follow guidelines for AGP_WBF#	
GMDA (Mux'd wioth G_GNT#)	Pullup to VCC3_3 (S)	4.7-10 KΩ	Internal Graphics Only. GMBUS is used to interface VCH only If using external graphics, folllow guidelines for G_GNT#	

Table 52. 82815EM – Digital Video Out (DVO) (Internal Graphics)

Signal	System Pull-up/Pull-down	Ω	Notes	✓
LTVCLKIN (DVOCLKIN)			If not used, 2K pullup required to 1.8V	
LTVCLKOUT[1:0] (DVOCLKOUT[1:0]			If not used, leave unconnected	
LTVDATA[11:0] (DVODATA[11:0])			If not used, leave unconnected	
LTVBLANK# (DVOBLANK)			If not used, leave unconnected	
LTVHSYNC (DVOHSYNC			If not used, leave unconnected	
LTVVSYNC (DVOVSYNC)			If not used, leave unconnected	
LTVCK (DVOI2CLK)	Pull-up to VCC3_3 (S)	4.7-10K KΩ	Open Drain Signal ; See RDDP for layout guidelines; If not used, leave unconnected If not used, pull-up still required	

Signal	System Pull-up/Pull-down	Ω	Notes	✓
LTVDA (DVOI2CDATA)	Pull-up to VCC3_3 (S)	4.7-10K KΩ	Open Drain Signal; See RDDP for layout guidelines; If not used, leave unconnected If not used, pull-up still required	
INTRPT#	Pull-up to VCC3_3(S)	10 KΩ	If not used, pull-up still required	

Table 53. 82815EM – Display Cache (Mux'd with AGP Interface)

Signal	System Pull-up/Pull-down	Ω	Notes	✓
L_FSEL (SBA7)	Pull-down needed for 100 MHz option	10 K Ω	Weak Internal Pull-up resistor for 133MHz(default) recommended	

Table 54. 82815EM – CRT Display Interface (Internal Graphics)

Signal	System Pull-up/Pull-down	Ω	Notes	✓
DDCK, DDDA	Pull-up to 3.3V(S)	10K	Pull-up required for internal and external graphics.	
RED, GREEN, BLUE	Pull-down to GND	75Ω 1%	3.3pF cap, ferrite bead; see below diagram and RDDP for layout guidelines	
HSYNC, VSYNC		N/A	No pull-up and pull-down need	
IREF	Rset Resistor from IREF to IWASTE	174 Ω 1 %	Current Reference for DAC. Do not route high speed signals near Rset. See RDDP for more layout guidelines	
IWASTE	Tie to GND	N/A		

Figure 72: CRT Display Interface

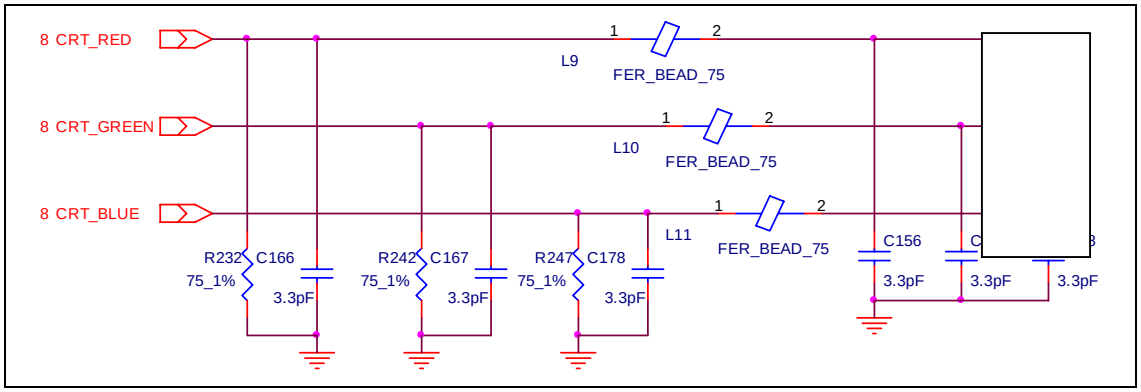


Table 55. 82815EM Impedance Control

Signal	System Pull-up/Pull-down	Ω	Notes	✓
GRCMP	Pull-down to GND	40.2Ω +/–1%	Assumes 60 ohm impedance board	
HLRCOMP	Pull-up to 1.8V(S)	40.2Ω +/–1%	Assumes 60 ohm impedance board. Use 10mil wide, very short (~0.5") trace	
SRCOMP	Pull-up to VCC3_3	40.2Ω +/–1%	Assumes 60 ohm impedance board	
LOCLK LRCLK	RC from LOCLK to LRCLK 10_1% Ω 22pF, 5%, NPO		Align Internal clocks with SDRAM clock flight times – tune to PC Board design; See RDDP for layout guidelines If not using internal graphics may connect LOCLK directly to LRCLK with short trace	

Table 56. 82815EM – Other

Signal	Value	Notes	✓
DCLKREF	4.7K-10K pull-down to GND	Pull-down only needed if using External graphics	
RESERVED (AA6)	N/A	Ball AA6 should be tied to 1.8V	

Table 57. 82815EM – VCCDA RLC Filter

Signal	Value	Notes	✓
L	68nH		
C1	33uF		
C2	0.1uF		

Table 58. 82815EM – Decoupling

Signal	Capacitor Value	QTY	Placement	Notes	✓
V_1.8				See CRB schematics for detail	
VDDQ				See CRB schematics for detail	
VSUS_3.3				See CRB schematics for detail	
VCCDA				See CRB schematics for detail	
VCCDPLL				See CRB schematics for detail	
VCCDACA1, VCCDACA2				See CRB schematics for detail	

Signal	Capacitor Value	QTY	Placement	Notes	✓
VCCBA				See CRB schematics for detail	
VGTLREF				See CRB schematics for detail	
VAGPREF				See CRB schematics for detail	
VHUBREF				See CRB schematics for detail	

Table 59. 82815EM Power-Up Strapping Options

Signal	Strap Description	Strapping Option	Recommended Board Configuration	✓
SBA[7]	Local Memory Frequency Select	High = 133MHz (default) Low = 100 MHz	None. Internal pullup resistor	
SCAS#	Host Frequency	High = Reserved Low = 100 MHz	REQUIRES Pull-down to GND through 10 K	
SMAA[11]	IOQ Depth	High = 4 (default) Low = 1	None. Internal 50K pullup resistor	
SMAA[10]	ALL Z	High = Normal operation Low = All Z	None. Internal 50K pullup resistor	
SMAA[9]	PSB P-MOS Kicker Enable	High = Reserved Low = Intel® Pentium® III processor and Intel® Celeron™ processor support	Pull-down to GND through 10K	
SMAC[5]#	Enable Quick Start Support	High = Stop Graant (default) Low = Quick-start support	Pull-down to GND through 10K	

B.5. VCH

Table 60. VCH – DVO

Signal	Pull-up/Pull-down	Ω	Notes	✓
LCD_VREF	R-Div needed 2.0K 1% with 0.1 uF decoupling cap		*requires specific circuit (see RDDP for details)	

Table 61. VCH – CMOS Panel Interface

Signal	Pull-up/Pull-down	Ω	Notes	✓
P[35:0]	No Connect		Driven low when CMOS panel is disabled	
DE	No Connect		- same -	
FLM	No Connect		- same -	
LP	No Connect		- same -	
SHFCLK	No Connect		Output tristated when CMOS panel is disabled	

VCH – LVDS Panel Interface				
Signal	**Pull-up/Pull-down**	**Ω**	**Notes**	**✓**
YA[3:0][P:M], YB[3:0][P:M]	No Connect		Buffers Disabled	
CLKA[P:M], CLKB[P:M]	No Connect		- same -	
VREF_LO	Pull-down to ground	150 Ω		
VREF_HI	Pull-up to 1.8V (S)	150 Ω		

Table 62. VCH – Digital Video Out Bypass

Signal	System Pull-up/Pull-down	Ω	Notes	✓
DVOrCLKIN	< 2K		This buffer is always in input mode. Pull low if not used	
DVOrCLKOUT[1:0]	No Connect			
DVOrDATA[11:0]	No Connect			
DVOrBLANK#	No Connect			
DVOrVSYNC	No Connect			
DVOrHSYNC	No Connect			
DVOrRCOM	Pull up to VCC_1.8 (S)	36.5 1%	Assume PCB impedance is 55 Ω	

Table 63. VCH – Miscellaneous Signals

Signal	System Pull-up/Pull-down	Ω	Notes	✓
RCOMP (TV_ZCOMP)	Pull-up to 1.8V	36.5 1%	Assume PCB impedance is 55 Ω	
ENABKL	No Connect		In output mode by default	
ENAVDD	No Connect			
ENEXBUF	No Connect			
TESTIN	tie to GND	tie to GND directly		

Table 64. VCH – Decoupling

Signal	Capacitor Value	Quantity	Placement	Notes	✓
PLL_VCC				See CRB schematics	
LVDSpll_VCC				See CRB schematics	
LVDSdc_VCC				See CRB schematics	
VCC_3.3				See CRB schematics	
VCC_1.8				See CRB schematics	

Table 65. VCH – Strapping Options

Signal	Strap Description	Ω	Notes	✓
GPIO[5:2]	Can be used for panel ID	10-4.7 KΩ	Can be used for Panel Select Detect. Default state is GPI with Internal weak pull down.	
GPIO6	For normal VCH operation pin has to be read as low. Note: default setting is for internal pull down	10-4.7 KΩ	Default state is GPI with Internal weak pull down.	
GPIO[8:7]	Used for GMBus base address	10-4.7 KΩ	Used for GMBus address select. Default state is GPI with Internal weak pull down.	

B.6. 82801BAM

Table 66. 82801BAM – PCI/LPC Interface

Signal	System Pull-up/Pull-down	Ω	Notes	✓
DEVSEL#	Pull-up to VCC3_3 (S)	8.2 KΩ		
FRAME#	Pull-up to VCC3_3 (S)	8.2 KΩ		
IRDY#	Pull-up to VCC3_3 (S)	8.2 KΩ		
TRDY#	Pull-up to VCC3_3 (S)	8.2 KΩ		
STOP#	Pull-up to VCC3_3 (S)	8.2 KΩ		
PLOCK#	Pull-up to VCC3_3 (S)	8.2 KΩ		
PERR#	Pull-up to VCC3_3 (S)	8.2 KΩ		
SERR#	Pull-up to VCC3_3 (S)	8.2 KΩ		
CLKRUN#	Pull-up to VCC3_3 (S)	8.2 KΩ		
PME#	None		Internal Pull-up to VCCSUS3_3	
REQ[5:0]#	Pull-up to VCC3_3 (S)	8.2 KΩ		
GNT[5:0]#	None		Actively driven by 82801BAM	
PC/PCI_REQ[B:A]	Pull-up to VCC3_3 (S)	8.2 KΩ		
GNTA#/GPIO16	None		Integrated pull-up Resistor	
GNTB#//GNT5#/GPIO17	None		Integrated pull-up Resistor	
PIRQ[D:A]#	Pull-up to VCC3_3 (S)	8.2 KΩ		
PIRQ#[H,E]#	Pull-up to VCC3_3 (S)	8.2 KΩ	Can no longer be used as GPIOs and requires pull-ups	
PIRQ[G, F]#	Pull-up to VCC3_3 (S)	8.2 KΩ	Can be used as GPIO[4:3]	
THRM#	Pull-up to VCC3_3 (S)	8.2 KΩ		
A20GATE	Pull-up to VCC3_3 (S)	8.2 KΩ		
RCIN#	Pull-up to VCC3_3 (S)	8.2 KΩ		
SERIRQ	Pull-up to VCC3_3 (S)	8.2 KΩ		

Table 67. 82801BAM HUB Interface

Signal	System Pull-up/Pull-down	Ω	Notes	✓
HL[11]	None	NA	Recommend Test Point for debug	
HL_RCOMP	Pull-up to 1.8V (S)	36.5Ω +/–2%	Assumes 55 ohm board impedance. Use 10mil wide, very short (~0.5”) trace	

Table 68. 82801BAM IDE Interface

Signal	System Pull-up/Pull-down	Ω	Notes	✓
IRQ_14	Pull-up to VCC3_3 (S)	8.2 KΩ		
IRQ_15	Pull-up to VCC3_3 (S)	8.2 KΩ		
PIORDY	Pull-up to VCC3_3 (S)	4.7 KΩ	Integrated Series termination resistor	
SIORDY	Pull-up to VCC3_3 (S)	4.7 KΩ	Integrated Series termination resistor	
PDDREQ	None	N/A	Integerated Pull-Down Resistor. Integrated Series termination resistor*	
SDDREQ	None	N/A	Integerated Pull-Down Resistor. Integrated Series termination resistor*	
PDD7	None	N/A	Integerated Pull-Down Resistor. Integrated Series termination resistor*	
SDD7	None	N/A	Integerated Pull-Down Resistor. Integrated Series termination resistor*	
PDIOW#, PDIOR#, PDDACK#, PDA[2:0]. PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#, PDD[15:0], SDD[15:0]	None	N/A	Integrated Series termination resistor (33 Ω nominal but can range from 31-43 ohms)	

Table 69. 82801BAM USB Interface

Signal	Capacitor Filter (place closest to 82801BAM)	Series resistor	Pull-down Resistor (placed on USB side of 15Ω series resistor	Notes	✓
USBP0+	47pF to GND	15 Ω	15 KΩ		
USBP0-	47pF to GND	15 Ω	15 KΩ	Only 15 KΩ pull-down if not used	
USBP1+	47pF to GND	15 Ω	15 KΩ	Only 15 KΩ pull-down if not used	
USBP1-	47pF to GND	15 Ω	15 KΩ	Only 15 KΩ pull-down if not used	
USBP2+	47pF to GND	15 Ω	15 KΩ	Only 15 KΩ pull-down if not used	
USBP2-	47pF to GND	15 Ω	15 KΩ	Only 15 KΩ pull-down if not used	

Signal	Capacitor Filter (place closest to 82801BAM)	Series resistor	Pull-down Resistor (placed on USB side of 15Ω series resistor	Notes	✓
USBP3+	47pF to GND	15 Ω	15 KΩ	Only 15 KΩ pull-down if not used	
USBP3-	47pF to GND	15 Ω	15 KΩ	Only 15 KΩ pull-down if not used	

Figure 73: USB Interface

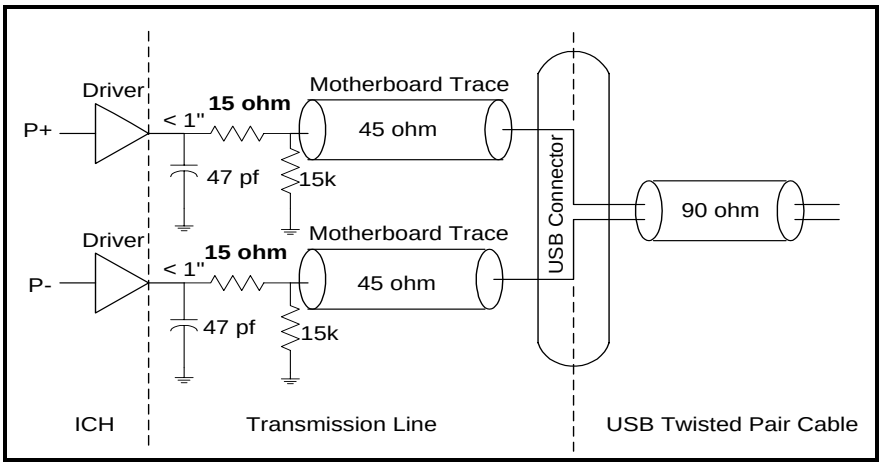


Table 70. 82801BAM LAN

Signal	System Pull-up/Pull-down	Ω	Notes	✓
LAN_CLK	N/A	N/A	Internal Weak Pull-down. Leave unconnected if LAN interface is not used	
LAN_RXD[2:0]	N/A	N/A	Internal Pull-up resistors. Leave unconnected if LAN interface is not used	
LAN_TXD[2:0]	N/A	N/A	Leave unconnected if LAN interface is not used	
LAN_RSTSYNC	N/A	N/A	Leave unconnected if LAN interface is not used	
EE_DIN	N/A	N/A	Internal Weak Pull-up resistor. Leave unconnected if LAN interface is not used	
EE_DOUT	Pull-down to GND	DO NOT POPULATE	Inlcude placeholder for pull-down resistor for a future strapping option. Do not populate the resistor	

Table 71 82801BAM AC'97

Signal	System Pull-up/Pull-down	Ω	Notes	✓
AC_SDATA_IN0	Pull-down to GND	10 KΩ		
AC_SDATA_IN1	Pull-down to GND	10 KΩ		
AC_SYNC	None		Optional 33 Ω series termination resistor	
AC_BIT_CLK	Pull-down to GND	10 KΩ		

Table 72. 82801BAM Other

Signal	System Pull-up/Pull-down	Ω	Notes	✓
RI#	Pull-up to VCCSUS3_3	8.2 KΩ		
PWRBTN#	None	N/A	Internal pull-up resistor	
SMBDATA	Pull-up to VCC3_3(S)	10 KΩ	Pull-up to switched, non-switched, or always rail depending on implementation	
SMBCLK	Pull-up to VCC3_3(S)	10 KΩ	Pull-up to switched, non-switched, or always rail depending on implementation	
SMBALERT#/GPI11	Pull-up to VCC3_3	10 KΩ	Not Used or as Alert on LAN ; if used for GPIO Pull-up depends on loading of GPIO signal	
SMLINK0	Pull-up to VCC3_3	100 KΩ	Pull-up to switched, non-switched, or always rail depending on implementation	
SMLINK1	Pull-up to VCC3_3	100 KΩ	Pull-up to switched, non-switched, or always rail depending on implementation	
INTRUDER#	Pull-up to VCC_RTC	10 KΩ		
GPIO[7:0]	Pull-up to VCC3_3 (S)	10 KΩ	All inputs to 82801BAM must not be left floating. Pull-up unused inputs	
GPIO[8] (UNUSED GPIs)	Pull-up to VCCSUS3_3	10 KΩ	All inputs to 82801BAM must not be left floating. Pull-up unused inputs	
GPIO[13:11] (UNUSED GPIs)	Pull-up to VCCSUS3_3	10 KΩ	All inputs to 82801BAM -Must not be left floating. Pull-up unused inputs	
FS[0]	Include place-holder for pull-down	2 KΩ	RESERVED for future use; DO NOT STUFF. Internal weak pull-up	

Table 73. 82801BAM APIC (NOT RECOMMENDED TO USE)

Signal	System Pull-up/Pull-down	Ω	Notes	✓
APICCLK	Pull-down to GND	0 Ω	APIC is not recommended.	
APICD0	Pull-down to GND	10 KΩ	APIC is not recommended.	
APICD1	Pull-down to GND	10 KΩ	APIC is not recommended.	

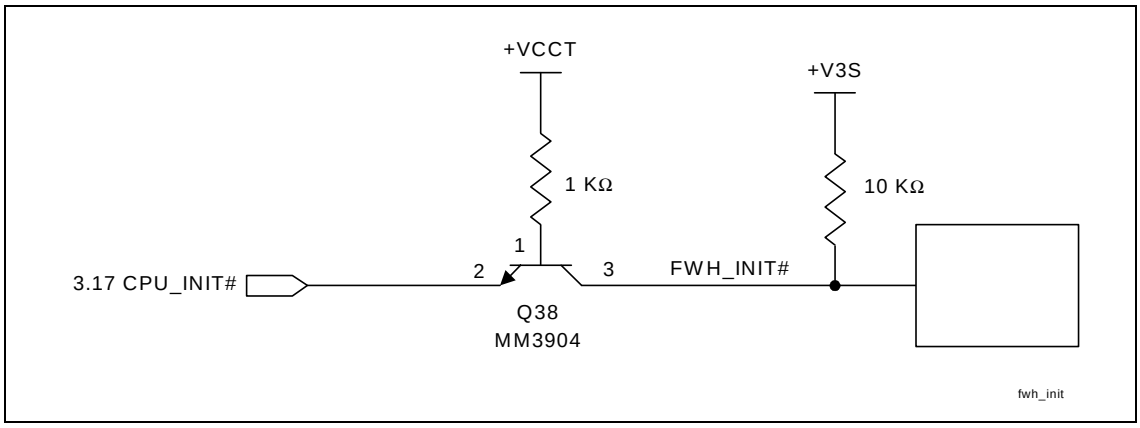
82801BAM Power-Up Strapping Options				
Signal	**Strap Description**	**Strapping Option**	**Recommended Board Configuration**	**✓**
AC_SDOUT	Safe Mode	High = safe mode **Low = Normal (Default)**	None. Internal pull-down	
EE_DOUT	Reserved	Include place-holder for pull-down	Pull-down to GND but do not populate	✓
FS[0]	Reserved	Include place-holder for pull-down	Pull-down to GND but do not populate	✓
GNT[A]#	Top Swap Overrride	**High = Normal (default)** Low = Top-Swap	None. Internal pullup resistor	
HLCOMP	Enhanced Hub Interface	High = Normal Low = Enhanced Hub	Extermal pull-up required	✓
SPKR	No Reboot	**High = enabled (default)** Low = No Reboot mode/TCO	None. Internal pullup resistor	

B.7. FWH

Table 74. FWH

Signal	System Pull-up/Pull-down	Ω	Notes	✓
INIT#	Pull-up to VCC3.3 (S) at FWH	10 KΩ	Need NPN3904 transistor for voltage translation to FWH	
IC	None	N/A	Internal Pull-down enables normal FWH operation	
FWH[3:0]/LAD[3:0]	None	N/A	Integrated pullup resistors	
LDRQ[1:0]#	None	N/A	Integrated pullup resistors	
FGPIO[4:0]	Pull-down to GND	10K	Needed Only if GPI is Unused	

Figure 74: Initialization Circuitry of FWH

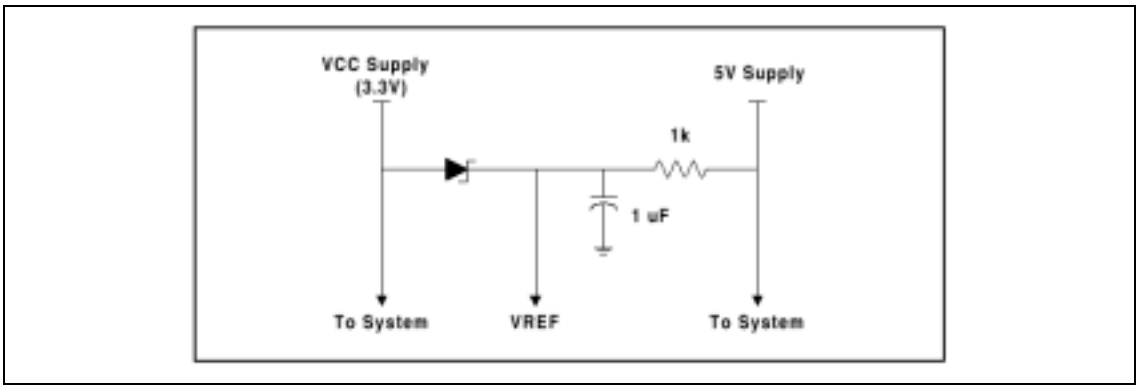


B.8. Voltage Rails

Table 75. Voltage Rails

Signal		Notes	✓
VCC_CPU[1:0]	Tie to VCCT equivalent power supply. Use one .1uF decoupling cap.	Used to pull up all CPU I/F signals.	
VccRTC	No clear CMOS jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safemode strapping for Clear CMOS		
Vcc3.3V	**Requires six .1uF decoupling caps**		
VccSus3.3V	Requires one .1uF decoupling cap.		
Vcc1.8V	Requires two .1uF decoupling caps.		
VccSus1.8V	**Requires one .1uF decoupling cap.**		
5V_REF SUS	**Requires one .1uF decoupling cap.**		
5V_REF	5VREF is the reference voltage for 5V tolerant inputs in the 82801BAM Tied to pins VREF[2:1] 5VREF must power up before or simultaneous to Vcc3_3. It must power down after or simultaneous to Vcc3_3.b	Refer to Figure 75 below for an example circuit schematic that may be used to ensure the proper 5VREF sequencing.	

Figure 75: Example Schematics for Proper 5VREF Sequencing

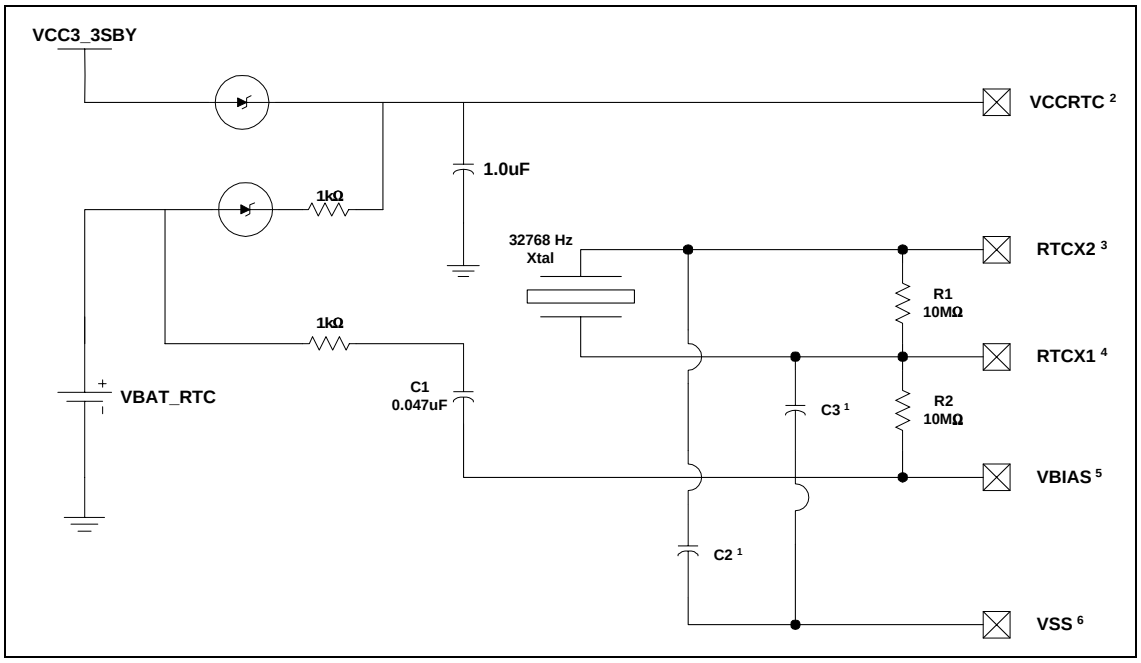


B.9. RTC

Table 76. RTC

Signal		Notes	✓
VBIAS	The VBIAS pin of the 82801BAM is connected to a .047uF cap. See Figure 76.		
RTCX1 RTCX2	Connect a 32.768kHz Crystal Oscillator across these pins with a 10MΩ resistor and use 12pF decoupling caps at each signal. The 82801BAM implements new internal oscillator circuit as compared with the PIIX4 to reduce power consumption. The external circuitry shown in The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100mV will temporarily shut off the oscillator for hundreds of milliseconds.	Figure 76 below will be required to maintain the accuracy of the RTC.	

Figure 76: 82801BAM Oscillator Circuitry



*Capacitors C2 and C3 are crystal Dependent

B.10. IMVP

For designs implementing the IMVP solution, please fill out the chart below. The information will be used along with the schematics to provide the appropriate IMVP design feedback.

Table 77. System Design Targets

IMVP Vendor	Vendor
Maximum Processor Speed Target	CPU MHz
Maximum Processor Current	ICCMAX =
Maximum Processor DC Voltage	VCCDCMAX =
Typical Processor VCC	VCCTYP =
Maximum DC Input Voltage (AC/DC)	VDCMAX =
Minimum DC Input Voltage (AC/DC)	VDCMIN =

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