Product Brief

Intel® 3100 Chipset

Embedded Computing

Intel® 3100 Chipset

for Intel® Core™2 Duo Processors, Intel® Core™ Duo Processors and Intel® Celeron® M Processors on 65nm

Product Overview

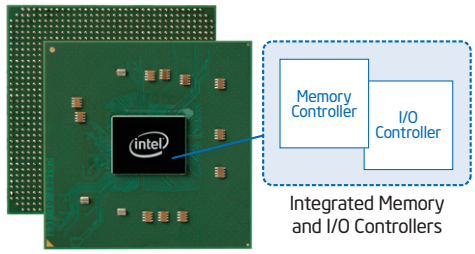
The Intel® 3100 chipset combines server-class memory and I/O controller functions into a single component, creating the first integrated Intel® chipset specifically optimized for embedded, communications, and storage applications. This single-chip system controller replaces a separate memory controller hub and I/O controller hub, significantly conserving board real estate and power consumption.

The Intel 3100 chipset supports the following processors, addressing the needs of high-performance, low-power platforms within small form factor designs such as PrAMC, Compact PCI,* and COM Express*:

- Intel® Core™2 Duo processor L7400Δ with 667 MHz front-side bus (FSB) and 17 watts thermal design power (TDP)
- Intel® Core™2 Duo processor U7500Δ with 533 MHz FSB and 10 watts TDP
- Intel® Core™ Duo processor U2500Δ with 533 MHz FSB and 9 watts TDP
- Intel® Celeron® M processor Ultra Low Voltage 423Δ with 533 MHz FSB and 5.5 watts TDP

Intel Core 2 Duo processors are based on Intel® Core™ microarchitecture with support for Intel® 64 architecture[1] and 36 bits of physical addressing, delivering breakthrough, energy-efficient performance to help equipment manufacturers optimally balance processing capabilities within power and space constraints. Intel Core Duo processors are derived from the Intel® Pentium® M processor with significant hardware architecture enhancements in stack management, instruction execution, and branch prediction. Intel Celeron M processors, based on 65nm process technology, provide a value-sensitive single-core solution. These processors, when paired with the Intel 3100 chipset, provide an ideal solution for a wide range of performance-intensive, thermally sensitive, embedded, communications and storage applications.

Along with a strong ecosystem of hardware and software vendors, including members of the Intel® Communications Alliance (intel.com/go/ica), Intel helps cost-effectively meet development challenges and speed time-to-market.



Integrated Memory and I/O Controllers

PCI Express*

For demanding I/O and networking applications, PCI Express* interfaces attach a variety of Intel and third-party I/O solution components and adapters directly to the Intel 3100 chipset (one x8 PCI Express interface and one x4 PCI Express interface). Each interface may be bifurcated to provide additional configuration flexibility. The interfaces provide throughput speeds of up to 4 GB/s on the x8 interface, and up to 2 GB/s on the x4 interface, allowing I/O to keep pace with the rest of the platform.

Memory

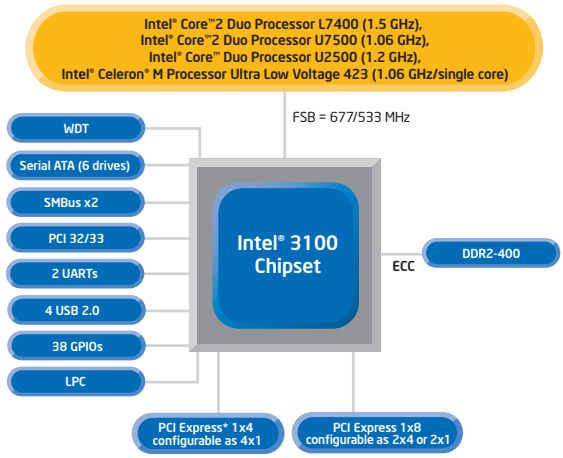
Intel 3100 chipset-based platforms are ECC-enabled and support single-channel DDR2-400 memory (up to 16 GB), which is ideal for storage and memory-intensive applications. The memory subsystem interface supports up to four ranks for a total system bandwidth of 3.2 GB/s.

Data Protection

The Intel 3100 chipset is designed to bring enterprise-level reliability, availability, serviceability, usability, and manageability (RASUM) to the embedded platform. The chipset supports FSB parity and two bits of parity on 64 bits of data on internal buses. The PCI Express interface supports 32-bit cyclic redundancy check (CRC) for detection and automatic recovery of transient signaling errors. Memory interface supports Single Error Correct/Double Error Detect (SEC/DED) ECC and auto retry on uncorrectable errors, and integrates a hardware memory scrubber to scan the populated memory space, proactively seeking out soft errors in the memory subsystem.

Enhanced Direct Memory Access (EDMA)

A four-channel EDMA controller efficiently moves data within local system memory or from the local system memory to the I/O subsystem. Each EDMA channel provides low-latency, high-throughput data transfer capability with no CPU intervention for higher overall system performance. These transfers may be individually designated to be coherent (snooped on the FSB) or non-coherent (not snooped on the FSB), providing improvements in system performance and utilization when cache coherence is managed by software rather than hardware. EDMA also enables quality of service by prioritization of data.



Features	Benefits
Supports Intel® Core™2 Duo processor L7400[Δ], Intel® Core™2 Duo processor U7500,[Δ] and Intel® Core™ Duo processor U2500[Δ]	▪ Two high-performance cores per platform meet the needs of high-performance, low-power applications with small form-factor constraints. Intel Core 2 Duo processor offers additional performance improvement with Intel® 64 architecture,[1] 36 bits of physical address, and SSE3 instruction.
Supports Intel® Celeron® M processor Ultra Low Voltage 423[Δ]	▪ Single-core solution offers scalable performance and value
40 mm x 40 mm FC-BGA package	▪ Requires 50% less board space than prior-generation two-chip chipsets[2]
PCI Express*	▪ Direct connection between the Intel® 3100 chipset and PCI Express component/adapters; bandwidth up to 4 GB/s on the x8 PCI Express interface; higher bandwidth and less I/O bottlenecks than PCI-X
DDR2-400 memory interface	▪ Maximum memory bandwidth of 3.2 GB/s ▪ Decreased power consumption – especially important on dense rack, hot-plug controller, and blade configurations
Advanced Platform RAS	▪ Memory ECC, SEC/DED, and DIMM scrubbing can improve system reliability ▪ 32-bit ECRC on PCI Express ▪ Hot-swap PCI Express enhances serviceability ▪ SMBus port hooks for remote management operation and support for a variety of third-party base management controller and BIOS solutions
GPIO	▪ 38 pins (25 dedicated, 13 mux'ed)
USB 2.0	▪ One USB 2.0 host controller with a total of four ports ▪ Supports wakeup from sleeping in S3 and S5 states
Two integrated UARTs (serial ports)	▪ Supports full function of a standard 16550 UART, including hardware flow control interface
32/33-bit PCI bus interface	▪ Supports PCI Rev 2.3 specification at 33 MHz ▪ Supports two request/grant pairs
SMBus x2	▪ First SMBus dedicated as slave; second configurable as master or slave
Integrated Serial ATA host controllers	▪ Six ports provide independent DMA operation in AHCI mode, four ports support in SATA 1.0a mode
Watchdog timer	▪ Multiple modes (WDT and free-running)
Power management	▪ ACPI 2.0 support

Product Number	Product Code	Thermal Design Power	Package
Intel® 3100 chipset	LE3100MICH	10.4 – 12.4W	1284 Flip Chip-Ball Grid Array (FC-BGA3)

[Δ]Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See www.intel.com/products/processor_number for details.

[1]64-bit computing on Intel architecture requires a computer system with a processor, chipset, BIOS, operating system, device drivers, and applications enabled for Intel® 64 architecture. Performance will vary depending on your hardware and software configurations. Consult with your system vendor for more information.

[2]Comparison with Intel® E7520 Memory Controller Hub plus Intel® 6300ESB I/O Controller Hub.

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