Intel® Pentium® M Processor and Intel® 855PM Chipset DDR 333/266/200 MHz Platform

Design Guide Update

April 2005

Notice: The Intel® 855PM chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the *Intel® 855PM Chipset Datasheet Specification Update*.

Document Number: 253479-003

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial release	July 2003
-002	Updates include: • Added revised wireless design recommendations	September 2003
-003	Updates include: • Clarification to USB ESD protection	March 2005

Preface

This Design Guide Update document is an update to the information contained in the *Intel® Pentium® M Processor and Intel® 855PM DDR 266/200 MHz Chipset Platform Design Guide*, March 2003, Document Number 252614-001. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2003. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public design guide update document when the public design guide document is first published. This design guide update document contains a complete list of all known information types. However, only the detail for new material is included in this document. Both the public design guide document and this design guide update document are required to allow the users to have a complete list of information types and the associated details. This design guide update document will contain information that has not been previously published.

Affected Documents

Document Title/ Document Number	Document Location
Intel® Pentium® M Processor and Intel® 855PM DDR 266/200 MHz Chipset Platform Design Guide, 252614-003	http://www.intel.com/design/mobile/desguide/252614.htm

Related Documents

Document Title	Document Number
Intel® 855PM Chipset Memory Controller Hub (MCH) Datasheet	http://www.intel.com/design/chipsets/datashts/252613.htm
Intel® 855PM Chipset Memory Controller Hub (MCH) Specification Update	http://www.intel.com/design/chipsets/specupdt/253488.htm
Intel® 82801DB I/O Controller Hub 4 Mobile (ICH4-M) Datasheet	http://www.intel.com/design/mobile/datashts/252337.htm
Intel® 82801DB I/O Controller Hub 4 Mobile (ICH4-M) Datasheet Specification Update	http://www.intel.com/design/chipsets/specupdt/252663.htm

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel 855PM chipset.

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Summary Tables of Changes

Codes Used in Summary Table

Doc:	Document change or update that will be implemented.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
1	Doc	Updated design guidelines for supporting PC2700 (333MHz) DDR SDRAM
2	Doc	Transition from Intel 855PM DDR 266/200 MHz Chipset to Intel 855PM DDR 333/266/200 MHz Chipset Design Guidelines
3	Doc	System Memory SMVREF Design Update
4	Doc	Intel® PRO/Wireless 2100 and Bluetooth Design Requirements

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	PSB to FSB nomenclature Change
2	Doc	High-density Memory Support Update
3	Doc	Clarification on USB ESD protection

§

General Design Considerations

1. Updated Design Guidelines for Supporting PC2700 (333 MHz) DDR SDRAM

The latest stepping of the Intel 855PM chipset MCH (S-Spec#) includes the capability of supporting PC2700 Double Data Rate (DDR) SDRAM with a nominal data rate of 333 MT/s. Update to the current PC1600 and PC2100 layout guidelines is required to sustain the higher data transfer rate. For a **new** design that plans to support PC1600, PC2100, and PC2700 DDR SDRAM, Table 25 "Data Signal Group Routing Guidelines," of the Design Guide should be updated as follows:

Table 25. Data Signal Group Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	Data – SDQ[71:0], SDQS[8:0]		1
Motherboard Topology	Daisy Chain with Parallel Termination		
Reference Plane	Ground Referenced		
Characteristic Trace Impedance (Zo)	55 Ω ±15%		
Trace Width	Inner layers: 4 mils Outer layers: 5 mils		
Trace to Space ratio	1:2 (e.g. 4 mil trace to 8 mil space)		6
Group Spacing	Isolation spacing for non-DDR related signals = 20 mils minimum		
Trace Length L1 – MCH Signal Ball to Series Termination Resistor Pad	Min = 0.5" Max = 3.75"	Figure 74	3, 5
Trace Length L2 – Series Termination Resistor Pad to First SO-DIMM Pad	Max = 0.75"	Figure 74	3
Trace Length L3 – First SO-DIMM Pad to Last SO-DIMM Pad	Max = 1.0"	Figure 74	3
Trace Length L4 – Last SO-DIMM Pad to Parallel Termination Resistor Pad	Max = 0.80"	Figure 74	
Overall routing length from 855PM MCH to last SO-DIMM Pad– L1+Rs+L2+L3 (required for DDR333 support)	**Min = 0.5"** **Max= 4.5"**		
Series Termination Resistor (Rs)	10 Ω ± 5%		
Parallel Termination Resistor (Rt)	56 Ω ± 5%		
Maximum Recommended Motherboard Via Count Per Signal	6		2, 4
Length Matching Requirements	• SDQ[71:0] to SDQS[8:0] • SDQS[8:0] to SCK/SCK#[5:0] • See Section 6.2.1for details		

NOTES:

1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using 4 vias if trace length L2 is routed on same external layer as SO-DIMM0 and a via is shared between SO-DIMM1 and parallel termination resistor.
5. L1 trace length does not include MCH-M package length and should not be used when calculating L1 length.
6. Implementing a space to trace ratio of 3:1 (e.g. 12-mil space to 4-mil trace) for DQS[8:0] will produce a design with increased timing margins.

For designs based on existing layout guidelines supporting PC1600 and PC2100 DDR SDRAM, the current platform may be able to support PC2700 as is or with minor modifications. Consult General Design Considerations #2 for more details

2. Transition from Intel® 855PM DDR 266/200 MHz Chipset to Intel® 855PM DDR 333/266/200 MHz Chipset Design Guidelines

For designs based on existing layout guidelines supporting PC1600 and PC2100 DDR SDRAM, the current platform may be able to support PC2700 as is. Otherwise, it is possible to extend platform support for PC2700 with minor modifications.

Recommended design option to support PC2700 with existing platforms based on PC1600/PC2100 layout guidelines is summarized below.

The following should be included as a new section, Section 6.2.7, in the Design Guide.

6.2.7 Recommended Design Option to Support PC2700 DDR SDRAM with Existing Intel® 855PM Platforms

The following sections document the currently available design option for enabling PC2700 DDR SDRAM support based on existing platform layouts.

6.2.7.1 Shortened Data Signal Group Trace Length

Modifications to current platforms to support PC2700 are possible by reducing the overall motherboard trace length for the data signal group if current trace lengths exceed the PC2700 trace length guidelines. This includes all DDR data signals, SDQ[71:0], and data strobe signals, SDQS[8:0].

Design guidelines for supporting PC2700 based on an existing PC1600 and PC2100 layout are presented in Section 6.2.7.1.1. A list of general design considerations for adapting current platforms to support PC2700 is summarized in Section 6.2.7.1.2.

6.2.7.1.1 Supporting PC2700 Based on an Existing PC Platform Layout

While the maximum length of L1, L2, L3, and L4 remains unchanged from previous revisions of this design guide, the maximum overall length allowed from the MCH-M to the second SO-DIMM (L1 + Rs + L2 + L3) for PC2700 support is limited to 4.5 inches**. This represents a reduction of 1.0 inches compared to that allowed for PC2100 and PC1600 design guidelines**. As a result, platforms based on current PC2100 and PC1600 layout guidelines may require a reduction in trace lengths of up to 1.0 inches, in order to meet the PC2700 maximum data signal group length requirements.

Figure 91. Data Signal Group (SDQ[71:0], SDQS[8:0]) Routing Topology – PC2700, PC2100 and PC1600 Compliant

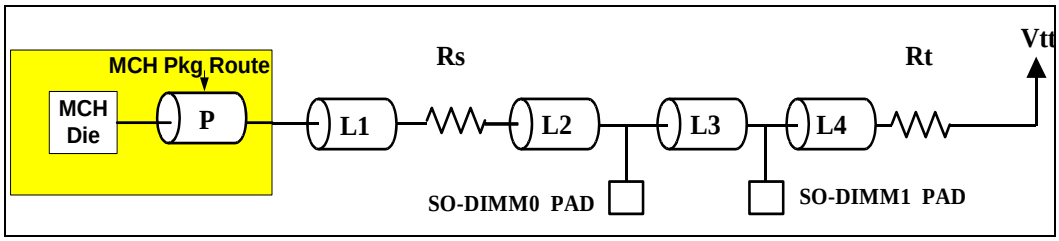


Table 33. Data Signal Group (SDQ[71:0], SDQS[8:0]) Routing Guidelines – PC2700, PC2100 and PC1600 Compliant

	L1	L2	L3	L4	Rs	Rt	L1 + Rs + L2 + L3
DDR Data Signal Group (for platform supporting PC2700, PC2100, PC1600 DDR SDRAM)	Min = 0.5” Max = 3.75”	Min = 0” Max = 0.75”	Min = 0” Max = 1.0”	Min = 0” Max = 0.8”	22.6 Ω ± 1%	54.9 Ω ± 1%	**Min = 0.5”** **Max = 4.5**”
DDR Data Signal Group (for platform supporting PC2100 and PC1600 DDR SDRAM)	Min = 0.5” Max = 3.75”	Min = 0” Max = 0.75”	Min = 0” Max = 1.0”	Min = 0” Max = 0.8”	22.6 Ω ± 1%	54.9 Ω ± 1%	Min = 0.5” Max =5.5”

6.2.7.1.2 Additional Design Considerations for Adapting Intel® 855PM DDR 200/266 MHz Platforms to Support PC2700

In addition to meeting the updated routing length requirements specified in Section 6.2.7.1, future DDR 333-MHz platforms must also adhere to all other existing design guidelines for the DDR 200-MHz and 266-MHz platforms. Table34 contains section references to all other existing design guidelines that need to be followed for the different signal groups.

Table 34. Existing PC2100/PC1600 DDR SDRAM Design Guidelines Required for PC2700 Support

Group	Signal	Section Reference
Data	SDQ[71:0]; SDQS[8:0]	6.2.1
Control	SCKE[3:0]; SCS#[3:0]	6.2.2
Command	SMA[12:0]; SBS[1:0]; SRAS#; SCAS#; SWE#	6.2.3
Clock	SCK[5:0]; SCK#[5:0]	6.2.4
Feedback	RCVENOUT#; RCVENIN#	6.2.5

.

3. System Memory SMVREF Design Update

SMVREF is required to be powered ON during S3. Without valid SMVREF to MCH, CKE lines may float high during S3. The second paragraph of Section 11.5.6 “DDR SMRCOMP and VTT 1.25-V Supply Disable in S3/Suspend” should be updated as follows:

SMRCOMP and VTT 1.25-V supplies can be disabled during the S3 suspend state to further save power on the platform. This is possible because the MCH does not require resistive compensation during suspend. However, the 2.5-V VCCSM power pins of the MCH, the **SMVREF** pin of the MCH, and the VDD power pins of the DDR memory devices are required to be on in S3 state.

4. Intel® PRO/Wireless 2100 and Bluetooth* Design Requirements

Replace Section 12, *Intel PRO/Wireless Network Connection – Bluetooth Coexistence Interface Design Requirements*, with the following:

12. Intel® PRO/Wireless 2100 and Bluetooth* Design Requirements

This section describes the design requirements needed to interface an Intel 802.11 wireless LAN device (Intel® PRO/Wireless 2100 family) to a Bluetooth module of choice that supports Intel’s Wireless Coexistence System (WCS) specification. Other requirements for supporting Intel PRO/Wireless and Bluetooth features are also addressed. The following topics are covered in this section:

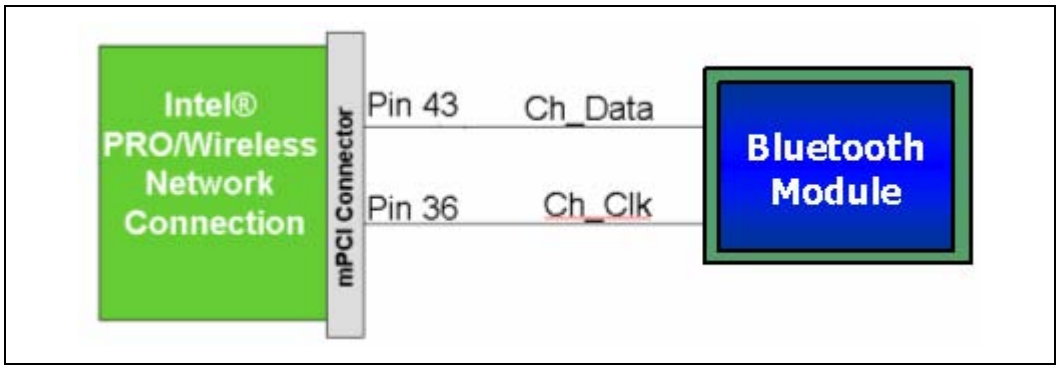
1. PCB interface requirements
2. DC power requirements for Bluetooth
3. Selective Suspend support requirements
4. Wake on Bluetooth support requirements
5. RF Disable support requirements for Intel PRO/Wireless and Bluetooth Devices

Detailed information about the coexistence specification is provided in the *RS - Intel® Centrino™ Mobile Technology Coexistence System Specification* (reference number 11823).

12.1 PCB Interface Requirements

Two PCB traces shall be used to carry channel number and clock signals between Bluetooth and Intel PRO/Wireless 2100. Although these traces do not need to match any length, width or impedance constraints a typical width of 5 mils and spacing of 5 mils is recommended. Pin # 43 of the mPCI connector needs to be routed to the Channel_Data signal of the Bluetooth module. Pin # 36 of the mPCI connector needs to be routed to the Channel_Clock signal of the Bluetooth module. The Channel_Data and Channel_Clock pins on the Bluetooth module are vendor specific. Please refer to the corresponding Bluetooth module vendor for this information. The traces between Calexico and Bluetooth are a point-to-point connection and do not require any intervening components.

Figure 1. Recommended Topology for Coexistence Traces



12.2 DC Power Requirements for Bluetooth*

Voltage levels to power Bluetooth modules are vendor specific. Typical voltage requirement to power Bluetooth module is 3.3Vwith 2% tolerance. This source may be derived from any power rail available on the platform capable of providing the Bluetooth module power requirements. Please note that if implementing Wake on Bluetooth or Selective Suspend an appropriate power rail should be selected. See Section 0, 12.3 Selective Suspend Support and Section 0, 12.4 Wake on Bluetooth* Requirements for details. The Fishhook reference board provides multiple power delivery solutions for the Bluetooth module including a 3.3-V source from the CRB and a 3.3-V source derived from the 5-V USB power rail.

12.3 Selective Suspend Support

USB based Bluetooth modules that plan to support the Microsoft Selective Suspend feature must be self-powered. Selective Suspend allows the processor to enter the C3/C4 state with the presence of a USB based Bluetooth module. The USB power rail is not a sufficient source for a self-powered module. The power rail must be always on in system states S0, S1 and S2 for a self-powered device. Generally it is recommended for all internal USB devices (in this case the Bluetooth module) to self-powered for best power efficiency and to be capable of waking up the system. For more information refer to:

"Power saving of using USB selective Suspend Support" published in
http://www.intel.com/design/mobile/platform/downloads/Power_Saving_USB_Selective_Suspend.pdf

12.4 Wake on Bluetooth* Requirements

WoBT (Wake on Bluetooth) provides a method for the Bluetooth module to wake the system upon Bluetooth device activity. This functionality is similar to Wake on LAN. Support for WoBT requires the device to be self-powered and the power rail to be always on in system states S0-S4. The same signal used for WOL (Wake on LAN) is planned for use by the WoBT signal. This is a point to point interface and does not require any interface logic. There are no trace length or spacing requirements for this low speed signal. Further information is TBD.

12.5 RF Disable Support Requirements for Calexico and Bluetooth* Devices

The RF Disable interface to the Calexico module occurs via pin 13 of the mini-PCI connector. This interface provides support to disable the Calexico radio through methods including, but not limited to, an external mechanical switch or button on the notebook or through an embedded controller. This is an active low signal which provides the ability to disable the RF portions of Calexico. The Calexico radio remains disabled until RF_KILL# is unasserted Further information is TBD.

§

Documentation Changes

1. Processor System Bus (PSB) to Front Side Bus (FSB) Nomenclature Change

The interface between the Intel Pentium M processor and Intel 855PM Memory Controller Hub (MCH) will be referred to as the FSB instead of PSB, in Intel future collateral. This is purely a nomenclature change to ensure consistent usage across Intel product lines.

2. High-Density Memory Support Update

The 855PM chipset architecture supports 2-GB of system memory using "DDP stacked" memory devices as well as other high density memory devices based on various package configurations. In summary, Section 6.2.4.2 of the Design Guide should be updated as follows:

6.2.4.2 Intel® 855PM Chipset High Density Memory Support

The 855PM chipset architecture supports 2-GB of system memory. This memory capacity can be achieved using "high-density" memory devices of various package types. Intel has done only limited simulation and bench testing on these high-density SO-DIMM memory modules and has not seen any functional or analog inspection failures using existing layout guidelines. Due to a lack of JEDEC standard for high density memory; however, Intel has not done complete simulation or validation with all the available package configurations. Customers are strongly encouraged to perform complete validation on their platforms based on the particular high-density memory package of their choice.

3. Clarification on USB ESD Protection

Added reference to USB ESD Application Note.

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. ESD protection is needed for USB lines. Refer to the *Intel® ICH Family USB ESD Considerations Application Note* for ESD protection implementation guidelines. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 108. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, Intel recommends including footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.