Intel® Pentium® M Processor and Intel® 855GM/GME Chipset Platform

Design Guide Update

August 2005

Notice: The Intel® 855GM chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 253176-004

Contents

Revision History

Revision Number.	Description	Revision Date
-001	Updates include: • Memory SMVREF design update • Correction on buffer pinout/connection for CRT VSYNC/HSYNC • Figure reference update for “Processor RESET# Routing Examples” • Clarification on CPURST# pull-up resistor value at ITP connector • Correction on HLSTB signal name • Figure reference update for “Start Up Conditions and Logic Protection” for Wireless/Bluetooth coexistence interface design. • High-density memory support update • CRT VSYNC/HSYNC design update	May, 2003
-002	Updates include: Clarification on Host Clock (BCLK) CPU package length	December 2004
-003	Updates include: • Clarification on USB ESD protection	April 2005
-004	Updates include: • Correction on PCICLK trace length matching	August 2005

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Preface

This Design Guide Update document is an update to the specifications and information contained in the *Intel® Pentium® M Processor and Intel® 855GM Chipset Platform Design Guide*, Document Number 252616. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2003. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public design guide update document when the public design guide document is first published. This design guide update document contains a complete list of all known information types. However, only the detail for new material is included in this document. Both the public design guide document and this design guide update document are required to allow the users to have a complete list of information types and the associated details. This design guide update document will contain information that has not been previously published.

Affected Documents

Document Title/Document Number	Document Location
Intel® Pentium® M Processor and Intel® 855GM/GME Chipset Platform Design Guide, 252616-004	252616

Related Documents

Document Title	Document Location
Intel® 855GM Chipset Graphics and Memory Controller Hub (GMCH) Datasheet	252615
Intel® 82801DB I/O Controller Hub 4 Mobile (ICH4-M) Datasheet	252337

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 855GM chipset.

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Summary Tables of Changes

Codes Used in Summary Table

Doc:	Document change or update that will be implemented.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
1	Doc	System Memory SMVREF Design Update

NO.	Plans	SCHEMATIC, LAYOUT, AND ROUTING UPDATES
1	Doc	Correction on Buffer Pin-Out/Connection for CRT VSYNC/HSYNC

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Figure Reference Update for “Processor RESET# Routing Examples”
2	Doc	Clarification on CPURST# Pull-Up Resistor Value at ITP Connector
3	Doc	Correction on HLSTB Signal Name
4	Doc	Figure reference Update for “Start Up Conditions and Logic Protection” for Wireless/Bluetooth Coexistence Interface Design
5	Doc	High-density Memory Support Update
6	Doc	CRT VSYNC/HSYNC Design Update
7	Doc	Clarification on Host Clock (BCLK) CPU package length
8	Doc	Clarification on USB ESD protection
9	Doc	Correction on PCICLK Trace Length Matching

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General Design Considerations

1. System Memory SMVREF Design Update

SMVREF is required to be on during S3. Without valid SMVREF to GMCH, CKE lines may float high during S3. Section 11.5.3.5 “DDR SMRCOMP and VTT 1.25-V Supply Disable in S3/Suspend” should be updated as follows:

SMRCOMP and VTT 1.25-V supplies can be disabled during the S3 suspend state to further save power on the platform. This is possible because the GMCH does not require resistive compensation during suspend. However, the 2.5-V VCCSM power pins of the GMCH, the **SMVREF** pin of the GMCH, and the VDD power pins of the DDR memory devices are required to be on in S3 state. Note that **some DDR memory devices may or may not require a valid reference voltage during suspend.** It is the responsibility of the system designer to ensure that requirements of the DDR memory devices are met.

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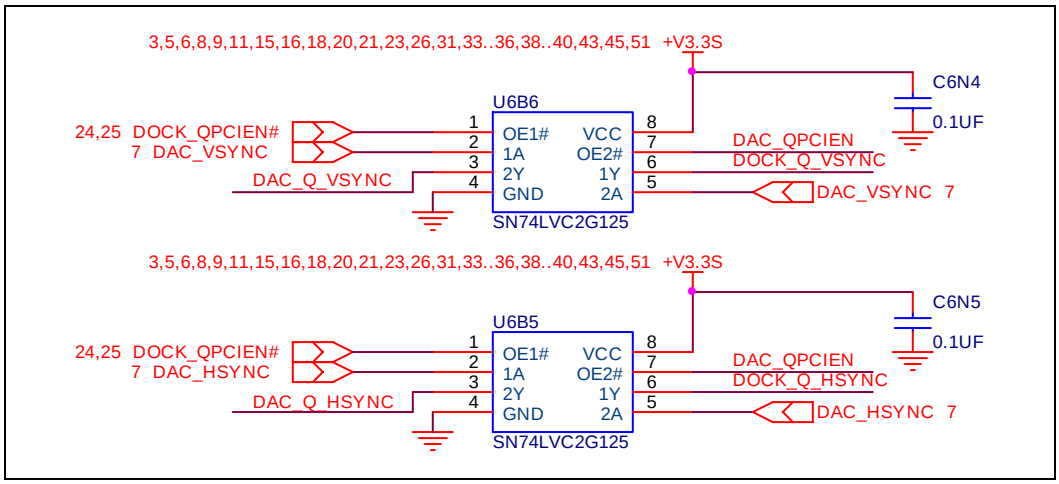
Schematic, Layout, and Routing Updates

1. Correction on Buffer Pinout/Connection for CRT VSYNC/HSYNC

Schematic net connections for CRT VSYNC/HSYNC to onboard VGA connector and docking connector via SN74LVC2G125 should be corrected as follows (schematics sheet 17).



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Documentation Changes

1. Figure Reference Update for "Processor RESET# Routing Examples"

In Section 4.1.5.1, the figure reference for this section should be Figure 19 (instead of Figure 18) as follows:

Figure 19 illustrates a board routing example for the RESET# signal with an ITP700FLEX debug port implemented. It illustrates how the CPURST# pin of GMCH forks out into two branches on Layer 6 of the motherboard. One branch is routed directly to the processor RESET# pin amongst the rest of the common clock signals. Another branch routes below the address signals and vias down to the secondary side that route to the Rs and Rtt resistors. These resistors are placed in the vicinity of the ITP700FLEX debug port.

2. Clarification on CPURST# Pull-up Resistor Value at ITP Connector

CPURST# pull-up resistor value at ITP connector should be 220 Ω ± *5%*. The appropriate paragraph in Section 4.3.1 should be corrected as follows:

Note: Value shown in Table 17, Table 19, and Figure 28 is correct.

As explained in Sections 4.1.5, the RESET# signal forks (see Figure 17) out from the GMCH's CPURST# pin and is routed to the processor and ITP700FLEX debug port. One branch from the fork connects to the processor's RESET# pin and the second branch connects to a **220 Ω ± 5%** termination pull-up resistor to VCCP placed close to the ITP700FLEX debug port. A series 22.6 Ω ± 1% resistor is used to continue the path to the ITP700FLEX RESET# pin with the RESETITP# net in Figure 28. The length of the RESETITP# net (labeled as net L4) should be limited to be less than 0.5 inches.

3. Correction on HLSTB Signal Name

Hub interface strobe names listed in Table 50 should be "HLSTB."

Table 1. Hub Interface Signals Internal Layer Routing Summary

Signal	Min length (inch)	Max length (inch)	Width (mils)	Space (mils)	Mismatch length (mils)	Relative To	Space with other signals (mils)	Notes
HL[10:0]	1.5"	6"	4	8	± 100	Differential **HLSTB** pair	20	
HLSTB HLSTB#	1.5"	6"	4	8	± 100	Data lines	20	HLSTB and HLSTB# must be ± 10 mils of each other

4. Figure Reference Update for "Start Up Conditions and Logic Protection" for Wireless/Bluetooth* Coexistence Interface Design

In section 12.3, figure reference for protection logic should be Figure 120.

A recommended implementation that will protect both components from potential damage caused by asynchronous power on/off is depicted in **Figure 120**. For the Bluetooth module, it is recommended that a tri-state buffer (powered by the Bluetooth module supply) and a 1-kΩ series resistor be placed near the Bluetooth module. Likewise, a tri-state buffer (powered by the mini-PCI 3.3V supply) should be placed near to the Intel PRO/Wireless Network Connection. This low cost solution has been validated and noted to have a minimal impact on board area if implemented as recommended.

5. High-Density Memory Support Update

The 855GM chipset architecture supports 2-GB memory. However, only limited simulation and bench testing have been done on various package configurations. Section 6.5 "Routing Updates for High-Density Memory Device Support" should be updated as follows:

The 855GM chipset architecture supports 2-GB memory. This memory capacity can be achieved using "high-density" memory devices of various package types. Intel has done only limited simulation and bench testing on these high-density SO-DIMM memory modules and has not seen any functional or analog inspection failures using existing layout guidelines. However, Intel has not done complete simulation nor validation with all the available package configurations. Customers are strongly encouraged to perform complete validation on their platforms based on the particular high-density memory package of their choice.

6. CRT VSYNC/HSYNC Design Update

New / updated recommendations are provided for HSYNC/VSYNC isolation buffer / switch implementations. Customers need to ensure that there is no back-drive on these signals from the monitors and that electrical specifications are met at both the buffer and at the VGA connectors. Section 7.1.6 "HSYNC and VSYNC Design Considerations" should be updated as follows:

HSYNC and VSYNC signals are connected to the analog display attached to the VGA connector. These are 3.3-V outputs from the GMCH. Some monitors have been found to drive HSYNC and VSYNC signals during reset. Because these signals are used as straps on the 852GM/GME and 855GM/GME, the GMCH can enter an illegal state under these conditions. In order to prevent these signals from being driven to the GMCH during reset, system designers must utilize appropriate logic to ensure the GMCH is isolated from any monitor driving HSYNC or VSYNC while PCI_RST# is active. Appropriate logic is required between the GMCH and the VGA connector (both the on-board VGA connector and the VGA connector at the docking station).

Intel's recommended solution is to use an analog switch (i.e. discrete FET, Q-buffer) to switch these signals between the on-board VGA connector and the docking connector. In this case, footprints for a series resistor and an optional capacitor are needed on each of these signals to meet the VESA electrical specifications for video signals. Resistor and capacitor values of 39ohm and 33pF respectively are used on the CRB. These values were calculated based on the GMCH buffer strength and board routing. Customers are advised to perform a signal integrity check

specific to their board topology, to determine the appropriate resistor and capacitor values for their platforms.

An alternative option is to use a unidirectional buffer on each of these signals. For each of the HSYNC and VSYNC signals, a footprint for a series resistor must be placed between the GMCH and the unidirectional buffer to prevent excessive overshoot and undershoot at the input of the buffer. Consideration should also be taken in designing the filter circuit on the output of these buffers to ensure that the VESA electrical specifications for video signals are met at both the on-board VGA connector as well as on the docking station. Customers are strongly encouraged to perform complete signal integrity validation at the input of the buffer and at the VGA connectors.

7. Clarification on Host Clock (BCLK) Package Length

Replace Table 100 with the following:

CPU host clock package lengths (BCLK0/BCLK1) are matched at 447 mils. The GMCH package trace lengths should be 1138 mils for BCLK and 1145 mils for BCLK#.

Table 100. Clock Package Length

Parameter	Length
Intel Pentium M Processor / Intel Celeron M Processor Package Length	**BCLK0: 447 mils** **BCLK1: 447 mils**
Intel 855GM/GME Chipset GMCH Package Length	**BCLK: 1138 mils** **BCLK#: 1145 mils**
CPU Socket Equivalent Length	157 mils

8. Clarification on USB ESD Protection

Added reference to USB ESD Application Note.

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. ESD protection is needed for USB lines. Refer to the *Intel® ICH Family USB ESD Considerations Application Note* for ESD protection implementation guidelines. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 108. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, Intel recommends including footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

9. Correction on PCICLK Trace Length Matching

There is a correction to the Total Length Range parameter in the PCICLK Clock Group Routing Constraints table. The total length range should not include L3. Update to Table 103 highlighted in blue.

Table 103. PCICLK Clock Group Routing Constraints

Parameter	Definition
Total Length Range – L1 + L2 ~~Total Length Range – L1 + L2 + L3~~	CLK33 – 2.5” (for nominal matching)

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