Intel® 855GM/855GME Chipset Platform

Design Guide

May 2004

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Revision History

Revision Number	Description	Revision Date
001	Initial Release	March 2003
002	Updates Include: • Added 855GME design guidelines	September 2003
003	Updates Include: • Added Intel Celeron M processor support	January 2004
004	Updates include: • Added section 7 Memory Down/Micro-DIMM design guidelines • Added section 9 AGP Port Design guidelines • Added support for Intel® Pentium® M on 90 nm Process with 2 MB L2 Cache	May 2004

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1. Introduction

This design guide provides Intel's design recommendations for the Intel 855GM/855GME chipset based systems. The guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues.

Table 1. Conventions and Terminology

Convention/Terminology	Definition
AC	Audio Codec
AMC	Audio/Modem Codec
Anti-Etch	Any plane-split, void or cutout in a VCC or GND plane is referred to as an anti-etch
ASF	Alert Standards Format
BER	Bit Error Rate
FSB	Intel Pentium M/ Pentium M on 90 nm Process with 2 MB L2 Cache/Celeron M Front Side Bus –Processor to GMCH interface.
CMC	Common Mode Choke
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge
FS	Full Speed – Refers to USB 1.1 Full Speed
FWH	Firmware Hub – A non-volatile memory device used to store the system BIOS.
HS	High Speed – Refers to USB 2.0 High Speed
ICH4-M	I/O Controller Hub Fourth Generation – Mobile (82801DBM)
Intel Pentium M	Refers to the Intel Pentium M Processor and Intel Pentium M Processor on 90 nm Process with 2 MB L2 Cache. This document refers to both processors as the Intel Pentium M Processor unless explicitly specified
LCI	LAN Connect Interface
LOM	LAN on Motherboard
LPC	Low Pin Count
LS	Low Speed – Refers to USB 1.0 Low Speed
MC	Modem Codec
Montara-GM	Intel 852GM Chipset GMCH
Montara-GM+	Intel 852GME Chipset GMCH
GMCH	Graphics Memory Controller Hub – Applies to both Intel855GM / Intel 855GME
PCM	Pulse Code Modulation
PLC	Platform LAN Connect
RTC	Real Time Clock
PWM	Pulse Width Modulation
SMBus	System Management Bus – A two-wire interface through which various system

Convention/Terminology	Definition
	components can communicate
SPD	Serial Presence Detect
STD	Suspend-To-Disk
STR	Suspend-To-Ram
TCO	Total Cost of Ownership
TDM	Time Division Multiplexed
UBGA	Micro Ball Grid Array
USB	Universal Serial Bus
VRM	Voltage Regulator Module

1.1. Referenced Documents

Document	Location
Intel®Pentium® M Processor Datasheet (252612)	http://developer.intel.com/design/mobile/datashts
Intel®Pentium® M Processor on 90 nm Process with 2-MB L2 Cache Datasheet	http://developer.intel.com
Intel® Celeron® M Processor Datasheet (300302)	http://developer.intel.com/design/mobile/datashts
Intel® 855GM/855GME Chipset (GMCH) Datasheet	http://developer.intel.com
Intel® 82801DBM I/O Controller Hub 4-Mobile (ICH4-M) Datasheet and Spec Update	http://developer.intel.com http://developer.intel.com/design/chipsets/specupdt/
Application Note AP-728: ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions (Application Note AP-728)	http://developer.intel.com/design/chipsets/applnots/
ITP700 Debug Port Design Guide	Contact your Intel Field Representative
JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification	Contact your Intel Field Representative
Intel® DDR 200/266/333 JEDEC Spec Addendum	http://developer.intel.com
PC2100 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification	http://developer.intel.com

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2. System Overview

2.1. Platform Component Features

The technologies represented by the Intel Centrino brand will include the Intel Pentium M processor, related chipsets, and 802.11 (Wi-Fi) wireless networking capability. The Intel Pentium M processor is a higher performance, lower power mobile processor with several micro-architectural enhancements over existing Intel mobile processors. Key features include: Dynamic Execution; data pre-fetch logic; 400-MHz, source-synchronous PSB; on-die, 1-MB second level cache with Advanced Transfer Cache Architecture; Streaming SIMD Extensions 2 (SSE2); and Enhanced Intel® SpeedStep® technology.

Intel Centrino mobile technology also incudes the 855GM chipset components: the GMCH and the ICH4-M. The accelerated hub architecture interface (the chipset component interconnect) is designed into the chipset to provide an efficient, high bandwidth, communication channel between the GMCH and the ICH4-M.

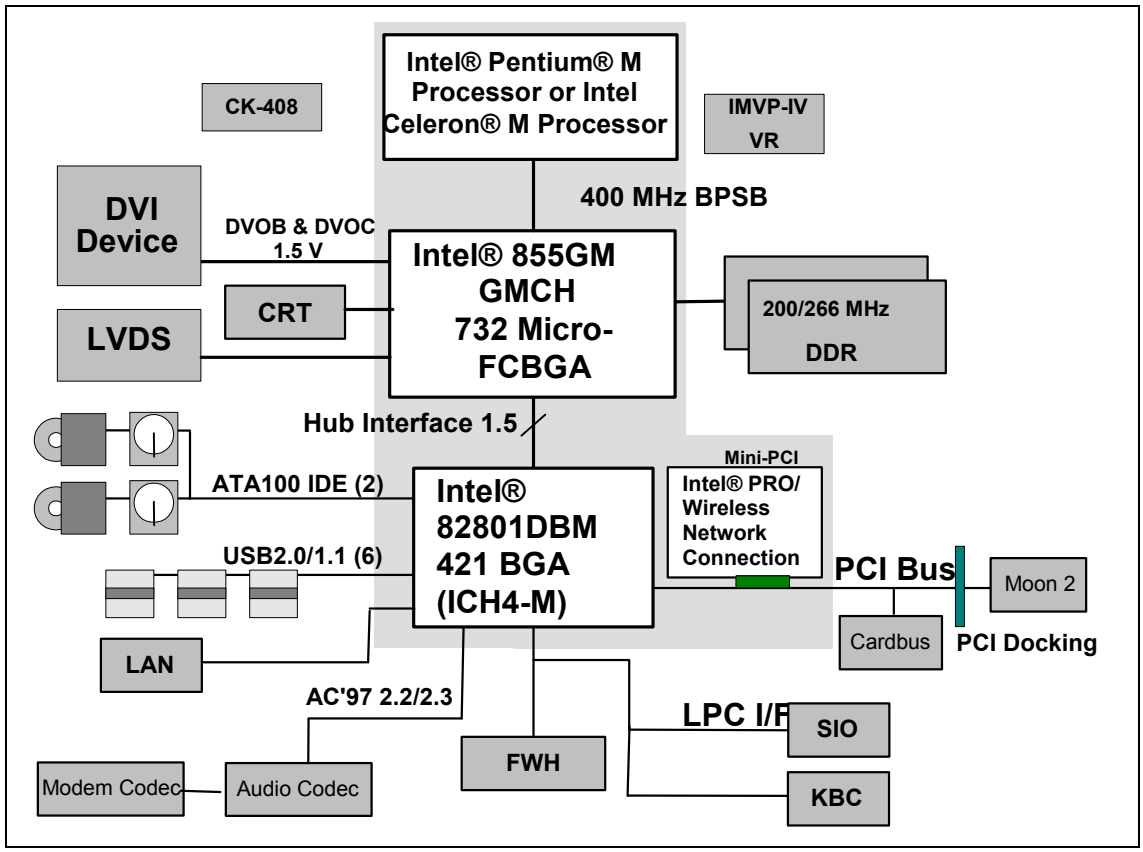
The GMCH component contains a PSB controller, a graphics controller, and a memory controller, while providing an LVDS interface and two Digital Video Out ports. The ICH4-M component integrates USB host controllers (supporting the USB 1.1 and USB 2.0 specification), an Ultra ATA 100/66/33 controller, a LAN controller, and an AC'97 digital controller, while providing interfaces for PCI and LPC devices, as well as FWH Flash BIOS.

The integrated Wi-Fi Certified Intel PRO/Wireless 2100 Network Connection has been designed and validated to work with all of the Intel Centrino™ mobile technology components and is able to connect to 802.11b Wi-Fi certified access points. It also supports advanced wireless LAN security including Cisco* LEAP, 802.1X, and WEP in addition to providing software-upgradeable support for future security protocols, like WPA and full Cisco compatible features. Finally, for comprehensive security support, the Intel PRO/Wireless 2100 Network Connection has been verified with leading VPN suppliers like Cisco, CheckPoint*, Microsoft* and Intel NetStructure™.

An ACPI-compliant Intel 855GM / Intel 855GME chipset based system can support the *Full-On (S0), Power On Suspend (S1-M), Suspend to RAM (S3), Suspend to Disk (S4), and Soft-Off (S5)* power management states. Through the use of an appropriate LAN device, the chipset also supports *wake-on LAN** for remote administration and troubleshooting. The chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true *plug-and-play* for the platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97 allows the OEM to use *software configurable* AC'97 audio and modem coder/decoders (codecs) instead of the traditional ISA devices.

2.2. Intel 855GM Platform Component Features

Figure 1. Intel Pentium M Processor and Intel 855GM Chipset Block Diagram



2.2.1. Intel® Pentium® M Processor and Intel Celeron M Processor

- On-die primary 32-kbyte, instruction cache and 32-kbyte, write-back data cache
- On-die 1-MB second level cache; On-die 512-kB second level cache (Intel Celeron M Processor)
- Supports Streaming SIMD Extensions 2 (SSE2)
- Advanced Gunning Transceiver Logic (AGTL+) bus driver technology
- Enhanced Intel SpeedStep technology to enable real-time dynamic switching between multiple voltage and frequency points (not supported by Intel Celeron M processor)
- Supports host bus dynamic bus inversion (DINV)
- Dynamic power down of Data Bus buffers
- BPRI# control to Disable Address/Control buffers
- Package/Power
  - 478-pin, Micro-FCPGA and 479-ball Micro-FCBGA packages
  - VCC-CORE:
    - Intel Pentium M processor: 1.484 V (highest frequency mode) to 0.844 V (lowest
    - frequency mode); 0.748 V (Deeper Sleep) core voltage

  - Intel Celeron M processor: 1.356 V (Standard Voltage core version), 1.004 V (Ultra-
  - Low Voltage core version)
- VCCA (1.8 V):
- VCCP (1.05 V)

2.2.2. Intel® 855GM Chipset Graphics Memory Controller Hub (GMCH)

2.2.2.1. Intel Pentium M Processor and Intel Celeron M Processor FSB Support

- Optimized for Intel Pentium M/Intel Celeron M processor in 478-pin Micro-FCPGA package
- AGTL+ bus driver technology with integrated GTL termination resistors (gated AGTL+ receivers for reduced power)
- Supports 32-bit AGTL+ bus addressing (no support for 36-bit address extension)
- Supports Uni-processor (UP) systems
- 400-MHz, source-synchronous PSB
- 2X Address, 4X data
- 12 deep In-Order queue

2.2.2.2. Integrated System Memory DRAM Controller

- Supports up to two double-sided SO-DIMMs (four rows populated) with unbuffered PC1600/PC2100 DDR-SDRAM (with or without ECC)
- Supports 64-Mb, 128-Mb, 256-Mb, and 512-Mb technologies for x8 and x16 width devices
- Maximum of 1 GB of system memory with 512-Mb technology devices; maximum of 2 GB of system memory with high-density 512Mb technology devices
- Supports 200-MHz and 266-MHz DDR devices
- 64-bit data interface (72-bit with ECC)
- Supports up to 16 simultaneous open pages
- Support for SO-DIMM serial presence detect (SPD) scheme via SMBus interface
- S3 power management support via self refresh mode using CKE

2.2.2.3. Internal Graphics Controller

- Graphics Core Frequency
  - Display / Render frequency up to 200 MHz
- 3D Graphics Engine
  - 3D Setup and Render Engine
  - Zone Rendering
  - High quality performance Texture Engine
- Analog Display Support
  - 350-MHz integrated 24-bit RAMDAC
  - Hardware color cursor support

- — Accompanying I2C and DDC channels provided through multiplexed interface
- — Dual independent pipe for dual independent display
- — Simultaneous display: same images and native display timings on each display device

- Digital Video Out Port (DVOB and DVOC) support
  - — DVOB & DVOC with 165-MHz dot clock support for each 12-bit interface
  - — Compliant with DVI Specification 1.5

- Dedicated LFP (local flat panel) support
  - — Single or dual channel LVDS panel support up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz per channel
  - — SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
  - — Supports data format of 18 bpp
  - — LCD panel power sequencing compliant with SPWG timing specification
  - — Compliant with ANSI/TIA/EIA –644-1995 spec
  - — Integrated PWM interface for LCD backlight inverter control
  - — Bi-linear Panel fitting

2.2.2.4. Package/Power

- 732-pin Micro-FCBGA (37.5 mm x 37.5 mm)
- VTTLF, VTTHF (*1.05 V*)
- VCC, VCCASM, VCCHL, VCCAHPLL, VCCAGPLL, VCCADPLLA, VCCADPLLB (*1.2 V*)
- VCCADAC, VCCDVO, VCCDLVDS, VCCALVDS, (*1.5 V*)
- VCCSM, VCCQSM, VCCTXLVDS (*2.5 V*)
- VCCGPIO (*3.3 V*)

2.2.3. Intel® 82801DBM I/O Controller Hub 4-Mobile (ICH4-M)

- Upstream Accelerated Hub Architecture interface for access to the GMCH
- PCI 2.2 interface (6 PCI Request/Grant Pairs)
- Bus Master IDE controller (supports Ultra ATA 100/66/33)
- USB 1.1 and USB 2.0 Host Controllers
- I/O APIC
- SMBus 2.0 Controller
- FWH Interface
- LPC Interface
- AC’97 2.2 / 2.3 Interface
- Alert-On-LAN*
- IRQ Controller
- Package/Power
  - — 421-pin, BGA package (31 mm x 31 mm)
  - — VCC1_5 (1.5 V main logic voltage), VCC3_3 (3.3 V main I/O voltage)

- VCCSUS1_5 (1.5 V resume logic voltage), VCCSUS3_3 (3.3 V resume I/O voltage)
- VCCLAN1_5 (1.5 V LAN logic voltage), VCCLAN3_3 (3.3 V LAN I/O voltage)
- V5REF (5 V) , V5REF_SUS (5 V)
- VCCRTC (2.0V – 3.3V)
- VCCHI (1.5 V)
- VCCP (1.05 V)

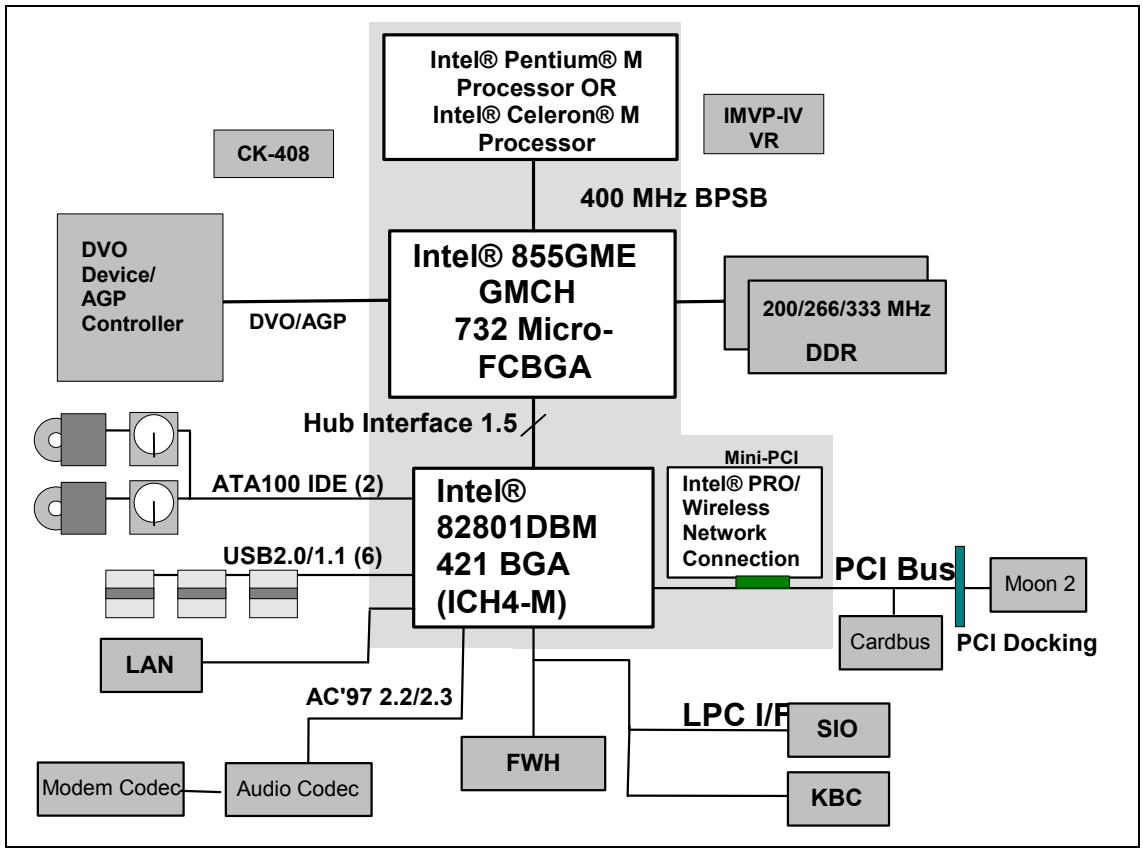
2.2.4. Intel® Pro/Wireless Network Connection

- Ability to connect to 802.11 Wi-Fi Certified networks
- Industry standard and extended wireless security support (WEP, 802.1X and Cisco* LEAP)
- Intel PROSet software with advanced profile management support, allows multiple setup profiles to connect to different WLAN networks
- Intel PROSet software with automatic WLAN switching support enables automatic switching between wired and wireless LAN connections
- Intel PROSet software supports Cisco, Check Point*, Microsoft* and Intel VPN connections†
- Intel PROSet software with ad hoc connection wizard support provides a simple interface for setting up ad hoc networks
- Intel Wireless Coexistence System support enables reduced interference between Intel PRO/Wireless and certain Bluetooth* devices
- Per-packet antenna selection enables optimized WLAN performance
- Intel Intelligent Scanning technology, reduces power by controlling the frequency of scanning for access points
- Power saving capability with five different power settings allows users to trade off performance

2.3. Intel 855GME Platform Component Features

The Intel 855GME chipset based system supports the Intel® Pentium® M processor in the 90 nm process.. This section lists only additional features supported on the Intel 855GME chipset based system. All features in Intel 855GM chipset based system are supported in the Intel 855GME chipset based system as well.

Figure 2. Intel Pentium M, Intel Pentium M Processor on 90 nm Process with 2 MB L2 Cache, Intel Celeron M Processor and 855GME Chipset System Block Diagram



2.3.1. Intel Pentium® M Processor on 90 nm Process with 2 MB L2 Cache

All features of the Intel Pentium M processor are supported by the Intel Pentium M Processor on 90 nm Process with 2 MB L2 Cache. This section only lists the additional enhancements.

- On-die 2-MB second level cache
- Package/Power
  - VCC-CORE: 1.308 V (highest frequency mode) to 0.844 V (lowest frequency mode); 0.748 V (Deeper Sleep) core voltage
  - VCCA (1.8 V) or (1.5V)

2.3.2. Intel 855GME Chipset Graphics Memory Controller Hub (GMCH)

All chipset and graphics features of Intel 855GM chipset GMCH is supported in Intel 855GME chipset GMCH. This section lists the additional enhancements.

- Integrated System Memory DRAM controller
  - — Supports up to two double-sided SO-DIMMs (four rows populated) with unbuffered PC1600/PC2100/PC2700 DDR-SDRAM (ECC is not supported)
  - — Support for memory self refresh in C3
- Integrated graphics core frequency
  - — Display / Render Core frequency up to 250 MHz
- Integrated graphics engine
  - — Frame Buffer Compression
  - — Bi-Cubic Filtering supported
  - — Video Mixer Rendering support
  - — Linear Gamma Blending for VMR
- Backlight Image Adaptation Technology
  - — Allows image enhancement by direct control of the backlight inverter through the PWM signal
- Package/Power
  - — VCC, VCCASM, VCCHL, VCCAHPLL, VCCAGPLL, VCCADPLLA, VCCADPLLB (*1.35V*)

2.3.2.1. Accelerated Graphics Port (AGP) Interface

The 855GME platform is configurable to support either the AGP interface for external graphics or the DVO interface when using internal graphics.

- Supports AGP 2.0 data transfers
- Supports a single AGP (1X/2X/4X) device (either via a connector or on the motherboard)
- Only supports 1.5-V VDDQ for AGP electricals
- PCI semantic (FRAME# initiated) accesses to DRAM are snooped
- AGP semantic (PIPE# and SBA) traffic to DRAM is not snooped on the PSB and is therefore not coherent with the CPU caches
- High priority access support
- Delayed transaction support for AGP reads that cannot be serviced immediately
- AGP Busy/Stop Protocol support
- Support for D3 Hot and Cold Device states
- AGP Clamping and Sense Amp control

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3. General Design Considerations

This section documents motherboard layout and routing guidelines for the Intel 855GM/GME chipset based systems. It does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, Intel recommends that critical signals be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e. 55 Ω ± 15%) is the "nominal" trace impedance for a 5-mil wide external trace and a 4-mil wide internal trace. **However**, some stack-ups may lead to narrower or wider traces on internal or external layers in order to meet the 55-Ω impedance target, that is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. Note the trace impedance target assumes that the trace is not subjected to the EM fields created by changing current in neighboring traces. It is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces when calculating flight times. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this Section should be followed. Also, all high speed, impedance controlled signals should have continuous GND referenced planes and cannot be routed over or under power/GND plane splits.

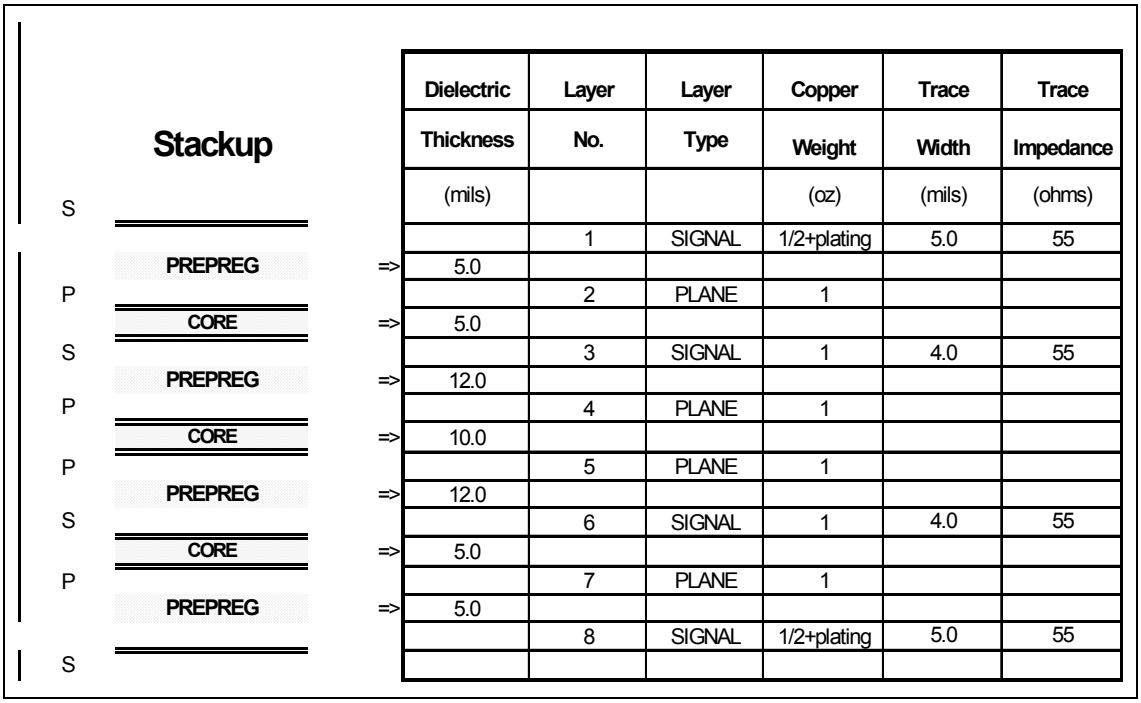
3.1. Nominal Board Stack-Up

The Intel 855GM/GME chipset based platforms require a board stack-up yielding a target impedance of 55 Ω ± 15%. An example of an 8-layer board stack-up is shown in Figure 3. The left side of the figure illustrates the starting dimensions of the metal and dielectric material thickness as well as drawn trace width dimensions prior to lamination, conductor plating, and etching. After the motherboard materials are laminated, conductors plated, and etched, somewhat different dimensions will result. Dielectric materials become thinner, under/over etching of conductors alters their trace width, and conductor plating makes them thicker. It is important to note that for the purpose of extracting electrical models from transmission line properties, the final dimensions of signals after lamination, plating, and etching should be used.

The stack-up uses 1.2-mil (1 oz) copper on power planes to reduce I*R drops and 0.6-mil copper thickness on the signal layers: primary side layer (L1), Layer 3 (L3), Layer 6 (L6), and secondary side layer (L8). After plating, the external layers become 1.2 to 2 mils thick.

To ensure impedance control of 55 Ω, the primary and secondary side layer micro-strip lines should reference solid ground planes on Layer 2 and Layer 7, respectively.

Figure 3. Recommended Board Stack-Up Dimensions



Dielectric Thickness (mils)		Layer No.	Layer Type	Copper Weight (oz)	Trace Width (mils)	Trace Impedance (ohms)
		1	SIGNAL	1/2+plating	5.0	55
	=>	5.0				
		2	PLANE	1		
	=>	5.0				
		3	SIGNAL	1	4.0	55
	=>	12.0				
		4	PLANE	1		
	=>	10.0				
		5	PLANE	1		
	=>	12.0				
		6	SIGNAL	1	4.0	55
	=>	5.0				
		7	PLANE	1		
	=>	5.0				
		8	SIGNAL	1/2+plating	5.0	55

Internal signal traces on Layer 3 and Layer 6 are unbalanced strip-lines. To meet the nominal 55-Ω characteristic impedance for these traces, they reference a solid ground plane on Layer 2 and Layer 7. Since the coupling to Layer 4 and Layer 5 is still significant, (especially true when thinner stack-ups use balanced strip-lines on internal layers) these layers are converted to ground floods in the areas of the motherboard where the speed critical interfaces like the PSB or DDR system memory are routed. In the remaining Sections of the motherboard layout the Layer 4 and Layer 5 layers are used for power delivery.

The secondary side layer (L8) is also used for power delivery in many cases, since it benefits from the thick copper plating of the external layer plating as well as referencing the close Layer 7 ground plane. The benefit of such a stack-up is low inductance power delivery.

3.2. Alternate Stack Ups

OEMs may choose to use different stack-ups (number of layers, thickness, trace width, etc.) from the one example outlined in Figure 3. However, the following key elements should be observed:

1. Final post lamination, post etching, and post plating dimensions should be used for electrical model extractions.
2. Power plane layers should be 1 oz thick and signal layers should be ½ oz thick. External layers become 1 – 1.5 oz (1.2 – 2 mils) thick after plating.
3. All high-speed signals should reference solid ground planes through the length of their routing and should not cross plane splits. To guarantee this, both planes surrounding strip-lines should be GND.
4. Intel recommends that high-speed signal routing be done on internal, strip-line layers.
5. For high-speed signals transitioning between layers next to the component, the signal pins should be accounted for by the GND stitching vias that would stitch all the GND plane layers in that area

of the motherboard. Due to the arrangement of the processor and the GMCH pin-maps, GND vias placed near all GND land pads will also be very close to high-speed signals that may be transitioning to an internal layer. Thus, no additional ground stitching vias (besides the GND pin vias) are required in the immediate vicinity of the processor and the GMCH packages to accompany the signal transitions from the component side into an internal layer.

6. High-speed routing on external layers should be minimized in order to avoid EMI. Routing on external layers also introduces different delays compared to internal layers. This makes it extremely difficult to do length matching if routing is done on both internal and external layers.
7. If Intel's recommended stackup guidelines are not used, then the OEM is liable for all aspects of their board design (i.e. understanding impacts of SI and power distribution).

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4. Intel Pentium M/Celeron M Front Side Bus Design Guidelines

The following layout guidelines support designs using the Intel Pentium M processor or Intel Celeron processor and the Intel 855GM/GME GMCH chipset. Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the motherboard for most PSB signals. A simple point-to-point interconnect topology is used in these cases.

4.1. Intel Pentium M Processor / Intel Celeron M FSB Design Recommendations

For proper operation of the Intel Pentium M / Intel Celeron M processor and the GMCH PSB interface, it is necessary that the system designer meet the timing and voltage specification of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions, which may be different than an OEM's system design. The most accurate way to understand the signal integrity and timing of the FSB in your platform is by performing a comprehensive simulation analysis. It is possible that adjustments to trace impedance, line length, termination impedance, board stack-up, and other parameters can be made that improve system performance.

Refer to the latest *Intel® Pentium® M Processor Datasheet or Intel Celeron M Datasheet* for a FSB signal list, signal types, and definitions. Below are the design recommendations for the data, address, and strobes. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate. The following topology and layout guidelines are preliminary and subject to change. The guidelines are derived from empirical testing with GMCH package models.

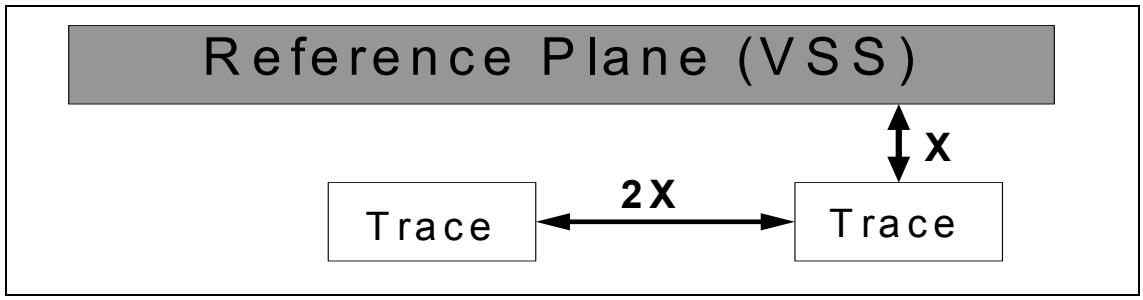
4.1.1. Recommended Stack-up Routing and Spacing Assumptions

The following section describes in more detail, the terminology and definitions used for different routing and stack-up assumptions that apply to the recommended motherboard stack-up show in Section 3.1.

4.1.1.1. Trace Space to Trace – Reference Plane Separation Ratio

Figure 4 illustrates the recommended relationship between the edge-to-edge trace spacing (2X) versus the trace to reference plane separation (X). An edge-to-edge trace spacing (2X) to trace – reference plane separation (X) ratio of 2 to 1 ensures a low crosstalk coefficient. All the effects of crosstalk are difficult to simulate. The timing and layout guidelines for the processor have been created with the assumption of a 2:1 trace spacing to reference plane ratio. A smaller ratio would have an unpredictable impact due to crosstalk.

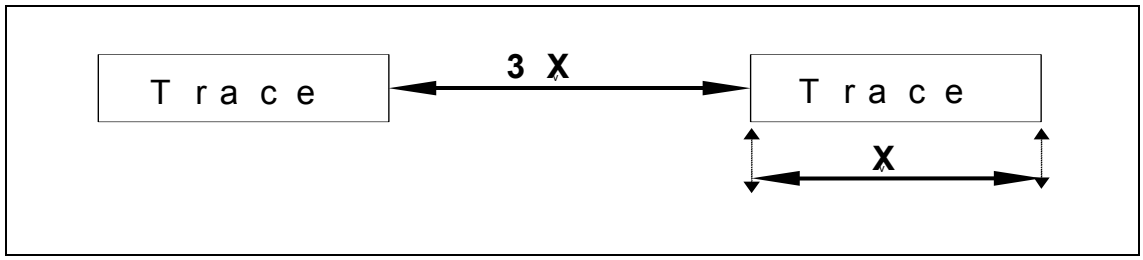
Figure 4. Trace Spacing vs. Trace to Reference Plane Example



4.1.1.2. Trace Space to Trace Width Ratio

Figure 5 illustrates the recommended relationship between the edge-to-edge trace spacing versus trace width ratio for the best signal quality results. In general, a 3:1 trace space to trace width ratio is preferred and highly recommended. In case of routing difficulties on the motherboard, using a 2:1 ratio would be acceptable **only** if additional simulations conclude that it is possible, which may include some changes to the stack-up or routing assumptions.

Figure 5. Three to One Trace Spacing to Trace Width Example



4.1.2. Common Clock Signals

All common clock signals use an AGTL+ bus driver technology with on die integrated GTL termination resistors connected in a point-to-point, Zo = 55 Ω, controlled impedance topology between the processor and the GMCH. No external termination is needed on these signals. These signals operate at the PSB frequency of 100 MHz.

Common clock signals should be routed on an internal layer while referencing solid ground planes. Based on current simulation results, routing on internal layers allows for a minimum pin-to-pin motherboard length of approximately 1.0 inch and a maximum of 6.5 inches. Trace length matching for the common clock signals is not required. For details on minimum motherboard trace length requirements, please refer to Section 4.1.2.1 and Table 2 for more details. Intel recommends routing these signals on the same internal layer for the entire length of the bus. If routing constraints require routing of these signals with a transition to a different layer, a minimum of one ground stitching via for every two signals should be placed within 100 mils of the signal transition vias.

Routing of the common clock signals should use 2:1 trace spacing to trace width. This implies a minimum of 8 mils spacing (i.e. 12-mil minimum pitch) for a 4-mil trace width for routing on internal layers. Practical cases of escape routing under the GMCH or processor package outline and vicinity may not allow the implementation of 2:1 trace spacing requirements. Although every attempt should be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the GMCH and the processor package outlines and up to 200 – 300 mils outside the package outline.

Table 2 summarizes the list of common clock and key routing. RESET# (CPURST# of GMCH) is also a common clock signal but requires a special treatment for the case where an ITP700FLEX debug port is used. See Section 4.1.5 for further details.

Table 2. Processor System Bus Common Clock Signal Internal Layer Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Spacing & Width
CPU	GMCH		Min (mils)	Max (inches)		
ADS#	ADS#	Strip-line	997	6.5	55 ± 15%	2:1
BNR#	BNR#	Strip-line	1298	6.5	55 ± 15%	2:1
BPRI#	BPRI#	Strip-line	1215	6.5	55 ± 15%	2:1
BR0#	BR0#	Strip-line	1411	6.5	55 ± 15%	2:1
DBSY#	DBSY#	Strip-line	1159	6.5	55 ± 15%	2:1
DEFER#	DEFER#	Strip-line	1291	6.5	55 ± 15%	2:1
DPWR#	DPWR#	Strip-line	1188	6.5	55 ± 15%	2:1
DRDY#	DRDY#	Strip-line	1336	6.5	55 ± 15%	2:1
HIT#	HIT#	Strip-line	1303	6.5	55 ± 15%	2:1
HITM#	HITM#	Strip-line	1203	6.5	55 ± 15%	2:1
LOCK#	HLOCK#	Strip-line	1198	6.5	55 ± 15%	2:1
RS0#	RS0#	Strip-line	1315	6.5	55 ± 15%	2:1
RS1#	RS1#	Strip-line	1193	6.5	55 ± 15%	2:1
RS2#	RS2#	Strip-line	1247	6.5	55 ± 15%	2:1
TRDY#	HTRDY#	Strip-line	1312	6.5	55 ± 15%	2:1
RESET#[1]	CPURST#	Strip-line	1101	6.5	55 ± 15%	2:1

NOTE: For topologies where an ITP700FLEX debug port is implemented, see Section 4.1.5 for RESET# (CPURST#) implementation details.

4.1.2.1. Processor Common Clock Signal Package Length Compensation

Trace length matching for the common clock signals is not required. However, **package compensation** for the common clock signals is required for the minimum board trace. Please refer to Table 3 and the example below for more details. Package length compensation should not be confused with length matching. Length matching refers to constraints on the min and max length bounds of a signal group based on clock length, whereas package length compensation refers to the process of compensating for package length variance across a signal group.

All common clock signals are required to meet the minimum pad-to-pad requirement of **2.212** inches, based on ADS# (as this signal has the longest package lengths). This implies a minimum pin-to-pin motherboard trace length of **997 mils**. Additional motherboard trace will be added to some of the shorter common clock nets on the system board in order to meet the same minimum requirement for trace lengths from the **die-pad** of the processor to the **associated die-pad** of the chipset.

For example:

ADS# = 997 mils board trace + 454 CPU PKG + 761 GMCH PKG = 2212 pad-to-pad length

BR0# = X mils board trace + 336 CPU PKG + 465 GMCH PKG = 2212 pad-to-pad length

Therefore: X = BR0# board trace = 2212 - 336 - 465 = 1411 pin to pin length.

Figure 6. Common Clock Topology

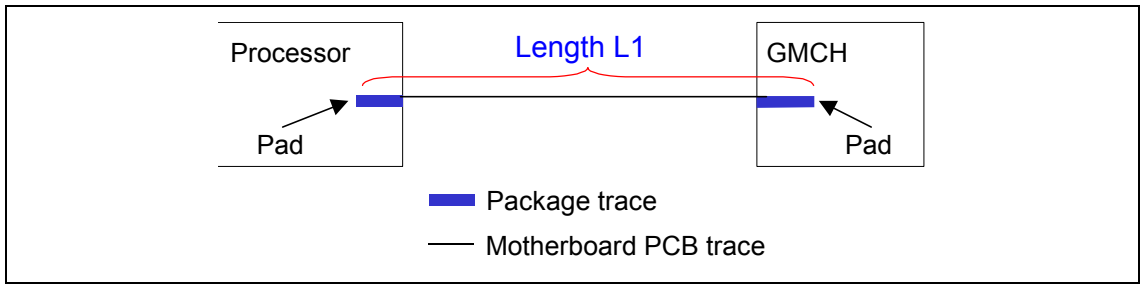


Table 3. Processor and GMCH PSB Common Clock Signal Package Lengths and Minimum Board Trace Lengths

Signal Names		Package Length		Total Pad-to-Pad Min. Length Requirements L1 (mils)	Min. Board Trace Length (mils)
CPU	GMCH	Intel Pentium M/Celeron Processor	GMCH		
ADS#	ADS#	454	761	2212	997
BNR#	BNR#	506	408	2212	1298
BPRI#	BPRI#	424	573	2212	1215
BR0#	BR0#	336	465	2212	1411
DBSY#	DBSY#	445	608	2212	1159
DEFER#	DEFER#	349	572	2212	1291
DPWR#	DPWR#	506	518	2212	1188
DRDY#	DRDY#	529	347	2212	1336
HIT#	HIT#	420	489	2212	1303
HITM#	HITM#	368	641	2212	1203
LOCK#	HLOCK#	499	515	2212	1198
RS0#	RS0#	576	321	2212	1315
RS1#	RS1#	524	495	2212	1193
RS2#	RS2#	451	514	2212	1247
TRDY#	HTRDY#	389	511	2212	1312
RESET#	CPURST#	455	656	2212	1101

4.1.3. Source Synchronous Signals General Routing Guidelines

All source synchronous signals use an AGTL+ bus driver technology with on-die GTL termination resistors connected in a point-to-point, Zo = 55 Ω controlled impedance topology between the processor and the GMCH. No external termination is needed on these signals. Source synchronous PSB address signals operate at a double pumped rate of 200 MHz while the source synchronous PSB data signals operate at a quad pumped rate of 400 MHz. High-speed operation of the source synchronous signals

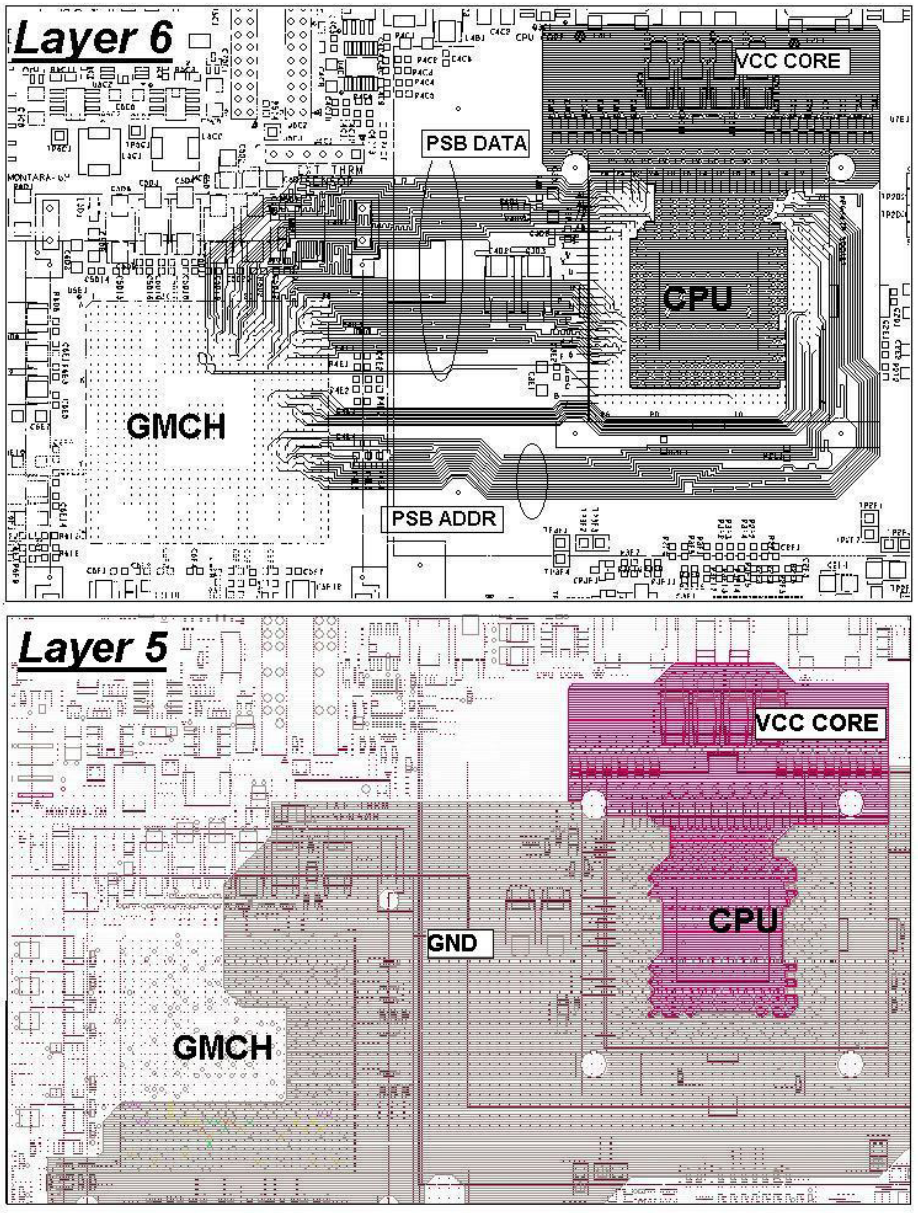
requires careful attention to their routing considerations. The following guidelines should be strictly adhered to, to guarantee robust high frequency operation of these signals.

Source synchronous data and address signals and their associated strobes are partitioned into groups of signals. Flight time skew minimization within the same group of source synchronous signals is a key parameter that allows their high frequency (400 MHz) operation. All the source synchronous signals that belong to **the same group** should be routed on **the same internal layer** for the entire length of the bus. It is OK to split different groups of source synchronous signals between different motherboard layers as long as all the signals that belong to that group are kept on the same layer. Grouping of PSB source synchronous signals is summarized in Table 4 and Table 6. This practice results in a significant reduction of the flight time skew since the dielectric thickness, line width, and velocity of the signals will be uniform across a single layer of the stack-up.

The source synchronous signals should be routed as a strip-line on an internal layer with complete reference to ground planes both above and below the signal layer. Routing with references to split planes or power planes other than ground is **not** recommended. For the recommended stack-up example as shown in Figure 3, source synchronous PSB signals are routed on Layer 3 and Layer 6. Layer 2 and Layer 7 are solid grounds across the entire motherboard. However, this is not sufficient since significant coupling exists between signal layer, Layer 3 and power plane Layer 2 as well as signal layer, Layer 6 and power plane Layer 5. To guarantee complete ground referencing, Layer 4 and Layer 5 are converted to ground plane floods in the areas where the source synchronous PSB signals are routed. In addition all the ground plane areas are stitched with ground vias in the vicinity of the processor and the GMCH package outlines with the vias of the ground pins of the processor and the GMCH pin-map.

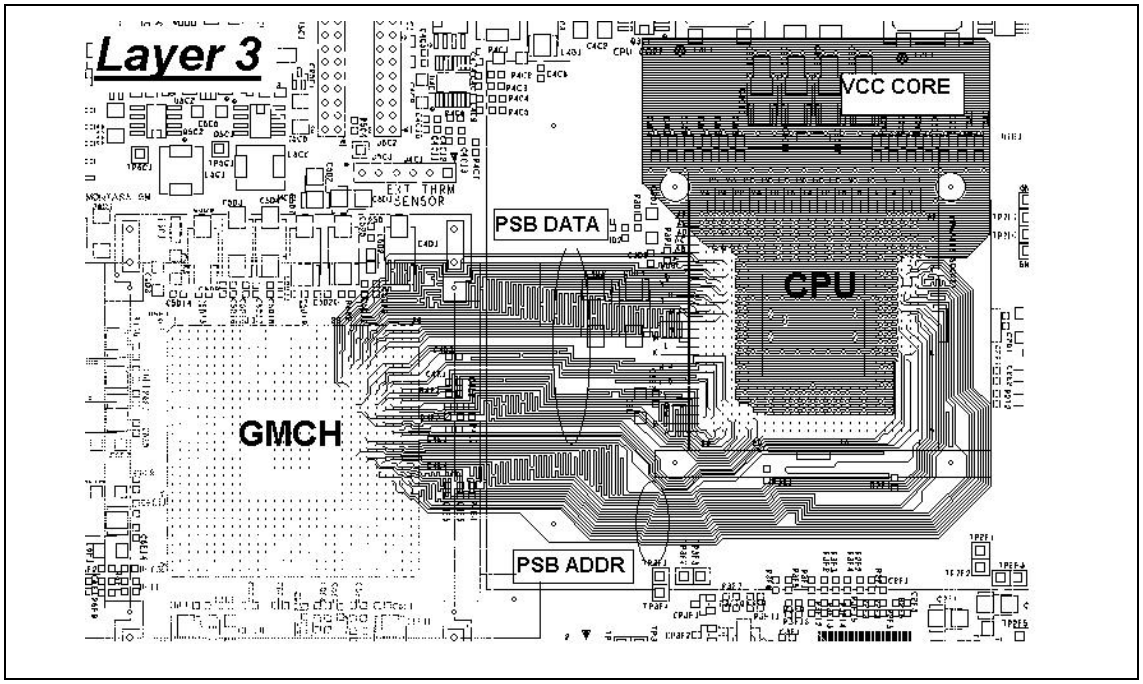
Figure 7 illustrates a motherboard layout of the recommended stack-up of the PSB source synchronous DATA and ADDRESS signals referencing ground planes on both Layer 7 and Layer 5. Note that in the socket cavity of the processor, Layer 5 and Layer 6 is used for VCC core power delivery. However, outside the socket cavity Layer 6 signals are routed on top of a solid Layer 7 ground plane and also Layer 5 is converted to a ground flood under the shadow of the PSB signals routing between the processor and the GMCH. Stitching of all the GND planes is provided by the ground vias in the pin-map of the processor and the GMCH.

Figure 7. Layer 6 PSB Source Synchronous Signals GND Referencing to Layer 5



In a similar way, Figure 8 illustrates a recommended layout and stack-up example of how another group of PSB source synchronous DATA and ADDRESS signals can reference ground planes on both Layer 2 and Layer 4. Note that in the socket cavity of the processor, Layer 3 is used for VCC core power delivery to reduce the I*R drop. However, outside of the socket cavity Layer 3 signals are routed below a solid Layer 2 ground plane and also Layer 4 is converted to a ground flood under the shadow of the PSB signals routing between the processor and the GMCH.

Figure 8. Layer 3 PSB Source Synchronous Signals



4.1.3.1. Source Synchronous Signal Length Matching Constraints

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching requirements called length-matching constraints. These additional requirements further restrict the minimum to maximum length range of each signal group with respect to strobe, within the overall boundaries defined in the guideline tables, as required to guarantee adequate timing margins. The amount of minimum to maximum length variance allowed for each group around the strobe reference length varies from signal group to signal group depending on the amount of timing variation, which can be tolerated.

4.1.3.2. Package Length Compensation

The Intel Pentium M / Intel Celeron M processor package length **does not need** to be accounted for in the motherboard routing since the processor has the source synchronous signals and the strobes length matched within the group inside the package routing. However trace length matching of the **GMCH** package length **does need** to be accounted for in the motherboard routing since the package does not have the source synchronous signals and the strobes length matched within the group inside the package routing. See Table 8 for the processor and the GMCH package lengths. Skew minimization requires GMCH die-pad to processor pin (pad-to-pin) trace length matching of the PSB source synchronous signals that belong to the same group including the strobe signals of that group.

Package length compensation should not be confused with length matching. Length matching refers to constraints on the min and max length bounds of a signal group based on clock length, whereas package length compensation refers to the process of compensating for package length variance across a signal group. There is some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction

with nominal package lengths and that package length compensation be performed as secondary operation.

4.1.3.3. Source Synchronous – Data Group

Robust operation of the 400-MHz, source synchronous data signals require tight skew control. For this reason, these signals are split into matched groups as outlined in Table 4. All the signals within the same group should be kept on the same layer of motherboard routing and should be routed to the same pad-to-pin length within ±100 mils of the associated strobes. Only the Intel Pentium M / Intel Celeron M processor has the package trace equalization for signals within each data and address group. The GMCH does not have the package trace equalization for signals within each data and address group. See Table 8 for the package lengths. Please refer to Section 4.1.2.1 for trace length and package compensation requirements. The two complementary strobe signals associated with each group should be length matched (pad-to-pin) to each other within ± 25 mils and tuned to the average length of the data signals (pad-to-pin) of their associated group. This will optimize setup/hold time margin.

Current simulation results provide routing guidelines using 3:1 spacing for the PSB source synchronous data and strobe signals. This implies a minimum of 12-mil spacing (i.e. 16-mil minimum pitch) for a 4-mil trace width. Practical cases of escape routing under the GMCH or the processor package outline and vicinity may not even allow the implementation of 2:1 trace spacing requirements. Although every attempt should be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the GMCH and the processor package outlines and up to 200 – 300 mils outside the package outline. The benefits of additional spacing include increased signal quality and voltage margining. The trace routing and length matching requirements are as follows in Section 4.1.3.1 to Section 4.1.3.5. Note that if trace impedance can be controlled to within ± 10%, the PSB data signals can then be routed using 2:1 spacing guidelines. The strobes, however, must still be routed with 3:1 spacing.

Table 4. Processor PSB Data Source Synchronous Signal Trace Length Mismatch Mapping

Data Group	DINV signal for associated Data Group	Signal Matching	Data Strobes associated With the Group	Strobe Matching	Notes
D[15:0]#	DINV0#	± 100 mils	DSTBP0#, DSTBN0#	± 25 mils	1,2
D[31:16]#	DINV1#	± 100 mils	DSTBP1#, DSTBN1#	± 25 mils	1,2
D[47:32]#	DINV2#	± 100 mils	DSTBP2#, DSTBN2#	± 25 mils	1,2
D[63:48]#	DINV3#	± 100 mils	DSTBP3#, DSTBN3#	± 25 mils	1,2

NOTES:
1. Strobes of the same group should be trace length matched to each other within ±25 mil and to the average length of their associated Data signal group.
2. Note that all length matching formulas are based on GMCH die-pad to processor pin total length per byte lane. Package length table are provided for all signals in order to facilitate this pad to pin matching.

Table 5 lists the source synchronous data signal general routing requirements. Due to the 400-MHz, high frequency operation of the data signals should be limited to a pin-to-pin trace length minimum of 0.50 inches and maximum of 5.5 inches.

Table 5. Processor System Bus Source Synchronous Data Signal Routing Guidelines

Signal Names				Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Spacing & Width (mils)
Data Group #1	Data Group #2	Data Group #3	Data Group #4		Min (inches)	Max (inches)		
D[15:0]#	D[31:16]#	D[47:32]#	D[63:48]#	Strip-line	0.5	5.5	55 ± 15%	3:1
DINV0#	DINV1#	DINV2#	DINV3#	Strip-line	0.5	5.5	55 ±15%	3:1
DSTBN[0]#	DSTBN[1]#	DSTBN[2]#	DSTBN[3]#	Strip-line	0.5	5.5	55 ± 15%	3:1
DSTBP[0]#	DSTBP[1]#	DSTBP[2]#	DSTBP[3]#	Strip-line	0.5	5.5	55 ±15%	3:1

NOTES:
1. These data signals can be routed with 2:1 spacing if using 55 ± 10% nominal impedance. However, spacing to associated strobes must still be kept at 3:1.

4.1.3.4. Source Synchronous – Address Group

Source synchronous address signals operate at 200 MHz. Thus, their routing requirements are very similar to the data signals. Refer to Sections 4.1.3 and 4.1.3.1 for further details. Table 6 details the partition of the address signals into matched length groups. Due to the lower operating frequency of the address signals, pad-to-pin length matching is relaxed to ± 200 mils. Each group is associated with only one strobe signal. To maximize setup/hold time margin, the address strobes should be trace length matched to the average trace length of the address signals of their associated group. In addition, each address signal should be trace length matched within ± 200 mils of its associated strobe signal.

Table 6. Processor PSB Address Source Synchronous Signal Trace Length Mismatch Mapping

CPU Signal Name	Signal Matching	Strobe Associated With the Group	Strobe to Assoc. Address Signal Matching	Notes
REQ[4:0]#, A[16:3]#	± 200 mils	ADSTB0#	± 200 mils	1,2,3
A[31:17]#	± 200 mils	ADSTB1#	± 200 mils	1,2,3

NOTES:
1. ADSTB[1:0]# should be should be trace length matched to the average length of their associated Address signals group
2. Each Address signal should be trace length matched to its associated Address Strobe within ± 200 mils.
3. Note that all length matching formulas are based on GMCH die-pad to processor pin total length per signal group. Package length table are provided for all signals in order to facilitate this pad to pin matching.

Table 7 lists the source synchronous address signals general routing requirements. They should be routed to a pin-to-pin length minimum of 0.50 inches and maximum of 6.5 inches. Due to the 200-MHz, high frequency operation of the address signals, the routing guidelines listed in Table 7 allows for 2:1 spacing for the address signals given a 55 Ω ± 15% characteristic trace impedance except for address strobe signals. But if space permits, 3:1 spacing is strongly advised for these signals.

Table 7. Processor PSB Source Synchronous Address Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance (Ω)	Width & Spacing (mils)
Address Group #1	Address Group #2		Min (inches)	Max (inches)		
A[16:3]#	A[31:17]#	Strip-line	0.50	6.5	55 ± 15%	4 & 8
REQ[4:0]#		Strip-line	0.50	6.5	55 ± 15%	4 & 8
ADSTB#[0]	ADSTB#[1]	Strip-line	0.50	6.5	55 ± 15%	4 & 12

4.1.3.5. Intel Pentium M / Intel Celeron M Processor and Intel 855GM/GME Chipset GMCH PSB Signal Package Lengths

Table 8 lists the preliminary package trace lengths of the Intel Pentium M / Intel Celeron M processor and the Intel 855GM/GME chipset GMCH for the source synchronous data and address signals. The processor PSB package signals within the same group are **routed** to the same package trace length, but the GMCH package signals within the same group are **not routed** to the same package trace length. As a result of this package length compensation is required for GMCH. Refer to Section 4.1.3.1 for length matching constrains and to Section 4.1.3.2 package length compensation for further details. The processor package traces are routed as micro-strip lines with a nominal characteristic impedance of 55 Ω ± 15%.

Table 8. Intel Pentium M / Intel Celeron M Processor and GMCH Source Synchronous FSB Signal Package Lengths

Signal Group	CPU Signal Name	CPU Package Length (mils)	GMCH Signal Name	GMCH Package Length (mils)	Signal Group	CPU Signal Name	CPU Package Length (mils)	GMCH Signal Name	GMCH Package Length (mils)
Data Group 1	D15#	721	HD15#	554	Data Group 2	D31#	564	HD31#	914
	D14#	721	HD14#	393		D30#	564	HD30#	464
	D13#	721	HD13#	494		D29#	564	HD29#	691
	D12#	721	HD12#	620		D28#	564	HD28#	768
	D11#	721	HD11#	319		D27#	564	HD27#	453
	D10#	721	HD10#	504		D26#	564	HD26#	815
	D9#	721	HD9#	438		D25#	564	HD25#	837
	D8#	721	HD8#	458		D24#	564	HD24#	493
	D7#	721	HD7#	329		D23#	564	HD23#	766
	D6#	721	HD6#	518		D22#	564	HD22#	731
	D5#	721	HD5#	693		D21#	564	HD21#	522
	D4#	721	HD4#	600		D20#	564	HD20#	714
	D3#	721	HD3#	387		D19#	564	HD19#	412
	D2#	721	HD2#	438		D18#	564	HD18#	834
	D1#	721	HD1#	620		D17#	564	HD17#	634
	D0#	721	HD0#	329		D16#	564	HD16#	593
	DINV[0]#	721	DINV[0]#	514		DINV[1]#	564	DINV[1]#	628
	DSTBP[0]#	721	HDSTBP[0]#	662		DSTBP[1]#	564	HDSTBP[1]#	736
	DSTBN[0]#	721	HDSTBN[0]#	763		DSTBN[1]#	564	HDSTBN[1]#	787
Data Group 3	D47#	661	HD47#	654	Data Group 4	D63#	758	HD63#	579
	D46#	661	HD46#	647		D62#	758	HD62#	509
	D45#	661	HD45#	460		D61#	758	HD61#	431
	D44#	661	HD44#	563		D60#	758	HD60#	522
	D43#	661	HD43#	726		D59#	758	HD59#	490
	D42#	661	HD42#	828		D58#	758	HD58#	347
	D41#	661	HD41#	608		D57#	758	HD57#	649
	D40#	661	HD40#	358		D56#	758	HD56#	372
	D39#	661	HD39#	655		D55#	758	HD55#	541
	D38#	661	HD38#	619		D54#	758	HD54#	598
	D37#	661	HD37#	747		D53#	758	HD53#	469
	D36#	661	HD36#	633		D52#	758	HD52#	575
	D35#	661	HD35#	675		D51#	758	HD51#	326
	D34#	661	HD34#	683		D50#	758	HD50#	549
	D33#	661	HD33#	501		D49#	758	HD49#	511
	D32#	661	HD32#	664		D48#	758	HD48#	372
	DINV[2]#	661	DINV[2]#	784		DINV[3]#	758	DINV[3]#	431

Signal Group	CPU Signal Name	CPU Package Length (mils)	GMCH Signal Name	GMCH Package Length (mils)	Signal Group	CPU Signal Name	CPU Package Length (mils)	GMCH Signal Name	GMCH Package Length (mils)
	DSTBP[2]#	661	HDSTBP[2]#	502		DSTBP[3]#	758	HDSTBP[3]#	463
	DSTBN[2]#	661	HDSTBN[2]#	538		DSTBN[3]#	758	H DSTBN[3]#	505
Addr Group 1	REQ4#	616	HREQ4#	276	Addr Group 2	A31#	773	HA31#	617
	REQ3#	616	HREQ3#	383		A30#	773	HA30#	484
	REQ2#	616	HREQ2#	247		A29#	773	HA29#	558
	REQ1#	616	HREQ1#	378		A28#	773	HA28#	579
	REQ0#	616	HREQ0#	569		A27#	773	HA27#	631
	A16#	616	HA16#	491		A26#	773	HA26#	556
	A15#	616	HA15#	375		A25#	773	HA25#	535
	A14#	616	HA14#	562		A24#	773	HA24#	353
	A13#	616	HA13#	501		A23#	773	HA23#	382
	A12#	616	HA12#	522		A22#	773	HA22#	545
	A11#	616	HA11#	566		A21#	773	HA21#	429
	A10#	616	HA10#	560		A20#	773	HA20#	414
	A9#	616	HA9#	327		A19#	773	HA19#	284
	A8#	616	HA8#	333		A18#	773	HA18#	389
	A7#	616	HA7#	274		A17#	773	HA17#	457
	A6#	616	HA6#	523		ADSTB[1]#	773	HADSTB[1]#	504
	A5#	616	HA5#	551	Host Clocks	BCLK0	447	BCLK	1138
	A4#	616	HA4#	352		BCLK1	447	BCLK#	1145
	A3#	616	HA3#	468					
	ADSTB[0]#	616	HADSTB[0]#	419					

4.1.4. Asynchronous Signals

The following sections describe the topologies and layout recommendations for the Asynchronous Open Drain and CMOS signals found on the platform. All Open Drain signals listed in the following sections must be pulled-up to VCCP (1.05 V). If any of these Open Drain signals are pulled-up to a voltage higher than VCCP, the reliability and power consumption of the processor may be affected. Therefore, it is very important to follow the recommended pull-up voltage for these signals. All signals must meet the AC and DC specifications as documented in the *Mobile Intel® Pentium® M Processor Datasheet*.

Table 9. Asynchronous AGTL+ Nets

Signal Names	Description	Topology #	CPU IO Type	Output	Output Buffer Type	Input	Input Power Well
IERR#	Internal error	1A	O	CPU	AGTL+	System Receiver	Vcc_Receiver
FERR#	Floating point error	1B	O	CPU	AGTL+	ICH4-M	Main I/O (3.3 V)
THRMTRIP#	Thermal sensor	1B	O	CPU	AGTL+	System Receiver	Vcc_Receiver
PROCHOT#	Thermal sensor	1C	O	CPU	AGTL+	System Receiver	Vcc_Receiver
PWRGOOD	System power good	2A	I	ICH4-M	OD CMOS	CPU	N/A
DPSLP#	Deep sleep	2B	I	ICH4-M	CMOS	CPU	N/A
LINT0/INTR	Local interrupts	2C	I	ICH4-M	CMOS	CPU	N/A
LINT1/NMI	Local interrupts	2C	I	ICH4-M	CMOS	CPU	N/A
SLP#	Sleep	2C	I	ICH4-M	CMOS	CPU	N/A
STPCLK#	Processor stop clock	2C	I	ICH4-M	CMOS	CPU	N/A
IGNNE#	Ignore next numeric error	2C	I	ICH4-M	CMOS	CPU	N/A
SMI#	System management interrupt	2C	I	ICH4-M	CMOS	CPU	N/A
A20M#	Address 20 mask	2C	I	ICH4-M	CMOS	CPU	N/A
INIT#	Processor initialize	3	I	ICH4-M	CMOS	CPU, FWH	N/A, 3.3V

4.1.4.1. Topology 1A: Open Drain (OD) Signals Driven by the Processor – IERR#

The Topology 1A OD signal IERR# should adhere to the following routing and layout recommendations. Table 10 lists the recommended routing requirements for the IERR# signal of the processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/ undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V). Due to the dependencies on system design implementation, IERR# can be implemented in a number of ways to meet design goals. IERR# can be routed as a test point or to any optional system receiver.

Figure 9. Routing Illustration for Topology 1A

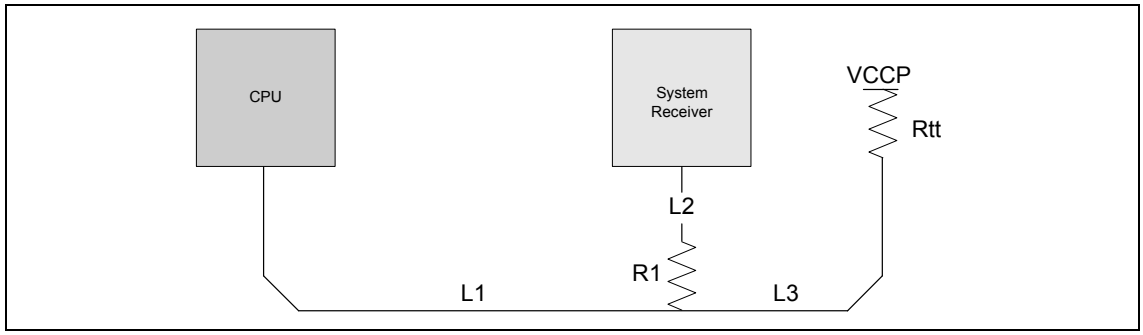


Table 10. Layout Recommendations for Topology 1A

L1	L2	L3	R1	Rtt	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 Ω ± 5%	56 Ω ± 5%	Micro-strip
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 Ω ± 5%	56 Ω ± 5%	Strip-line

4.1.4.2. Topology 1B: Open Drain (OD) Signals Driven by the Processor – FERR# and THERMTRIP#

The Topology 1B OD signals FERR# and THERMTRIP# should adhere to the following routing and layout recommendations. Table 11 lists the recommended routing requirements for the FERR# and THERMTRIP# signals of the processor. The routing guidelines allow the signals to be routed as either micro-strips or strip-lines using 55 Ω ± 15% characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V).

Intel recommends that the FERR# signal of the processor be routed to the FERR# signal of the ICH4-M. THERMTRIP# can be implemented in a number of ways to meet design goals. It can be routed to the ICH4-M or any optional system receiver. It is recommended that the THERMTRIP# signal of the processor be routed to the THRMTRIP# signal of the ICH4-M. The ICH4-M’s THRMTRIP# signal is a new signal to the I/O controller hub architecture that allows the ICH4-M to quickly put the whole system into a S5 state whenever the catastrophic thermal trip point has been reached.

If either FERR# or THERMTRIP# is routed to an optional system receiver rather than the ICH4-M and the interface voltage of the optional system receiver does not support a 1.05-V voltage swing, then a voltage translation circuit must be used. If the recommended voltage translation circuit described in Section 4.1.4.8 is used, the driver isolation resistor shown in Figure 16, Rs, should replace the series

dampening resistor R1 in Topology 1B. Thus, it is important to note that R1 will no longer be required in such a topology.

Figure 10. Routing Illustration for Topology 1B

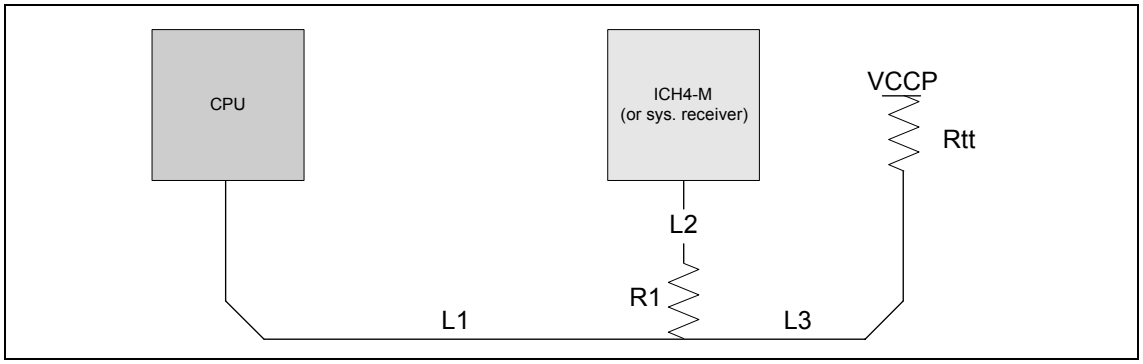


Table 11. Layout Recommendations for Topology 1B

L1	L2	L3	R1	Rtt	Transmission Line
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	56 Ω ± 5%	56 Ω ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	56 Ω ± 5%	56 Ω ± 5%	Strip-line

4.1.4.3. Topology 1C: Open Drain (OD) Signals Driven by the Processor – PROCHOT#

The Topology 1C OD signal PROCHOT# should adhere to the following routing and layout recommendations. Table 12 lists the recommended routing requirements for the PROCHOT# signal of the processor. The routing guidelines allow the signal to be routed as either a micro-strip or strip-line using 55 Ω ± 15% characteristic trace impedance. Figure 11 shows the recommended implementation for providing voltage translation between the processor's PROCHOT# signal and a system receiver that utilizes a 3.3-V interface voltage (shown as V_IO_RCVR). The receiver at the output of the voltage translation circuit can be any system receiver that can function properly with the PROCHOT# signal given the nature and usage model of this pin. PROCHOT# is capable of toggling hundreds of times per second to signal a hot temperature condition.

Series resistor Rs is a component of the voltage translation logic and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 16. Rs should be placed at the beginning of the T-split from the PROCHOT# signal. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V).

Figure 11. Routing Illustration for Topology 1C

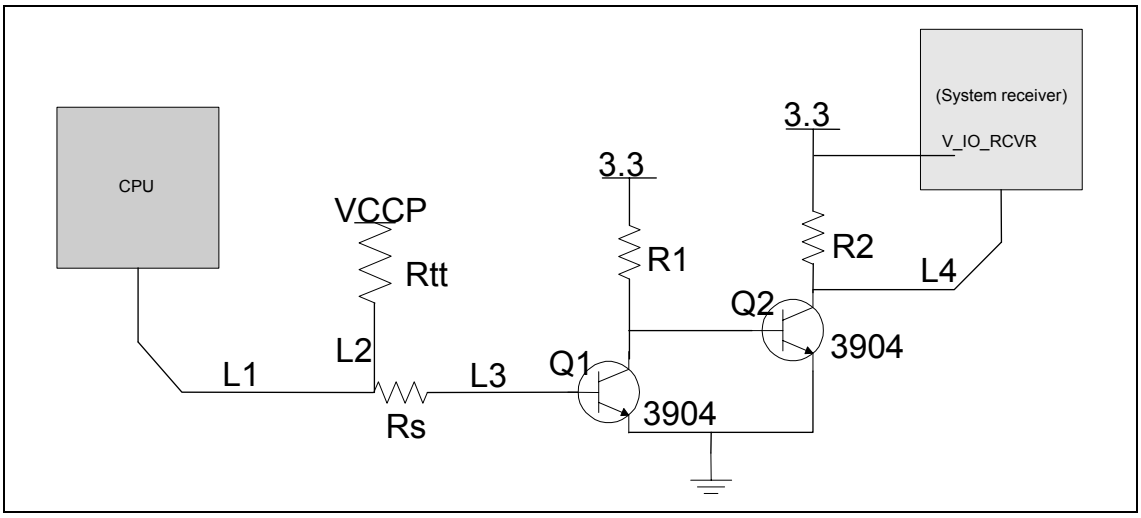


Table 12. Layout Recommendations for Topology 1C

L1	L2	L3	L4	Rs	R1	R2-	Rtt	Transmission
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	0.5” – 12.0”	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	56 Ω ± 5%	Micro-strip
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	0.5” – 12.0”	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	56 Ω ± 5%	Strip-line

4.1.4.4. Topology 2A: Open Drain (OD) Signals Driven by ICH4-M – PWRGOOD

The Topology 2A OD signal PWRGOOD, which is driven by the ICH4-M (CMOS signal input to processor) should adhere to the following routing and layout recommendations. Table 13 lists the recommended routing requirements for the PWRGOOD signal of the processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. The pull-up voltage for termination resistor Rtt is VCCP (1.05 V).

Note: The ICH4-M’s CPUPWRGD signal should be routed point-to-point to the processor’s PWRGOOD signal. The routing from the processor’s PWRGOOD pin should fork out to both to the termination resistor, Rtt, and the ICH4-M. Segments L1 and L2 from Table 13 should not T-split from a trace from the pin.

Figure 12. Routing Illustration for Topology 2A

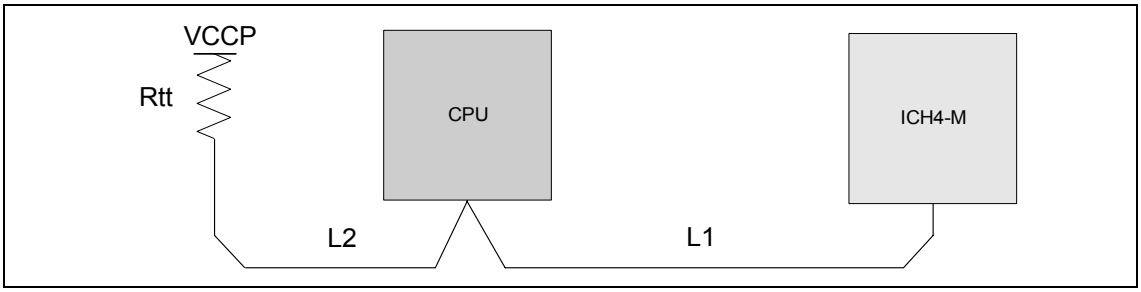


Table 13. Layout Recommendations for Topology 2A

L1	L2	Rtt	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	330 Ω ± 5%	Micro-strip
0.5” – 12.0”	0” – 3.0”	330 Ω ±5%	Strip-line

4.1.4.5. Topology 2B: CMOS Signals Driven by ICH4-M – DPSLP#

The Topology 2B CMOS DPSLP# signal, which is driven by the ICH4-M (CMOS signal input to the processor), should adhere to the routing and layout recommendations illustrated in Figure 13. As listed in Figure 13, the L1 and L2 segments of the DPSLP# signal topology can be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance.

Note: The ICH4-M’s DPSLP# signal should be routed point-to-point with the daisy chain topology shown. The routing of DPSLP# at the CPU should fork out to both the ICH4-M and the GMCH. Segments L1 and L2 from Figure 13 should not T-split from a trace from the pin.

Figure 13. Routing Illustration for Topology 2B

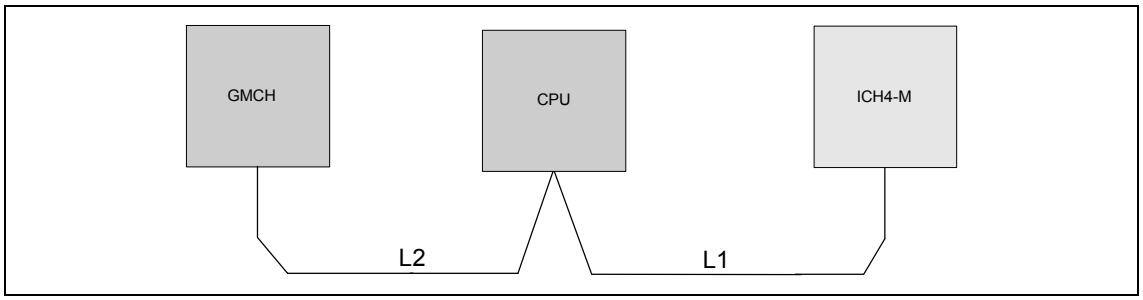


Table 14. Layout Recommendations for Topology 2B

L1	L2	Transmission Line Type
0.5” – 12.0”	0.5” – 6.5”	Micro-strip
0.5” – 12.0”	0.5” – 6.5”	Strip-line

4.1.4.6. Topology 2C: CMOS Signals Driven by ICH4-M – LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK#

The Topology 2C CMOS LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK# signals should implement a point-to-point connection between the ICH4-M and the processor. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. No additional motherboard components are necessary for this topology.

Figure 14. Routing Illustration for Topology 2C

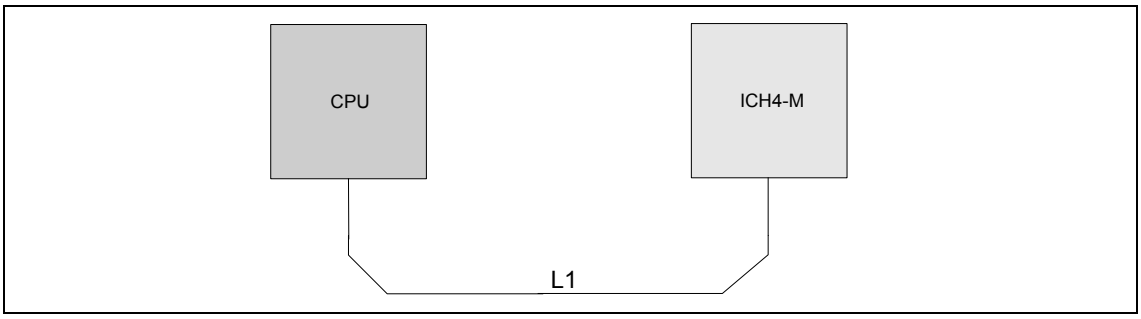


Table 15. Layout Recommendations for Topology 2C

L1	Transmission Line Type
0.5” – 12.0”	Micro-strip
0.5” – 12.0”	Strip-line

4.1.4.7. Topology 3: CMOS Signals Driven by ICH4-M to CPU and FWH – INIT#

The signal INIT# should adhere to the following routing and layout recommendations. Table 16 lists the recommended routing requirements for the INIT# signal of the ICH4-M. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 55 Ω ± 15% characteristic trace impedance. Figure 15 shows the recommended implementation for providing voltage translation between the ICH4-M’s INIT# voltage signaling level and any firmware hub (FWH) that utilizes a 3.3-V interface voltage (shown as a supply V_IO_FWH). See Section 4.1.4.8 for more details on the voltage translator circuit.

Series resistor Rs is a component of the voltage translator logic circuit and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance of L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 16. The routing recommendations of transmission line L3 in Figure 15 is listed in Table 16 and Rs should be placed at the beginning of the T-split of the trace from the ICH4-M’s INIT# pin.

Figure 15. Routing Illustration for Topology 3

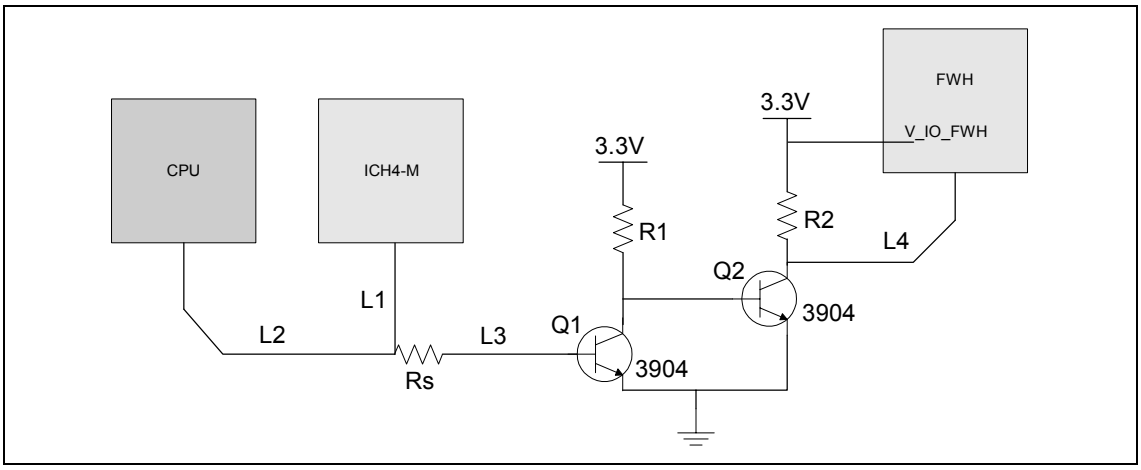


Table 16. Layout Recommendations for Topology 3

L1 + L2	L3	L4	Rs	R1	R2	Transmission Line
0.5" – 12.0"	0" – 3.0"	0.5" – 6.0"	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	0.5" – 6.0"	330 Ω ± 5%	1.3 kΩ ± 5%	330 Ω ± 5%	Strip-line

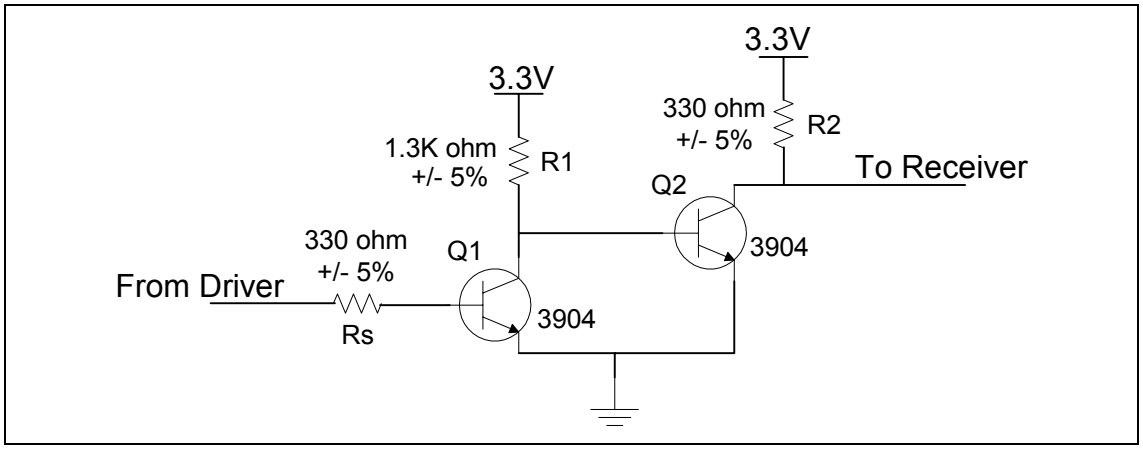
4.1.4.8. Voltage Translation Logic

A voltage translation circuit or component is required on any signals where the voltage signaling level between two components connected by a transmission line may cause unpredictable signal quality. The recommended voltage translation circuit for the platform is shown in Figure 16. The driver isolation resistor, Rs, is place at the beginning of a transmission line that connects to the first bipolar junction transistor, Q1. Though the circuit shown in Figure 16 was developed to work with signals that require translation from a 1.05-V to a 3.3-V voltage level, the same topology and component values, in general, can be adapted for use with other signals as well, provided the interface voltage of the receiver is also 3.3 V. Any component value changes or component placement requirements for other signals must be simulated in order to guarantee good signal quality and acceptable performance from the circuit.

In addition to providing voltage translation between driver and receiver devices, the recommended circuit also provides filtering for noise and electrical glitches. A larger first-stage collector resistor, R1, can be used on the collector of Q1, however, it will result in a slower response time to the output falling edge. In the case of the INIT# signal, resistors with value*s as close as possible to those listed in Figure 16 should be used without exception.

With the low 1.05-V signaling level of the Intel Pentium M / Intel Celeron M Front Side Bus, the voltage translation circuit provides ample isolation of any transients or signal reflections at the input of transistor Q1 from reaching the output of transistor Q2. Based on simulation results, the voltage translation circuit can effectively isolate transients as large as 200 mV and that last as long as 60 ns.

Figure 16. Voltage Translation Circuit

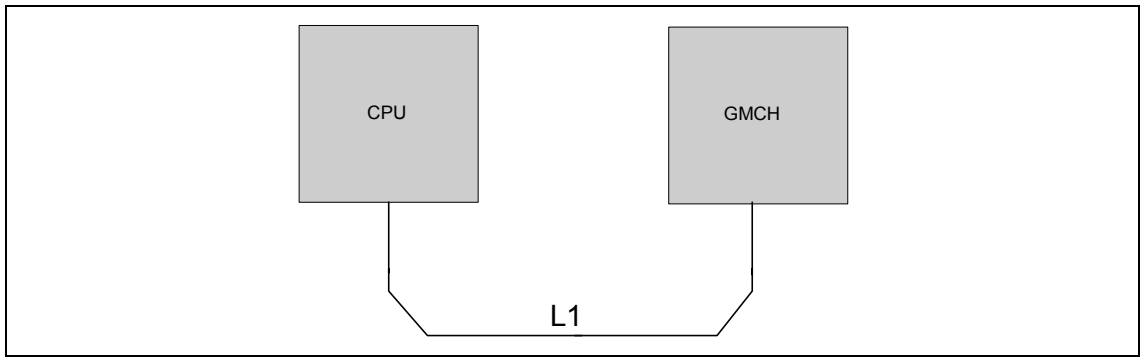


4.1.5. Processor RESET# Signal

The RESET# signal is a common clock signal driven by the GMCH CPURST# pin. In a production system where no ITP700FLEX debug port is implemented, a simple point-to-point connection between the CPURST# pin of the GMCH and processor RESET# pin is recommended (see Figure 17). On-die

termination of the AGTL+ buffers on both the processor and the GMCH provide proper signal quality for this connection. This is the same case as for the other common clock signals listed Section 4.1.2. Length L1 of this interconnect should be limited to minimum of 1 inch and maximum of 6.5 inches.

Figure 17. Processor RESET# Signal Routing Topology with NO ITP700FLEX Connector



For a system that implements an ITP700FLEX debug port a more elaborate topology is required in order to guarantee proper signal quality at both the processor signal pad and the ITP700FLEX input receiver. In this case the topology illustrated in Figure 18 should be implemented. The CPURST# signal from the GMCH should fork out (do not route one trace from GMCH pin and then T-split) towards the processor's RESET# pin as well as towards the Rtt and Rs resistive termination network placed next to the ITP700FLEX debug port connector. Rtt (54.9 Ω + 1%) pulls-up to the VCCP voltage and is placed at the end of the L2 line that is limited to a 12-inch maximum length. Rs (22.6 Ω +/- 1%) should be placed right next to Rtt to minimize the routing between them in the vicinity of the ITP700FLEX connector to limit the L3 length to less than 0.5 inches. ITP700FLEX operation requires the matching of L2 + L3 - L1 length to the length of the BPM[4:0]# signals length within ± 250 mils. Refer to Section 0 for more details on ITP700FLEX signal routing. See Table 17 for routing length summary and termination resistor values.

Currently 1% tolerance resistors are recommended for Rs and Rtt. The use of 5% tolerant resistors for these resistors and whether it could provide adequate signal quality performance is under investigation.

Figure 18. Processor RESET# Signal Routing Topology with ITP700FLEX Connector

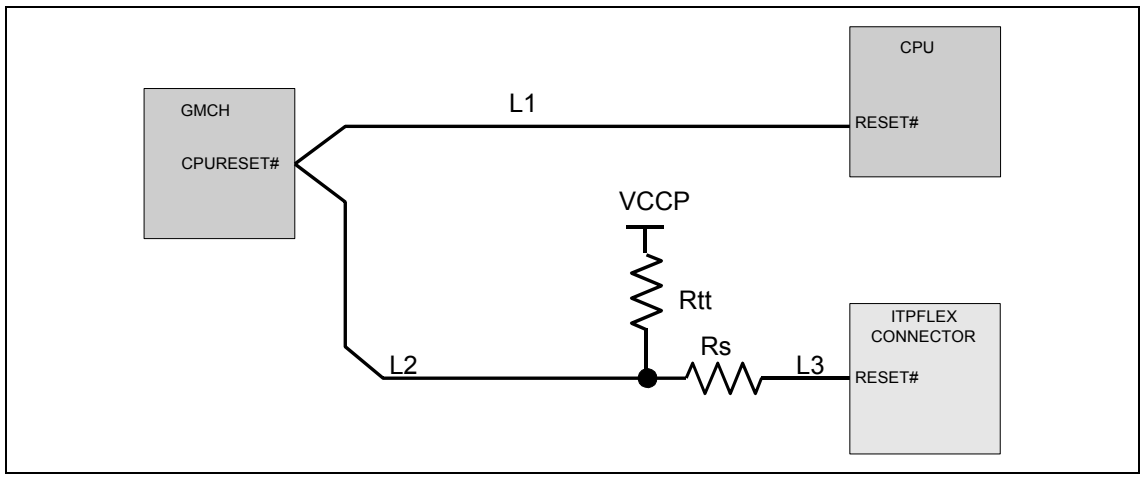


Table 17. Processor RESET# Signal Routing Guidelines with ITP700FLEX Connector

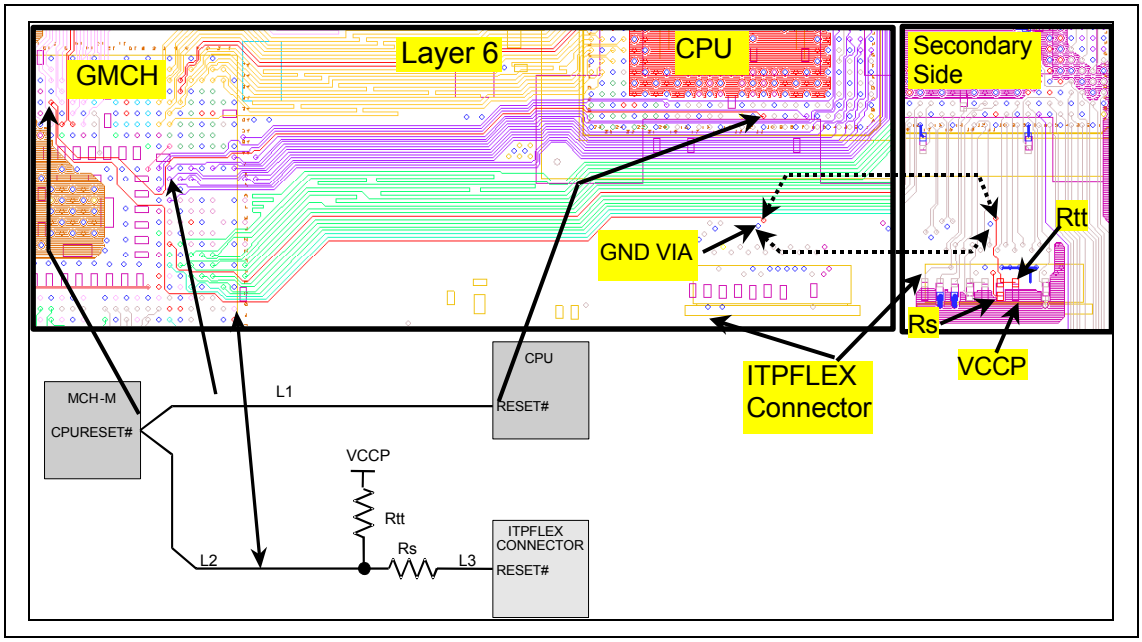
L1	L2 + L3	L3	Rs	Rtt
1.0” – 6.0”	6.0” max	0.5” max	Rs = 22.6 Ω ± 1%	Rtt = 220 Ω ± 5%

4.1.5.1. Processor RESET# Routing Example

Figure 19 illustrates a board routing example for the RESET# signal with an ITP700FLEX debug port implemented. It illustrates how the CPURST# pin of GMCH forks out into two branches on Layer 6 of the motherboard. One branch is routed directly to the processor RESET# pin amongst the rest of the common clock signals. Another branch routes below the address signals and vias down to the secondary side that route to the Rs and Rtt resistors. These resistors are placed in the vicinity of the ITP700FLEX debug port.

Note: The placement of Rs and Rtt next to each other is to minimize the routing between Rs and Rtt as well as the minimal routing between Rs and the ITP700FLEX connector. Also, since a transition between Layer 6 and the secondary side occurs, a GND stitching via is added to guarantee continuous ground reference of the secondary side routing of the RESET# signal to ITP700FLEX connector.

Figure 19. Processor RESET# Signal Routing Example with ITP700FLEX Debug Port



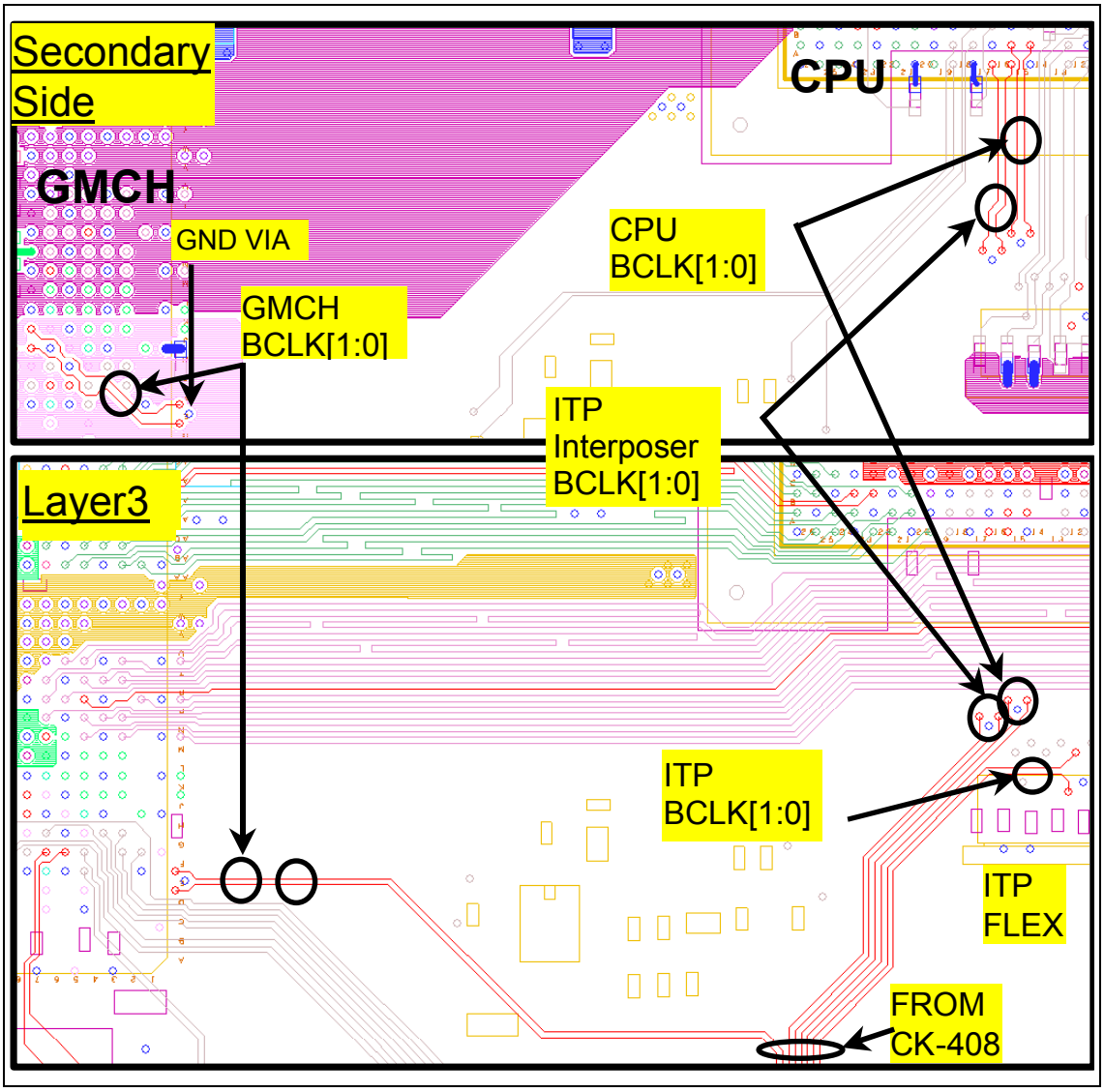
4.1.6. Processor and GMCH Host Clock Signals

Figure 20 illustrates processor and GMCH host clock signal routing. Both the processor and the GMCH’s BCLK[1:0] signals are initially routed from the CK-408 clock generator on Layer 3.In the recommended routing example (Figure 20) secondary side layer routing of BCLK[1:0] is 507 mils long. To meet length-matching requirements between the processor and GMCH’s BCLK[1:0] signals, a similar transition from Layer 3 to the secondary side layer is done next to the GMCH package outline. Routing of the GMCH’s BCLK[1:0] signals on the secondary side is also trace tuned to 507 mils.

BCLK[1:0] layer transition vias are accompanied by GND stitching vias. For similar reasons, routing for the ITP interposer's BCLK[1:0] signals also transition from Layer 3 to the secondary side layer and have 507-mil long traces on this layer. Throughout the routing length on Layer 3, BCLK[1:0] signals should reference a solid GND plane on Layer 2 and Layer 4 as shown in Figure 8.

If a system supports either the on-board ITP700FLEX connector or ITP Interposer only, then differential host clock routing to either the ITP700FLEX connector or CPU socket (but not both) is required.

Figure 20. Processor and GMCH Host Clock Layout Routing Example



4.1.7. Processor GTLREF Layout and Routing Recommendations

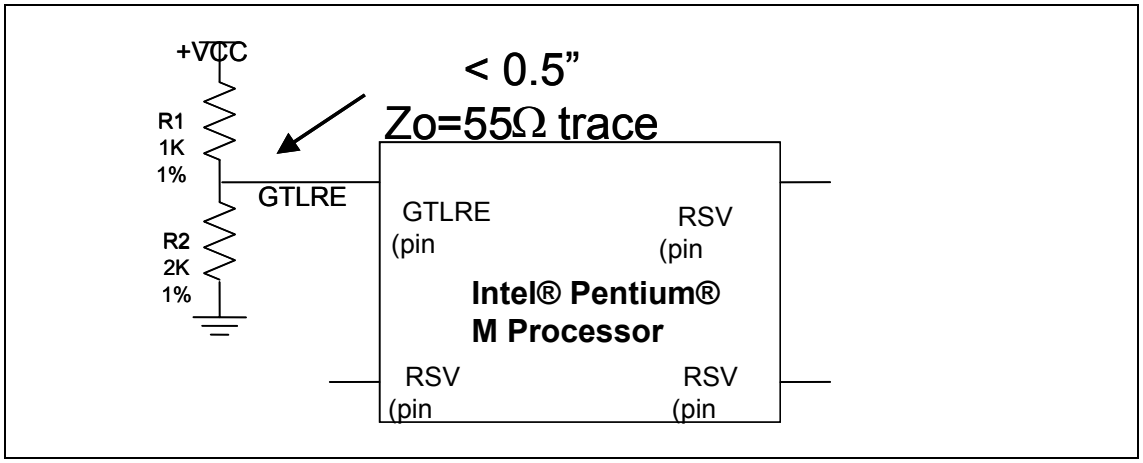
There is one AGTL+ reference voltage pin on the Intel Pentium M / Intel Celeron M processor, GTLREF, which is used to set the reference voltage level for the AGTL+ signals (GTLREF). The reference voltage must be supplied to the GTLREF pin. The voltage level that needs to be supplied to GTLREF must be equal to 2/3 * VCCP ± 2%. The GMCH also requires a reference voltage

(MCH_GTLREF) to be supplied to its HVREF[4:0] pins. The GTLREF voltage divider for both the processor and GMCH cannot be shared. Thus, both the processor and GMCH must have their own locally generated GTLREF networks. Figure 21 shows the recommended topology for generating GTLREF for the processor using a R1 = 1 kΩ ± 1% and R2 = 2 kΩ ± 1% resistive divider.

Since the input buffer trip point is set by the 2/3*VCCP on GTLREF and to allow tracking of VCCP voltage fluctuations, **no** decoupling should be placed on the GTLREF pin. The node between R1 and R2 (GTLREF) should be connected to the GTLREF pin of the processor with Zo = 55 Ω trace shorter than 0.5 inches. Space any other switching signals away from GTLREF with a minimum separation of 25 mils. Do not allow signal lines to use the GTLREF routing as part of their return path (i.e. do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the Processor System Bus signals).

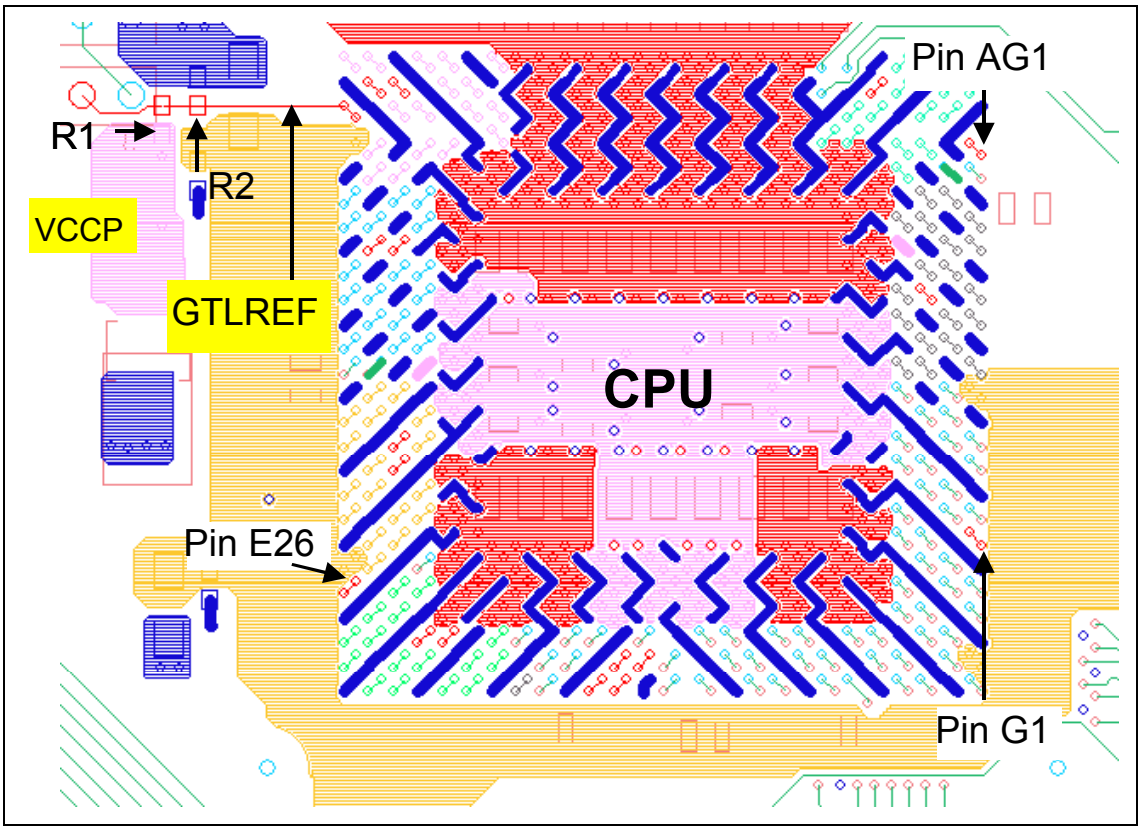
RSVD signal pins E26, G1, and AC1 are to be left unconnected on Intel® Pentium® M and Intel Celeron M processor-based systems.

Figure 21. Processor GTLREF Voltage Divider Network



A recommended layout of GTLREF for the processor is shown in Figure 22. To avoid interaction with PSB routing and power delivery, GTLREF's R1 and R2 components are placed next to each other on the primary side of the motherboard and connected with a Zo = 55 Ω to the GTLREF pin on the processor. The BGA ball lands on the primary side for the RSVD signal pins E26, G1, and AC1 are shown for illustrative purposes and are not routed.

Figure 22. Processor GTLREF Motherboard Layout



4.1.8. AGTL+ I/O Buffer Compensation

The Intel Pentium M / Intel Celeron M processor has 4 pins, COMP[3:0], and the GMCH has 2 pins, HRCOMP[1:0], that require compensation resistors to adjust the AGTL+ I/O buffer characteristics to specific board and operating environment characteristics. Also, the GMCH requires two special reference voltage generation circuits to pins HSWNG[1:0] for the same purpose described above. Refer to the *Intel® Pentium® M Processor Electrical, Mechanical, and Thermal Specification, Intel® Pentium® M (90nm process) Processor Electrical, Mechanical, and Thermal Specification,* and *RS – Intel® 855GM/GME (Montara-GM/GM+) Chipset GMCH External Design Specification* for details on resistive compensation.

4.1.8.1. Processor AGTL+ I/O Buffer Compensation

For the Intel Pentium M / Intel Celeron M processor, the COMP[2] and COMP[0] pins (see Figure 23) must each be pulled-down to ground with 27.4 Ω ± 1% resistors and should be connected to the processor with a Zo = 27.4 Ω trace that is less than 0.5 inches from the processor pins. The COMP[3] and COMP[1] pins (see Figure 24) must each be pulled-down to ground with 54.9 Ω ± 1% resistors and should be connected to the processor with a Zo = 55 Ω trace that is less than 0.5 inches from the processor pins. COMP[3:0] traces should be at least 25 mils (> 50 mils preferred) away from any other toggling signal.

Figure 23. Processor COMP[2] & COMP[0] Resistive Compensation

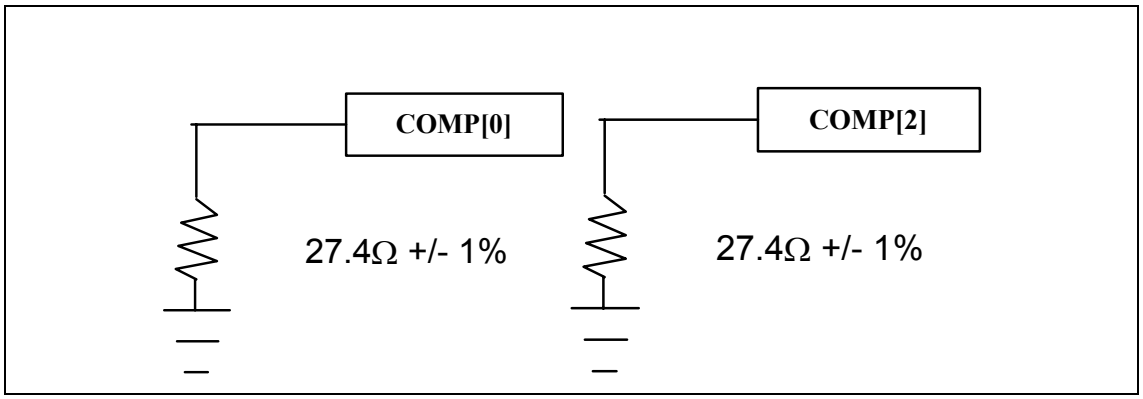
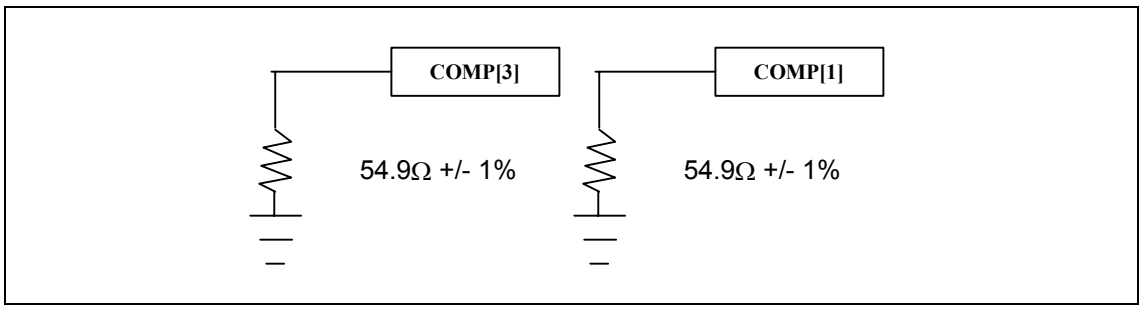


Figure 24. Processor COMP[3] & COMP[1] Resistive Compensation



The recommended layout of the processor COMP[3:0] resistors is illustrated in Figure 25. To avoid interaction with PSB routing on internal layers and VCCA power delivery on the primary side, Layer 1, COMP[1:0] resistors are placed on the secondary side. Ground connections to the COMP[1:0] resistors use a small ground flood on the secondary side layer and connect only with a single GND via to stitch the GND planes. The compact layout as shown in Figure 25 should be used to avoid excessive "perforation" of the V_{CCP} plane power delivery. Figure 25 illustrates how a 27.4 Ω resistor connects with an ~18-mil wide (Zo = 27.4 Ω) trace to COMP0. Necking down to 14 mils is allowed for a short length to pass in between the dog bones. The 54.9-Ω resistor connects with a regular 5-mil wide (Zo = 55 Ω) trace to COMP1. Placement of COMP[1:0] on the primary side is possible as well. An alternative placement implementation is shown in Figure 26.

To minimize motherboard space usage and produce a robust connection, the COMP[3:2] resistors are also placed on the secondary side (Figure 25, right side). A 27.4-Ω resistor connects with an 18-mil wide (Zo = 27.4 Ω) and 260-mil long trace to COMP2. Necking down to 14 mils is allowed for a short length to pass in between the dog bones. Notice that the COMP2 (Figure 25, left side) dog bone trace connection on the primary side is also widened to 14 mils to meet the Zo = 27.4-Ω characteristic impedance target. The right side of Figure 25 also illustrates how the 54.9 Ω ± 1% resistor connects with a regular 5-mil wide (Zo = 55Ω) and 100-mil long trace to COMP3. The ground connection of COMP[3:2] is done with a small flood plane on the secondary side that connects to the GND vias of pins AA1 and Y2 of the processor pin-map. This is done to avoid via interaction with the PSB routing on Layer 3 and Layer 6.

For COMP2 and COMP0, it is extremely important that 18-mil wide dog bone connections on the primary side and 18-mil wide traces on the secondary sides be used to connect the signals to

compensation resistors on the secondary side. The use of 18-mil wide dog bones and traces is used to achieve the Zo = 27.4-Ω target to ensure proper operation of the PSB. See Figure 27 for more details.

Figure 25. Processor COMP[3:0] Resistor Layout

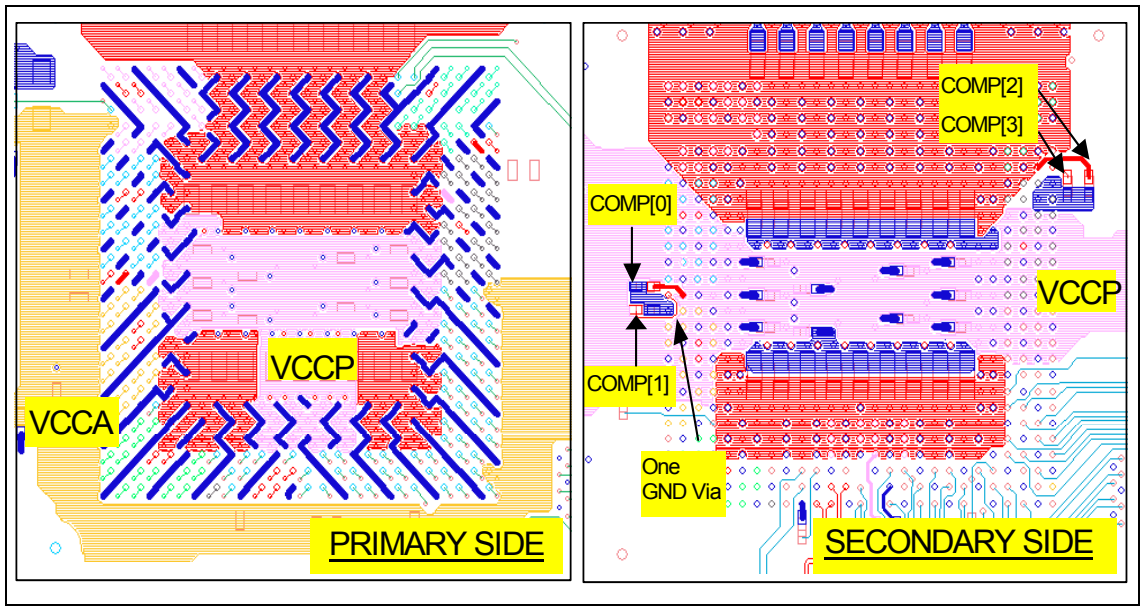


Figure 26. Processor COMP[1:0] Resistor Alternative Primary Side Layout

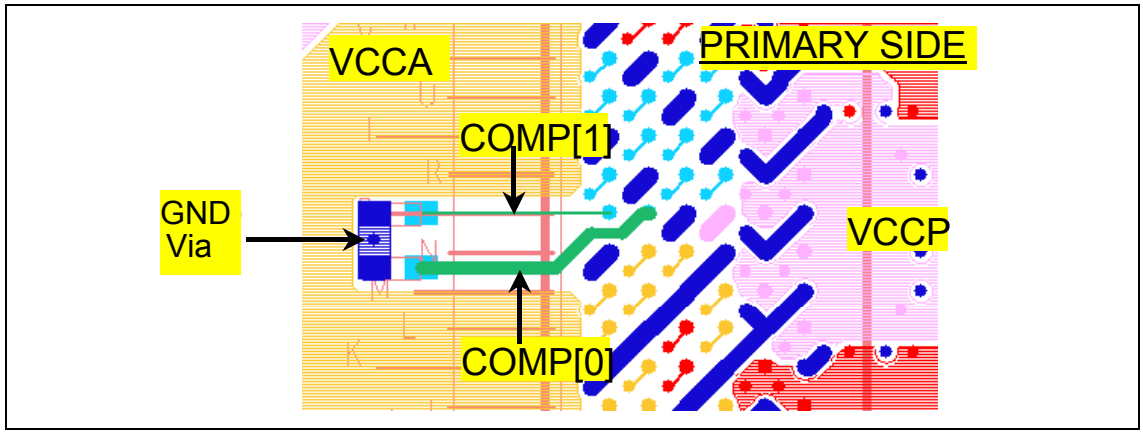
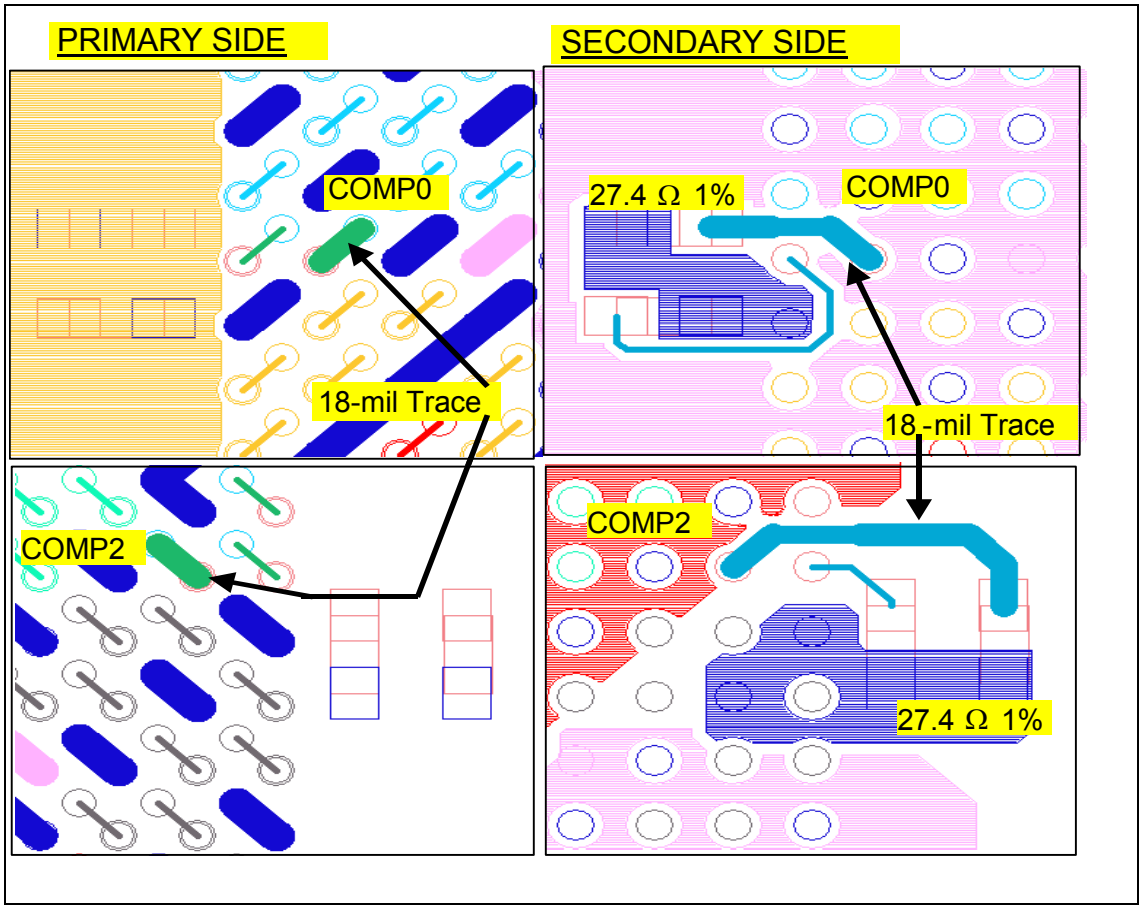


Figure 27. COMP2 & COMP0 27.4-Ω Traces



4.1.9. Intel Pentium M / Intel Celeron M Front Side Bus Strapping and Debug Port

The Intel Pentium M / Intel Celeron M processor and GMCH both have pins that require termination for proper component operation.

1. For the processor, a stuffing option should be provided for the TEST[3:1] pin to allow a 1 kΩ ± 5% pull-down to ground for testing purposes. For proper processor operation, the resistor should not be stuffed. Resistors for the stuffing option on these pins should be placed within 2.0 inches of the processor. For normal operation, these resistors should not be stuffed.
2. The processor's ITP signals, TDI, TMS, TRST and TCK should assume default logic values even if the ITP debug port is not used. The TDO signal may be left open or no connect in this case. The table below summarizes the default strapping resistors for these signals. These resistors should be connected to the processor within 2.0 inches from their respective pins. It is important to note that Table 18 is applicable only when neither the onboard ITP nor ITP interposer are planned to be used. See Section 4.3 on cautions against designs with lack of debug tools support. Intel does not recommend use of the ITP interposer debug port if there is a dependence only on the motherboard termination resistors. The signals below should be isolated from the motherboard via specific termination resistors on the ITP interposer itself per interposer debug port recommendations. For the case where the onboard ITP700FLEX debug port is used refer to Section 4.3 for default termination recommendations

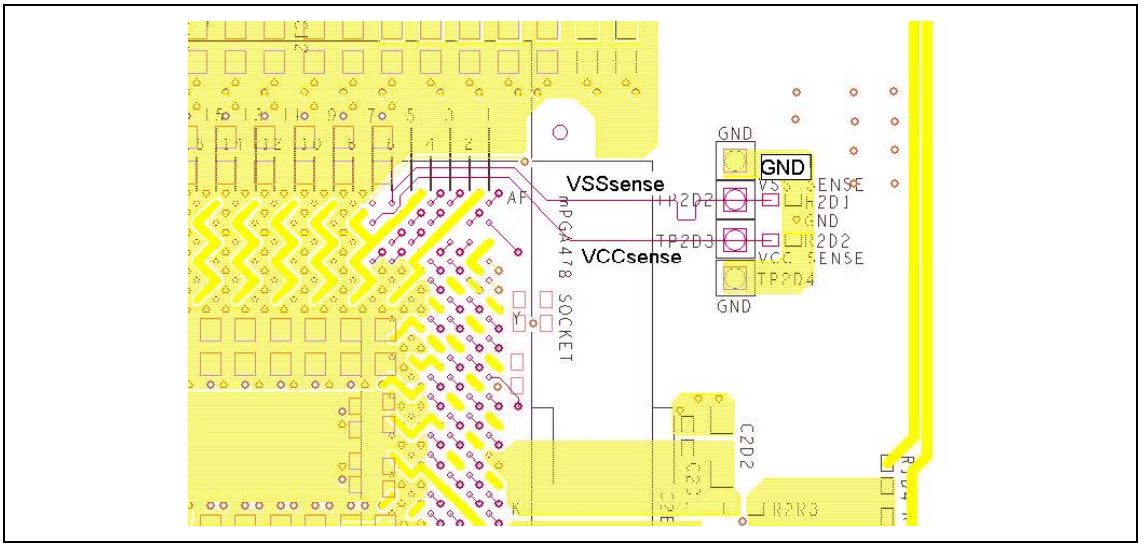
Table 18. ITP Signal Default Strapping When ITP Debug Port Not Used

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 Ω ± 5%	VCCP	Within 2.0” of the CPU
TMS	39 Ω ± 5%	VCCP	Within 2.0” of the CPU
TRST#	680 Ω ± 5%	GND	Within 2.0” of the CPU
TCK	27 Ω ± 5%	GND	Within 2.0” of the CPU
TDO	Open	NC	N/A

4.1.10. Processor $V_{CCSENSE}/V_{SSSENSE}$ Design Recommendations

The VCCSENSE and VSSSENSE signals of the Intel Pentium M processor and Intel Celeron M provide isolated, low impedance connections to the processor’s core power (VCC) and ground (VSS). These pins can be used to sense or measure power (VCC) or ground (VSS) near the silicon with little noise. To make them available for measurement purposes, it is recommended that VCCSENSE and VSSSENSE both be routed with a Zo = 55 Ω ± 15% trace of equal length. Use 3:1 spacing between the routing for the two signals and all other signals should be a minimum of 25 mils (preferably 50 mils) from VCCSENSE and VSSSENSE routing. Terminate each line with an optional (default is No Stuff) 54.9 Ω ± 1% resistor. Also, a ground via spaced 100 mils away from each of the test point vias for VCCSENSE and VSSSENSE should be added. A third ground via should also be placed in between them to allow for a differential probe ground. See Figure 28 for the recommended layout example.

Figure 28. $V_{CCSENSE}/V_{SSSENSE}$ Routing Example



4.2. Intel System Validation Debug Support

In any PC design, it is critical to enable industry-standard tools to allow for debug of a wide range of issues that come up in the normal design cycle. In a mobile design, electrical/logic visibility is very limited, often making progress on debugging such issues very time consuming. In some cases progress it not possible without board re-design or extensive rework. The following sections describe the three debug capabilities: ITP, LAI, and ODLAT.

4.2.1. ITP Support

4.2.1.1. Background/Justification

One key tool that is needed to debug BIOS, logic, signal integrity, general software, and general hardware issues involving CPUs, chipsets, SIOs, PCI devices, and other hardware in a platform design is the In Target Probe (ITP). The ITP is widely used by various validation, test, and debug groups within Intel (as well as by third party BIOS vendors, OEMs, and other developers).

It is extremely important to note that any Intel Pentium M Processor / Intel Celeron M Processor / Intel 855GM/GME chipset based systems designed without ITP support may prevent assistance from various Intel validation, test, and debug groups in debugging various issues. For this reason, it is a critical piece of insurance that ITP support is provided. This can be done with zero additional BOM cost and very minimal layout/footprint costs.

The cost for not providing this support vary, from no cost (if there are no blocking issues found in the system design) to schedule slips of a month or more. The latter scenario represents the time needed to spin a board design and required assembly time to add an ITP port when it is absolutely required and other mechanical and routing issues prevent the use of an ITP interposer, if one exists.

4.2.1.2. Implementation

To minimize the ITP connector footprint, the ITP700FLEX alternative is a better option for mobile designs. However, standard signal connection guidelines for the CPU's TAP logic signals for the non-ITP case still need to be followed. In other words, only the traces and component **footprints** need to be added to the design, with all previous "non-ITP" guidelines followed otherwise. This way, when ITP support is needed, the termination values and connector can be populated as needed for debug support. Note that if the ITP700FLEX footprint cannot be followed due to mechanical, routing, or footprint reasons, it is may be adequate to have a simple via grouping in lieu of the connector to allow for "blue-wiring" of the ITP, provided that footprints for the resistors are available on board and that the "blue-wiring" from the signal vias to the ITP700FLEX connector is as short as possible.

4.2.2. Intel Pentium M / Intel Celeron M Processor Logic Analyzer Support (FSB LAI)

4.2.2.1. Background/Justification

The Intel Pentium M / Intel Celeron M FSB Logic Analyzer probe (LAI) is the second key tool. It is widely used by various validation, test, and debug groups within Intel (as well as by third party BIOS vendors, OEMs, and other developers) and is needed to debug BIOS, logic, signal integrity, general software, and general hardware issues involving CPUs, chipsets, SIOs, PCI devices, and other hardware. For the processor, Agilent* Corporation will develop this tool and will likely be the only visibility to this critical system bus.

Note: Any Intel Pentium M processor / Intel Celeron M processor / Intel 855GM/GME chipset based systems designed without FSB LAI support may severely limit the ability of various Intel validation, test, and debug groups from debugging various issues in a reasonable amount of time.

Because support may be limited, it is critical that the following FSB LAI support is provided:

1. Provide a motherboard with a CPU socket. The FSB LAI is an interposer that plugs into the CPU socket, and the CPU then plugs into the LAI. The use of non-standard sockets may also prohibit the LAI from working as the locking mechanism may become inaccessible. It is important to check the LAI design guidelines to ensure a particular socket will work. Note that the LAI was designed to accommodate the most common (and at the time the only known) processor sockets on the market.
2. Observe FSB LAI keepout requirements. There are several options to achieving this. For example removing the motherboard from the case (typically the first step to meeting keepout requirements) or relocating any components that would otherwise be in the keepout area for debug purposes (i.e. axial lead devices that can be de-soldered and re-soldered to the other side of the board, parts that can be removed and blue-wired further away, etc.). If keepouts still cannot be met, Intel strongly recommends that a separate debug motherboard be built which has the same bill of material (BOM) and Netlist, but with FSB LAI keepout requirements met (this also gives the opportunity to add other test-points).

4.2.2.2. Implementation

Details from Agilent Corporation on the FSB LAI mechanicals (i.e. design guide with keepout volume info) are available for ordering. Please contact your local Intel field representative on how to obtain the latest design info. See Section 4.3.3 for more details.

4.2.3. Intel Pentium M / Intel Celeron M Processor On-Die Logic Analyzer Trigger (ODLAT) Support

The Intel Pentium M / Intel Celeron M processor provides support for 3 address/data recognizers on-die for setting on-die logic analyzer triggers (ODLAT) or breakpoints. Details from American Arium* on the ODLAT are currently available for ordering.

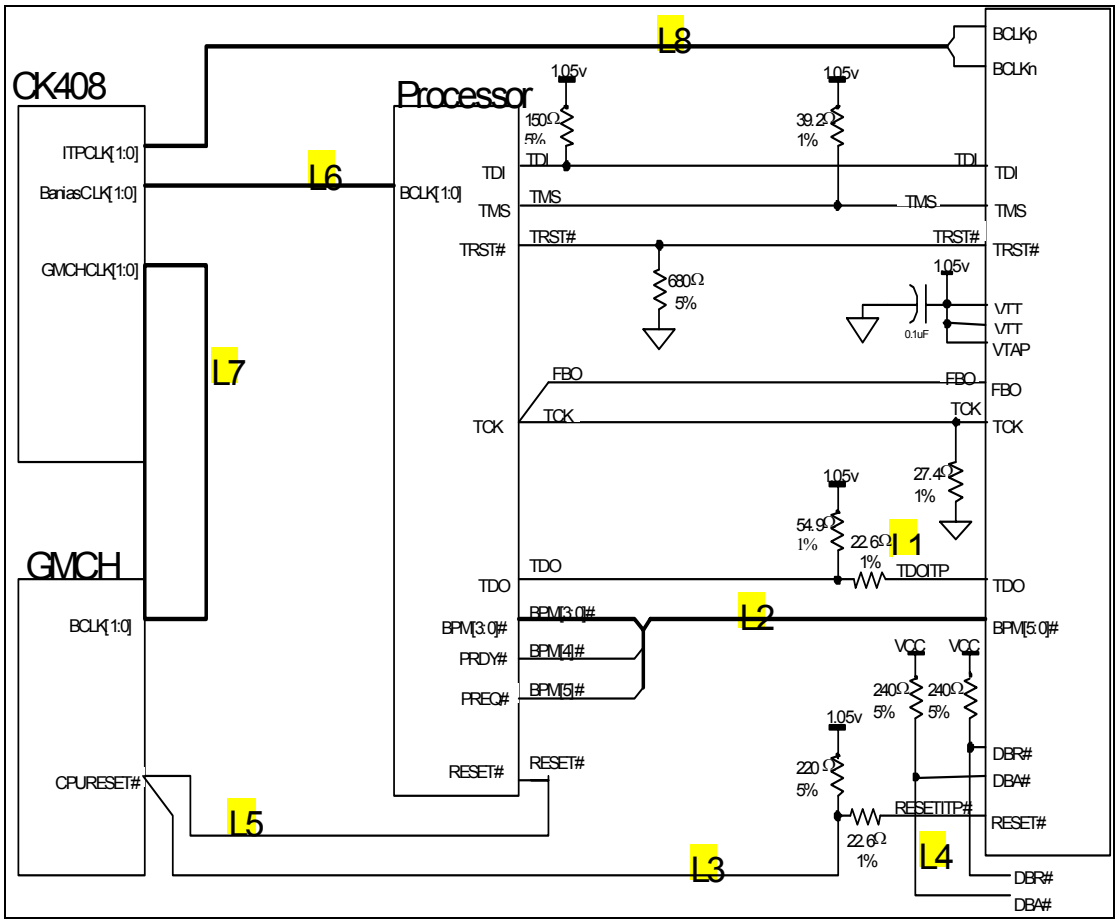
4.3. Onboard Debug Port Routing Guidelines

For systems incorporating the Intel Pentium M / Intel Celeron M processor, the debug port should be implemented as either an onboard debug port or via an interposer. Please reference the document *ITP700 Debug Port Design Guide*, which can be found on http://www.intel.com/design/Xeon/guides/24967912.pdf, for the most up to date information

4.3.1. ITP Signal Routing Guidelines

Figure 29 illustrates recommended connections between the onboard ITP700FLEX debug port, processor, GMCH, and CK-408 clock chip in the cases where the debug port is used.

Figure 29. ITP700FLEX Debug Port Signals



To connect to the debug port, follow the steps below:

1. Route the TDI signal between the ITP700FLEX connector and the processor. A 150-Ω ± 5% pull-up to VCCP (1.05 V) should be placed within ± 1.5" of the TDI pin.
2. Route the TMS signal between ITP700FLEX connector and the processor. A 39.2-Ω ± 1% pull-up to VCCP should be placed within ± 1" of the ITP700FLEX connector pin.
3. Route the TRST# signal between ITP700FLEX connector and the processor. A 510-Ω to 680-Ω ± 5% pull-down to ground should be placed on TRST#. Placement of the pull down resistor is not critical. Avoid having any trace stub from the TRST# signal line to the termination resistor.
4. Route the TCK signal from the ITP700FLEX connector's TCK pin to the processor's TCK pin and then fork back from the TCK pin and route back to ITP700FLEX connector's FBO pin. A 27.4-Ω ± 1% pull-down to ground should be placed within ± 1" of the ITP700FLEX connector pin.
5. Route the TDO signal from the processor to a 54.9-Ω ± 1% pull-up resistor to VCCP that should be placed close to ITP700FLEX connector's TDO pin. Then insert a 22.6-Ω ± 1% series resistor to connect the 54.9-Ω pull-up and the ITP connector (see Figure 29). Limit the L1 segment length of the TDOITP net to be less than 1.0 inch.

The processor drives the BPM[4:0]# signals to the ITP700FLEX at a 100-MHz clock rate. Route the BPM[4:0]# as a Zo=55 Ω point-to-point transmission line connection between the processor and the ITP700FLEX connector. Connect the ITP700FLEX connector's BPM[3:0]# pins to processor's BPM[3:0]# pins. Connect the ITP700FLEX's BPM[4]# signal to processor's PRDY# pin. The ITP700FLEX's integrated far-end terminations as well as the processor's AGTL+ integrated on-die

termination guarantee proper signal quality for the BPM[4:0]# signals. Due to the length of the ITP700FLEX cable, the length L2 of the BPM[4:0]# signals on the motherboard should be limited to be shorter than 6.0 inches. The BPM[4:0]# signals' length L2 should be length matched to each other within ± 250 mils. The BPM[4:0]# signal trace lengths are matched inside the processor package, thus motherboard routing does **not** need to compensate for any processor package trace length mismatch.

Due to the processor's AGTL+ on-die termination for BPM[3:0]# and PRDY#, there is no issue or concern if the BPM[4:0]# pins of the ITP700FLEX connector are left floating when the ITP is not being used and the ITP700FLEX cable is unplugged.

Route the ITP700FLEX connector's BPM[5]# signal as a Zo = 55 Ω point-to-point connection to the processor's PREQ# pin. Integrated on the ITP700FLEX BPM[5]# driver signal is a resistive pull-up that guarantees proper signal quality at the processor's PREQ# input pin. The processor has an integrated, weak, on-die pull-up to VCCP for the PREQ# signal to guarantee a proper logic level when the ITP700FLEX port connector is not plugged in. There is no need for any external termination on the motherboard for the BPM[5]# = PREQ# signal. The maximum length of BPM[5]#/PREQ# should not exceed 6.0 inches.

As explained in Sections 4.1.5, the RESET# signal forks (see Figure 17) out from the GMCH's CPURST# pin and is routed to the processor and ITP700FLEX debug port. One branch from the fork connects to the processor's RESET# pin and the second branch connects to a 220 W ± 5% termination pull-up resistor to VCCP placed close to the ITP700FLEX debug port. A series 22.6 W ± 1% resistor is used to continue the path to the ITP700FLEX RESET# pin with the RESETITP# net in Figure 28. The length of the RESETITP# net (labeled as net L4) should be limited to be less than 0.5 inches.

There is no need for pull-up termination on the processor side of the RESET# net due to presence of AGTL+ on-die termination on the processor and the GMCH.

The ITP700FLEX debug port's BCLK/BCLK# inputs are driven with a 100-MHz differential clock from the CK-408 clock chip. The CK-408 also feeds another two pairs of 100-MHz differential clocks to the processor BCLK[1:0] and the GMCH BCLK[1:0] input pins. Common clock signal timing requirements of the GMCH and the processor requires matching of processor and GMCH BCLK[1:0] nets L6 and L7, respectively. To guarantee correct operation of ITP700FLEX, the BCLK/BCLK# net L8 should be tuned to be within ± 250mils to the sum of length L6 of the BCLK[1:0] lines and the additional length L2 of the BPM#[4:0] signals.

i.e. L6 + L2 = L8 (within ± 250mils).

The timing requirements for the BPM[5:0]#, RESET#, and BCLK/BCLK# signals of the ITP700FLEX debug port requires careful attention to their routing. Standard high frequency bus routing practices should be observed.

1. Keep a minimum of 2:1 spacing in between these signals and to other signals.
2. Reference these signals to ground planes and avoid routing across power plane splits.
3. The number of routing layer transitions should be minimized. If layout constraints require a routing layer transition, any such transition should be accompanied with ground stitching vias placed within 100 mils of the signal via with at least one ground via for every two signals making a layer transition.

DBR# should be routed to the system reset logic (e.g. the SYSRST# signal of the ICH4-M) and initiate the equivalent of a front panel reset commonly found in desktop systems. The 150 Ω to 240 Ω pull-up resistor should be placed within 5.5" of the ITP700FLEX connector. Note that the CPU should **not** be power cycled when DBR# is asserted.

DBA# is an optional system signal that can be used to indicate to the system that the ITP/TAP port is being used. If not implemented, this signal can be left as no connect. If implemented, it should be routed with a 150 Ω to 240 Ω pull-up resistor placed within 5.5" of the ITP700FLEX connector. See the *ITP700 Debug Port Design Guide* for more details on DBA# usage.

The ITP700FLEX VTT and VTAP pins should be shorted together and connected to the VCCP (1.05 V) plane with a 0.1-µF decoupling capacitor placed within 0.1 inch of the VTT pins.

Table 19 summarizes termination resistors values, placement, and voltages the ITP signals need to connect to for proper operation for onboard ITP700FLEX debug port.

Table 19. Recommended ITP700FLEX Signal Terminations

Signal	Termination Value	Termination Voltage	Termination/Decap Location	Notes
TDI	150 Ω ± 5%	VCCP (1.05 V)	Within ± 1.5" of the CPU TDI pin	3
TMS	39.2 Ω ± 1%	VCCP (1.05 V)	Within ± 1" of the ITP700FLEX connector TMS pin	3
TRST#	510 – 680 Ω ± 5%	GND	Anywhere between CPU and ITP700FLEX connector	3
TCK	27.4 Ω ± 1%	GND	Within ± 1" of the ITP700 FLEX connector TCK pin	3
TDO	54.9 Ω ± 1% pull-up and 22.6 Ω ± 1% series resistor	VCCP (1.05 V)	Within 1" of the ITP700FLEX connector TDO pin	3
BCLK(p/n)				
FBO	Connect to TCK pin of CPU	N/A	N/A	
RESET#	220 Ω ± 5% pull-up and 22.6 Ω ± 1% series resistor	VCCP (1.05 V)	Within 0.5" of the ITP700FLEX connector RESET# pin	3
BPM[5:0]#	Not Required			1
DBA#	150-240 Ω ± 5%	VCC of target system recovery circuit.	Within 5.5" of the ITP700FLEX connector DBA# pin	2
DBR#	150-240 Ω ± 5%	VCC of target system recovery circuit	Within 5.5" of the ITP700FLEX connector DBR# pin	
VTAP	Short to VCCP plane	VCCP (1.05 V)		
VTT	Short to VCCP plane	VCCP (1.05 V)	Add 0.1-µF decap within 0.1 inch of VTT pins of ITP700FLEX connector	

NOTES:
1. All the needed terminations to guarantee proper signal quality are integrated inside the processor AGTL+ buffers or inside the ITP700FLEX debug port. No need for any external components for the BPM[5:0]# signals.
2. Only required if DBA# is used with any target system circuitry. This signal may be left unconnected if unused.
3. In cases where a system is designed to utilize the ITP700FLEX debug port for debug purposes but the ITP700FLEX connector may or may not be populated at all times although the signal routing and termination or decoupling components are implemented, the component placement guidelines should adhere to the ones listed in.

4.3.1.1. ITP Signal Routing Example

Figure 30 illustrates a recommended layout example for the ITP700FLEX signals. The ITP700FLEX connector is placed on the primary side of the motherboard and results in a smooth, straight-forward routing solution.

Note that the V_{CCP} (1.05 V) power delivery continues from the processor socket cavity on the secondary side of the motherboard through the pin field as shown on the right side of Figure 30. Three V_{CCP} vias in conjunction with three ground stitching vias allow a transition to the primary side to connect to the VTT and VTAP pins of the ITP700FLEX connector and also a transition back to the secondary side of the motherboard. A small V_{CCP} flood is created on the secondary side under the body of the ITP700FLEX connector with a 0.1-µF decoupling capacitor. This also provides a convenient connection for the 220-Ω pull-up for RESET#, the 54.9-Ω pull-ups for TDO, as well as the 39.2-Ω pull-up for the TMS signal.

Notice the very short trace from the 22.6-Ω series resistors for the RESET# and TDO signals to the ITP700FLEX pins. See also Section 4.1.5 for more details on RESET# signal routing.

The 150-Ω TDI pull-up is connected to the V_{CCP} (1.05 V) flood on the secondary side close to processor pin.

The ITP700FLEX TCK pin has a 27.4-Ω pull-down to ground very close to the ITP700FLEX connector and also routes to the processor's TCK pin and loops back with no stub to the FBO pin of the ITP700FLEX connector.

BCLK/BCLK# are routed in this example on Layer 3. For more BCLK/BCLK# routing details, refer to Figure 20 in Section 4.1.6.

4.3.1.2. ITP_CLK Routing to ITP700FLEX Connector

A layout example for ITP_CLK/ITP_CLK# routing to an ITP700FLEX connector is shown in Figure 30. The CK-408 clock chip is mounted on the primary side of the motherboard and the differential clock pair also breaks out on the same side. The differential ITP clock pair routing requires the use of a pair of 33-Ω ± 5% series resistors placed within 0.5 inches of the clock chip output pins followed by a pair of 49.9-Ω ± 1% termination resistors to ground. The ITP_CLK/ITP_CLK# signals are routed as a differential pair from the junction of the 33-Ω and 49.9-Ω ± 5% resistors across the internal Layer 6 through an open channel to the ITP700FLEX connector. Serpentining of the ITP_CLK traces is also performed in order to meet the ± 250 mils length matching requirement between ITP_CLK and the sum of length L6 of the BCLK[1:0] lines and the additional length L2 of the BPM#[5:0] signals in Figure 29. The ITP_CLK pair routing then switches back to the primary side layer through a via near the ITP700FLEX connector.

Figure 30. ITP700FLEX Signals Layout Example

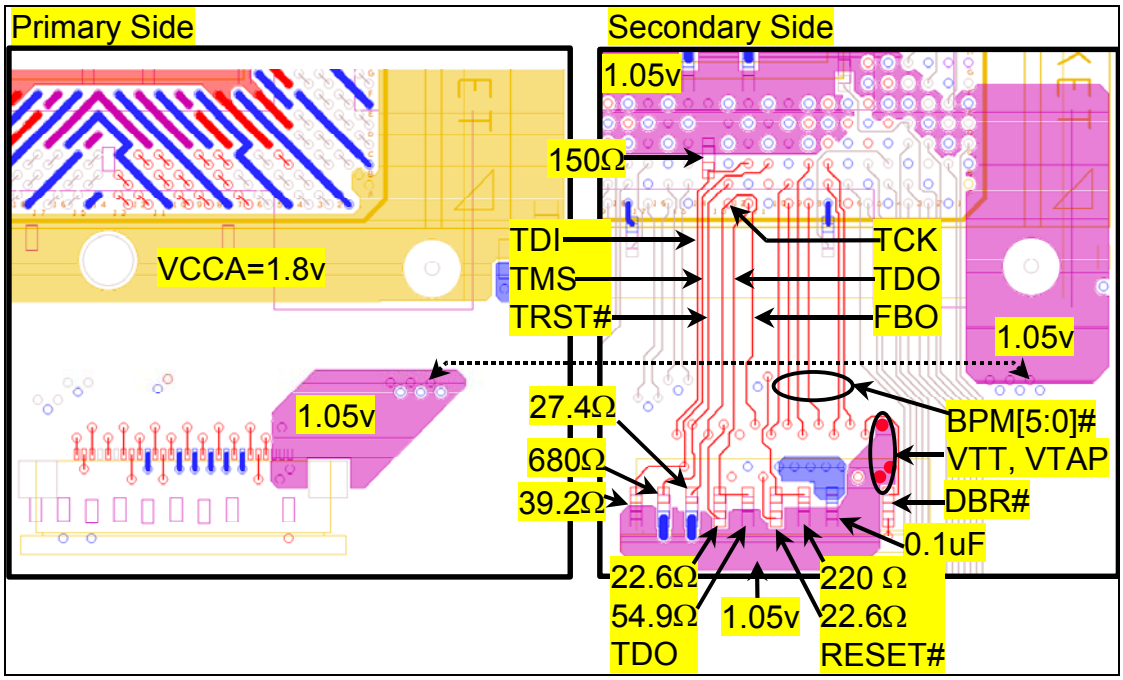
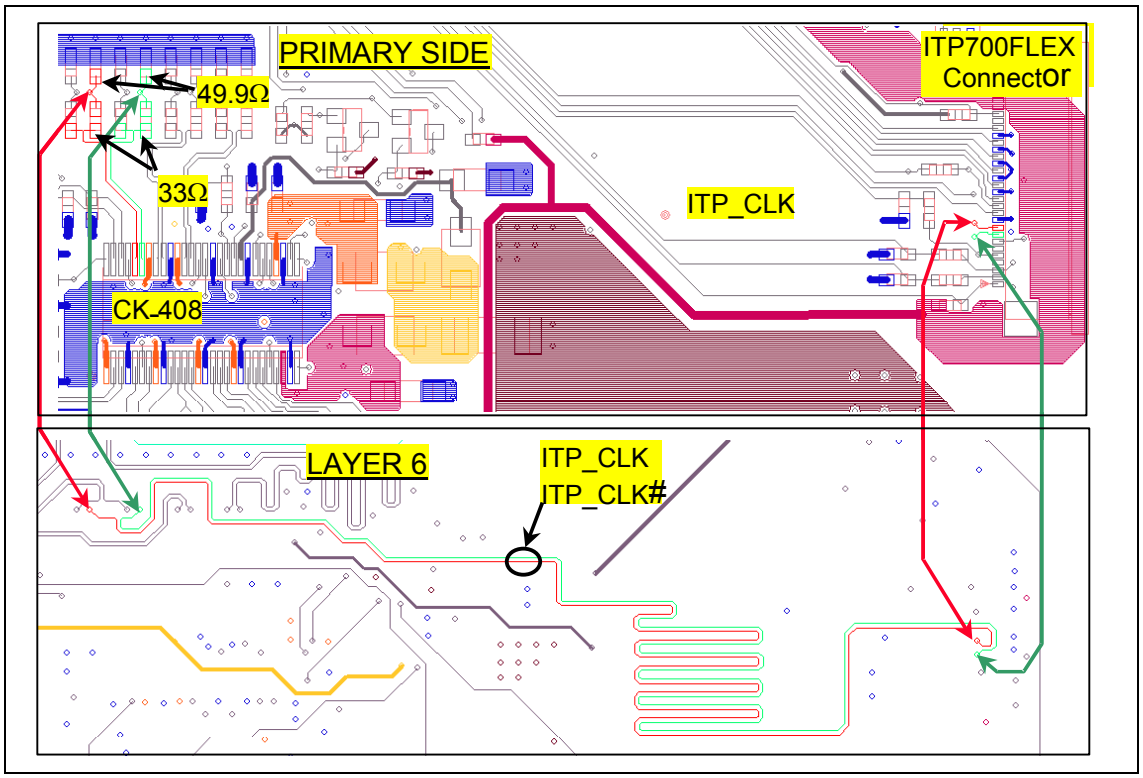


Figure 31. ITP_CLK to ITP700FLEX Connector Layout Example



4.3.1.3. ITP700FLEX Design Guidelines for Production Systems

For production systems that do not populate the onboard ITP700FLEX debug port connector, the following guidelines should be followed to ensure that all necessary signals are terminated properly.

Table 18 summarizes all the signals that require termination when a system does not populate the ITP700FLEX connector but still implements the routing for all the signals. This includes TDI, TMS, TRST#, and TCK. Based on the recommended values in this table, the resistor tolerances for TMS and TCK can be relaxed from ±1% to ±5% to reduce cost. Also, TDO can be left as a no connect, thus the 54.9 Ω ±1% pull-up and 22.6 Ω ±1% series resistors can be removed.

For the ITP700FLEX connector's RESET# input signal, the 220 Ω ±5% resistor should be removed as well as the 22.6 Ω ±1% series resistor.

The series 33 Ω and 49.5 Ω ±1% parallel termination resistors on the ITP_CLK/ITP_CLK# differential host clock inputs to the ITP700FLEX connector can also be depopulated for production systems. The only requirement is that the BIOS should disable the third differential host clock pair routed from the CK-408 clock chip to the ITP700FLEX connector.

Finally, the 150 Ω to 240 Ω pull-up resistor for the DBR# output signal from the ITP700FLEX connector may or may not be depopulated depending on how it affects the system reset logic that it is connected to. Thus, it is the responsibility of the system designer to determine whether termination for DBR# is required or not for a given system implementation. The same is also true for DBA#, if implemented. This signal is not required and can be left as no connect. However, it is the responsibility of the system designer to determine whether termination for DBA# is required or not.

4.3.2. Recommended ITP Interposer Debug Port Implementation

Intel is working with American Arium* to provide ITP interposer cards for use in debugging processor based systems as an alternative to the onboard ITP700FLEX in cases where the onboard connector cannot be supported. The ITP interposer card is an additional component that integrates the processor socket along with ITP700 connector on a single interposer card that is compatible with the 478-pin Intel Pentium M / Intel Celeron M processor socket.

Table 18 summarizes all the signals that require termination for a system designed for use with the ITP interposer. This includes TDI, TMS, TRST#, and TCK. TDO can be left as a no connect.

DBR# should be routed to the system reset logic (e.g. the SYSRST# signal of the ICH4-M) and initiate the equivalent of a front panel reset commonly found in desktop systems. The 150 Ω to 240 Ω pull-up resistor should be placed within 5.5" of the ITP connector. Note that the processor should **not** be power cycled when DBR# is asserted.

DBA# is an optional system signal that can be used to indicate to the system that the ITP/TAP port is being used. If not implemented, this signal can be left as no connect. If implemented, it should be routed with a 150 Ω to 240 Ω pull-up resistor placed within 1ns of the ITP connector., it should be routed with a 150 Ω to 240 Ω pull-up resistor placed within 1ns of the ITP connector.

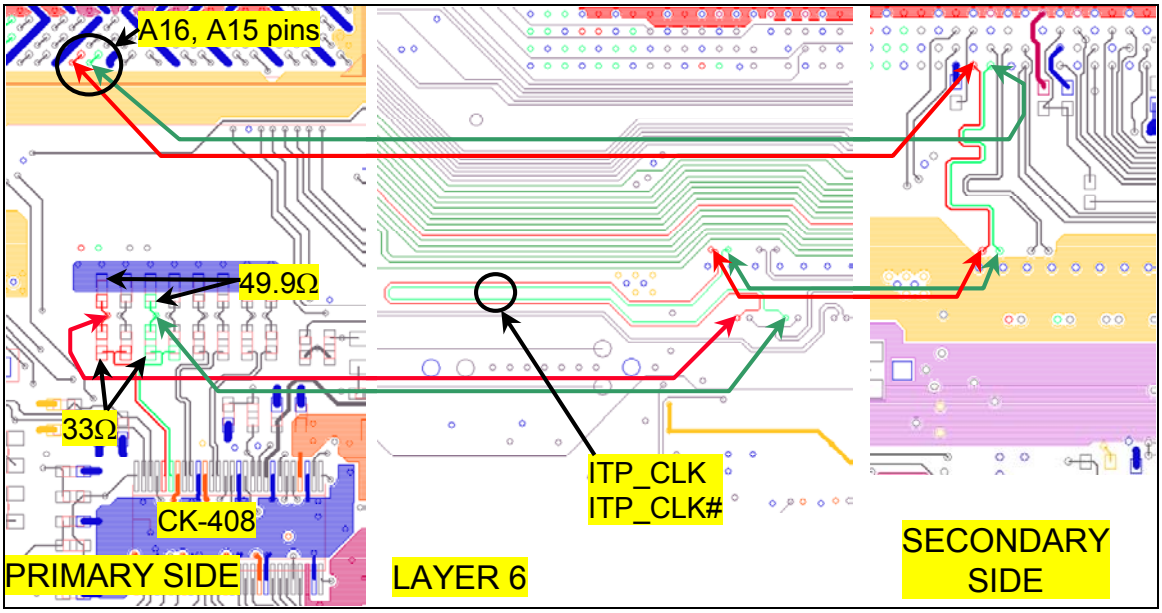
4.3.2.1. ITP_CLK Routing to ITP Interposer

A layout example for ITP_CLK/ITP_CLK# routing to the CPU socket for supporting an ITP interposer is shown in Figure 32. The CK-408 clock chip is mounted on the primary side layer of the motherboard and the differential clock pair also breaks out on the same side. The differential ITP clock pair routing

also requires the use of a pair of 33-Ω ± 5% series resistors placed within 0.5 inches of the clock chip output pins and followed by a pair of 49.9-Ω ± 1% termination resistors to ground. The majority of the ITP_CLK differential serpentine routing takes place on internal Layer 6 below the PSB address signal routing.

Completion of ITP+CLK routing on Layer 6 is not possible due to PSB routing on Layer 6. Therefore the ITP_CLK differential pair then is routed to the secondary side layer to complete routing to the ITP_CLK (pin A16) and ITP_CLK# (pin A15) pins of the processor while matching the BCLK[1:0] routing on the secondary side for a 507-mil length (see Figure 20 and description in Section 4.1.6). Routing to the CPU socket on the primary side layer is not possible because of the presence of the VCCA 1.8V plane flood along the A-signal side row of the pin-map. ITP_CLK routing to the ITP interposer should achieve the ± 250 mil length matching requirement of the BCLK[1:0] lines.

Figure 32. ITP_CLK to CPU ITP Interposer Layout Example



4.3.2.2. ITP Interposer Design Guidelines for Production Systems

For production systems that do not use the ITP interposer, the following guidelines should be followed to ensure that all necessary signals are terminated properly.

Table 18 summarizes all the signals that require termination when a system does not utilize the ITP interposer. This includes TDI, TMS, TRST#, and TCK. TDO can be left as a no connect.

The series 33 Ω and 49.9 Ω ±1% parallel termination resistors on the ITP_CLK/ITP_CLK# differential host clock inputs to the processor socket can also be depopulated for production systems. The only requirement is that the BIOS should disable the third differential host clock pair routed from the CK-408 clock chip to the processor socket.

Finally, the 150 Ω to 240 Ω pull-up resistor for the DBR# output signal from processor socket may or may not be depopulated depending on how it affects the system reset logic that it is connected to. Thus, it is the responsibility of the system designer to determine whether termination for DBR# is required or not for a given system implementation. The same is also true for DBA#, if implemented. This signal is

not required and can be left as no connect. However, it is the responsibility of the system designer to determine whether termination for DBA# is required or not.

4.3.3. Logic Analyzer Interface (LAI)

Intel is working with Agilent Corporation to provide logic analyzer interfaces (LAIs) for use in debugging Intel Pentium M processor / Intel Celeron M processor based systems. LA vendors should be contacted to get specific information about their logic analyzer interfaces. The following information is general and specific information must be obtained from the logic analyzer vendor.

Due to the complexity of a processor based system, the LAI is critical in providing the ability to probe and capture the Processor System Bus signals. There are two sets of considerations to keep in mind when designing a processor based system that can make use of an LAI: mechanical and electrical.

4.3.3.1. Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI pins plug into the socket, while the Intel Pentium M processor / Intel Celeron M processor in the 478-pin package plugs into a socket on the LAI. Cabling this part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keep-out volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include space normally occupied by the processor heat sink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

4.3.3.2. Electrical Considerations

The LAI will also affect the electrical performance of the Intel Pentium M Processor / Intel Celeron M processor FSB. Therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications as load models for the LAI solution they provide.

5. Intel® Mobile Voltage Positioning IV General Description

Please contact your Intel Field Representative for more information on the electrical requirements for the DC-to-DC Voltage Regulator for the Intel Pentium M processor / Intel Celeron M processor.

6. System Memory Design Guidelines (DDR-SDRAM) for SO-DIMM configuration

The Intel 855GM/GME chipset GMCH Double Data Rate (DDR) SDRAM system memory interface consists of SSTL-2 compatible signals. These SSTL-2 compatible signals have been divided into several signal groups: Data, Control, Command, CPC, Clock, and Feedback signals. Table 20 summarizes the different signal grouping. Refer to the *Intel® 855GM/GME (Montara-GM/GM+) Chipset GMCH External Design Specification* for details on the signals listed.

Table 20. GMCH Chipset Memory Signal Groups

Group	Signal Name	Description
Clocks	SCK[5:0]	DDR-SDRAM Differential Clocks - (3 per SO-DIMM)
	SCK#[5:0]	DDR-SDRAM Inverted Differential Clocks - (3 per SO-DIMM)
Data	SDQ[63:0]	Data Bus
	SDQ[71:64]	Check Bits for ECC Function
	SDQS[8:0]	Data Strobes
	SDM[8:0]	Data Mask
Control	SCKE[3:0]	Clock Enable - (One per Device Row)
	SCS#[3:0]	Chip Select - (One per Device Row)
Command	SMA[12:6,3,0]	Memory Address Bus
	SBA[1:0]	Bank Select
	SRAS#	Row Address Select
	SCAS#	Column Address Select
	SWE#	Write Enable
CPC	SMA[5,4,2,1]	Command per Clock (SO-DIMM0)
	SMAB[5,4,2,1]	Command per Clock (SO-DIMM1)
Feedback	RCVENOUT#	Receive Enable Output (no external connection)
	RCVENIN#	Receive Enable Input (no external connection)

6.1. Length Matching and Length Formulas

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching formulas are also provided which further restrict the minimum to maximum length range of each signal group with respect to clock, within the overall boundaries defined in the guideline tables, as required to guarantee adequate timing margins. These secondary constraints are referred to as length matching constraints and the formulas used are referred to as length matching formulas.

All signal groups except the clocks and feedback signals are length matched per slot to the DDR clocks, with the clocks themselves being length tuned to a fixed length across each SO-DIMM slot. The amount of minimum to maximum length variance allowed for each group around the clock reference length varies from signal group to signal group depending on the amount of timing variance which can be tolerated. A simple summary of the length matching formulas for each signal group is provided in the tables below.

Table 21. Intel 855GM Chipset GMCH DDR 200/266 Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock –1.0”	Clock + 0.5”
Command to Clock	Clock – 1.0”	Clock + 2.0”
CPC to Clock	Clock – 1.0”	Clock + 0.5”
Strobe to Clock	Clock – 1.0”	Clock + 0.5”
Data to Strobe	Strobe – 25 mils	Strobe + 25 mils

NOTE: All length matching formulas are based on GMCH die-pad to SO-DIMM connector pin total length.

Table 22. Intel 855GME Chipset GMCH DDR 200/266/333 Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock –2.0”	Clock - 0.5”
Command to Clock	Clock – 2.0”	Clock + 2.0”
CPC to Clock	Clock – 2.0”	Clock - 1.0”
Strobe to Clock	Clock – 2.0”	Clock + 0.5”
Data to Strobe	Strobe – 25 mils	Strobe + 25 mils

NOTE: All length matching formulas are based on GMCH die-pad to SO-DIMM connector pin total length.

Package length tables are provided for all signals in order to facilitate this pad to pin matching. Note that the clock length used for length matching may vary by SO-DIMM slot, based on SO-DIMM spacing. Length formulas should be applied to each SO-DIMM slot independently. An offset of up to 1.0” between clock groups is allowed under the guidelines. The full geometry and routing guidelines along with the exact length matching formulas and associated diagrams are provided in the individual signal group guidelines sections to follow.

6.2. Package Length Compensation

As mentioned in Section 6.1, all length matching is done GMCH die-pad to memory device pin. The reason for this is to compensate for the package length variation across each signal group. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the GMCH requires length matching.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the min and max length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting out package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

6.3. Topologies and Routing Guidelines

The GMCH Double Data Rate (DDR) SDRAM system memory interface implements the low swing, high-speed, terminated SSTL_2 topology. This section contains information related to the recommended interconnect topologies and routing guidelines for each of the signal groups which comprise the DDR interface. When implemented as defined, these guidelines will provide for a robust DDR solution on a GMCH chipset based design.

6.3.1. Clock Signals – SCK[5:0], SCK#[5:0]

The clock signal group includes the differential clock pairs SCK/SCK#[5:0]. The GMCH generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. The GMCH only supports unbuffered DDR SO-DIMMs; three differential clock pairs are routed to each SO-DIMM connector. Table 23 summarizes the clock signal mapping.

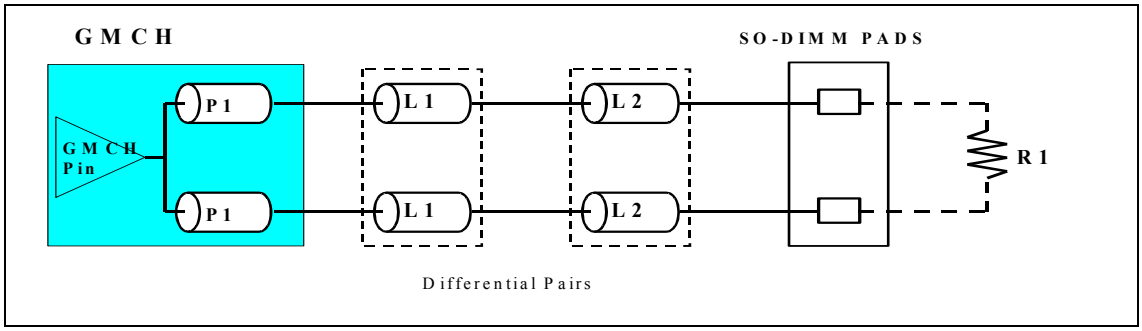
Table 23. Clock Signal Mapping

Signal	Relative To
SCK/SCK#[2:0]	SO-DIMM0
SCK/SCK#[5:3]	SO-DIMM1

6.3.2. Clock Topology Diagram

The GMCH provides 6 differential clock output pairs, or 3 clock pairs per SO-DIMM socket. The motherboard clock routing topology is shown below for reference. Refer to the routing guidelines in table 3 on the follow page for detailed length and spacing rules for each segment. The clock signals should be routed as closely coupled differential pairs over the entire length. Spacing to other DDR signals should not be less than 20 mils. Isolation spacing to non-DDR signals should be 25 mils.

Figure 33. Memory Clock Routing Topology SCK/SCK#[5:0]



6.3.3. Memory Clock Routing Guidelines

Table 24. Clock Signal Group Routing Guidelines

Parameter	Definition
Signal Group	SCK[5:0] and SCK#[5:0]
Topology	Differential Pair Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo) (**see note on trace width** below)	42 Ω +/-15% (for reference only)
Differential Mode Impedance (Zdiff) (**see note on trace width** below)	70 Ω +/- 15% (for reference only)
Nominal Trace Width (**see note on trace width** and exceptions for breakout region below)	Inner Layers: 7 mils Outer Layers: 8 mils (pin escapes only)
Nominal Pair Spacing (edge to edge) (see exceptions for breakout region below)	Inner Layers: 4 mils Outer Layers: 5 mils (pin escapes only)
Minimum Pair to Pair Spacing (see exceptions for breakout region below)	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other DDR Signals (see exceptions for breakout region below)	20 mils
Minimum Isolation Spacing to non-DDR Signals	25 mils
Maximum Via Count	2 (per side)
Package Length Range – P1	1000 mils +/- 350mils (Refer to Table 25 for exact lengths.)
Trace Length Limits – L1	Max = 300 mils (breakout segment)
Total MB Length Limits – L1 + L2	Min = 0.5” Max = 5.0”
Total Length – P1 + L1 + L2	Total length target is determined by placement (see Figure 33) Total length for SO-DIMM0 group = X0 (see Figure 34) Total length for SO-DIMM1 group = X1 (see Figure 34)
SCK to SCK# Length Matching	Match total length to +/- 10 mils (see Section 6.3.3.1)
Clock to Clock Length Matching (Total Length)	Match all SO-DIMM0 clocks to X0 +/- 25 mils (see Figure 34) Match all SO-DIMM1 clocks to X1 +/- 25 mils (see Figure 34)

Parameter	Definition
Breakout Exceptions (Reduced geometries for GMCH breakout region)	Inner Layers: 4 mil trace, 4 mil pair space allowed Outer Layers: 5 mil trace, 5 mil pair space allowed Pair to pair spacing of 5 mils allowed Spacing to other DDR signals of 5 mils allowed Maximum breakout length is 0.3”

NOTES:

1. Pad to Pin length tuning is utilized on clocks in order to achieve minimal variance. Package lengths range between approximately 600 mils and 1400 mils. Exact package lengths for each clock signal are provided at the end of this Section. Overall target length should be established based on placement and routing flow. The resulting motherboard segment lengths must fall within the ranges specified.
2. The DDR clocks should be routed on internal layers, except for pin escapes. It is recommended that pin escape vias be located directly adjacent to the ball pads on all clocks. Surface layer routing should be minimized.
3. Clock differential impedance is controlled indirectly through the single ended impedance specification for the board. Clock signal integrity and edge rates are improved when clock trace widths are widened from the standard 55 Ω single ended trace width. As the table indicates, a trace width of approximately 3 mils wider than standard width was found to be optimal (i.e. inner layers: 4mils std + 3mils = 7mils). The nominal single ended impedance of the widened clock traces is in the range of 42 Ω, and the nominal differential impedance is in the range of 70 Ω. However, impedance control is implemented through geometry control; these values are for reference only.
4. Exceptions to the trace width and spacing geometries are allowed in the breakout region in order to fan-out the interconnect pattern. Reduced spacing should be avoided as much as possible.

6.3.3.1. Clock Length Matching Requirements

The GMCH chipset provides three differential clock pair for each SO-DIMM. A differential clock pair is made up of a SCK signal and its complement signal SCK#. Refer to Section 6.1 for more details on length matching requirements.

The differential pairs for one SO-DIMM are:

SCK[0] / SCK#[0]
SCK[1] / SCK#[1]
SCK[2] / SCK#[2]

The differential pairs for the second SO-DIMM are:

SCK[3] / SCK#[3]
SCK[4] / SCK#[4]
SCK[5] / SCK#[5]

The two sets of differential clocks must be length tuned on the motherboard such that any pair to pair package length variation is tuned out. The three pairs associated with SO-DIMM0 are tuned to a fixed overall length, including package, and the three pairs associated with SO-DIMM1 are tuned to a fixed overall length.

The two traces associated with each clock pair are length matched within the package; however some additional compensation may be required on the motherboard in order to achieve the ± 10 mil length tolerance within the pair.

Between clock pairs the package length varies substantially. Therefore, the motherboard length of each clock pair must be length adjusted to tune out package variance. The total length including package should be matched to within ± 25 mils of each other, as shown in Figure 34. This may result in a clock length variance of as much as 700 mils on the motherboard.

The first step in determining the routing lengths for clocks and all other clock relative signal groups is to establish the target length for each SO-DIMM clock group. These target lengths are shown as X0 and

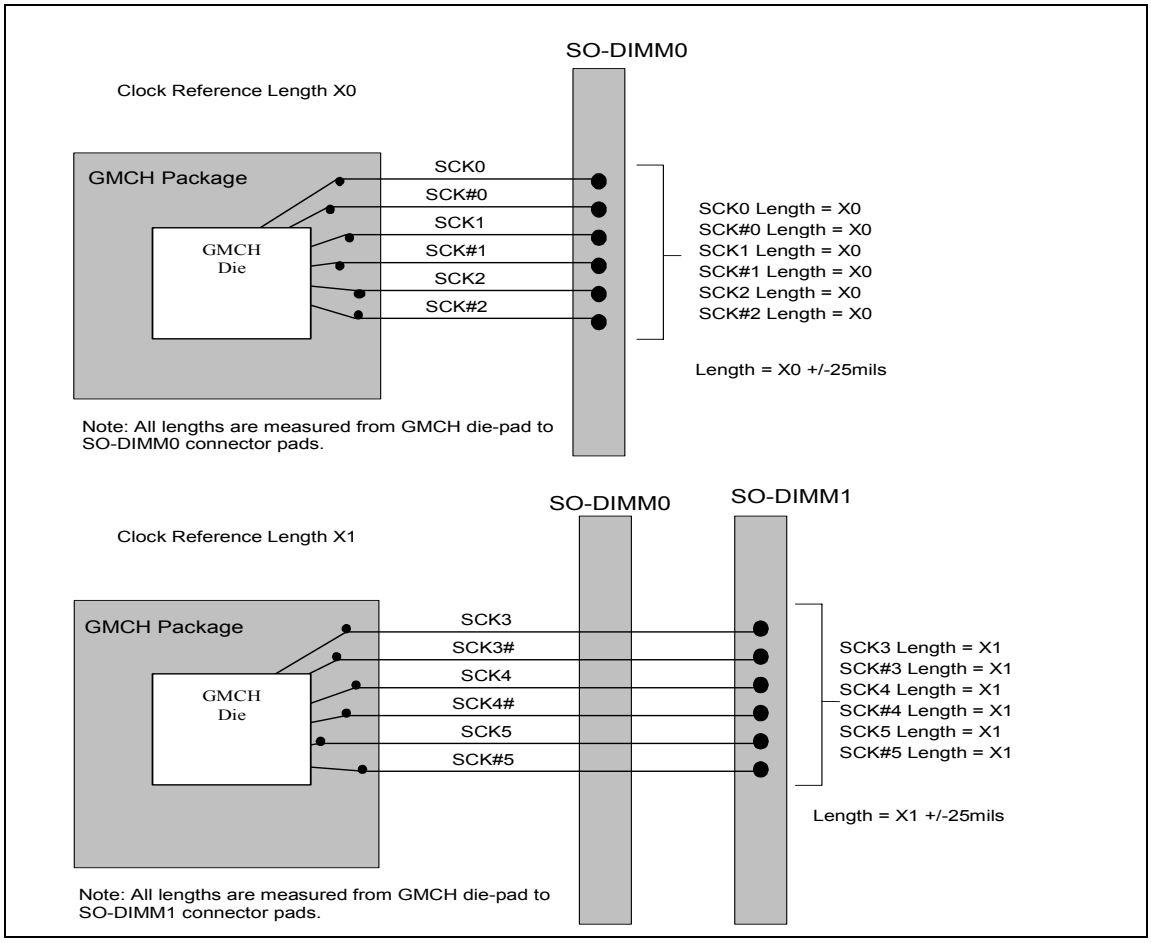
X1, in Figure 34. These are the lengths to which all clocks within the corresponding group will be matched and the reference length values used to calculate the length ranges for the other signal groups.

6.3.3.2. Clock Reference Lengths

The clock reference length for each SO-DIMM clock group is determined by first determining the longest total clock length required to complete the clock routing. A table of clock package lengths is provided in Table 25 to assist in this calculation. Once the longest total length is determined for each clock group, this becomes a lower bound for the associated clock reference length. At this point it is helpful to have completed a test route of the SDQ/SDQS bus such that final clock reference lengths can be defined with consideration of the impact on SDQ/SDQS bus routability. Some iteration may be required.

Once the reference lengths X0 & X1 are defined then the next step is to tune each clock pairs' motherboard trace segment lengths as required such that the overall length of each clock equals the associated clock reference length plus or minus the 25 mil tolerance. Again, the reference length for the two sets of clocks should be offset by the nominal routing length between SO-DIMM connectors.

Figure 34. Memory Clock Trace Length Matching Diagram



6.3.3.3. Clock Package Length Table

The package length data in the table below should be used to tune the motherboard length of each SCK/SCK# clock pair between the GMCH and the associated SO-DIMM socket. It is recommended that die-pad to SO-DIMM pin length be tuned to within ± 25 mils in order to optimize timing margins on the interface.

Table 25. Memory Clock Package Lengths

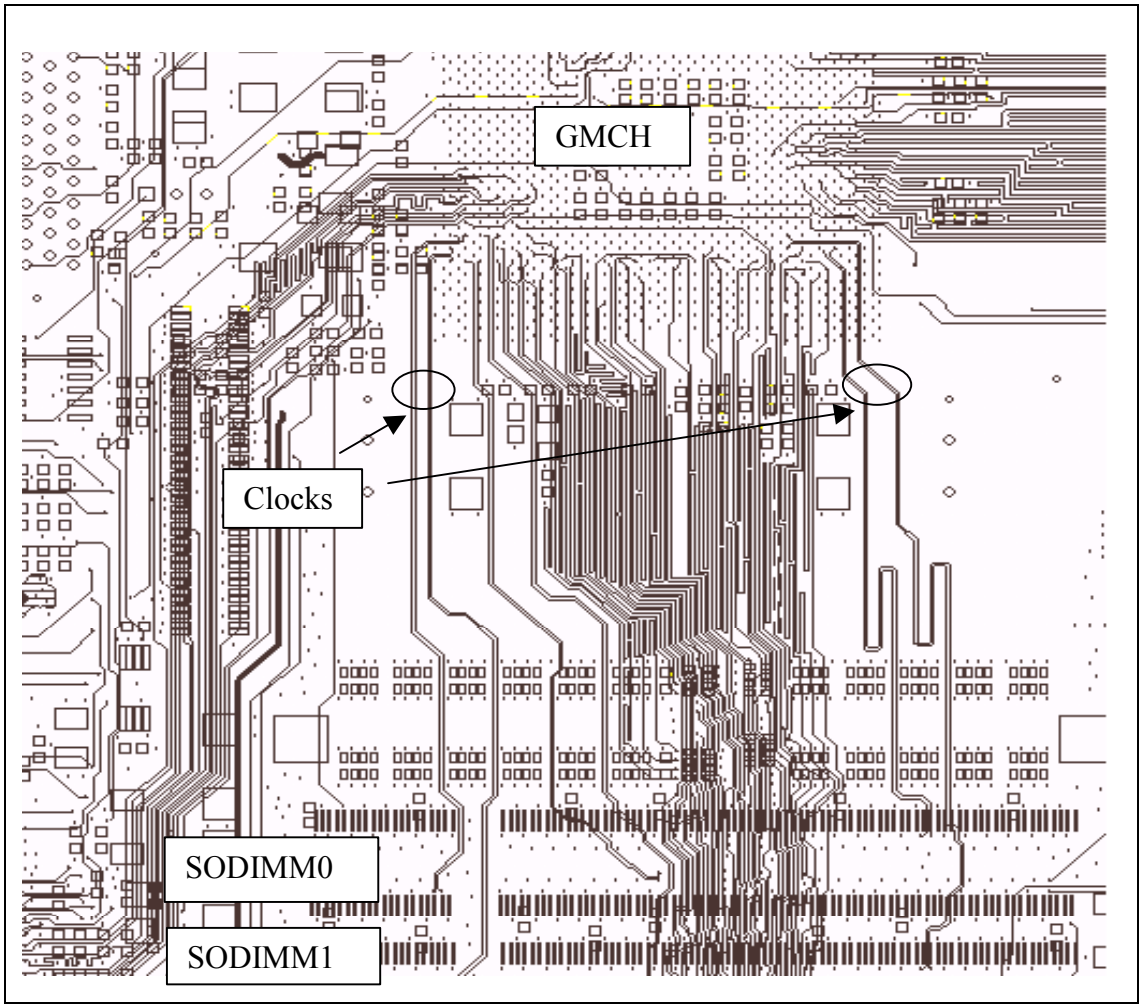
Signal	Pin Number	Package Length (mils)
SCK_0	AB2	1177
SCK#_0	AA2	1169
SCK_1	AC26	840
SCK#_1	AB25	838
SCK_2	AC3	1129
SCK#_2	AD4	1107
SCK_3	AC2	1299
SCK#_3	AD2	1305
SCK_4	AB23	643
SCK#_4	AB24	656
SCK_5	AA3	1128
SCK#_5	AB4	1146

Package length compensation can be performed on each individual clock output thereby matching total length on SCK/SCK# exactly, or alternatively the average package length can be used for both outputs of a pair and length tuning done with respect to the motherboard portion only.

6.3.3.4. Clock Routing Example

Figure 35 is an example of a board routing for the clock signal group.

Figure 35. Clock Signal Routing Example



6.3.4. Data Signals – SDQ[71:0], SDM[8:0], SDQS[8:0]

The GMCH data signals are source synchronous signals that include a 72-bit wide data bus, which includes 8 check bits for Error Checking and Correction (ECC), a set of 9 Data Mask bits, and a set of 9 data strobe signals. There is an associated data strobe and data mask bit for each of the 8-bit data byte groups, making for a total of nine – 10-bit byte lanes. This section summarizes the SDQ/SDM to SDQS routing guidelines and length matching recommendations.

The data signals include SDQ[71:0], SDM[8:0], and SDQS[8:0]. The data signals should transition from an external layer to an internal signal layer under the GMCH. The data signals should keep to the same internal layer until transitioning back to an external layer at the series resistor. After the series resistor, the signal should transition from the external layer to the same internal layer and route to SO-DIMM0. At SO-DIMM0, the signal should transition to an external layer and connect to the appropriate pad of the connector. After the SO-DIMM0 transition, continue to route the signal on the same internal layer to SO-DIMM1, then transition the signal back out to an external layer and connect to the appropriate pad of SO-DIMM1. Connection to the termination resistor should be via the same internal layer with a transition back to the external layer near the resistor. External trace lengths should be minimized.

To facilitate routing, swapping of the byte lanes is allowed for SDQ[63:0] only. Bit swapping within the byte lane is also allowed for SDQ[63:0] only. The check bits, SDQ[71:64], cannot be byte lane swapped with another SDQ byte lane. Also, bit swapping within the SDQ[71:64] byte lane is not allowed. It is suggested that the parallel termination be placed on both sides of SO-DIMM1 to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series (Rs) and parallel (Rt) data and strobe termination resistors, but data and strobe signals can't be placed within the same R pack as the command or control signals. The table and diagrams below depict the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Intel recommends that the full data bus SDQ[71:0], mask bus SDM[8:0], and strobe signals SDQS[8:0] be routed on the same internal signal layer. It is required that the SDQ byte group and the associated SDM and SDQS signals within a byte lane be routed on the same internal layer.

The total length of SDQ, SDM, and SDQS traces between the GMCH and the SO-DIMMs must be within the range defined in the overall guidelines, and is also constrained by a length range boundary based on SCK/SCK# clock length, and a SDQ/SDM to SDQS length matching requirement within each byte lane. Note also that all length matching must be done inclusive of package length. A table of SDQ, SDM, and SDQS package lengths is provided at the end of this Section to facilitate this process.

There are two levels of matching implemented on the data bus signals.

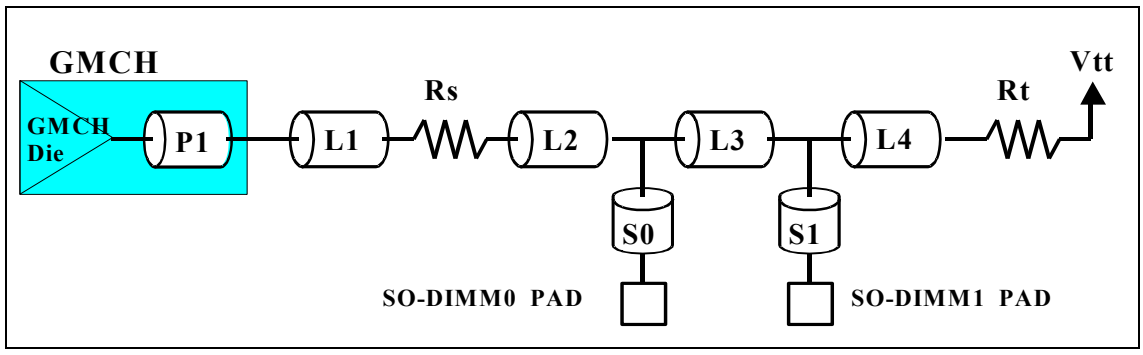
- The first is the length range constraint on the SDQS signals based on clock reference length.
- The second is SDQ/SDM to SDQS length matching within a byte lane.

The length of the SDQS signal for each byte lane must fall within a range determined by the clock reference length, as defined in the SDQS to SCK/SCK length matching Section. The actual length of SDQS for each byte lane may fall anywhere within this range based on placement and routing flow.

Once the SDQS length for a byte lane is established, the SDQ and SDM signals within the byte lane must be length matched to each other, inclusive of package length, as described in the SDQ to SDQS length matching Section 6.3.4.3.

6.3.4.1. Data Bus Topology

Figure 36. Data Signal Routing Topology



The data signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils of spacing to non-DDR related signals. Data signals should be routed on inner layers with minimized external trace lengths.

Table 26. Memory Data Signal Group Routing Guidelines

Parameter	Definition
Signal Group	SDQ[71:0], SDQS[8:0], SDM[8:0]
Motherboard Topology	Daisy Chain with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω +/- 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	SDQ/SDM: 2 to 1 (e.g. 8 mil space to 4 mil trace) SDQS: 3 to 1 (e.g. 12 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	700 mils +/- 300 mils (See Table 28 for details)
Trace Length L1 – GMCH Signal Ball to Series Termination Resistor Pad	Min = 0.5” Max = 3.75”
Trace Length L2 – Series Termination Resistor Pad to First SO-DIMM Via	Max = 0.75”
Stub Length S0, S1 – Stub from Via to SO-DIMM Pad	Max = 0.25”
Total Length L1 + L2 + S0 – Total Length from GMCH to First SO-DIMM Pad	Min = 0.5” Max = 4.0”
Total Length L1 + L2 + L3 + S1 – Total Length from GMCH to Second SO-DIMM Pad	Min = 0.75” Max = 4.5”
Total Length S0 + L3 + S1– Total SO-DIMM pad to SO-DIMM pad spacing	Min = 0.25” Max = 1.0”
Trace Length L4 – Last SO-DIMM Via to Parallel Termination Resistor Pad	Max = 1.0”
Series Termination Resistor (Rs)	10 Ω ± 5%
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Length Matching Requirements	SDQS to SCK/SCK# See length matching Section 6.3.4.2 SDQ/SDM to SDQS, to +/- 25mils, within each byte lane

NOTES:
1. Power distribution vias from Rt to Vtt are not included in this count.
2. The overall minimum and maximum length to the SO-DIMM must comply with clock length matching requirements.
3. It is possible to route using 4 vias if trace segments L2 and L4 are routed on the same external layer as the associated SO-DIMM, for example if L2 is on the same layer as SO-DIMM0.

6.3.4.2. SDQS to Clock Length Matching Requirements

The first step in length matching is to determine the SDQS length range based on the SCK/SCK# reference length defined previously. The total length of the SDQS strobe signals, including package length, between the GMCH die-pad and the SO-DIMMs must fall within the range defined in the formulas below. See the clock Section for the definition of the clock reference length. Refer to Figure

36 for the definition of the various trace segments. The length tuning requirements are also depicted in Figure 37. Refer to Section 6.1 for more details on length matching and length formula requirements.

Length range formula for SO-DIMM0:

X_0 = SCK/SCK#[2:0] total reference length, including package length

Y_0 = SDQS[8:0] total length = GMCH package + L1 + L2 + S0, as shown in Figure 37,

where: $(X_0 – 1.0”) \le Y_0 \le (X_0 + 0.5”)$ for DDR 200/266

$(X_0 – 2.0”) \le Y_0 \le (X_0 + 0.5”)$ for DDR 200/266/333

Length range formula for SO-DIMM1,

X_1 = SCK/SCK#[5:3] total reference length, including package length

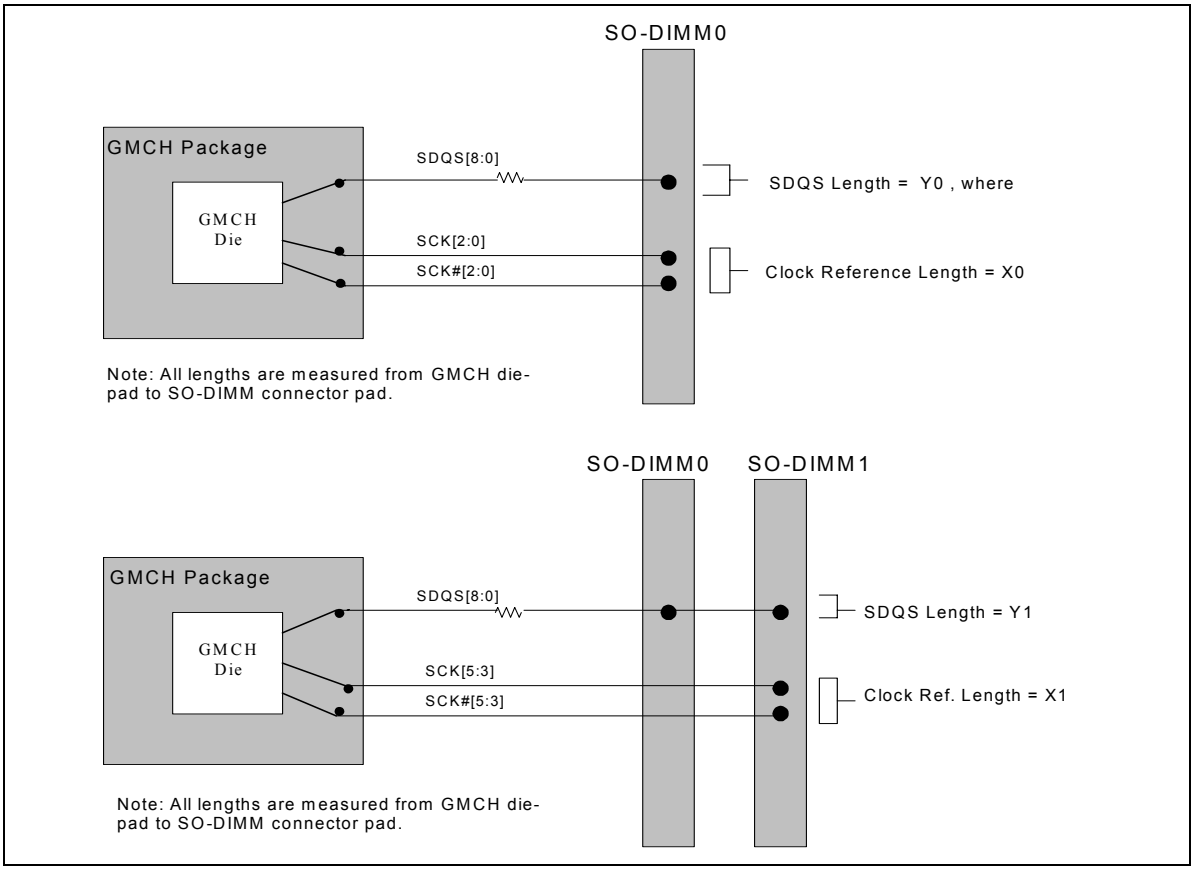
Y_1 = SDQS[8:0] total length = GMCH package + L1 + L2 + L3 + S1, as shown Figure 37,

where: $(X_1 – 1.0”) \le Y_1 \le (X_1 + 0.5”)$ for DDR 200/266

$(X_0 – 2.0”) \le Y_0 \le (X_0 + 0.5”)$ for DDR 200/266/333

Length matching is only performed from the GMCH to the SO-DIMMs, and does not involve the length of L4, which can vary over its entire range. Intel recommends that routing segment length L3 between SO-DIMM0 to SO-DIMM1 be held fairly constant and equal to the offset between clock reference lengths X0 and X1. This will produce the most straightforward length-matching scenario. Note that a nominal SDQS package length of 750 mils can be used to estimate MB lengths prior to performing package length compensation. Refer to Section 6.2 for more details on package length compensation.

Figure 37. SDQS to Clock Trace Length Matching Diagram



6.3.4.3. Data to Strobe Length Matching Requirements

The data bit signals, SDQ[71:0] are grouped by byte lanes and associated with a data mask signal SDM[8:0], and a data strobe, SDQS[8:0].

- The data and mask signals must be length matched to their associated strobe within ± 25 mils, including package.
- For SO-DIMM0 this length matching includes the motherboard trace length to the pads of the SO-DIMM0 connector (L1 + L2 + S0) plus package length.
- For SO-DIMM1, the motherboard trace length to the pads of the SO-DIMM1 connector (L1 + L2 + L3 + S1) plus package length.

Refer to Section 6.2 for more details on package length compensation.

Length range formula for SDQ and SDM,

X = SDQS total length, including package length, as defined previously

Y = SDQ, SDM total length, including package length, within same byte lane as show in Figure 38,

where: (X – 25 mils) ≤ Y ≤ (X + 25 mils)

Length matching is not required from the SO-DIMM1 to the parallel termination resistors. Figure 38 on the following page depicts the length matching requirements between the SDQ, SDM, and SDQS signals within a byte lane. Byte lane mapping is defined in Table 27 below.

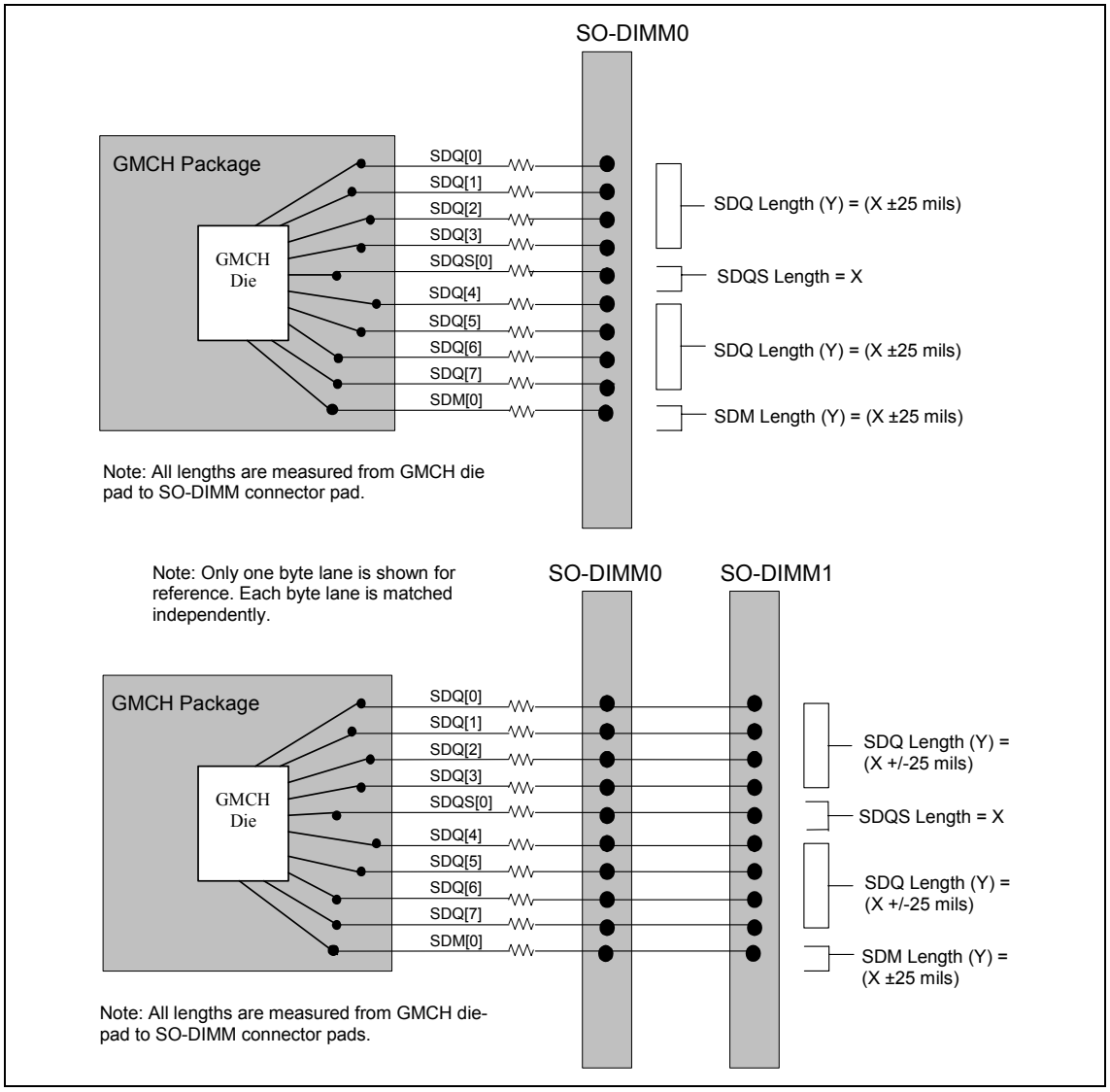
6.3.4.4. SDQ to SDQS Mapping

Table 27 below defines the mapping between the nine byte lanes, nine mask bits, and the nine SDQS signals, as required to do the required length matching.

Table 27. SDQ/SDM to SDQS Mapping

Signal	Mask	Relative To
SDQ[7:0]	SDM[0]	SDQS[0]
SDQ[15:8]	SDM[1]	SDQS[1]
SDQ[23:16]	SDM[2]	SDQS[2]
SDQ[31:24]	SDM[3]	SDQS[3]
SDQ[39:32]	SDM[4]	SDQS[4]
SDQ[56:40]	SDM[5]	SDQS[5]
SDQ[55:48]	SDM[6]	SDQS[6]
SDQ[63:56]	SDM[7]	SDQS[7]
SDQ[71:64]	SDM[8]	SDQS[8]

Figure 38. SDQ/SDM to SDQS Trace Length Matching Diagram



6.3.4.5. SDQ/SDQS Signal Package Lengths

The package length data in Table 28 below should be used to tune the length of each SDQ, SDM, and SDQS motherboard trace as required to achieve the overall length matching requirements defined in the prior Sections.

Table 28. Memory SDQ/SDM/SDQS Package Lengths

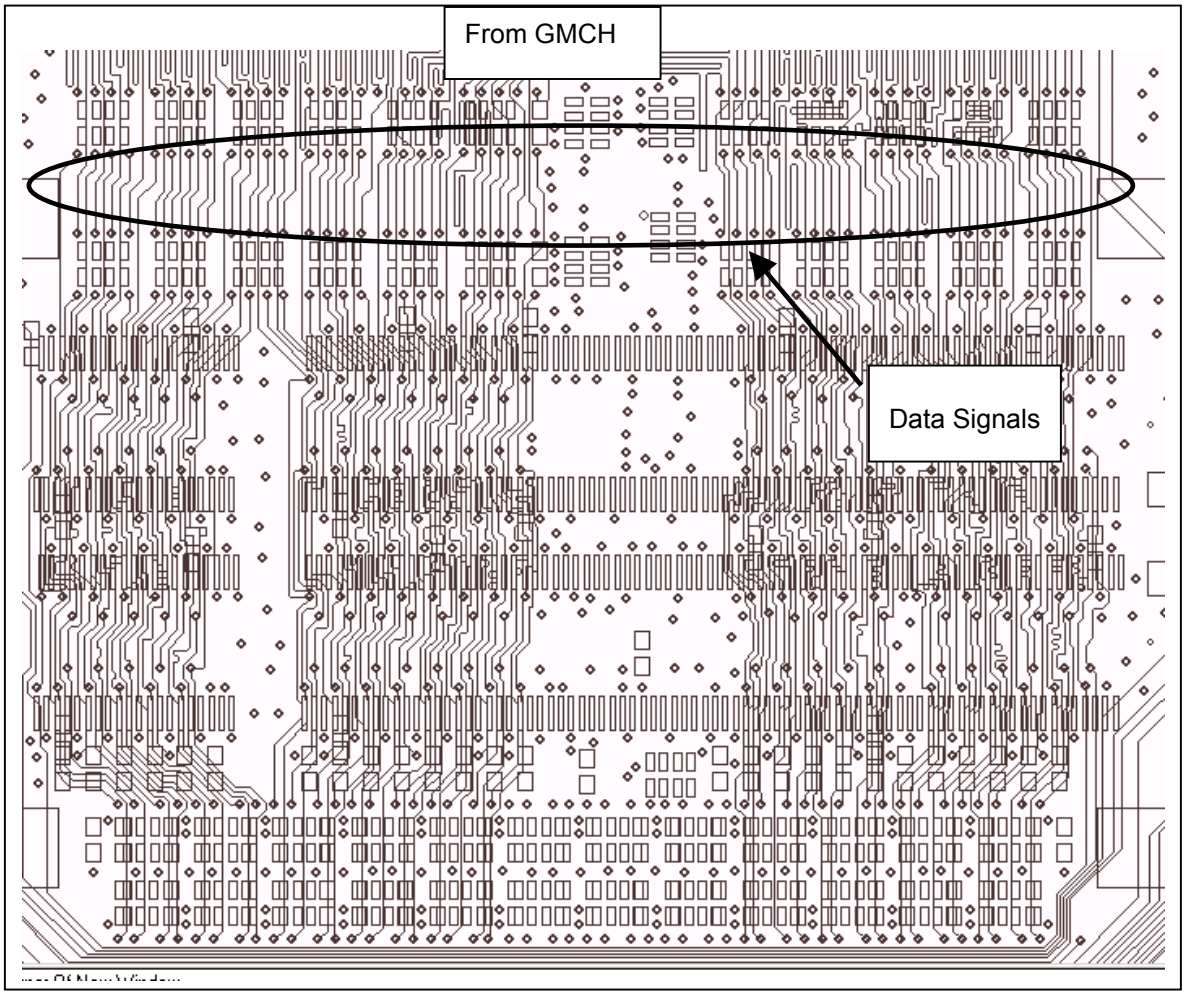
Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
SDQ_00	AF2	785	SDQ_24	AH10	648	SDQ_48	AE23	592

Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
SDQ_01	AE3	751	SDQ_25	AH11	622	SDQ_49	AH23	752
SDQ_02	AF4	690	SDQ_26	AG13	572	SDQ_50	AE24	666
SDQ_03	AH2	903	SDQ_27	AF14	655	SDQ_51	AH25	817
SDQ_04	AD3	682	SDQ_28	AG11	599	SDQ_52	AG23	639
SDQ_05	AE2	739	SDQ_29	AD12	460	SDQ_53	AF23	667
SDQ_06	AG4	741	SDQ_30	AF13	536	SDQ_54	AF25	707
SDQ_07	AH3	845	SDQ_31	AH13	642	SDQ_55	AG25	783
SDQ_08	AD6	607	SDQ_32	AH16	766	SDQ_56	AH26	834
SDQ_09	AG5	756	SDQ_33	AG17	558	SDQ_57	AE26	701
SDQ_10	AG7	685	SDQ_34	AF19	510	SDQ_58	AG28	808
SDQ_11	AE8	558	SDQ_35	AE20	579	SDQ_59	AF28	756
SDQ_12	AF5	734	SDQ_36	AD18	408	SDQ_60	AG26	782
SDQ_13	AH4	825	SDQ_37	AE18	458	SDQ_61	AF26	748
SDQ_14	AF7	644	SDQ_38	AH18	658	SDQ_62	AE27	673
SDQ_15	AH6	912	SDQ_39	AG19	596	SDQ_63	AD27	608
SDQ_16	AF8	622	SDQ_40	AH20	677	SDQ_64	AG14	566
SDQ_17	AG8	624	SDQ_41	AG20	730	SDQ_65	AE14	477
SDQ_18	AH9	676	SDQ_42	AF22	562	SDQ_66	AE17	571
SDQ_19	AG10	634	SDQ_43	AH22	702	SDQ_67	AG16	530
SDQ_20	AH7	710	SDQ_44	AF20	563	SDQ_68	AH14	701
SDQ_21	AD9	508	SDQ_45	AH19	644	SDQ_69	AE15	421
SDQ_22	AF10	569	SDQ_46	AH21	716	SDQ_70	AF16	491
SDQ_23	AE11	469	SDQ_47	AG22	783	SDQ_71	AF17	530
SDM_0	AE5	838	SDQS_0	AG2	925			
SDM_1	AE6	693	SDQS_1	AH5	838			
SDM_2	AE9	538	SDQS_2	AH8	756			
SDM_3	AH12	606	SDQS_3	AE12	466			
SDM_4	AD19	492	SDQS_4	AH17	678			
SDM_5	AD21	470	SDQS_5	AE21	487			
SDM_6	AD24	557	SDQS_6	AH24	770			
SDM_7	AH28	917	SDQS_7	AH27	858			
SDM_8	AH15	685	SDQS_8	AD15	418			

6.3.4.6. Memory Data Routing Example

Figure 39 is an example of a board routing for the Data signal group. The majority of the Data signal route is on an internal layer, both external layers can be used for parallel termination R-pack placement.

Figure 39. Data Signals Group Routing Example



6.3.5. Control Signals – SCKE[3:0], SCS#[3:0]

The GMCH control signals, SCKE[3:0] and SCS#[3:0], are clocked into the DDR SDRAM devices using clock signals SCK/SCK#[5:0]. The GMCH drives the control and clock signals together, with the clocks crossing in the valid control window. The GMCH provides one chip select (CS) and one clock enable (CKE) signal per SO-DIMM physical device row. Two chip select and two clock enable signals will be routed to each SO-DIMM. Refer to Table 29 for the CKE and CS# signal to SO-DIMM mapping.

Table 29. Control Signal to SO-DIMM Mapping

Signal	Relative To	SO-DIMM Pin
SCS#[0]	SO-DIMM0	AD23
SCS#[1]	SO-DIMM0	AD26
SCS#[2]	SO-DIMM1	AC22
SCS#[3]	SO-DIMM1	AC25
SCKE[0]	SO-DIMM0	AC7
SCKE[1]	SO-DIMM0	AB7
SCKE[2]	SO-DIMM1	AC9
SCKE[3]	SO-DIMM1	AC10

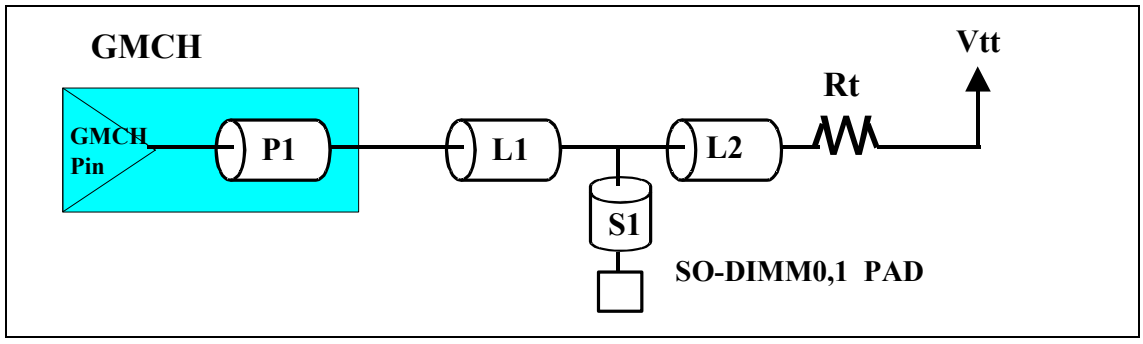
The control signal routing should transition from an external layer to an internal signal layer under the GMCH, keep to the same internal layer until transitioning back out to an external layer to connect to the appropriate pad of the SO-DIMM connector and the parallel termination resistor. If the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.

External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground reference to keep the path of return current continuous. Intel suggests that all control signals be routed on the same internal layer.

Resistor packs are acceptable for the parallel (Rt) control termination resistors, but control signals can't be placed within the same R pack as the data or command signals. Figure 40 and Table 30 below depicts the recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

6.3.5.1. Control Signal Topology

Figure 40. Control Signal Routing Topology



The control signals should be routed using 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20-mils of spacing to non-DDR related signals. Control signals should be routed on inner layers with minimized external trace lengths.

6.3.5.2. Control Signal Routing Guidelines

Table 30. Control Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SCKE[3:0], SCS#[3:0]
Motherboard Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ±15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils +/- 250 mils (Refer to Table 31 for details)
Stub Length S1 – Stub from Via to SO-DIMM Pad	Max = 0.25”
Trace Length L1+S1 – Total length from GMCH Signal Ball to SO-DIMM Pad	Min = 0.5 inches Max = 5.5 inches for DDR 266 Max = 4.5 inches for DDR 333
Trace Length L2 – SO-DIMM via to Parallel Termination Resistor Pad	Max = 2.0 inches
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	3
Length Matching Requirements	CTRL to SCK/SCK# [5:0] See length matching Section 6.3.5.3 and Figure 41.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. It is possible to route using 2 vias if one via is shared that connects to the SO-DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.

6.3.5.3. Control to Clock Length Matching Requirements

The length of the control signals, between the GMCH die pad and the SO-DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 40 for a definition of the various trace segments that make up this path. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 41. Refer to Section 6.1 for more details on length matching requirements.

Length range formula for SO-DIMM0:

X_0 = SCK/SCK#[2:0] total reference length, including package length.

Y_0 = SCS#[1:0] & SCKE[1:0] total length = GMCH package length + L1 + S1, as shown in Figure 41

where: $(X_0 – 1.0”) \le Y_0 \le (X_0 + 0.5”)$ for DDR 200/266

$(X_0 – 2.0”) \le Y_0 \le (X_0 - 0.5”)$ for DDR 200/266/333

Length range formula for SO-DIMM1:

X_1 = SCK/SCK#[5:3] total reference length, including package length.

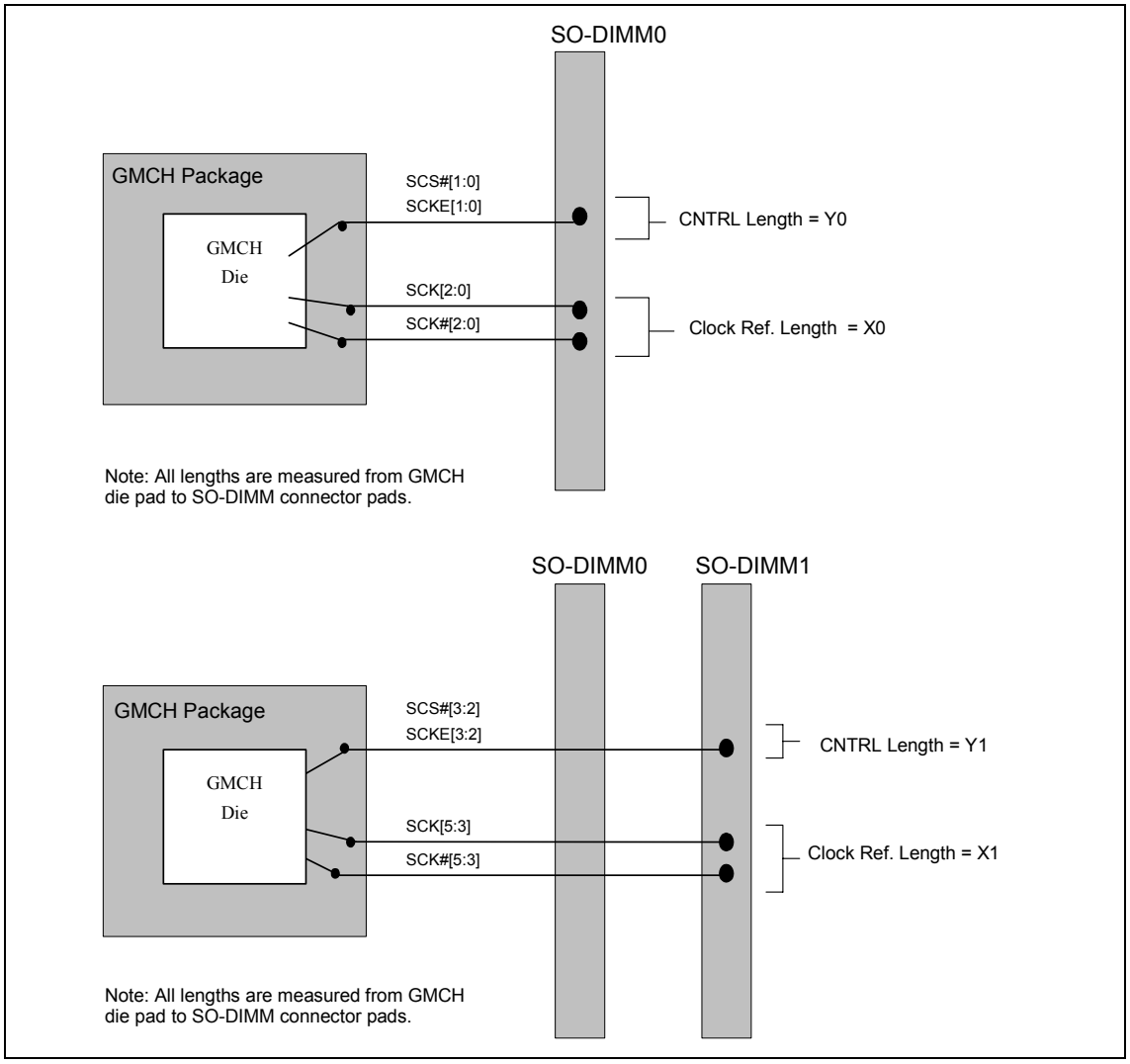
Y_1 = SCS#[3:2] & SCKE[3:2] total length = GMCH package length + L1 + S1, as shown in Figure 41,

where: $(X_1 – 1.0”) \le Y_1 \le (X_1 + 0.5”)$ for DDR 200/266

$(X_1 – 2.0”) \le Y_1 \le (X_1 - 0.5”)$ for DDR 200/266/333

No length matching is required from the SO-DIMM to the termination resistor. Figure 41 on the following page depicts the length matching requirements between the control signals and clock. A nominal CS/CKE package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 6.2 for more details on package length compensation.

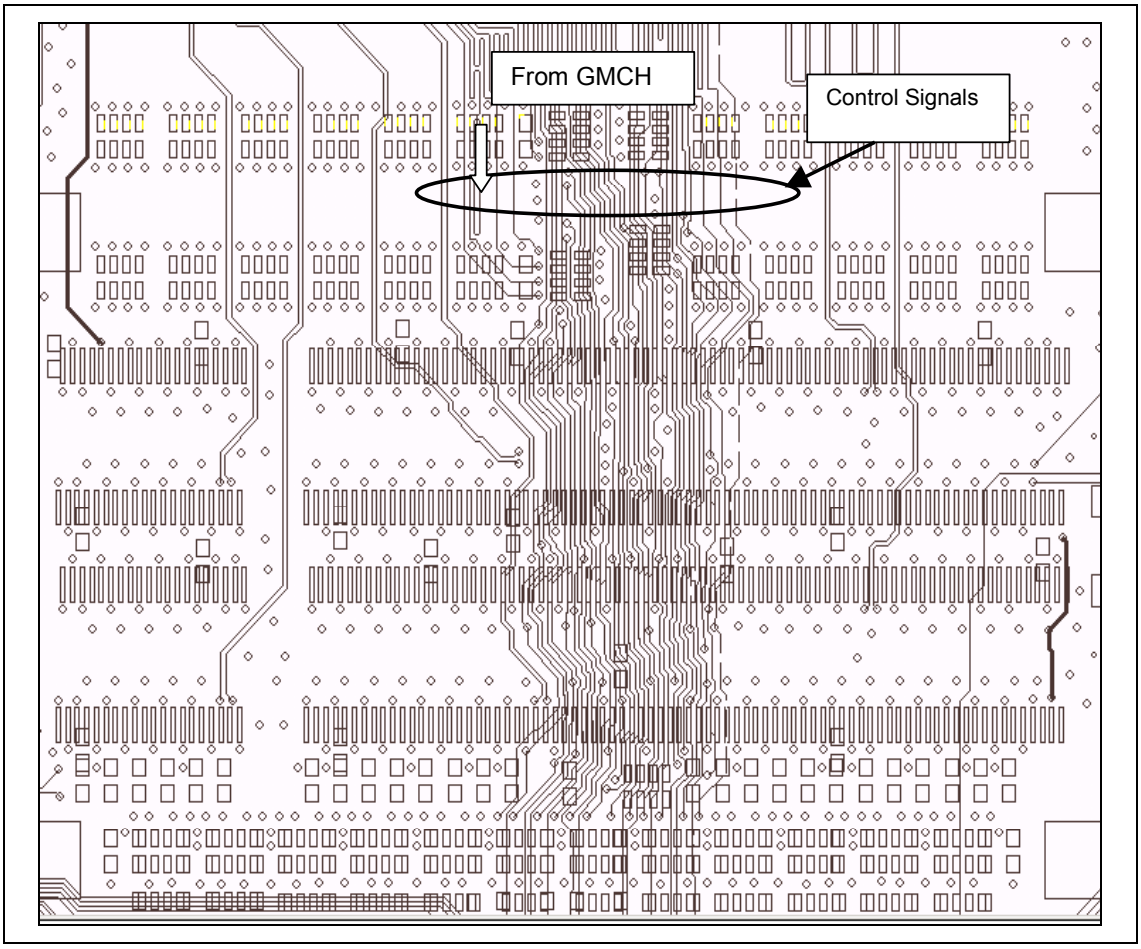
Figure 41. Control Signal to Clock Trace Length Matching Diagram



6.3.5.4. Memory Control Routing Example

Figure 42 is an example of a board routing for the Control signal group.

Figure 42. Control Signals Group Routing Example



6.3.5.5. Control Group Package Length Table

The package length data in Table 31 below should be used to match the overall length of each command signal to it's associated clock reference length. Note that due to the relatively small variance in package length and adequate timing margins it is acceptable to use a fixed 500-mil nominal package length for all control signals, thereby reducing the complexity of the motherboard length calculations.

Table 31. Control Group Package Lengths

Signal	Pin Number	Package Length (mils)		Signal	Pin Number	Package Length (mils)
SCS#[0]	AD23	502		SCKE[0]	AC7	443
SCS#[1]	AD26	659		SCKE[1]	AB7	389
SCS#[2]	AC22	544		SCKE[2]	AC9	386
SCS#[3]	AC25	612		SCKE[3]	AC10	376

6.3.6. Command Signals – SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#

The GMCH chipset command signals, SMA[12:0], SBA[1:0], SRAS#, SCAS#, and SWE# clocked into the DDR SDRAMs using the clock signals SCK/SCK#[5:0]. The GMCH drives the command and clock signals together, with the clocks crossing in the valid command window. There are three supported topologies for the command signal group. Topology 1 is a daisy chain topology. Topology 2 implements a T routing topology. Both topologies allow series resistors to be placed between the two SO-DIMMs to dampen the SO-DIMM to SO-DIMM resonance. Topology 2 is the topology that best allows for placement of the SO-DIMMs back to back in the butterfly configuration, thus minimizing the SO-DIMM footprint area. Topology 3 allows the series resistors to be physically placed after the farthest SO-DIMM, when there is no room between the two connectors. Note that series resistors are essential in all of the three topologies.

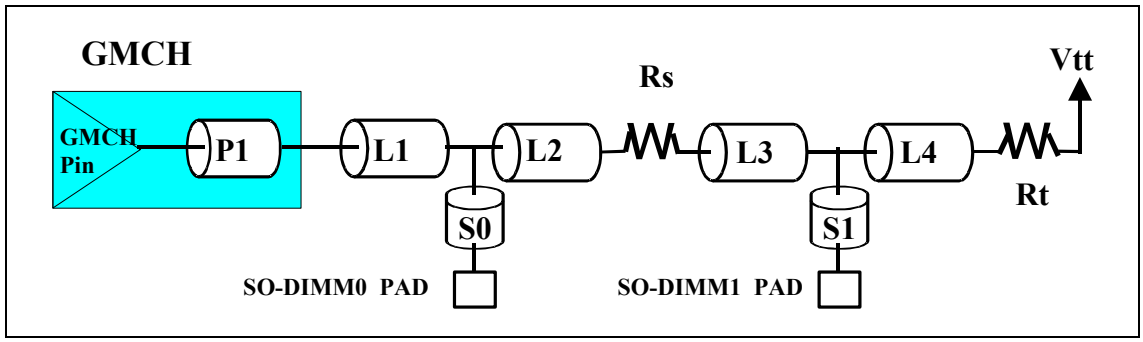
6.3.6.1. Command Topology 1

The command signal routing should transition from an external layer to an internal signal layer under the GMCH. Keep to the same internal layer until transitioning back to an external layer immediately prior to connecting the SO-DIMM0 connector pad. At the via transition for SO-DIMM0, continue the signal route on the same internal layer to the series termination resistor (Rs), collocated to SO-DIMM1. At this resistor the signal should transition to an external layer immediately prior to the pad of Rs. After the series resistor, Rs, continue the signal route on the external layer landing on the appropriate connector pad of SO-DIMM1. After SO-DIMM1, transition to the same internal layer or stay on the external layer and route the signal to Rt.

Intel suggests that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors but command signals can't be placed within the same R-packs as data, strobe, or control signals. Figure 43 and Table 32 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1.

Figure 43. Command Routing for Topology 1



The command signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils spacing to non-DDR related signals. Command signals should be routed on inner layers with minimized external traces.

6.3.6.2. Command Topology 1 Routing Guidelines

Table 32. Command Topology 1 Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#
Motherboard Topology	Daisy Chain with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils +/- 250 mils (See Table 35 for exact package lengths.)
Stub Lengths S0, S1	Max = 0.25”
Trace Length L1 + S0 – GMCH Command Signal Ball to First SO-DIMM Pad	Min = 0.5 inch Max = 4.0 inches
Total Length L1 + L2 + L3 + S1 – Total Length from GMCH Ball to Second SO-DIMM Pad	Min = 1.0” Max = 7.0”
Total Length S0 + L2 + L3 + S1– Total SO-DIMM pad to SO-DIMM pad spacing	Max = 3.0”
Trace Length L4 – Second SO-DIMM Via to Parallel Resistor Pad	Max = 1.5 inches
Series Termination Resistor (Rs)	10 Ω ± 5%
Parallel Termination Resistor (Rt)	56 Ω ± 5%

Maximum Recommended Motherboard Via Count Per Signal	6
Length Matching Requirements	CMD to SCK/SCK# [5:0] See length matching Section 6.3.6.3 and Figure 44 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using 4 vias if one via is shared that connects to the SO-DIMM1 pad and parallel termination resistor.

6.3.6.3. Command Topology 1 Length Matching Requirements

The routing length of the command signals, between the GMCH die pad and the SO-DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to Figure 43 for a definition of the various motherboard trace segments. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 44. Refer to Section 6.1 for more details on length matching requirements.

Length range formula for SO-DIMM0:

X0 = SCK/SCK#[2:0] total reference length, including package length.

Y0 = CMD signal total length = GMCH package + L1 + S0, as shown in Figure 44,

where: $(X_0 - 1.0") \le Y_0 \le (X_0 + 2.0")$ for DDR 200/266

$(X_0 - 2.0") \le Y_0 \le (X_0 + 2.0")$ for DDR 200/266/333

Length range formula for SO-DIMM1:

X1 = SCK/SCK#[5:3] total reference length, including package length.

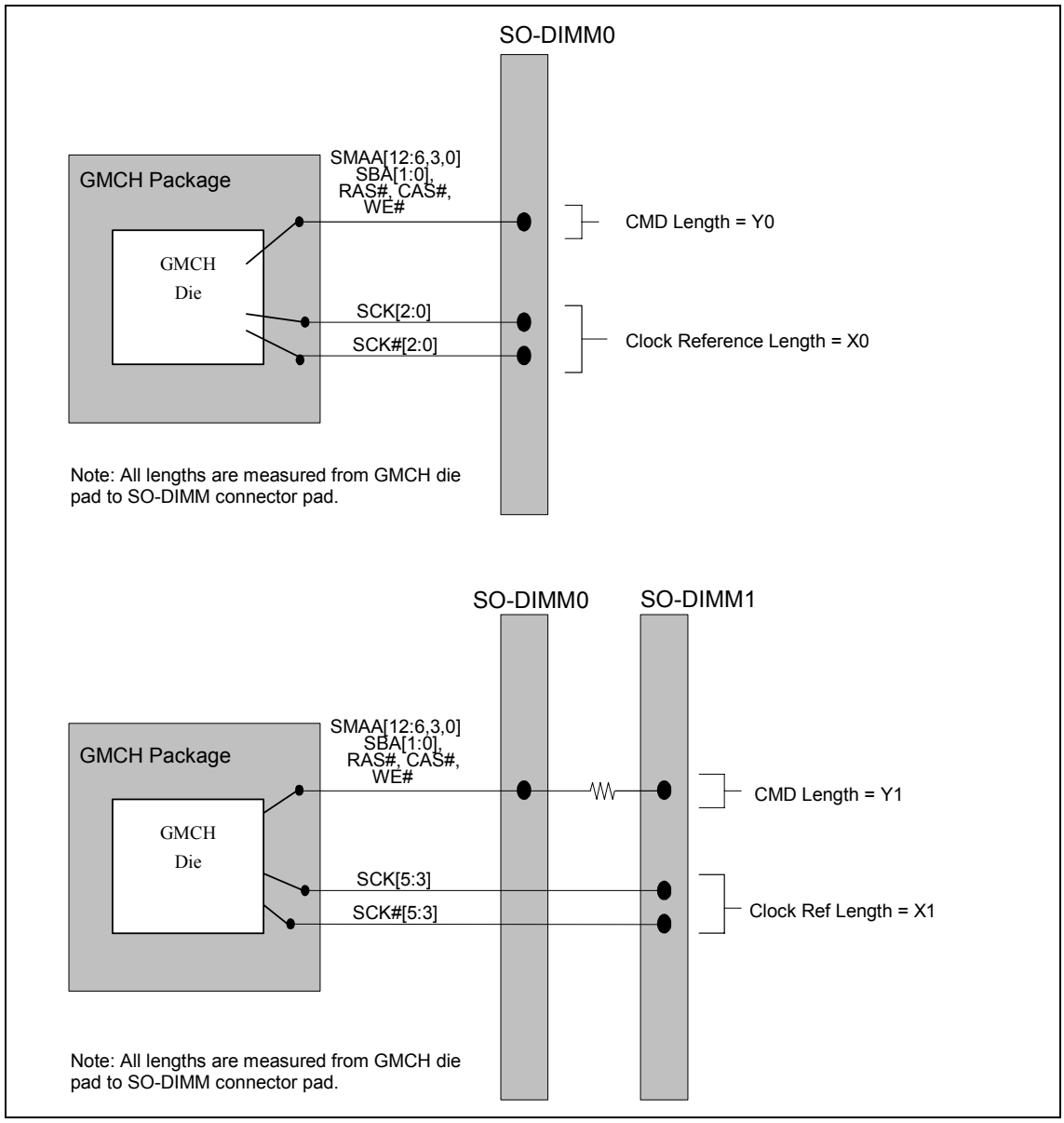
Y1 = CMD signal total length = GMCH package + L1 + L2 + L3 + S1, as shown in Figure 44,

where: $(X_1 - 1.0") \le Y_1 \le (X_1 + 2.0")$ for DDR 200/266

$(X_1 - 2.0") \le Y_1 \le (X_1 + 2.0")$ for DDR 200/266/333

No length matching is required from SO-DIMM1 to the termination resistor. Figure 44 on the following page depicts the length matching requirements between the command signals and clock. A nominal CMD package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 6.2 for more details on package length compensation.

Figure 44. Topology 1 Command Signal to Clock Trace Length Matching Diagram



6.3.6.4. Command Topology 2

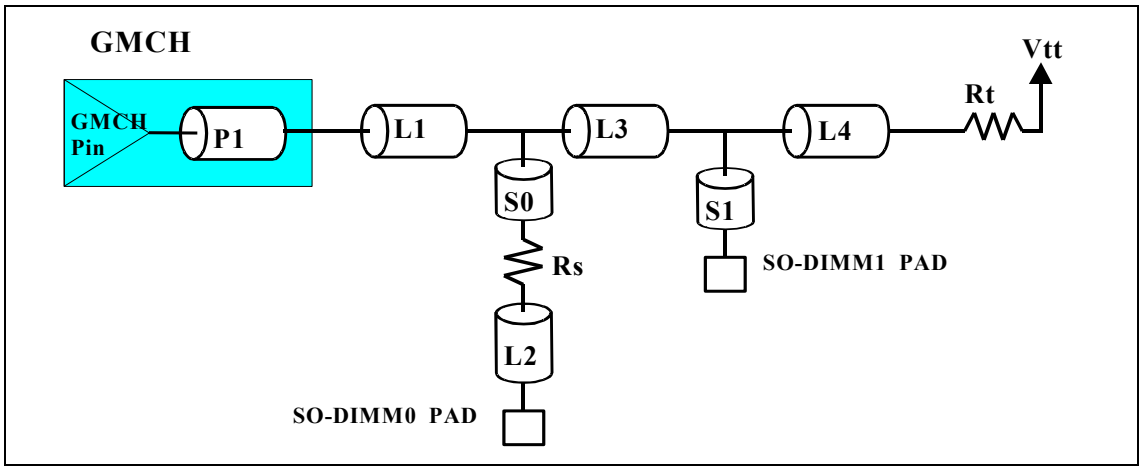
The command signal routing should transition from an external layer to an internal signal layer under the GMCH. Keep to the same internal layer until transitioning back to an external layer at the series resistor Rs. At this point there is a T in the topology. One leg of the T will route through Rs and either transition back to the same internal layer or stay external and landing on the appropriate connector pad of SO-DIMM0. If it was necessary to return to the internal layer the signal should return to the external layer immediately prior to landing on the appropriate connector pad of SO-DIMM0. The other leg of the T will continue on the same internal layer and return to the external layer immediately prior to landing on the appropriate connector pad of SO-DIMM1. If possible stay on the external layer and connect to the parallel termination resistor or if the parallel termination resistor is on the opposite side of the board from the SO-DIMM1 connector then share the via and route to the parallel termination resistor. If sharing the via or using the opposite side of the board is not possible, continue on the same internal layer and route to the external layer immediately prior to the termination resistor.

External trace lengths should be minimized. It is suggested that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous. It is recommended that command signal group be routed on same internal layer.

It is suggested that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors but command signals can't be placed within the same R-packs as data, strobe or control signals. Figure 45 and Table 33 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1.

Figure 45. Command Routing Topology 2



The command signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils of spacing to non-DDR related signals. Command signals should be routed on inner layers with minimized external trace lengths.

6.3.6.5. Command Topology 2 Routing Guidelines

Table 33. Command Topology 2 Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#
Motherboard Topology	Branched T with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils +/- 250 mils (See Table 35 for exact package length.)
Stub Length S0, S1	Max = 0.25”
Trace Length L2 – Series Resistor Pad to First SO-DIMM Pad	Max = 1.0 inches
Total Length L1+ S0 + L2 – Total length from GMCH ball to First SO-DIMM pad	Min = 0.5” Max = 5.0”
Total Length L1+ L3 + S1 – Total length from GMCH ball to Second SO-DIMM pad	Min = 1.0” Max = 7.0”
Total Length S0 + L2 + L3 + S1– Total SO-DIMM pad to SO-DIMM pad spacing	Max = 3.0”
Trace Length L4 – Second SO-DIMM Via to Parallel Resistor Pad	Max = 1.5”
Series Termination Resistor (Rs)	10 Ω ± 5%
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	6
Length Matching Requirements	CMD to SCK/SCK# [5:0] See length matching Section 6.3.6.6 and Figure 46 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using 3 vias if one via is shared that connects to the SO-DIMM0 pad and series termination resistor, if a via is shared that connects L1 to series termination and if one via is shared that connects to the SO-DIMM1 pad and parallel termination resistor.

6.3.6.6. Command Topology 2 Length Matching Requirements

The routed length of the command signals, between the GMCH package ball and the SO-DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to Figure 45 for a definition of the various motherboard trace segments. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 46. Refer to Section 6.1 for more details on length matching requirements.

Length range formula for SO-DIMM0

$\mathbf{X_0}$ = SCK/SCK#[2:0] total reference length, including package length.

$\mathbf{Y_0}$ = CMD signal total length = GMCH package + L1 + L2 + S0, as shown in Figure 46,

where: $(X_0 - 1.0") \le Y_0 \le (X_0 + 2.0")$ for DDR 200/266

$(X_0 - 2.0") \le Y_0 \le (X_0 + 2.0")$ for DDR 200/266/333

Length range formula for SO-DIMM1

$\mathbf{X_2}$ = SCK/SCK#[5:3] total reference length, including package length.

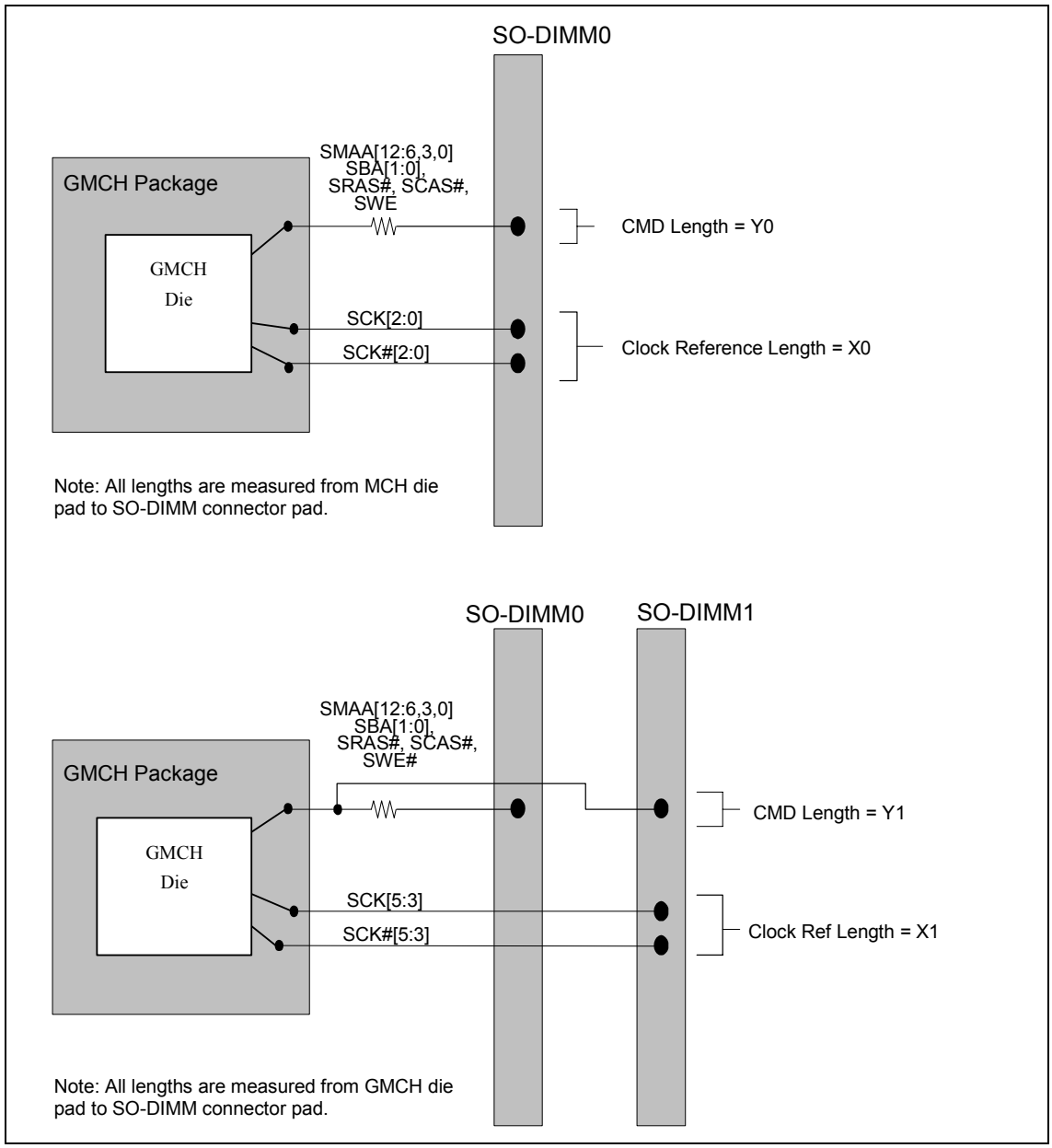
$\mathbf{Y_2}$ = CMD signal total length = GMCH package length + L1 + L3 + S1, as shown in Figure 46,

where: $(X_1 - 1.0") \le Y_1 \le (X_1 + 2.0")$ for DDR 200/266

$(X_1 - 2.0") \le Y_1 \le (X_1 + 2.0")$ for DDR 200/266/333

No length matching is required from SO-DIMM1 to the termination resistor. Figure 46 on the following page depicts the length matching requirements between the command signals and clock. A nominal CMD package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 6.2 for more details on package length compensation.

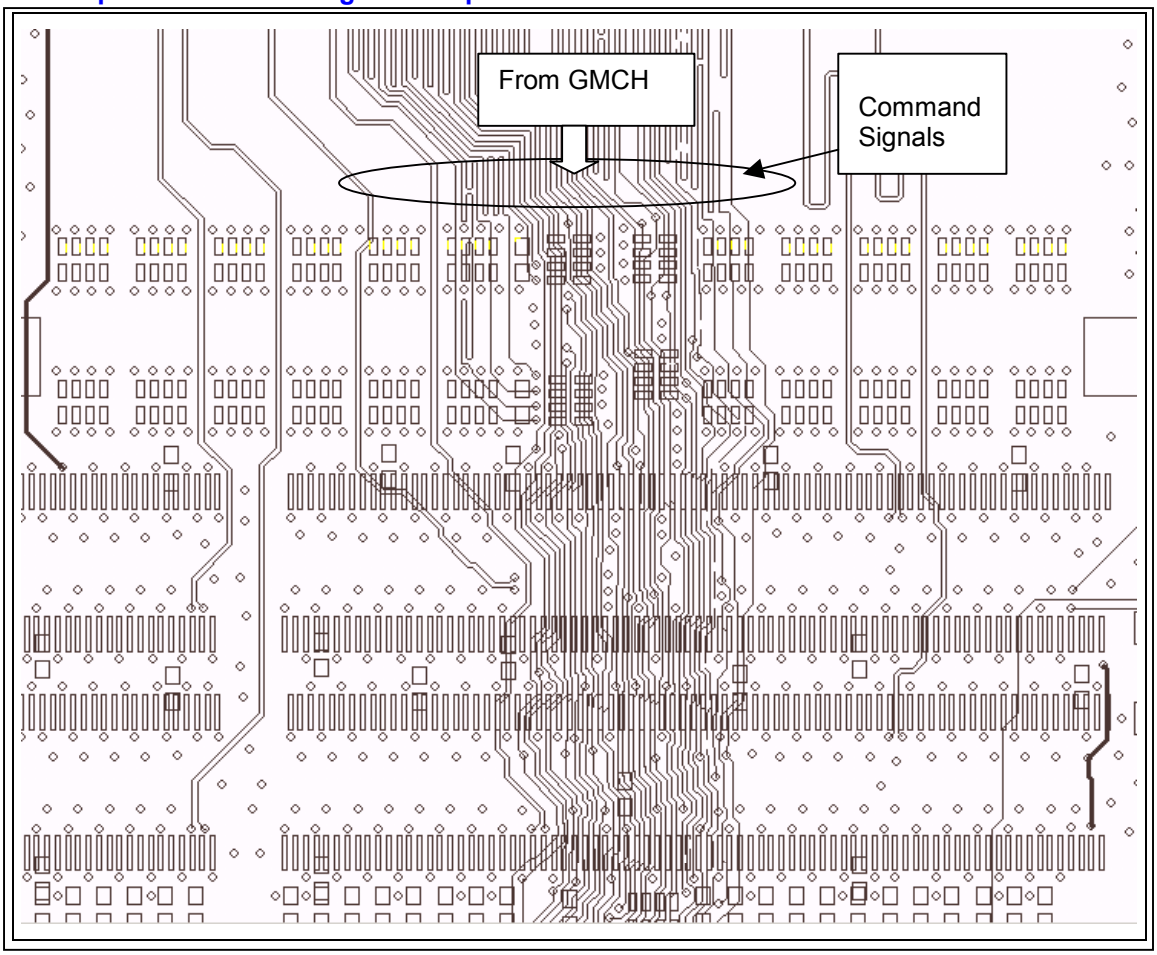
Figure 46. Topology 2 Command Signal to Clock Trace Length Matching Diagram



6.3.6.7. Command Topology 2 Routing Example

Figure 47 is an example of a board routing for the Command signal group.

Figure 47. Example of Command Signal Group



6.3.6.8. Command Topology 3

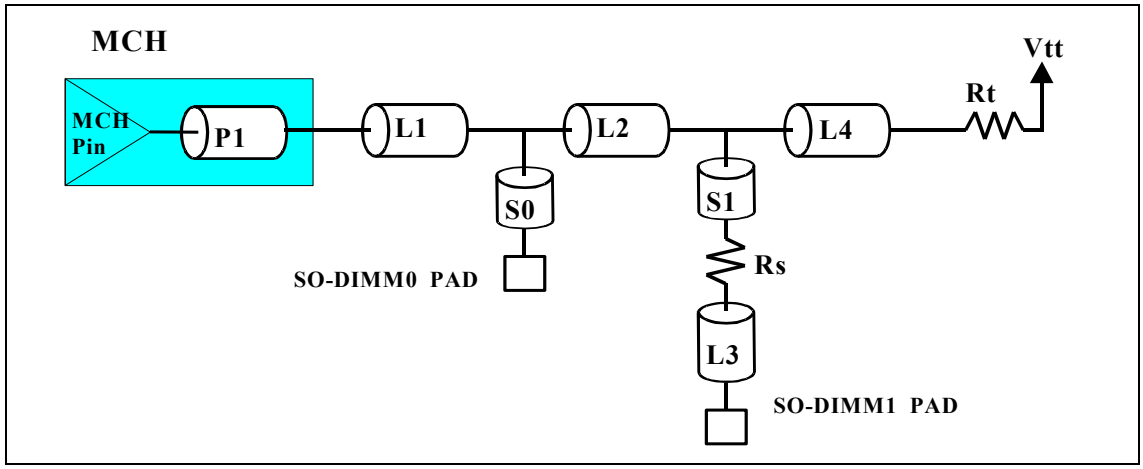
This topology is recommended when the SO-DIMMS are too close together for the series resistor to be placed between connectors. In this topology the series resistors are placed behind the second SO-DIMM.

External trace lengths should be minimized. It is suggested that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous. It is recommended that command signal group be routed on same internal layer.

It is suggested that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors but command signals can't be placed within the same R-packs as data, strobe or control signals. The diagrams and tables below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1.

Figure 48. Command Routing Topology 3



The command signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils of spacing to non-DDR related signals. Command signals should be routed on inner layers with minimized external trace lengths.

6.3.6.9. Command Topology 3 Routing Guidelines

Table 34. Command Topology 3 Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#
Motherboard Topology	Branched T with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils +/- 250 mils (See Table 35 for exact package lengths.)
Stub Length S0, S1	Max = 0.25”
Total Length L1+ S0 – Total length from GMCH ball to First SO-DIMM pad	Min = 0.5” Max = 4.0”
Trace Length L3 – Series Resistor Pad to Second SO-DIMM Pad	Max = 1.0”
Total Length L1+L2 + L3 + S1 – Total length from GMCH ball to Second SO-DIMM pad	Min = 1.0” Max = 7.0”
Total Length S0 + L2 + L3 + S1– Total SO-DIMM pad to SO-DIMM pad spacing	Max = 3.0”
Trace Length L4 – Second SO-DIMM Via to Parallel Resistor Pad	Max = 1.5”
Series Termination Resistor (Rs)	10Ω ± 5%
Parallel Termination Resistor (Rt)	56Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	6
Length Matching Requirements	CMD to SCK/SCK# [5:0] See length matching Section 6.3.6.10 and Figure 49 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using three vias if one via is shared that connects to the SO-DIMM0 pad and series termination resistor, if a via is shared that connects L1 to series termination and if one via is shared that connects to the SO-DIMM1 pad and parallel termination resistor.

6.3.6.10. Command Topology 3 Length Matching Requirements

The routed length of the command signals, between the GMCH package ball and the SO-DIMM must be within the range defined below, with respect to the associated clock reference length. Refer to Figure 45 for a definition of the various motherboard trace segments. The length of trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 46. Refer to Section 6.1 for more details on length matching requirements.

Length range formula for SO-DIMM0:

$\mathbf{X_0}$ = SCK/SCK#[2:0] total reference length, including package length.

$\mathbf{Y_0}$ = CMD signal total length = GMCH package + L1 + S0, as shown in Figure 49,

where: $(X_0 - 1.0") \le Y_0 \le (X_0 + 2.0")$ for DDR 200/266

$(X_0 - 2.0") \le Y_0 \le (X_0 + 2.0")$ for DDR 200/266/333

Length range formula for SO-DIMM1:

$\mathbf{X_2}$ = SCK/SCK#[5:3] total reference length, including package length.

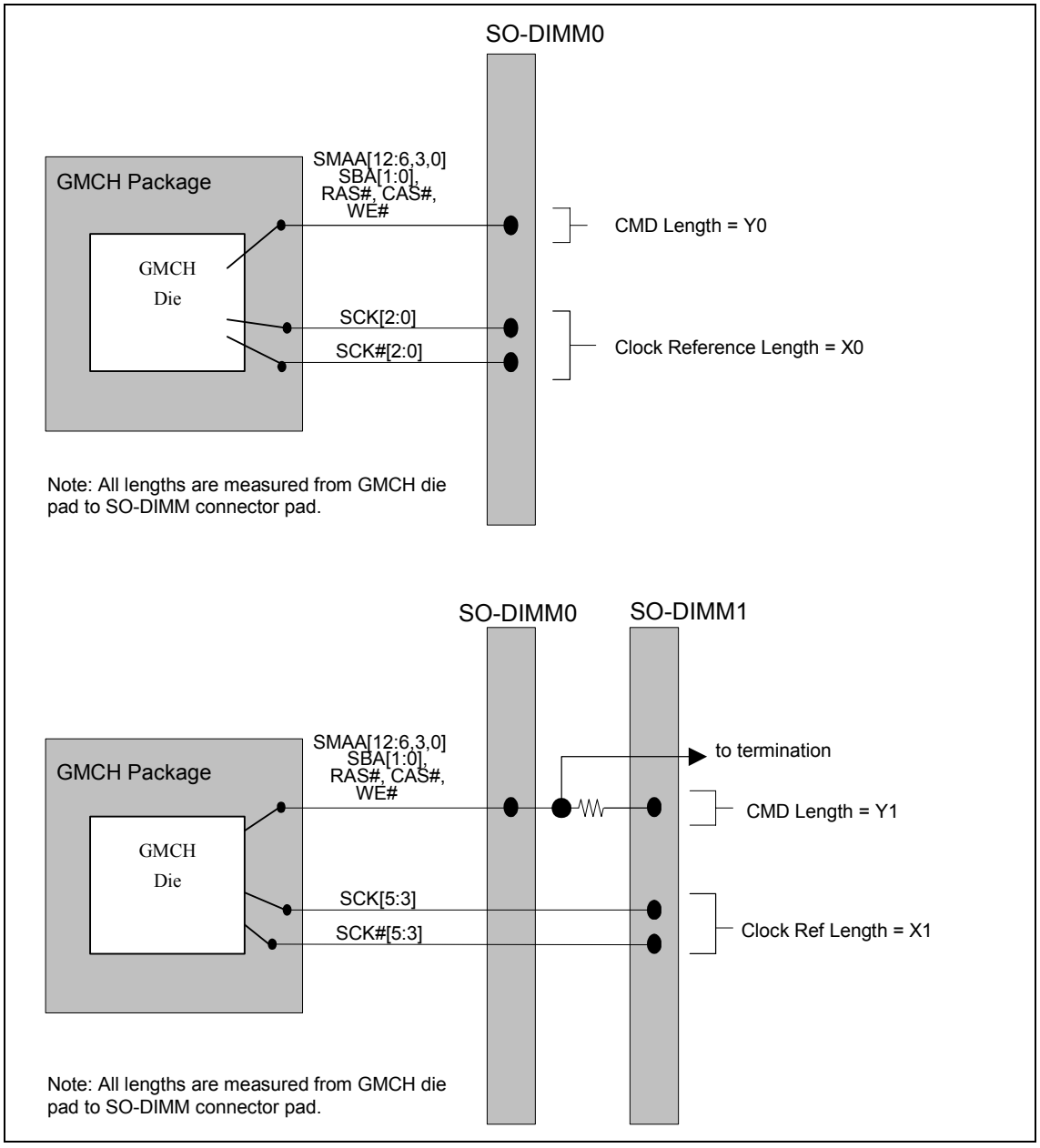
$\mathbf{Y_2}$ = CMD signal total length = GMCH package length + L1 + L2 +L3 + S1, as shown in Figure 49,

where: $(X_1 - 1.0") \le Y_1 \le (X_1 + 2.0")$ for DDR 200/266

$(X_1 - 2.0") \le Y_1 \le (X_1 + 2.0")$ for DDR 200/266/333

No length matching is required from SO-DIMM1 to the termination resistor. Figure 46 on the following page depicts the length matching requirements between the command signals and clock. A nominal CMD package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 6.2 for more details on package length compensation.

Figure 49. Topology 3 Command Signal to Clock Trace Length Matching Diagram



6.3.6.11. Command Group Package Length Table

The package length data in Table 35 below should be used to match the overall length of each command signal to its associated clock reference length.

Table 35. Command Group Package Lengths

Signal	Pin Number	Pkg Length (mils)
SMA[0]	AC18	420
SMA[3]	AD17	472
SMA[6]	AD8	591
SMA[7]	AD7	596
SMA[8]	AC6	630
SMA[9]	AC5	681
SMA[10]	AC19	377
SMA[11]	AD5	683
SMA[12]	AB5	609
SBA[0]	AD22	592
SBA[1]	AD20	435
SCAS#	AC24	562
SRAS#	AC21	499
SWE#	AD25	751

6.3.7. CPC Signals – SMA[5,4,2,1], SMAB[5,4,2,1]

The GMCH chipset CPC (clock-per-command) signals, SMA[5,4,2,1] and SMAB[5,4,2,1]are "clocked" into the DDR SDRAM devices using clock signals SCK/SCK#[5:0]. The GMCH drives the CPC and clock signals together, with the clocks crossing in the valid command window. The GMCH provides one set of CPC signals per SO-DIMM slot.

Refer to Table 29 for the CKE and CS# signal to SO-DIMM mapping.

Table 36. CPC Signal to SO-DIMM Mapping

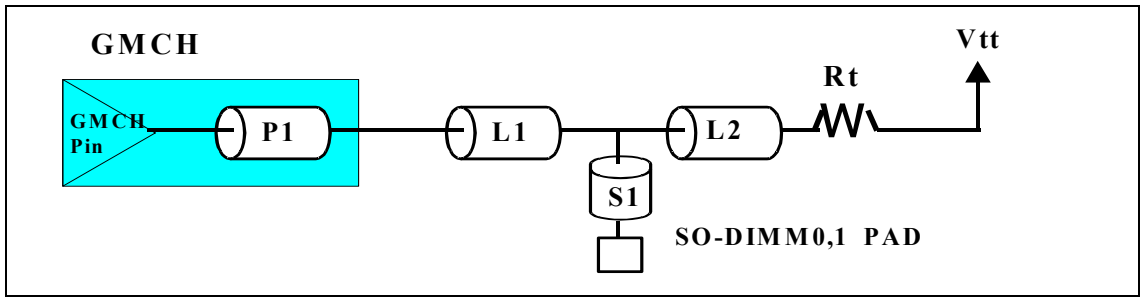
Signal	Relative To	SO-DIMM Pin
SMA[1]	SO-DIMM0	AD14
SMA[2]	SO-DIMM0	AD13
SMA[4]	SO-DIMM0	AD11
SMA[5]	SO-DIMM0	AC13
SMAB[1]	SO-DIMM1	AD16
SMAB[2]	SO-DIMM1	AC12
SMAB[4]	SO-DIMM1	AF11
SMAB[5]	SO-DIMM1	AD10

The guidelines below should be followed:

- The CPC signal routing should transition from an external layer to an internal signal layer under the GMCH.
- Keep to the same internal layer until transitioning back out to an external layer to connect to the appropriate pad of the SO-DIMM connector and the parallel termination resistor.
- If the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.
- External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths.
- All internal and external signals should be ground reference to keep the path of return current continuous. Intel suggests that all CPC signals be routed on the same internal layer.
- Resistor packs are acceptable for the parallel (Rt) CPC termination resistors. Figure 50 and Table 37 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM CPC signals.

6.3.7.1. CPC Signal Topology

Figure 50. Command per Clock Signal Routing Topology



The CPC signals should be routed using 2 to 1 trace space to width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20-mils of spacing to non-DDR related signals. CPC signals should be routed on inner layers with minimized external trace lengths.

6.3.7.2. CPC Signal Routing Guidelines

Table 37. CPC Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[5,4,2,1], SMAB[5,4,2,1]
Motherboard Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ±15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils +/- 250 mils (See Table 38 for exact package lengths.)
Stub Length S1	Max = 0.25”
Trace Length L1 – GMCH Control Signal Ball to SO-DIMM Pad	Min = 0.5 inches Max = 5.5 inches for DDR266 Max = 4.5 inches for DDR333
Trace Length L2 – SO-DIMM Via to Parallel Termination Resistor Pad	Max = 2.0 inches
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	3

Length Matching Requirements	CPC to SCK/SCK# [5:0] See length matching Section 6.3.7.3 and Figure 51 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. It is possible to route using 2 vias if one via is shared that connects to the SO-DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.

6.3.7.3. CPC to Clock Length Matching Requirements

The total length of the CPC signals, between the GMCH die pad and the SO-DIMM must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 50 for a definition of the various trace segments. The length the trace from the SO-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in

Figure 51. Refer to Section 6.1 for more details on length matching requirements. A table of CPC signal package length is provided in Section 6.3.7.4.

Length range formula for SO-DIMM0:

$\mathbf{X_0}$ = SCK/SCK#[2:0] total reference length, including package length.

$\mathbf{Y_0}$ = SMA[5,4,2,1] total length = GMCH package + L1 + S1, as shown in

Figure 51,

where: $(X_0 - 1.0") \le Y_0 \le (X_0 + 0.5")$ for DDR 200/266

$(X_0 - 2.0") \le Y_0 \le (X_0 - 1.0")$ for DDR 200/266/333

Length range formula for SO-DIMM1:

$\mathbf{X_1}$ = SCK/SCK#[5:3] total reference length, including package length.

$\mathbf{Y_1}$ = SMAB[5,4,2,1] total length = GMCH package + L1 + S1, as shown in

Figure 51,

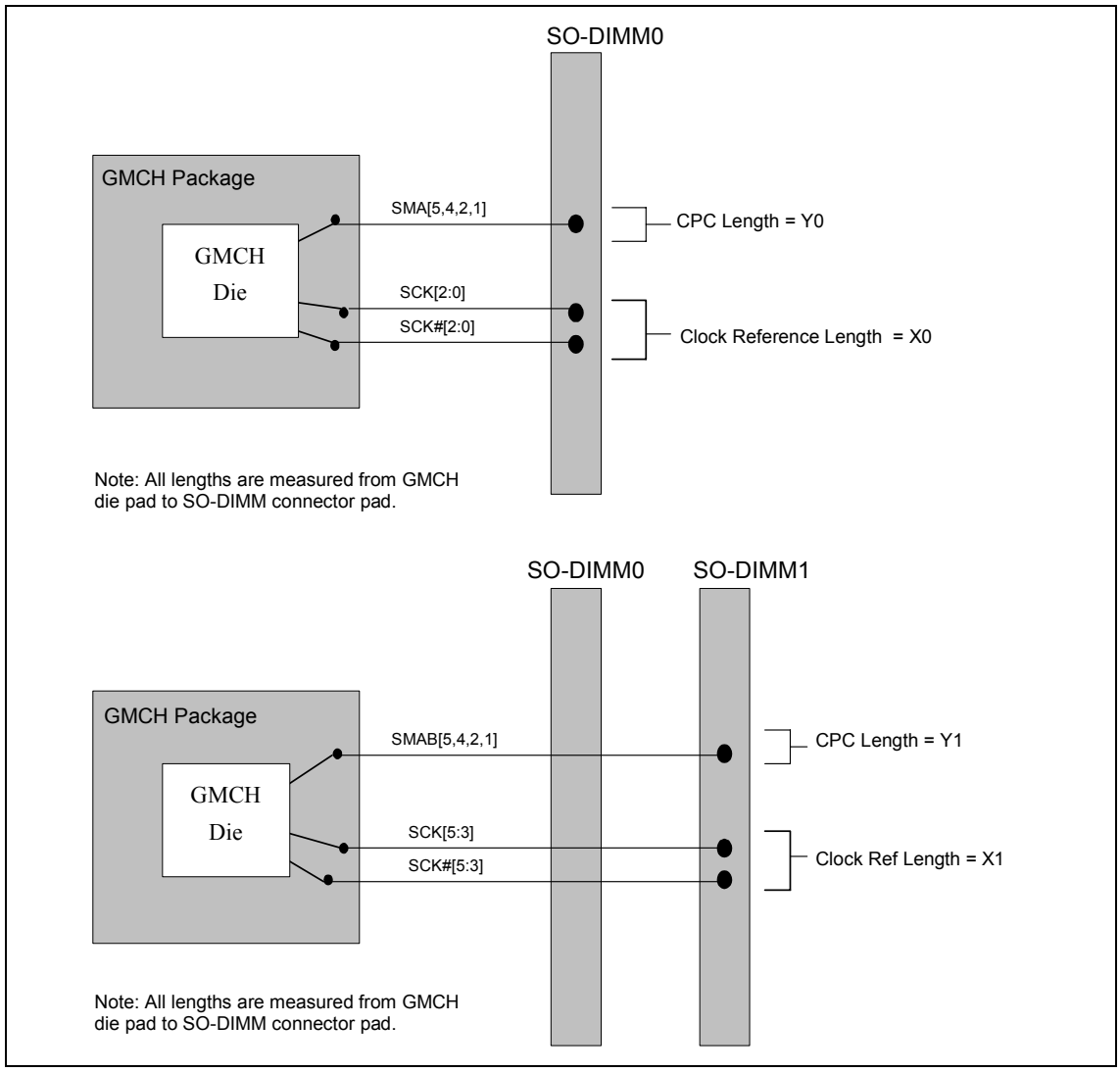
where: $(X_1 - 1.0") \le Y_1 \le (X_1 + 0.5")$ for DDR 200/266

$(X_1 - 2.0") \le Y_1 \le (X_1 - 1.0")$ for DDR 200/266/333

No length matching is required from SO-DIMM1 to the termination resistor.

Figure 51 on the following page depicts the length matching requirements between the CPC signals and clock. A nominal CPC package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 6.2 for more details on package length compensation.

Figure 51. CPC Signals to Clock Length Matching Diagram



6.3.7.4. CPC Group Package Length Table

The package length data in the table below should be used to match the overall length of each CPC signal to it's associated clock reference length.

Table 38. CPC Group Package Lengths

Signal	Pin Number	Pkg Length (mils)		Signal	Pin Number	Pkg Length (mils)
SMA[1]	AD14	398		SMAB[1]	AD16	427
SMA[2]	AD13	443		SMAB[2]	AC12	395
SMA[4]	AD11	430		SMAB[4]	AF11	716
SMA[5]	AC13	346		SMAB[5]	AD10	631

6.3.8. Feedback – RCVENOUT#, RCVENIN#

The Intel 855GM/GME chipset GMCH provides a feedback signal called "receive enable" (RCVEN#), which is used to measure timing for the read data.

The RCVENOUT# signal is shunted directly to RCVENIN# inside the package in order to reduce timing variance. With this change it is no longer necessary to provide an external connection. However, it is recommended that both signals be transitioned to the bottom side with vias located adjacent to the package ball in order to facilitate probing.

6.4. Routing Updates for "High-Density" Memory Device Support

The 855GM/GME chipset architecture supports 2GB memory. This memory capacity can be achieved using "high-density" memory devices of various package types. Intel has done only limited simulation and bench testing on these high-density SO-DIMM memory modules and has not seen any functional or analog inspection failures using existing layout guidelines. However, Intel has not done complete simulation nor validation with all the available package configurations. Customers are strongly encouraged to perform complete validation on their platforms based on the particular high-density memory package of their choice.

6.5. ECC Disable Guidelines

The GMCH can be configured to operate in an ECC data integrity mode that allows multiple bit error detection and single bit error correction. This option to support ECC DDR memory modules is dependent on design objectives. By default, ECC functionality is disabled on the platform.

6.5.1. GMCH ECC Functionality Disable

If non-ECC memory modules are to be the only supported memory type on the platform, then the 8 DDR check bits signals, associated strobe, data mask bit, and differential clock pairs associated with the ECC device for each SO-DIMM can be left as no connects on the GMCH. For the GMCH, this includes SDQ[71:64], SDQS8, SDM8 and the two differential clock pairs that are not routed to the SO-DIMMs.

The 855GM/GME chipset GMCH provides the capability to enable and disable the CS/CKE control and SCK signals to unpopulated SO-DIMMs to save power. Although DDR SO-DIMM connectors may provide motherboard lands for three clock pairs, non-ECC SO-DIMMs only require two pairs.

The GMCH provides some flexibility on how the SCK clock pairs, control signals and CPC signals are assigned to the SO-DIMMs, provided that BIOS initialization of memory matches the hardware configuration. Two examples are listed below. Refer to the *Intel(R) 855GM/GME Memory Reference Code* for more details.

Example 1		*Example 2*	
SO-DIMM0	**SO-DIMM1**	**SO-DIMM0**	**SO-DIMM1**
SCK0,1,2	SCK3,4,5	SCK0,1,2	SCK3,4,5
SMAA[1,2,4,5]	SMAB[1,2,4,5]	SMAB[1,2,4,5]	SMAA[1,2,4,5]
SCKE0,1; SCS#0,1	SCKE2,3; SCS#2,3	SCKE0,1; SCS#0,1	SCKE2,3; SCS#2,3

On platforms where ECC memory is supported, it is important that all relevant SDQ, SDQS, and SCK signals to the SO-DIMMs be disabled when the system is populated with only non-ECC or a combination of ECC and non-ECC memory.

Please see the *RS – Intel 855GM/GME (Montara-GM/GM+) Chipset GMCH BIOS Specification* for information on memory initialization and register programming.

6.5.2. DDR Memory ECC Functionality Disable

It is imperative that systems that do not support ECC memory ensure the SCK clock pairs that are normally sent to ECC SO-DIMMs be disabled. If the SCK clock pairs associated with the check bit signals were left floating in a non-ECC memory only system and ECC memory was used in one or more of the SO-DIMM slots, this could cause the ECC device on the SO-DIMM to be enabled. If SDQ[71:64] is disabled/tri-stated or not routed, then these floating inputs can cause the ECC device to draw current and potentially compromise the ECC device.

In *JEDEC PC2100 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Rev 1.0*, it is noted that pin 89 and pin 91 (CK2 and CK2#) of the SO-DIMM connector are reserved for x72 modules or registered modules. By default, 855GM/GME does not drive SCK2, SCK2#, SCK5, SCK5#. Therefore, it is important to make sure that the memory modules are not expected to use all clock pairs

6.6. System Memory Compensation

See Section 13.5.2.3 for details.

6.7. SMVREF Generation

See Section 13.5.2.2 for details.

6.8. DDR Power Delivery

See Section 13.5 for details.

6.9. External Thermal Sensor Based Throttling (ETS#)

The GMCH's ETS# input pin is an active low input that can be used with an external thermal sensor to monitor the temperature of the DDR SO-DIMMs for a possible thermal condition. Assertion of ETS# will result in the limiting of DRAM bandwidth on the DDR memory interface to reduce the temperature in the vicinity of the system memory.

By default, the functionality and input buffer associated with ETS# are disabled. Also, the GMCH can be programmed to send an SERR, SCI, or SMI message to the ICH4-M upon the assertion of this signal. External thermal sensors that are suitable for the purpose described above would need to have a small form factor and be able to accurately monitor the ambient temperature in the vicinity of the DDR system memory.

Intel is currently in the process of enabling this feature on the Intel 855GM/GME chipset GMCH and is actively engaging with thermal sensor vendors to ensure compatibility and suitability of vendors' products with the ETS# pin. This includes electrical design guidelines for the ETS# pin and usage/placement guidelines of the thermal sensors for maximum effectiveness. Current third party vendor product offerings that may be suitable for the ETS# pin application include ambient temperature thermal sensors and remote diode thermal sensors. Also, thermal sensors that implement an open-drain output for signaling a thermal event would provide the most flexibility from an electrical and for layout design perspective.

6.9.1. ETS# Usage Model

The thermal sensors targeted for this application with the GMCH's ETS# are planned to be capable of measuring the ambient temperature only and should be able to assert ETS# if the preprogrammed thermal limits/conditions are met or exceeded. Because many variables within a mobile system can affect the temperature measured at any given point in a system, the expected usage and effectiveness of ETS# is also very focused. Because of factors such as thermal sensor placement, airflow within a mobile chassis, adjacent components, thermal sensor sensitivity, and thermal sensor response time, ETS# can effectively be used for controlling skin temperatures. However, due to the location of the thermal sensor, ETS# should not be used for measuring or controlling the Tj or Tcase parameters of DDR-SDRAM devices since it cannot respond quickly enough to dynamic changes in DRAM power.

6.9.2. ETS# Design Guidelines

ETS#, as implemented in the GMCH, is an active low signal and does **not** have an integrated pull-up to maintain a logic 1. As a result of this, an external 8.2 kΩ to 10 kΩ pull-up resistor should be provided near the ETS# pin, connected to 3.3V. Ideally, the thermal sensor should implement an open drain type output buffer to drive ETS#. A system is expected to have one thermal sensor per SO-DIMM connector on the motherboard.

6.9.3. Thermal Sensor Routing and Placement Guidelines

Routing guidelines and other special, motherboard design considerations will vary with the vendor and type of thermal sensor chosen for this ETS# application. As a result, vendor specific design guidelines should also be followed closely to ensure proper operation of this feature. As a general rule, system designers should follow good design practices in ensuring good signal integrity on this signal as well as achieving adequate isolation from adjacent signals. Also, any thermal design considerations (e.g. proper ground flood placement underneath the external thermal sensor; proper isolation of the differential signal routing for thermal diode applications, etc.) for the external thermal sensor itself should also be met.

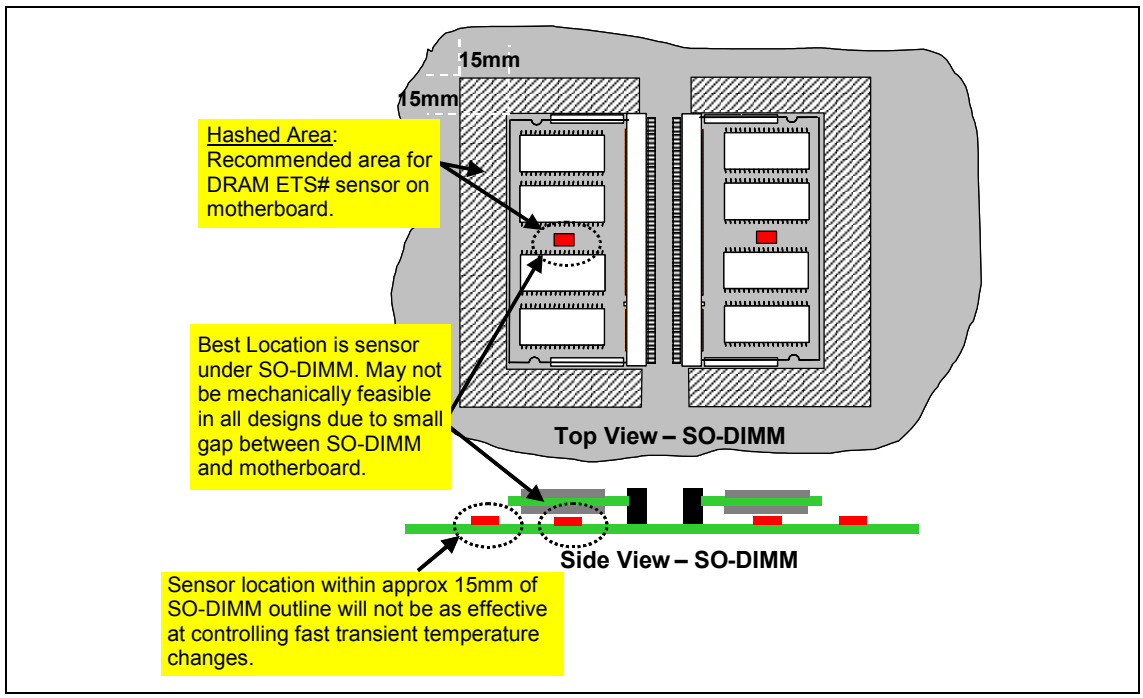
The many factors that can affect the accuracy of ambient temperature measurements by thermal sensors make the placement of them a very critical and especially challenging task. Ideally, one thermal sensor should be placed near each SO-DIMM in a system. The thermal sensor should be located in an area where the effects of airflow and effects of conduction from adjacent components are minimized. This

allows for the best correlation of thermal sensor temperature to chassis or notebook surface temperature. See Figure 52 for details.

Assuming airflow is negligible within a system, the optimal placement of the thermal sensor is on the surface of the motherboard directly beneath the shadow of an SO-DIMM module centered longitudinally and laterally in relation to the outline of the SO-DIMM. The thermal sensor should have a form factor small enough to allow it to fit beneath double-sided memory modules (i.e. modules with memory devices on both sides of a module). If placement within the outline of an SO-DIMM is not possible, then the next best option is to locate it within approximately 15 mm (0.6 inches) of the outline/SO-DIMM shadow. Again, this assumes negligible effects from airflow.

Please refer to the *Intel (R) 855GM (Montara-MG) Chipset Mobile Thermal Design Guide* for more details.

Figure 52. DDR Memory Thermal Sensor Placement



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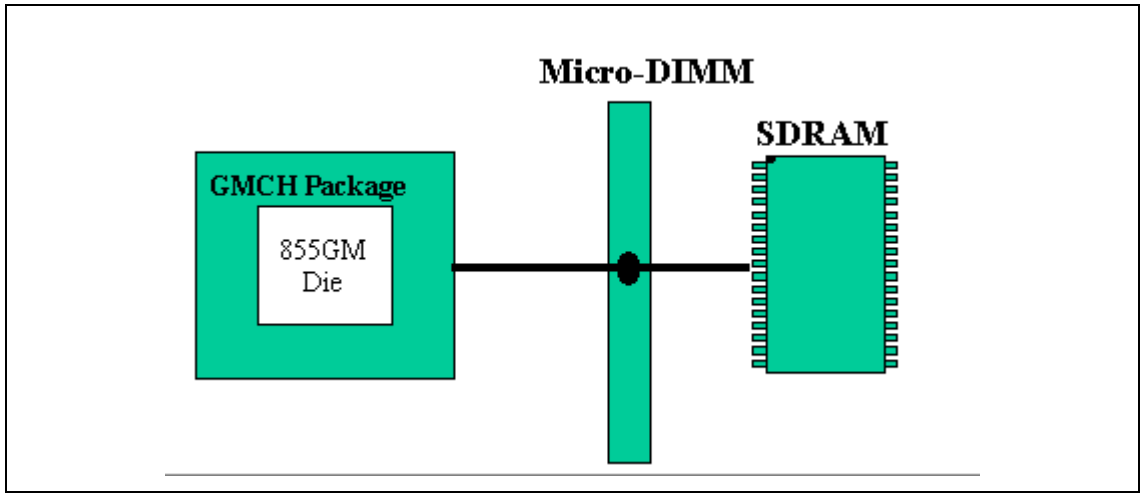
7. System Memory Design Guidelines (DDR-SDRAM) for Memory Down Configuration

This section contains routing guidelines for a Micro-DIMM and memory soldered onto the motherboard (Memory Down) configuration. The order of routing for this configuration is specific. It is recommended the designer route to the Micro-DIMM first and the Memory Down devices second (See Figure 53.)

Figure 53. Recommended Device Order for Micro-DIMM/Memory Down Combination



Trace length parameters for the memory down configuration are based on trace length recommendations given in the PC2700 Unbuffered DDR Micro-DIMM Reference Design Specification, PC2700/PC2100 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification rev 1.1, simulation and routing studies. The parameters were simulated at various trace lengths to provide designers with greater flexibility in placing and routing SDRAM devices.

These guidelines support PC2100 (266MHz) and PC2700 (333MHz) SDRAM devices. Table 1 shows the supported memory configurations for the Micro-DIMM per the PC2700 Unbuffered DDR Micro-DIMM Reference Design Specification and Table 39 shows the supported memory configurations for Memory Down.

Table 39. Supported Memory Configurations - Micro-DIMM

Device Type	Module Bus Width	Device Width	#Devices	Physical Banks	Capacity
TSOP	x64	x16	4	1	32-256 MB
BGA	x64	x16	4	1	32-512 MB
BGA	x64	x16	8	2	64 MB – 1 GB

Table 40. Supported Memory Configurations - Memory Down

Device Type	Bus Width	Device Width	#Devices	Physical Banks	Max Capacity
TSOP	x64	x16	4	1	256 MB
BGA	x64	x16	4	1	256 MB
BGA	x64	x16	8	2	512 MB
BGA	x64	x8	8	1	512 MB

These guidelines support standard TSOP and BGA packages in 64Mb, 128Mb, 256Mb, and 512Mb memory densities. Stacked memory technologies are not supported (i.e. Stacked TSOP, DDP). The following SDRAM device placement strategies are recommended for the different device types and configurations. For a 4-TSOP device configuration, two on the top and two on the bottom is recommended. For a 4-BGA device configuration, all devices are on the same side of the motherboard. For an 8-BGA device configuration, four devices are placed on one side of the motherboard and four on the opposite side.

The 855GM/GME chipset Double Data Rate (DDR) SDRAM system memory interface consists of SSTL-2 compatible signals. These SSTL-2 compatible signals have been divided into several signal groups: Data, Control, Command, CPC, Clock, and Feedback signals. Table 41 summarizes the different signal grouping. Refer to the *Intel® 855GM/GME Chipset External Design Specification* for details on the signals listed. ECC is not supported by these routing guidelines. Data bits SDQ[71:64], SDQS[8], and SDM[8] are no connects.

Table 41. Montara-GM GMCH Chipset DDR Signal Groups

Group	Signal Name	Description
Clocks	SCK[4,3,1,0]	DDR-SDRAM Differential Clocks
	SCK#[4,3,1,0]	DDR-SDRAM Inverted Differential Clocks
Data	SDQ[63:0]	Data Bus
	SDQS[8:0]	Data Strobes
	SDM[8:0]	Data Mask
Control	SCKE[3:0]	Clock Enable - (One per Device Row)
	SCS#[3:0]	Chip Select - (One per Device Row)
Command	SMA[12:6,3,0]	Memory Address Bus
	SBA[1:0]	Bank Select
	SRAS#	Row Address Select
	SCAS#	Column Address Select
	SWE#	Write Enable
CPC	SMA[5,4,2,1]	Command per Clock (Micro-DIMM)
	SMAB[5,4,2,1]	Command per Clock (Memory Down)
Feedback	RCVENOUT#	Receive Enable Output (no external connection)
	RCVENIN#	Receive Enable Input (no external connection)

7.1. Length Matching and Length Formulas

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width, spacing geometries, and absolute minimum and maximum routed lengths for each signal group. These parameters are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching formulas are also provided. These formulas further restrict the minimum to maximum length range of each signal group with respect to clock, within the overall boundaries defined in the guideline tables, as required to guarantee adequate timing margins. These secondary constraints are referred to as length matching constraints and the formulas used are referred to as length matching formulas.

All signal groups, except feedback signals, are length matched to the DDR clocks. The clocks on a given Micro-DIMM or memory down configuration are length matched to within ± 25 mils of the target length. A different clock target length may be used for each Micro-DIMM. The difference in clock target lengths between Micro-DIMM and Memory Down should not exceed 2 inches. A simple summary of the length matching formulas for each signal group is provided in Table 42

Table 42. Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock –1.0”	Clock + 0.5”
Command to Clock	Clock – 2.0”	Clock + 2.0”
CPC to Clock	Clock – 1.0”	Clock + 0.5”
Strobe to Clock	Clock – 2.0”	Clock + 0.5”
Data to Strobe	Strobe – 25 mils	Strobe + 25 mils

Note: All length matching formulas are based on GMCH die-pad to Micro-DIMM connector pad or Memory Down device pin total length.

Package length tables are provided for all signals in order to facilitate this pad-to-pin matching. The clock lengths to Memory Down may be up to 2 inches longer than the clock lengths to the Micro-DIMM. Length formulas should be applied to Micro-DIMM and Memory Down separately. The full geometry and routing guidelines along with the exact length matching formulas and associated diagrams are provided in the individual signal group guidelines sections.

7.2. Package Length Compensation

As mentioned in Section 7.1, all length matching is done from the GMCH die-pad to Micro-DIMM connector pad or memory device pin. The reason for this is to compensate for the package length variation across each signal group. The GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the 855GM/GME GMCH requires length matching.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the min and max length bounds of a signal group based on clock length, whereas package length compensation refers to the process of adjusting out package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the

length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as a secondary operation.

7.3. Topologies and Routing Guidelines

The 855GM/GME GMCH chipset's Double Data Rate (DDR) SDRAM system memory interface implements the low swing, high-speed, terminated SSTL_2 topology. This section contains information related to the recommended interconnect topologies and routing guidelines for each of the signal groups which comprise the DDR interface. When implemented as defined, these guidelines will provide for a robust DDR solution on a 855GM/GME GMCH chipset based design..

7.3.1. Clock Signals – SCK[4,3,1,0], SCK#[4,3,1,0]

The clock signal group includes the differential clock pairs SCK/SCK#[4,3,1,0]. SCK/SCK#[5,2] are not used for this configuration and are not connected on the motherboard. The GMCH generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. The GMCH supports unbuffered DDR Micro-DIMM; two differential clock pairs are routed to the Micro-DIMM connector and two to the Memory Down configuration. Table 43 summarizes the clock signal mapping.

Table 43. Clock Signal Mapping

Signal	Relative To
SCK/SCK#[1:0]	Micro-DIMM
SCK/SCK#[4:3]	Memory Down

7.3.2. Clock Topology Diagram

The 855GM/GME GMCH provides 6 differential clock output pairs. The motherboard clock routing topology is shown below for reference. Refer to the routing guidelines in Table 44 on the follow page for detailed length and spacing rules for each segment.

Figure 54. DDR Clock Routing to Micro-DIMM

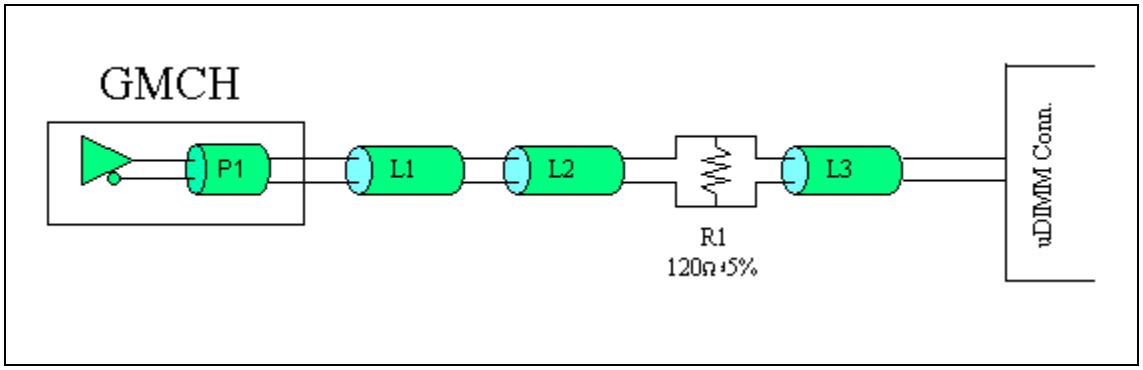


Figure 55. DDR Clock Routing to Memory Down Two Load BGA

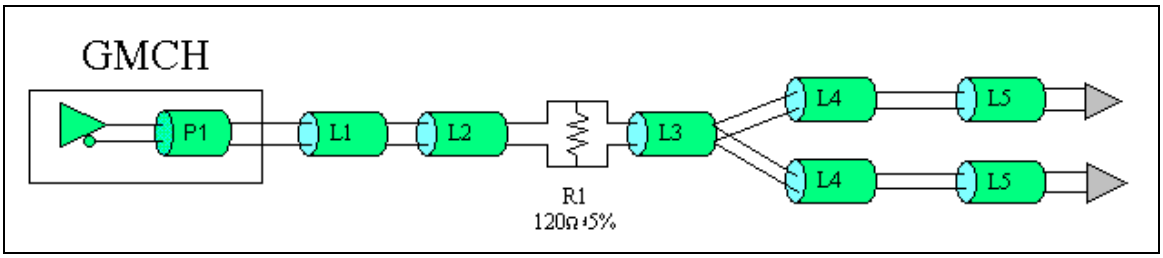


Figure 56. DDR Clock Routing to Memory Down Two Load TSOP

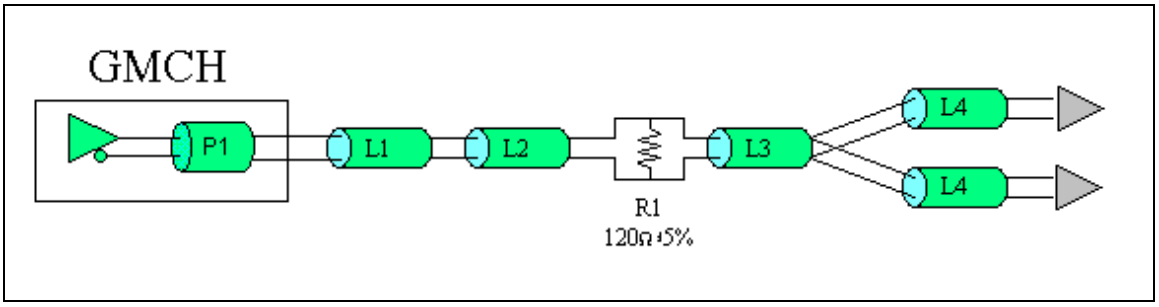
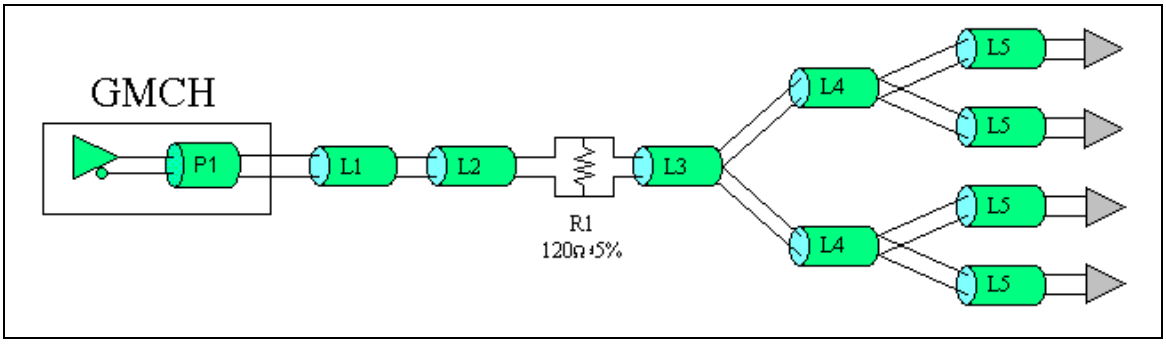


Figure 57. DDR Clock Routing to Memory Down 4 Load BGA



The clock signals should be routed as closely coupled differential pairs over the entire length. Spacing to other DDR signals should not be less than 20 mils. Isolation spacing to non-DDR signals should be 25 mils.

7.3.3. DDR Clock Routing Guidelines

Table 44. Clock Signal Group Routing Guidelines

Parameter	Definition
Signal Group	SCK[5:0] and SCK#[5:0]
Topology	Differential Pair Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	42 ohms +/-15%
Differential Mode Impedance (Zdiff)	70 ohms +/- 15%
Nominal Trace Width (see exceptions for breakout region below)	Inner Layers: 7 mils Outer Layers: 8 mils (pin escapes only)
Nominal Pair Spacing (edge to edge) (see exceptions for breakout region below)	Inner Layers: 4 mils Outer Layers: 5 mils (pin escapes only)
Minimum Pair to Pair Spacing (see exceptions for breakout region below)	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other DDR Signals (see exceptions for breakout region below)	20 mils
Minimum Isolation Spacing to non-DDR Signals	25 mils
Maximum Via Count	2 (per side Micro-Dimm) 5 (per side Memory Down)
Package Length Range – P1	1000 mils +/- 350mils (See clock package length Table 45 for exact lengths.)
L1	Max = 300 mils (breakout segment)
L2	Min = 0.25 inches Max = 4.5 inches
L3	Max = .5” inches (see Figure 54) Min = 0.25 in. Max = 1.0 in. (See Figure 55, Figure 56 and Figure 57)
L4	Max = 0.5 inches (see Figure 55 and Figure 57) Max = 0.25 inches (see Figure 56)
L5	Max = 0.25 inches
Total Length	Total length target is determined by placement (see Figure 54, Figure 55, Figure 56 and Figure 57) Total length for Micro-DIMM group = X0 (see Figure 58) Total length for Memory Down group = X1 (see Figure 58)
SCK to SCK# Length Matching	Match total length to +/- 10 mils (see Section 7.3.3.1)
Clock to Clock Length Matching (Total Length)	Match all Micro-DIMM clocks to X0 +/- 25 mils (see section 7.3.3.2) Match all Memory Down clocks to X1 +/- 25 mils (see section 7.3.3.2)

Parameter	Definition
Breakout Exceptions (Reduced geometries for GMCH breakout region)	Inner Layers: 4 mil trace, 4 mil pair space allowed Outer Layers: 5 mil trace, 5 mil pair space allowed Pair to pair spacing of 5 mils allowed Spacing to other DDR signals of 5 mils allowed Maximum breakout length is 0.3”

NOTES:
1. Pad to Pin length tuning is utilized on clocks in order to achieve minimal variance. Package lengths range between approximately 600 mils and 1400 mils. Exact package lengths for each clock signal are provided at the end of this Section. Overall target length should be established based on placement and routing flow. The resulting motherboard segment lengths must fall within the ranges specified.
2. The DDR clocks should be routed on internal layers, except for pin escapes. It is recommended that pin escape vias be located directly adjacent to the ball pads on all clocks. Surface layer routing should be minimized.
3. Exceptions to the trace width and spacing geometries are allowed in the breakout region in order to fanout the interconnect pattern. Reduced spacing should be avoided as much as possible.

7.3.3.1. Clock Length Matching Requirements

The GMCH chipset provides two differential clock pairs for the Micro-DIMM and two pairs for Memory Down. A differential clock pair is made up of a SCK signal and its complement signal SCK#. Refer to Section 2.2 for more details on length matching requirements.

The differential pairs for the Micro-DIMM are:

SCK[0] / SCK#[0]
SCK[1] / SCK#[1]

The differential pairs for Memory Down are:

SCK[3] / SCK#[3]
SCK[4] / SCK#[4]

The SCK[2]/SCK#[2] and SCK[5]/SCK#[5] differential clock signals are not routed for this configuration and should be left as no connects on the motherboard. These clocks are associated with ECC. ECC is not supported by these routing guidelines.

The two sets of differential clocks must be length tuned on the motherboard such that any pair to pair package length variation is tuned out. The three pairs associated with Micro-DIMM are tuned to a fixed overall length, including package, and the two pairs associated with Memory Down are tuned to a fixed overall length.

The two traces associated with each clock pair are length matched within the package, however some additional compensation may be required on the motherboard in order to achieve the ± 10 mil length tolerance within the pair.

Between clock pairs the package length varies substantially. Therefore, the motherboard length of each clock pair must be length adjusted to tune out package variance. The total length including package should be matched to within ± 25 mils of each other, as shown in the

Length Range Formula for Micro-DIMM:

X0 = SCK/SCK#[1:0] P1 + L1 + L2 + L3 (see Figure 54)

Length Range Formulas for Memory Down:

X1 = SCK/SCK#[4:3] P1 + L1 + L2 + L3 + L4 (see Figure 55)

= SCK/SCK#[4:3] P1 + L1 + L2 + L3 + L4 + L5 (see Figure 56 and Figure 57)

This may result in a clock length variance of as much as 700 mils on the motherboard.

The first step in determining the routing lengths for clocks and all other clock relative signal groups is to establish the target length for each clock group. These target lengths are shown as X0 and X1, in

Length Range Formula for Micro-DIMM:

X0 = SCK/SCK#[1:0] P1 + L1 + L2 + L3 (see Figure 54)

Length Range Formulas for Memory Down:

X1 = SCK/SCK#[4:3] P1 + L1 + L2 + L3 + L4 (see Figure 55)

= SCK/SCK#[4:3] P1 + L1 + L2 + L3 + L4 + L5 (see Figure 56 and Figure 57)

These are the lengths to which all clocks within the corresponding group will be matched, and the reference length values used to calculate the length ranges for the other signal groups.

7.3.3.2. Clock Reference Lengths

The clock reference length for each Micro-DIMM and Memory Down clock group is determined by first determining the longest total clock length required to complete the clock routing. A table of clock package lengths is provided in Table 45 to assist in this calculation. Once the longest total length is determined for each clock group, this becomes a lower bound for the associated clock reference length. At this point it is helpful to have completed a test route of the SDQ/SDQS bus such that final clock reference lengths can be defined with consideration of the impact on SDQ/SDQS bus routability. Some iteration may be required.

Once the reference lengths X0 and X1 are defined then the next step is to tune each clock pair's motherboard trace segment lengths as required such that the overall length of each clock equals the associated clock reference length plus or minus the 25 mil tolerance. Again, the reference length for the two sets of clocks should be offset by the nominal routing length between the Micro-DIMM connector pad and Memory Down Device Pin.

Length Range Formula for Micro-DIMM:

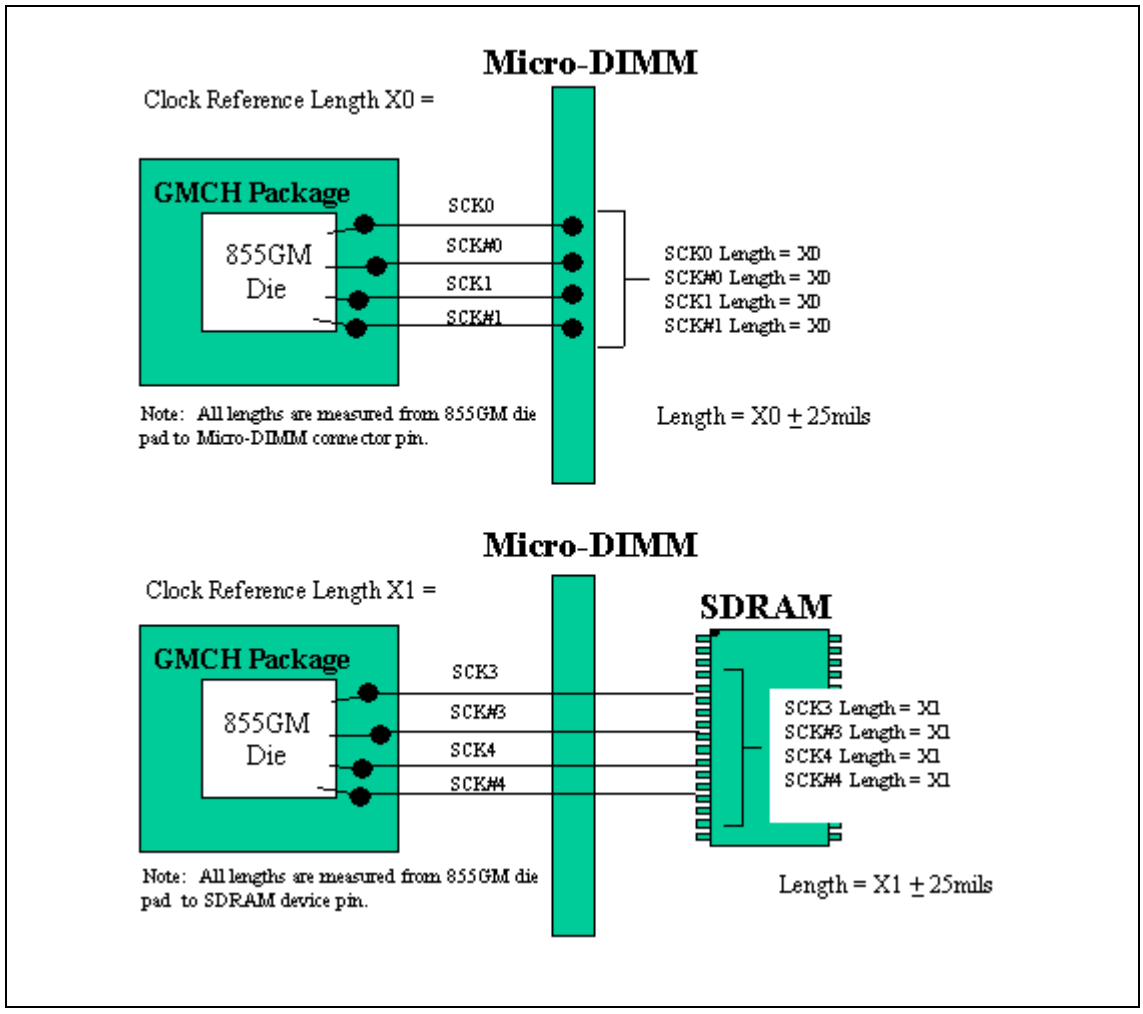
X0 = SCK/SCK#[1:0] P1 + L1 + L2 + L3 (see Figure 54)

Length Range Formulas for Memory Down:

X1 = SCK/SCK#[4:3] P1 + L1 + L2 + L3 + L4 (see Figure 55)

= SCK/SCK#[4:3] P1 + L1 + L2 + L3 + L4 + L5 (see Figure 56 and Figure 57)

Figure 58. DDR Clock Trace Length Matching Diagram



7.3.3.3. Clock Package Length Table

The package length data in the table below should be used to tune the motherboard length of each SCK/SCK# clock pair between the GMCH and the Micro-DIMM connector or memory down component. It is recommended that die-pad to Micro-DIMM or memory down component pad length be tuned to within ± 25 mils in order to optimize timing margins on the interface.

Table 45. DDR Clock Package Lengths

Signal	Pin Number	Package Length (mils)
SCLK_0	AB2	1177
SCLK#_0	AA2	1169
SCLK_1	AC26	840
SCLK#_1	AB25	838
SCLK_2	AC3	1129
SCLK#_2	AD4	1107
SCLK_3	AC2	1299
SCLK#_3	AD2	1305
SCLK_4	AB23	643
SCLK#_4	AB24	656
SCLK_5	AA3	1128
SCLK#_5	AB4	1146

Package length compensation can be performed on each individual clock output thereby matching total length on SCK/SCK# exactly, or alternatively the average package length can be used for both outputs of a pair and length tuning done with respect to the motherboard portion only.

7.3.4. Data Signals – SDQ[63:0], SDM[7:0], SDQS[7:0]

The GMCH data signals are source synchronous signals that include a 72-bit wide data bus, 8 check bits for Error Checking and Correction (ECC), a set of 9 Data Mask bits, and a set of 9 data strobe signals. There is an associated data strobe and data mask bit for each of the 8-bit data byte groups, making for a total of nine – 10-bit byte lanes. ECC is a feature not supported by Micro-DIMMs and will therefore not be supported by the memory down topology. It is recommended that these signals be left as no connects. Further reference to data signals reserved for ECC will not be made in this RDDP addendum. This section summarizes the SDQ/SDM to SDQS routing guidelines and length matching recommendations.

The data signals include SDQ [63:0], SDM[7:0], and SDQS[7:0].

- The data signals should transition from an external layer to an internal signal layer under the GMCH.
- At the Micro-DIMM connector, the signal should transition to an external layer and connect to the appropriate pad on the connector.
- After the Micro-DIMM transition, continue to route the signal on the same internal layer until transitioning back to an external layer at the series resistor.

- After the series resistor, the signal should transition from the external layer to the same internal layer and route to the SDRAM device.
- Transition back out to an external layer and connect to the appropriate SDRAM pad.
- Connection to the termination resistor should be via the same internal layer with a transition back to the external layer near the resistor. External trace lengths should be minimized.

To facilitate routing, swapping of the byte lanes is allowed for SDQ[63:0] only. Bit swapping within the byte lane is also allowed for SDQ[63:0] only. All internal and external signals should be ground sandwiched to keep the path of the return current continuous.

Resistor packs are acceptable for the series (Rs) and parallel (Rt) data and strobe termination resistors, but data and strobe signals cannot be placed within the same R pack as the command or control signals. The table and diagrams below depict the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Intel recommends that the full data bus SDQ[63:0], mask bus SDM[7:0], and strobe signals SDQS[7:0] be routed on the same internal signal layer. It is required that the SDQ byte group and the associated SDM and SDQS signals within a byte lane be routed on the same internal layer.

The total length of SDQ, SDM, and SDQS traces between the GMCH and the Micro-DIMM/Memory Down devices must be within the range defined in the overall guidelines, and is also constrained by a length range boundary based on SCK/SCK# clock length, and a SDQ/SDM to SDQS length matching requirement within each byte lane. Note also that all length matching must be done inclusive of package length. A table of SDQ, SDM, and SDQS package lengths is provided at the end of this Section to facilitate this process.

There are two levels of matching implemented on the data bus signals.

- The first is the length range constraint on the SDQS signals based on clock reference length.
- The second is SDQ/SDM to SDQS length matching within a byte lane.

The length of the SDQS signal for each byte lane must fall within a range determined by the clock reference length, as defined in the SDQS to SCK/SCK# length matching section. The actual length of SDQS for each byte lane may fall anywhere within this range based on placement and routing flow.

Once the SDQS length for a byte lane is established, the SDQ, SDM, and SDQS signals within the byte lane must be length matched to each other, inclusive of package length, as described in the SDQ to SDQS length matching section.

7.3.4.1. Data Bus Topology

Figure 59. Data Signal Routing GMCH to 1x16 TSOP/BGA & /1x8 BGA Configuration

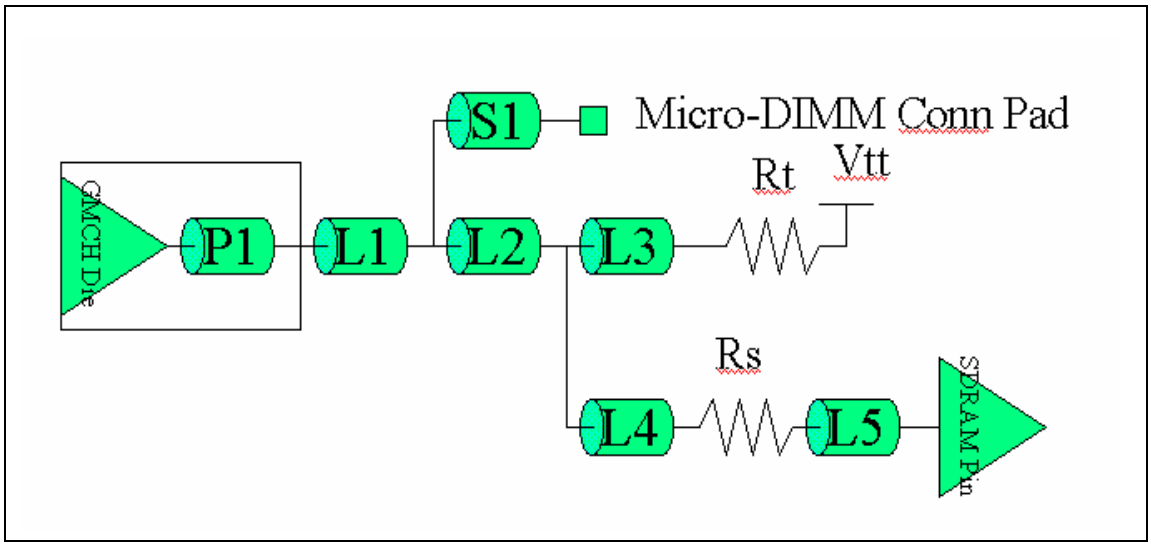
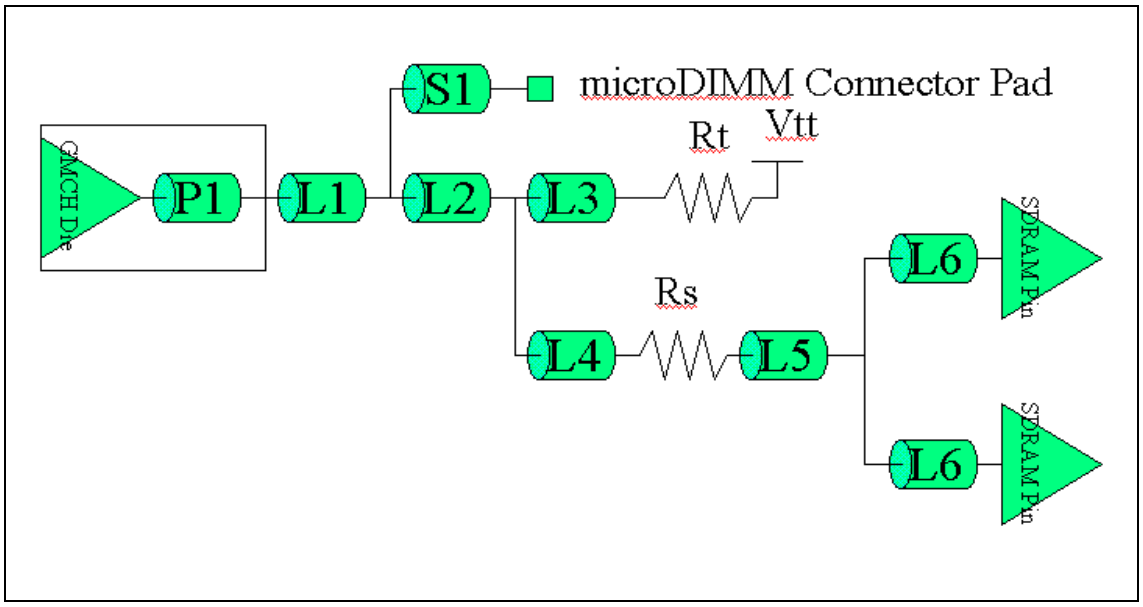


Figure 60. Data Signal Routing GMCH to 2x16 BGA Configuration



The data signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils of spacing to non-DDR related signals. Data signals should be routed on inner layers with minimized external trace lengths.

Table 46. Data Signal Group Routing Guidelines

Parameter	Definition
Signal Group	SDQ[63:0], SDQS[7:0], SDM[7:0]
Motherboard Topology	Daisy Chain with Parallel Termination
Reference Plane	Ground sandwiching required
Characteristic Trace Impedance (Zo)	55 Ω +/- 15%
Parallel Termination Resistor (Rt)	56 Ω +/- 5%
Series Resistor (Rs)	33 Ω +/- 5%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	SDQ/SDM: 2 to 1 (e.g. 8 mil space to 4 mil trace) SDQS: 3 to 1 (e.g. 12 mil space to 4 mil space)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	700 mils +/- 300 mils (see package length Table 48 for exact lengths.)
Stub Length S1	Max = 0.10 inches
L1	Min = 0.25 inches (See Figure 59 and Figure 60) Max = 2.5 inches
L2	Max = 0.75 inches (See Figure 59 and Figure 60)
L3	Max = 1.25 inches (See Figure 59 and Figure 60)
L4	Max = 0.25 inches(See Figure 59 and Figure 60)
L5	Max = 1.25 inches (See Figure 59 and Figure 60)
L6	Max = 0.05 inches (See Figure 60)
Max Length: L1+L2+L3+L4+L5 (see Figure 59) L1+L2+L3+L4+L5+L6 (see Figure 60)	Max = 4.25 inches

NOTES:
1. Power distribution vias from Rt to Vtt are not included in this count.
2. The overall minimum and maximum length to the Micro-DIMM and Memory Down must comply with clock length matching requirements.

7.3.4.2. SDQS to Clock Length Matching Requirements

The first step in length matching is to determine the SDQS length range based on the SCK/SCK# reference length defined previously. The total length of the SDQS strobe signals, including package length, between the GMCH die-pad and the Micro-DIMM/Memory Down device must fall within the range defined in the formulas below. See the clock Section for the definition of the clock reference length. Refer to Figure 59 and Figure 60 for the definition of the various trace segments. The length tuning requirements are also depicted in Figure 62. Refer to Section 7.1 for more details on length matching and length formula requirements.

Length range formula for Micro-DIMM:

X_0 = SCK/SCK#[1:0] total reference length, including package length

Y_0 = SDQS[7:0] total length = GMCH package(P1) + L1 + S1, see Figure 59 and Figure 60,

where: $(X_0 - 2.0") \le Y_0 \le (X_0 + 0.5")$

Length range formulas for Memory Down,

X_1 = SCK/SCK#[4:3] total reference length, including package length

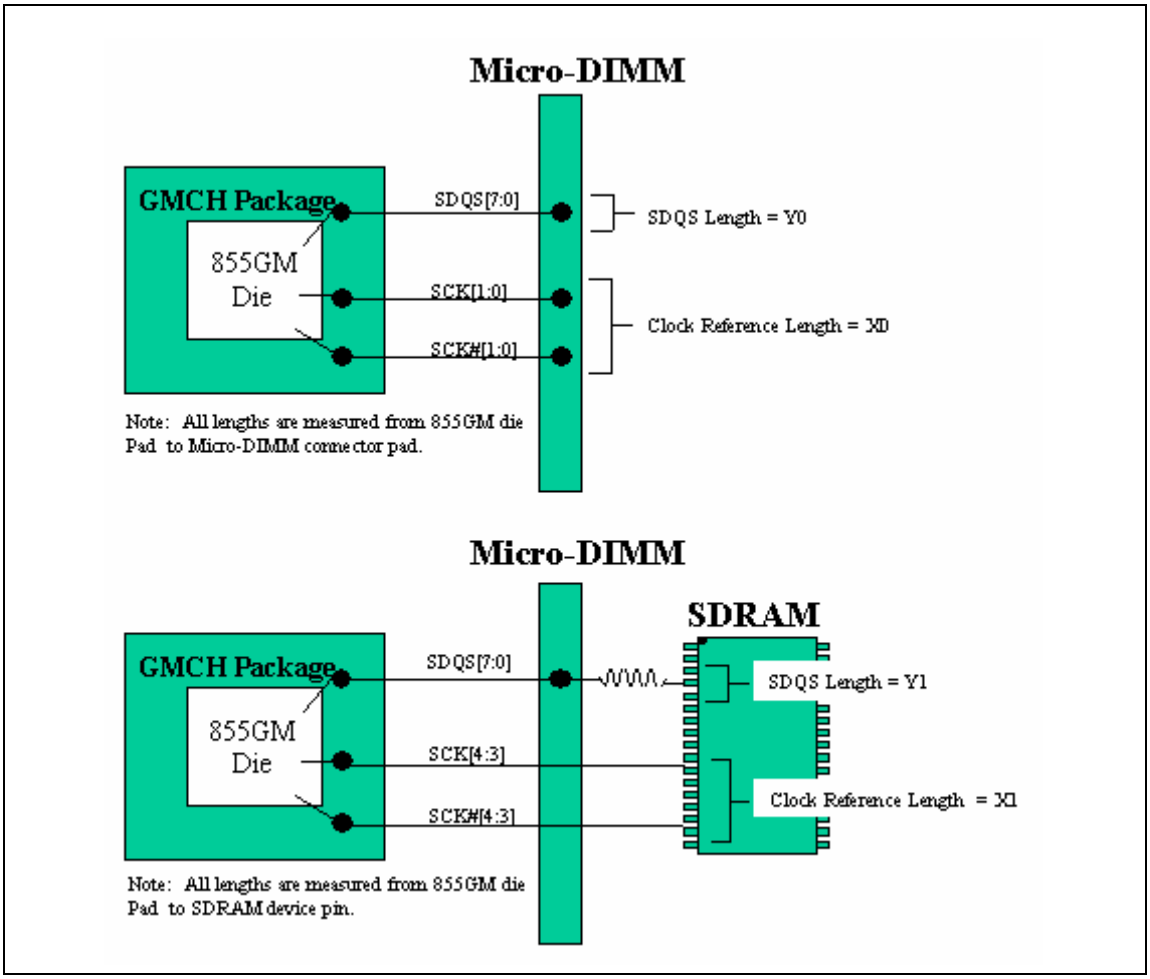
Y_1 = SDQS[7:0] total length = GMCH package(P1) + L1 + L2 + L4 + L5, see Figure 59,

= SDQS[7:0] total length = GMCH package(P1) + L1 + L2 + L4 + L5 + L6, see Figure 60,

where: $(X_1 - 2.0") \le Y_1 \le (X_1 + 0.5")$

Length matching is only performed from the GMCH to the Micro-DIMM or memory down devices, and does not involve the length of L3, which can vary over its entire range. Note that a nominal SDQS package length of 750 mils can be used to estimate motherboard lengths prior to performing package length compensation. Refer to Section 7.2 for more details on package length compensation.

Figure 61. SDQS to Clock Trace Length Matching Diagram



7.3.4.3. Data to Strobe Length Matching Requirements

The data bit signals, SDQ[63:0] are grouped by byte lanes and associated with a data mask signal SDM[8:0], and a data strobe, SDQS[8:0].

- The data and mask signals must be length matched to their associated strobe within ± 25 mils, including package.
- For the Micro-DIMM this length matching includes the motherboard trace length to the pads of the Micro-DIMM connector (L1+S1) plus package length.
- For Memory Down, the motherboard trace length to the pads of the SDRAM device (L1 + L2 + L4 + L5 + L6 for the 2x16 BGA case) plus package length.

Refer to Section 0 for more details on package length compensation.

Length range formula for SDQ and SDM,

X = SDQS total length, including package length, as defined previously

Y = SDQ, SDM total length, including package length, within same byte lane as shown in Figure 62,

where: (X – 25 mils) ≤ Y ≤ (X + 25 mils)

Length matching is not required for length L3 to the parallel termination resistors. Figure 62 on the following page depicts the length matching requirements between the SDQ, SDM, and SDQS signals within a byte lane. Byte lane mapping is defined in Table 47 below.

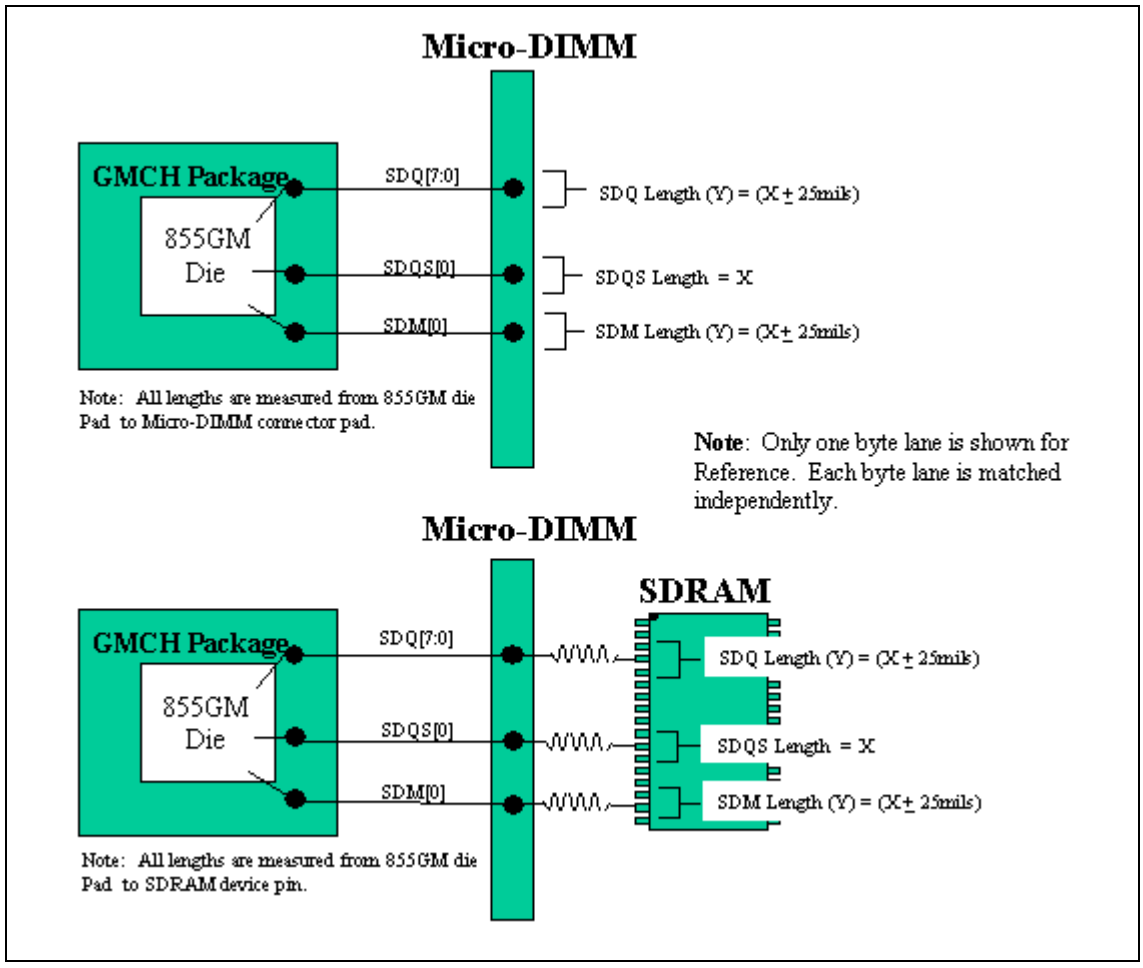
7.3.4.4. SDQ to SDQS Mapping

Table 47 below defines the mapping between the eight byte lanes, 8mask bits, and the 8 SDQS signals, as required to do the required length matching.

Table 47. SDQ/SDM to SDQS Mapping

Signal	Mask	Relative To
SDQ[7:0]	SDM[0]	SDQS[0]
SDQ[15:8]	SDM[1]	SDQS[1]
SDQ[23:16]	SDM[2]	SDQS[2]
SDQ[31:24]	SDM[3]	SDQS[3]
SDQ[39:32]	SDM[4]	SDQS[4]
SDQ[56:40]	SDM[5]	SDQS[5]
SDQ[55:48]	SDM[6]	SDQS[6]
SDQ[63:56]	SDM[7]	SDQS[7]

Figure 62. SDQ/SDM to SDQS Trace Length Matching Diagram



7.3.4.5. SDQ/SDQS Signal Package Lengths

The package length data in Table 48 below should be used to tune the length of each SDQ, SDM, and SDQS motherboard trace as required to achieve the overall length matching requirements defined in the prior Sections.

Table 48. DDR SDQ/SDM/SDQS Package Lengths

Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
SDQ_00	AF2	785	SDQ_32	AH16	766
SDQ_01	AE3	751	SDQ_33	AG17	558
SDQ_02	AF4	690	SDQ_34	AF19	510
SDQ_03	AH2	903	SDQ_35	AE20	579
SDQ_04	AD3	682	SDQ_36	AD18	408
SDQ_05	AE2	739	SDQ_37	AE18	458
SDQ_06	AG4	741	SDQ_38	AH18	658
SDQ_07	AH3	845	SDQ_39	AG19	596
SDQ_08	AD6	607	SDQ_40	AH20	677
SDQ_09	AG5	756	SDQ_41	AG20	730
SDQ_10	AG7	685	SDQ_42	AF22	562
SDQ_11	AE8	558	SDQ_43	AH22	702
SDQ_12	AF5	734	SDQ_44	AF20	563
SDQ_13	AH4	825	SDQ_45	AH19	644
SDQ_14	AF7	644	SDQ_46	AH21	716
SDQ_15	AH6	912	SDQ_47	AG22	783
SDQ_16	AF8	622	SDQ_48	AE23	592
SDQ_17	AG8	624	SDQ_49	AH23	752
SDQ_18	AH9	676	SDQ_50	AE24	666
SDQ_19	AG10	634	SDQ_51	AH25	817
SDQ_20	AH7	710	SDQ_52	AG23	639
SDQ_21	AD9	508	SDQ_53	AF23	667
SDQ_22	AF10	569	SDQ_54	AF25	707
SDQ_23	AE11	469	SDQ_55	AG25	783
SDQ_24	AH10	648	SDQ_56	AH26	834
SDQ_25	AH11	622	SDQ_57	AE26	701
SDQ_26	AG13	572	SDQ_58	AG28	808

Signal	Pin Number	Pkg Length (mils)	Signal	Pin Number	Pkg Length (mils)
SDQ_27	AF14	655	SDQ_59	AF28	756
SDQ_28	AG11	599	SDQ_60	AG26	782
SDQ_29	AD12	460	SDQ_61	AF26	748
SDQ_30	AF13	536	SDQ_62	AE27	673
SDQ_31	AH13	642	SDQ_63	AD27	608
SDQ_64	AG14	566	SDQS_0	AG2	925
SDQ_65	AE14	477	SDQS_1	AH5	838
SDQ_66	AE17	571	SDQS_2	AH8	756
SDQ_67	AG16	530	SDQS_3	AE12	466
SDQ_68	AH14	701	SDQS_4	AH17	678
SDQ_69	AE15	421	SDQS_5	AE21	487
SDQ_70	AF16	491	SDQS_6	AH24	770
SDQ_71	AF17	530	SDQS_7	AH27	858
			SDQS_8	AD15	418
SDM_0	AE5	838			
SDM_1	AE6	693			
SDM_2	AE9	538			
SDM_3	AH12	606			
SDM_4	AD19	492			
SDM_5	AD21	470			
SDM_6	AD24	557			
SDM_7	AH28	917			
SDM_8	AH15	685			

7.3.5. Control Signals – SCKE[3:0], SCS#[3:0]

The Montara-GM GMCH chipset control signals, SCKE[3:0] and SCS#[3:0], are clocked into the DDR SDRAM devices using clock signals SCK/SCK#[4,3,1,0]. The GMCH drives the control and clock signals together, with the clocks crossing in the valid control window. The GMCH provides one chip select (CS) and one clock enable (CKE) signal per Micro-DIMM physical device row. Two chip select and two clock enable signals will be routed to the Miro-DIMM. The remaining SCKE and CS# signals can be routed to the memory down device configuration that the developer has chosen. Should the memory down configuration contain one bank of memory SCKE[3] and SCS#[3] should be left as no connects. Refer to Table 49 for the CKE and CS# signal to Micro-DIMM or Memory Down mapping.

Table 49. Control Signal to Micro-DIMM/Memory Down Mapping

Signal	Relative To	SOPin
SCS#[0]	Micro-DIMM	Micro-DIMM Pin 95
SCS#[1]	Micro-DIMM	Micro-DIMM Pin 96
SCS#[2]	Mem Down – Bank 1	Mem Device CS#
SCS#[3]	Mem Down – Bank 2	Mem Device CS#
SCKE[0]	Micro-DIMM	Micro-DIMM Pin 72
SCKE[1]	Micro-DIMM	Micro-DIMM Pin 71
SCKE[2]	Mem Down – Bank 1	Mem Device CKE#
SCKE[3]	Mem Down – Bank 2	Mem Device CKE#

The following is an example layout description based on layout studies on an 8-layer board. The Control signals should transition from an external layer to an internal signal layer (L1) under the GMCH. If the signal is going to the Micro-DIMM connector, route the signal on the internal layer and via to the external layer and connect to the appropriate pad on the connector (S1). If the signal is going to the SDRAMs, route the signal on the internal layer until transitioning back to an external layer at the parallel termination (L2). When it is close to the SDRAMs, the signal should via to another internal layer and split into two traces (TL0). Each trace routes to the middle region of the SDRAM (TL1) and via to the external layer. Depending on the number of devices for memory down, the Control signal can be routed on the surface (TL2) to the ball or pad of one SDRAM or two SDRAMs. If 8 BGAs, the signal will continue on from the via on an internal layer (TL2 on 8 BGA devices topology) and go to the center region of the outer-most SDRAM then via to the external layer. Depending on the number of devices for memory down, the Control signal can be routed on the surface (TL3 on 8 BGA devices topology) to the ball or pad of one SDRAM device (4 TSOP SDRAMs) or two SDRAMs (8 BGAs).

External trace lengths should be minimized. All internal and external signals should be ground reference to keep the path of return current continuous. Intel suggests that all control signals be routed on the same internal layer.

Resistor packs are acceptable for the parallel (Rt) control termination resistors, but control signals can't be placed within the same R pack as the data or command signals. Figure 62, Figure 63, Figure 64, & Figure 65 and Table 50 below depicts the recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

7.3.5.1. Control Signal Topology

Figure 63. Control Signal Routing GMCH to Micro-DIMM Pad

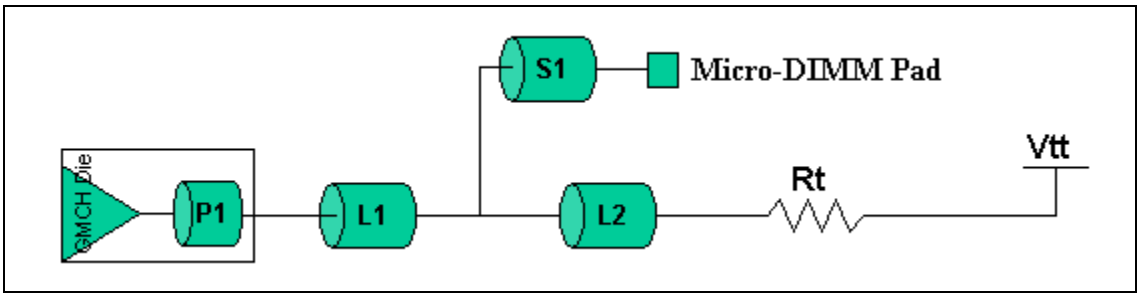


Figure 64. Control Signal Routing GMCH to Memory Down 1x16 4 Load TSOP

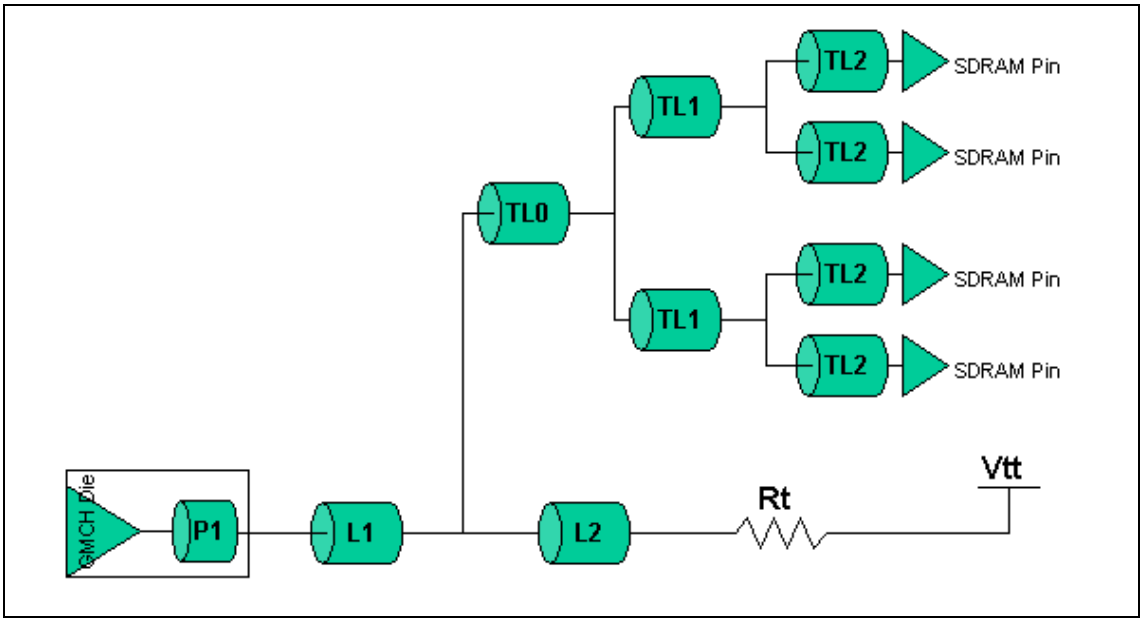


Figure 65. Control Signal Routing GMCH to Memory Down 1x16/2x16 4 Load BGA

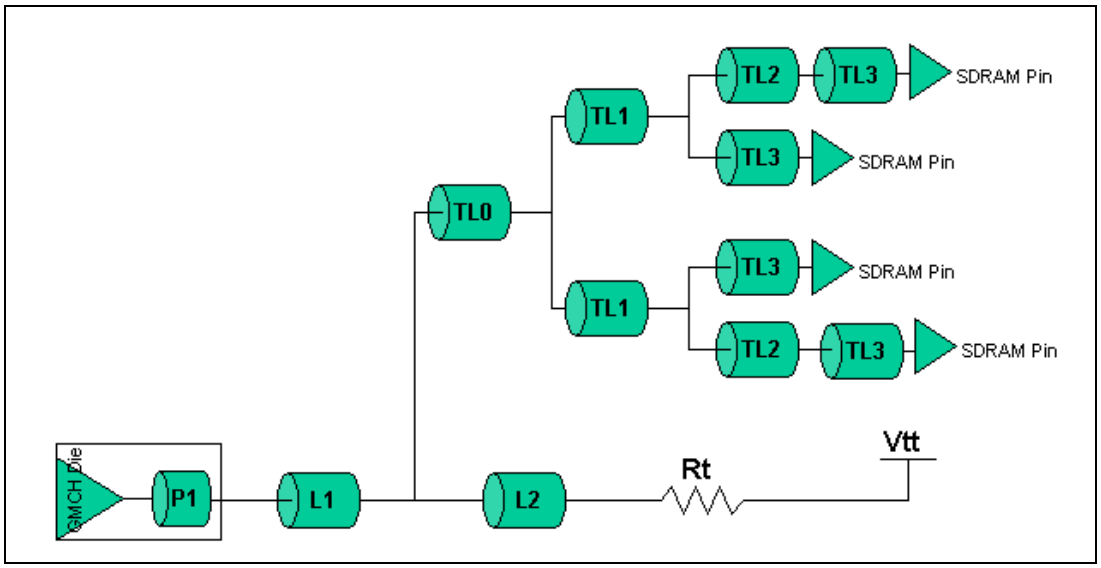
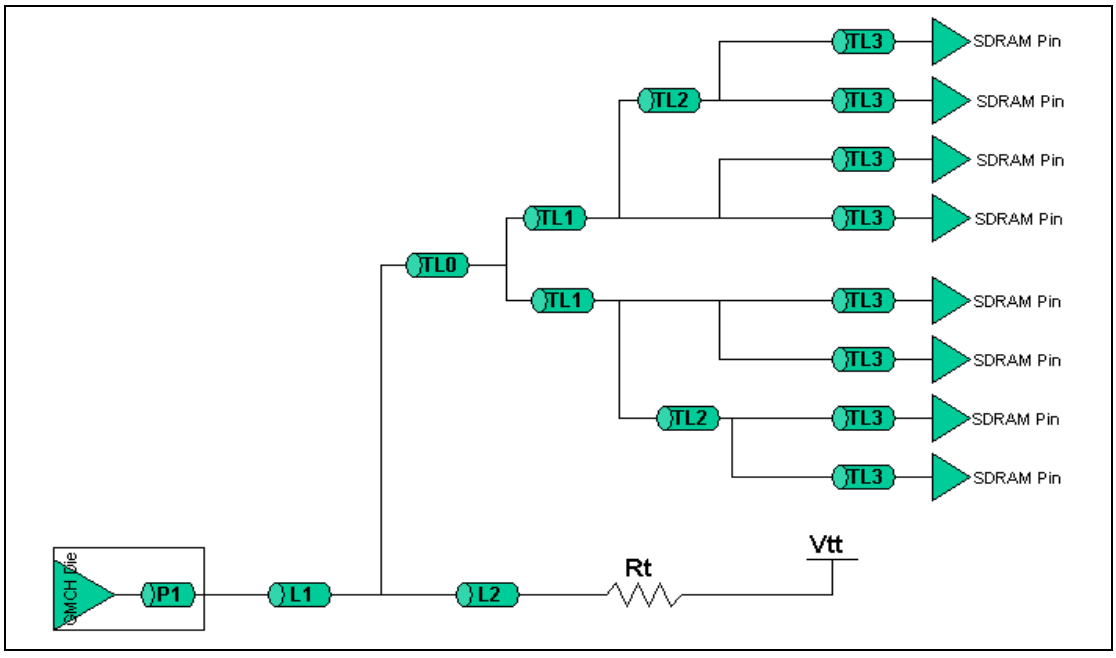


Figure 66. Control Signal Routing GMCH to Memory Down 1x8 8 Loads BGA



The control signals should be routed using 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20-mils of spacing to non-DDR related signals. Control signals should be routed on inner layers with minimized external trace lengths.

7.3.5.2. Control Signal Routing Guidelines

Table 50. Control Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SCKE[3:0], SCS#[3:0]
Motherboard Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils +/- 250 mils (see Table 51 for exact package lengths.)
Stub Length S1	Max = 250 mils
Trace Length L1 – GMCH Control Signal Ball to Micro-DIMM pad	Min = 0.25 inches Max = 4 inches
Trace Length L2 – Micro-DIMM Pad to Parallel Termination Resistor Pad	Max = 2 inches
TL0	Min = 0.5 inches Max = 1.5 inches
TL1	Min = 0.3 inches Max = 0.7 inches
TL2	Min = 100 mils Max = 500 mils (see Figure 64) Min = 0.3 in Max = 0.7 in (see Figure 65) Min = 0.3 in Max = 0.7 in (see Figure 66)
TL3	Min = 100 mils Max = 500 mils (see Figure 65) Min = 0.3 in Max = 0.7 in (see Figure 66)
TL4	Min = 100 mils Max = 500 mils
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	7
Length Matching Requirements	CTRL to SCK/SCK# [4,3,1,0] See length matching Section 7.3.5.3 and Figure 67.

NOTE: The overall maximum and minimum length to the Micro-DIMM must comply with clock length matching requirements.

7.3.5.3. Control to Clock Length Matching Requirements

The length of the control signals, between the GMCH die pad and the Micro-DIMM/Memory Down device must fall within the range defined below, with respect to the associated clock reference length. . Refer to Figure 63, Figure 64, Figure 65, and Figure 66 for a definition of the various trace segments that make up this path. The length of trace from the Micro-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 67. Refer to Section Note: for more details on length matching requirements.

Length range formula for Micro-DIMM:

X_0 = SCK/SCLK#[1:0] total reference length, including package length. See clock Section 7.3.1.

Y_0 = SCS#[1:0] & SCKE[1:0] total length = P1 + L1+ S1, as shown in Figure 63.

where: $(X_0 – 2.0”) \le Y_0 \le (X_0 - 0.5”)$

Length range formula for Memory-Down:

X_1 = SCK/SCLK#[4:3] total reference length, including package length. See clock Section 7.3.1.

Y_1 = SCS#[3:2] & SCKE[3:2] total length = P1+L1+TL0+TL1+TL2 , as shown in Figure 64

= SCS#[3:2] & SCKE[3:2] total length = P1+L1+TL0+TL1+TL2+TL3, as shown in Figure 65

= SCS#[3:2] & SCKE[3:2] total length = P1+L1+TL0+TL1+ TL3, as shown in Figure 65

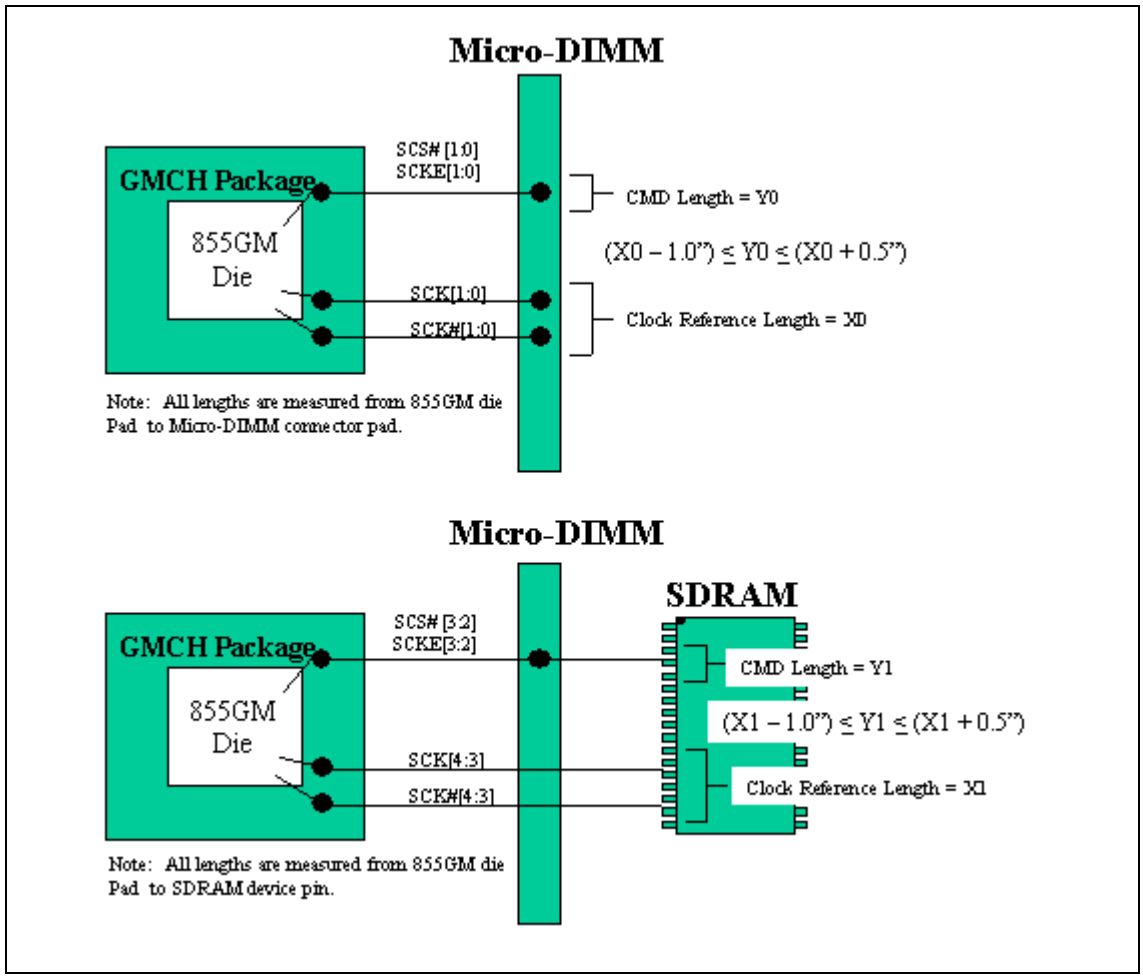
= SCS#[3:2] & SCKE[3:2] total length = P1+L1+TL0+TL1+TL2+TL3+TL4, as shown in Figure 66

= SCS#[3:2] & SCKE[3:2] total length = P1+L1+TL0+TL1+TL3+TL4, as shown in Figure 66,

where: $(X_1 – 1.0”) \le Y_1 \le (X_1 + 0.5”)$

No length matching is required to the termination resistor. Figure 67 on the following page depicts the length matching requirements between the control signals and clock. A nominal CS/CKE package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section Note: for more details on package length compensation.

Figure 67. Control Signal to Clock Trace Length Matching Diagram



7.3.5.4. Control Group Package Length Table

The package length data in Table 51 should be used to match the overall length of each command control signal to its associated clock reference length. Note that due to the relatively small variance in package length and adequate timing margins it is acceptable to use a fixed 500-mil nominal package length for all control signals, thereby reducing the complexity of the motherboard length calculations.

Table 51. Control Group Package Lengths

Signal	Pin Number	Package Length (mils)
SCS#[0]	AD23	502
SCS#[1]	AD26	659
SCS#[2]	AC22	544
SCS#[3]	AC25	612
SCKE[0]	AC7	443
SCKE[1]	AB7	389
SCKE[2]	AC9	386
SCKE[3]	AC10	376

7.3.6. Command Signals – SMAA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#

The Intel 855GM GMCH chipset command signals, SMA[12:0], SBA[1:0], SRAS#, SCAS#, and SWE# clocked into the DDR SDRAMs using the clock signals SCK/SCK#[5:0]. The GMCH drives the command and clock signals together, with the clocks crossing in the valid command window. A series resistor is placed between the Micro-DIMM and Memory Down configuration to dampen the Micro-DIMM to Memory Down resonance.

7.3.6.1. Command Topology

The following is an example layout description based on layout studies on an 8 layer board. The command signal routing should transition from an external layer to an internal signal layer (L1) under the GMCH. At the via transition for the Micro-DIMM connector, the signal should transition to an external layer (S1) and connect to the appropriate pad on the connector. After the Micro-DIMM transition, continue to route the signal on the same internal layer (L2) until transitioning back to an external layer at the series resistor Rs. At the via transition to the Rs resistor, parallel termination resistor may be placed on the other side through the same via (L3). After the series resistor, the signal should transition from the external layer to the same internal layer (TL0) and route until it is near the SDRAMs. Via to another internal layer and split into two traces (TL1). Each trace routes to the middle region of the SDRAM and then via to the external layer. Depending on the number of devices for memory down, the command signal can route on the surface to the ball or pad (TL2) of one SDRAM (4 TSOP SDRAMs memory down) or two SDRAMs (8 BGA SDRAMs, TL4). If 8 BGAs, the signal will continue on from the via on an internal layer (TL3) and go to the outer-most SDRAM. Via to the external layer. Depending on the number of devices for memory down, the command signal can route on the surface (TL4) to the ball or pad of one SDRAM (4 TSOP SDRAMs) or two SDRAM (8 BGAs).

All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors but command signals cannot be placed within the same R-packs as data, strobe, or control signals. Figure 68, Figure 69 and Table 52 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to the Micro-DIMM and Memory Down.

Figure 68. CMD Signal Routing GMCH to Micro-DIMM and Mem Down TSOP 4 Load

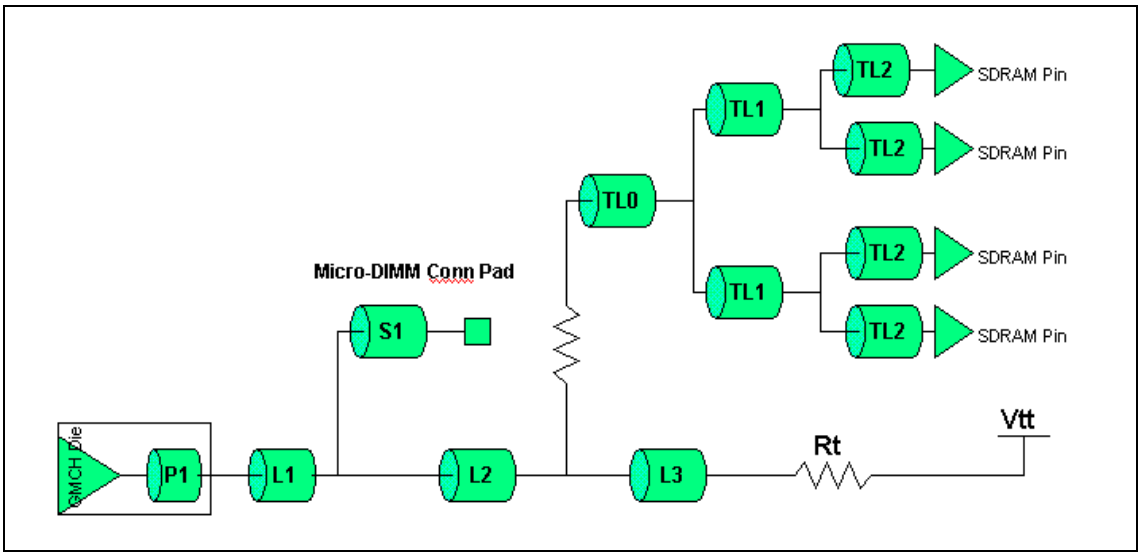


Figure 69. CMD Signal Routing GMCH to Micro-DIMM and Mem Down BGA 4 Load

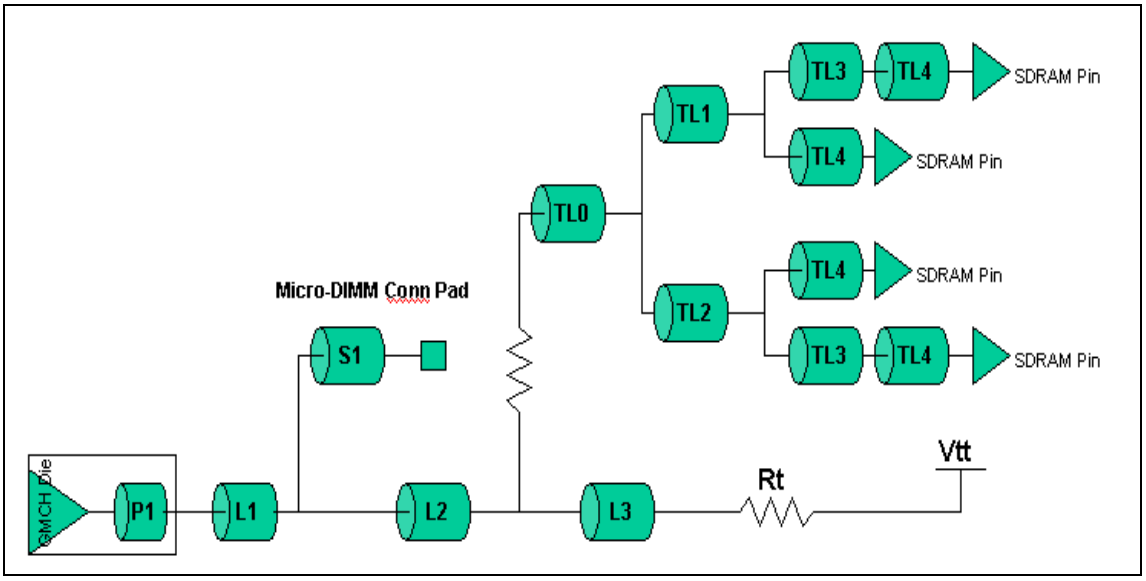
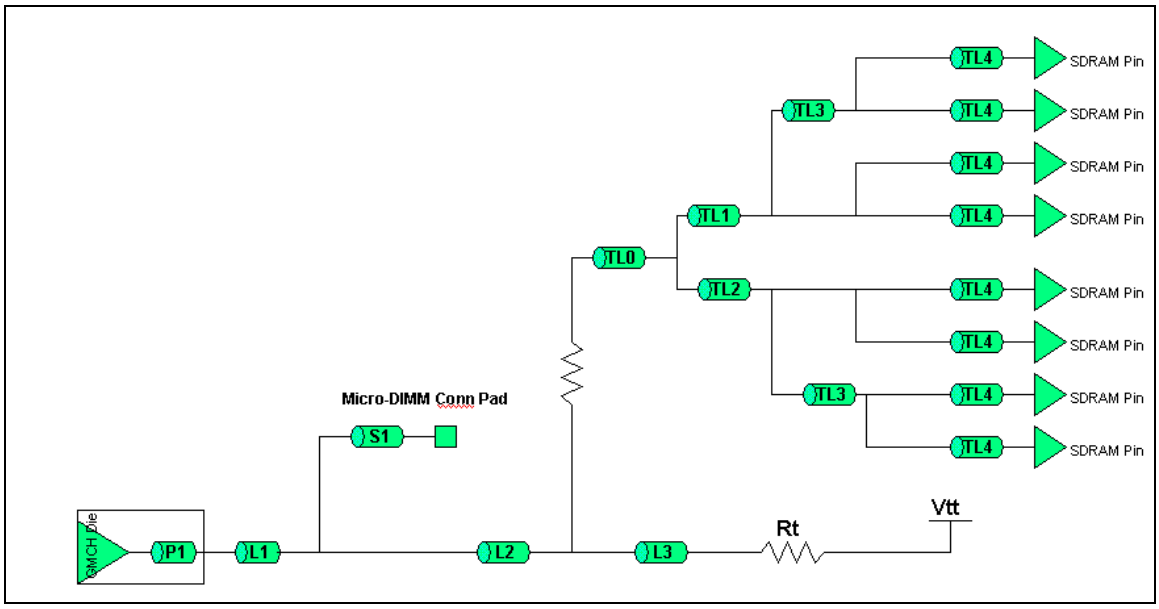


Figure 70. CMD Signal Routing GMCH to Micro-DIMM and Memory Down BGA 8-Load



The command signals should be routed using a 2 to 1 trace spacing to trace width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20 mils spacing to non-DDR related signals. Command signals should be routed on inner layers with minimized external traces.

7.3.6.2. Command Topology Routing Guidelines

Table 52. Command Topology 1 Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#
Motherboard Topology	Daisy Chain with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ± 15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils +/- 250 mils (see Table 53 for exact package lengths.)
Stub Length S1	Max = 0.25 inches
Stub Length S2	Max = 0.25 inches
Trace Length L1	Min = 0.5 inch Max = 4.0 inches
Trace Length L2	Max = 1.0 inches
Trace Length L3	Max = 1.0 inches
Trace Length TL0	Min = 0.5 inches Max = 1.5 inches
Trace Length TL1	Max = 0.5 inches
Trace Length TL2	Max = 0.5 inches
Trace Length TL3	Min = 0.4 inches Max = 0.8 inches
Trace Length TL4	Max = 0.5 inches
Series Termination Resistor (Rs)	10 Ω ± 5%
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	18
Length Matching Requirements	CMD to SCK/SCK# [5:0] See length matching Section 7.3.6.3 and Figure 71 for details.

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the Micro-DIMM and Memory Down must comply with clock length matching requirements.

7.3.6.3. Command Topology Length Matching Requirements

The routing length of the command signals between the GMCH die pad and Micro-DIMM/Memory Down must be within the range defined below. This is with respect to the associated clock reference length. Refer to Figure 43 for a definition of the various motherboard trace segments. The length of trace from the Micro-DIMM to the termination resistor need not be length matched. The length matching requirements are also depicted in Figure 71 Refer to Section 7.1 for more details on length matching requirements.

Length range formula for Micro-DIMM:

X0 = SCK/SCLK#[1:0] total reference length, including package length (P1). See clock Section 7.3.1.

Y0 = CMD signal total length = P1 + L1+ S1, as shown in Figure 68, Figure 69, and Figure 70

where: $(X_0 - 2.0") \le Y_0 \le (X_0 + 2.0")$

Length range formula for Memory-Down:

X1 = SCK/SCLK#[4:3] total reference length, including package length (P1). See clock section 7.3.1.

Y1 = CMD signal total length = P1 + L1 + L2 + TL0 + TL1 + TL2, as shown in Figure 68

= CMD signal total length = P1 + L1 + L2 + TL0 + TL1 + TL3 +TL4, as shown in Figure 69 & Figure 70

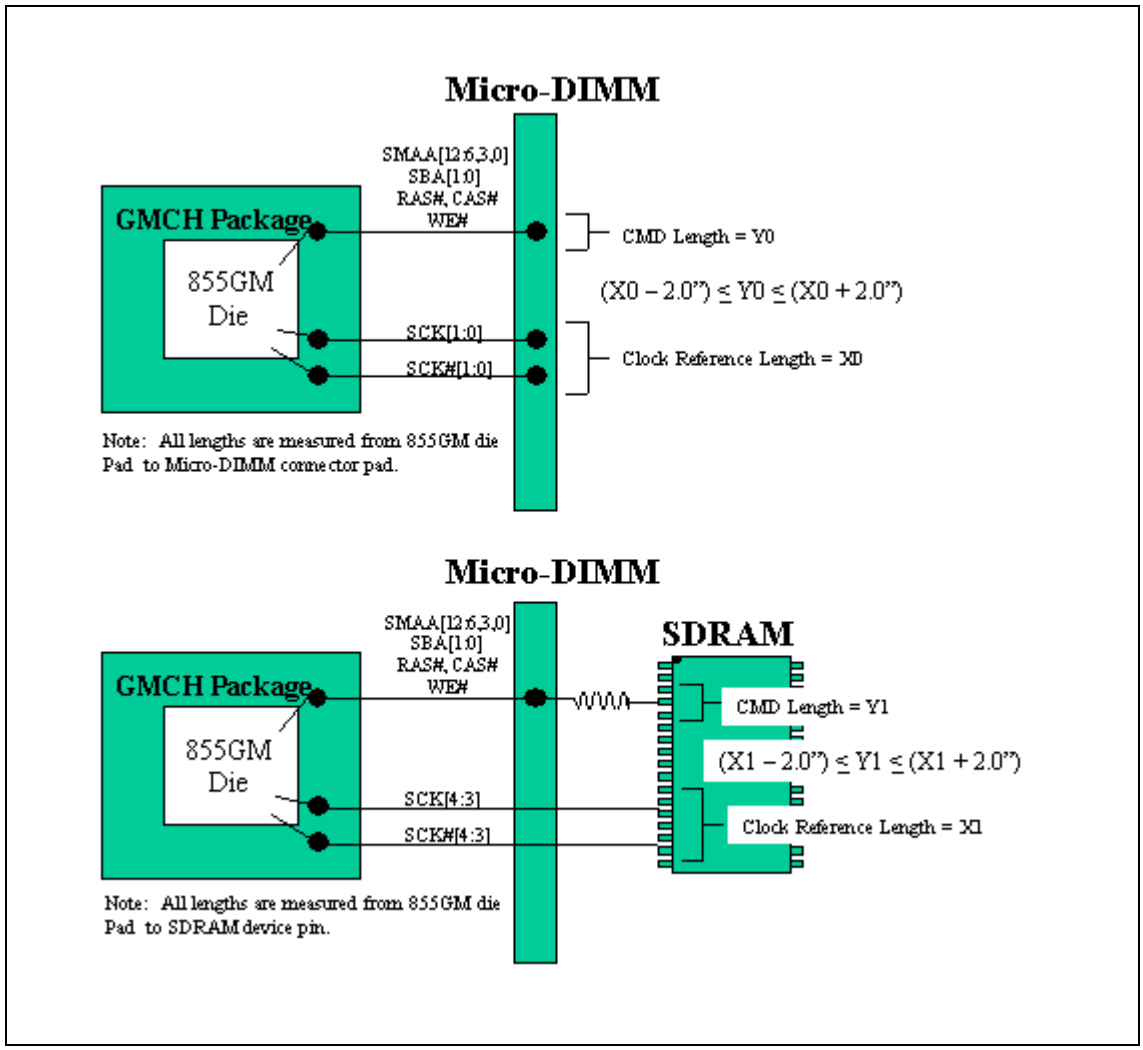
= CMD signal total length = P1 + L1 + L2 + TL0 + TL1 + TL4, as shown in Figure 69 & Figure 70

= CMD signal total length = P1 + L1 + L2 + TL0 + TL2 + TL4, as shown in Figure 69 & Figure 70

= CMD signal total length = P1 + L1 + L2 + TL0 + TL2 + TL3 + TL4, as shown in Figure 69 & Figure 70 where: $(X_1 - 2.0") \le Y_1 \le (X_1 + 2.0")$

No length matching is required from Rs to the termination resistor. Figure 71 on the following page depicts the length matching requirements between the command signals and clock. A nominal CMD package length of 500 mils can be used to estimate baseline MB lengths. Refer to Note: for more details on package length compensation.

Figure 71. Topology 1 Command Signal to Clock Trace Length Matching Diagram



7.3.6.4. Command Group Package Length Table

The package length data in Table 53 below should be used to match the overall length of each command signal to its associated clock reference length.

Table 53. Command Group Package Lengths

Signal	Pin Number	Pkg Length (mils)
SMAA_00	AC18	420
SMAA_03	AD17	472
SMAA_06	AD8	591
SMAA_07	AD7	596
SMAA_08	AC6	630
SMAA_09	AC5	681
SMAA_10	AC19	377
SMAA_11	AD5	683
SMAA_12	AB5	609
SBA[0]	AD22	592
SBA[1]	AD20	435
SCAS#	AC24	562
SRAS#	AC21	499
SWE#	AD25	751

7.3.7. CPC Signals – SMA[5,4,2,1], SMAB[5,4,2,1]

The GMCH drives the CPC and clock signals together, with the clocks crossing in the valid control window. The GMCH provides one set of CPC signals for the Micro-DIMM slot and one set for the Memory Down configuration.

Refer to Table 49 for the CKE and CS# signal to Micro-DIMM mapping.

Table 54. CPC Signal to SO-DIMM Micro-Dimm and/or Memory Down Mapping

Signal	Relative To	Pin
SMA[1]	Micro-DIMM	Micro-DIMM pad #85
SMA[2]	Micro-DIMM	Micro-DIMM pad #84
SMA[4]	Micro-DIMM	Micro-DIMM pad #82
SMA[5]	Micro-DIMM	Micro-DIMM pad #81
SMAB[1]	Mem Down	Mem Device Pin
SMAB[2]	Mem Down	Mem Device Pin
SMAB[4]	Mem Down	Mem Device Pin
SMAB[5]	Mem Down	Mem Device Pin

The following is an example layout description based on layout studies on an 8-layer board. The CPC signals should transition from an external layer to an internal signal layer (L1) under the GMCH. If the signal is going to the Micro-DIMM connector, route the signal on the internal layer and via to the external layer and connect to the appropriate pad on the connector (S1). If the signal is going to the SDRAMs, route the signal on the internal layer until transitioning back to an external layer at the parallel termination (L2). When it is close to the SDRAMs, the signal should via to another internal layer and split into two traces (TL0). Each trace routes to the middle region of the SDRAM (TL1) and via to the external layer. Depending on the number of devices for memory down, the CPC signal can be routed on the surface (TL2) to the ball or pad of one SDRAM or two SDRAMs. If 8 BGAs, the signal will continue on from the via on an internal layer (TL2 on 8 BGA devices topology) and go to the center region of the outer-most SDRAM then via to the external layer. Depending on the number of devices for memory down, the CPC signal can be routed on the surface (TL3 on 8 BGA devices topology) to the ball or pad of one SDRAM device (4 TSOP SDRAMs) or two SDRAMs (8 BGAs).

External trace lengths should be minimized. All internal and external signals should be ground reference to keep the path of return current continuous. Intel suggests that all control signals be routed on the same internal layer.

Resistor packs are acceptable for the parallel (Rt) control termination resistors, but control signals cannot be placed within the same R pack as the data or command signals. Figure 74, Figure 75, Figure 76, and Table 55 below depict the recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

7.3.7.1. CPC Signal Topology

Figure 72. Command Per Clock Signal Routing Topology 4 Load BGA

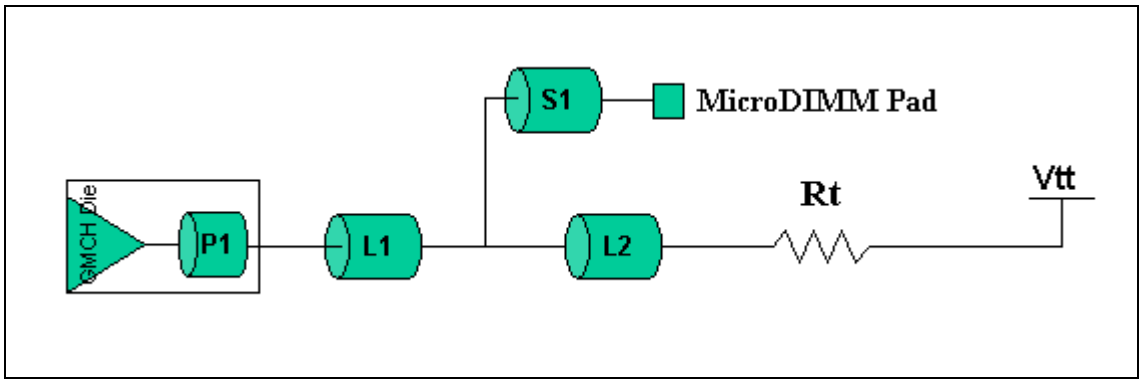


Figure 73. CPC Signal Routing Topology 4 Load TSOP

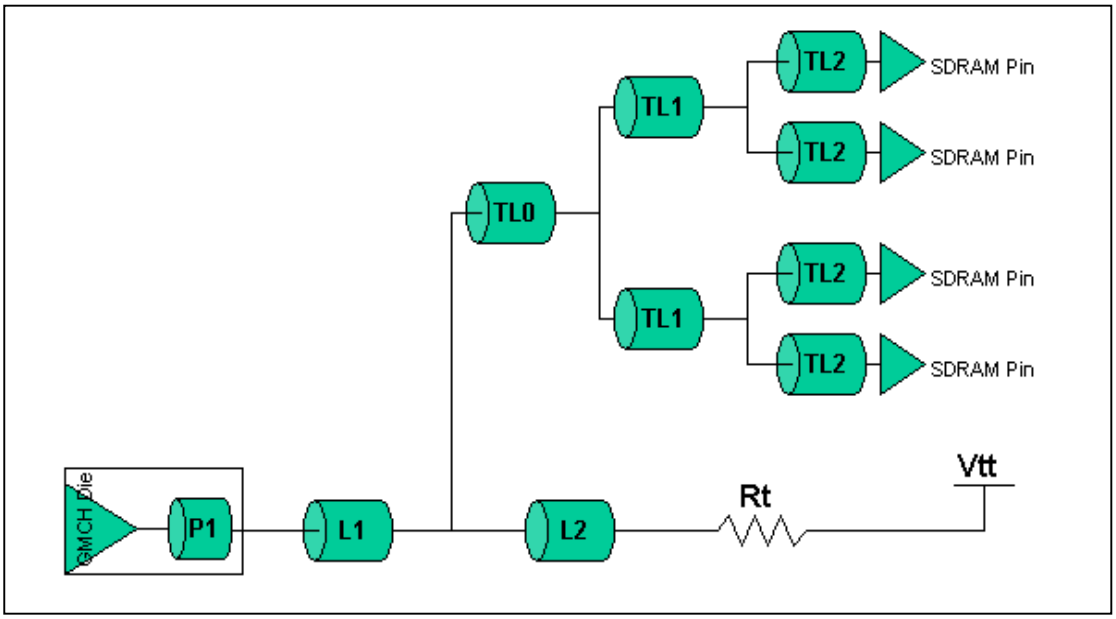


Figure 74. CPC Signal Routing 8 Load BGA Topology

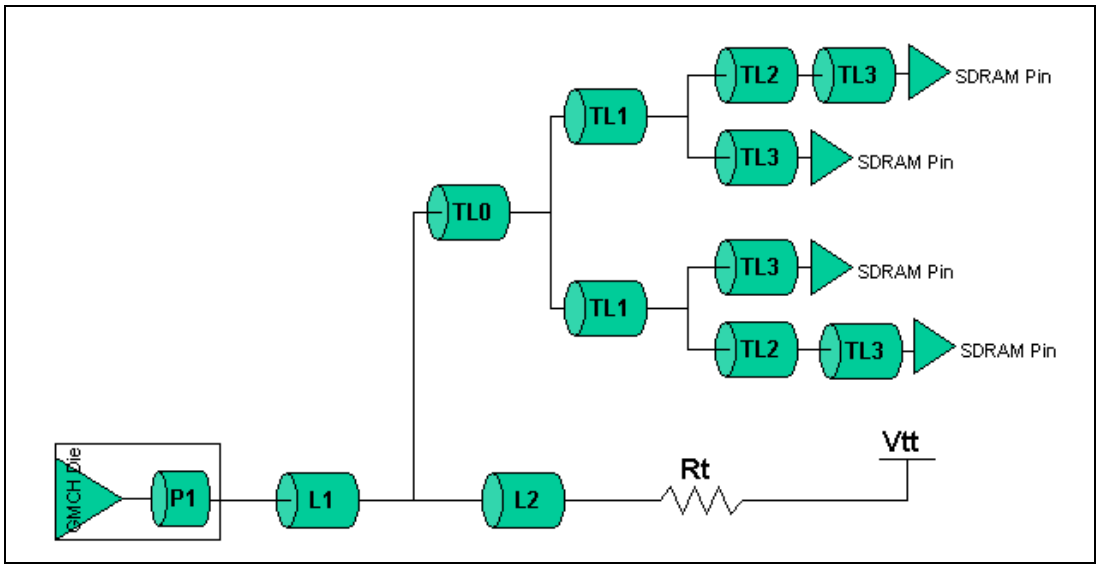
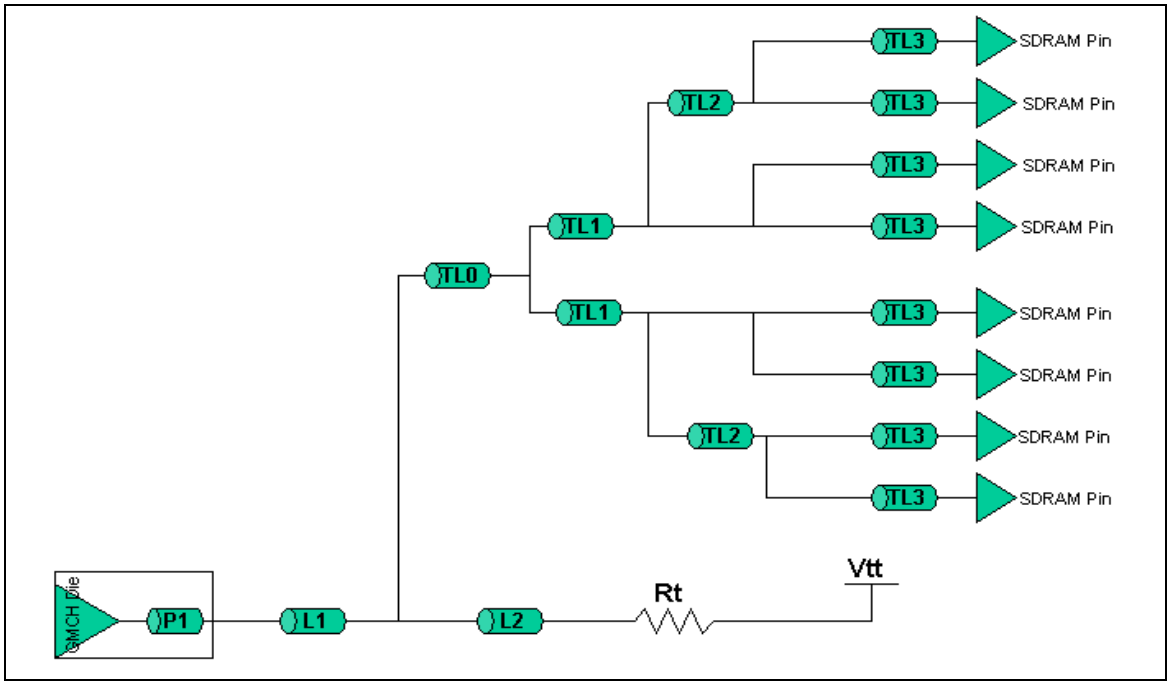


Figure 75. CPC Signal Routing Micro-DIMM



The CPC signals should be routed using 2 to 1 trace space to width ratio for signals within the DDR group, except clocks and strobes. There should be a minimum of 20-mils of spacing to non-DDR related signals. CPC signals should be routed on inner layers with minimized external trace lengths.

7.3.7.2. CPC Signal Routing Guidelines

Table 55. CPC Signal Routing Guidelines

Parameter	Routing Guidelines
Signal Group	SMA[5,4,2,1], SMAB[5,4,2,1]
Motherboard Topology	Point-to-Point with Parallel Termination
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ±15%
Nominal Trace Width	Inner layers: 4 mils Outer layers: 5 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DDR Signals	20 mils
Package Length P1	500 mils +/- 250 mils (see Table 56 for exact package lengths.)
Trace Length S1 – Stub Length to Micro-DIMM Connector	Max = 0.25”
Trace Length L1 – GMCH Control Signal Ball to Micro-DIMM Pad	Min = 0.25 inches Max = 4.0 inches
Trace Length L2 – Micro-DIMM Pad to Parallel Termination Resistor Pad	Max = 2.0 inches
Trace Length TL0	Min = 0.25 inches Max = 1.5 inches
Trace Length TL1	Min = 0.3 inches Max = 0.7 inches
Trace Length TL2	Min = 0.3 in Max = 0.7 in (see Figure 74 and Figure 75) Min = 0.1 in Max = 0.5 in (see Figure 73)
Trace Length TL3	Min = 0.1 inches Max = 0.5 inches
Parallel Termination Resistor (Rt)	56 Ω ± 5%
Maximum Recommended Motherboard Via Count Per Signal	14
Length Matching Requirements	CPC to SCK/SCK# [5:0] See length matching Section 7.3.7.3 and Figure 76 for details.

NOTES:
1. Variance per topology for TL1, TL2, and TL3 ± 10 mils.

7.3.7.3. CPC to Clock Length Matching Requirements

The total length of the CPC signals, between the GMCH die pad and the Micro-DIMM/Memory Down device must fall within the range defined below, with respect to the associated clock reference length. Refer to Figure 72, Figure 73, Figure 74, and Figure 75 for a definition of the various trace segments. The trace length from the Micro-DIMM to the termination resistor does not need to be length matched. The length matching requirements are also depicted in Figure 76. Refer to Section 7.1 for more details on length matching requirements. A table of CPC signal package length is provided in Section 7.3.7.4.

Length range formula for Micro-DIMM:

$\mathbf{X_0}$ = SCK/SCK#[1:0] total reference length, including package length. See Section 7.3.3.1

$\mathbf{Y_0}$ = SMA[5,4,2,1] total length = P1 + L1+ S1, see Figure 72

where: $(X_0 - 1.0") \le Y_0 \le (X_0 + 0.5")$

Length range formula for Memory Down:

$\mathbf{X_1}$ = SCK/SCK#[4:3] total reference length, including package length. See Section 7.3.3.1.

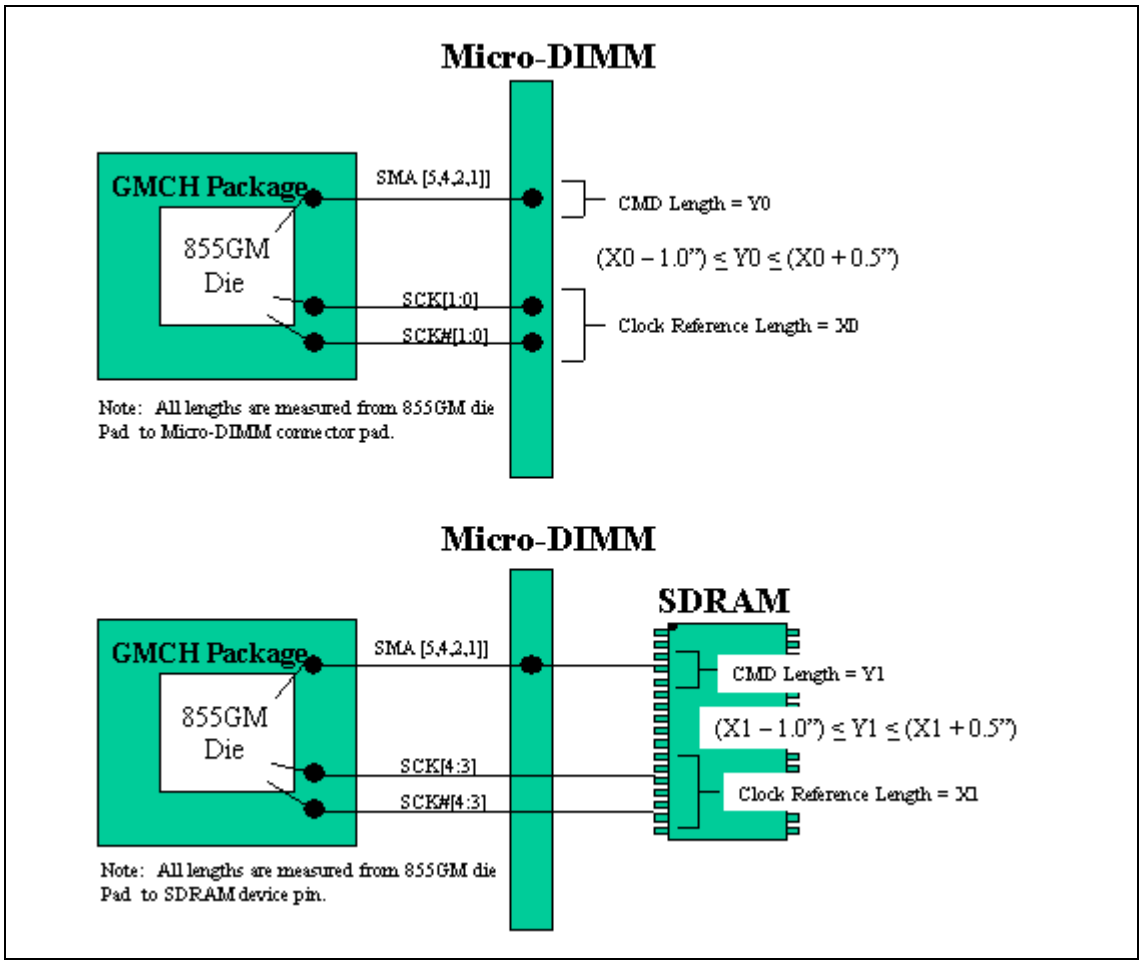
$\mathbf{Y_1}$ = SMAB[5,4,2,1] total length = P1 + L1 + TL0 + TL1 + TL2, see Figure 73

= SMAB[5,4,2,1] total length = P1 + L1 + TL0 + TL1 + TL2 + TL3, see Figure 74, and Figure 75
= SMAB[5,4,2,1] total length = P1 + L1 + TL0 + TL1 + TL3, see Figure 74, and Figure 75

where: $(X_1 - 1.0") \le Y_1 \le (X_1 + 0.5")$

No length matching is required to the termination resistor. Figure 76on the following page depicts the length matching requirements between the CPC signals and clock. A nominal CPC package length of 500 mils can be used to estimate baseline MB lengths. Refer to Section 7.2 for more details on package length compensation.

Figure 76. CPC Signals to Clock Length Matching Diagram



7.3.7.4. CPC Group Package Length Table

The package length data in the table below should be used to match the overall length of each CPC signal to its associated clock reference length.

Table 56. CPC Group Package Lengths

Signal	Pin Number	Pkg Length (mils)
SMAA_01	AD14	398
SMAA_02	AD13	443
SMAA_04	AD11	430
SMAA_05	AC13	346
SMAB_01	AD16	427
SMAB_02	AC12	395
SMAB_04	AF11	716
SMAB_05	AD10	631

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8. Integrated Graphics Display Port

The GMCH contains four display ports: an analog CRT port, a dedicated LVDS port, and two 12-bit Digital Video Out (DVO) ports. Section 8.1 will discuss the CRT and RAMDAC routing requirements. Section 8.2 will discuss the dedicated LVDS port. Section 0 will discuss the DVOB and DVOC design guideline. Section 8.3.4 provides recommendations for a flexible modular design guideline for DVOB and DVOC muxed interfaces. Section 8.5 provides recommendations for the GPIO signal group.

8.1. Analog RGB/CRT Guidelines

8.1.1. RAMDAC/Display Interface

The GMCH integrated graphics/chipset design interfaces to an analog display via a RAMDAC. The RAMDAC is a subsection of the graphics controller display engine and consists of three identical 8-bit digital-to-analog converter (DAC) channels, one for the display's red, green, and blue electron guns.

Each RGB output is doubly terminated with a 75-Ω resistance: One 75-Ω resistance is connected from the DAC output to the board ground, and the other termination resistance exists within the display. The equivalent DC resistance at the output of each DAC is 37.5 Ω. The current output from each DAC flows into this equivalent resistive load to produce a video voltage, without the need for external buffering. There is also a pi-filter on each channel that is used to reduce high-frequency noise and to reduce EMI. In order to maximize the performance, the filter impedance, cable impedance, and load impedance should be matched.

Since the DAC operates at pixel frequencies up to 350 MHz, special attention should be paid to signal integrity and EMI. RGB routing, component placement, component selection, cable and load impedance (monitor) all play a large role in the analog display's quality and robustness. This holds true for all resolutions, but especially for those at 1600x1200 resolutions or higher.

8.1.2. Reference Resistor (REFSET)

A reference resistor, Rset, is used to set the reference current for the DAC. This resistor is an external resistor with a 1% tolerance that is placed on the circuit board. A reference resistor can be selected from a range between 124 Ω to 137 Ω (1%). Based on board design, DAC RGB outputs may be measured when the display is completely white. If the RGB voltage value is between 665 mV to 770 mV, then the video level is within VESA specification and the resistor value that was chosen will be optimal for board design.

A reference voltage is generated on the GMCH from a bandgap voltage reference circuit. The bandgap reference voltage level is approximately 1.2 V and this voltage is divided by four to generate the reference voltage. The VESA video standard defines the LSB current for each DAC channel. The RAMDAC reference current is designed on-die to be equal to 32LSB. Therefore, the external reference resistor value is defined as:

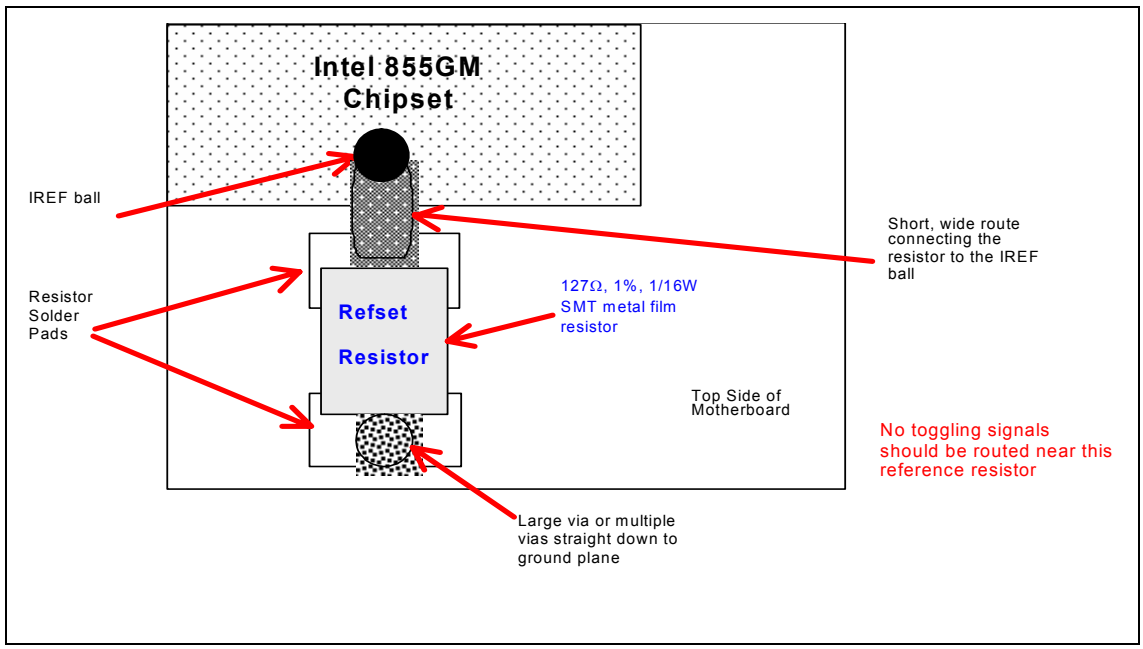
Equation 1.

$$REFSET = \frac{Vreference}{Ireference} = \frac{(Vbg / 4)}{32 * (73.2uA)}$$

A 127 Ω 1% precision resistor value is the recommend value to use. See Figure 77 for the recommended Rset placement.

Note: When using 855GME platform with external graphics only, Rset resistor is not needed.

Figure 77. Refset Placement



8.1.3. RAMDAC Board Design Guidelines

Care should be taken when routing the analog RAMDAC signals. This is especially true to successfully support high display resolution where pixel frequency can be as high as 350 MHz. Intel recommends that each analog R, G, B signal be routed single-endedly. The analog RGB signals should be routed with an impedance of 37.5 Ω. Intel recommends that these routes be routed on an inner routing layer and that it be shielded with VSS planes, if possible. Spacing between DAC channels and to other signals should be maximized; 20-mil spacing is recommended. The RGB signals require pi filters that should be placed near the VGA connector. It consists of two 3.3-pF caps with a 75 Ω ferrite bead at 100-MHz between them. The RGB signals should have a 75-Ω, 1% terminating pull-down resistor. The complement signals (R#, G#, and B#) should be grounded to the ground plane.

Note: When using 855GME platform with external graphics only, the RGB 75-Ω termination resistors are not needed.

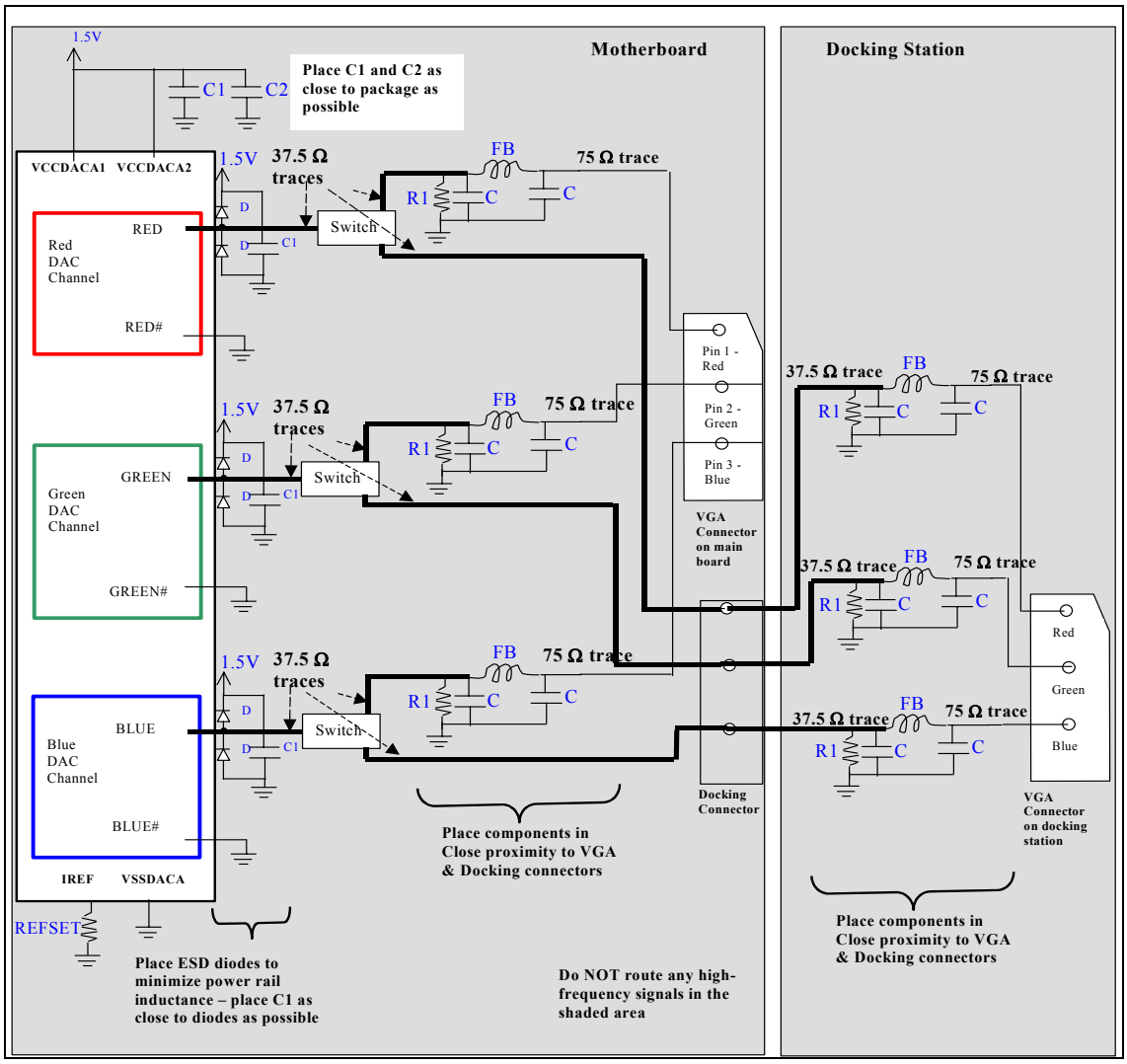
Intel recommends that the pi filter and terminating resistors be placed as close as possible to the VGA connector. After the 75-Ω termination resistor, the RGB signals routing to the pi-filters and the VGA connector *should ideally be routed with 75-Ω impedance (~ 5 mil traces), or as close to* 75-Ω *impedance as possible.*

The RGB signals also require protection diodes between 1.5 V and ground. These diodes should have low C ratings (~5 pF max) and small leakage current (~ 10 µA at 120˚C) and should be properly decoupled with a 0.1-µF cap. These diodes and decoupling should be placed to minimize power rail inductance. The choice between diodes (or diode packs) should comprehend the recommended electrical characteristics in addition to cost.

The RGB signals should be length matched as closely as possible (from the GMCH to the VGA connector) and should not exceed 200 mils of mismatch.

8.1.4. RAMDAC Routing Guidelines

Figure 78. GMCH DAC Routing Guidelines with Docking Connector



The DAC channel (red, green, blue) outputs should be routed as single-ended shielded routes to an analog switch to support a docking station. An analog switch should be used in order to provide the proper termination that is required for high-performance video signal integrity. See Figure 79.

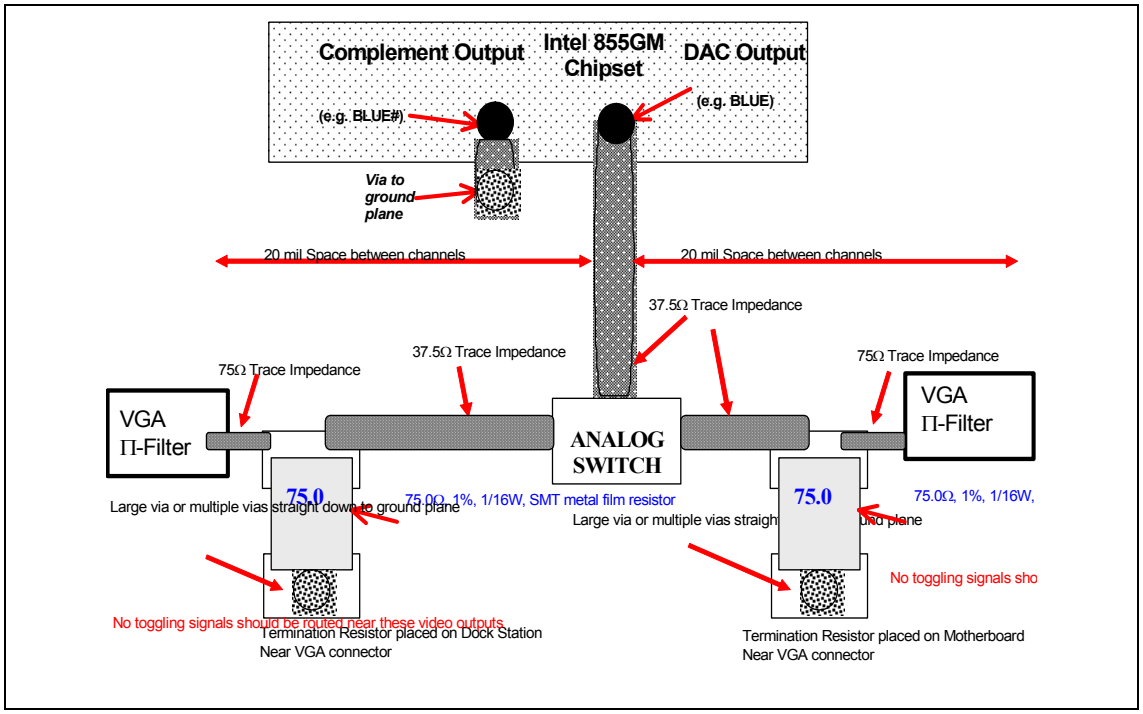
The analog switch should exhibit a low "on" resistance (< 8 Ω) and low parasitic capacitance (<10 pF). The output routing from the analog switch should be routed as single-ended, 37.5-Ω impedance to the 75-Ω termination resistors that are located near the VGA connector on the motherboard and the VGA connector on the docking station. The single-ended routing after these 75-Ω termination resistors to the pi-filter and then to the VGA connector should be ideally 75-Ω. The recommended routing of the termination resistors is shown in Figure 79.

Table 57. Recommended GMCH DAC Components

Recommended DAC Board Components				
Component	**Value**	**Tolerance**	**Power**	**Type**
R1	75.0 Ω	1%	1/16 W	SMT, Metal Film
Refset[1]	127.0 Ω	1%	1/16 W	SMT, Metal Film
C1	0.1 uF	20%	-----	SMT, Ceramic
C2	0.01 uF	20%	-----	SMT, Ceramic
C	3.3 pF	10%	-----	SMT, Ceramic
D	PAC DN006	-------	350 mW	California Micro Devices – ESD diodes for VGA, SOIC package Or equivalent diode array
FB	75 Ω @ 100 MHz	--------	-------	MuRata* BLM11B750S
Analog Switch	-------	-------	Rated for a continuous channel current of 100mA (min)	Ron < 8 Ω, Con < 10 pF Texas Instruments SN74CB3Q3306

NOTE: Not needed when using 855GME platform with external graphics only.

Figure 79. DAC R, G, B Routing and Resistor Layout example



NOTE: The routing to the docking connector is not shown in this figure; however, this routing scheme applies to the docking connector as well.

8.1.5. DAC Power Requirements

The DAC requires a 1.5-V supply through its two VCCADAC balls. The two may share a set of capacitors, 0.1 µF and 0.01 µF, but this connection should have low inductance. Separate analog power or ground planes are not required for the DAC.

However, since the DAC is an analog circuit, it is particularly sensitive to AC noise seen on its power rail. Designs should provide as clean and quiet a supply as possible to the VCCA_DAC. Additional filtering and/or separate voltage rail may be needed to do so. On the Intel CRB, there is a placeholder for a LC filter in case there is noise present in the VCCA power rail.

Video DAC Power Supply DC Specification: 1.50 V ± 5%
Video DAC Power Supply AC Specification:
+/- 0.3% from 0.10 Hz to 10 MHz
+/- 0.95% from 10 MHz to max pixel clock frequency
Absolute minimum voltage at the VCCA package ball = 1.40 V

Please refer to the *latest Intel 855GM/GME (Montara-GM/GM+) Chipset GMCH EDS Addendum* for AC/CD specification.

8.1.6. HSYNC and VSYNC Design Considerations

HSYNC and VSYNC signals are connected to the analog display attached to the VGA connector. These are 3.3-V outputs from the GMCH. Some monitors have been found to drive HSYNC and VSYNC signals during reset. Because these signals are used as straps on the 852GM/GME and 855GM/GME chipsets, the GMCH can enter an illegal state under these conditions. In order to prevent these signals from being driven to the GMCH during reset, system designers must ensure the GMCH is isolated from any monitor driving HSYNC or VSYNC while PCI_RST# is active. Appropriate logic is required between the GMCH and the VGA connector (both the on-board VGA connector and the VGA connector at the docking station) to accomplish this.

Intel's recommended option is to use an analog switch (i.e. discrete FET, Q-buffer) to switch these signals between the on-board VGA connector and the docking connector. In this case, footprints for a series resistor and an optional capacitor are needed on each of these signals to meet the VESA electrical specifications for video signals. Resistor and capacitor values of 39ohm and 33pF respectively are used on the CRB. These values were calculated based on the GMCH buffer strength and board routing. Customers are recommended to perform a signal integrity check specific to their board topology to determine the appropriate resistor and capacitor values for their platforms.

An alternative option is to use a unidirectional buffer on each of these signals. For each of the HSYNC and VSYNC signals, a footprint for a series resistor must be placed between the GMCH and the unidirectional buffer to prevent excessive overshoot and undershoot at the input of the buffer. Consideration should also be taken in designing the filter circuit on the output of these buffers to ensure that the VESA electrical specifications for video signals are met at both the on-board VGA connector as well as on the docking station. Customers are strongly encouraged to perform complete signal integrity validation at the input of the buffer and at the VGA connectors.

8.1.7. DDC and I2C Design Considerations

DDCADATA and DDCACLK are 3.3-V IO buffers connecting the GMCH to the monitor. If higher signaling voltage (5V) is required by the monitor, level shifting devices may be used. Pull-up resistors of 2.2-kΩ (or of the appropriate value derived from simulation) are required on each of these signals.

8.2. LVDS Transmitter Interface

The Intel LVDS (Low Voltage Differential Signaling) transmitter serializer converts up to 24 bits of parallel digital RGB data, (8 bits per RGB), along with up to 4 bits for control (SHFCLK, HSYNC, VSYNC, DE) into 2, 4 channel serial bit streams, for output by the LVDS transmitter.

The transmitter is fully differential and utilizes a current mode drive with a high impedance output. The drive current develops a differential swing in the range of 250 mV to 450 mV across a 100-Ω termination load.

The parallel digital data is serially converted to a 7-bit serial bit stream that is transmitted over the 8 channel LVDS interface at 7x the input clock. The differential output clock channel transmits the output clock at the input clock frequency. While the differential output channels transmit the data at the 7x clock rate (1 bit time is 7x the input clock). The 7x serializer will synchronize and regenerate and input clock from 35 MHz to 112 MHz. Typical operation is at 65 MHz (15.4 ns), therefore, at a 7x clock rate, 1bit time would be 2.2 ns. With data cycle times as small as 2.2 ns, propagation delay mismatch is critical, such that intra-channel skew (skew between the inverting and non-inverting output) must be

kept minimal. LIBG pin is a current reference on the LVDS interface. A 1.5-kΩ pulldown is required unless 855GME platform is being used with external graphics only option.

The following differential signal groups comprise the LVDS Interface. The topology rules for each group are defined in subsequent sections.

Table 58. Signal Group and Signal Pair Names

Channel	Signal Group	Signal Pair Names
Channel A	Clocks	ICLKAM, ICLKAP
	Data Bus	IYAM[3:0], IYAP[3:0]
Channel B	Clocks	ICLKBM, ICLKBP
	Data Bus	IYBM[3:0], IYBP[3:0]

8.2.1. LVDS Length Matching Constraints

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group. These recommendations are provided to achieve optimal SI and timing. In addition to the absolute length limits provided, more restrictive length matching requirements are also provided. The additional requirements further restrict the minimum to maximum length range of each signal group with respect to clock strobe, as required to guarantee adequate timing margins.

8.2.2. LVDS Package Length Compensation

As mentioned in Section 8.2.1, all length matching is done from GMCH die-pad to LVDS connector pin. The reason for this is to compensate for the package length variation across each signal group in order to minimize timing variance. The 855GM chipset GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the 855GM chipset GMCH requires a length matching process. See Table 60 for the GMCH LVDS package lengths information.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of compensating for package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

8.2.3. LVDS Routing Guidelines

Each LVDS channel is required to be length matched to within ± 20 mils of the LVDS clock strobe signals. The two complementary signals in each clock strobe pair, as well as in each data pair, are also required to be length matched to within ± 20 mils of each other. See Table 59 for summary of LVDS signal group routing guidelines.

Table 59. LVDS Signal Group Routing Guidelines

Parameter	Definition
Signal Group	LVDS
Topology	Differential Pair Point to Point
Reference Plane	Ground Referenced
Differential Mode Impedance (Zdiff)	100 Ω ± 15%
Nominal Trace Width	4 mils
Nominal Pair Spacing (edge to edge)	7 mils
Minimum Pair to Pair Spacing (see exceptions for breakout region below)	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other LVDS Signals (see exceptions for breakout region below)	20 mils
Minimum Isolation Spacing to non-LVDS Signals	20 mils
Maximum Via Count	2 (per line)
Package Length Range	550 mils ± 150mils (See LVDS package length Table 60 for exact lengths)
Total Length	Max 10”
Data to Clock Length Matching	Match all segments to within +/- 20 mils of associated clock pair
Clock to Clock# Length Matching (Total Length)	Match clocks to +/- 20 mils
Data to Data# Length Matching (Total Length)	Match data to +/- 20 mils
Breakout Exceptions (Reduced geometries for GMCH breakout region)	Breakout section should be as shorter as possible. Try to maintain trace width as 4 mils, spacing 7 mils, while the spacing between pairs can be 10-20 mils.

The traces associated with the LVDS Transmitter timing domain signals are differential traces terminated across 100 Ω ± 15 % and should be routed as:

- Strip-line only.
- Isolate all other signals from the LVDS signals to prevent coupling from other sources onto the LVDS lines.
- Use controlled impedance traces that match the differential impedance of your transmission medium (i.e. cable) and termination resistor
- Run the differential pair trace lines as close together as possible as soon as they leave the IC, not greater than 10 mils. This will help eliminate reflections and ensure noise is coupled as common mode. Plus, noise induced on the differential lines is much more likely to appear as common mode, which is rejected by the receiver.
- The LVDS Transmitter timing domain signals have a maximum trace length of 10.0 inches. This maximum applies to all of the LVDS Transmitter signals.
- Traces must be ground referenced and must not switch layers between the GMCH and connector.

When choosing cables, it is important to remember:

- Use controlled impedance media. The differential impedance of cable LVDS uses should be 100 Ω ± 15%. Cables should not introduce major impedance discontinuities that cause signal reflection.
- Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality.
- Cable length must be less than 16 inches.

Table 60. LVDS Package Lengths

Signal Group	GMCH Signal Name	Package Trace Length (mils)	Signal Group	GMCH Signal Name	Package Trace Length (mils)
CHANNEL A	ICLKAP	503.7	CHANNEL B	ICLKAP	502.0
	ICLKAM	498.8		ICLKAM	499.1
	IYAP0	399.6		IYBP0	359.8
	IYAM0	385.4		IYBM0	353.7
	IYAP1	487.5		IYBP1	524.7
	IYAM1	466.2		IYBM1	516.6
	IYAP2	572.6		IYBP2	623.3
	IYAM2	566.2		IYBM2	604.2
	IYAP3	643.2		IYBP3	441.8
	IYAM3	637.8		IYBM3	441.7

8.3. Digital Video Out Port

The GMCH DVO port interface supports a wide variety of third party DVO compliant devices (e.g. TV encoder, TMDS transmitter or integrated TV encoder and TMDS transmitter). The GMCH has two dedicated Digital Video Out Ports, DVOB and DVOC. Intel's DVO port is a 1.5-V only interface that can support transactions up to 165 MHz. Some of the DVO port command signals may require voltage translation circuit depending on the third party device. The table below lists the DVO interface signals.

Table 61. DVO Interface Signal Groups

Signal Group	GMCH Signal Name	Signal Type	Signal Group	GMCH Signal Name	Signal Type
DVOB	DVOBFLDSTL	Input	**DVOC**	DVOCFLDSTL	Input
	DVOBHSYNC	Output		DVOCHSYNC	Output
	DVOBVSYNC	Output		DVOCVSYNC	Output
	DVOBBLANK#	Output		DVOCBLANK#	Output
	DVOBD[11:0]	Output		DVOCD[11:0]	Output
	DVOBCLK (DVOBCLK[0])	Output Strobe		DVOCCLK (DVOCCLK[0])	Output Strobe
	DVOBCLK# (DVOBCLK[1])	Output Strobe		DVOCCLK# (DVOCCLK[1])	Output Strobe
Common Signals for Both DVO Ports	DVOBCCLKINT	Input	**Voltage Reference, RCOMP**	DVORCOMP	
	DVOBCINTR#	Input		GVREF	
	ADDID[7:0]	Input			
	DVODETECT	Input			

8.3.1. Length Matching Requirements

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal SI and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching requirements are also provided which further restrict the minimum to maximum length range of each signal group with respect to clock strobe, as required to guarantee adequate timing margins. Refer to Table 62 for DVO length matching requirements.

Table 62. DVO Interface Trace Length Mismatch Requirements

Data Group	Signal Matching to Clock Strobe	DVO Clock Strobes Associated With the Group	Clock Strobe Matching	Notes
DVOBD [11:0]	± 100 mils	DVOBCLK[1:0]	± 10 mils	1,2
DVOCD [11:0]	± 100 mils	DVOCCLK[1:0]	± 10 mils	1,2

NOTES:
1. Data signals of the same group should be trace length matched to the clock within ±100 mil including package lengths.
2. ***All length matching formulas are based on GMCH die-pad to DVO device pin total length.*** Package length table are provided for all signals in order to facilitate this pad to pin matching.

8.3.2. Package Length Compensation

As mentioned in Section 8.3.1, all length matching is done from GMCH die-pad to DVO connector pin. The reason for this is to compensate for the package length variation across each signal group in order to minimize timing variance. The 855GM chipset GMCH does not equalize package lengths internally as some previous GMCH components have, and therefore, the 855GM chipset GMCH requires a length matching process. See Table 64 for the DVO interface package lengths information.

Package length compensation should not be confused with length matching as discussed in the previous section. Length matching refers to constraints on the minimum and maximum length bounds of a signal group based on clock length, whereas package length compensation refers to the process of compensating for package length variance across a signal group. There is of course some overlap in that both affect the target length of an individual signal. Intel recommends that the initial route be completed based on the length matching formulas in conjunction with nominal package lengths and that package length compensation be performed as secondary operation.

8.3.3. DVOB and DVOC Routing Guidelines

Table 63 provides the DVOB and DVOC routing guideline summary.

Table 63. DVOB and DVOC Routing Guideline Summary

Parameter	Definition
Signal Group	DVOBD [11:0], DVCBD [11:0]
Motherboard Topology	Point to point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Zo)	55 Ω ±15%
Nominal Trace Width	Inner layers: 4 mils
Minimum Spacing to Trace Width Ratio	2 to 1 (e.g. 8 mil space to 4 mil trace)
Minimum Isolation Spacing to non-DVO Signals	20 mils
Minimum Spacing to Other DVO Signals	12 mils (see exceptions for breakout region below)
Minimum Spacing of DVOBCLK [1:0] or DVOCCLK [1:0] to any other signals	12 mils
Package Length Range	See Table 64. DVO Interface Package Lengths for package lengths.
Total Length	Min 1.5” Max 6”
Data to Clock Strobe Length Matching Requirements	± 100 mils
CLK0 to CLK1 Length Matching Requirements	± 10 mils

The DVO interface does not require external termination. They are routed point to point as follows:

- All signals should be routed as striplines (inner layers).
- All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal.
- Route the DVOBCLK[1:0] or DVOCCLK[1:0] signal pairs 4 mils wide and 8 mils apart with a max trace length of 6in. This signal pair should be a minimum of 12 mils from any adjacent signals.
- In order to break out of the GMCH, the DVOB and/or DVOC data signals can be routed with a trace width of 4 mils and a trace spacing of 7 mils. The signals should be separated to a trace width of 4 mils and a trace spacing of 8 mils within 0.3 inches of the GMCH component.

Table 64. DVO Interface Package Lengths

Signal	Pin Number	Package Length (mils)	Signal	Pin Number	Package Length (mils)
DVOBCLK	P3	475	DVOCCLK	J3	601
DVOBCLK#	P4	439	DVOCCLK#	J2	675
DVOBD[0]	R3	489	DVOCD[0]	K5	489
DVOBD[1]	R5	439	DVOCD[1]	K1	692
DVOBD[2]	R6	343	DVOCD[2]	K3	622
DVOBD[3]	R4	415	DVOCD[3]	K2	685
DVOBD[4]	P6	409	DVOCD[4]	J6	536
DVOBD[5]	P5	387	DVOCD[5]	J5	518
DVOBD[6]	N5	466	DVOCD[6]	H2	720
DVOBD[7]	P2	553	DVOCD[7]	H1	771
DVOBD[8]	N2	568	DVOCD[8]	H3	649
DVOBD[9]	N3	504	DVOCD[9]	H4	625
DVOBD[10]	M1	611	DVOCD[10]	H6	521
DVOBD[11]	M5	510	DVOCD[11]	G3	762
DVOBFLDSTL	M2	566	DVOCFLDSTL	H5	566
DVOBHSYNC	T6	339	DVOCHSYNC	K6	491
DVOBVSYNC	T5	362	DVOCVSYNC	L5	440
DVOBBLANK#	L2	583	DVOCBLANK#	L3	541
DVOBCCLKINT	M3	520			
DVOBCINTR#	G2	712			

8.3.4. DVOB and DVOC Assumptions, Definitions, and Specifications

The source synchronous solution space consists of all designs in which the flight time mismatch between a strobe and its associated data is less than the total allowable skew:

$$\mathbf{T}_{skew} = \mathbf{T}_{\mathbf{flight}data} - \mathbf{T}_{\mathbf{flight}strobe}$$

Where $\mathbf{T}_{\mathbf{flight}data}$ and $\mathbf{T}_{\mathbf{flight}strobe}$ are the driver-pad-to-receiver-pin flight times of the data and the strobe respectively.

The DVO physical interface is a point-to-point topology using 1.5-V signaling. The DVO uses a 165-MHz clock.

The flight time skew simulations simulate all parameters that could cause a skew between two signals, including motherboard and add-in card line lengths, effective capacitance in the buffer models, crosstalk on each of the different interconnect combinations, data pattern dependencies, and ISI induced skews.

8.3.5. DVOB and DVOC Simulation Method

A model for simulation purposes is shown in Figure 80. The DVO component is a third party-chip.

Figure 80. DVOB and DVOC Simulations Model

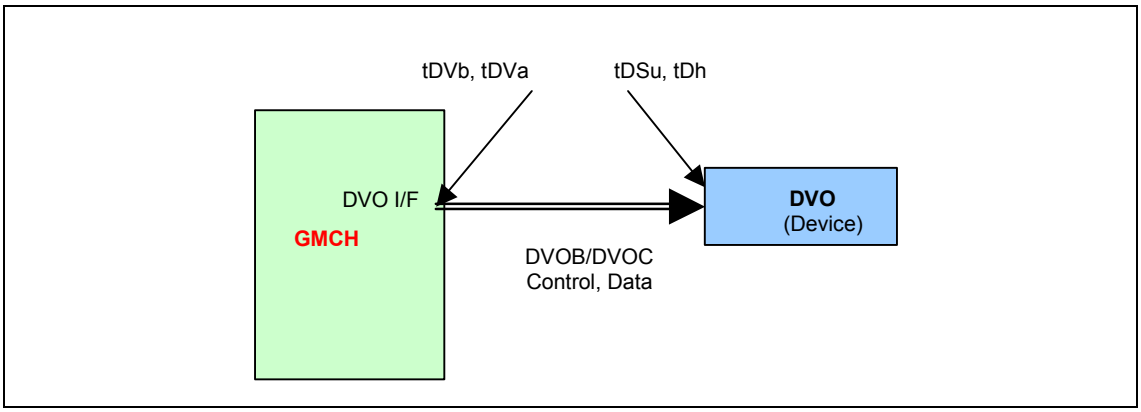
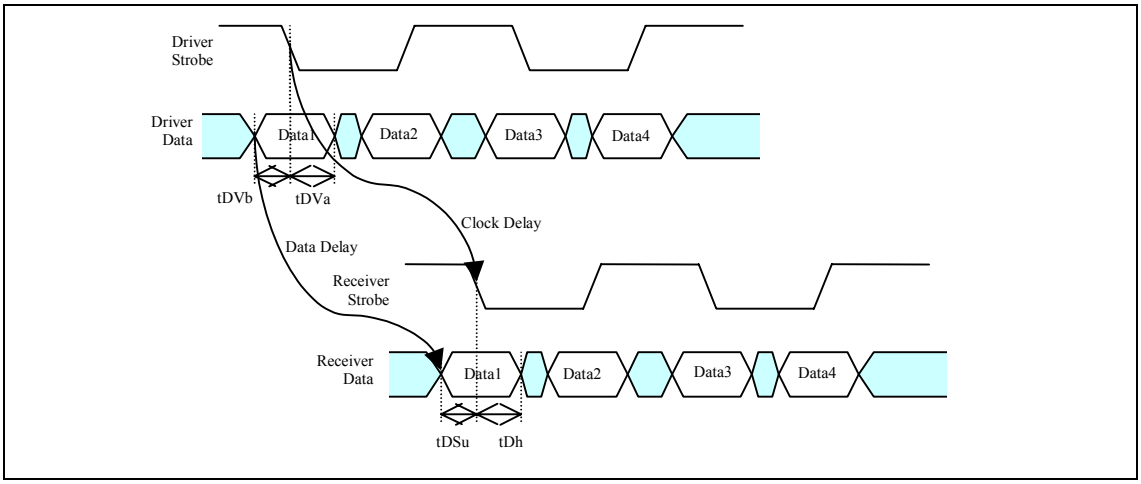


Figure 81. Driver-Receiver Waveforms Relationship Specification



The setup margin and the hold margin for a particular design depends on the values of the data valid times and the data setup and hold times on both the driver and the receiver sides. However, note that available margins are not absolute values. Any skew due to routing and loading differences, any coupling differences in the parallel traces, and any effects of SSO (ISI, ground bounce, etc.) should be accounted for in the timing budget as they will reduce the total available margin for the design.

Table 65. Allowable Interconnect Skew Calculation

Component	Skew Element	Symbol	Setup	Hold	Units
Driver	Data Valid before Strobe	tDVb	570		ps
	Data Valid after Strobe	tDVa		770	ps
Interconnect	Allowable Skew		Vendor specific	Vendor specific	ps
Receiver	Data Setup to Strobe	tDSu	Vendor specific		ps
	Data Hold from Strobe	tDh		Vendor specific	ps

All numbers in this table are from the GMCH specification for DVO interface at 165MHz. For third party receiver devices, please refer to appropriate third party vendor specifications.

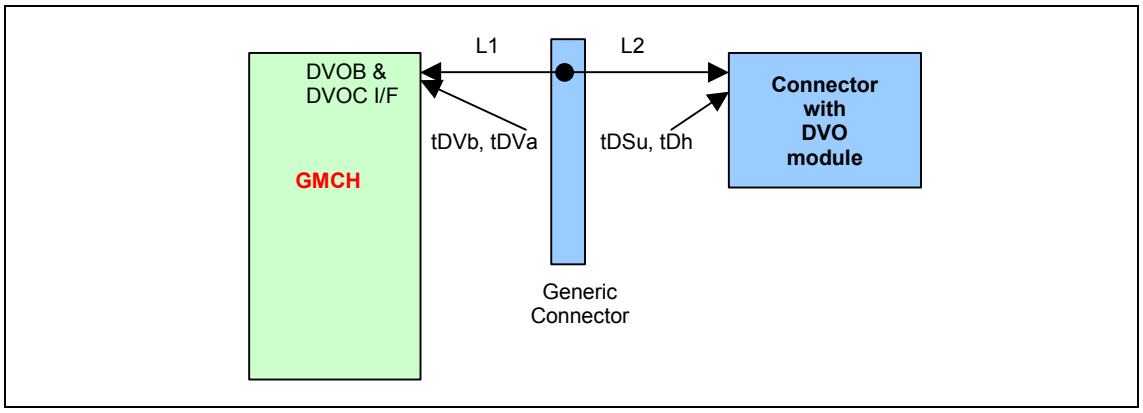
8.4. DVOB and DVOC port Flexible (Modular) Design

The GMCH supports flexible design interfaces described in this section.

8.4.1. DVOB and DVOC Module Design

The GMCH supports a DVO module design connected to the GMCH through a generic connector. Simulation method is the same as in previous section. Lengths L1 and L2 are determined by simulation as L1= 4 inches and L2= 2 inches. Refer to Figure 83 for the generic connector parasitic model.

Figure 82. DVO Enabled Simulation Model



All signals should be routed as striplines (inner layers).All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to ± 100 mils with respect to the strobe clocks as possible to provide optimal timing margin. Each strobe pair must be separated from other signals by at least 12 mils

Table 66 shows DVO enabled routing guideline summary.

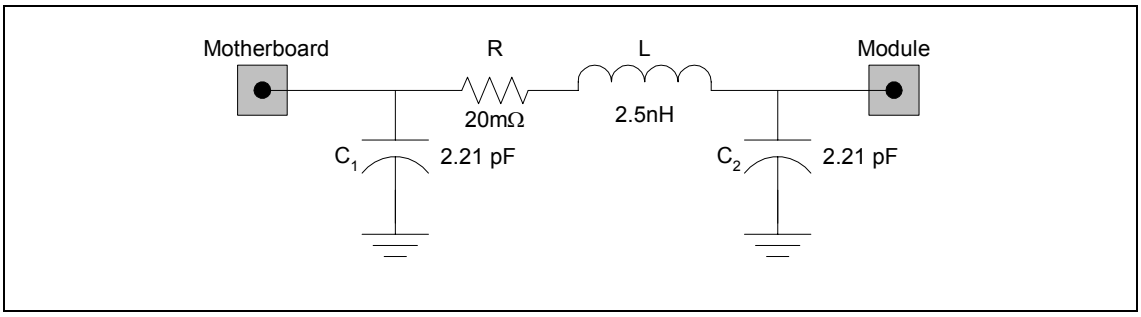
Table 66. DVO Enabled Routing Guideline Summary

Signal	Maximum Length	Trace Width	Trace Spacing	Length Mismatch	Notes
DVO Timing Domain	L1=4 in L2=2 in	4 mils	8 mils	± 100 mils	

8.4.1.1. Generic Connector Model

Figure 83 shows the generic connector model used in simulation for flexible DVO implementation. This is only for reference. Actual connector may have different parasitic values. Designs using this approach need to be simulated first.

Figure 83. Generic Module Connector Parasitic Model



8.5. DVO GMBUS and DDC Interface Considerations

The GMCH DVOB and/or DVOC port controls the video front-end devices via the GMBUS (I2C) interface. DDCADATA and DDCACLK should be connected to the CRT connector. The GMBUS should be connected to the DVO device, as required by the specifications for those devices. The protocol and bus may be used to configure registers in the TV encoder, TMDS transmitter, or any other external DVI device. The GMCH also has an option to utilize the DDCPCLK and DDCPDATA to collect EDID (Extended Display Identification) from a digital display panel.

Pull-ups (or pull-ups with the appropriate value derived from simulating the signal) typically ranging from 2.2 kΩ to 10 kΩ are required on each of these signals.

The following GMCH signal groups list the six possible GMBUS pairs.

Table 67. GMBUS Pair Mapping and Options

Pair #	Signal Name	Buffer Type	Description	Notes
0	DDCADATA	3.3 V	DDC for Analog monitor (CRT) connection.	This cannot be shared with other DDC or I2C pairs due to legacy monitor issues.
	DDCACLK			
1	LCLKCTRLA	3.3 V	For control of SSC clock generator devices down on motherboard.	If SSC is not supported then can be used for DVOB or DVOC GMBUS.
	LCLKCTRLB			
2	DDCPDATA	3.3 V	DDC for Digital Display connection via the integrated LVDS display port for support for EDID panel.	If EDID panels are not supported. Can optionally use as GMBUS for DVOB or DVOC.
	DDCPCLK			
3	MDVIDATA	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	Can optionally use as GMBUS for DVOB or DVOC.
	MDVICLK			
4	MI2CDATA	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	Can optionally use as GMBUS for DVOB or DVOC.
	MI2CCLK			
5	MDDCDATA	1.5 V	DDC for Digital Display connection via TMDS device	Can optionally use as GMBUS for DVOB or DVOC.
	MDDCCLK			

NOTE: All GMBUS pairs can be optionally programmed to support any interface and is programmed through the BMP utility.

If any of GMBUS pairs are not used, 2.2 k – 100 kΩ pull-up (or pull-ups with the appropriate value derived from simulating the signal) resistors are required, except for CRT DDCADATA/DDCCLK and

LCLKCTRLA/LCLKCTRLB GMBUS pair. LCLKCTRLA/LCLKCTRLB are used as bootup straps. Please refer to the *Intel 855GM/GME (Montara-GM/GM+) Chipset GMCH External Design Specification* for details on strapping option. This will prevent the GMCH from confusing noise on these lines for false cycles.

8.5.1. Leaving the GMCH DVOB or DVOC Port Unconnected

If the motherboard does not implement any of the possible video devices with the DVO port, DVO Data output signals may be left unconnected. However pull-up or pull-down resistors are required for the following:

Pull-down resistors are required:

- DVOBFLDSTL
- DVOCFLDSTL
- DVOBCCLKINT

Pull-up resistors are required:

- DVOBCINTR#

8.5.2. Miscellaneous Input Signals and Voltage Reference

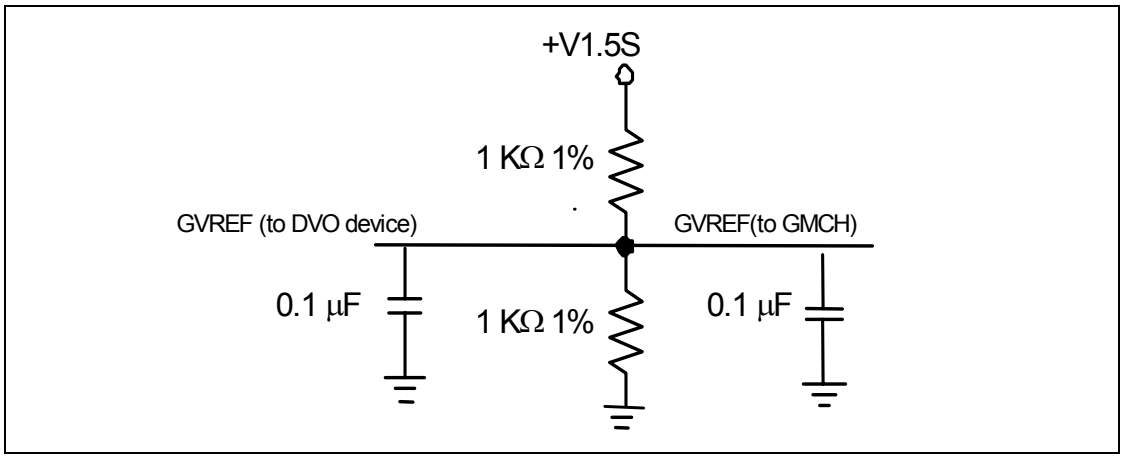
- ADDID[7]: Pulldown to ground with a 1-kΩ resistor when using the DVOB or DVOC port. This is a strapping option for video BIOS to load the TPV AIM module for DVOB and DVOC port. Pulldown not required if DVOB or DVOC is not enabled.
- ADDID[6:0]: Leave unconnected (NC).
- DVODETECT: Leave unconnected (NC) when using the DVOB or DOVC port.
- AGPBUSY#: Connects directly to ICH4-M. A 10-k pullup resistor is required. If using 855GME platform with external AGP graphics this signal may be left no connect.
- DVORCOMP is used to calibrate the DVOB and DVOC buffers. It should be connected to ground via a 40.2 Ω 1% resistor using a routing guideline of 10mil trace and 20mil spacing.
- DPMS: connects to 1.5V version of the ICH4-M's SUSCLK or a clock that runs during S1.
- GVREF: Reference voltage for the DVOB and DVOC input buffers. Refer to the figure below for proper signal conditioning.

8.5.3. PM_SUS_CLK/AGP_PIPE# Design Consideration

The following design consideration provides the option to support both AGP and DVO devices with one AGP/ADD Connector. Refer to Figure 86 for more detail.

The GMCH expects PM_SUS_CLK when there is no AGP device. However, when there is an AGP device this pin functions as AGP_PIPE#. The AGP_TYPEDET# signal is driven high when no AGP card is detected, allowing DPMS_CLK to be driven by PM_SUS_CLK. In the case where an AGP card is detected, AGP_TYPE# signal goes high which disconnects PM_SUS_CLK and allows direct connect of AGP_PIPE# between GMCH and AGP connector.

Figure 84. GVREF Reference Voltage



9. AGP Port Design Guidelines

For detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to the latest AGP Interface Specification, Revision 2.0, which can be obtained from http://www.agpforum.org. This section focuses only on specific Intel 855GME chipset platform recommendations.

9.1. AGP Interface

The *AGP Interface Specification Revision 2.0* enhances the functionality of the original AGP Interface Specification (revision 1.0) by allowing 4X data transfers (4 data samples per clock) and 1.5-volt operation. In addition to these major enhancements, additional performance enhancement and clarifications, such as *fast write* capability, are included in Revision 2.0 of the *AGP Interface Specification*.

The 4X operation of the AGP interface provides for "quad-sampling" of the AGP AD (Address/Data) and SBA (Side-band Addressing) buses. That is, the data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of a 15 ns period (66-MHz clock) or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, the data is sampled twice during a 66-MHz clock cycle. Therefore, the data cycle time is 7.5 ns.

In order to allow for these high-speed data transfers, the AGP interface uses source synchronous data strobing in 2X mode and differential source synchronous data strobing in 4X mode.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great, or there is noise on the interface, incorrect data will be sampled.

The low-voltage operation on AGP (1.5 V) requires even more noise immunity. For example, during 1.5-V operation, $V_{il_{max}}$ is 570 mV. Without proper isolation, crosstalk could create signal integrity issues.

The Intel 855GME GMCH AGP interface supports a single AGP controller. LOCK# and SERR#/PERR# are not supported. AGP 4X, 2X, and 1X operate at 1.5 V *only*.

AGP semantic cycles to DRAM are not snooped on the host bus.

The Intel 855GME GMCH supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization.

The AGP interface is clocked from the 66-MHz clock input to the GCLKIN pin on the GMCH.

9.1.1. AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: 1X timing domain signals, 2X timing, and 4X timing domain signals. Each group has different routing requirements.

All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. Because of the multiplexed AGP/DVO interface, there are trace length matching requirements within each set of 2X/4X signals, as well as between sets of 2X/4X signals.

The signal groups are documented in Table 68.

Table 68. AGP 2.0 Signal Groups

1X Signals	2X Signals	4X Signals
CLK (3.3V) RBF# WBF# GST[2:0] PIPE# REQ# GNT# PAR FRAME# IRDY# TRDY# STOP# DEVSEL# AD[31:0] C/BE[3:0]# SBA[7:0]	2X signals include all 1X signals and AD_STB[1:0] SB_STB AD[31:0] signals and associated C/BE[3:0]# signals are running at 2X mode.	4X signals include all 1X signals and AD_STB[1:0] AD_STB[1:0]# SB_STB SB_STB# AD[31:0] signals and associated C/BE[3:0]# signals are running at 4X mode.

Table 69. AGP 2.0 Data/Strobe Associations

Address/Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

The routing guidelines for each group of signals (1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals) will be addressed separately.

9.2. AGP Routing Guidelines

9.2.1. 1x Timing Domain Routing Guidelines

9.2.1.1. Trace Length Requirements for AGP 1X

This section contains information on the 1X timing domain routing guidelines. The AGP 1X timing domain signals have a maximum trace length of 10 inches (pin to pin). The target impedance is 55-Ω ± 15%. This maximum applies to ALL of the signals listed as 1X timing domain signals in Table 68. In addition to this maximum trace length requirement (refer to Table 70 and Table 71) these signals must meet the trace spacing and trace length mismatch requirements in Sections 9.2.1.2 and 9.2.1.3.

Table 70. Layout Routing Guidelines for AGP 1X Signals

1X signals	Max. Length (inches)	Width (mils)	Space (mils)
CLK_AGP	10	4	4
AGP_PIPE#	10	4	4
AGP_RBF#	10	4	4
AGP_WBF#	10	4	4
AGP_ST[2:0]	10	4	4
AGP_FRAME#	10	4	4
AGP_IRDY#	10	4	4
AGP_TRDY#	10	4	4
AGP_STOP#	10	4	4
AGP_DEVSEL#	10	4	4
AGP_REQ#	10	4	4
AGP_GNT#	10	4	4
AGP_PAR	10	4	4

9.2.1.2. Trace Spacing Requirements

AGP 1X timing domain signals (refer to Table 68) can be routed with 4-mil minimum trace separation.

9.2.1.3. Trace Length Mismatch

There are no trace length mismatch requirements for 1X timing domain signals. These signals must meet minimum and maximum trace length requirements.

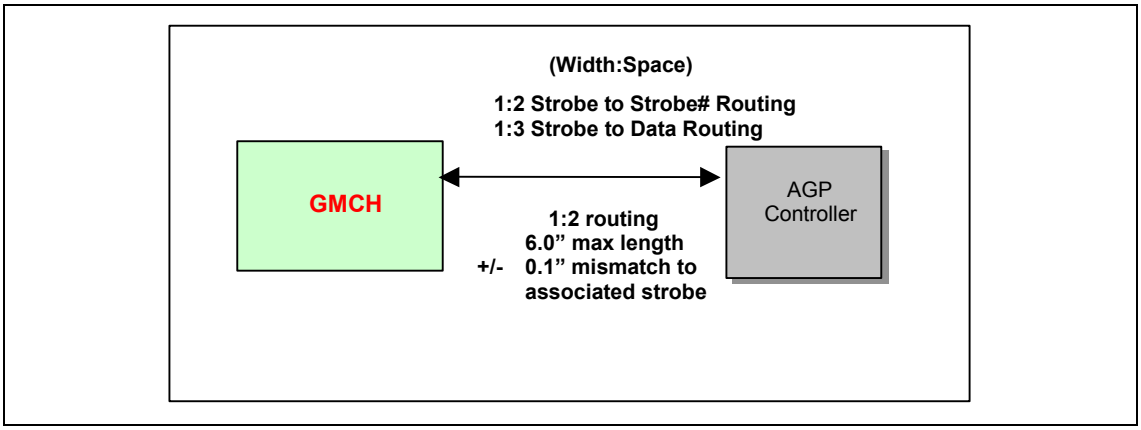
9.2.2. 2x/4x Timing Domain Routing Guidelines

9.2.2.1. Trace Length Requirements for AGP 2X/4X

These trace length guidelines apply to ALL of the signals listed as 2X/4X timing domain signals in Table 68. In addition to these maximum trace length requirements, these signals must meet the trace spacing and trace length mismatch requirements in Sections 9.2.2.2 and 9.2.2.3.

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. These routing rules are divided by trace spacing. In 1:2 spacing, the distance between the traces is two times the width of traces.

Figure 85. AGP Layout Guidelines



For 2X/4X lines in AGP interface, the max length is 6.0 inches (pin to pin) and 1:2 trace spacing is required. 2X signals must be matched to their associated strobe within 0.1 inch. 4X signals must be matched to both of their associated strobes within 0.1 inch. Reduce line length mismatch to ensure added margin.

9.2.2.2. Trace Spacing Requirements

AGP 2X/4X timing domain signals must be routed as documented in Table 71. They should be routed using 4-mil traces. Additionally, the signals can be routed with 5-mil spacing when breaking out of the GMCH. The routing must widen to the requirement in Table 72 within 0.3 inches of the GMCH package.

Since the strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source synchronous AGP interface, special care should be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g. for 4x timing, AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 4-mil traces with 8 mils of space (1:2) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 15 mils (1:3).

Table 71. Layout Routing Guidelines for AGP 2X/4X Signals

Signal	Maximum Length (inch)	Trace Space (mils) (4 mil traces)	Length Mismatch (inch)	Relative To	Notes
2X/4X Timing Domain Set#1	6	8	± 0.1	AGP_ADSTB0 and AGP_ADSTB0#	AGP_ADSTB0, AGP_ADSTB0# must be the same length (±10 mils)
2X/4X Timing Domain Set#2	6	8	± 0.1	AGP_ADSTB1 and AGP_ADSTB1#	AGP_ADSTB1, AGP_ADSTB1# must be the same length (±10 mils)
2X/4X Timing Domain Set#3	6	8	± 0.1	AGP_SBSTB and AGP_SBSTB #	AGP_SBSTB, AGP_SBSTB# must be the same length (±10 mils)

9.2.2.3. Trace Length Mismatch Requirements

Table 72. AGP 2.0 Data Lengths Relative to Strobe Length

Max Trace Length	Trace Spacing	Strobe Length	Min Trace Length	Max Trace Length
< 6 in	1:2	X	X – 0.1 in	X + 0.1 in

The trace length minimum and maximum (relative to strobe length) should be applied to each set of 2X/4X timing domain signals **independently**. That is, if AD_STB0 is 5 inches and ADSTB0# is 5.01 inches, then AD[15:0] and C/BE[1:0] must be between 4.91 inches and 5.1 inches. However AD_STB1 and ADSTB1# can be 3.5 inches and 3.51 inches (and therefore AD[31:16] and C/BE#[3:2] must be between 3.41 inches and 3.6 inches). In addition, all 2X/4X timing domain signals must meet the maximum trace length requirements.

- All signals should be routed as strip lines (inner layers).
- All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to 0 inches as possible to provide optimal timing margin.

The strobe pair must be length matched to less than ± 0.01 inches (that is, a strobe and its compliment must be the same length within ± 0.01 inches).

Table 73 shows the AGP 2.0 routing summary.

Table 73. AGP 2.0 Routing Guideline Summary

Signal	Maximum Length	Trace Spacing (4 mil traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	10 in	4 mils	No Requirement	N/A	None
2X/4X Timing Domain Set#1	6 in	8 mils	± 0.1 in	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	6 in	8 mils	± 0.1 in	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	6 in	8 mils	± 0.1 in	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length

9.2.3. AGP Clock Skew

The maximum total AGP clock skew, between the MCH-M and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter, which originates on the motherboard, add-in module (if used), and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but also at all points on the clock edge that falls in the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew (the motherboard designer shall determine how the 0.9 ns is allocated between the board and the synthesizer).

9.2.4. AGP Signal Noise Decoupling Guidelines

The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the Intel 855GME chipset GMCH. The following guidelines are not intended to replace thorough system validation on Intel 855GME chipset-based products.

- A minimum of six 0.01-µF capacitors are required and must be as close as possible to the GMCH. These should be placed within 70 mils of the outer row of balls on GMCH for VDDQ decoupling. Ideally, this should be as close as possible.
- Intel recommends that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.
- In order to add the decoupling capacitors within 70 mils of the GMCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1.0 inch max.).

In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. One extra 0.01-µF capacitor per 10 vias is required. The capacitor should be placed as close as possible to the center of the via field.

9.2.5. AGP Interface Package Lengths

Table 74. AGP Interface Package Length

GAD0	T6	339
GAD1	T5	362
GAD2	R5	440
GAD3	R3	489
GAD4	R4	415
GAD5	R6	343
GAD6	P5	387
GAD7	P6	409
GAD8	N5	466
GAD9	N3	504
GAD10	N2	568
GAD11	M5	510
GAD12	M1	611
GAD13	M3	520
GAD14	M2	566
GAD15	T7	296
GAD16	L5	440
GAD17	K6	491
GAD18	L3	541
GAD19	K5	489
GAD20	K1	692
GAD21	K3	622
GAD22	K2	685
GAD23	J6	536
GAD24	H1	772
GAD25	H2	720
GAD26	H4	625
GAD27	H3	649
GAD28	G3	762
GAD29	H6	521
GAD30	G2	712
GAD31	H5	566

GADSTB_0	P3	475
GADSTBB_0	P4	439
GADSTB_1	J3	601
GADSTBB_1	J2	675
GSBA_0	E5	686
GSBA_1	F5	617
GSBA_2	E3	738
GSBA_3	E2	865
GSBA_4	G5	668
GSBA_5	F4	688
GSBA_6	G6	518
GSBA_7	F6	613
GSBSTB	F2	799
GSBSTBB	F3	761
GPIPEB	D5	644
GCBEB_0	P2	553
GCBEB_1	L2	583
GCBEB_2	L4	515
GCBEB_3	J5	518
GST_0	C4	750
GST_1	C3	797
GST_2	C2	856
GRBFB	D3	962
GWBFB	D2	947
GFRAMEB	M6	486
GIRDYB	K7	751
GTRDYB	N7	350
GSTOPB	P7	423
GDEVSELB	N6	399
GREQB	B3	762
GGNTB	B2	849
GPAR	L7	623

9.2.6. AGP Routing Ground Reference

Intel strongly recommends that at least the following critical signals be referenced to ground from the GMCH to an AGP controller connector using a minimum number of vias on each net: AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_TRDY#, G_IRDY#, G_GNT#, and ST[2:0].

9.2.7. Pull-ups

The AGP 2.0 Specification requires AGP control signals to have pull-up resistors to VDDQ to ensure they contain stable values when no agent is actively driving the bus. Also, the AD_STB[1:0]# and ST_STB# strobes require pull-down resistors to GND. The GMCH has integrated many of these pull-up/pull-down resistors on the AGP interface and a few other signals not required by the AGP 2.0 Specification. Pull-ups are allowed on any signal except AD_STB[1:0]# and SB_STB#.

The GMCH has no support for the PERR# and SERR# pins for AGP graphics controller with PERR# and SERR# support. Pull-ups to a 1.5-V source are required down on the motherboard in such cases.

Table 75. AGP Pull-Up/Pull-Down Requirements and Straps

Signal	AGP 2.0 Signal Pull-Up/Pull-Down Requirements	GMCH Integrated Pull-Up/Pull-Down	Notes
DEVSEL#		Pull-Up	
FRAME#		Pull-Up	
GNT#		Pull-Up	
INTA#	Pull-Up		3, 5
INTB#	Pull-Up		3, 5
IRDY#		Pull-Up	
PERR#	Pull-Up		2
PIPE#		Pull-Up	
RBF#		Pull-Up	
REQ#		Pull-Up	1
SERR#	Pull-Up		2
ST[2:0]		Pull-Up	4
STOP#		Pull-Up	
TRDY#		Pull-Up	
WBF#		Pull-Up	
AD_STB[1:0]		Pull-Up	
AD_STB[1:0]#		Pull-Down	
SB_STB		Pull-Up	
SB_STB#		Pull-Down	
SBA[7:0]		Pull-Up	1

NOTES:
1. The Intel 855GME chipset GMCH has integrated pull-ups to ensure that these signals do not float when there is no add-in card in the connector.
2. The Intel 855GME chipset GMCH does not implement the PERR# and SERR# signals. Pull-ups on the motherboard are required for AGP graphics controllers that implement these signals.
3. The AGP graphics controller's INTA# and INTB# signals must but routed to the system PCI interrupt request handler where the pull-up requirement should be met. For Intel 855GME chipset-based systems, they can be routed to the ICH4-M's PIRQ signals that are open drain and require pull-ups on the motherboard.
4. ST[1:0] provide the strapping options for 100-MHz PSB operation and DDR memory, respectively.
5. INTA# and INTB# should be pulled to 3.3 V, not VDDQ.

The pull-up/pull-down resistor value requirements are shown in Table 76.

Table 76. AGP 2.0 Pull-up Resistor Values

Rmin	Rmax
4 kΩ	16 kΩ

The recommended AGP pull-up/pull-down resistor value is 8.2 kΩ.

9.2.8. AGP VDDQ and VCC

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller. VDDQ is the interface voltage.

9.2.9. VREF Generation for AGP 2.0 (2X and 4X)

9.2.9.1. 1.5-V AGP Interface (2X/4X)

The voltage divider networks consist of AC and DC elements. The reference voltage that should be supplied to the Vref pins of the graphics controller is ½ * VDDQ. Two 1-kΩ ± 1% resistors can be used to divide VDDQ down to the necessary voltage level.

The Vref divider network should be placed as close to the AGP interface as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the Vref signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity.

9.2.10. AGP Compensation

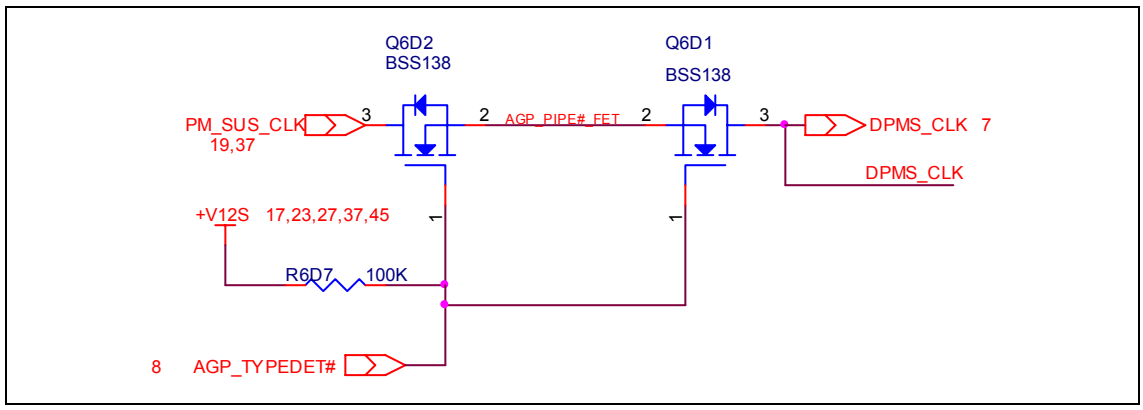
The Intel 855GME chipset GMCH AGP interface supports resistive buffer compensation. For Printed Circuit Boards with characteristics impedance of 55 Ω, connect the GRCOMP pin to a 40.2 Ω ± 1% pull-down resistor (to ground) via a 10-mil wide, very short (≈ 0.5 inches) trace.

9.2.11. PM_SUS_CLK/AGP_PIPE# Design Consideration

The following design consideration provides the option to support both AGP and DVO devices with one AGP/ADD Connector. Refer to Figure 86 for more detail.

The GMCH expects PM_SUS_CLK when there is no AGP device. However, when there is an AGP device this pin functions as AGP_PIPE#. The AGP_TYPEDET# signal is driven high when no AGP card is detected, allowing DPMS_CLK to be driven by PM_SUS_CLK. In the case where an AGP card is detected, AGP_TYPE# signal goes high which disconnects PM_SUS_CLK and allows direct connect of AGP_PIPE# between GMCH and AGP connector.

Figure 86. DPMS Circuit

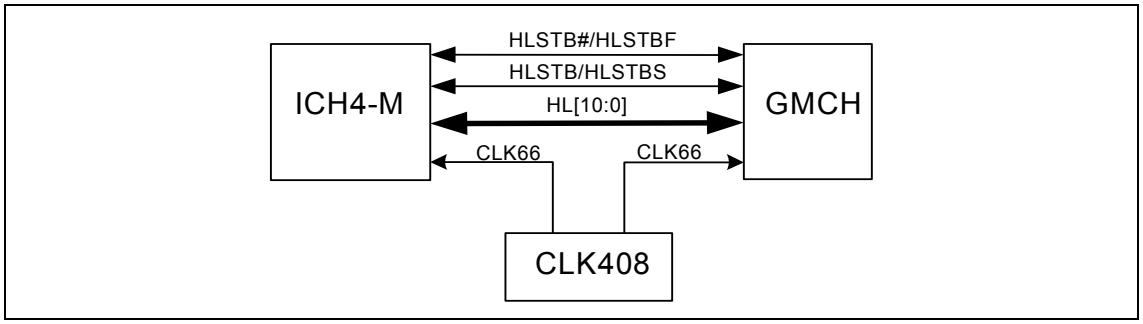


10. Hub Interface

The GMCH and ICH4-M pin-map assignments have been optimized to simplify the hub interface routing between these devices. It is recommended that the hub interface signals be routed directly from the GMCH to the ICH4-M with all signals referenced to VSS. Layer transitions should be kept to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer.

The hub interface signals are broken into two groups: data signals (HL) and strobe signals (HLSTB). For the 11-bit hub interface, HL[10:0] are associated with the data signals while HLSTB and HLSTB# are associated with the strobe signals.

Figure 87. Hub Interface Routing Example



10.1. Hub Interface Compensation

This section documents the routing guidelines for the 11-bit hub interface using enhanced (parallel) termination. This hub interface connects the ICH4-M to the GMCH. The ICH4-M should strap its HLRCOMP pin to V_{CC}=1.5 V, as summarized in Table 77. The 855GM chipset GMCH should strap its HLRCOMP pin to V_{CC}=1.2 V, the 855GME chipset GMCH should strap its HLRCOMP pin to V_{CC}=1.35 V as summarized in Table 77.

The trace impedance must equal 55 Ω ± 15%.

Table 77. Hub Interface RCOMP Resistor Values

Component	Trace Impedance	HLCOMP Resistor Value	HLCOMP Resistor Tied to
ICH4-M	55 Ω ± 15%	48.7 Ω ± 1%	Vcc1_5
855GM GMCH	55 Ω ± 15%	27.4 Ω ± 1%	Vcc1_2
855GME GMCH	55 Ω ± 15%	37.4 Ω ± 1%	Vcc1_35

10.2. Hub Interface Data HL[10:0] and Strobe Signals

The hub interface HL[10:0] data signals should be routed on the same layer as hub interface Strobe signals.

10.2.1. HL[10:0] and Strobe Signals Internal Layer Routing

Traces should be routed 4 mils wide with 8 mils trace spacing (4 on 8) and 20 mils spacing from other signals. In order to break out of the GMCH and ICH4-M packages, the HL[10:0] signals can be routed 4 on 7. The signal must be separated to 4 on 8 within 300 mils from the package.

The minimum HL[10:0] on board signal trace length is 1.5 inches, while the maximum is 6 inches. The HL[10:0] signals must be matched within ± 100 mils of the HLSTB differential pair. There is no explicit matching requirement between the individual HL[10:0] signals.

The hub interface strobe signals HLSTB and HLSTB# should be routed as a differential pair, 4 mils wide with 8 mils trace spacing (4 on 8). The maximum length for strobe signals is 6 inches. Each strobe signal must be the same length and each HL[10:0] signal must be matched to within ± 100 mils of the strobe signals. All length matching should be done from GMCH die to the ICH4-M die. Refer to the package length Table 79 and Table 80.

Table 78. Hub Interface Signals Internal Layer Routing Summary

Signal	Min length (inch)	Max length (inch)	Width (mils)	Space (mils)	Mismatch length (mils)	Relative To	Space with other signals (mils)	Notes
HL[10:0]	1.5”	6”	4	8	± 100	Differential HLSTB pair	20	
HLSTB HLSTB#	1.5”	6”	4	8	± 100	Data lines	20	HLSTB and HLSTB# must be ± 10 mils of each other

Table 79. Hub Interface Package Lengths for ICH4-M

Signal	Pin Number	Package Length (mils)
HUB_PD0	L19	551
HUB_PD1	L20	562
HUB_PD2	M19	552
HUB_PD3	M21	567
HUB_PD4	P19	599
HUB_PD5	R19	627
HUB_PD6	T20	623
HUB_PD7	R20	593
HUB_PD8	P23	668
HUB_PD9	L22	559
HUB_PD10	N22	682
HUB_PD11	K21	560
HUB_CLK	T21	605
HUB_PSTRB	P21	541
HUB_PSTRB#	N20	565

Table 80. Hub Interface Package Lengths for GMCH

Signal	Pin Number	Package Length (mils)
HL[0]	U7	281
HL[1]	U4	408
HL[2]	U3	476
HL[3]	V3	484
HL[4]	W2	551
HL[5]	W6	355
HL[6]	V6	328
HL[7]	W7	343
HL[8]	T3	499
HL[9]	V5	399
HL[10]	V4	457
GCLKIN	Y3	539
HLSTB	W3	504
HLSTB#	V2	548

10.2.2. Terminating HL[11]

The HL[11] signal exists on the ICH4-M but not the GMCH and is not used on the platform. HL[11] must be pulled down to ground via a 56-Ω resistor.

10.3. Hub VREF/VSWING Generation/Distribution

The hub interface reference voltage (VREF) is used on both the GMCH (HLVREF) and the ICH4-M (HIREF). The hub interface also has a reference voltage (VSWING) for the GMCH (PSWING) and the ICH4-M (HI_VSWING), to control voltage swing and impedance strength of the hub interface buffers. The VREF voltage requirements must be set appropriately for proper operation. See Table 81 for the VREF and VSWING voltage specifications. Sections 10.3.1 to 10.3.4 provide details on the different options for VREF and VSWING voltage divider circuitry requirements.

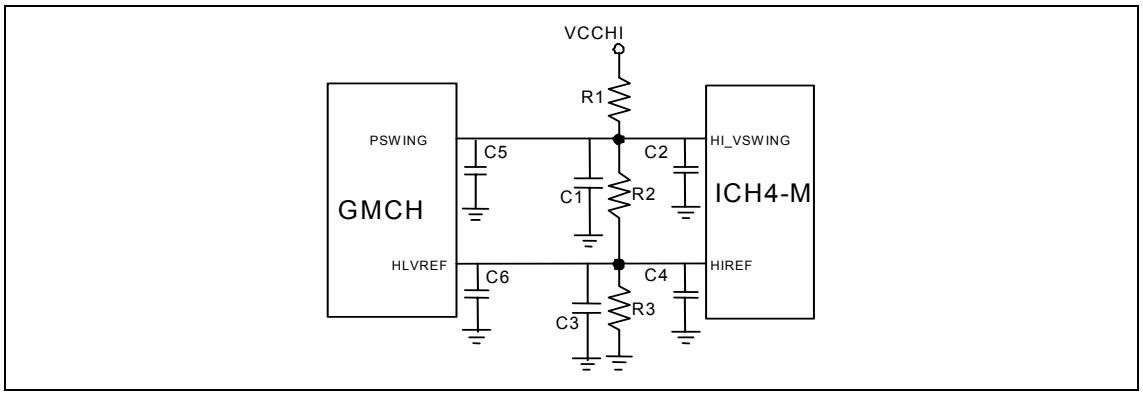
Table 81. Hub Interface VREF/VSWING Reference Voltage Specifications

VREF	VSWING	NOTES
HIREF (ICH4-M) HLVREF (GMCH)	HI_VSWING (ICH4-M) PSWING (GMCH)	
350 mV +/- 8%	800 mV +/- 8%	See Sections 10.3.1, 10.3.2, 10.3.3, and 10.3.4 for recommendations for the VREF/VSWING voltage generation circuitry. See Table 82, Table 83, and Table 84 for recommended resistor values.

10.3.1. Single Generation Voltage Reference Divider Circuit

The GMCH and ICH4-M may share the same single voltage divider circuit. This option provides one voltage divider circuit to generate both VREF and VSWING reference voltage. The reference voltage for both VREF and VSWING must meet the voltage specification in Table 81. If the voltage specifications are not met then individual locally generated voltage divider circuit is required. The maximum trace length from the GMCH to ICH4-M is 4 inches or less. The voltage divider circuit should be place midway between the GMCH and ICH4-M. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). If the trace length exceeds 4 inches then the locally generated voltage reference divider should be used. See section 10.3.2 for the more details.

Figure 88. Single VREF/VSWING Voltage Generation Circuit for Hub Interface



The resistor values, R1, R2, and R3 must be rated at 1% tolerance. See Table 82 for recommended resistor value. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. Two, 0.1-µF capacitors (C1 and C3) should be placed close to the divider. In addition, the 0.01-µF bypass capacitor (C2, C4, C5, and C6) should be placed within 0.25 inches of HLVREF/VREF pin (for C4 and C6) and HI_VSWING pin (for C2 and C5).

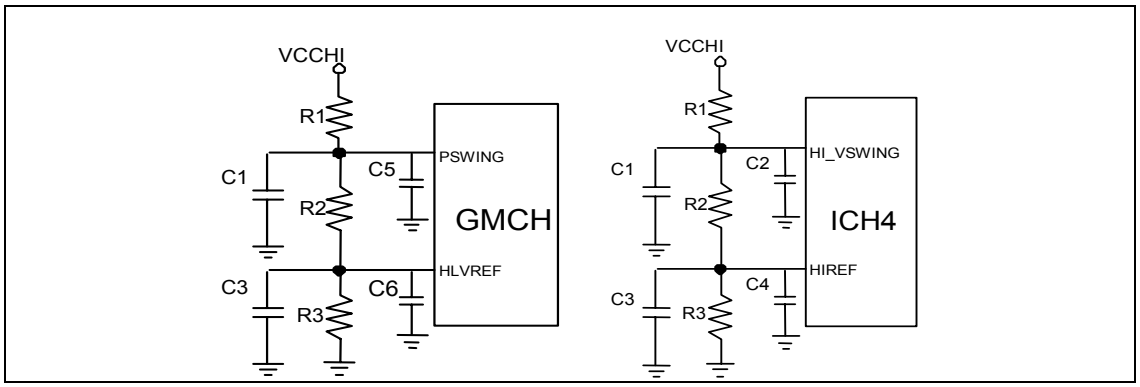
Table 82. Recommended Resistor Values for Single VREF/VSWING Divider Circuit

	Recommended Resistor Values			VCCHI
Option 1	R1 = 80.6 Ω ± 1%	R2 = 51.1 Ω ± 1%	R3 = 40.2 Ω ± 1%	1.5 V
Option 2	R1 = 255 Ω ± 1%	R2 = 162 Ω ± 1%	R3 = 127 Ω ± 1%	1.5 V
Option 3	R1 = 226 Ω ± 1%	R2 = 147 Ω ± 1%	R3 = 113 Ω ± 1%	1.5 V
	C1 and C3 = 0.1 µF (near divider) C2, C4, C5, C6 = 0.01 µF (near component)			

10.3.2. Locally Generated Voltage Reference Divider Circuit

This section describes the option to generate the voltage references separately for GMCH and ICH4-M, to be used if the routing distance between GMCH and ICH4-M is greater than 4 inches. One voltage divider circuit is used to generate both HIVREF and HI_VSWING voltage references for ICH4-M. Another voltage divider circuit is used for GMCH. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 81. The resistor values R1, R2, and R3 must be rated at 1% tolerance (see Table 82). Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). If the voltage specifications are not met then individually generated voltage divider circuit for HIVREF and HI_VSWING is required.

Figure 89. ICH4-M and GMCH Locally Generated Reference Voltage Divider Circuit



10.3.3. Single GMCH and ICH4-M Voltage Generation / Separate Divider Circuit for VSWING/VREF

This section describes the option to use one voltage divider circuit for VREF, shared by both ICH4-M and GMCH, while using another voltage divider circuit for VSWING. This allows for tuning the two reference voltages independently. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 81. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV).

Figure 90. Shared GMCH & ICH4-M Reference Voltage with Separate Voltage Divider Circuit for VSWING and VREF

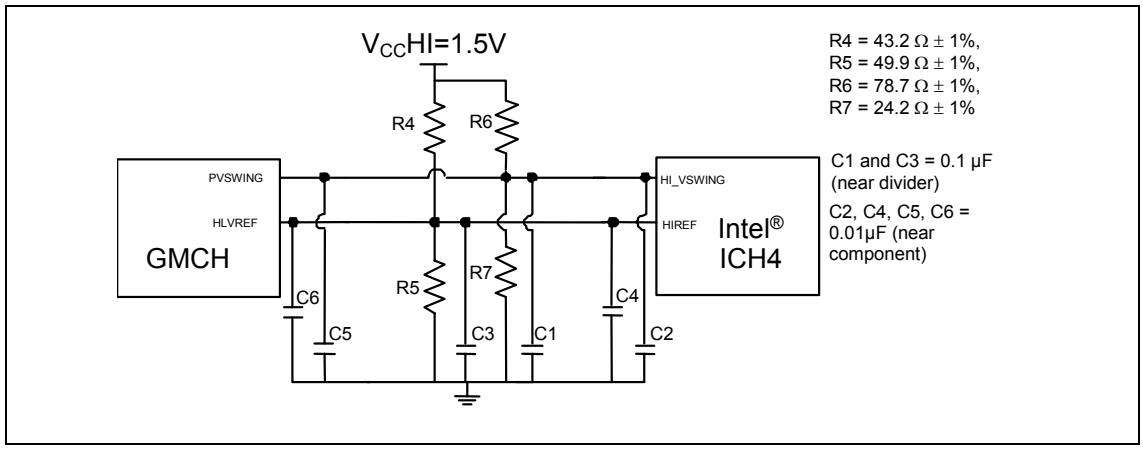


Table 83. Recommended Resistor Values for Separate HIVREF and HI_VSWING Divider Circuits

Signal	Recommended Resistor Values	VCCHI	Capacitor value
HIVREF (350mV)	R4 = 43.2 Ω ± 1% R5 = 49.9 Ω ± 1%,	VCCHI=1.5 V	C3 = 0.1 µF (near divider) C2, C5 = 0.01 µF (near component)
HI_VSWING (800mV)	R6 = 78.7 Ω ± 1% R7 = 24.2 Ω ± 1%,	VCCHI=1.5 V	C1 = 0.1 µF (near divider) C4, C6 = 0.01 µF (near component)

10.3.4. Separate GMCH and ICH4-M Voltage Generation / Separate Divider Circuits for VREF and VSWING

This option allows for tuning the voltage references HIVREF and HI_VSWING individually, for both ICH4-M and GMCH. The reference voltage for both HIVREF and HI_VSWING must meet the voltage specification in Table 81. Normal care needs to be taken to minimize crosstalk to other signals (< 10-15 mV). Note that resistor values used for 855GM chipset GMCH and 855GME chipset GMCH are different since Vcc GMCH is different.

Figure 91. Individual HIVREF and HI_VSWING Voltage Reference Divider Circuits for ICH4-M and GMCH

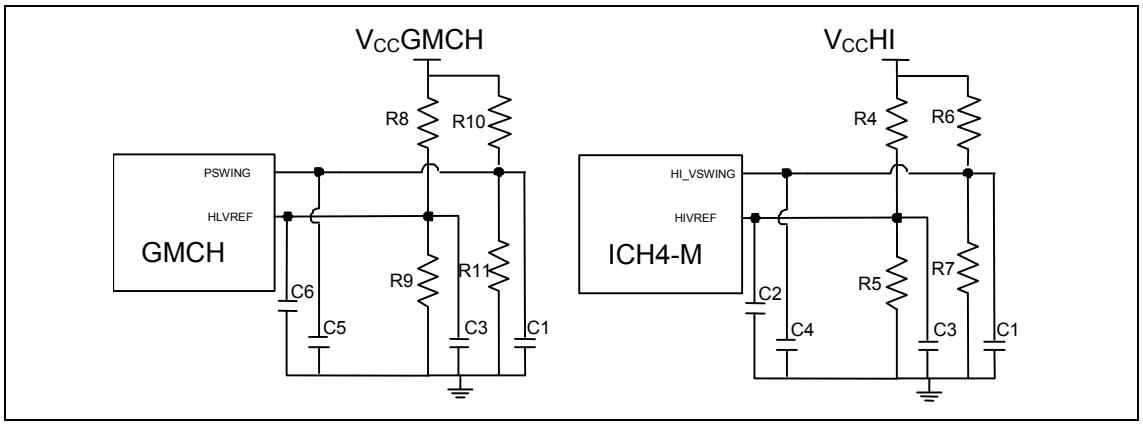


Table 84. Recommended Resistor Values for HIVREF and HI_VSWING Divider Circuits for ICH4-M

Chipset Component	Signal	Recommended Resistor Values	VCCHI	Capacitor value
ICH4-M	HIVREF (350mV)	R4 = 487 Ω ± 1% R5 = 150 Ω ± 1%,	VCCHI=1.5 V	C3 = 0.1 µF (near divider) C2 = 0.01 µF (near component)
	HI_VSWING (800mV)	R6 = 130 Ω ± 1% R7 = 150 Ω ± 1%,	VCCHI=1.5 V	C1 = 0.1 µF (near divider) C4 = 0.01 µF (near component)
855GM	HLVREF (350mV)	R8 = 243 Ω ± 1% R9 = 100 Ω ± 1%	VCCGMCH=1.2 V	C3 = 0.1 µF (near divider) C6 = 0.01 µF (near component)
	PSWING (800mV)	R10 = 49.9 Ω ± 1% R11 = 100 Ω ± 1%	VCCGMCH=1.2 V	C1 = 0.1 µF (near divider) C5 = 0.01 µF (near component)
855GME	HLVREF (350mV)	R8 = 287 Ω ± 1% R9 = 100 Ω ± 1%	VCCGMCH=1.35 V	C3 = 0.1 µF (near divider) C6 = 0.01 µF (near component)
	PSWING (800mV)	R10 = 68.1 Ω ± 1% R11 = 100 Ω ± 1%	VCCGMCH=1.35 V	C1 = 0.1 µF (near divider) C5 = 0.01 µF (near component)

10.4. Hub Interface Decoupling Guidelines

See Section 13.5.5 for more details.

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11. I/O Subsystem

11.1. IDE Interface

This section contains guidelines for connecting and routing the Intel 82801DBM ICH4-M IDE interface. The ICH4-M has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH4-M has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5-mil traces on 7-mil spaces, and must be less than 8 inches long (from ICH4-M to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inches.

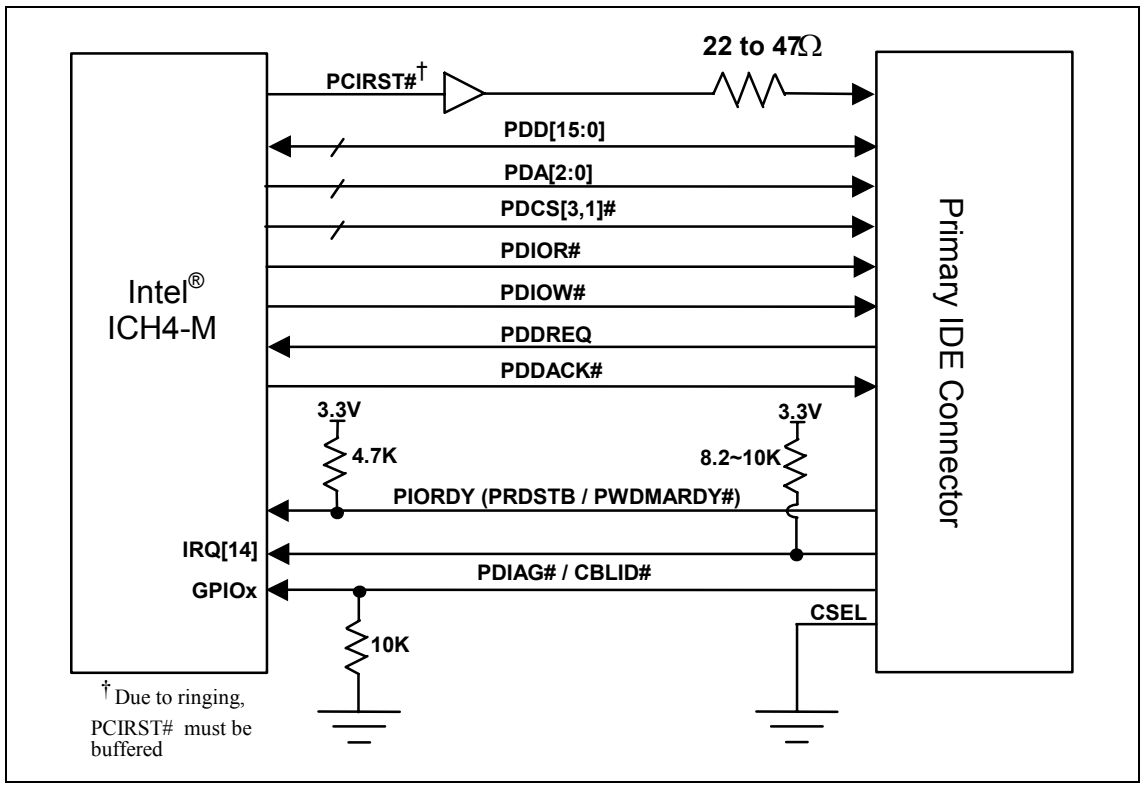
11.1.1. Cabling

The cabling guidelines below must be followed:

- Length of cable: Each IDE cable must be equal to or less than 18 inches.
- Capacitance: Less than 35 pF.
- Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).
- Grounding: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- ICH4-M Placement: The ICH4-M must be placed equal to or less than 8 inches from the ATA connector(s).

11.1.2. Primary IDE Connector Requirements

Figure 92. Connection Requirements for Primary IDE Connector

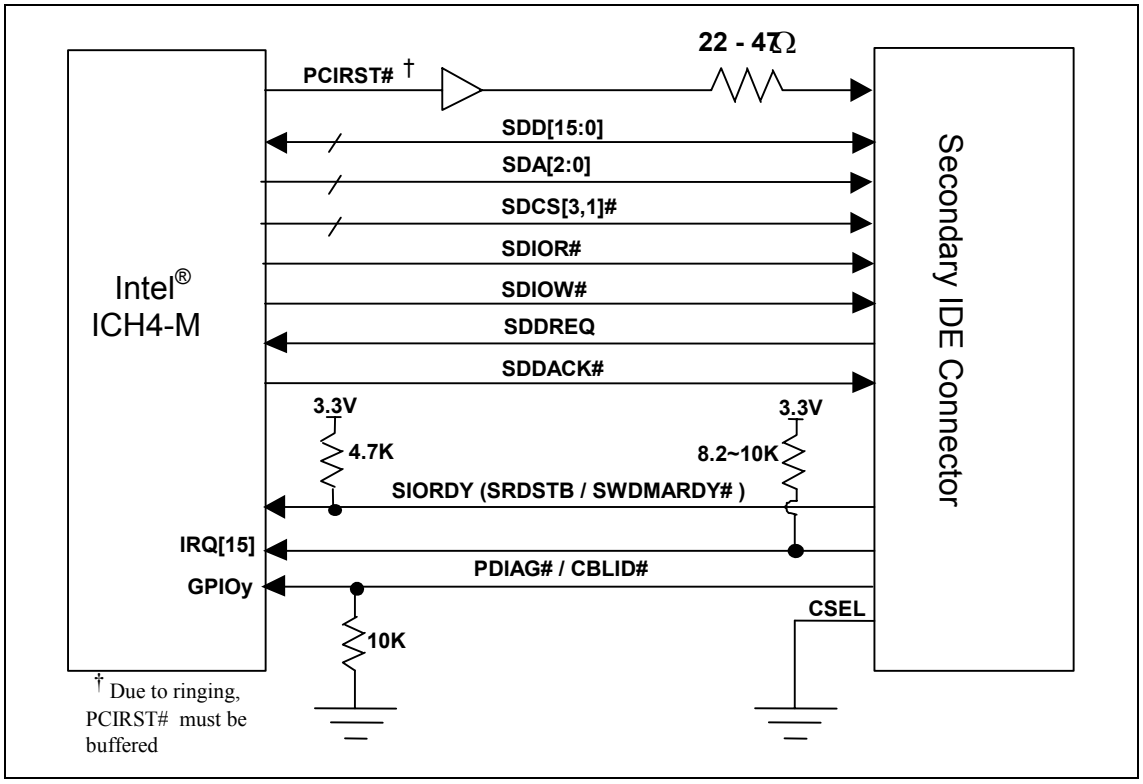


Follow these connection requirements for Primary IDE connector:

- 22 Ω - 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ - 10 kΩ pull-up resistor is required on IRQ14 to VCC3_3.
- A 4.7-kΩ, pull-up resistor to VCC3_3 is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10-kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

11.1.3. Secondary IDE Connector Requirements

Figure 93. Connection Requirements for Secondary IDE Connector



Follow these requirements for Secondary IDE Connector:

- 22 Ω - 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ - 10 kΩ pull-up resistor is required on IRQ15 to VCC3_3.
- A 4.7-kΩ, pull-up resistor to VCC3_3 is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10-kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the Secondary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

11.1.4. Mobile IDE Swap Bay Support

Systems that require the support for an IDE "hot" swap drive bay can be designed to utilize the ICH4-M's IDE interface disable feature to achieve this functionality. To support a mobile "hot" swap bay, the ICH4-M allows the IDE output signals to be tri-stated or driven low and input buffers to be turned off. This requires certain hardware and software requirements to be met for proper operation.

From a hardware perspective, the equivalent of two spare control signals (e.g. GPIO's) and a FET are needed to properly utilize the IDE tri-state feature. An IDE drive must have a reset signal (i.e. first additional control signal) driving its reset pin and a power supply that is isolated from the rest of the IDE interface. To isolate the power supplied to the IDE drive bay, a second additional control signal is needed to control the enabling/disabling of a FET that supplies a separate plane flood powering the IDE drive and its interface.

Although actual hardware implementations may vary, the isolated reset signal and power plane are strict requirements. Systems that connect the IDE swap bay drive to the same power plane and reset signals of the ICH4-M should not use this IDE tri-state feature. Many IDE drives use the control and address lines as straps that are used to enter test modes. If the IDE drive is powered up along with the ICH4-M while the IDE interface is tri-stated rather than being driven to the default state, then the IDE drive could potentially enter a test mode. To avoid such a situation, the aforementioned hardware requirements or equivalent solution should be implemented.

11.1.4.1. ICH4-M IDE Interface Tri-State Feature

The new IDE interface tri-state capabilities of the ICH4-M also include a number of configuration bits that must be programmed accordingly for proper system performance. The names of the critical registers, their location, and brief description are listed below.

1. B0:D31:F0 Offset D5h (BACK_CNTL – Backed Up Control register) bits [7:6] need to be set to 1 in order to enable the tri-stating of the primary and secondary IDE pins when the interfaces are put into reset. By default both bits are set to 1.

2. B0:D31:F0 Offset D0-D3h (GEN_CNTL – General Control Register) bit [3] should be set to 1 in order to lock the state of bits [7:6] at B0:D31:F0 Offset D5h. This prevents any inadvertent reprogramming of the IDE interface pins to a non-tri-state mode during reset by a rogue software program. By default this bit is set to 0 and BIOS should set this bit to 1. This is a write once bit only and requires a PCIRST# to reset to 0. Thus, this bit also needs to be set to 1 after resume from S3-S5.

3. B0:D31:F1 Offset 54h (IDE_CONFIG – IDE I/O Configuration Register) bits [19:18] (SEC_SIG_MODE) and bits [17:16] (PRIM_SIG_MODE) control the reset states of the secondary and primary IDE channels, respectively. The values in SEC_SIG_MODE and PRIM_SIG_MODE are tied to the values set by the BACK_CNTRL register bits [7:6], respectively. When bits [7:6] are set to 1, the PRIM_SIG_MODE and SEC_SIG_MODE will be set to '01' for tri-state when the either IDE channel is put in reset.

4. B0:D31:F1 Offset 40-41h (Primary) and 42-23h (Secondary) bit [5] and bit [1] (IDE_TIM – IDE Timing Register) are the IORDY Sample Point Enable bits for drive 1 and 0 of the primary and secondary IDE channels, respectively. By default, these bits are set to 0 and during normal power up, should be set to 1 by the BIOS to enable IORDY assertion from the IDE device when an access is requested.

11.1.4.2. S5/G3 to S0 Boot Up Procedures for IDE Swap Bay

The procedures listed below summarize the steps that must be followed during power up of an IDE swap bay drive:

1. ICH4-M powers up, IDE interface is tri-stated, disk drive is not powered up. IDE drive is recognized as being on a separate power plane and its reset is different from the ICH4-M.
2. BIOS powers on the IDE drive. e.g. GPIO is used to switch on a FET on the board.
3. Once the IDE drive and interface is powered up, the ICH4-M exits from tri-state mode and begins to actively drive the interface.
4. Once ready, the BIOS can de-assert the reset signal to the IDE drive. e.g. GPIO routed to the IDE drive's reset pin.

11.1.4.3. Power Down Procedures for Mobile Swap Bay

The procedures listed below summarize the steps that must be followed in order to remove an IDE device from the mobile swap bay:

1. User indicates to the system that removal of IDE device from the mobile swap bay should begin. Once the system recognizes that all outstanding IDE accesses have completed, the reset signal to the swap device should be asserted.

2. The IDE channel (primary or secondary) that the device resides on should then be set to drive low mode rather than the default tri-state mode. This requires setting the IDE_CONFIG register (B0:D31:F0 Offset 54h) bits [19:18] or [17:16] to '10' (10b). This will cause all IDE outputs to the IDE drive to drive low rather than the default tri-state (which is useful during boot up to prevent any IDE drives from entering a test mode).

3. The IORDY Sample Point Enable bit of the IDE_TIM register for the appropriate IDE device should then be set to 0 to disable IORDY sampling by the ICH4-M. This ensures that zeros will always be returned if the OS attempts to access the IDE device being swapped.

4. Power to the isolated power plane of the IDE device can then be removed and the system can indicate to the user that the mobile swap bay can be removed and the IDE device replaced.

11.1.4.4. Power Up Procedures After Device "Hot" Swap Completed

The procedures listed below summarize the steps that must be followed after a new IDE device has been added to the mobile swap bay and the swap bay must be powered back up:

1. Once the IDE swap bay is replaced into the system, the power plane to the device should be enabled once again.

2. The IORDY Sample Point Enable bit of the IDE_TIM register for the appropriate IDE device should then be set to 1 to enable IORDY sampling by the ICH4-M. This allows the OS to access the IDE device once again and waits for the assertion of IORDY in response to an access request.

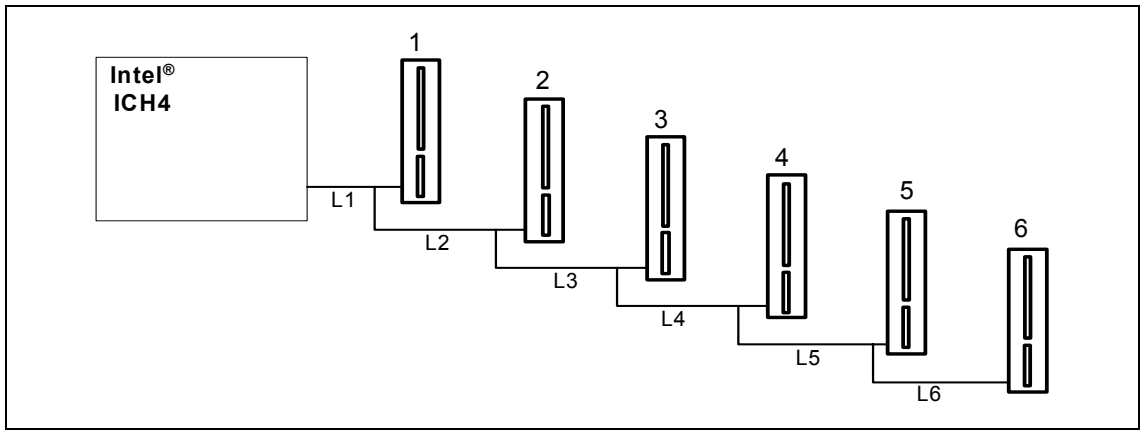
3. Once the system IDE interface is configured for normal operation once again, the reset signal to the swap device should be de-asserted to allow the drive to initialize.

11.2. PCI

The Intel 82801DBM ICH4-M provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high performance data streaming when the ICH4-M is acting as either the target or the initiator in the PCI bus.

The ICH4-M supports six PCI Bus masters (excluding the ICH4-M), by providing six REQ#/GNT# pairs. In addition, the ICH4-M supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 94. PCI Bus Layout Example



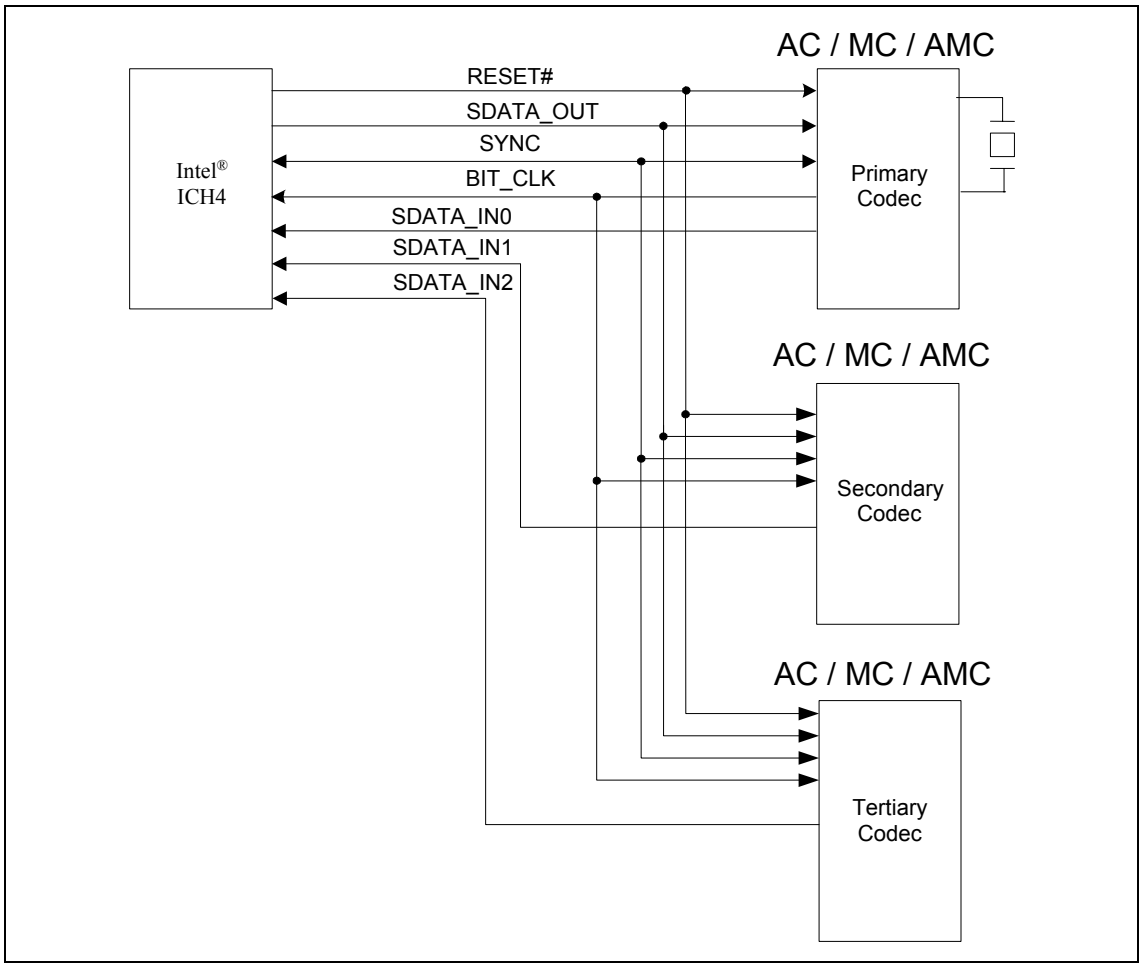
11.3. AC'97

The Intel 82801DBM ICH4-M implements an AC'97 2.1, 2.2, and 2.3 compliant digital controller. Please contact your codec IHV (Independent Hardware Vendor) for information on 2.2 compliant products. The AC'97 2.2 specification is on the Intel website:

http://developer.intel.com/ial/scalableplatforms/audio/index.htm - 97spec/

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH4-M AC-link allows a maximum of three codecs to be connected. Figure 95 shows a three-codec topology of the AC-link for the ICH4-M.

Figure 95. Intel 82801DBM ICH4-M AC'97 – Codec Connection



NOTE: If a modem codec is configured as the primary AC-link Codec, there should not be any Audio Codecs residing on the AC-link. The primary codec may be connected to AC_SDIN0 as documented in the Intel ICH4-M Datasheet.

Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576-MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH4-M) and to any other codec present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK directly off the CK-408 clock chip's 14.31818 MHz output is not supported.**

The ICH4-M supports wake-on-ring from S1M-S5 via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4-M has weak pull-down/pull-ups that are always enabled. This will keep the link from floating when the AC-link is off or there are no codecs present.

If the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT will be driven by the codec and the ICH4-M respectively. However, AC_SDIN0,

AC_SDIN1, and AC_SDIN2 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

Figure 96. Intel 82801DBM ICH4-M AC'97 – AC_BIT_CLK Topology

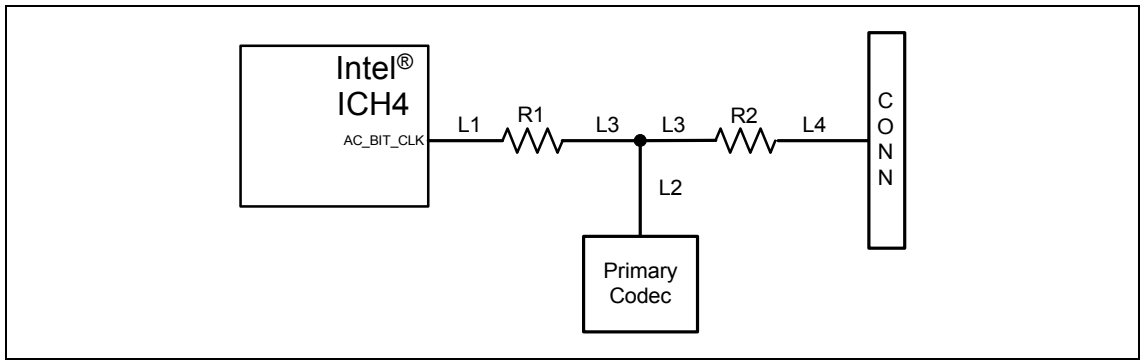


Table 85. AC'97 AC_BIT_CLK Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_BIT_CLK Signal Length Matching
5 on 5	L1 = (1 to 8) – L3 L2 = 0.1 to 6 L3 = 0.1 to 0.4 L4 = (1 to 6) – L3	R1 = 33 Ω - 47 Ω R2 = Option 0 Ω resistor for debugging purposes	N/A

NOTES:
1. Simulations were performed using Analog Device's* Codec (AD1885) and the Cirrus Logic's* Codec (CS4205b). Results showed that if the AD1885 codec was used a 33-Ω resistor was best for R1 and if the CS4205b codec was used a 47-Ω resistor for R1 was best.
2. Bench data shows that a 47-Ω resistor for R1 is best for the Sigmatel* 9750 codec.

Figure 97. Intel 82801DBM AC'97 – AC_SDOUT/AC_SYNC Topology

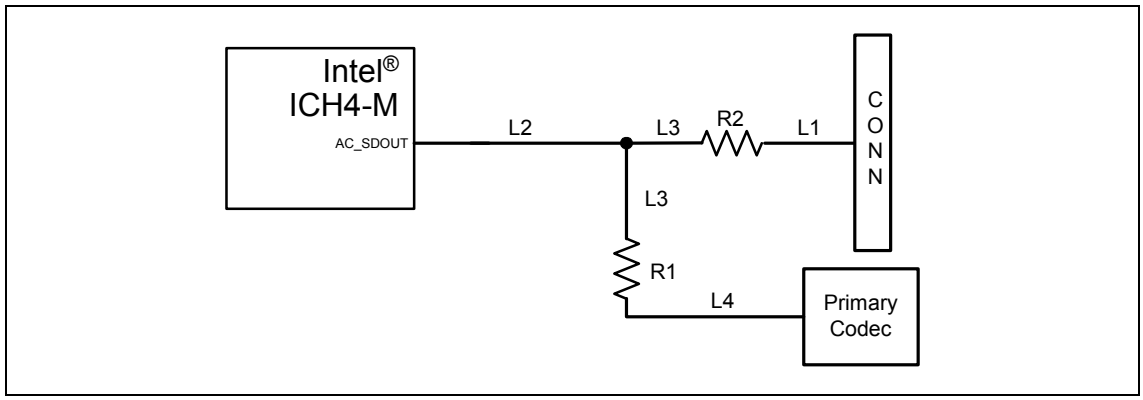


Table 86. AC'97 AC_SDOUT/AC_SYNC Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_SDOUT/AC_SYNC Signal Length Matching
5 on 5	L1 = (1 to 6) – L3 L2 = 1 to 8 L3 = 0.1 to 0.4 L4 = (0.1 to 6) – L3	R1 = 33Ω - 47 Ω R2 = R1 if the connector card that will be used with the platform does not have a series termination on the card. Otherwise R2 = 0 Ω	N/A

NOTES:
1. Simulations were performed using Analog Device's* Codec (AD1885) and the Cirrus Logic's* Codec (CS4205b). Results showed that if the AD1885 codec was used a 33-Ω resistor was best for R1 and if the CS4205b codec was used a 47-Ω resistor for R1 was best.
2. Bench data shows that a 47-Ω resistor for R1 is best for the Sigmatel* 9750 codec.

Figure 98. Intel 82801DBM AC'97 – AC_SDIN Topology

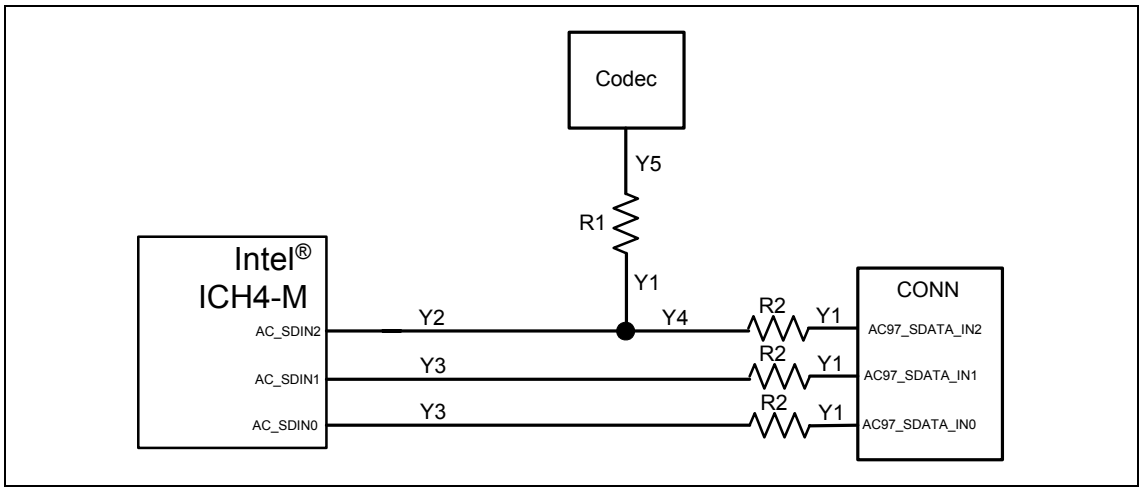


Table 87. AC'97 AC_SDIN Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_SDIN Signal Length Matching
5 on 5	Y1 = 0.1 to 0.4 Y2 = (1 to 8) – Y1 Y3 = (1 to 14) – Y1 Y4 = (1 to 6) – Y1 Y5 = (0.1 to 6) – Y1	R1 = 33 Ω - 47 Ω R2 = R1 if the connector card that will be used with the platform does not have a series termination on the card. Otherwise R2 = 0 Ω	N/A

NOTES:
1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33-Ω resistor was best for R1 and if the CS4205b codec was used a 47-Ω resistor for R1 was best.
2. Bench data shows that a 47-Ω resistor for R1 is best for the Sigmatel 9750 codec.

11.3.1. AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground plane, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

11.3.2. Motherboard Implementation

The following design considerations are provided for the implementation of an ICH4-M platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH4-M platform.

- Active components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH4-M supports wake-on-ring from S1M-S5 states via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

11.3.2.1. Valid Codec Configurations

Table 88. Supported Codec Configurations

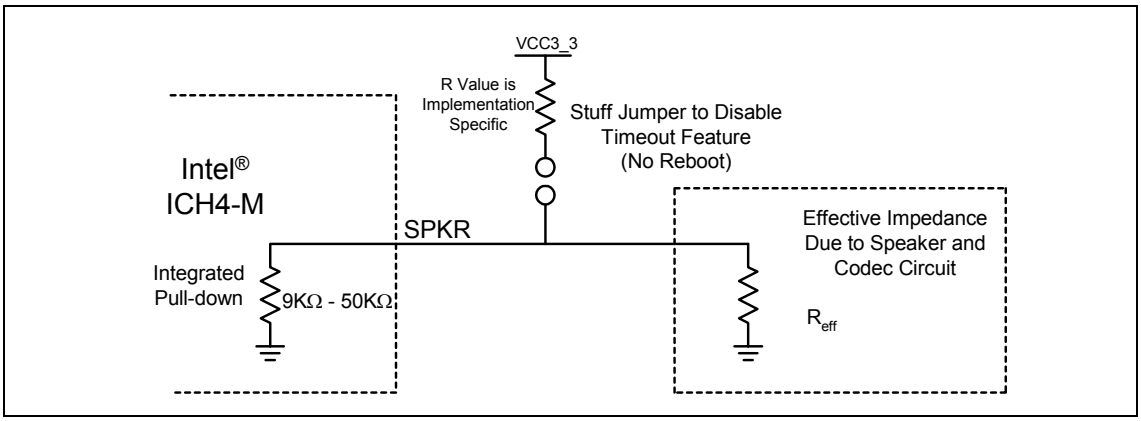
Option	Primary Codec	Secondary Codec	Tertiary Codec	Notes
1	Audio	Audio	Audio	1
2	Audio	Audio	Modem	1
3	Audio	Audio	Audio/Modem	1
4	Audio	Modem	Audio	1
5	Audio	Audio/Modem	Audio	1
6	Audio/Modem	Audio	Audio	1

NOTES:
1. For power management reasons, codec power management registers are in audio space. As a result, if there is an audio codec in the system it must be Primary.
2. There cannot be two modems in a system since there is only one set of modem DMA channels.
3. The ICH4-M supports a codec on any of the AC_SDIN lines, however the modem codec ID must be either 00 or 01.

11.3.3. SPKR Pin Configuration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4-M sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see Figure 99). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{eff}), and the ICH4-M's integrated pull-down resistor will be read as logic high (0.5 * VCC3_3 to VCC3_3 + 0.5 V).

Figure 99. Example Speaker Circuit



11.4. USB 2.0 Guidelines and Recommendations

11.4.1. Layout Guidelines

11.4.1.1. General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems. The USB 2.0 validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second plane is power, the third plane is ground and the fourth is a signal layer. This results in the placement of most of the routing on the fourth plane (closest to the ground plane), allowing a higher component density on the first plane.

1. Place the ICH4-M and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e. I/O connectors, control and signal headers, or power connectors).
2. USB 2.0 signals should be ***ground referenced*** (on recommended stack-up this would be the bottom signal layer).
3. Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities. (As shown in Figure 119.)
5. Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
6. Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs for a particular signal line should not exceed 200 mils.
7. Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0

traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 11.4.2.

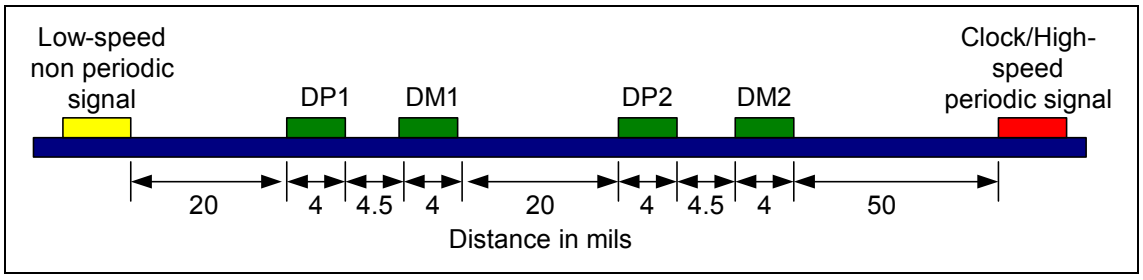
8. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
9. Keep USB 2.0 USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
10. Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

11.4.1.2. USB 2.0 Trace Separation

Use the following separation guidelines.

1. Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90-Ω differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations is kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. 4-mil traces with 4.5-mil spacing results in approximately 90-Ω differential trace impedance.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
4. Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

Figure 100. Recommended USB Trace Spacing



11.4.1.3. USBRBIAS Connection

The USBRBIAS pin and the USBRBIAS# pin can be shorted and routed 5 on 5 to one end of a 22.6 Ω ±1% resistor to ground. Place the resistor within 500 mils of the ICH4-M and avoid routing next to clock pins.

Figure 101. USBRBIAS Connection

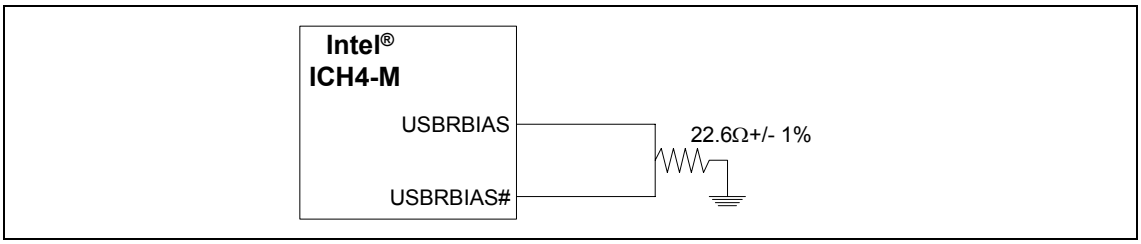


Table 89. USBRBIAS/USBRBIAS# Routing Summary

USBRBIAS/ USBRBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
5 on 5	500 mils	N/A	N/A

11.4.1.4. USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See Section 11.4.4 for details.

11.4.1.5. USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should be no greater that 150 mils.

11.4.1.6. USB 2.0 Trace Length Guidelines

Table 90. USB 2.0 Trace Length Guidelines (With Common-mode Choke)

Configuration	Signal Referencing	Signal Matching	Motherboard Trace Length	Card Trace Length	Maximum Total Length
Back Panel	Ground	The max mismatch between data pairs should not be greater than 150 mils	17 inches	N/A	17 inches

NOTES:
1. These lengths are based upon simulation results and may be updated in the future.
2. All lengths are based upon using a common-mode choke (see Section 11.4.4.1 for details on common-mode choke).

11.4.2. Plane Splits, Voids, and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cutouts.

11.4.2.1. VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the V_{CC} plane.

1. Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the Full-speed Single Ended Zero is common mode).
2. Avoid routing of USB 2.0 signals 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates $V_{CC}5$ and $V_{CC}3\_3$ planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to $V_{CC}5$ and the other side should tie to $V_{CC}3\_3$. Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

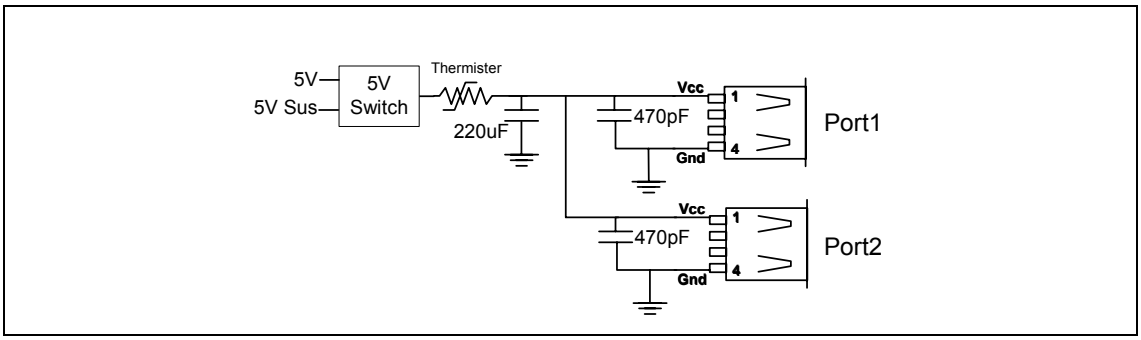
11.4.2.2. GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

11.4.3. USB Power Line Layout Topology

The following is a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach fly-back protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach fly-back voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port and the power carrying traces should be as wide as possible, preferably, a plane. A good "rule-of-thumb" is to make the power carrying traces wide enough that the system fuse will blow on an over current event. If the system fuse is rated at 1amps then the power carrying traces should be wide enough to carry at least 1.5 amps.

Figure 102. Good Downstream Power Connection



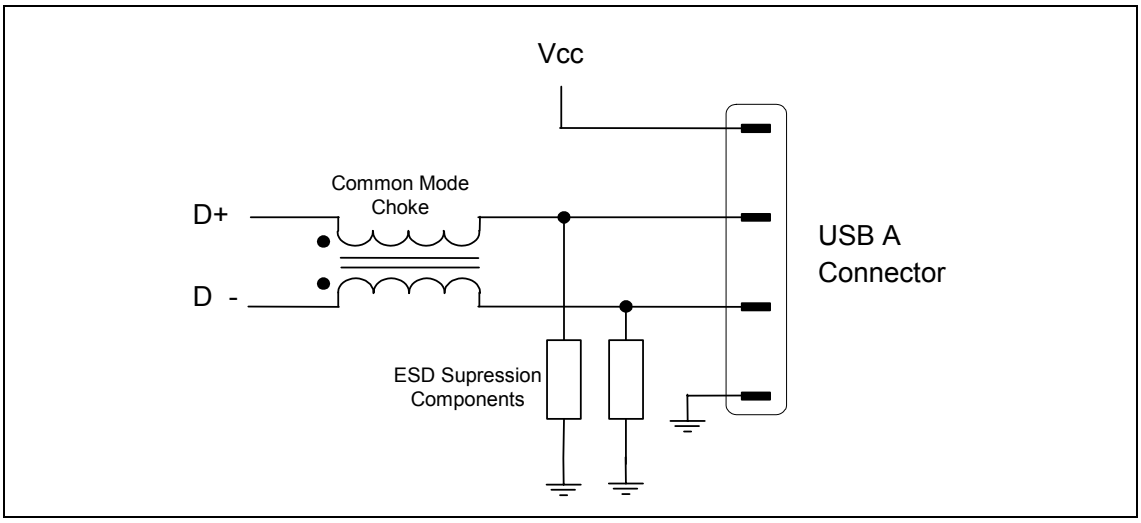
11.4.4. EMI Considerations

The following guidelines apply to the selection and placement of common-mode chokes and ESD protection devices.

11.4.4.1. Common Mode Chokes

Testing has shown that common-mode chokes can provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option **in the event** the choke is needed to pass EMI testing. Figure 103 shows the schematic of a typical common-mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins.

Figure 103. Common Mode Choke Schematic



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality. Common mode chokes with a target impedance of 80 Ω to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
2. Once you have a part that gives passing EMI results the second step is to test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for Low-speed, Full-speed and High-speed USB operation.

11.4.5. ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 103. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, it is recommended to include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

11.4.6. USB Selective Suspend

The USB Specification states that the maximum current consumption on the "USB bus" is 500 mA for normal operation, 2.5mA for suspend power when remote wakeup is supported, and 500 uA otherwise. However, some Bluetooth devices may require more current in suspend state than specified in the USB specification. Therefore, the system designers should ensure that, on their particular system implementation, there is enough current supplied to the Bluetooth device during suspend state in order for selective suspend to function properly.

11.5. I/O APIC (I/O Advanced Programmable Interrupt Controller)

The Intel ICH4-M is designed to be backwards compatible with a number of the legacy interrupt handling mechanisms as well as to be compliant with the latest I/O (x) APIC architecture. In addition to implementing two 8259 interrupt controllers (PIC), the ICH4-M also incorporates an Advanced Programmable Interrupt Controller (APIC) that is implemented via the 3-wire serial APIC bus that connects all I/O and local APICs. An advancement in the interrupt delivery and control architecture of the ICH4-M is represented by support for the I/O (x) APIC specification where PCI devices deliver interrupts as write cycles that are written directly to a register that represents the desired interrupt. These are ultimately delivered via the serial APIC bus or FSB. Furthermore, on Intel Pentium M processor / Intel Celeron M based systems, the ICH4-M has the option to let the integrated I/O APIC behave as an I/O (x) APIC. This allows the ICH4-M to deliver interrupts in a parallel manner rather than just a serial one. This is accomplished by I/O APIC writes to a region of memory that is snooped by the processor and thereby knows what interrupt goes active.

On Intel Pentium M / Intel Celeron M processor-based platforms, the serial I/O APIC bus interface of the ICH4-M should be disabled. I/O (x) APIC is supported on the platform and the servicing of interrupts is accomplished via a PSB interrupt delivery mechanism.

The serial I/O APIC bus interface of the ICH4-M should be disabled as follows.

- Tie APICCLK directly to ground.
- Tie APICD0, APICD1 to ground through a 10-kΩ resistor. (Separate pull-downs are required if using XOR chain testing)

The Intel Pentium M processor and Intel Celeron M processor do not have pins dedicated for a serial I/O APIC bus interface and thus, no hardware change is necessary. However, it is strongly encouraged to enable I/O APIC support in the BIOS and operating system on Intel Pentium M processor / Intel Celeron M based systems rather than the legacy 8259 interrupt controller due to the performance benefits and efficiencies that the I/O (x) APIC architecture enjoys over the older PIC architecture.

11.6. SMBus 2.0/SMLink Interface

The SMBus interface on the ICH4-M uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH4-M.

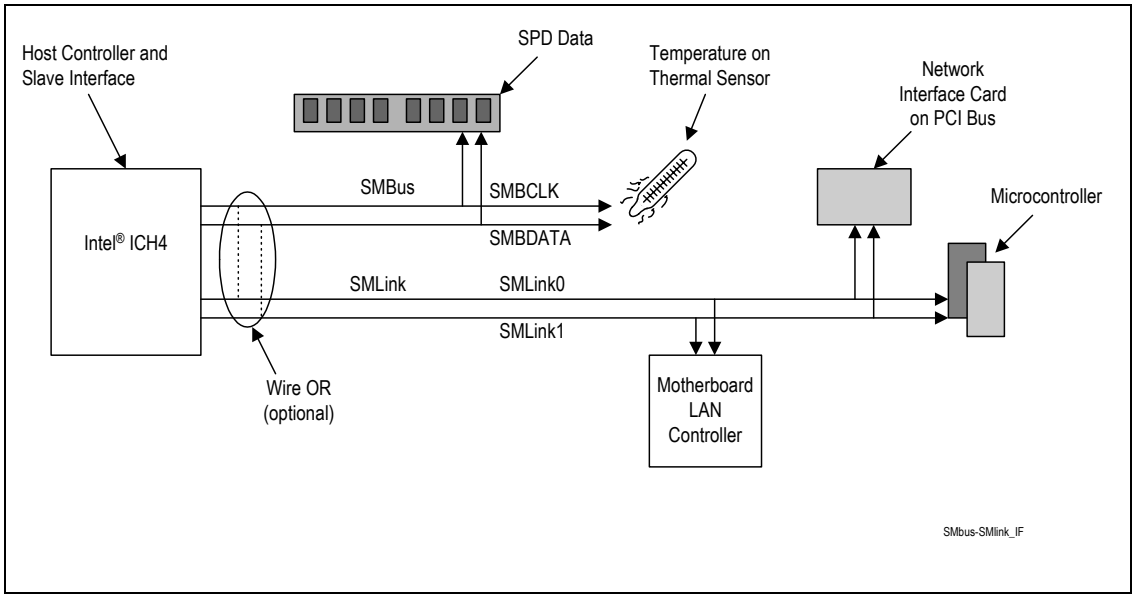
The ICH4-M incorporates an SMLink interface supporting Alert-on-LAN*, Alert-on-LAN2*, and a slave functionality. It uses two signals SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert-on-LAN* functionality, the ICH4-M transmits heartbeat and event messages over the interface. When using the Intel 82562EM Platform LAN Connect Component, the ICH4-M's integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert-on-LAN2*-enabled LAN Controller (i.e. Intel 82562EM 10/100 Mbps Platform LAN Connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4-M SMBus Slave Interface. The slave interface function allows an external

micro-controller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'ed together to allow an external management ASIC (such as Intel 82562EM 10/100 Mbps Platform LAN Connect) to access targets on the SMBus as well as the ICH4-M Slave Interface. Additionally, the ICH4-M supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, in order to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals **must** be tied together externally. This is done by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA.

Figure 104. SMBUS 2.0/SMLink Protocol



Intel does not support external access of the ICH4-M's Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH4-M's SMBus Slave Interface by the ICH4-M's SMBus Host Controller. Refer to *the Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

11.6.1. SMBus Architecture and Design Considerations

11.6.1.1. SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

1. Device class (High/Low power). Most designs use primarily High Power Devices.
2. Are there devices that must run in S3?
3. Amount of $V_{CC\_SUSPEND}$ current available, i.e. minimizing load of $V_{CC\_SUSPEND}$.

11.6.1.2. General Design Issues/Notes

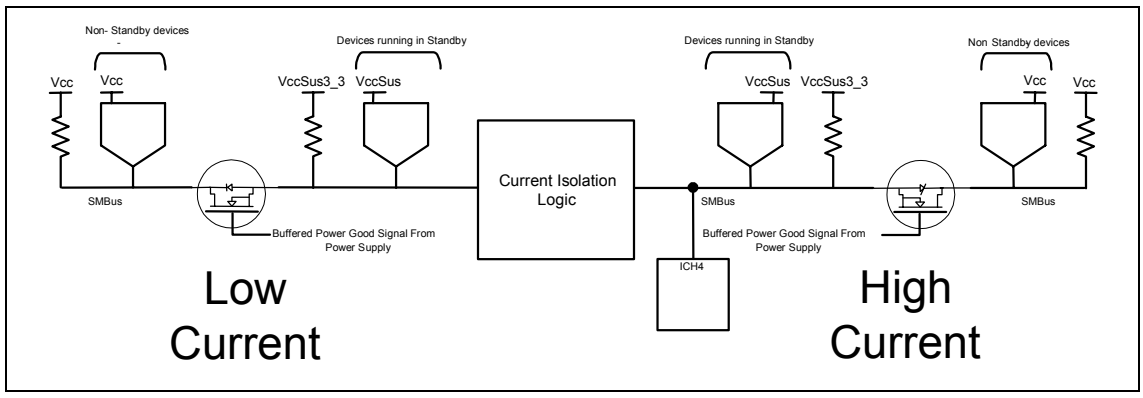
Regardless of the architecture used, there are some general considerations.

1. The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and fall time specification.
2. The maximum bus capacitance that a physical segment can reach is 400 pF.
3. The Intel ICH4-M does not run SMBus cycles while in S3.
4. SMBus devices that can operate in S3 must be powered by the $V_{CC\_SUSPEND}$ supply.

11.6.1.3. High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices while also allowing SMBus devices to communicate during the S3 state. $V_{CC\_SUSPEND}$ leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of a "FET" to isolate the devices powered by the core and suspend supplies. See Figure 105.

Figure 105. High Power/Low Power Mixed $V_{CC\_SUSPEND}$/V_{CC_CORE} Architecture



Added Considerations for Mixed Architecture

1. The bus switch must be powered by $V_{CC\_SUSPEND}$.
2. Devices that are powered by the $V_{CC\_SUSPEND}$ well must not drive into other devices that are powered off. This is accomplished with the "bus switch".
3. The bus bridge can be a device like the Phillips PCA9515.

11.6.1.4. Calculating the Physical Segment Pull-Up Resistor

The following tables are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. If any physical bus segment exceeds 400 pF, then a bus bridge device like the Phillips PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 91. Bus Capacitance Reference Chart

Device	# of Devices/ Trace Length	Capacitance Includes	Cap (pF)
ICH4-M	1	Pin Capacitance	12
CK408	1	Pin Capacitance	10
SO-DIMMS	2	Pin Capacitance (10 pF) + 1 inch worth of trace capacitance (2 pF/inch) per SO-DIMM and 2 pF connector capacitance per SO-DIMM	28
	3		42
PCI Slots	2	Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector	86
	3		129
	4		172
	5		215
	6		258
Bus Trace Length in inches	≥24	2 pF per inch of trace length	48
	≥36		72
	≥48		96

Table 92. Bus Capacitance/Pull-Up Resistor Relationship

Physical Bus Segment Capacitance	Pull-Up Range (For Vcc = 3.3 V
0 to 100 pF	8.2 kΩ to 1.2 kΩ
100 to 200 pF	4.7 kΩ to 1.2 kΩ
200 to 300 pF	3.3 kΩ to 1.2 kΩ
300 to 400 pF	2.2 kΩ to 1.2 kΩ

11.7. FWH

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the *FWH BIOS Specification* or equivalent.

11.7.1. FWH Decoupling

Refer to section 13.5.6 for more details.

11.7.2. In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The ICH4-M hub interface to PCI Bridge will put all CPU boot cycles out on PCI (before sending them out on the FWH interface). If the ICH4-M is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. In order to boot from a PCI card, it is necessary to keep the ICH4-M in subtractive decode mode. If a PCI boot card is inserted and the ICH4-M is programmed for positive decode, there will be two devices positively decoding the same cycle.

11.7.3. FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the ICH4-M INIT# signal needs to be at a value slightly higher than the V_{IH} min FWH INIT# pin specification. The inactive state of this signal is typically governed by the formula V_CPU_IO(min) – noise margin. Therefore if the V_CPU_IO(min) of the processor is 1.60 V, the noise margin is 200 mV and the V_{IH} min spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because 1.6 V – 0.2 V = 1.40 V which is greater than the 1.35 V minimum of the FWH. If the V_{IH} min of the FWH was 1.45 V, then there would be an incompatibility and logic translation would need to be used. The examples above do not take into account any noise that may be encountered on the INIT# signal. Care must be taken to ensure that the V_{IH} min specification is met with ample noise margin. In applications where it is necessary to use translation logic, refer to Section 4.1.4.7.

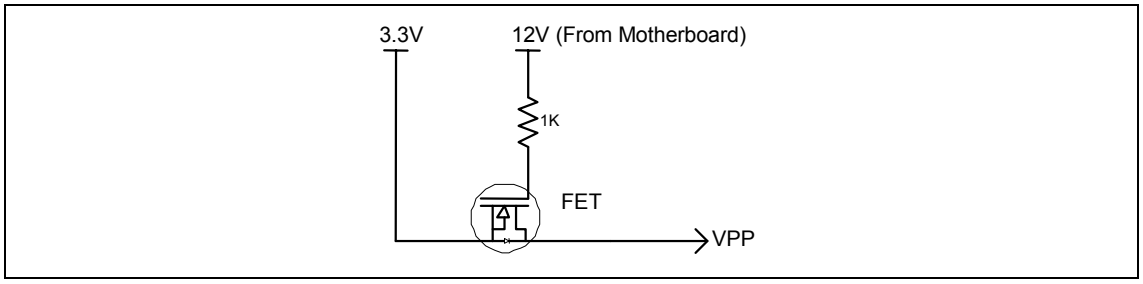
The solution assumes that level translation is necessary. The figure in Section 4.1.4.7 implements a solution for the ICH4-M FWH signal INIT#. Trace lengths and resistor values can be found in Table 16. The Voltage Translator circuitry is shown in Figure 16. It is strongly recommended that any system that implements a FWH should have its INIT# input connected to the ICH4-M.

11.7.4. FWH V_{PP} Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports V_{PP} of 3.3 V or 12 V. If V_{PP} is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12-V V_{PP} for 80 hours (3.3 V on Vpp does not affect the life of the device). The 12 V V_{PP} would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3-V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 106. FWH VPP Isolation Circuitry



11.7.5. FWH INIT# Assertion/Deassertion Timings

Due to the large routing solution space and necessity of a voltage translator in the design of a FWH on Intel Pentium M processor / Intel Celeron M processor and ICH4-M based platforms, the following timing requirements must be met to ensure proper system operation.

For INIT# assertion timings, a conservative analysis of the worst case signal propagation times shows that no timing concerns exist because the ICH4-M asserts INIT# for 16 PCI clocks (485 ns) before deasserting. This provides adequate time for INIT# to propagate to both the processor and FWH.

For the INIT# deassertion event, the critical timing is the minimum period of time before the processor is ready to begin fetching code from the FWH after the INIT# based reset begins. This minimum period is conservatively set at 1 CPU clock (10 ns). This also represents the maximum allowed propagation time for the INIT# signal from the ICH4-M to the FWH.

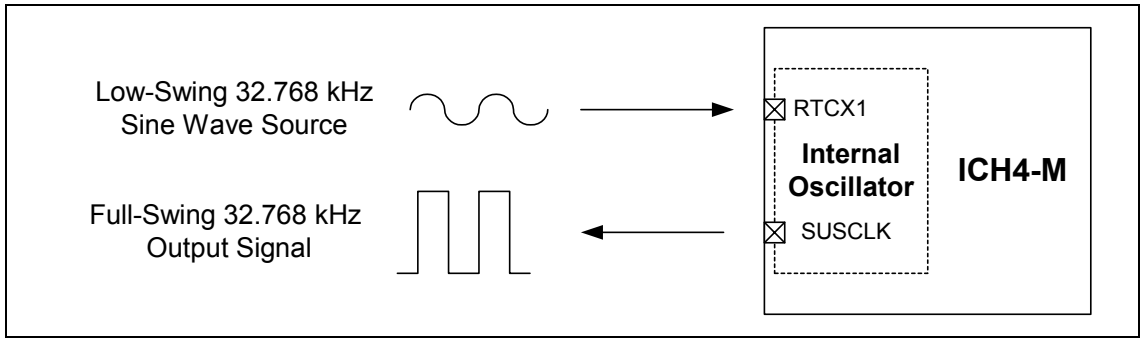
Systems that use alternative devices (i.e. not a FWH) to store the firmware may or may not require the use of INIT#. If INIT# is not used, an analysis should be done to ensure there is no negative impact to system operation. If INIT# is implemented on such a device, voltage translation may be necessary, and the assertion/deassertion timings noted above still apply.

11.8. RTC

The Intel 82801DBM ICH4-M contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH4-M uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4-M, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the ICH4-M is called SUSCLK. This is illustrated in Figure 107.

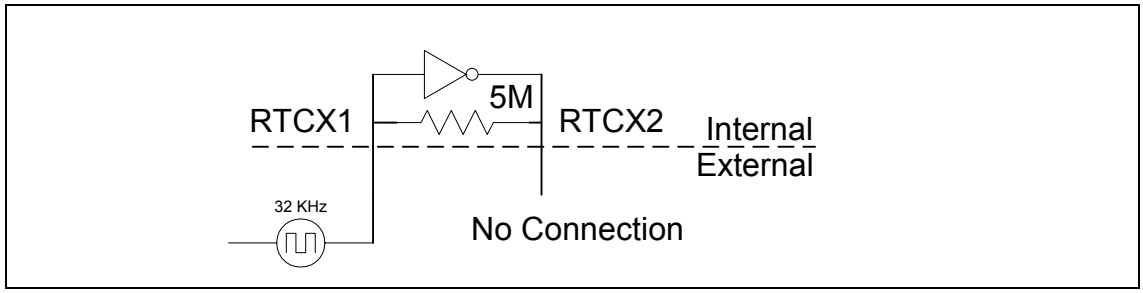
Figure 107. RTCX1 and SUSCLK Relationship in ICH4-M



For further information on the RTC, please consult Application Note AP-728 *ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*. This application note is valid for the ICH4-M.

Even if the ICH4-M internal RTC is not used, it is still necessary to supply a clock input to RTCX1 of the ICH4-M because other signals are gated off that clock in suspend modes. However, in this case, the frequency accuracy (32.768 kHz) of the clock inputs is not critical; a cheap crystal can be used or a single clock input can be driven into RTCX1with RTCX2 left as no connect; Figure 108 illustrates the connection. **This is not a validated feature on the ICH4-M. Please note that the peak-to-peak swing on RTCX1 cannot exceed 1.0 V.**

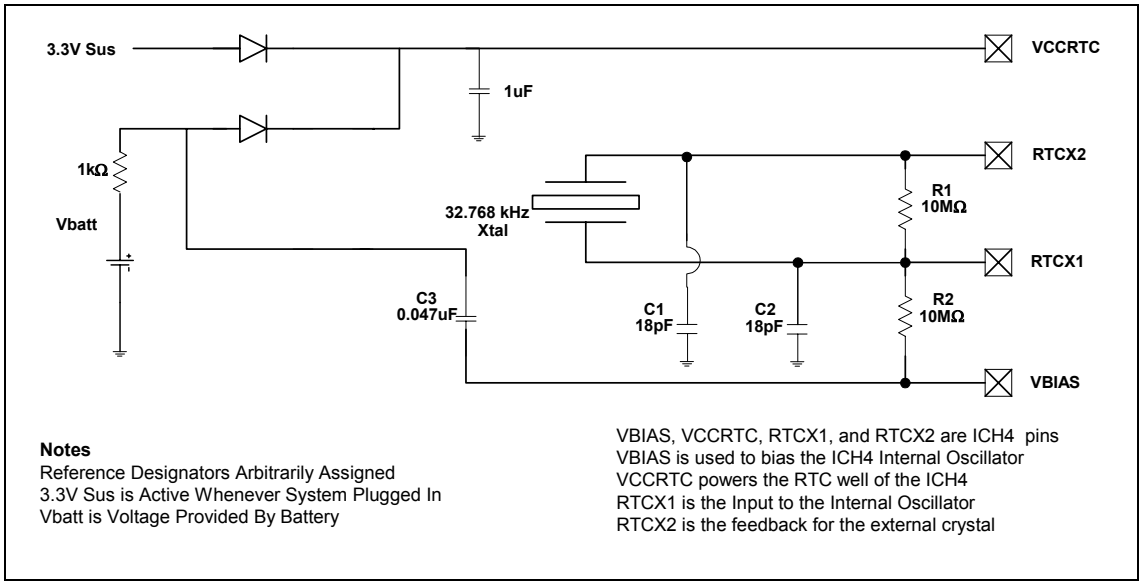
Figure 108. External Circuitry for the ICH4-M Where the Internal RTC is Not Used



11.8.1. RTC Crystal

The Intel 82801DBM ICH4-M RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 109 documents the external circuitry that comprises the oscillator of the ICH4-M RTC.

Figure 109. External Circuitry for the ICH4-M RTC



NOTES:

1. The exact capacitor value needs to be based on what the crystal maker recommends. (Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF)
2. V_{CCRTC}: Power for RTC Well
3. RTCX2: Crystal Input 2 – Connected to the 32.7 68 kHz crystal.
4. RTCX1: Crystal Input 1 – Connected to the 32.7 68 kHz crystal.
5. V_{BIAS}: RTC BIAS Voltage – This ball is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.
6. V_{SS}: Ground

Table 93. RTC Routing Summary

RTC Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, R2, C1, and C2 tolerances	Signal Referencing
5 mil trace width (results in ~2 pF per inch)	1 inch	NA	R1 = R2 = 10 MΩ ± 5% C1 = C2 = (NPO class) See Section 11.8.2 for calculating a specific capacitance value for C1 and C2	Ground

11.8.2. External Capacitors

To maintain the RTC accuracy, the external capacitor C_3 needs to be 0.047 µF and capacitor values C_1 and C_2 should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})]/[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

- C_{load} = Crystal's load capacitance. This value can be obtained from Crystal's specification.
- C_{in1}, C_{in2} = input capacitances at RTCX1, RTCX2 balls of the ICH4-M. These values can be obtained in the ICH4-M's data sheet.
- C_{trace1}, C_{trace2} = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to :

  C_{trace} = trace length * 2 pF/inch
- $C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of 2 electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C_1, C_2 can be chosen such that $C_1 = C_2$. Using the equation of C_{load} above, the value of C_1, C_2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C_2 can be chosen such that $C_2 > C_1$. Then C_1 can be trimmed to obtain the 32.768 kHz.

In certain conditions, both C_1, C_2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C_1, C_2 values are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example will illustrates the use of the practical values C_1, C_2 in the case that theoretical values cannot guarantee the accuracy of the RTC in low temperature condition:

Example 1:

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH4-M, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25°C) to yield a 32.768 kHz oscillation.

At 0°C the frequency stability of crystal gives – 23 ppm (assumed that the circuit has 0 ppm at 25°C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C_1, C_2 are chosen to be 6.8 pF instead of 10pF, the RTC will oscillate at a higher frequency at room temperature (+23 ppm) but this configuration of C_1 / C_2 makes the circuit oscillate closer to 32.768 kHz at 0°C. The 6.8 pF value of C1 and 2 is the **practical value**.

Note that the temperature dependency of crystal frequency is a parabolic relationship (ppm / degree square). The effect of changing the crystal's frequency when operating at 0°C (25°C below room temperature) is the same when operating at 50°C (25°C above room temperature).

11.8.3. RTC Layout Considerations

Since the RTC circuit is very sensitive and requires high accuracy oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

1. Reduce trace capacitance by minimizing the RTC trace length. The ICH4-M requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.

2. Trace signal coupling must be limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 & RTCX2, and VBIAS.

3. Ground guard plane is highly recommended.

4. The oscillator V_{CC} should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

11.8.4. RTC External Battery Connections

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH4-M is not powered by the system.

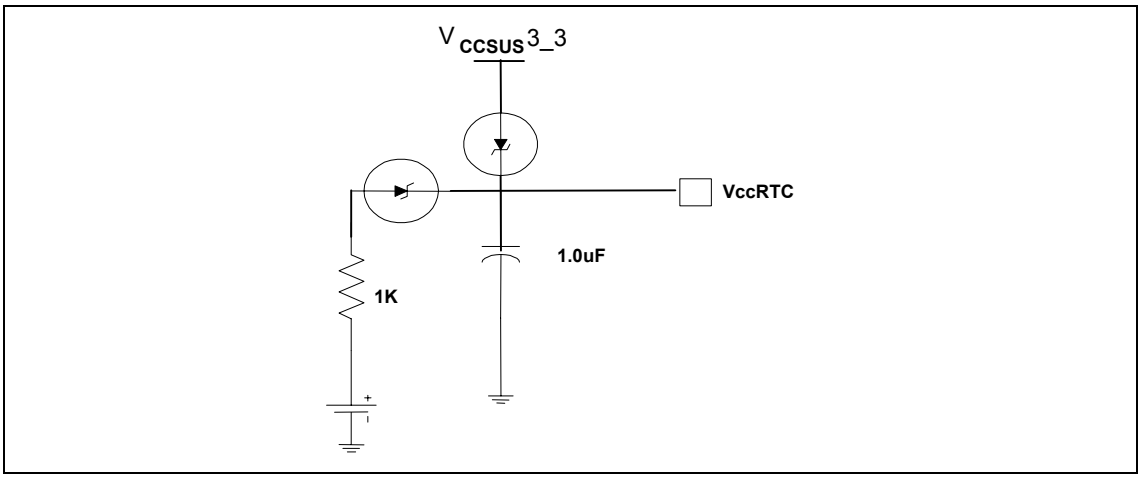
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 5 µA, the battery life will be at least:

170,000 µAh / 5 µA = 34,000 h = 3.9 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH4-M via a Schottky diode circuit for isolation. The Schottky diode circuit allows the ICH4-M RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 110 is an example of a diode circuit that is used.

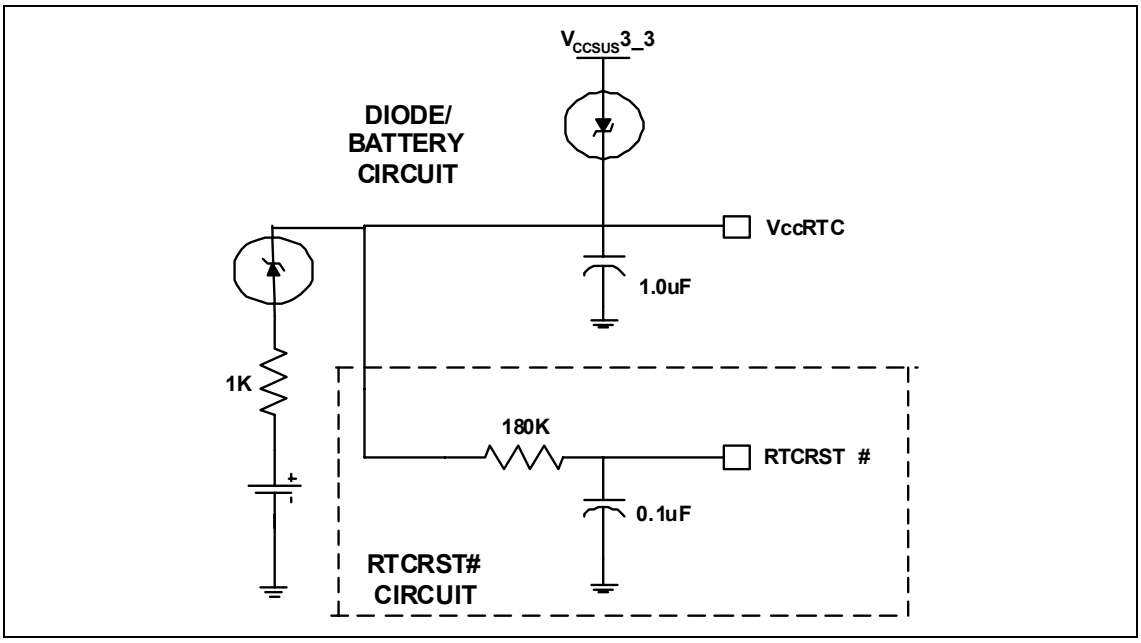
Figure 110. Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

11.8.5. RTC External RTCRST# Circuit

Figure 111. RTCRST# External Circuit for the ICH4-M RTC



The ICH4-M RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18 ms - 25 ms. Any resistor and capacitor combination that yields the proper time constant is acceptable. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and

remains set until software clears it. As a result, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 110) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 111 is an example of this circuitry that is used in conjunction with the external diode circuit.

11.8.6. V_{BIAS} DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC network of R2 and C3 (see Figure 109). Therefore, it is a self-adjusting voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200 mV DC. The RC network of R2 and C3 will filter out most of AC signal noise that exists on this ball. However, the noise on this ball should be kept minimal in order to guarantee the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details on measuring techniques.

Note that VBIAS is also very sensitive to environmental conditions.

11.8.7. SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30-70%. If the SUSCLK duty cycle is beyond 30-70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50-Ω input impedance probe) and it is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH4-M's RTC Clock (see Application Note AP-728 for further details at http://developer.intel.com/design/chipsets/applnots/).

11.8.8. RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to V_{CC}RTC or pulled-down to ground while in the G3 state. RTCRST# when configured as shown in Figure 111 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to V_{CC}RTC. This will prevent these nodes from floating in G3, and correspondingly will prevent I_{CC}RTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

11.9. Internal LAN Layout Guidelines

The Intel 82801DBM ICH4-M provides several options for LAN capability. The platform supports several components depending upon the target market. Available LAN components include the Intel

82540EP Gigabit Ethernet Controller, Intel® 82551QM Fast Ethernet Controller, Intel® 82562ET, and Intel® 82562EM Platform LAN Connect components.

Table 94. LAN Component Connections/Features

LAN Component	Interface to ICH4-M	Connection	Features
Intel® 82540EP (196 BGA)	PCI	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82551QM (196 BGA)	PCI	Performance 10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82562EM (48 Pin SSOP)	LCI	Advanced 10/100 Ethernet	Ethernet 10/100 connection, Alert on LAN* (AoL)
Intel® 82562ET (48 Pin SSOP)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

Design guidelines are provided for each required interface and connection.

11.9.1. Footprint Compatibility

The Intel 82540EP Gigabit Ethernet Controller and the Intel 82551QM Fast Ethernet Controller are all manufactured in a footprint compatible 15 mm x 15 mm (1-mm pitch), 196-ball grid array package. Many of the critical signal pin locations on the 82540EM and the 82551QM are identical, allowing designers to create a single design that accommodates any one of these parts. Because the usage of some pins on the 82540EM differ from the usage on the 82551QM, the parts are not referred to as “pin compatible”. The term “footprint compatible” refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design.

Design guidelines are provided for each required interface and connection. Refer to the following figures and the subsequent table for the corresponding section of this design guide.

Figure 112. Intel 82801DBM ICH4-M/Platform LAN Connect Section

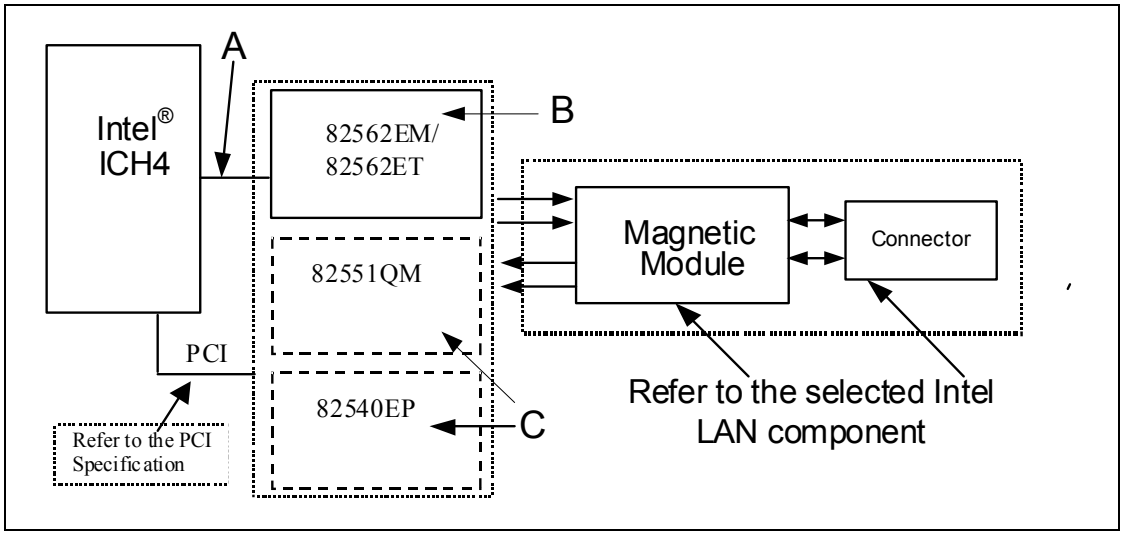


Table 95. LAN Design Guide Section Reference

Layout Section	Figure 112 Reference	Design Guide Section
Intel ICH4-M – LAN Connect Interface (LCI)	A	Reference Section 11.9.2
Intel 82562ET / Intel 82562EM	B	Reference Section 11.9.3
Intel 82551QM / Intel 82540EP	C	Reference Section 11.9.5

11.9.2. Intel® 82801DBM ICH4-M – LAN Connect Interface Guidelines

This section contains guidelines on how to implement a Platform LAN Connect device on a system motherboard. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH4-M to LAN Connect Interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports Intel 82562ET and Intel 82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by all components. The AC characteristics for this interface are found in the *Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Specification Update.*

11.9.2.1. Bus Topologies

The Platform LAN Connect Interface can be configured in several topologies:

- Direct point-to-point connection between the ICH4-M and the LAN component
- LOM Implementation

11.9.2.1.1. LAN On Motherboard Point-To-Point Interconnect

The following are guidelines for a single solution motherboard. Either Intel 82562EM or Intel 82562ET is uniquely installed.

Figure 113. Single Solution Interconnect

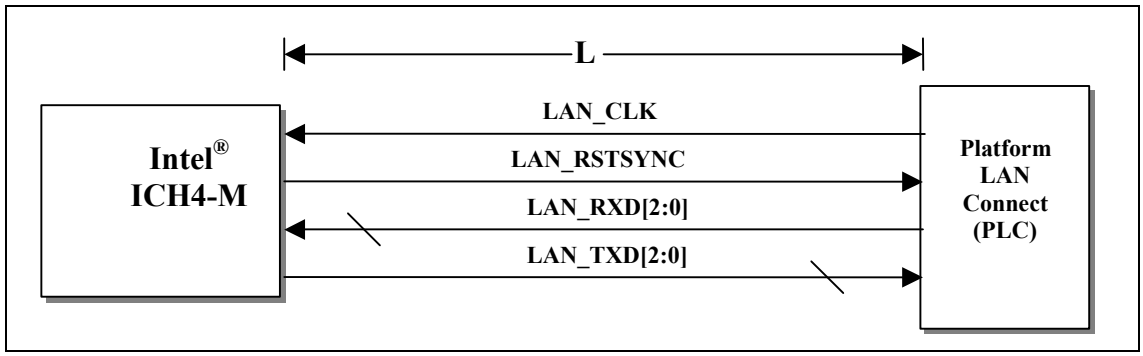


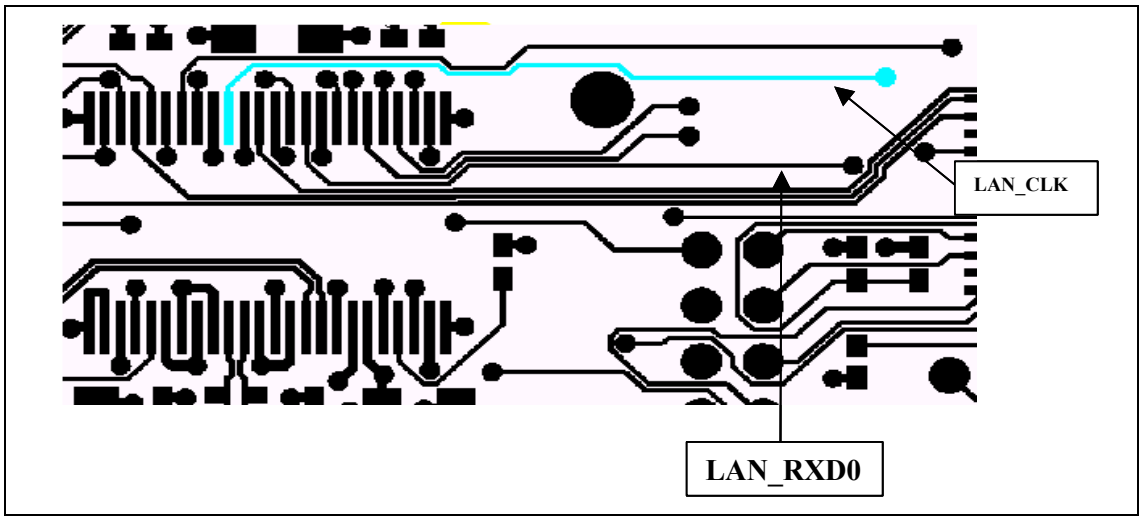
Table 96. LAN LOM Routing Summary

Trace Impedance	LAN Routing Requirements	Maximum Trace Length	Signal Referencing	LAN Signal Length Matching
55Ω ± 15%	5 on 10	4.5 to 12 inches	Ground	Data signals must be equal to or no more than 0.5 inches (500 mils) shorter than the LAN clock trace.

11.9.2.2. Signal Routing and Layout

Platform LAN Connect Interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. Intel recommends that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 114. LAN_CLK Routing Example



11.9.2.3. Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter. t_{RMATCH} is the sum of the trace length mismatch between LAN_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

11.9.2.4. Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard. An impedance of 55 Ω ± 15% is strongly recommended; otherwise, signal integrity requirements may be violated.

11.9.2.5. Line Termination

Line termination mechanisms are not specified for the LAN Connect Interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 0-Ω to 33-Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

11.9.2.6. Terminating Unused LAN Connect Interface Signals

The LAN Connect Interface on the ICH4-M can be left as a no-connect if it is not used.

11.9.3. Intel 82562ET / Intel 82562 EM Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 11.9.6. Additional guidelines for implementing an Intel 82562ET or Intel 82562EM Platform LAN Connect component are provided below.

11.9.3.1. Guidelines for Intel 82562ET / Intel 82562EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

11.9.3.2. Crystals and Oscillators

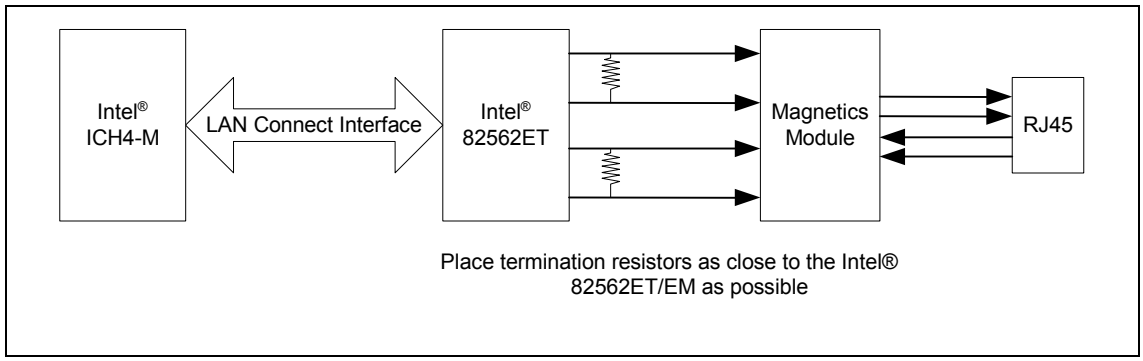
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent the possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discrete components as close as possible to the Intel 82562ET/EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

11.9.3.3. Intel 82562ET / Intel 82562EM Termination Resistors

The 100 Ω ± 1% resistor used to terminate the differential transmit pairs (TDP/TDN) and the 121 Ω ± 1% receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN connect component (Intel 82562ET or Intel 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e. Intel 82562ET), including the wire impedance reflected through the transformer.

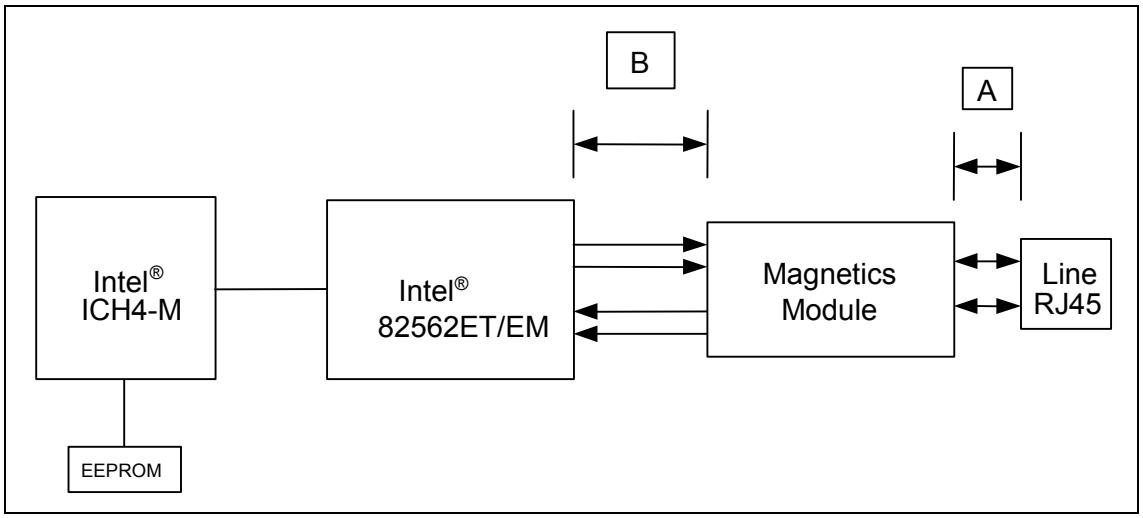
Figure 115. Intel 82562ET / Intel 82562EM Termination



11.9.3.4. Critical Dimensions

There are two dimensions to consider during layout. Distance ‘A’ from the line RJ-45 connector to the magnetics module and distance ‘B’ from the Intel 82562ET or Intel 82562EM to the magnetics module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches). (See Figure 116.)

Figure 116. Critical Dimensions for Component Placement



Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

11.9.3.4.1. Distance from Magnetics Module to RJ-45 (Distance A)

The distance A in Figure 116 above should be given the highest priority in board layout. The distance between the magnetics module and the RJ-45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit’s performance and contribute to radiated emissions from the transmit circuit. If the Intel 82562ET must be placed further than a couple of inches from the RJ-45 connector, distance B can be sacrificed. Keeping the total distance between the Intel 82562ET and RJ-45 will as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 Ω to 110 Ω should compensate for second order effects.

11.9.3.4.2. Distance from Intel 82562ET / 82562ET to Magnetics Module (Distance B)

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100-Ω differential value. These traces should also be symmetric and equal length within each differential pair.

11.9.3.5. Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible because signals with fast rise and fall times contain many high frequency harmonics that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

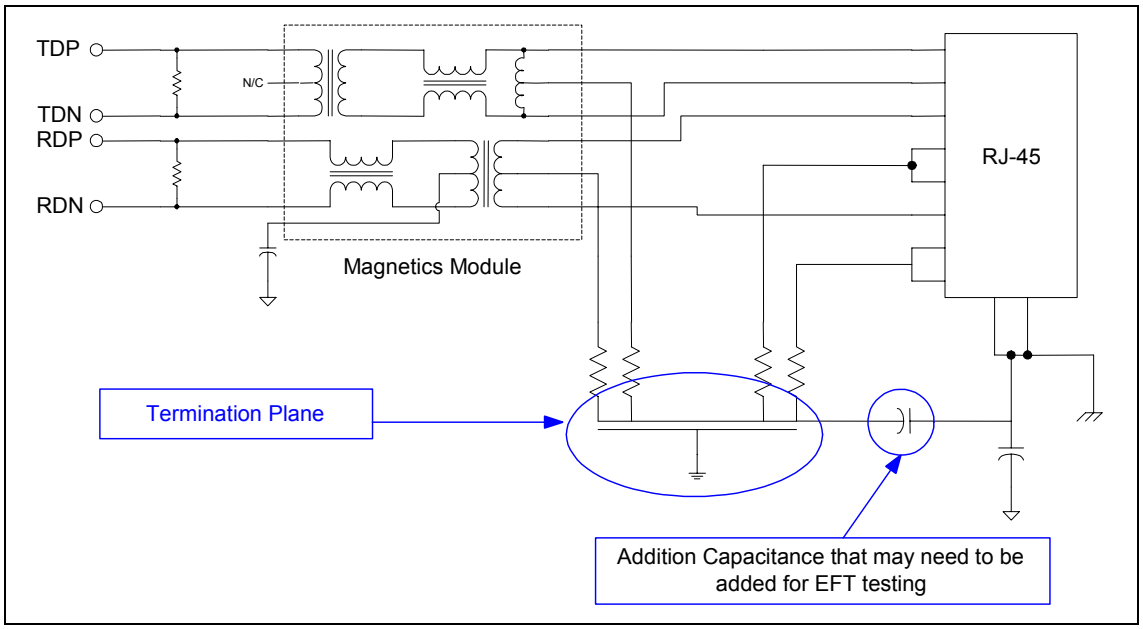
11.9.3.5.1. Terminating Unused Connections

In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75-Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

11.9.3.5.2. Termination Plane Capacitance

Intel recommends that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ-45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

Figure 117. Termination Plane

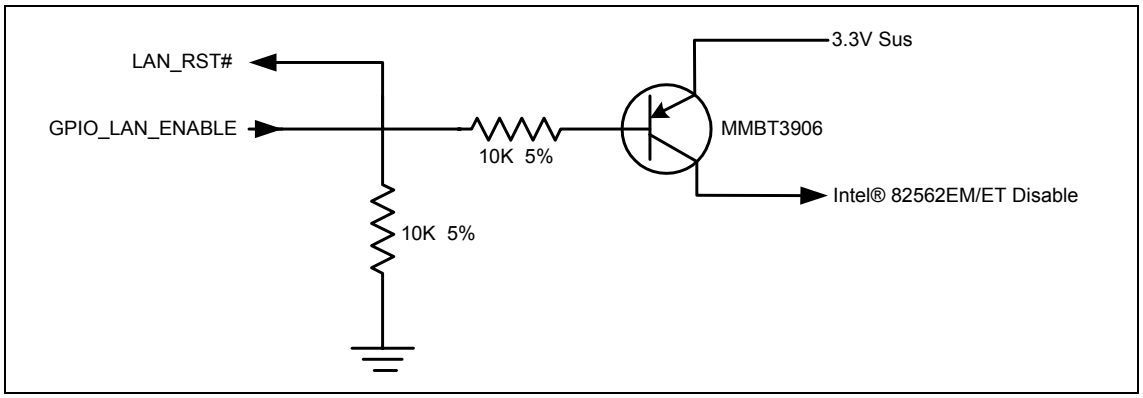


11.9.4. Intel 82562ET/EM Disable Guidelines

To disable the Intel 82562ET/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. The BIOS controlling the GPIO can disable the LAN micro-controller.

Note: LAN_RST# needs to be held low for 10ms after power is stable. It is assumed that RSMRST# logic will provide this delay. Because GPIO28 will default to high during power up, an AND gate has been implemented to ensure the required delay for LAN_RST# is met.

Figure 118. Intel 82562ET/EM Disable and Power Down Circuitry



There are four pins which are used to put the Intel 82562ET/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. The table below describes the operational/disable features for this design.

The four control signals shown in the below table should be configured as follows: Test_En should be pulled-down thru a 100-Ω resistor. The remaining 3 control signals should each be connected thru 100-Ω series resistors to the common node “Intel 82562ET/EM _Disable” of the disable circuit.

Table 97. Intel 82562ET/EM Control Signals

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

In addition, if the LAN Connect Interface of the ICH4-M is not used, the VccLAN1_5 and the VccLAN3_3 are still required to be powered during normal operating states. It is acceptable to power the VccLAN1_5 and VccLAN3_3 power pins by the same voltage source that supplies power to the Vcc1_5 and Vcc3_3 power pins. Also, the LAN_RST# pin of the ICH4-M should be pulled-down to GND with a 10-kΩ resistor to keep the interface disabled.

11.9.5. Design and Layout Consideration for Intel 82540EP / 82551QM

For specific design and layout considerations for the Intel 82540EP Gigabit Ethernet Controller and the Intel 82551QM Faster Ethernet Controller, please refer to the following documents:

- *82551QM / 82540EM Interchangeable LOM Design Application Note (AP 432) (Reference #10565)*
- *82540EP Gigabit Ethernet Controller Networking Silicon Product Preview Datasheet*
- *82540EP Gigabit Ethernet Controller Specification Update*
- *82540EP/82541EI & 82562EZ(EX) Dual Footprint Design Guide Application Note (AP-444) (Reference# 12504)*

11.9.6. General Intel 82562ET / 82562EM / 82551QM / 82540EP Differential Pair Trace Routing Considerations

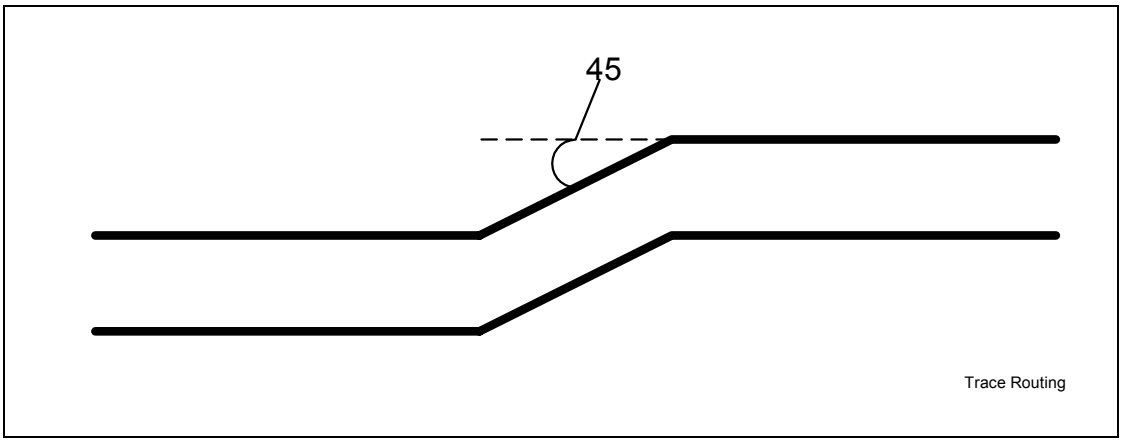
Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance.

Note: Some suggestions are specific to a 4.3-mil stack-up.

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).]
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to Figure 119.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 119. Trace Routing



11.9.6.1.1. Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

11.9.6.1.2. Signal Isolation

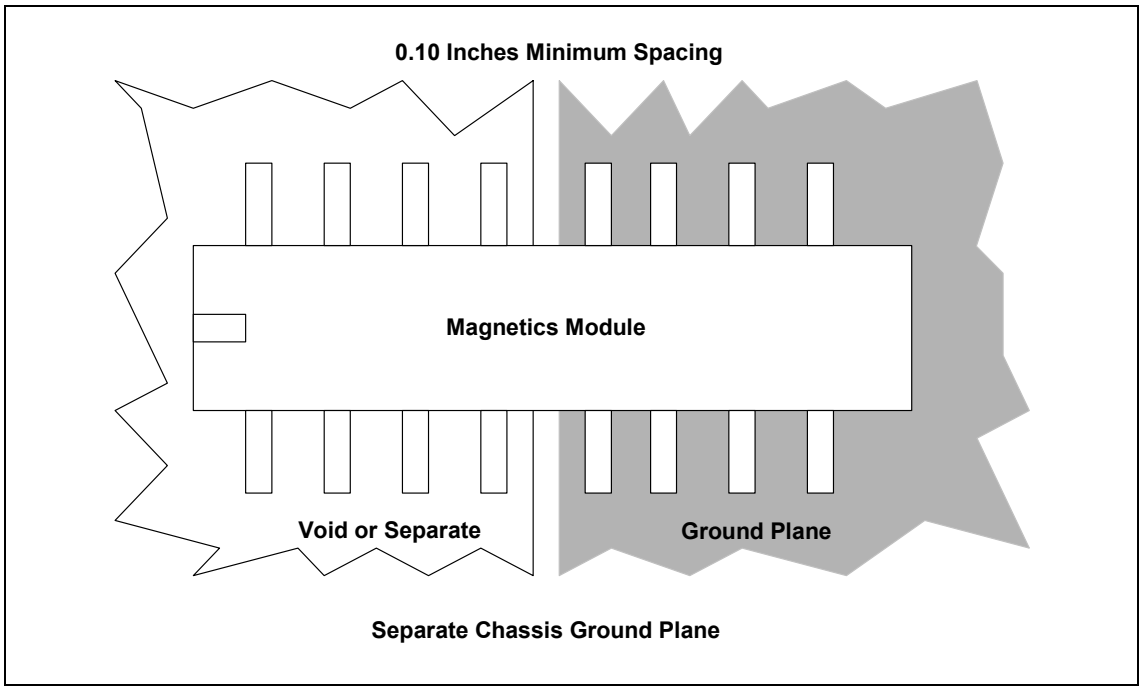
Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

11.9.6.1.3. Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum

Figure 120. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both back planes and motherboards.

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ-45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

11.9.6.2. Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. (Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (≤ one inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45, and the PLC.
6. Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
7. Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Please follow the appropriate reference schematic or App.-Note.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The App.-Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have ~100-Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they've designed for 100 Ω. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close† to each other, the edge coupling can lower the effective differential impedance by 5 Ω - 20 Ω. A 10-Ω - 15-Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.
10. Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetics' transmit center-tap (on the Intel 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail

at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These caps are not necessary, unless there is some overshoot in 100 Mbps mode.

Note: It is important to keep the two traces within a differential pair close† to each other. Keeping them close† helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e. FCC compliance) from the transmit traces, and better receive BER for the receive traces.

† Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

11.10. Power Management Interface

11.10.1. SYS_RESET# Usage Model

The System Reset signal (SYS_RESET#) of the ICH4-M can be connected directly to a reset button or any other equivalent driver in the system where the desired effect is to immediately put the system into reset. If an Intel Pentium M / Intel Celeron M processor ITP700FLEX debug port is implemented on the system, it is recommended that the DBR# signal of the ITP interface be connected to SYS_RESET# as well. If SYS_RESET# is implemented, a weak pull-up resistor pulled-up to the 3.3-V standby rail (VccSUS3_3) should also be implemented to ensure that no potential floating inputs to SYS_RESET# cause a system reset. The ICH4-M will debounce signals on this pin (16 ms) and allow the SMBus to go idle before resetting the system. This delay to allow all outstanding SMBus cycles to complete first and to prevent a slave device on the SMBus from “hanging” by resetting in the middle of an SMBus cycle.

11.10.2. PWRBTN# Usage Model

The Power Button signal (PWRBTN#) of the ICH4-M can be connected directly to a power button or any other equivalent driver (e.g. power management controller) where the desired effect is to indicate a system request to go to a sleep state (if in a normal operating mode) or to cause a wake event (if in a sleep state already). This signal is internally pulled-up in the ICH4-M to the 3.3-V standby rail (VccSUS3_3) through a weak pull-up resistor (20 kΩ nominal). The ICH4-M has 16ms of internal debounce logic on this pin.

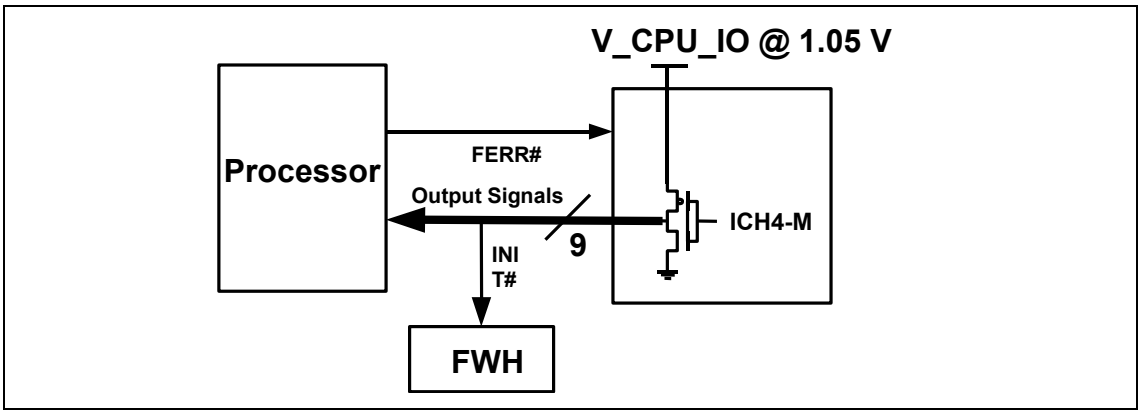
11.10.3. Power Well Isolation Control Strap Requirements

The RSMRST# signal of the ICH4 must transition from 20% signal level to 80% signal level and vice-versa in 50us. Slower transitions may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node can potentially cause the CMOS to be cleared or corrupted, the RTC to loose time after several AC power cycles, or the intruder bit might assert erroneously.

11.11. CPU I/O Signal Considerations

The Intel 82801DBM ICH4-Mhas been designed to be voltage compatible with the CMOS signals of the Intel Pentium M / Intel Celeron M processor. For Intel Pentium M / Intel Celeron M processor -based systems, the ICH4-M's V_CPU_IO rail uses the same 1.05-V voltage as the V_{CCP} rails for the processor the GMCH. It is important to verify that the voltage requirements of all CPU and ICH4-M signals are compatible with the FWH as well. See Section 11.7 for FWH details. Figure 121 shows a typical interface between the ICH4-M, CPU, and FWH. See Section 4.1.3.5 for recommended topologies and routing guidelines.

Figure 121. ICH4-M CPU I/O Signals with Processor and FWH



12. Platform Clock Routing Guidelines

12.1. System Clock Groups

The system clocks are considered as a subsystem in themselves. At the center of this subsystem is the Clock Synthesizer/Driver component. Several vendors offer suitable products, as defined in the Intel CK-408 Synthesizer/Driver Specification. This device provides the set of clocks required to implement a platform level motherboard solution. Table 98 below provides a breakdown of the various individual clocks.

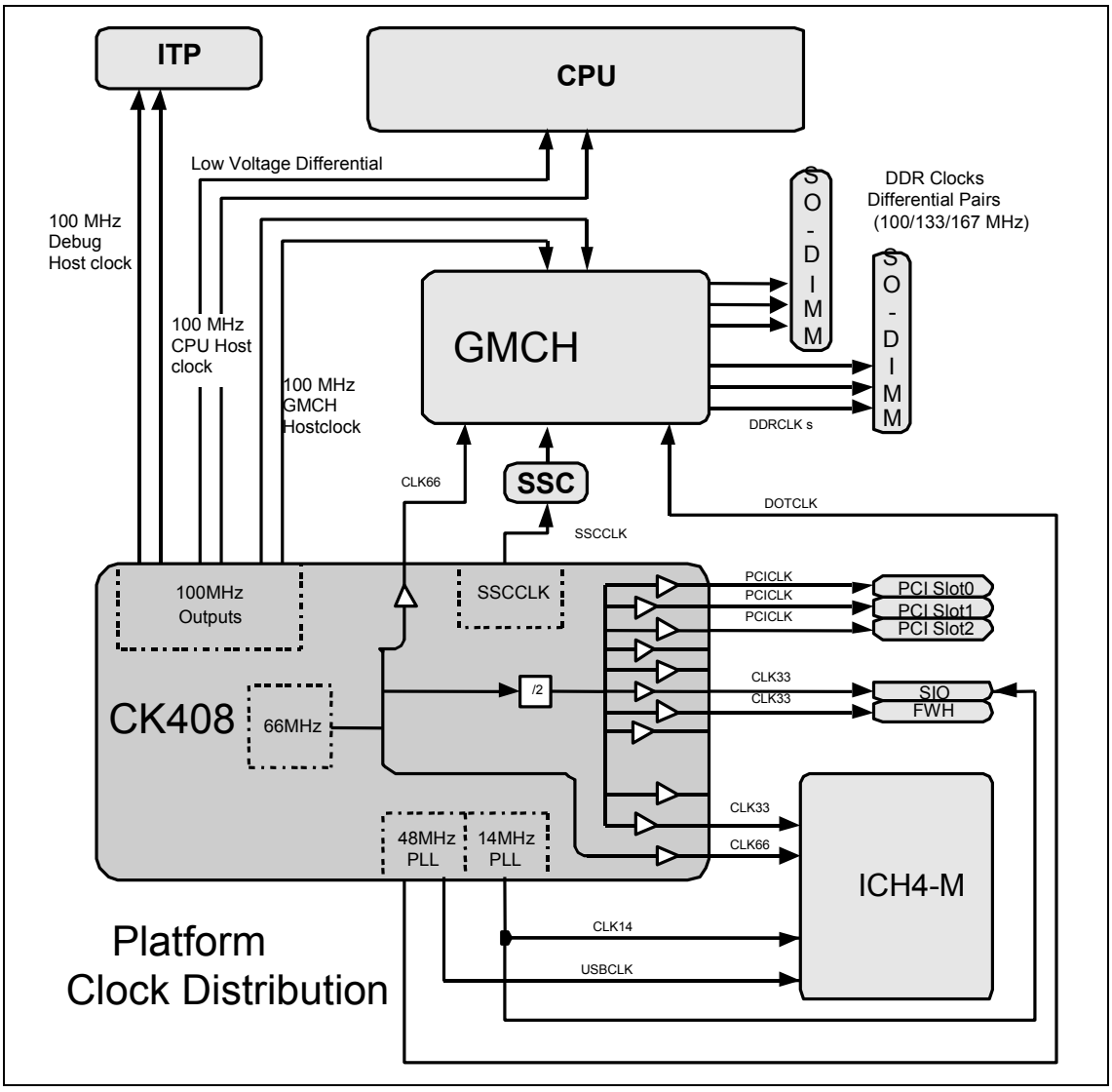
Note: When used in an Intel 855GM/GME chipset based system, the CK408 is configured in the unbuffered mode and has a host clock swing of 710 mV.

Table 98. Individual Clock Breakdown

Clock Group	Frequency	Driver/Pin	Receiver/s	Comments
HOST_CLK	100 MHz	CK408 CPU[2:0]	CPU GMCH Debug Port	Length matched Differential signaling (See 4.3 more details on Debug Port Clock routing)
CLK66	66 MHz	CK408 3V66[5:0]	GMCH ICH4-M	Length matched
CLK33	33MHz	CK408 PCIF[2:0]	ICH4-M	Length matched to CLK66 Synchronous but not edge aligned with CLK66 Phase delay of 1.5ns to 3.5ns
	MHz	CK408 PCI[6:0]	SIO FWH	
PCICLK (Expansion)	33 MHz	CK408 PCI[6:0]	PCI Conn #1 PCI Conn #2 PCI Conn #3	Length matched to CLK33 * * CLK33 length minus 2.5”
CLK14	14 MHz	CK408 REF0	ICH4-M SIO	Independent clock
DOTCLK	48 MHz	CK408 48 MHz	GMCH	Independent clock
SSCCLK	48/66 MHz	CK408 VCH	GMCH	Independent clock
USBCLK	48 MHz	CK408 48 MHz	ICH4-M	Independent clock

Figure 122 below depicts the system clock subsystem including the clock generator, major platform components, and all the related clock interconnects.

Figure 122. Clock Distribution Diagram



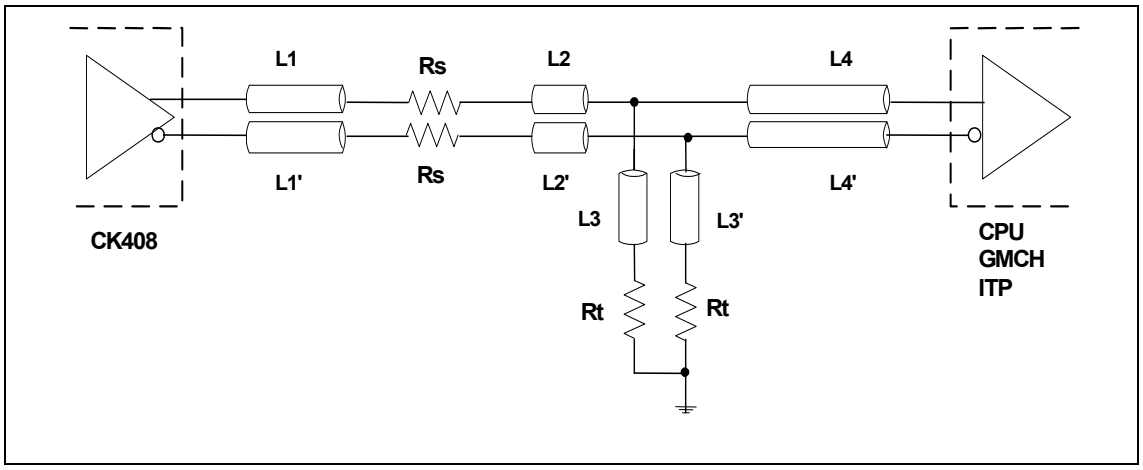
12.2. Clock Group Topologies and Routing Constraints

The topology diagrams and routing constraint tables provided on the following pages define the recommended topology and routing rules for each of the platform level clocks. These topologies and rules have been simulated and verified to produce the required waveform integrity and timing characteristics for reliable platform operation.

12.2.1. Host Clock Group

The clock synthesizer provides three pairs of 100-MHz differential clock outputs utilizing a 0.7-V voltage swing. The 100-MHz differential clocks are driven to the processor, the GMCH, and the processor debug port with the topology shown in the figure below. The host clocks are routed point to point as closely coupled differential pairs on the motherboard, with dedicated buffers for each of the three loads. These clocks utilize a Source Shunt Termination scheme as shown below.

Figure 123. Source Shunt Termination Topology



The clock driver differential bus output structure is a "Current Mode Current Steering" output which develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedances or to accommodate future load requirements.

The recommended termination for the differential bus clock is a "Source Shunt termination." Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The recommended value for Rt is a 49.9-Ω ±1% resistor. The tight tolerance is required to minimize crossing voltage variance. The recommended value for Rs is 33 Ω ± 5%. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

The MULT0 pin (CK408 pin #43) should be pulled-up through a 10 kΩ to VCC – setting the multiplication factor to 6.

The IREF pin (CK408 pin #42) should be tied to ground through a 475 Ω ± 1 % resistor – making the IREF 2.32 mA.

Table 99. Host Clock Group Routing Constraints

Parameter	Definition
Class Name	HOST_CLK
Class Type	Individual Differential Pairs
Topology	Differential Source Shunt Terminated
Reference Plane	Ground Referenced (contiguous over length)
Single Ended Trace Impedance (Zo)	55 Ω +/-15%
Differential Mode Impedance (Zdiff)	100 Ω +/- 15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Inner Layer Pair Spacing (edge to edge) (except as allowed below)	7.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Nominal Outer Layer Pair Spacing (edge to edge) (except as allowed below)	5.0 mils
Minimum Spacing to Other Signals	25 mils
Serpentine Spacing	25 mils
Maximum Via Count	5 (per side)
Series Termination Resistor Value	33 Ω +/- 5%
Shunt Termination Resistor Value	49.9 Ω+/- 1%
Trace Length Limits – L1 & L1'	Up to 500mils
Trace Length Limits – L2 & L2'	Up to 200 mils
Trace Length Limits – L3 & L3'	Up to 500 mils
Trace Length Limits – L4 & L4'	2.0" to 8.0"
Total Length Range– L1 + L2 + L4	2.0" to 8.5"
Length Matching Required	Yes (Pin to Pad)
HCLK to HCLK# Length Matching	+/- 10 mils (per segment) +/- 10 mils (overall)
CPU Clock to GMCH Clock Length Matching	Match HCLKs (pin to pad) +/- 20 mils Match L1 segment to +/- 10 mils across all pairs. (See Section 12.2.1.2.)
CPU Clock to ITP Clock Length Matching	Match CPU HCLKs + CPU BPM[3:0]# to ITP HCLKs +/- 250 mils (See Section 0)
Breakout Region Exceptions	No breakout exceptions allowed.

NOTES:
1. Differential pairs should be routed as a closely coupled side-by-side pair on a single layer over their entire length.
2. To minimize skew it is recommended that all clocks be routed on a single layer. If clock pairs are to be routed on multiple layers, the routed length on each layer should be equalized across all clock pairs.

3. To minimize skew it is recommended that all clock pairs be length matched from CK408 pin to CPU and GMCH die-pad, and length compensated on the motherboard for differences in package length and for socket/interposer effective length. A table of package lengths and equivalent socket lengths are provided.
4. The motherboard length of the ITP connector clock pair should be matched to the sum of the motherboard length of the CPU clock pair and the BPM[3:0]# signals.
5. A trace length offset (depends on CK408 vendor clock skew) between CLK66 going to the GMCH (GCLKIN) and HCLK going to the GMCH (BCLK) is recommended in order to prevent the CLK66 rising edge from occurring within the +/- 350ps keepout area on either side of the HCLK edge. See Section 12.2.1.3 for details.

12.2.1.1. Host Clock Group General Routing Guidelines

When routing the 100-MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.

If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.

Do not place vias between adjacent complementary clock traces. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

12.2.1.2. Clock to Clock Length Matching and Compensation

The HCLK pairs to the CPU and GMCH should be matched as close as possible in total length from CK408 pin to the die-pad of the receiving device. In addition, the L1/L1' segments of all three clock pairs should be length matched to within ± 10 mils. Pair to pair overall length matching requires knowledge of the package lengths of various CPUs, and the GMCH, as well as the effective length of the CPU socket/interposer if used. This information is provided in Table 100.

Once routing lengths are defined for the CPU and GMCH, match the motherboard length of the ITP clock pair to the motherboard length of the CPU clock pair.

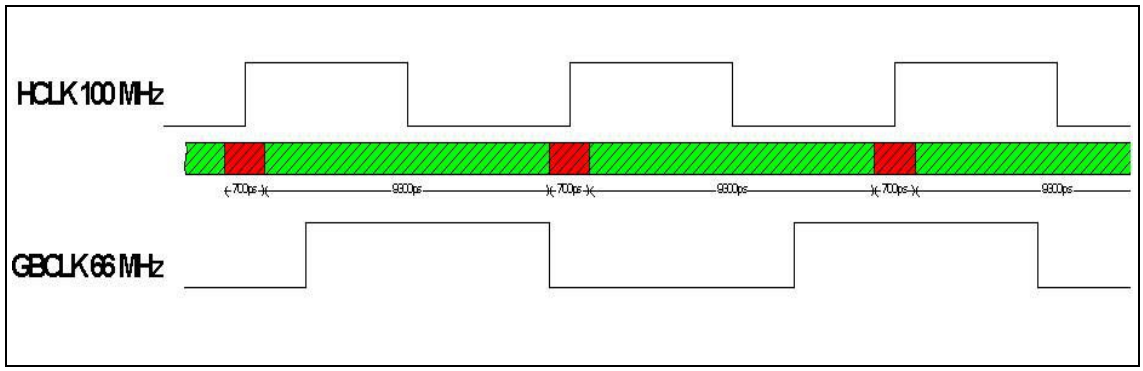
Table 100. Clock Package Length

Parameter	Length
Intel Pentium M Processor / Intel Celeron M Processor Package Length	485 mils
Intel 855GM/GME Chipset GMCH Package Length	1142 mils
CPU Socket Equivalent Length	157 mils

12.2.1.3. Host Clock to CLK66 Routing Recommendations

The rising edge of the HCLK (BCLK) input must either lead or lag the rising edge of CLK66 (GCLKIN) by more than 350 ps at the input balls of the GMCH as measured at the 50% point of each rising edge. Refer to Figure 124 for details.

Figure 124. BCLK to GCLKIN Timing Requirement



When assessing whether a system design meets the required BCLK/GCLKIN phase relationship, the following factors should be taken into account:

- Selected clock synthesizer chip's worst case (minimum) phase relationship between CLK66 (GCLKIN) and HCLKx (BCLK) rising edges. This includes the following clock timing parameters:
  - Min phase offset. Since the CK408 spec does not specify the phase offset between CLK66 and CPUx, the actual worst case (min) offset must be determined by consulting with the selected clock synthesizer chip's vendor.
  - Cycle-to-cycle jitter on each clock output. Max jitter is specified by the CK408 clock spec, but may be less than the max specified for any particular CK408 compatible clock synthesizer chip.
- Trace length difference between BCLK and GCLKIN routing.
- Board manufacturing variations affecting signal delay across clock traces.
- All relevant variables should be evaluated over the system's full specified operating temperature range.

12.2.1.4. EMI Constraints

Clocks are a significant contributor to EMI and should be treated with care. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to the VSS reference plane only.

12.2.2. CLK66 Clock Group

The 66-MHz clocks are series terminated and are routed point to point on the motherboard, with dedicated buffers for each of the loads. These clocks are all length tuned to match each other and as well as to the CLK33 clocks.

Figure 125. CLK66 Clock Group Topology

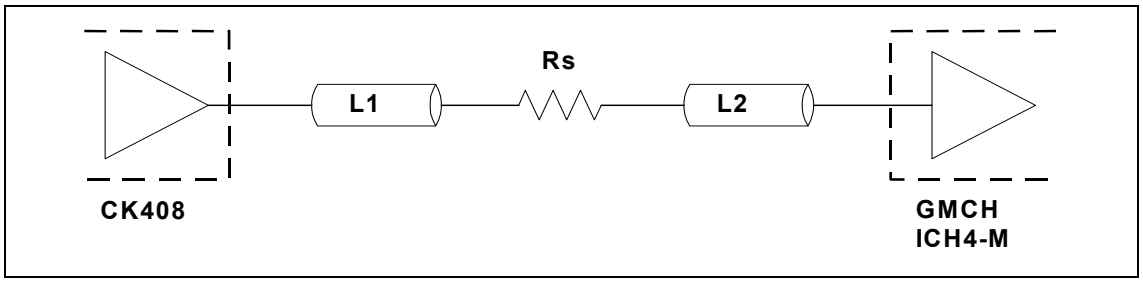


Table 101. CLK66 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK66
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω+/-15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω+/- 5 %
Trace Length Limits – L1	Up to 500mils (breakout segment)
Trace Length Limits – L2	4.0” to 8.5”
Total Length Range – L1 + L2	4.0” to 9.0”
Minimum Length Requirements	CLK66 < HCLK + X.X"
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	+/- 100 mils CLK66 to CLK66
Breakout Region Exceptions (Reduced spacing for GMCH & ICH breakout region)	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

NOTES:

1. The overall length of CLK66 is considered the reference length for CLK33 and PCICLK. The length of this clock should be set within the range and then used as the basis for defining the length of all other length matched clocks
2. A trace length offset (depends on CK408 vendor clock skew) between CLK66 going to the GMCH (GCLKIN) and HCLK going to the GMCH (BCLK) is recommended in order to prevent the CLK66 rising edge from occurring within the +/- 350ps keepout area on either side of the HCLK edge. See Section 12.2.1.3 for details.

12.2.3. CLK33 Clock Group

The 33-MHz clocks are series terminated and routed point to point on the motherboard with dedicated buffers for each of the loads. These clocks are length tuned to match the CLK66 clocks, however, they are out of phase due to an internal phase delay in the CK408.

Figure 126. CLK33 Group Topology

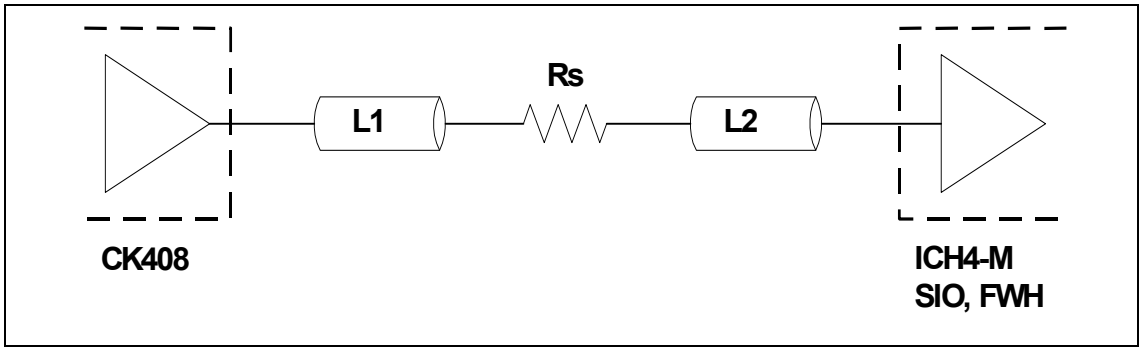


Table 102. CLK33 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK33
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω+/-15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω+/- 5 %
Trace Length Limits – L1	Up to 500mils
Trace Length Limits – L2	4.0” to 8.5”
Total Length Range – L1 + L2	CLK66 Length
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Matching	+/- 100 mils CLK33 to CLK66
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

12.2.4. PCI Clock Group

The PCI clocks are series terminated and routed point to point as on the Inter reference motherboard between the CK408 and the PCI connectors, with a dedicated buffer for each slot. These clocks are synchronous to the CLK33 clocks and are length tuned to compensate for the segment on the PCI daughter card.

Figure 127. PCI Clock Group Topology

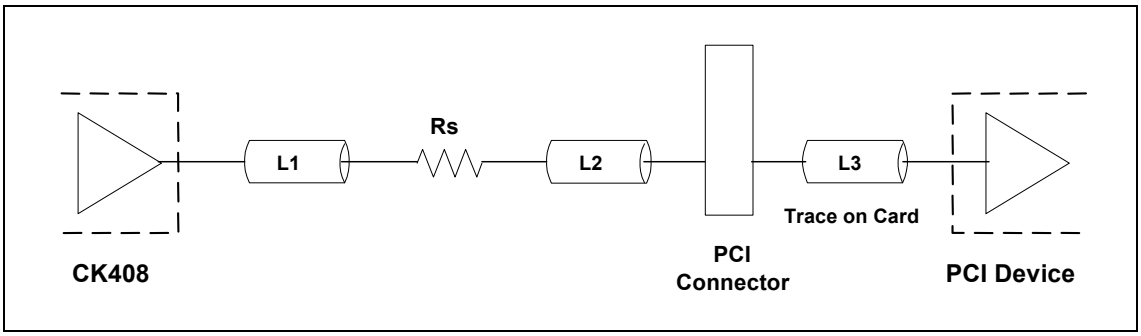


Table 103. PCICLK Clock Group Routing Constraints

Parameter	Definition
Class Name	PCICLK
Class Type	Individual Nets
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω+/-15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω+/- 5 %
Trace Length Limits – L1	Up to 500 mils (breakout segment)
Trace Length Limits – L2	1.5” to 8.0”
Trace Length Limits – L3	2.5” (as per PCI specification)
Total Length Range – L1 + L2 + L3	CLK33 – 2.5” (for nominal matching)
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	+/- 2.0” PCICLK to (CLK33 – 2.5”)
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

12.2.5. CLK14 Clock Group

The 14-MHz clocks are series terminated and routed point to point on the motherboard. A single clock output is shared between the two loads. These clocks are length tuned to each other but are not synchronous with any other clocks.

Figure 128. CLK14 Clock Group Topology

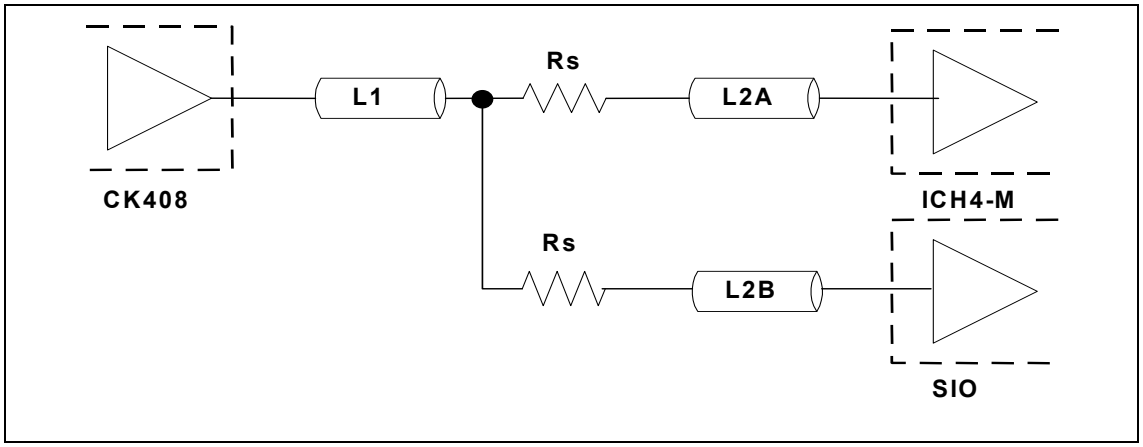


Table 104. CLK14 Clock Group Routing Constraints

Parameter	Definition
Class Name	CLK14
Class Type	Individual Nets
Topology	Dual Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω+/-15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	20 mils
Serpentine Spacing	20 mils
Maximum Via Count	4 (per driver/receiver path)
Series Termination Resistor Value	33 Ω+/- 5 %
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2A, L2B	2.0” to 8.5”
Total Length Range – L1 + L2A & L1 + L2B	2.0” to 9.0”
Length Matching Required	Yes (Pin to Pin)
Clock to Clock Length Matching	+/- 500 mils CLK14A to CLK14B
Breakout Region Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

12.2.6. DOTCLK Clock Group

The 48-MHz DOTCLK is series terminated and routed point to point on the motherboard. This clock operates independently and is not length tuned to any other clock.

Figure 129. DOTCLK Clock Topology

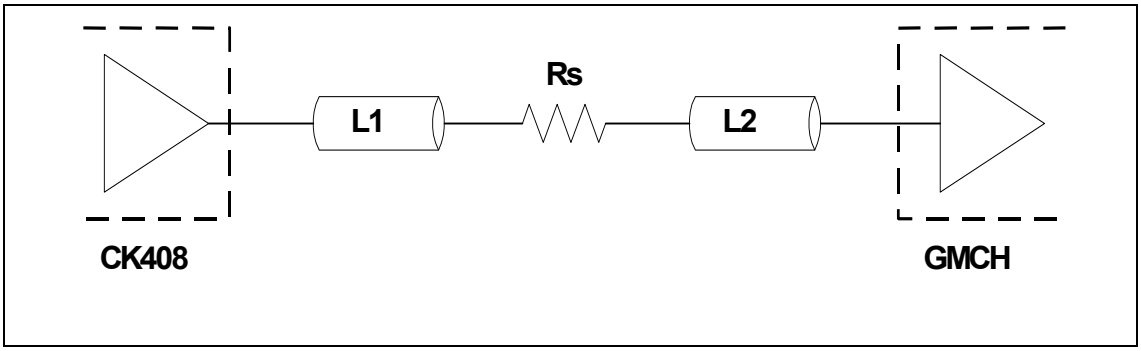


Table 105. DOTCLK Clock Routing Constraints

Parameter	Definition
Class Name	DOTCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω+/-15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	25 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω+/- 5 %
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	2.0” to 8.0”
Total Length Range – L1 + L2	2.0” to 8.5”
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

NOTE: The DOTCLK is used internally by the GMCH to generate the pixel clock and must exhibit very low jitter. Care should be taken to avoid routing through noisy areas and spacing rules should be observed. Guard traces may be employed if necessary with ground stake vias on no less than 0.5- inch intervals.

12.2.7. SSCCLK Clock Group

The 48/66-MHz SSCCLK operates independently and is not length tuned to any other clock. This clock employs a spread-spectrum device in its path to reduce EMI. The overall clock path is divided into two segments as shown in Figure 130, with each segment series terminated and routed point to point.

Figure 130. SSCCLK Clock Topology

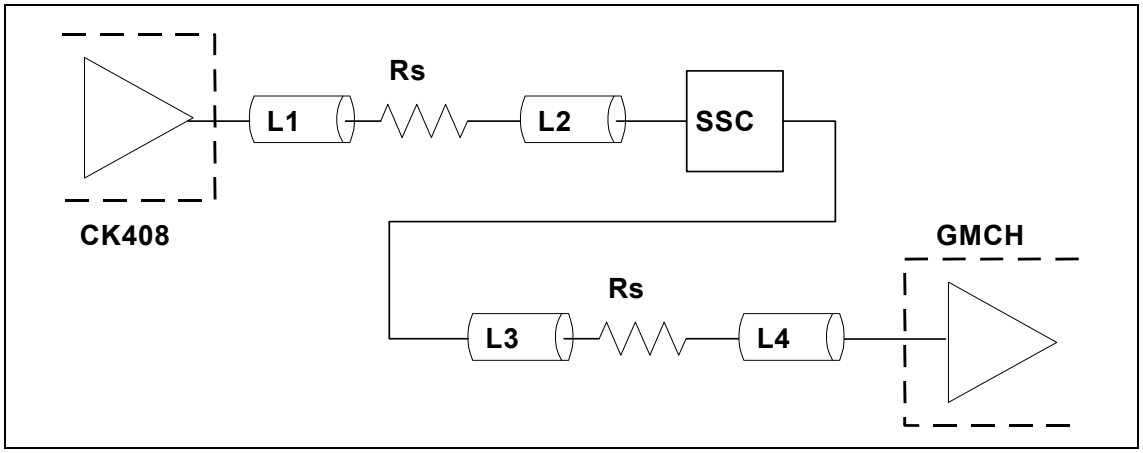


Table 106. SSCCLK Clock Routing Constraints

Parameter	Definition
Class Name	SSCCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω+/-15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	20 mils
Maximum Via Count	4 (per driver/receiver path)
Series Termination Resistor Value	33 Ω+/- 5 %
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	1.0” to 4.0”
Trace Length Limits – L3	Up to 500 mils
Trace Length Limits – L4	1.0” to 7.0”
Total Length Range – L1 + L2 + L3 + L4	3.0” to 8.5”
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

12.2.8. USBCLK Clock Group

The 48-MHz USBCLK is series terminated and routed point to point on the motherboard. This clock operates independently and is not length tuned to any other clock.

Figure 131. USBCLK Clock Topology

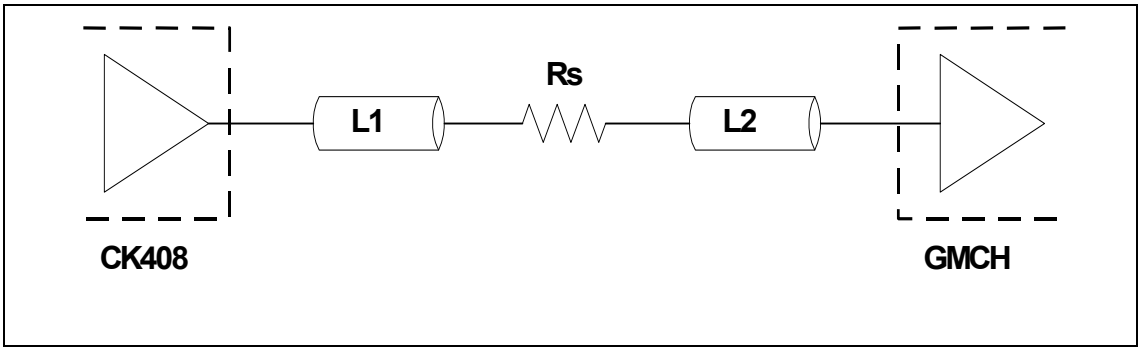


Table 107. USBCLK Clock Routing Constraints

Parameter	Definition
Class Name	USBCLK
Class Type	Individual Net
Topology	Series Terminated Point to Point
Reference Plane	Ground Referenced
Single Ended Trace Impedance (Zo)	55 Ω+/-15%
Nominal Inner Layer Trace Width	4.0 mils
Nominal Outer Layer Trace Width	5.0 mils (pin escapes only)
Minimum Spacing (see exceptions below)	20 mils
Maximum Via Count	4
Series Termination Resistor Value	33 Ω+/- 5 %
Trace Length Limits – L1	Up to 500 mils
Trace Length Limits – L2	3.0” to 12.0”
Total Length Range – L1 + L2	3.0” to 12.5”
Length Matching Required	No
Breakout Exceptions	5 mil trace with 5 mil space on outers 4 mil trace with 4 mil space in inners Maximum breakout length is 0.3”

12.3. CK-408 Clock Updates for Intel Pentium M Processor and Intel Celeron M Processor Platforms

To maximize the power savings on 855GM chipset based systems, additional control registers have been added to the CK-408clock generator to allow option to tri-state the CPU[2:0] host clocks during CPU_STOP# or PWRDWN assertion. The option to have CPU[2:0] driven (default) or tri-stated can be programmed via the serial I^2C bus interface to the CK-408 clock driver. If the tri-state feature on the CPU[2:0] signals is chosen, it is recommended that the STP_CPU# signal from the Intel ICH4-M drive the CK-408's CPU_STOP# signal. Also, it is recommended that the ICH4-M's DPSLP# signal be connected to the DPSLP# pin of the processor and GMCH. Functionally, the ICH4-M's STP_CPU# and DPSLP# signals are equivalent. However, STP_CPU# is powered by the main I/O well (3.3 V) and is sent to the CK-408 whereas DPSLP# is driven to the processor interface voltage (1.05 V).

12.4. CK-408 PWRDWN# Signal Connections

For systems that support the S1M state, the PWRDWN# input of the CK-408 clock chip is **required** to be driven by **both** the SLP_S1# and SLP_S3# signals from the ICH4-M, i.e. the PWRDWN# pin of the CK-408 should be driven by the output of the logical AND of the SLP_S1# and SLP_S3# signals. This configuration best allows CPU[2:0] to be tri-stated during S1-M or lower (numerically higher) states.

For systems that do not support S1M but do support the S3 state, the PWRDWN# input of the CK-408 clock chip should be connected to the SLP_S3# output of the ICH4-M. It is **not** recommended that PWRDWN# be pulled-up to the CK-408's 3.3-V power supply if the S3 state is the second highest, power consuming state supported by the platform (i.e. S1M and S2 not supported). The advantage of using SLP_S3# rather than the 3.3-V supply to qualify PWRDWN# is that it reduces the likelihood of the CK-408 clocks driving into unpowered components and potentially damaging the clock input buffers. Also SLP_S3# can help reduce power consumption because it will be asserted before the 3.3-V supply will be shut off, thus minimizing the amount of time that the clocks will be left toggling.

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13. Intel 855GM/GME Chipset Based System Power Delivery Guidelines

13.1. Definitions

Table 108. Power Delivery Definitions

Term	Definition
S0/Full-On operation:	During S0 operation, all components on the motherboard are powered and the system is fully functional.
S1-M/Power-On-Suspend (POS, Mobile):	In the mobile implementation of the Power-On-Suspend state, the outputs of the clock chip are stopped in order to save power. All components remain powered but may or may not be in a low power state.
S3/Suspend-To-RAM (STR):	In the S3 state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered.
S4/Suspend-To-Disk (STD):	In the S4 state, the system state is stored in non-volatile secondary storage (e.g. a hard disk) and all unnecessary system logic is turned off. Only logic required to wake the system remain powered. Standby power rails may or may not be powered depending on system design and the presence of AC or battery power.
S5/Soft-Off:	The S5 state corresponds to the G2 state. Restart is only possible with the power button.
Full-Power operation:	During Full-Power operation, all components remain powered. Full-power operation includes both S0 and the S1M (CPU Stop-Grant state).
Suspend operation:	855GM/GME chipset-based systems can be designed to support a number of suspend states such as Power-On-Suspend (S1M), Suspend-to-RAM (S3), Suspend-to-Disk (S4), and Soft-Off (S5). During suspend operation, with exception of S1M, power is removed from some components on the motherboard.
Core power rail:	A power rail that is only on during full-power operation.
Standby power rail:	A power rail that is on during a suspend operation (S3, S4 or S5). The rail is also on during full-power operation.
Derived power rail:	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3 V_{SB} is usually derived (on the motherboard) from 5 V_{SB} using a voltage regulator.

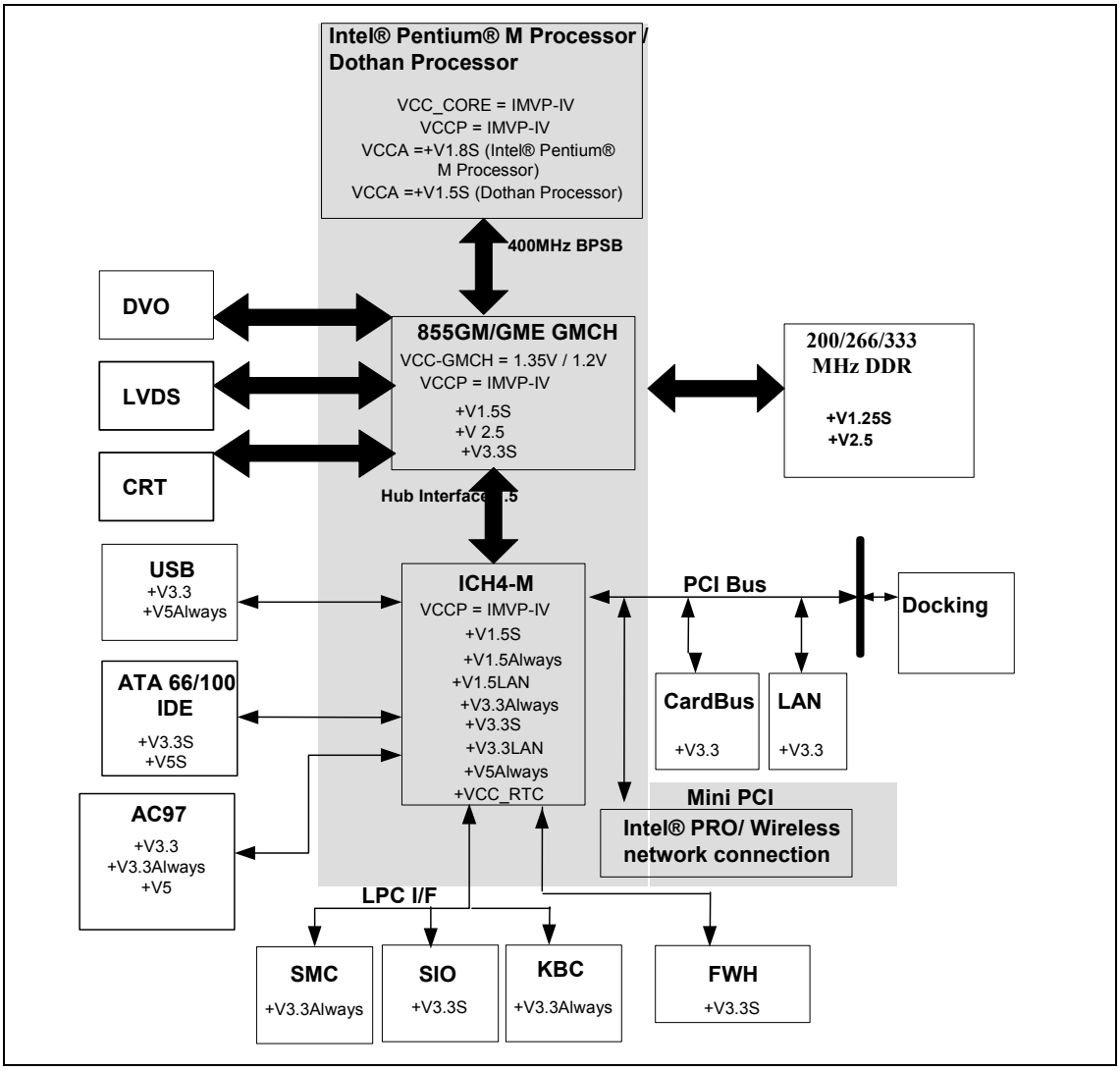
13.2. Platform Power Requirements

The following figure shows the power delivery architecture for an example of the Intel 855GM/GME chipset based system. To ensure that enough power is available during S3, a thorough power budget should be completed. The power requirements should include each device's power requirements, both in *suspend* and in *Full-On*. The power requirements should be compared against the power budget supplied by the power supply.

The solutions given in this document are only examples. There are many power distribution methods that achieve similar results. It is critical, when deviating from these examples, to consider the effect of the change.

13.2.1. Platform Power Delivery Architectural Block Diagram

Figure 132. Platform Power Delivery Map



13.3. Voltage Supply

13.3.1. Power Management States

Table 109. Power Management States on Intel Reference Board

Signal	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*	+V*S	Clocks
S0 (FULL ON)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M (POS)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (STR)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (STD)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

13.3.2. Power Supply Rail Descriptions

Table 110. Power Supply Rail Descriptions on Intel Reference Board

Signal Names	Voltage (V)	Current (A)	Tolerance	Enable	Description
+V1_25	1.25	0.01	+/- 3.2%	SLP_S3# - HIGH	GMCH, DDR Termination
				SLP_S4# - HIGH	DDR Reference (VREF)
+V1_5	1.5	0.03	+/- 5%	SLP_S4# - HIGH	LAN logic CPU VCCA (Intel Pentium M Processor on 90 nm Process with 2 MB L2 Cache only)
+V1_5S	1.5	1.35	+/- 5%	SLP_S3# - HIGH	GMCHDVO-Core, GMCH DLVDS, GMCH DAC, GMCH ALVDS, ICH4-M core, ICH4-M VCCHL
+V1_5ALWAYS	1.5	0.1	+/- 5%	+V3ALWAYS	ICH4-M Resume
+V1_8S	1.8	0.6	+/- 5%	SLP_S3# - HIGH	CPU VCCA (Intel Pentium M Processor only)
+V1_2S for 855GM +V1_35S for 855GME	1.2 1.35	1.8	+/- 5%	SLP_S3# - HIGH	GMCH Core, GMCH HL, GMCH DPLL, GMCH HPLL, GMCH GPLL, GMCH VCCASM
+V2_5	2.5	8.12	+/- 5%	SLP_S4# - HIGH	GMCH DDR I/O, DDR SO-DIMM, GMCH TXLVDS[1]

Signal Names	Voltage (V)	Current (A)	Tolerance	Enable	Description
+V3ALWAYS	3.3	0.4	+/- 5%	+VDC_ON	ICH4-M Resume, SMC/KBC, AC'97
+V3	3.3	0.9	+/- 5%	SLP_S5# - HIGH	ICH4-M LAN I/O, AC'97, RS232
+V3S	3.3	7.0	+/- 5%	SLP_S3# - HIGH	GMCH GPIO, ICH4-M I/O, CK-408, FWH, SIO,PCI
+V5	5	9.0	+/- 5%	SLP_S5# - HIGH	AC'97,
+V5S	5	1.0	+/- 5%	SLP_S3# - HIGH	ICH4-M VREF, MSE/KBD, FDD, IDE, PCI
+V5ALWAYS	5	3.0	+/- 5%	+VDC	ICH4-M VREFSUS, USB Supply
+V12S	12	0.2	+/- 5%	SLP_S3# - HIGH	PCI, IDE
+VCC_CORE	0.844 - 1.356	32	±1.5% (static)	VID	Intel Pentium M / Intel Celeron M processor core voltage by IMVP-IV VR ± 10 mV (ripple & transient)
+VCCP	1.05	2.4	+/- 5%	VR_ON	Intel Pentium M / Intel Celeron M processor I/O voltage by IMVP-IV VR

NOTE: GMCH VREF, DDR memory VREF, DDR termination, and GMCH TXLVDS can be turned off during S3. However, for some DDR memory devices may require a valid reference voltage during S3.

13.4. 855GM/GME Chipset Based System Power-Up Sequence

The following sections describe the power-up timing sequence for Intel 855GM/GME chipset GMCH based platforms.

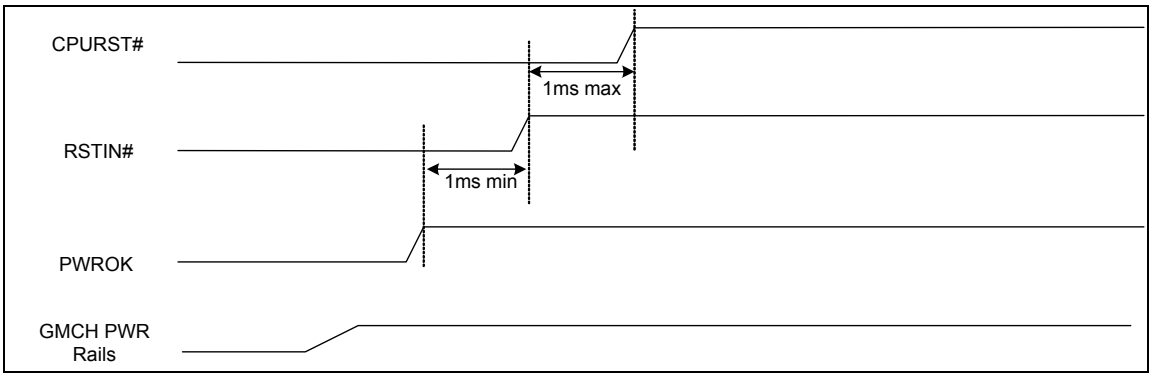
13.4.1. Processor Power Sequence Requirement

Contact your Intel Field Representative for details on the Intel Pentium M processor or Intel Celeron M processor with IMVP-IV voltage regulator..

13.4.2. GMCH Power Sequencing Requirements

All GMCH power rails should be stable before PWROK is asserted. The power rails can be brought up in any order desired. **However, good design practice would have all GMCH power rails come up as close in time as practical, with the core voltage (1.2 V for 855GM / 1.35 V for 855GME) coming up first.** RSTIN#, which brings GMCH out of reset, should be deasserted only after PWROK has been active for 1 ms. Once GMCH is out of reset, it will deassert CPURST# within 1 ms.

Figure 133. GMCH Power-Up Sequence



13.4.3. ICH4-M Power Sequencing Requirements

The following figure describes the power-on timing sequence for ICH4-M. The VGATE input should be connected to the processor voltage regulator PWRGD output. When both PWROK and VGATE are asserted, it indicates that core power and system power are stable and PCIRST# will be de-asserted a minimum of 1 ms later. It is the responsibility of the system designer to ensure that the power and timing requirements for the processor and GMCH are met.

Please refer to *Intel® 82801DBM I/O Controller Hub 4-Mobile (ICH4-M) Datasheet* for more details.

Figure 134. ICH4-M Power-Up Sequence

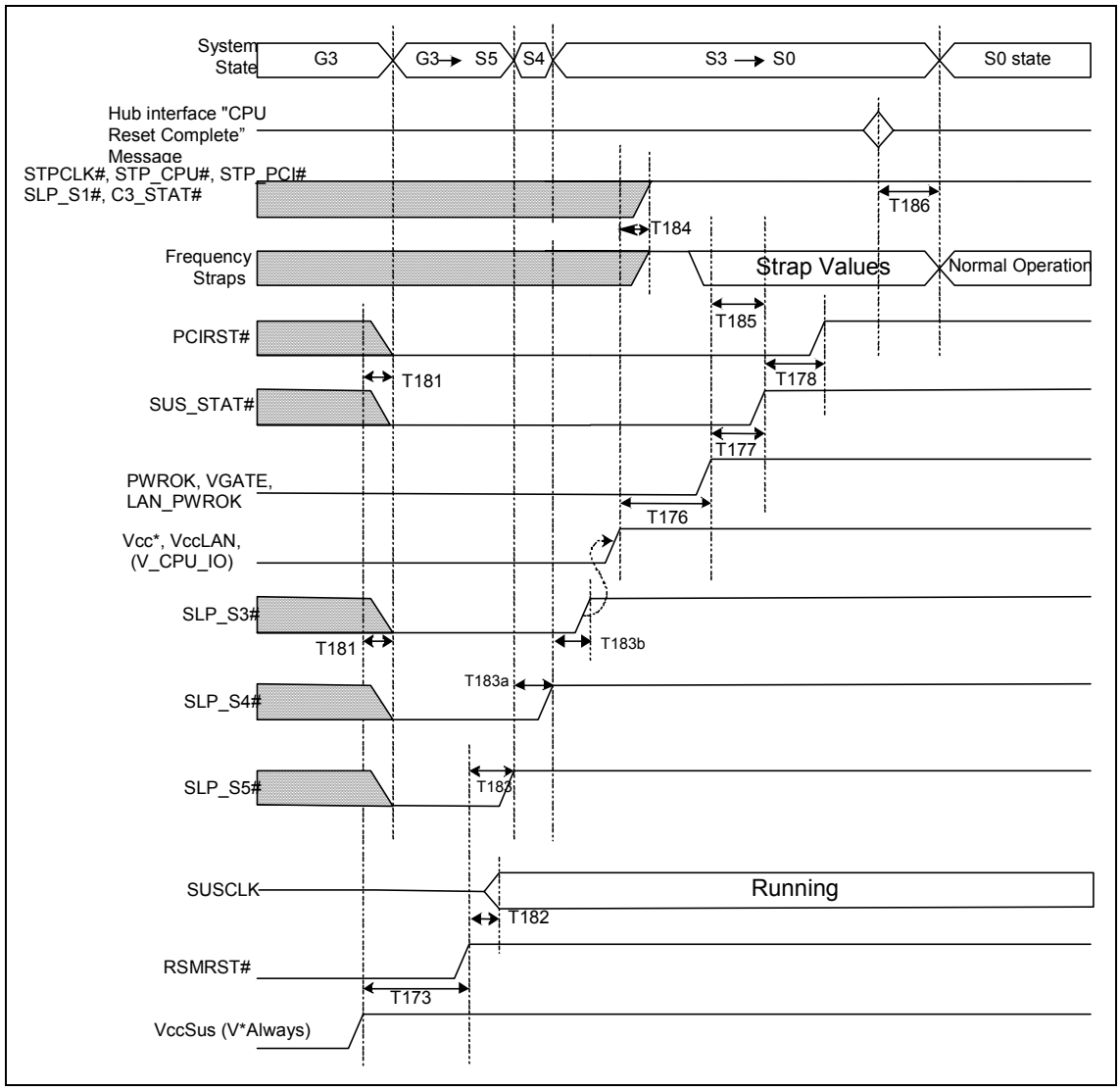


Table 111. Timing Sequence Parameters ICH4-M

Sym	Description	Min	Max	Units	Notes
T173	VccSus supplies active to RSMRST# inactive	10	-	ms	
T176	Vcc1.5, Vcc3.3, VccHI, V_CPU_IO supplies active to PWROK, VGATE active	10	-	ms	
T177	PWROK and VGATE active and SYS_RESET# inactive to SUS_STAT# inactive	32	38	RTCCLK	2
T178	SUS_STAT# inactive to PCIRST# inactive	1	3	RTCCLK	2
T181	VccSus active to SLP_S5#, SUS_STAT# and PCIRST# active		50	ns	
T182/T183	RSMRST# inactive to SUSCLK running, SLP_S5# inactive		110	ms	1
T183a	SLP_S5# inactive to SLP_S4# inactive	1	2	RTCCLK	2
T183b	SLP_S4# inactive to SLP_S3# inactive	1	2	RTCCLK	2
T184	V_CPU_IO active to STPCLK#, CPUSLP#, STP_CPU#, STP_PCI#, SLP_S1#, C3_STAT# inactive, and CPU Frequency Strap signals high		50	ns	
T185	PWROK and VGATE active and SYS_RESET# inactive to SUS_STAT# inactive and CPU Frequency Straps latched to strap values	32	38	RTCCLK	2
T186	CPU Reset Complete to Frequency Straps signals unlatched from strap values	7	9	CLK66	3

NOTES:
1. If there is no RTC battery in the system, so VccRTC and the VccSus supplies come up together, the delay from RTCRST# and the RSMRST# inactive to SUSCLK toggling may be as much as 1000 ms.
2. These transitions are clocked off the internal RTC. 1 RTC clock is approximately 32 µs.
3. This transition is clocked off the 66-MHz CLK66. 1CLK66 is approximately 15 ns.

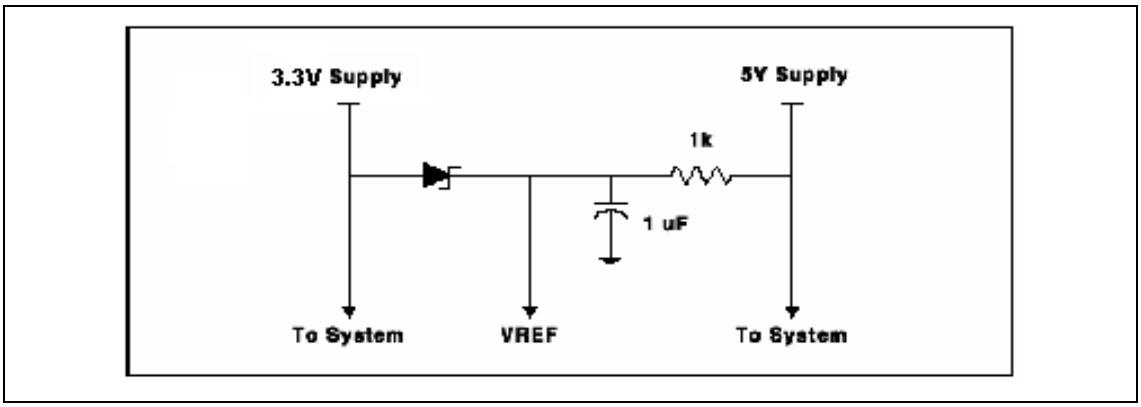
13.4.3.1. 3.3/1.5 V Power Sequencing

No power sequencing requirements exist for the associated 3.3 V/1.5 V rail of the ICH4-M chip. It is generally good design practice to power up the core before or at the same time as the other rails.

13.4.3.2. V_{5REF} Sequencing

V_{5REF} is the reference voltage for 5-V tolerance on inputs to the Intel ICH4-M. V_{5REF} must be powered up before V_{CC3_3}, or after V_{CC3_3} within 0.7 V. Also, V_{5REF} must power down after V_{CC3_3}, or before V_{CC3_3} within 0.7 V. These rules must be followed in order to ensure proper functionality of the Intel ICH4-M. Figure 135 shows a sample implementation of how to satisfy the V_{5REF}/ 3.3 V sequencing rule.

Figure 135. Example V_{5REF} / $V_{5REFSUS}$ Sequencing Circuitry



13.4.3.3. $V_{5REFSUS}$ Design Guidelines

The aforementioned rule for V_{5REF} also applies to the V_{5REF_SUS} input pin. However, in some platforms, the V_{CCSUS3_3} rail is derived from the V_{CCSUS5} and therefore, the V_{CCSUS3_3} rail will always come up after the V_{CCSUS5} rail. As a result, V_{5REF_SUS} will always be powered up before V_{CCSUS3_3}. In platforms where the V_{CCSUS3_3} rail is not derived from the V_{CCSUS5} rail, the V_{5REF} sequencing rule must be comprehended in the platform design.

In order to meet reliability and testing requirements for the USB interface, the following design recommendations for the V_{5REF_SUS} pins of the ICH4-M should be followed. There are changes to the USB specification regarding continuous short conditions must be addressed. The USB 1.1 specification requires host controllers to withstand a continuous short between the USB 5-V connector supply and a USB signal at the connector. However, the duration is unspecified. The USB 2.0 specification requires this duration to be at least 24 hours. This in turn requires that the $V_{5REFSUS}$ pin be at 5 V as long as the attached USB devices are powered. The recommendation is to provide a +V5ALWAYS (active S0-S5) supply to the $V_{5REFSUS}$ pin if available as shown in Figure 136. However, if support for wake on USB from S3 and support for self-powered USB devices are not required, then option shown in Figure 137 can be used. $V_{5REFSUS}$ can be supplied by combination of +V5S (active in S0 only) and +V3ALWAYS (active S0-S5).

Figure 136. V5REFSUS With +V5ALWAYS Connection Option

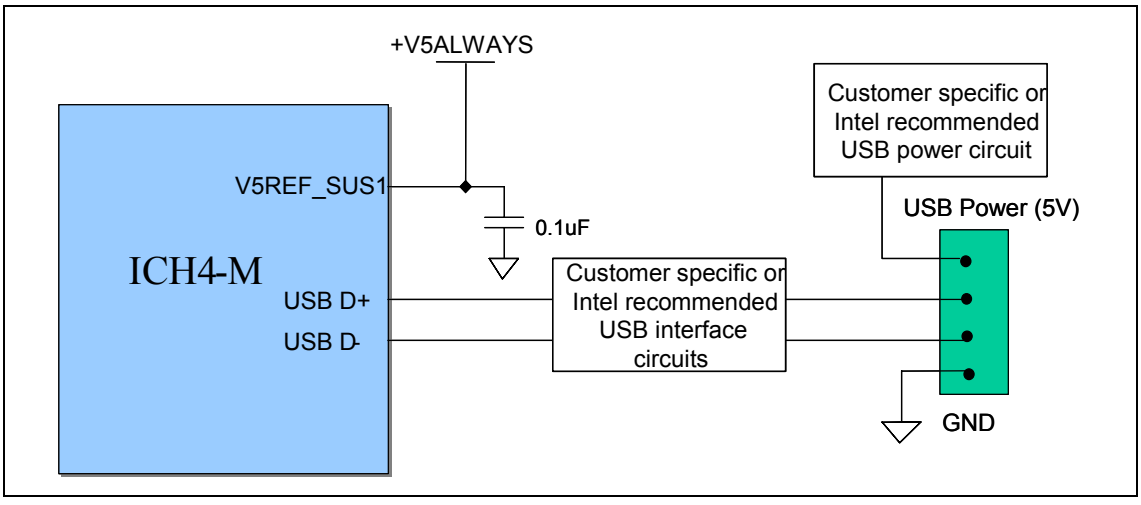
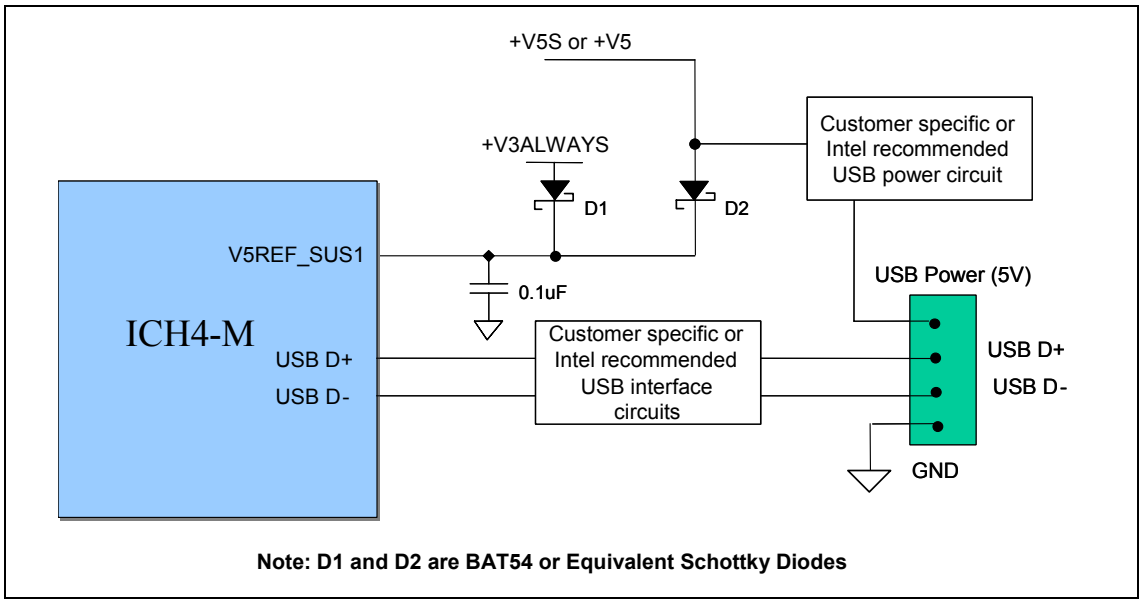


Figure 137. V5REFSUS With +V3ALWAYS and +V5S or +V5 Connection Option



13.4.4. DDR Memory Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements are specified during power up or power down if the following criteria are met:

- VDD and VDDQ to memory devices are driven from a single power converter output.
- VTT is limited to 1.44 V (reflecting VDDQ(max)/2 + 50 mV VREF variation + 40 mV VTT variation)
- VREF tracks VDDQ/2
- A minimum resistance of 42 Ω (22 Ω series resistor + 22 Ω parallel resistor ± 5% tolerance) limits the input current from the VTT supply into any pin.

If the above criteria cannot be met by the system design, then the following Table 112 must be adhered to during power up. Refer to *Intel® DDR 200 JEDEC Spec Addendum* for more details.

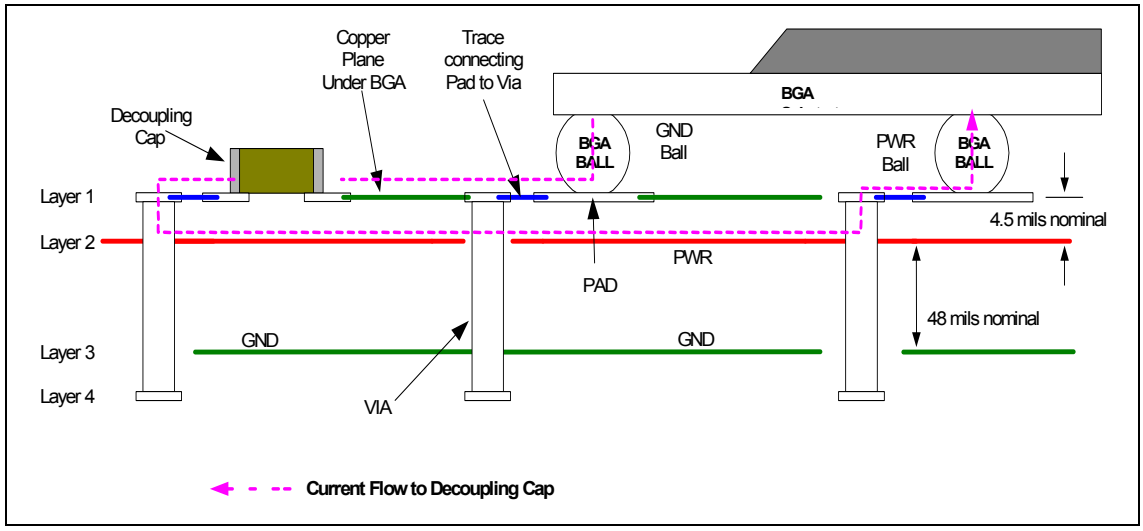
Table 112. DDR Power-Up Initialization Sequence

Voltage Description	Sequencing	Voltage Relationship to Avoid Latch-up
VDDQ	After or with VDD	< VDD + 0.3 V
VTT	After or with VDDQ	< VDDQ + 0.3 V
VREF	After or with VDDQ	< VDQ + 0.3 V

13.5. Intel 855GM/GME Chipset Based System Power Delivery Guidelines

Each component is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of decoupling capacitors specified in this document to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible. Rotate caps that set over power planes so that the loop inductance is minimized (see Figure 138). The basic theory for minimizing loop inductance is to consider which voltage is on Layer 2 (power or ground) and spin the decoupling cap with the opposite voltage towards the BGA (Ball Grid Array). This greatly minimizes the total loop inductance. Intel recommends that for prototype board designs, the designer should include pads for extra power plane decoupling caps.

Figure 138. Example for Minimizing Loop Inductance



13.5.1. 855GM/GME Chipset GMCH Decoupling Guidelines

Decoupling in Table 15 is based on voltage regulator solution used on the customer reference board design.

Table 113. GMCH Decoupling Recommendations

Pin Name	Configuration	F	Qty	TYPE	Notes
VCC	Connect to VCC1_2S for 855GM Connect to VCC1_35S for 855GME	0.1 µF 10 µF 150 µF	4 1 2	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	1 X 0.1 µF within 200 mils 3 X 0.1 µF on bottom side
VTTLF	Connect to VCCP	0.1 µF 10 µF 150 µF	2 1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	2 X 0.1 µF on bottom side
VTTHF	Connect to caps directly	0.1 µF	5	XR7, 0603, 16 V, 10%	
VCCHL	Connect to VCC1_2S for 855GM Connect to VCC1_35S for 855GME	0.1 µF 10 µF	2 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20%	1 X 0.1 µF within 200 mils 1 X 0.1 µF on bottom side
VCCSM	Connect to VCCSus2_5	0.1 µF 150 µF	11 2	XR7, 0603, 16 V, 10% TANT, D, 10 V, 20%	See section 1.5.2.1
VCCDVO	Connect to VCC1_5S	0.1 µF 10 µF 150 µF	2 1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20% SPC, E, 6.3 V, 20%	1 X 0.1 µF within 200 mils 1 X 0.1 µF on bottom side
VCCDLVDS	Connect to VCC1_5S	0.1 µF 22 µF 47 µF	1 1 1	XR7, 0603, 16 V, 10% TANT, B, 10 V, 20% TANT, D, 10 V, 20%	1 X 0.1 µF within 200 mils
VCCTXLVDS[1]	Connect to VCCSus2_5	0.1 µF 22 µf 47 µF	3 1 1	XR7, 0603, 16 V, 10% TANT, B, 10 V, 20% TANT, D, 10 V, 20%	1 X 0.1 µF within 200 mils 2 X 0.1 µF on bottom side
VCCGPIO	Connect to Vcc3_3S	0.1 µF 10 µF	1 1	XR7, 0603, 16 V, 10% XR5, 1206, 6.3 V, 20%	
SMVREF		0.1 µF	1	XR7, 0603, 16 V, 10%	1 X 0.1 µF on bottom side

NOTE: Not required when using 855GME platform design with external graphics only.

13.5.1.1. GMCH VCCSM Decoupling

For the VCCSM pins of the GMCH, a minimum of eleven, 0603 form factor, 0.1-µF, high frequency capacitors is required and must be placed within 150 mils of the GMCH package. The capacitors should be evenly distributed along the GMCH DDR system memory interface and must be placed perpendicular to the GMCH with the power (2.5 V) side of the capacitors facing the GMCH.

- Every GMCH ground and VCCSM power ball in the system memory interface should have its own via.
- Each capacitor should also have its own 2.5-V via within 25 mils of the capacitor pad for connecting to a 2.5-V copper flood. The traces from the capacitors should also be wide and connect to the outer row of balls on the GMCH.
- The ground end of each capacitor must connect to the ground flood and to the ground plane through a via. Each via should be as close to the associated capacitor pad as possible, within 25 mils and with as thick a trace as possible.

13.5.1.2. DDR Memory Device VDD Decoupling

Discontinuities in the DDR signal return paths will occur when the signals transition between the motherboard and the SO-DIMMs. To account for this ground to 2.5-V discontinuity, a minimum of nine 0603 form factor 0.1-µF high frequency bypass capacitors is required between the SO-DIMMs to help minimize any anticipated return path discontinuities that will be created. The capacitors should be distributed as evenly as possible between the two SO-DIMMs.

- A wide ground trace from each capacitor should be connect to a via that transitions to the ground plane. Each ground via should be placed as close to the ground pad as possible.
- A wide 2.5-V trace from each capacitor should connect to a via that transitions to the 2.5-V copper flood. Each via should be placed as close to the capacitor pad as possible. Each capacitor pad should also connect to the closet 2.5-V SO-DIMM pin on either the first or second SO-DIMM connector with a wide trace.

13.5.1.3. DDR VTT Decoupling Placement and Layout Guidelines

The VTT termination rail must be decoupled using high-speed bypass capacitors, one 0603 form factor 0.1-µF capacitor and one 0603 form factor 0.01-µF capacitor per four DDR signals.

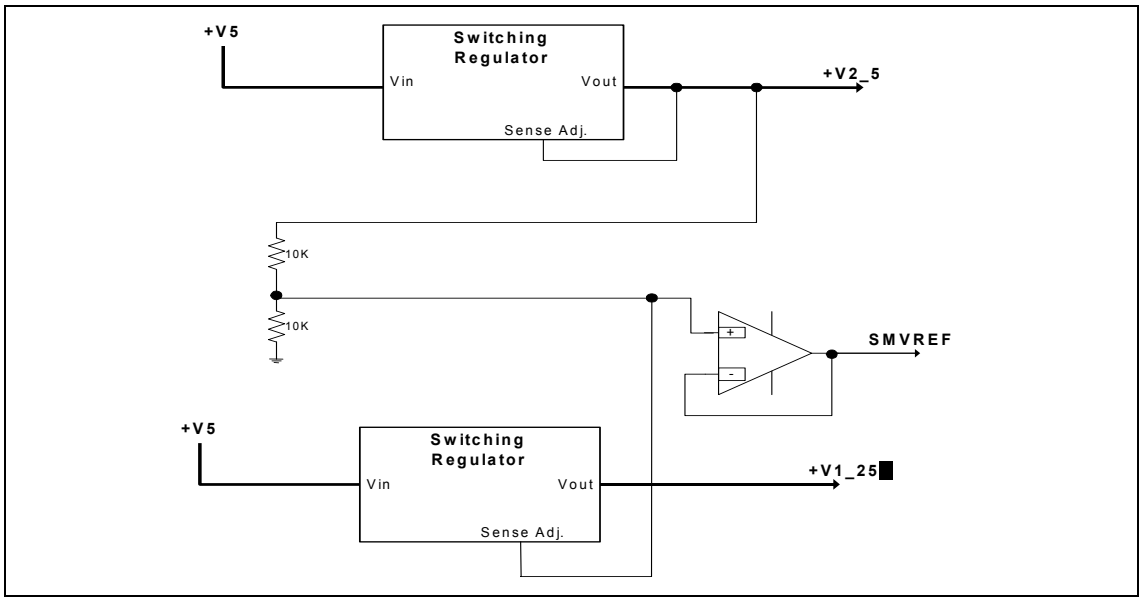
- A VTT copper flood must be used. The decoupling capacitors must be spread out across the termination island so that all the parallel termination resistors are near high frequency capacitors.
- Each capacitor ground via should be as close to the capacitor pad as possible, within 25 mils with as thick a trace as possible.

13.5.2. DDR Memory Power Delivery Design Guidelines

The main focus of these GMCH guidelines is to minimize signal integrity problems and improve the power delivery to the GMCH system memory interface and the DDR memory SO-DIMMs. This section discusses the DDR memory system voltage and current requirements as of publishing for this document. This document is not the original source for these specifications. Figure 139 shows the implementation 2.5 V, 1.25 V and SMVREF on the CRB only as an example. It is the responsibility of the system designer to ensure that the power requirements for the DDR and GMCH are met. Refer to the following documents for the latest details on voltage and current requirements found in this design guide.

- *JEDEC Standard, JESD79 (release 2), Double Data Rate (DDR) SDRAM Specification*
- *Intel DDR 266 JEDEC Spec Addendum* Rev 1.0 or later

Figure 139. DDR Power Delivery Block Diagram



NOTE: +V1.25 used for VTT can optionally be on the switched rail and turned off in S3.

13.5.2.1. 2.5-V Power Delivery Guidelines

The 2.5-V power for the GMCH system memory interface and the DDR SO-DIMMs is delivered around the DDR command, control, and clock signals. Special attention must be paid to the 2.5-V copper flooding to ensure proper GMCH and SO-DIMM power delivery. This 2.5-V flood must extend from the GMCH 2.5-V power vias all the way to the 2.5-V DDR voltage regulator and its bulk capacitors. The 2.5-V DDR voltage regulator must connect to the 2.5-V flood with a minimum of six vias. The SO-DIMM connector 2.5-V pins as well as the GMCH 2.5-V power vias must connect to the 2.5-V copper flood.

In the areas where the copper flooding necks down around the GMCH, make sure to keep these neck down lengths as short as possible. The 2.5-V copper flooding under the SO-DIMM connectors must encompass all the SO-DIMM 2.5-V pins and must be solid except for the small areas where the clocks are routed within the SO-DIMM pin field to their specified SO-DIMM pins.

Note: A minimum of 12-mil isolation spacing should be maintained between the copper flooding and any signals on the same layer.

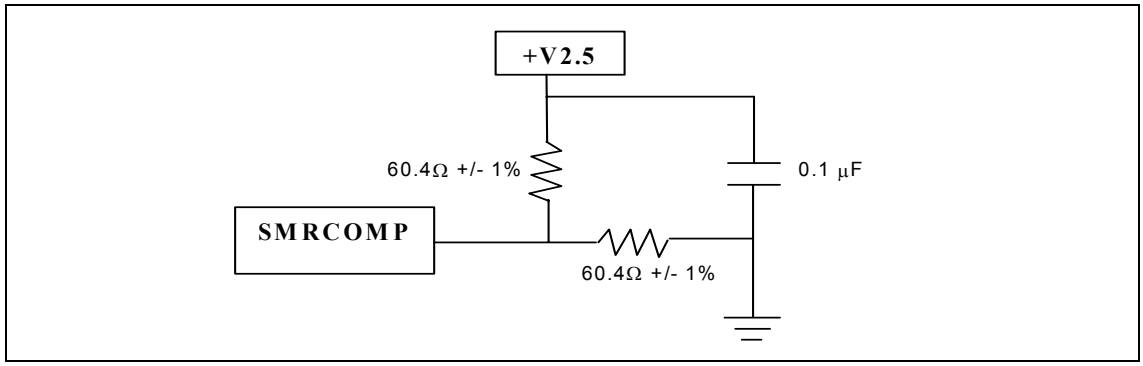
13.5.2.2. GMCH and DDR SMVREF Design Recommendations

There is one SMVREF pin on the GMCH that are used to set the reference voltage level for the DDR system memory signals (SMVREF). The voltage level that needs to be supplied to these pins must be equal to VCCSM/2. As shown in Figure 139 an OpAmp buffer is recommended to generate SMVREF from the 2.5-V supply. This should be used as the “VREF” signals to both the DDR memory devices and the SMVREF signal to the GMCH. A resistor divider is not a recommended solution since SMVREF has a tight tolerance of ± 2%.

13.5.2.3. DDR SMRCOMP Resistive Compensation

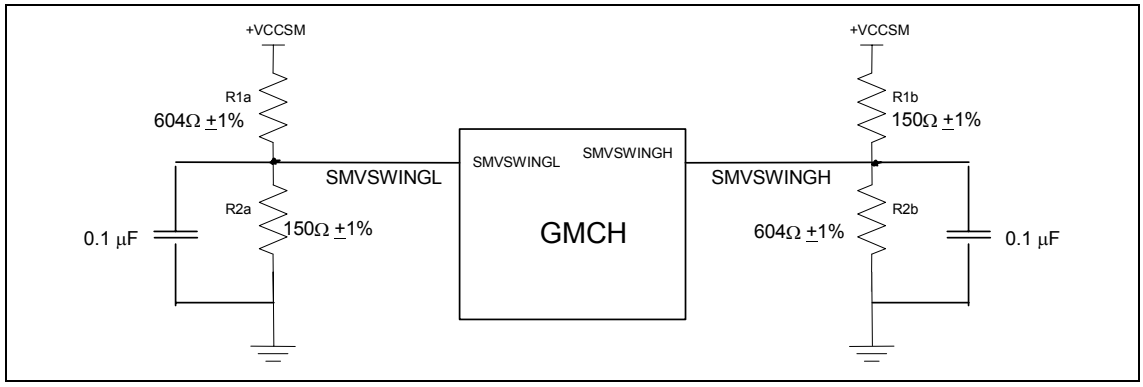
The GMCH requires a system memory compensation resistor, SMRCOMP, to adjust buffer characteristics to specific board and operation environment characteristics. Refer to the *RS – Intel*® 855GM/GME (*Montara-GM/GM+) Chipset GMCH External Design Specification* and Figure 140 for details on resistive compensation. The SMRCOMP signal should be routed with as wide a trace as possible. It should be a minimum of 12 mils wide and be isolated from other signals with a minimum of 10 mils spacing. A 0.1-uF capacitor should be placed near the 2.5-V supply to the voltage divider, and not on the SMRCOMP pin.

Figure 140. GMCH SMRCOMP Resistive Compensation



The GMCH's system memory resistive compensation mechanism also requires the generation of reference voltages to the SMVSWINGL and SMVSWINGH pins. The schematic for SMVSWINGL and SMVSWINGH voltage generation is illustrated in Figure 141. Two resistive dividers with R1b = R2a = 150 Ω ± 1% and R1a = R2b = 604 Ω ± 1% generate the SMVSWINGL and SMVSWINGH voltages. SMVSWINGL and SMVSWINGH components should be placed within 0.5 inches of their respective pins and connected with a 15-mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

Figure 141. GMCH System Memory Reference Voltage Generation Circuit



13.5.2.4. DDR VTT Termination

The recommended topology for DDR-SDRAM Data, Control, and Command signal groups requires that all these signals to be terminated to a 1.25V source, VTT, at the end of the memory channel opposite the GMCH. It is recommended that VTT be generated from the same source as that used for VCCSM, and not be shared with the GMCH and DDR SMVREF. This is because SMVREF has a much tighter

tolerance and VTT can vary more easily depending on signal states. A solid 1.25V termination island should be used to for this purpose and be placed on the surface signal layer, just beyond the last SO-DIMM connector and must be at least 50 mils wide.

The Data and Command signals should be terminated using one resistor per signal. Resistor packs and ± 5% tolerant resistors are acceptable for this application. Only signals from the same DDR signal group can share a resistor pack. See Chapter 6 for system memory guidelines.

13.5.2.5. DDR SMRCOMP and VTT 1.25-V Supply Disable in S3/Suspend

SMRCOMP and VTT 1.25V supplies can be disabled during the S3 suspend state to further save power on the platform. This is possible because the GMCH does not require resistive compensation during suspend. However, the 2.5-V VCCSM power pins of the GMCH, the SMVREF pin of the GMCH, and the VDD power pins of the DDR memory devices are required to be on in S3 state. Note that **some DDR memory devices may or may not require a valid reference voltage during suspend.** It is the responsibility of the system designer to ensure that requirements of the DDR memory devices are met.

13.5.3. Other GMCH Reference Voltage and Analog Power Delivery

13.5.3.1. GMCH GTLVREF

For GMCH, the GTLREF generation circuit has been broken down into three separate voltage references; host data reference voltage (HDVREF[2:0]), host address reference voltage (HAVREF) and host common clock reference voltage (HCCVREF). Maximum length from pin to voltage divider for each reference voltage should be less than 0.5 inches. 10 mil wide traces are recommended. GMCH VREF can be maintained as individual voltage dividers as shown in Figure 142, Figure 143, and Figure 144.

Figure 142. GMCH HDVREF[2:0] Reference Voltage Generation Circuit

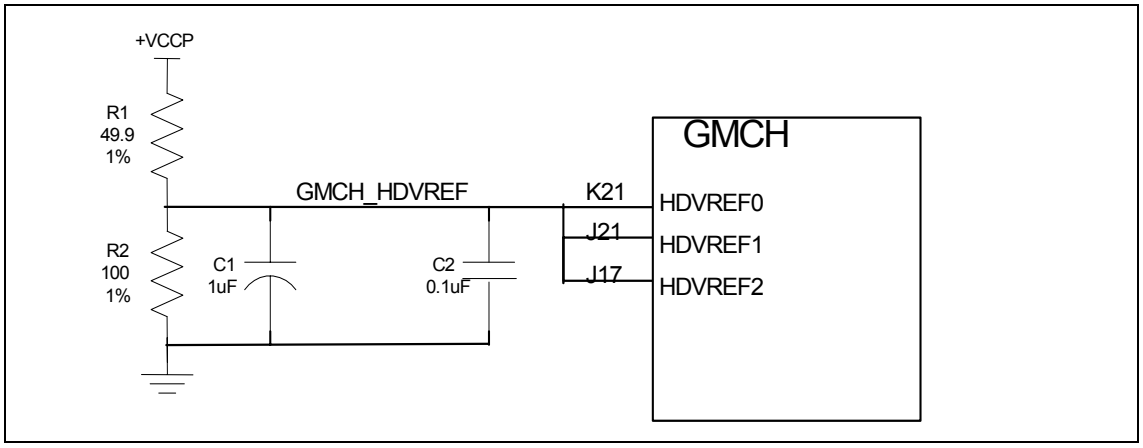


Figure 143. GMCH HAVREF Reference Voltage Generation Circuit

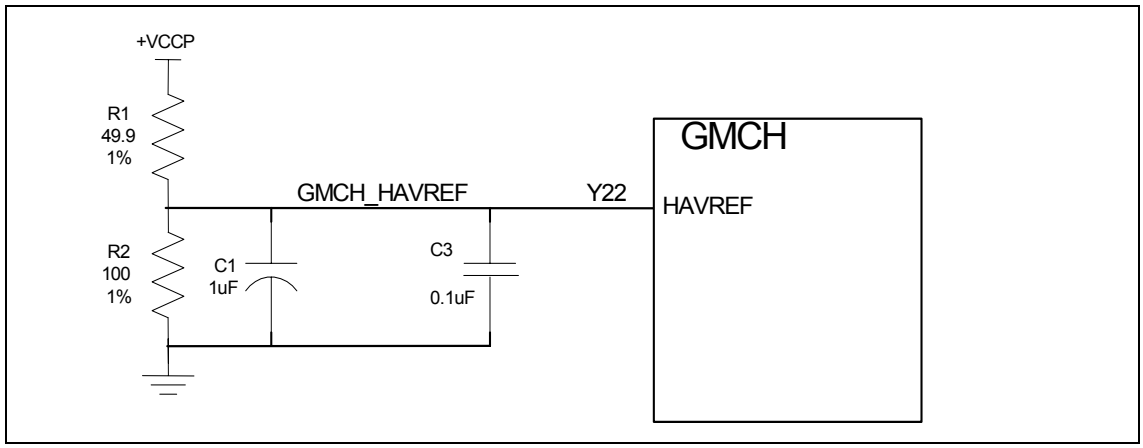
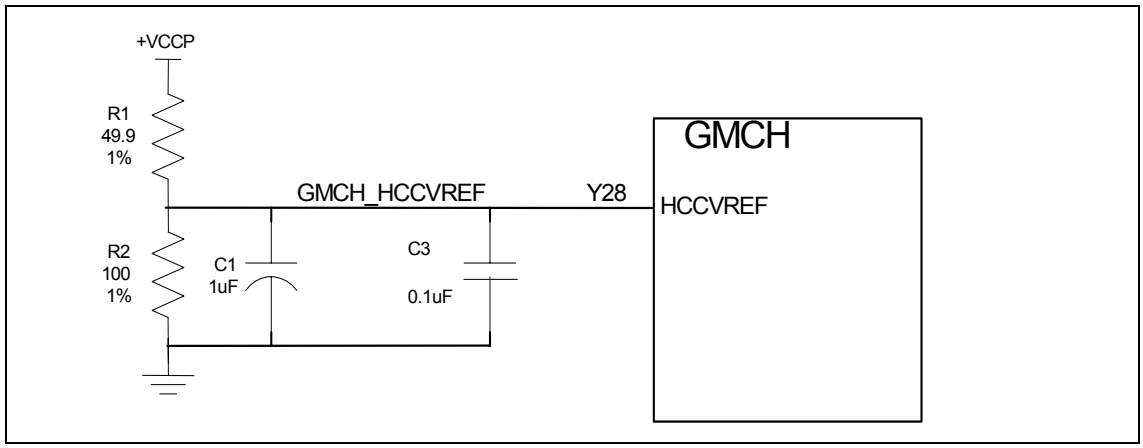


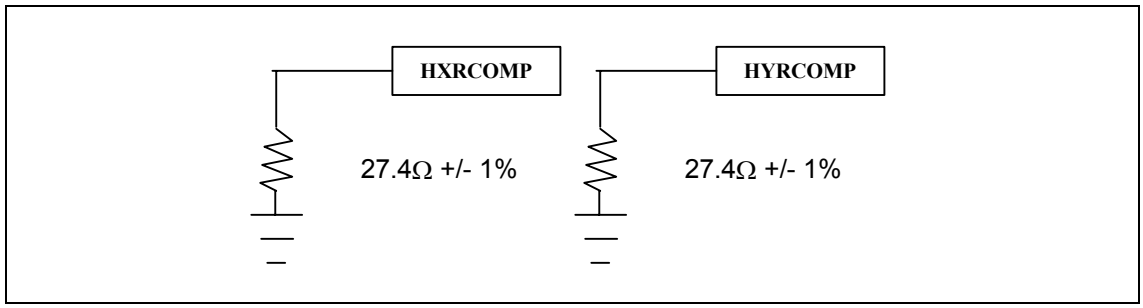
Figure 144. GMCH HCCVREF Reference Voltage Generation Circuit



13.5.3.2. GMCH AGTL+ I/O Buffer Compensation

The HXRCOMP and HYRCOMP pins of the GMCH should each be pulled-down to ground with a 27.4 Ω ± 1% resistor. See Figure 145. The maximum trace length from pin to resistor should be less than 0.5 inches and should be 18-mil wide to achieve the Zo = 27.4 Ω target. Also, the routing for HRCOMP should be at least 25 mils away from any switching signal.

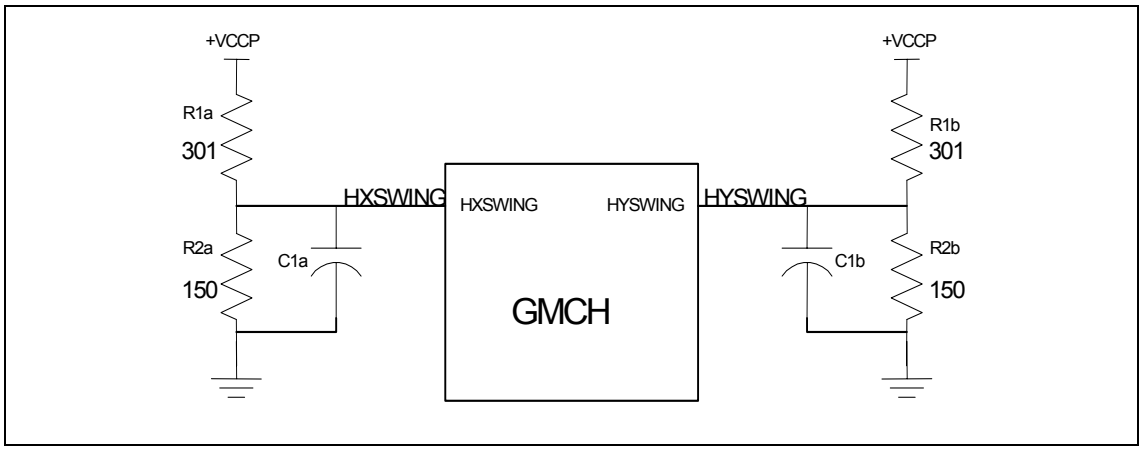
Figure 145. GMCH HXRCOMP and HYRCOMP Resistive Compensation



13.5.3.3. GMCH AGTL+ Reference Voltage

The GMCH's AGTL+ I/O buffer resistive compensation mechanism also requires the generation of reference voltages to the HXSWING and HYSWING pins with a value of 1/3*VCCP. Implementations for HXSWING and HYSWING voltage generation are illustrated in Figure 146. Two resistive dividers with R1a = R1b = 301 Ω ± 1% and R2a = R2b = 150 Ω ± 1% generate the HXSWING and HYSWING voltages. C1a = C1b = 0.1 µF act as decoupling capacitors and connect HXSWING and HYSWING to VCC_CORE. HSWING components should be placed within 0.5 inches of their respective pins and connected with a 15-mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

Figure 146. GMCH HXSWING and HYSWING Reference Voltage Generation Circuit



13.5.3.4. GMCH Analog Power

Table 114 summarizes the eight analog circuits that require filtered supplies on the GMCH. They are: VCCASM, VCCQSM, VCCAHPLL, VCCADPLLA, VCCADPLLB, VCCADAC, VCCAGPLL, and VCCALVDS. VCCADAC, VCCAGPLL, and VCCALVDS do not require an RLC filter but do require decoupling capacitors.

Figure 147. Example Analog Supply Filter

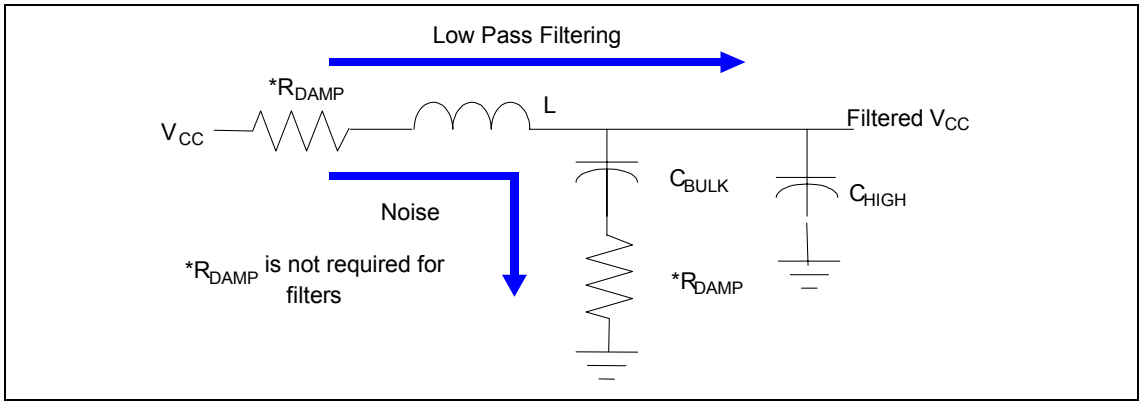


Table 114. Analog Supply Filter Requirements

Required GMCH Filters	Config	Rdamp	Rdamp location	L	Cbulk	Chigh
VCCASM	V1.5S	None	N/A	1210 1.0 µH DCRmax 0.169 Ωs	100 µF	0603 0.1 µF X5R
VCCQSM	V2.5S	1 Ω	In series with Cbulk	0805 0.68 µH DCRmax 0.80 Ωs	1206 4.7 µF X5R	0603 0.1 µF X5R
VCCAHPLL	V_1.2S[2] V_1.35S[3]	None	N/A	None		0603 0.1 µF X5R
VCCADPLLA[1]	V_1.2S[2] V_1.35S[3]	1 Ω	In series with inductor	0805 0.10 µH	220uF	0603 0.1 µF X5R
VCCADPLLB[1]	V_1.2S[2] V_1.35S[3]	1 Ω	In series with inductor	0805 0.10 µH	220 µF	0603 0.1 µF X5R
VCCADAC[1]	V1.5S	None	N/A	None	None	0603 0.1 µF X5R 0603 0.01 µF X5R
VCCAGPLL	V_1.2S[2] V_1.35S[3]	None	N/A	None	None	0603 0.1 µF X5R
VCCALVDS[1]	V1.5S	None	N/A	None	None	0603 0.1 µF X5R 0603 0.01 µF X5R

NOTES:
1. Not required when using 855GME platform design with external graphics only.
2. For 855GM platform
3. For 855GME platform

13.5.4. ICH4-M Decoupling / Power Delivery Guidelines

13.5.4.1. ICH4-M Decoupling

The ICH4-M is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of decoupling capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of high frequency decoupling capacitors specified in table below to ensure that component maintains stable supply voltages. Low frequency decoupling is dependent on layout and system power supply design.

Table 115. ICH4-M Decoupling Requirements

Pin Name	Configuration	F	Qty
VCC3_3	Connect to Vcc3_3S	0.1 µF	6
VCCSUS3_3	Connect to Vcc3_3A	0.1 µF	2
VCCLAN3_3	Connect to Vcc3_3	0.1 µF	2
V_CPU_IO	Connect to Vccp IMVP-IV	1 µF	1
		1 µF	1
VCC1_5	Connect to Vcc1_5S	0.1 µF	2
VCCSUS1_5	Connect to Vcc1_5A	0.1 µF	2
VCCLAN1_5	Connect to Vcc1_5	0.1 µF	2
V5REF	Connect to Vcc5_Ref	0.1 µF	1
V5REF_SUS	Connect to Vcc5A	0.1 µF	1
VCCRTC	Connect to Vcc_RTC	0.1 µF	1
VCCHI	Connect to Vcc1_5S	0.1 µF	2
VCCPLL	Connect to Vcc1_5S	0.1 µF	1
		0.01 µF	1

NOTE: Capacitors should be placed less than 100 mils from the package.

13.5.5. Hub Interface Decoupling

To improve I/O power delivery, use two 0.1-µF capacitors per each component (i.e. the ICH4-M and GMCH). These capacitors should be placed within 50 mils from each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the V_{SS} side of the board should connect the V_{CC}HI side of the capacitors to the V_{CC}HI power pins. Similarly, if layout allows, metal fingers running on the V_{CC}HI side of the board should connect the groundside of the capacitors to the V_{SS} power pins.

13.5.6. FWH Decoupling

Place a 0.1-µF capacitor between the V_{CC} supply pins and the V_{SS} ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, place a 4.7-µF capacitor between the V_{CC} supply pins and the V_{SS} ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the V_{CC} supply pins.

13.5.7. General LAN Decoupling

The following are general LAN decoupling recommendations:

- All VCC pins should be connected to the same power supply.
- All VSS pins should be connected to the same ground plane.
- Four to six decoupling capacitors, including two 4.7-µF capacitors are recommended
- Place decoupling as close as possible to power pins.

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14. Intel Pro/Wireless 2100/2100A – Bluetooth Coexistence Interface Design Requirements

This section describes the design requirements needed to support the Intel PRO/Wireless 2100/2100A wireless component, a critical component of the latest Intel Centrino mobile technology. The following discussion provides guidelines on the interface design between the Intel PRO/Wireless 2100/2100A 802.11a/b wireless LAN device and the Bluetooth module of choice supporting the coexistence algorithm. The following areas will be covered:

1. Coexistence interface design requirements
2. DC power requirements for Bluetooth
3. Start up conditions and logic protection

Detailed information on the coexistence specification is disclosed in the *RS - Banias Coexistence System Specification* and *Intel Banias Wireless Platform Design Guide*.

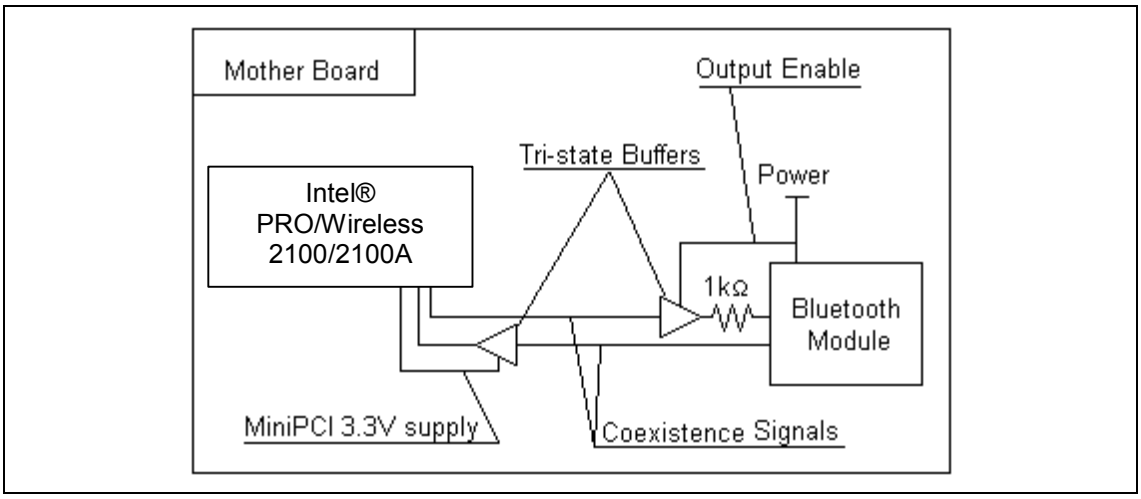
14.1. PCB Interface Requirements

The Intel PRO/Wireless 2100/2100A (2100/2100A) wireless LAN device is a PCI based component that is designed to fit into the standard mini-PCI connector. No standard connector is specified for use with the Bluetooth* module and vendor implementations may vary. The coexistence solution that exists between the Intel PRO/Wireless 2100/2100A and Bluetooth* modules is composed of a two signal interface. These two signals are used to transmit the channel number and clock signals between the two devices.

Although these traces do not have any length, width or impedance matching constraints, a typical routing solution of 5 mils trace width on 5 mils spacing is recommended. The 2100/2100A's PCI pin #43 needs to be routed to the Channel_Data signal of the Bluetooth module. The 2100/2100A's PCI pin #36 needs to be routed to the Channel_Clock signal of the Bluetooth module.

In order to protect the Bluetooth module and 2100/2100A modules, CMOS tri-state buffers (e.g. 74AHC1G126 or equivalent) and a 1-kΩ resistor are recommended as illustrated in Figure 148. A detailed explanation of this recommendation is described in Section14.3.

Figure 148. Recommended Topology for Coexistence Traces



14.2. DC Power Requirements for Bluetooth

The Bluetooth* module requires a 3.3-V power supply that can be regulated within a tolerance of ±2%. This source may be derived from any power rail available on the platform.

14.3. Start Up Conditions and Logic Protection

It is assumed that the power on/off and initialization of the Bluetooth module and Intel PRO/Wireless 2100/2100A are asynchronous and the power delivery to each device is not coupled. As a result, concerns arise as to the logic state of the coexistence lines when the module intended to receive a signal is not powered up. This could possibly cause damage to either the Bluetooth* module or Intel PRO/Wireless 2100/2100A and/or place one of the components into an indeterminate state.

A recommended implementation that will protect both components from potential damage caused by asynchronous power on/off is depicted in Figure 148. For the Bluetooth module, it is recommended that a tri-state buffer (powered by the Bluetooth* module supply) and a 1-kΩ series resistor be placed near the Bluetooth module. Likewise, a tri-state buffer (powered by the mini-PCI 3.3V supply) should be placed near to the Intel PRO/Wireless 2100/2100A module. This low cost solution has been validated and noted to have a minimal impact on board area if implemented as recommended.

The *RS - Banias Coexistence System Specification* requires that no logic "high" signals be asserted by the Bluetooth module on the coexistence signal lines until the Intel PRO/Wireless 2100/2100A has signaled to the Bluetooth module that it is ready. It is assumed that the Bluetooth module will initialize upon power up of the platform and that during this period (estimated to be < 15 ms) the Bluetooth module's GPIOs will default to either inputs or a high impedance state. Since the logic level of the Intel PRO/Wireless 2100/2100A coexistence signals is not known during this time, it is important that no logic "high" signal be asserted by the Bluetooth* module on either of the coexistence signal lines. Such signals could cause damage or entry into an indeterminate state if the Intel PRO/Wireless 2100/2100A is not ready to accept them. It is also possible that the Bluetooth module could assert a logic high signal when the Intel PRO/Wireless 2100/2100A is powered down since the power sources for the modules are not coupled.

This concern exists for any condition in which the power provided to either component has been disabled through any number of means. The solution illustrated in Figure 148 will adequately prevent any of these possible conditions from affecting system performance or damaging the hardware.

14.4. USB Selective Suspend

See section 11.4.6 for information regarding Bluetooth power requirements during selective suspend.

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15. Reserved, NC, and Test Signals

The Intel Pentium M processor, Intel Pentium M Processor on 90 nm Process with 2 MB L2 Cache, 855GM/GME chipset GMCH may have signals listed as “RSVD”, “NC”, or other name whose functionality is Intel reserved. The following section contains recommendations on how these Intel reserved signals on the processor or GMCH should be handled.

15.1. Intel Pentium M Processor and Intel Celeron M Processor RSVD Signals

The Intel Pentium M processor and Intel Celeron M processor each have a total of three TEST, and eight RSVD signals that are Intel reserved in the pin-map. All other RSVD signals are to be left unconnected but should have access to open routing channels for possible future use. The location of the Intel reserved signals in the processor pin-map is listed in Table 116.

Table 116. Processor RSVD and TEST Signal Pin-Map Locations

Signal Name	Ball Name
RSVD (LAI usage)	AF7
RSVD (key)	A1
RSVD	B2
RSVD	C3
RSVD	C14
RSVD (PSI#)	E1
RSVD (former GTLREF1)	E26
RSVD (former GTLREF2)	G1
RSVD (former GTLREF3)	AC1
TEST1	C5
TEST2	F23
TEST3	C16

15.2. Intel Pentium M Processor on 90 nm Process with 2 MB L2 Cache Processor RSVD Signals

The Intel Pentium M Processor on 90 nm Process with 2 MB L2 Cache Processor is pin compatible with the Intel Pentium M processor. Pins C14 and C16 are defined as BSEL1 and BSEL0 respectively for Intel Pentium M Processor on 90 nm Process with 2 MB L2 Cache processor for future platform functionality. They should be left as NC on 855GM/GME chipset based systems.

15.3. Intel 855GM/GME Chipset GMCH RSVD Signals

The Intel 855GM/GME chipset GMCH has a total of 13 RSVD and 12 NC signals that are Intel reserved in the pin-map. The recommendation is to provide test points for all RSVD signals for possible future use. All NC signals should be left as no connects. The location of the Intel reserved signals in the GMCH pin-map is listed in Table 117.

Table 117. Intel 855GM/GME Chipset GMCH RSVD and NC Signal Pin-Map Locations

Signal Name	Ball Name
AJ29	NC
AH29	NC
B29	NC
A29	NC
AJ28	NC
A28	NC
AA9	NC
AJ4	NC
AJ2	NC
A2	NC
AH1	NC
B1	NC
D7	RSVD
F12	RSVD
D12	RSVD
B12	RSVD
AA5	RSVD
L4	RSVD
F3	RSVD
D3	RSVD
B3	RSVD
F2	RSVD
D2	RSVD
C2	RSVD
B2	RSVD

16. Platform Design Checklist

The following checklist provides design recommendations and guidance for the Intel Pentium M processor and Intel Celeron M processor systems with the Intel 855GM/855GME chipset. It should be used to ensure that design recommendations in the design guide have been followed **prior** to schematic reviews. However, this is not a complete list and does not contain detailed layout information.

Note: Unless otherwise specified the default tolerance on resistors is ± 5%. Also note that the (S) reference after power rails such as VCC3_3 (S) indicates a switched rail - one that is powered off during S3-S5.

16.1. General Information

The following section should be filled out by the OEM or Intel field representative.

Intel Pentium M Processor / Intel Celeron M Processor	
Processor Min Frequency targeted for this platform	
Processor Max Frequency targeted for this platform	
Voltage Regulator Solution	Part#/Vendor: Target ICC(max):
Target Thermal Envelope (Watts)	
Battery Life	Target:
Form Factor	
Panel Vendor and Size	Part#/Vendor:
Backlight Inverter	Part#/Vendor:
DVO Device	Part#/Vendor:
LOM or mini-PCI LAN?	
Wireless Solution?	
Target FCS (First Customer Ship) Date	

16.2. Customer Implementation of Voltage Rails

Fill in schematic name of voltage rails and mark boxes of when rails are powered on.

Name of Rail	On S0-S1	On S3	On S4	On S5

16.3. Design Checklist Implementation

The voltage rail designations in this Design Checklist are intended to be as general as possible. The following table describes the equivalent voltage rails in the Intel CRB Schematics.

Checklist Rail	Intel CRB Rail	On S0-S1	On S3	On S4	On S5	Notes
Vcc1_2	+V1.2S_GMCH_CORE, +V1.2S_GMCH_HUB, +V1.2S_GMCH_HGPLL, +V1.2S_GMCH_DPLL, +V1.2S_GMCH_ASM	X				
Vcc1_25	+V1.25S [DDR_Vtt]	X				4
Vcc1_5	+V1.5S_GMCH_DVO, +V1.5S_GMCH_ALVDS, +V1.5S_GMCH_ADAC, +V1.5S_GMCH_DLVDS, +V1.5S_ICH, +V1.5S_ICHHUB	X				
VccSus1_5	+V1.5_ICHLAN	X	X			1,3
V1_5ALWAYS	+V1.5A_ICH	X	X	X	X	
VccSus2_5	+V2.5_GMCH_SM, +V2.5_GMCH_QSM, +V2.5_GMCH_TXLVDS, +V2.5_DDR	X	X			

Checklist Rail	Intel CRB Rail	On S0-S1	On S3	On S4	On S5	Notes
Vcc3_3	+V3.3S_ICH, +V3.3S_GMCH_GPIO, +V3.3S_CLKRC, +V3.3S_SPD, +V3.3S_LVDS, +V3.3S_FWH	X				
VccSus3_3	+V3.3_ICHLAN, +V3.3_LAN	X				1,2,3
V3ALWAYS	+V3.3ALWAYS_ICH	X	X	X	X	
Vcc5	+V5S_DAC	X				
VccSus5	+V5_USB	X	X			1,3
V5ALWAYS	+V5A_ICH	X	X	X	X	
Vcc12	+V12S	X				
VccRTC	+V_RTC	X	X	X	X	
VCCP	+VCC_IMVP	X				
VCCA	+V1.8S_PROC	X				5
VccCORE	+VCC_CORE	X				

NOTES:

1. A rail powered in Sx is dependent on implementation.
2. VccLANx rail is powered on in Sx is dependent on implementation.
3. VxALWAYS rail can be the SUS rail depending on implementation.
4. Vcc1_25 is the 1.25 V VTT rail for DDR.
5. For Pentium M processor / Celeron M processor, VCCA is 1.8V, used for PLL.

16.4. Intel Pentium M Processor / Intel Celeron M Processor

16.4.1. Resistor Recommendations

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
A20M#				Point-to-point connection to ICH4-M.	
BR0#				Point-to-point connection to GMCH.	
COMP0, COMP2	27.4 Ω ± 1% pull-down to gnd			Resistor placed within 0.5" of processor pin. Trace should be 27.4 Ω ± 15%.	
COMP1, COMP3	54.9 Ω ± 1% pull-down to gnd			Resistor placed within 0.5" of processor pin. Trace should be 55Ω ± 15%.	
DPSLP#				Connect to GMCH and ICH4-M.	
FERR#	56 Ω pull-up to VCCP	56 Ω from pull-up to ICH4-M pin.		Point-to-point connection to ICH4-M, with pull-up resistor and series resistor placed by ICH4-M.	
GTLREF	1 KΩ ± 1% pull-up to VCCP 2 KΩ ± 1% pull-down to gnd			Voltage divider should be placed within 0.5" of processor pin.	
IERR#	56 Ω pull-up to VCCP			IERR# is a 1.05 V signal. Voltage translation logic and/or series resistor may be required if used.	
INIT#			R1 = 1.3 KΩ R2 = 330 Ω Rs = 330 Ω	Point-to-point connection to ICH4-M. Voltage transition circuit is required if connecting to FWH. Signal is T-split from the ICH4-M to FWH. See Figure 149.	
IGNNE#				Point-to-point connection to ICH4-M.	
LINT0/INTR				Point-to-point connection to ICH4-M.	
LINT1/NMI				Point-to-point connection to ICH4-M.	
PROCHOT#	56 Ω pull up to VCCP		R1 = 1.3 KΩ R2 = 330 Ω Rs = 330 Ω	PROCHOT# is a VCCP signal. This signal is not used on the CRB. So, voltage translation logic may be required if used. **If Voltage Translation is Required**: Driver isolation resistor should be placed at the beginning of the T-split to the system receiver. See Figure 150.	
PSI#				Can be left as NC, if not used for IMVP.	
PWRGOOD	330 Ω pull-up to VCCP			Point-to-point connection to ICH4-M, with resistor placed by the processor.	

Pin Name	System Pull-up/Pull-down	Series Termination	Voltage Translation	Notes	✓
RESET#	54.9 Ω ± 1% pull-up to VCCP If USING ITP700FLEX	22.6 Ω ± 1% from pull-up to ITP700FLEX		**If ITP700FLEX is Not Used**: Point-to-point connection to GMCH. **If ITP700FLEX is Used**: RESET# connects from processor to GMCH and then forks out to ITP700 FLEX, with pull-up and series damping resistor placed next to ITP.	
RSVD (pin AC1, AF7, C3, C14, E26, G1)				Route to test points.	
SLP#				Point-to-point connection to ICH4-M.	
SMI#				Point-to-point connection to ICH4-M.	
STPCLK#				Point-to-point connection to ICH4-M.	
TEST[3:1]	1 kΩ pull-down to gnd (default: no stuff)			For each signal, stuffing option for pull-down should be provided for testing purposes. For normal operation, leave the resistors unpopulated.	
THERMTRIP#	56 Ω pull-up to VCCP	56 Ω from pull-up to ICH4-M pin		Point-to-point connection to ICH4-M, with pull-up and series resistors placed by ICH4-M. THERMTRIP# is a VCCP signal. If connecting to other device, voltage translation logic may be required.	
VCC[71:0]	Connect to VccCORE				
VCCA[3:0]	Connect to Vcc1_8			Connect to Vcc1_8 for Intel Pentium M processor. Connect to either Vcc1_8 or Vcc1_5 for Intel Pentium M Processor on 90 nm Process with 2 MB L2 Cache.	
VCCP[26:0]	Connect to VCCP				
VCCSENSE, VSSSENSE	54.9 Ω ± 1% pull-down to gnd (default: no stuff)			For each signal, stuffing option for pull-down should be provided for testing purposes. Also, a test point for differential probe ground should be placed between the two resistors. For normal operation, leave the resistors unpopulated.	
VSS[191:0]	Connect to gnd				

Figure 149. Routing Illustration for INIT#

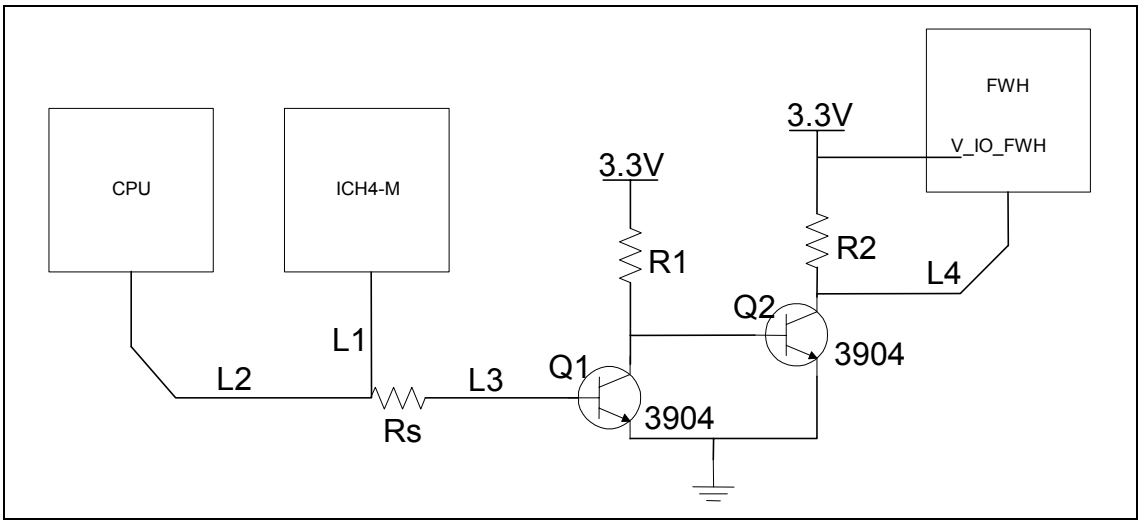
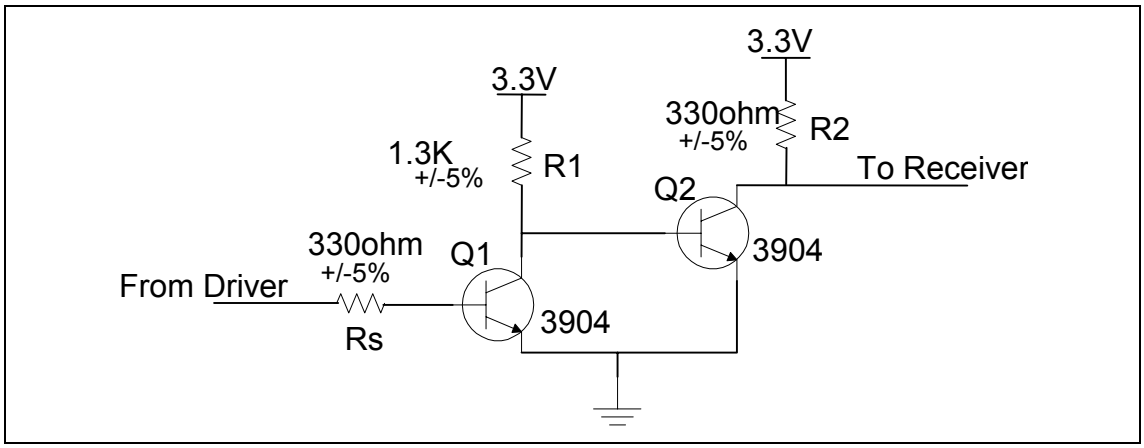


Figure 150. Voltage Translation Circuit for PROCHOT#



16.4.2. In Target Probe (ITP)

Pin Name	System Pull-up /Pull-down	Series Termination Resistor (Ω)	Notes	✓
BPM[5:0]#			Connect to processor directly.	
DBR#	150-240 Ω pull-up to V3ALWAYS		If using ITP on interporser card, then DBR# should also be connected to DBRESET pin at the processor. The 150-240 Ω pull-up resistor should be placed within 1 ns of the ITP700FLEX connector. The CPU should **not** be power cycled when DBR# is asserted.	
RESET#	54.9 Ω ± 1% pull-up to VCCP IF USING ITP700FLEX	22.6 Ω ± 1% from pull-up to ITP700FLEX	See notes in Section 16.4.1	
FBO			Connect to TCK pin of processor.	
TCK	27.4 Ω ± 1% pull-down to gnd		Connect to processor, with resistor placed by ITP.	
TDI	150 Ω pull-up to VCCP		Connect to processor, with resistor placed by the processor.	
TDO	54.9 Ω ± 1% pull-up to VCCP	22.6 Ω ± 1% from pull-up to ITP700FLEX	Connect to processor, with resistors placed by ITP. If ITP not used, this signal can be left as NC.	
TMS	39.2 Ω ± 1% pull-up to VCCP		Connect to processor, with resistor placed by ITP.	
TRST#	680 Ω pull-down to gnd		Connect to processor.	
VTAP, VTT[1:0]	Connect to VCCP		One 0.1 µF decoupling cap is required.	

16.4.3. Decoupling Recommendations

16.4.3.1. VCCP (I/O)

Description	C, µF	ESR, mΩ	ESL, nH	Notes	✓
Low Frequency Decoupling (Polymer Covered Tantalum - POSCAP, Neocap, KO Cap)	1 x 150 µF	42 mΩ (typ) / 2	2.5 nH / 12		
High Frequency Decoupling (0603 MLCC, >= X7R)	10 x 0.1 µF	16 mΩ (typ) / 10	0.6 nH / 10		

16.4.3.2. VCCA (PLL)

Description	C, µF	Notes	✓
Mid Frequency Decoupling (Polymer Covered Tantalum - POSCAP, Neocap, KO Cap)	4 x 10 µF	Place one 10 µF and one 0.01 µF for each VCCA pin.	
High Frequency Decoupling (0603 MLCC, >= X7R) Place next to the processor	4 x 0.01 µF	Place one 10 µF and one 0.01 µF for each VCCA pin.	

16.4.3.3. VCC (CORE)

Option	Description	C, µF	ESR, mΩ	ESL, nH	✓
#1	Low-Frequency Decoupling (Polymer Covered Tantalum – POSCAP, Neocap, KO Cap)	12 x 150 µF	36 mΩ (typ) / 12	2.5 nH / 12	
	Mid-Frequency Decoupling (0612 MLCC, X5R or better)	15 x 2.2 µF	5 mΩ (typ) / 15	0.2 nH / 15	
#2	Low-Frequency Decoupling (1206 MLCC, X5R or better)	40x10 µF	5 mΩ (typ) / 40	1.2 nH / 40	
	Mid-Frequency Decoupling (0612 MLCC, X5R or better)	15 x 2.2 µF	5 mΩ (typ) / 15	0.2 nH / 15	
#3	Low Frequency Decoupling (Polymer Covered Aluminum – SP Cap, A0 Cap)	5 x 330 µF	15 mΩ (max) / 5	3.5 nH / 5	
	Low Frequency Decoupling (1206 MLCC, >= X5R)	25 x 10 µF	5 mΩ (typ) / 25	1.2 nH / 25	
	Mid Frequency Decoupling (0612 MLCC, >= X5R)	15 x 2.2 µF	5 mΩ (typ) / 15	0.2 nH / 15	
#4	Low-Frequency Decoupling (Polymer Covered Aluminum – SP CAP, AO Cap)	4 x 220 µF	12 mΩ (max) / 4	3.5 nH / 4	
	Mid-Frequency Decoupling (0805 MLCC>= X5R)	35 x 10 µF	5 mΩ (typ) / 35	0.6 nH / 35	

NOTES:

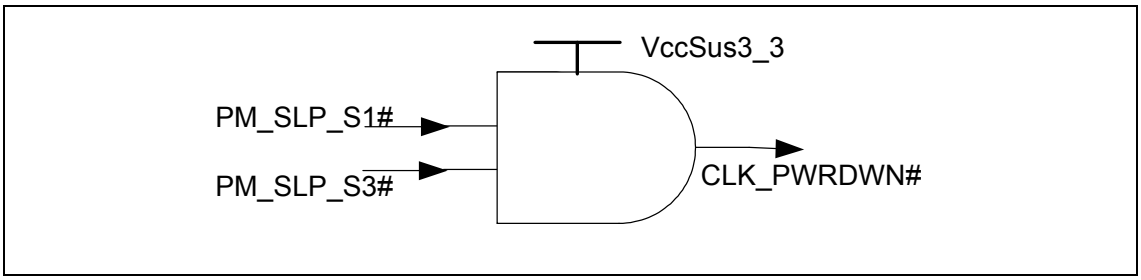
1. Decoupling guidelines are recommendations based on our reference board design. The Intel Customer Reference Board uses option #4. This is the preferable option to use.
2. When deciding on overall decoupling solution, customers will need to take layout & PCB board design into consideration.
3. Options #4 is to be used with small footprint (100 mm^2 or less) 0.36 µH ± 20% inductors.

16.5. CK-408 Clock Checklist

16.5.1. Resistor Recommendations

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	✓
3V66[0] 3V66[1]		33 Ω	If the signal is used, one 33-ohm series resistor is required. If the signal is NOT used, it should be left as NC (Not Connected) or connected to a test point.	
66BUF[2:0]		33 Ω	Use 66BUF[1] (pin 22) for GMCH. Use one of the other two signals for ICH4-M.	
CPU[0], CPU[0]# CPU[1], CPU[1]# CPU[2], CPU[2]#	49.9 Ω ± 1% pull- down to gnd	33 Ω	Use one pair for the processor and another pair for GMCH. If on-board ITP is implemented, the third pair of clock signals is used for the ITP connector. Otherwise, it can be routed to the dedicated ITP clock pins on the processor socket.	
48MDOT		33 Ω	Connect to GMCH's DREFCLK.	
3V66/VCH		33 Ω	Two possible topologies: • Use directly for GMCH's DREFSSCLK. • Use as input to an SSC component and use the SSC component output for GMCH's DREFSSCLK.	
IREF	475 Ω ± 1% pull-down to gnd			
MULT[0]	10 kΩ pull-up to Vcc3_3			
PCI[6:0]		33 Ω	Connect to various PCI devices.	
PCIF[2], PCIF[1], PCIF[0]		33 Ω	Use one clock for ICH4-M. Unused clock pins should be left as NC or connected to a test point.	
PWRDWN#		AND gate	This signal is needed for supporting S1M. It needs to be driven low by both SLP_S1# and SLP_S3# through an AND gate. See Figure 151.	
REF		33 Ω	This is the 14.318MHz clock reference signal for ICH4-M, SIO and LPC. Each receiver requires one 33-ohm series resistor.	
SEL[2:1]	10 k-20 kΩ pull-down to gnd			
SEL[0]	10 k-20 kΩ pull- up to Vcc3_3			
48MUSB		33 Ω	Connect to ICH4-M's 48-MHz clock input.	
XTAL_IN, XTAL_OUT			Connect to a 14.318 MHz crystal, placed within 500 mils of CK-408	
VDD[7:0], VDDA	Connect to Vcc3_3		Refer to clock vendor datasheet for decoupling info.	
VSS[5:0], VSSA	Connect to gnd			
VSSIREF	Connect to gnd			

Figure 151. Clock Power-down Implementation



16.6. Intel 855GM/855GME Checklist

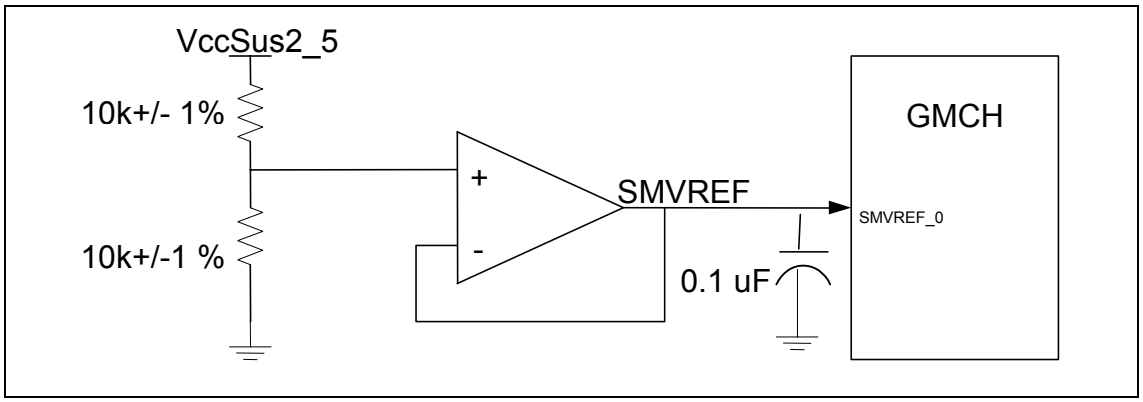
16.6.1. System Memory

16.6.1.1. GMCH System Memory Interface

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	✓
RCVENIN#			This signal should be routed to a via next to ball and left as a NC (No Connect).	
RCVENOUT#			This signal should be routed to via next to ball and left as a NC (No Connect).	
SBA[1:0], SCAS#, SRAS#, SWE#	56 Ω pull-up to Vcc1_25	10 Ω	Three topologies available for routing these signals.	
SCKE[3:0], SCS#[3:0]	56 Ω pull-up to Vcc1_25			
SDQ[63:0], SDM[7:0], SDQS[7:0]	56 Ω pull-up to Vcc1_25	10 Ω		
SDQ[71:64], SDM8, SDQS8	56 Ω pull-up to Vcc1_25	10 Ω	If ECC support is not implemented, SDQ[71:64], SDM8, and SDQS8 should be left as NC. For ECC support, these signals connect to SO-DIMMs.	
SMA[12:6,3,0]	56 Ω pull-up to Vcc1_25	10 Ω	Three topologies available for routing these signals.	
SMA[5,4,2,1] SMAB[5,4,2,1]	56 Ω pull-up to Vcc1_25		Use SMA[5,4,2,1] for one SO-DIMM connector; use SMAB[5,4,2,1] for the other SO-DIMM connector.	
SCK0, SCK0# SCK1, SCK1#			These clock signals connect to SO-DIMM 0.	
SCK2, SCK2#			If ECC supported is not implemented, these clock signals should be left as NC. For ECC support, these signals connect to SO-DIMM 0.	
SCK3, SCK3# SCK4, SCK4#			These clock signals connect to SO-DIMM 1.	
SCK5, SCK5#			If ECC supported is not implemented, these clock signals should be left as NC. For ECC support, these signals connect to SO-DIMM 1.	
SMVREF	10 kΩ 1% pull-up to VccSus2_5 10 kΩ 1% pull-down to gnd		Signal voltage level = VccSus2_5/ 2. Note that a buffer is used to provide the necessary current and reference voltage to SMVREF. Place a 0.1uF cap by GMCH. See Figure 152.	
SMVSWINGL	604 Ω 1% pull-up to VccSus2_5 150 Ω 1% pull-down to gnd		Signal voltage level = 1/5 * VccSus2_5. Need 0.1 µF cap at pin. This signal may be optionally connected to Vcc2_5 and powered off in S3.	
SMVSWINGH	150 Ω 1% pull-up to VccSus2_5 604 Ω 1% pull-down to gnd		Signal voltage level = 4/5 * VccSus2_5. Need 0.1 µF cap at pin. This signal may be optionally connected to Vcc2_5 and powered off in S3.	

Pin Name	System Pull-up/Pull-down	Series Resistor	Notes	✓
SMRCOMP	60.4 Ω 1% pull-up to VccSus2_5 60.4 Ω 1% pull-down to gnd		Signal voltage level = 1/2 * VccSus2_5. Need 0.1 µF cap by the voltage divider. This signal may be optionally connected to Vcc2_5 and powered off in S3.	

Figure 152. Reference Voltage Level for SMVREF



16.6.1.2. DDR SO-DIMM Interface

Pin Name	Configuration	Notes	✓
VREF[2:1]		Signal voltage level = VCCSus2_5 / 2.	
VDD[33:1]	Connect to VccSus2_5	Power must be provided during S3.	
VDDSPD	Connect to Vcc3_3		
SA[2:0]	Connect to either VC3_3 or gnd	These lines are used for strapping the SPD address for each SO-DIMM.	
VSS[31:1]	Connect to gnd		
RESET(DU)		Signal can be left as NC (“Not Connected)	
VDDID		Signal can be left as NC (“Not Connected)	
DU[4:1]		Signal can be left as NC (“Not Connected)	
GND[1:0]		Signal can be left as NC (“Not Connected)	

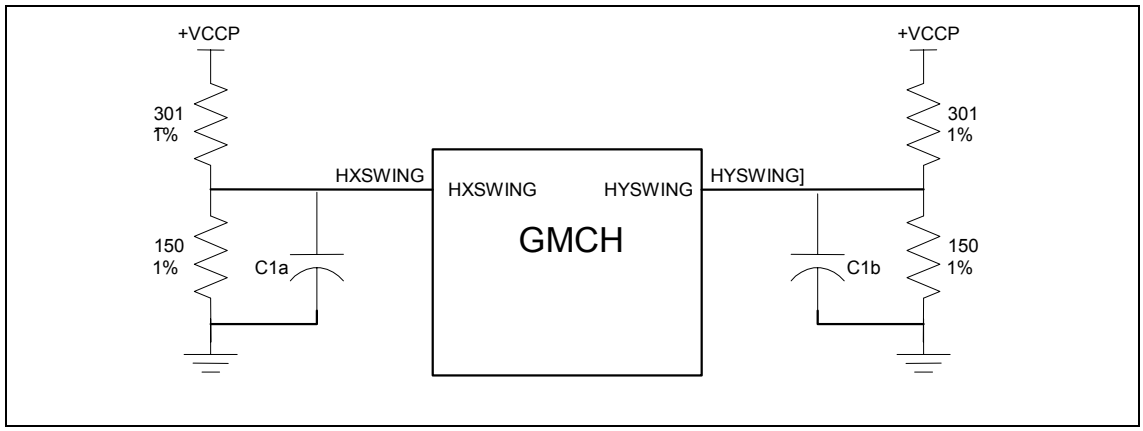
16.6.1.3. SODIMM Decoupling Recommendation

Pin Name	F	Qty	Notes	✓
Vcc1_25	0.1 µF 0.01 µF		Place one 0.1 µF cap and one 0.01 µF close to every 4 pull-up resistors terminated to Vcc1_25 (VTT for DDR signal termination). In S3, Vcc1_25 is powered OFF.	
Vcc2_5Sus	0.1 µF 100-150 µF	9 4	A minimum of 9 high frequency caps are recommeneded to be placed bewteen the SO-DIMMS. A minimum of 4 low frequency caps are required.	

16.6.2. FSB

Pin Name	System Pull-up/Pull-down	Notes	✓
HXSWING, HYSWING	301 Ω 1% pull-up to VCCP 150 Ω 1% pull-down to gnd	Signal voltage level = 1/3 of VCCP. C1a=0.1 µF. C1b=0.1 µF. Trace should be 10-mil wide with 20-mil spacing. See Figure 153.	
HXRCOMP, HYRCOMP	27.4 Ω 1% pull down to gnd	One pulled-down resistor per pin. Trace should be 10-mil wide with 20-mil spacing.	
HDVREF[2:0]	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to gnd	Signal voltage level = 2/3 of VCCP. Need one 0.1 µF cap and one 1 µF cap for voltage divider.	
HAVREF	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to gnd	Signal voltage level = 2/3 of VCCP. Need one 0.1 µF cap and one 1 µF cap for voltage divider.	
HCCVREF	49.9 Ω 1% pull-up to VCCP 100 Ω 1% pull-down to gnd	Signal voltage level = 2/3 of VCCP. Need one 0.1 µF cap and one 1 µF cap for voltage divider.	

Figure 153. GMCH HXSWING & HYSWING Reference Voltage Generation Circuit



16.6.3. Hub Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
HLVREF	See Section16.7.9.	Signal voltage level = 0.35 V ± 8%.	
PSWING	See Section16.7.9.	Signal voltage level = 2/3 of VCC1_2 or 0.8 V ± 8%.	
HLZCOMP	27.4 Ω 1% pull-up to Vcc1_2		

16.6.4. Graphics Interfaces

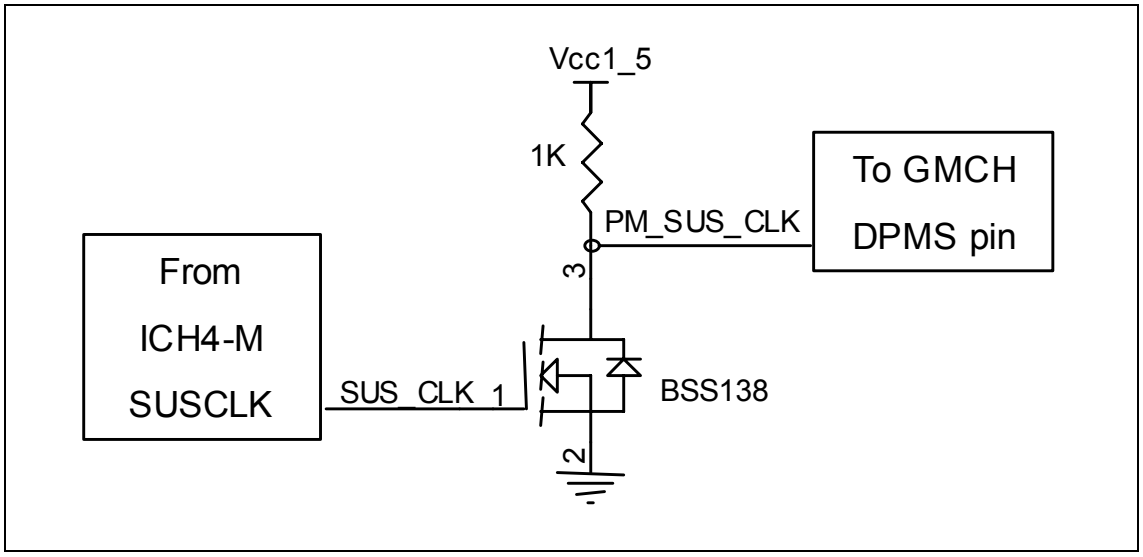
16.6.4.1. LVDS

Pin Name	System Pull-up/Pull-down	Notes	✓
LIBG	1.5 KΩ 1% pull-down to gnd		
YAP[3:0]/YAM[3:0] YBP[3:0]/YBM[3:0]		If any of these LVDS data pairs are unused, they can be left as “no connect.”	
CLKAP/CLKAM CLKBP/CLKBM		If any of these LVDS clock pairs are not used, they can be left as “no connect.”	
LVREFH, LVREFL, LVBG		These signals should be left as NC.	

16.6.4.2. DVO

Pin Name	System Pull-up/Pull-down	Notes	✓
DVORCOMP	40.2 Ω 1% pull-down to gnd	Trace should be 10-mil wide with 20-mil spacing.	
GVREF	1 kΩ 1% pull-up to Vcc1_5 1 kΩ 1% pull-down to gnd	Signal voltage level = 1/2 of Vcc1_5. Need 0.1 µF cap at pin.	
DVOCD[11:0] DVOCCLK DVOCCLK# DVOCHSYNC DVOCVSYNC DVOCBLANK#		If unused, these signals can be left as NC.	
DVOCFLDSTL	100 kΩ pull-down to gnd	Pull-down resistor required only if signal is unused (10 k-100 k). It is up to DVO device to drive this signal.	
DVOBCINTR#	100 kΩ pull-up to Vcc1_5	Pull-up resistor required only if signal is unused (10 k-100 k). It is up to the DVO device to drive this signal.	
DVOBCCLKINT	100 kΩ pull-down to gnd	Pull-down resistor required only if signal is unused (10 k-100 k). It is up to the DVO device to drive this signal.	
DVOBD[11:0] DVOBCLK DVOBCLK# DVOBHSYNC DVOBVSYNC DVOBBLANK#		If unused, these signals can be left as NC.	
DVOBFLDSTL (pin M2)	100 kΩ pull-down to gnd	Pull-down resistor required only if this signal is unused (10 k-100 k).	
MI2CCLK, MI2CDATA	2.2 kΩ pull-up to Vcc1_5	Pull-up resistor required on each signal even if they are unused (2.2 k-100 k). This signal is 1.5-V tolerant. It may require voltage translation circuit.	
MDVICLK, MDVIDATA	2.2 kΩ pull-up to Vcc1_5	Pull-up resistor required on each signal even if they are unused (2.2 k-100 k). This signal is 1.5-V tolerant. It may require voltage translation circuit.	
MDDCCLK, MDDCDATA	2.2 kΩ pull-up to Vcc1_5	Pull-up resistor required on each signal even if they are unused (2.2 k-100 k). This signal is 1.5V tolerant. It may require voltage translation circuit.	
ADDID[6:0]		Leave as NC.	
ADDID7	1 kΩ pull-down to gnd if DVO device is onboard	If DVO interface is not used, this signal can be left as “no connect”. Otherwise, pull-down is needed.	
DVODETECT	1 kΩ pull-up to Vcc1_5 if DVO interface is unused	If DVO interface is used, leave as NC. This signal has internal pull-down.	
DPMS		Connect to 1.5-V version of ICH4-M’s SUSCLK or a clock that runs during S1. See Figure 154.	

Figure 154. DPMS Clock Implementation



16.6.4.3. DAC

Pin Name	System Pull-up /Pull-down	In Series	Notes	✓
REFSET	127 Ω 1% pull-down to gnd			
RED #	Connect to gnd		Need to connect to RED's return path	
BLUE #	Connect to gnd		Need to connect to BLUE's return path	
GREEN#	Connect to gnd		Need to connect to GREEN's return path	
RED	On GMCH side of ferrite bead: 75 Ω 1% pull-down to gnd, 3.3 pF cap to gnd, ESD diode protection for Vcc1_5 On VGA side of ferrite bead: 3.3 pF cap to gnd	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
BLUE	On GMCH side of ferrite bead: 75 Ω 1% pull-down to gnd, 3.3 pF cap to gnd, ESD diode protection for Vcc1_5 On VGA side of ferrite bead: 3.3 pF cap to gnd	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
GREEN	On GMCH side of ferrite bead: 75 Ω 1% pull-down to gnd, 3.3 pF cap to gnd, ESD diode protection for Vcc1_5 On VGA side of ferrite bead: 3.3 pF cap to gnd	Ferrite bead: 75 Ω at 100 MHz	Ferrite bead for EMI suppression between GMCH and VGA connector.	
HSYNC	On VGA side of seires resistor: 33 pF cap to gnd	39 Ω	Use unidirectional buffer to prevent potential electrical overstress and illegal operation of the GMCH.	
VSYNC	On VGA side of series resistor: 33 pF cap to gnd	39 Ω	Use to unidirectional buffer to prevent potential electrical overstress and illegal operation of the GMCH.	

16.6.5. Miscellaneous

Pin Name	System Pull-up/Pull-down	Notes	✓
EXTTS	10 kΩ 1% pull-up to Vcc3_3		
DPWR# (pin AA22)		Connect to the processor.	
LCLKCTLB		Leave as NC if not used.	
LCLKCTLA		Leave as NC if not used.	
GST[2:0]	Leave as NC or 1 kΩ pull-up to Vcc1_5	These pins have internal pull-down.	

16.6.6. GMCH Decoupling Recommendations

Pin Name	Configuration	F	Qty	Notes	✓
VCC	Connect to Vcc1_2	0.1 µF 150 µF 10 µF	4 2 1	Bulk decoupling is based on VR solutions used on CRB design.	
VTTLF	Connect to VCCP	0.1 µF 150 µF 10 µF	2 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VTTHF		0.1 µF	5	Connect pins directly to caps.	
VCCHL	Connect to Vcc1_2	0.1 µF 10 µF	2 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCCSM	Connect to VccSus2_5	0.1 µF 150 µF	11 2	Bulk decoupling is based on VR solutions used on CRB design.	
VCCQSM	Connect to VccSus2_5 with filter network	0.1 µF 4.7 µF+1Ω	1 1 each	0.68 uH from power supply to GMCH pins. On GMCH side of inductor: one 0.1 µF to GND, 4.7 µF + 1 Ω to GND	
VCCASM	Connect to Vcc1_2 with network filter	0.1 µF 100 µF	1 1	1uH from power supply to GMCH pins, with caps on GMCH side of inductor.	
VCCDVO	Connect to Vcc1_5	0.1 µF 10 µF 150 µF	2 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCCADAC	Connect to Vcc1_5	0.01 µF 0.1 µF 220 µF (no stuff)	1 1 1	Route VSSADAC to other side of the caps, then to ground. A 0-ohm 0805 resisor is recommended between the caps and Vcc1_5. This and the 220 µF cap footprints are there in case there is noise issue with the VGA supply.	
VCCALVDS	Connect to Vcc1_5	0.1 µF 0.01 µF	1 1	Route VSSALVDS to other side of the caps, then to ground.	
VCCDLVDS	Connect to Vcc1_5	0.1 µF 22 µF 47 µF	1 1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCCTXLVDS	Connect to VccSus2_5	0.1 µF 22 µf 47 µF	3 1 1	Bulk decoupling is based on VR solutions used on CRB design. This power signal may be optionally connected to Vcc2_5 and powered off in S3.	
VCCGPIO	Connect to Vcc3_3	0.1 µF 10 µF	1 1	Bulk decoupling is based on VR solutions used on CRB design.	
VCCAHPLL	Connect to Vcc1_2	0.1 µF	1		

Pin Name	Configuration	F	Qty	Notes	✓
VCCAGPLL	Connect to Vcc1_2	0.1 µF	1		
VCCADPLLA	Connect to Vcc1_2 with network filter	0.1 µF 220 µF	1 1	0.1 uH from power supply to GMCH pins, with caps on GMCH side of inductor.	
VCCADPLLB	Connect to Vcc1_2 with network filter	0.1 µF 220 µF	1 1	0.1 uH from power supply to GMCH pins, with caps on GMCH side of inductor.	

NOTE: Decoupling guidelines are recommendations based on our reference board design. Customers will need to take layout & PCB board design into consideration when deciding on overall decoupling solution.

16.7. ICH4-M Checklist

Note: All inputs to the ICH4-M must not be left floating. Many GPIO signals are fixed inputs that must be pulled up to different sources.

16.7.1. PCI Interface and Interrupts

Pin Name	System Pull-up /Pull-down	Notes	✓
PCI_DEVSEL#	8.2 kΩ pull-up to Vcc3_3		
PCI_FRAME#	8.2 kΩ pull-up to Vcc3_3		
PCI_GPIO0 / REQA# PCI_GPIO1 / REQB_L/REQ5#	8.2 kΩ pull-up to Vcc3_3	Each signal requires a pull-up resistor.	
PCI_GPIO16 / GNTA#		GNTA is also used as a strap for “top block swap”. It is sampled on the rising edge of PWROK. By default, this signal is HIGH (strap function DISABLED). It can be enabled by a pull-down to gnd through a 1-kΩ resistor.	
PCI_IRDY#	8.2 kΩ pull-up to Vcc3_3		
PCI_LOCK#	8.2 kΩ pull-up to Vcc3_3		
PCI_PERR#	8.2 kΩ pull-up to Vcc3_3		
PCI_SERR#	8.2 kΩ pull-up to Vcc3_3		
PCI_STOP#	8.2 kΩ pull-up to Vcc3_3		
PCI_TRDY#	8.2 kΩ pull-up to Vcc3_3		
PCI_REQ[4:0]#	8.2 kΩ pull-up to Vcc3_3	Each signal requires a pull-up resistor.	
PCI_PME#		ICH4-M has internal pull-up to VccSus3_3.	
PCI_RST#, PAR, GNT[4:0]#, GNTA#, GNTB#	None		
APICCLK	0 Ω to gnd	Can also be connected directly to ground.	
APICD[1:0]	10 kΩ pull-down to gnd	If XOR chain testing is **NOT** used: Pull down the signals through a shared 10 kΩ resistor. If XOR chain testing is used: Each signal requires a separate 10-kΩ pull-down resistor.	
INT_IRQ[15:14]	8.2 kΩ pull-up to Vcc3_3	Each signal requires a pull-up resistor.	
INT_PIRQ#[A:D] INT_PIRQE#/GPIO2 INT_PIRQF#/GPIO3 INT_PIRQG#/GPIO4 INT_PIRQH#/GPIO5	8.2 kΩ pull-up to Vcc3_3	External pull up is required for INT_PIRQ#[A:D]. External pull up is required when muxed signal (INT_PIRQ[E:H]#/ GPIO[2:5]) is implemented as PIRQ.	
INT_SERIRQ	8.2 kΩ pull-up to Vcc3_3		

16.7.2. GPIO

Note: Ensure ALL unconnected signals are OUTPUTS ONLY. Only GPIO[7:0] are 5 V tolerant.

Recommendations	✓
GPIO[7] & [5:0]: • These pins are in the Main Power Well. Pull-ups must use the $V_{CC}3\_3$ plane. • Unused core well inputs must be pulled up to $V_{CC}3\_3$. • GPIO[1:0] can be used as REQ[B:A]#. • GPIO[1] can be used as PCI REQ[5]#. • GPIO[5:2] can be used as PIRQ[H:E]#. • These signals are 5 V tolerant. • These pins are inputs.	
GPIO[8] & [13:11]: • These pins are in the Resume Power Well. Pull-ups go to $V_{CC}Sus3\_3$ plane. • Unused resume well inputs must be pulled up to $V_{CC}Sus3\_3$. • These are the only GPIs that can be used as ACPI compliant wake events. • These signals are not 5V tolerant. • GPIO[8] can be used as SMC_EXTSMI# • GPIO[11] can be used as SMBALERT#. • GPIO[13] can be used as SMC_WAKE_SCI# • These pins are inputs	
GPIO[23:16]: • Fixed as output only. Can be left NC. • In Main Power Well ($V_{CC}3\_3$). • GPIO[17:16] can be used as GNT[B:A]#. • GPIO[17] can be used as PCI GNT[5]#. • STP_PCI#/GPIO[18] – used in mobile as STP_PCI# only. • SLP_S1#/GPIO[19] - used in mobile as SLP_S1# only. • STP_CPU#/GPIO[20] - used in mobile as STP_CPU# only. • C3_STAT#/GPIO[21] - used in mobile as C3_STAT# only. • CPUPERF#/GPIO[22] - open drain signal. Used in mobile as CPUPERF# only. • SSMUXSEL/GPIO[23] - used in mobile as SSMUXSEL only.	
GPIO[28,27,25,24]: • I/O pins. Default as outputs. Can be left as NC. • These pins are in the Resume Power Well. • CLKRUN#/GPIO[24] (Note: use $V_{CC}3\_3$ if signal is required to be pulled-up) • GPIO[28, 27, 25] from resume power well ($V_{CC}Sus3\_3$). (Note: use $V_{CC}3\_3$ if this signal is required to be pulled-up) • These signals are NOT 5-V tolerant. • GPIO[25] can be used as AUDIO_PWRDN.	
GPIO[43:32]: • I/O pins. From main power well ($V_{CC}3\_3$). • Default as outputs when enabled as GPIOs. • These signals are **NOT** 5-V tolerant. • GPIO[32] can be used as AGP_SUSPEND#. • GPIO[33] can be used as KSC_VPPEN#. • GPIO[34] can be used as SER_EN. • GPIO[35] can be used as FWH_WP#. • GPIO[36] can be used as FWH_TBL#. • GPIO[40] can be used as IDE_PATADET. • GPIO[41] can be used as IDE_SATADET.	

16.7.3. AGP_BUSY# Design Requirement

Signal	System Pull-up/Pull-down	Notes	✓
AGPBUSY#	10 KΩ pull-up to Vcc3_3	This ICH4-M signal requires a pull-up to the switched 3.3-V rail (powered OFF during S3). This ICH4-M signal must be connected to the AGP_BUSY# output of GMCH.	

NOTE: Please also consult Intel for the latest AGP Busy and Stop signal implementation.

16.7.4. (SMBus) System Management Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
SM_INTRUDER#	100 kΩ pull-up to VccRTC	RTC well input requires pull-up (10 k-100 k) to reduce leakage from coin cell battery in G3.	
SMB_ALERT#/ GPIO[11]	10 kΩ pull-up to V3ALWAYS		
SMBCLK, SMBDATA, SMLINK[1:0]	Pull-up to V3ALWAYS	Require external pull-up resistors. Pull up value is determined by bus characteristics. CRB schematics use 10 kΩ pull-up resistors. The SMBus and SMLink signals must be connected together externally in S0 for SMBus 2.0 compliance: SMBCLK connected to SMLink[0] and SMBDATA connected to SMLink[1].	

16.7.5. AC ’97 Interface

Pin Name	System Pull-up/Pull-down	Series Termination Resistor	Notes	✓
AC_BIT_CLK	None	33-47 Ω	The internal pull-down resistor is controlled by the AC’97 Global Control Register, ACLINK Shut Off bit: 1 = enabled; 0 = disabled When no AC'97 devices are connected to the link, BIOS must set the ACLINK Shut Off bit for the internal keeper resistors to be ENABLED. At that point, pull-ups/pull-downs are NOT needed on ANY of the link signals.	
AC_SDATAIN[2:0]	None	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. A series termination resistor is required for the SECONDARY and TERTIARY CODEC if the resistor is not found on CODEC.	
AC_SDATAOUT	None	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. One series termination resistor is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card.	
AC_SYNC	None	33-47 Ω	A series termination resistor is required for the PRIMARY CODEC. One series termination resistor is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card.	

16.7.6. ICH4-M Power Management Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
PM_DPRSLPVR		Signal has integrated pull-down in ICH4-M.	
PM_SLP_S1#/GPIO19 PM_SLP_S3#, PM_SLP_S4#, PM_SLP_S5#		Signals driven by ICH4-M.	
PM_BATLOW#	10 kΩ pull-up to V3ALWAYS IF NOT USED	Pull up is not required if it is used. However, signal must not float if it is NOT being used	
PM_CLKRUN#	10 kΩ pull-up to Vcc3_3		
PM_PWRBTN#		Has integrated pull-up of 18 kΩ – 42 kΩ.	
PM_PWROK	Weak pull-down to gnd	RTC well input requires pull-down to reduce leakage from coin cell battery in G3. Input must not float in G3. This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_5 have reached their nominal voltages. CRB uses 100 KΩ pull-down.	
PM_RI#	8.2 kΩ-10 kΩ pull-up to V3ALWAYS	If this signal is enabled as a wake event, it needs to be powered during a power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.	
PM_RSMRST#	Weak pull-down to gnd	RSMRST# is a RTC well input and requires pull-down to reduce leakage from coin cell battery in G3. Input must not float in G3. This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_5 have reached their nominal voltages. CRB uses 100 KΩ pull-down. Timing Requirement: See LAN_RST#.	
PM_THRM#	8.2 kΩ Pull-up to Vcc3_3 If TEMP SENSOR not sued	External pull-up not required if connecting to temperature sensor.	
PM_SYSRST#	10 kΩ pull-up to V3ALWAYS if not actively driven.	This signal to ICH4-M should not float. It needs to be at valid level all the time.	

16.7.7. FWH/LPC Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
LPC_AD[3:0]		No extra pull-ups required. Connect straight to FWH/LPC.	

16.7.8. USB Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
USB_OC[5:0]#	10 kΩ pull-up to V3ALWAYS if not driven	No pull-up is required if signalsl are driven.. Signals must NOT float if they are not being used.	
USBRBIAS, USBRBIAS#	22.6 Ω ± 1% pull-down to gnd	Connect signals together and pull down through a common resistor, placed within 500 mils of the ICH4-M. Avoid routing next to clock pin.	

16.7.9. Hub Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
HUB_RCOMP	48.7 Ω 1% pull-up to to Vcc1_5	Place resistor within 0.5” of ICH4-M pad using a thick trace.	
HUB_VREF, HUB_VSWING	See Figure 155 and Figure 156.	HUB_VREF signal voltage level = 0.35 V ± 8%. HUB_VSWING signal voltage level = 0.80 V ± 8%. Three options are available for generating these references.	
HUB_PD11	56 Ω pull-down to gnd		

Figure 155. Single or Locally Generated GMCH and ICH4-M HIVREF/HI_VSWING Circuit

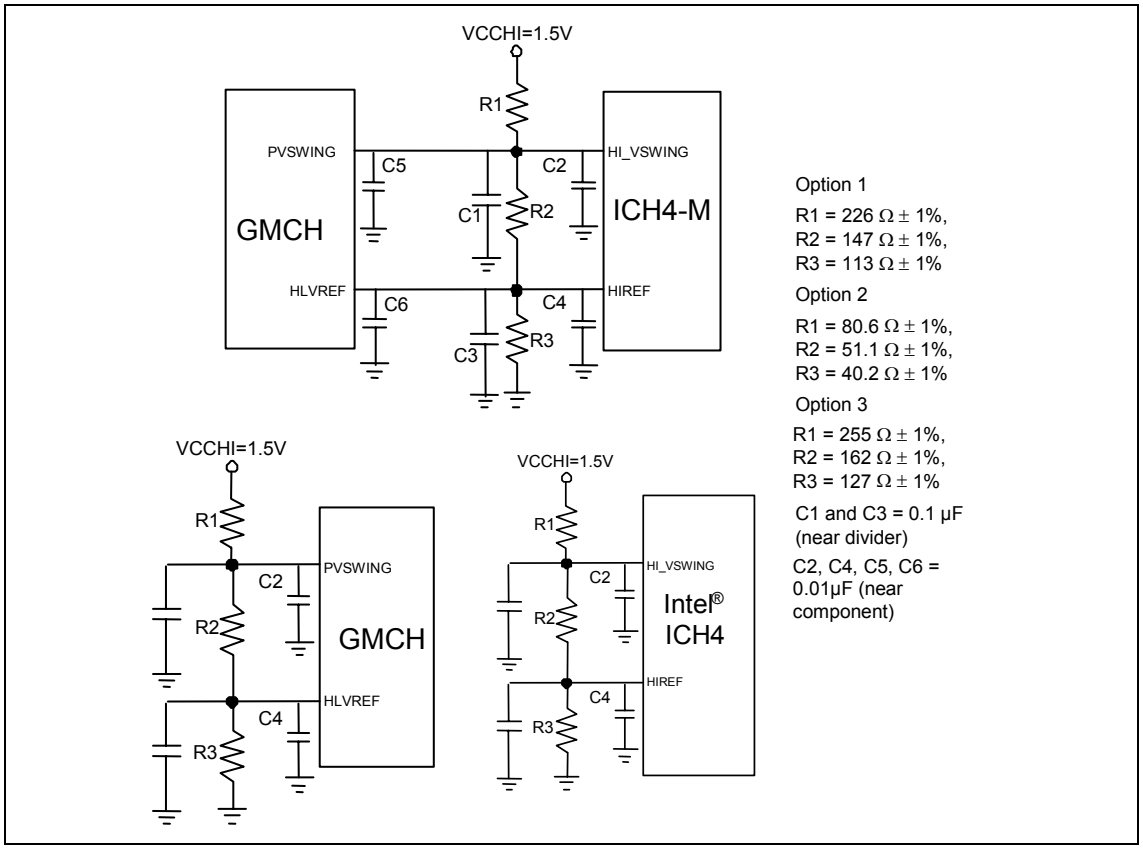
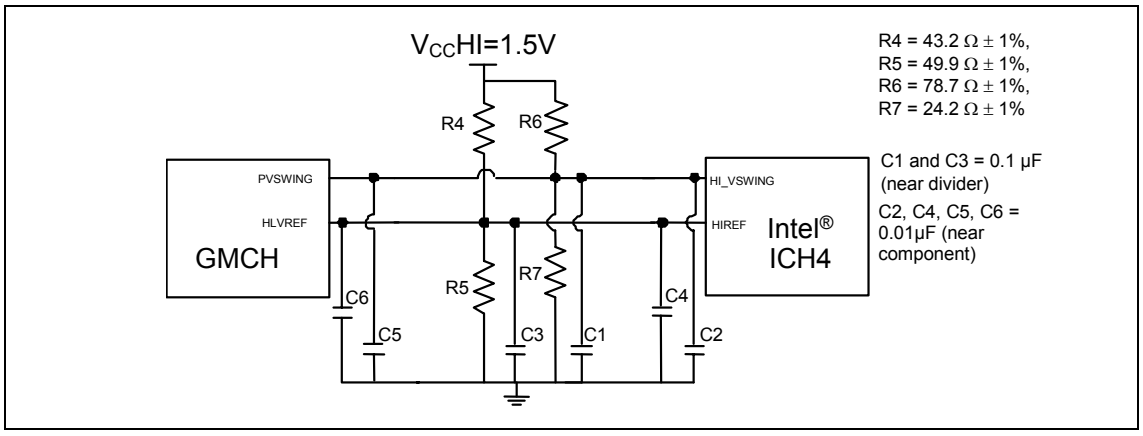


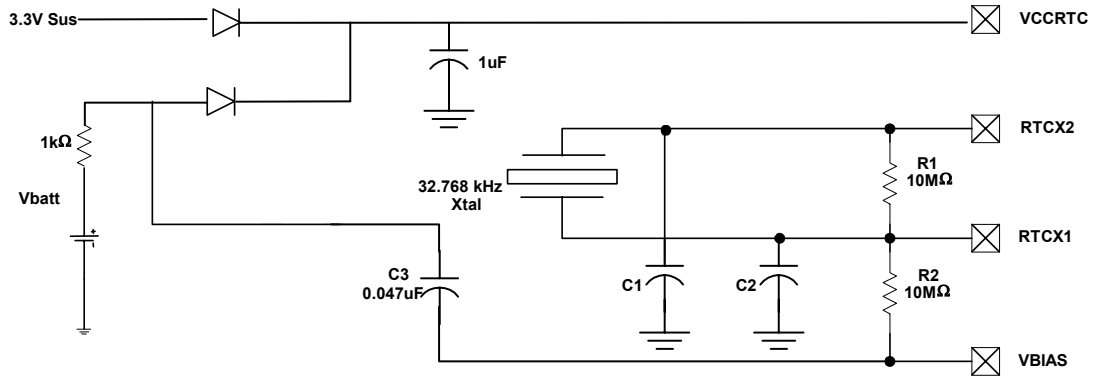
Figure 156. Single Generated GMCH and ICH4-M VSWING/VREF Reference Voltage/ Local Voltage Divider Circuit for VSWING/VREF



16.7.10. RTC Circuitry

Pin Name	System Pull-up/Pull-down	In Series	Notes	✓
RTCRST#	180 kΩ pull-up to VccRTC		RTCRST# requires 18-25 ms delay. Use a 0.1 µF cap to ground Pull up with 180 kΩ resistor. Any resistor or capacitor combination that yields a time constant is acceptable.	
CLK_RTCX1, CLK_RTCX2			Connect a 32.768 kHZ crystal oscillator across these pins with a 10 MΩ resistor and a decoupling cap at each signal. Values for C1 and C2 are dependent on crystal. See Figure 157.	
CLK_VBIAS		1 KΩ 0.047 µF	Connect to CLK_RTCX1 through a 10 MΩ resistor. Connect to VBATT through a 1 kΩ in series with a 0.047 µF capacitor.	

Figure 157. External Circuitry for the RTC



Notes
Reference Designators Arbitrarily Assigned
3.3V Sus is Active Whenever System Plugged In
Vbatt is Voltage Provided By Battery

VBIAS, VCCRTC, RTCX1, and RTCX2 are ICH4-M pins
VBIAS is used to bias the ICH4 Internal Oscillator
VCCRTC powers the RTC well of the ICH4-M
RTCX1 is the Input to the Internal Oscillator
RTCX2 is the feedback for the external crystal

16.7.11. LAN Interface

Pin Name	System Pull-up/Pull-down	Notes	✓
LAN_JCLK		Connect to LAN_CLK on the platform LAN Connect Device. If LAN interface is not used, leave the signal unconnected (NC).	
LAN_RST#	10 kΩ pull-down to gnd If ICH4-M LAN not used	Timing Requirement: Signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. **NOTE**: If ICH4-M LAN controller is NOT used, pull LAN_RST# down through a 10 kΩ resistor.	
LAN_RXD[2:0], LAN_TXD[2:0]		Connect to LAN_RXD on the platform LAN Connect Device. If LAN interface is not used, leave the signal unconnected (NC)	
LAN_RSTYSNC		Connect to LAN_RSTSYNC on Platform LAN Connect Devce. If LAN interface is not used, leave the signal unconnected (NC).	

16.7.12. Primary IDE Interface

Pin Name	System Pull-up/Pull-down	Series Damping	Notes	✓
IDE_PDD[15:0]			These signals have integrated series resistors.	
IDE_PDA[2:0], IDE_PDCS1#, IDE_PDCS3#, IDE_PDDACK#, IDE_PDIOW#, IDE_PDIOR#			These signals have integrated series resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	
IDE_PDDREQ			These signals have integrated series resistors and pull-down resistors in ICH4-M.	
IDE_PIORDY	4.7 kΩ pull-up to Vcc3_3		This signal has integrated series resistor in ICH4-M.	

16.7.13. Secondary IDE Interface

Pin Name	System Pull-up/Pull-down	Series Damping	Notes	✓
IDE_SDD[15:0]			These signals have integrated series resistors.	
IDE_SDA[2:0], IDE_SDCS1#, IDE_SDCS3#, IDE_SDDACK#, IDE_SDIOW#, IDE_SDIOR#			These signals have integrated series resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	
IDE_SDDREQ			These signals have integrated series resistors and pull-down resistors in ICH4-M.	
IDE_SIORDY	4.7 kΩ pull-up to Vcc3_3		This signal has integrated series resistor in ICH4-M.	
IDE_SRST#		22-47 Ω	The signal must be buffered to provide IDE_RST# for improved signal integrity.	

16.7.14. Miscellaneous Signals

Pin Name	System Pull-up/Pull-down	Notes	✓
SPKR		SPKR is a strapping option for the TCO Timer Reboot function and is sampled on the rising edge of PWROK. An integrated weak pull-down is enabled only at boot/reset. Status of strap is readable via the NO_REBOOT bit (D31:F0, Offset D4h, bit 1) 1 = disabled; 0 = enabled (normal operation) To disable, a jumper can be populated to pull SPKR high. Value of pull-up must be such that the voltage divider output caused by the pull-up, effective impedance of speaker and codec circuit, and internal pull-down will be read as logic high (0.5 * Vcc3_3 to Vcc3_3 + 0.5)	

16.7.15. ICH4-M Decoupling Recommendations

Pin Name	Configuration	Value	Q	Notes	✓
VCC1.5	Connect to Vcc1_5	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF and one 100 µF.	
VCC3.3	Connect to Vcc3_3	0.1 µF	6	Low frequency decoupling is dependent on layout and power supply design. CRB uses two 22 µF.	
VCCSUS1.5	Connect to V1_5ALWAYS	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 10 µF.	
VCCSUS3.3	Connect to V3ALWAYS	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF.	
VCCLAN1.5	Connect to VccSus1_5	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF.	
VCCLAN3.3	Connect to VccSus3_3	0.1 µF 4.7 µF	2 1	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF.	
VCC5REF	Connect to Vcc5 through 1 kΩ	0.1 µF 1 µF	1 1	Caps from VCC5REF to ground. Also connect diode from VCC5REF to Vcc3_3.	
VCC5REFSUS	Connect to V5ALWAYS through 1 kΩ	0.1 µF 1 µF	1 1	Caps from VCC5REFSUS to ground. Also connect diode from VCC5REFSUS to V3ALWAYS.	
VCC_CPU_IO	Connect to VCCP	0.1 µF 1 µF	1 1		
VCCPLL	Connect to Vcc1_5	0.1 µF 0.01 µF	1 1		
VCCRTC	Connect to VccRTC	0.1 µF	1		
VCCHI	Connect to Vcc1_5	0.1 µF	2	Low frequency decoupling is dependent on layout and power supply design. CRB uses one 22 µF.	

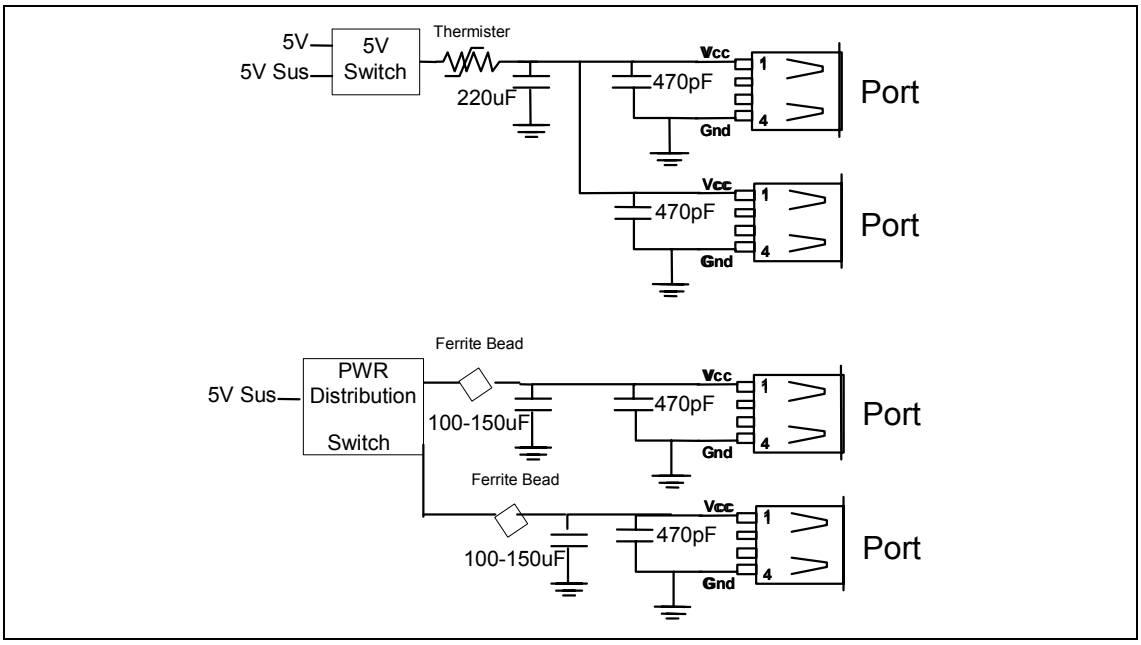
NOTE: All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, & PCB board design into consideration when deciding on their overall decoupling solution. Capacitors should be place less than 100 mils from the package

16.8. USB Power Checklist

16.8.1. Downstream Power Connection

Pin Name	Notes	✓
USB_VCC[E:A]	One 220 µF and two 470 pF are recommended for every two power lines. Either a thermister or a power distribution switch (with short circuit and thermal protection) is required. See Figure 158.	

Figure 158. Good Downstream Power Connection



16.9. FWH Checklist

16.9.1. Resistor Recommendations

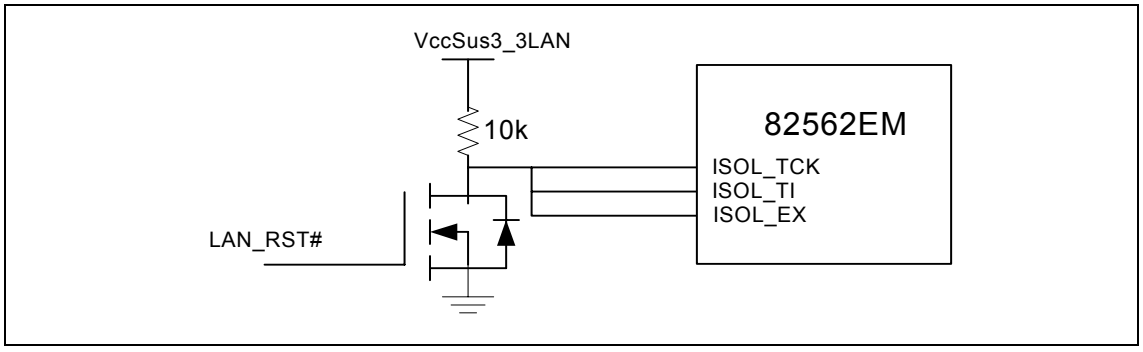
Pin Name	System Pull-up/Pull-down	Series Damping	Notes	✓
FGPI[4:0]	100 Ω pull-down to gnd		Each signal requires a 100 Ω pull-down resistor.	
IC	10 kΩ pull-down to gnd			
RST#		100 Ω		
ID[3:0]			Signals are recommended to be connected to test points.	
RSVD[5:1]			Signals are recommended to be connected to test points.	
NC[8:1]			The signals should be left as NC (“Not Connected”)	

16.10. LAN / HomePNA Checklist

16.10.1. Resistor Recommendations (for 82562ET / 82562EM)

Pin Name	System Pull-up/Pull-down	Term Resistor	Notes	✓
ISOL_EX, ISOL_TCK, ISOL_TI	10 kΩ pull-up to VccSus3_3LAN		If LAN is enabled, all three signals needs to be pulled up to VccSus3_3LAN through a common 10 kΩ pull-up resistor. See Figure 159.	
RBIAS10	549 Ω ± 1%pull-down to gnd			
RBIAS100	619 Ω ± 1%pull-down to gnd			
RDP, RDN		121 Ω ±1%	Connect 121-ohm resistor between RDP and RDN.	
TDP, TDN		100 Ω ± 1%	Connect 100-ohm resistor between TDP and TDN.	
TESTEN	100 Ω pull-down to gnd			
X1, X2			Connect a 25-MHz crystal across these two pins. 22pF on each pin to ground.	
LAN_RST#			On CRB, the power monitoring logic waits for PM_PWROK to go high before deasserting this signal to enable the LAN device. It also keeps this signal high during S3. See Figure 159.	

Figure 159. LAN_RST# Design Recommendation

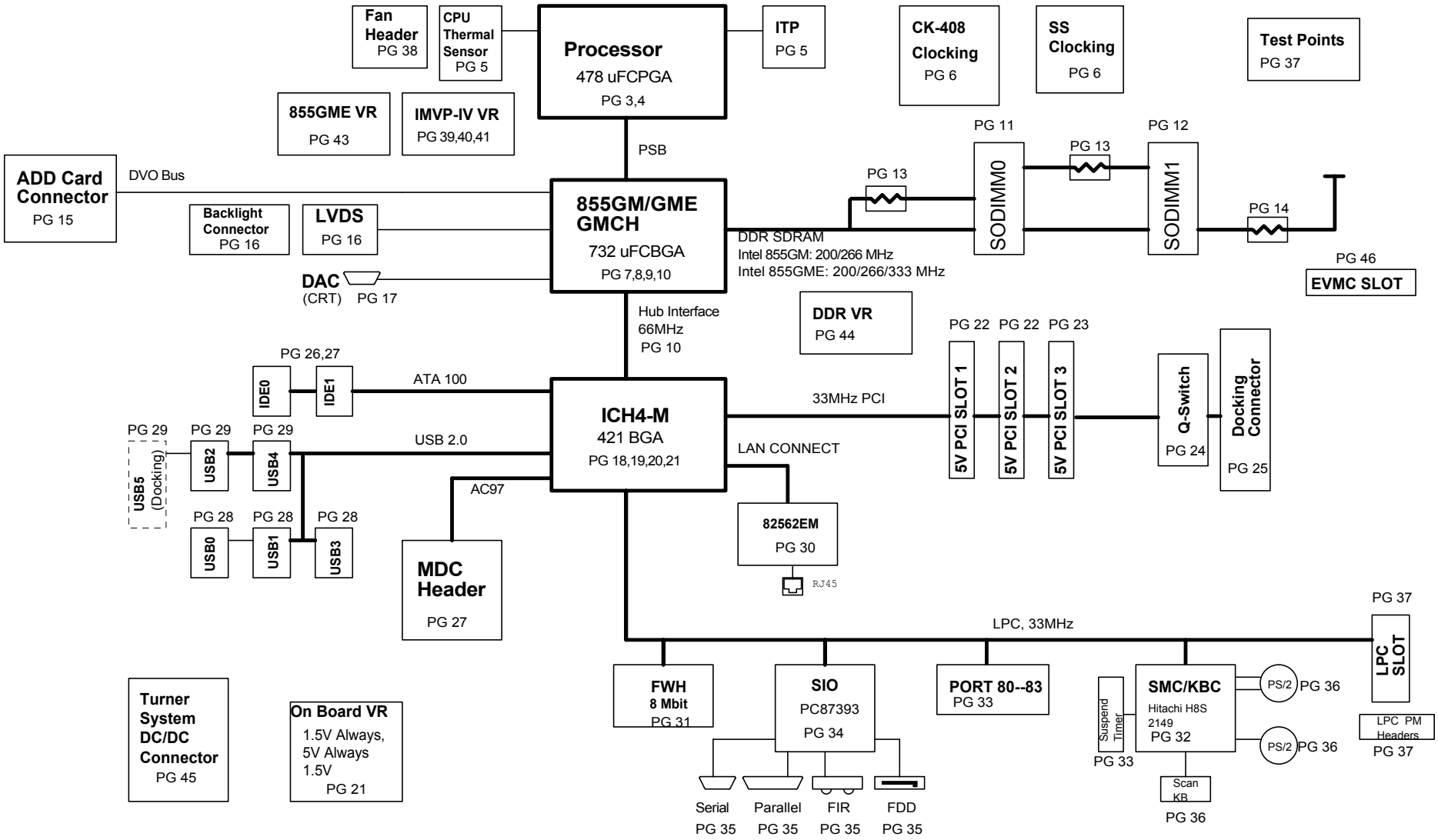


16.10.2. Decoupling Recommendations

Signal Name	Configuration	F	Qty	Notes	✓
VCC[2:1], VCCP[2:1], VCCA[2:1], VCCT[4:1]	Connect to VccSus3_3LAN	0.1 µF 4.7 µF	4 2		
VCCR[2:1]	Connect to VccSus3_3LAN via filter	0.1 µF 4.7 µF	1 1	4.7 uH from power supply to VCCR pins. Caps on VCCR side of the inductor.	

17. Schematics

Refer to the following page for schematics.



Title: BLOCK DIAGRAM			
Size: A	Project: Intel 855GM/GME CRB	Document Number	Rev: 4.401
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Intel 855GM/GME CUSTOMER REFERENCE PLATFORM

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

+VDC	Primary DC system power supply (10 to 21V)
+VCC_CORE	Core voltage for processor
+VCCP	1.05V rail for processor PSB, 855GME PSB
+V1.8S	1.8V for processor PLL and VID circuitry
+V1.25S	1.25V DDR Termination voltage
+V1.35S	1.35V for 855GM core
+V1.5S	1.5V switched power rail (off in S3-S5)
+V1.5ALWAYS	1.5V always on power rail
+V1.5	1.5V power rail (off in S4-S5)
+V2.5	2.5V power rail for DDR
+V3.3ALWAYS	3.3V always on power rail
+V3.3	3.3V power rail (off in S4-S5)
+V3.3S	3.3V switched power rail (off in S3-S5)
+V5ALWAYS	5.0V for ICH4M's VCC5REFSUS
+V5	5.0V power rail (off in S4-S5)
+V5S	5.0V switched power rail (off in S3-S5)
+V12S	12.0V switched power rail (off in S3-S5)
-V12S	-12.0V switched power rail for PCI (off in S3-S5)

I²C / SMB Addresses

Device	Address	Hex	Bus
Clock Generator	1101 001x	D2	SMB_ICH_S
Spread Spectrum Clock	1101 010x	D4	SMB_ICH_S
SO-DIMM0	1010 000x	A0	SMB_ICH_S
SO-DIMM1	1010 001x	A2	SMB_ICH_S
Thermal Sensor Header	1001 000x	90	SMB_ICH
LVDS Backlight Inverter	____ ____	__	SMB_ICH
Dock Connector	____ ____	__	SMB_ICH
Smart Battery	0001 011x	16	SMB_SB
Smart Battery Charger	0001 001x	12	SMB_SB
Smart Selector	0001 010x	14	SMB_SB
Bluetooth Header	____ ____	__	SMB_SB
LPC Pwr Mngmnt Header	____ ____	__	SMB_SB
LPC Pwr Mngmnt Header	____ ____	__	SMB_THRM
Thermal Diode	1001 110x	9C	SMB_THRM
EV Support:			
DV0-DV3	0101 0001	51	SMB_ICH
V5-V8	0101 0010	52	SMB_ICH
PV0-PV3	0101 0011	53	SMB_ICH
DV4	0101 0100	54	SMB_ICH
V9-V12	0101 0101	55	SMB_ICH
I1-I4	0101 0110	56	SMB_ICH
EP1-EP4	0101 0111	57	SMB_ICH
PV4	0101 0100	58	SMB_ICH
V1-V4	0101 1001	59	SMB_ICH

Default Jumper Settings

Jumper	Default	Option	Description	Page
J7B2	1-X	1-2	GMCH Strap: PSB Voltage	08
J7B3	1-X	1-2	GMCH Strap: DVO Strap	08
J7B4	1-2	1-X	GMCH Strap: Clock Config	08
J7B5	1-2	1-X	GMCH Strap: Clock Config	08
J7C1	1-2	1-X	GMCH Strap: Clock Config	08
J6E1	2-3	1-2	LVDS EV	08
J6D1	1-X	1-2	No-Shunt Default	09
J4F1	1-X	1-2	No-Shunt Default	09
J2J3	1-X	1-2	CMOS Clear	19
J8J2	2-3	1-2	CRB/SV Detect	19
J9E2	1-2	2-3	Moon ISA Support	23
J9E4	1-2	2-3	Moon ISA Support	23
J9E5	2-3	1-2	Moon ISA Support	23
J9B1	1-X	1-2	SMC/KBC Programming	32
J8A2	1-2	2-3	SMC/KBC Disable	32
J9A1	1-X	1-2	KBC 60/64 Decode Disable	32
J9A3	1-X	1-2	SMC_LID Disable	32
J8A1	1-2	1-X	NMI Jumper	33
J9H1	1-X	1-2	Port 80-81/82-83 Select	33
J9G2	1-2	2-3	SIO Disable	34
J3G1	1-X	1-2	DDR EV Support	44
J1H4	1-X	1-2	A_FAN_P1	46
J1H5	1-X	1-2	A_FAN_P0	46

PCI Devices

Device	IDSEL #	REQ	GNT #	Interrupts	PC/PCI
Slot 1	AD16	1	1	F, G, H, E	A
Slot 2	AD17	2	2	G, F, E, H	A
Slot 3	AD18	3	3	C, D, B, A (E, F, G, H optional)	A
Docking	AD28	4	4	B, C, D, A	B
LAN	(AD24 internal)			A, B	

LEDs and Switches

LED	Page	Reference
Primary IDE	27	DS2J2
Secondary IDE	27	DS2J1
SMC/KBC Num Lock	32	DS8A1
SMC/KBC Scroll Lock	32	DS8A2
SMC/KBC Caps Lock	32	DS8B1
VID0	34	DS1J1
VID1	34	DS1J2
VID2	34	DS1J3
VID3	34	DS1J4
VID4	34	DS2J3
VID5	34	DS2J4
S0 State	38	DS1H1
S1 State	38	DS1H3
S3 State	38	DS1H2
S4 State	38	DS2H2
S5 State	38	DS2H1

Switch	Page	Reference
Virtual Battery On/Off	32	SW8A1
Lid	32	SW9A1
Power On/Off	45	SW8J1
Reset	45	SW7J1

Wake Events

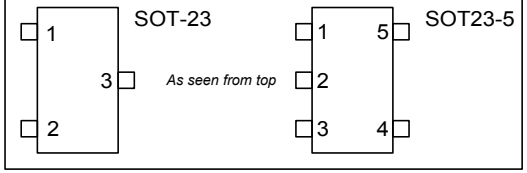
RI# (Ring Indicate) from serial port
PME# (Power Management Event) from PCI/mini-PCI slots, ADD slot, LPC slot
LAN Connect Interface from 82562EM
LID switch attached to SMC
USB
AC97 wake on ring
SmLink for AOL II
Hot Key from the scan matrix keyboard

Net Naming Conventions

Suffix
= Active Low Signal

Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



Power States

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*	+V*S	Clocks
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend To Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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Size: A	Project: Intel 855GM/GME CRB	Document Number: <Doc>	Rev: 4.401
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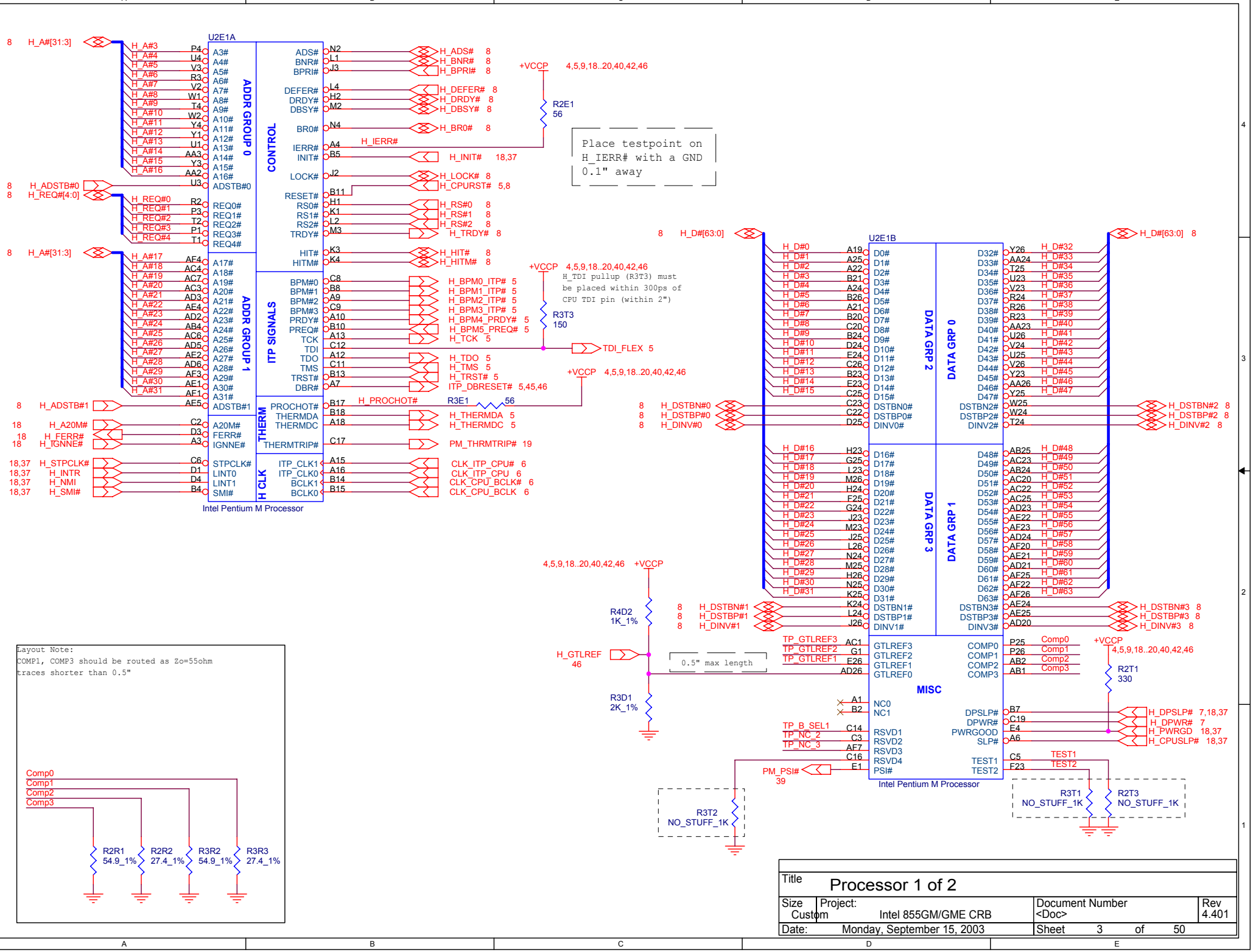
U2E1A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
ITP SIGNALS
THERM
H CLK
Intel Pentium M Processor
U2E1B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Intel Pentium M Processor
Place testpoint on H_IERR# with a GND 0.1" away
H_TDI pullup (R3T3) must be placed within 300ps of CPU TDI pin (within 2")
0.5" max length
Layout Note:
COMP1, COMP3 should be routed as Zo=55ohm traces shorter than 0.5"
Title
Processor 1 of 2
Size
Custom
Project:
Intel 855GM/GME CRB
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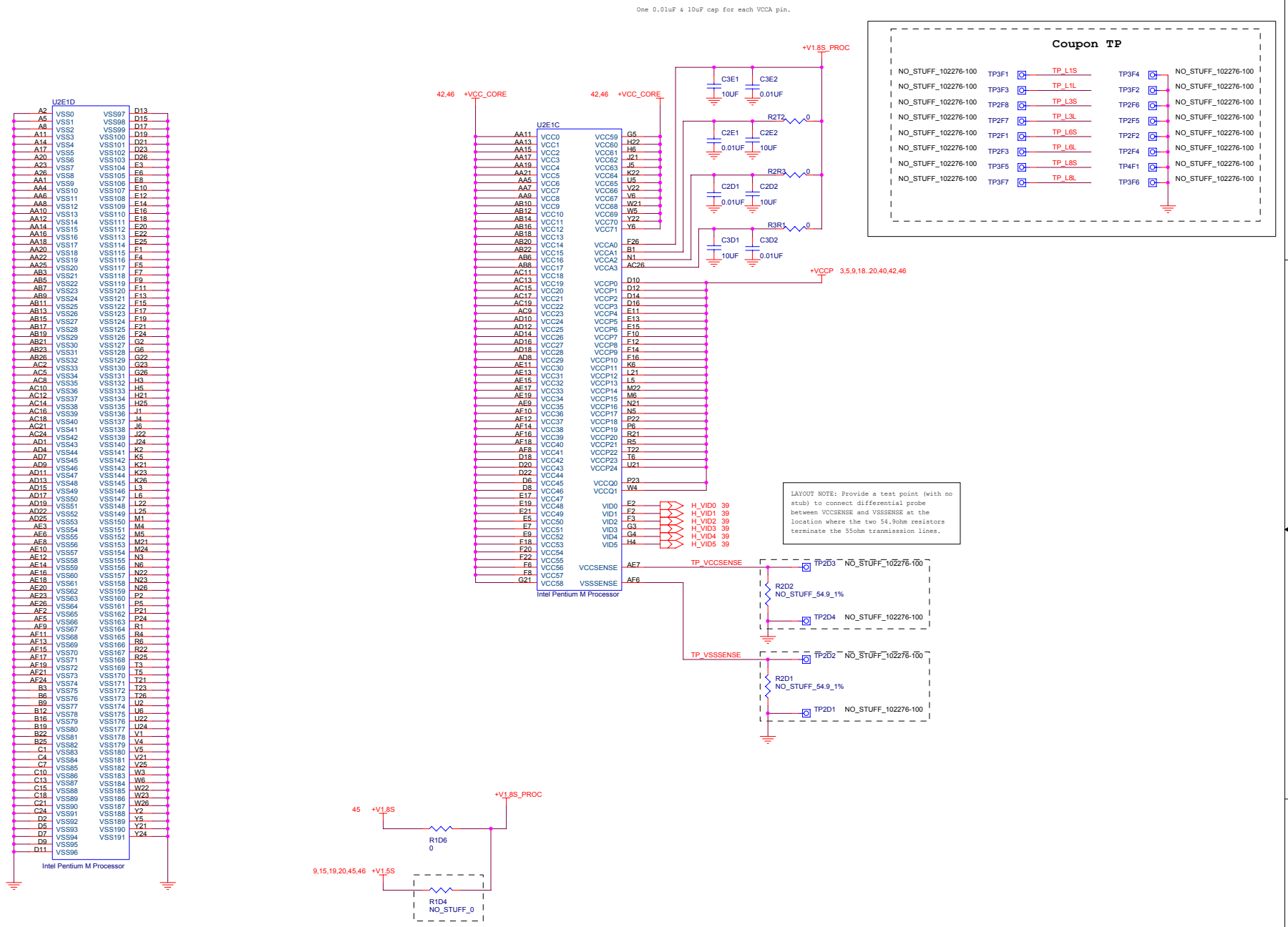

Title	Processor 2 of 2		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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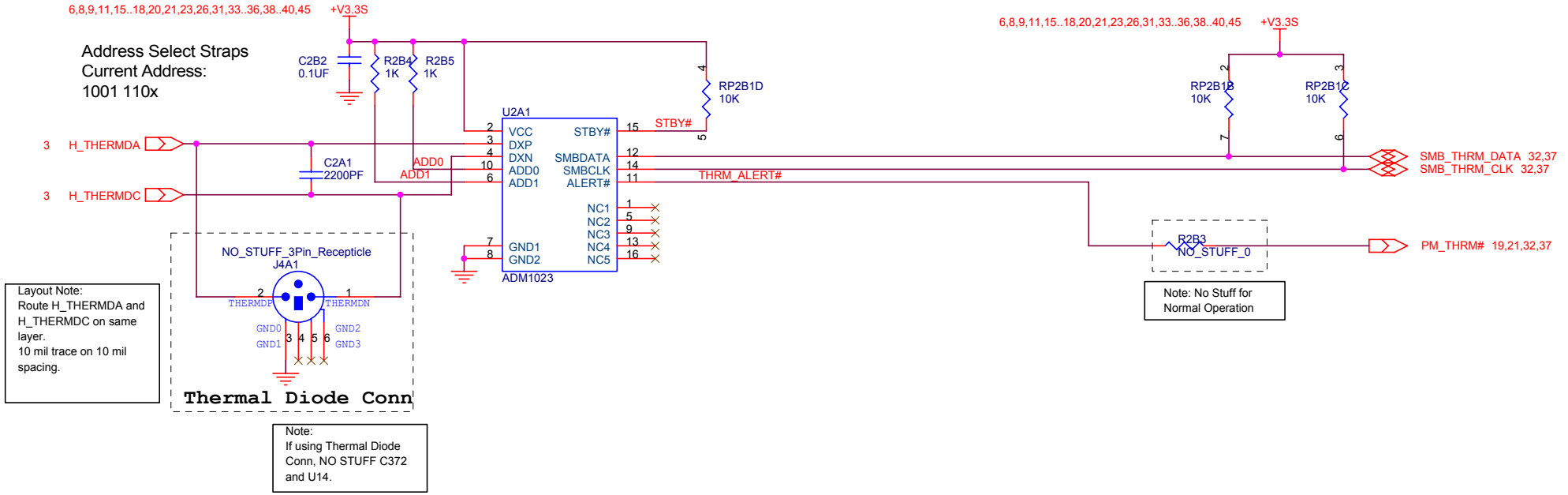
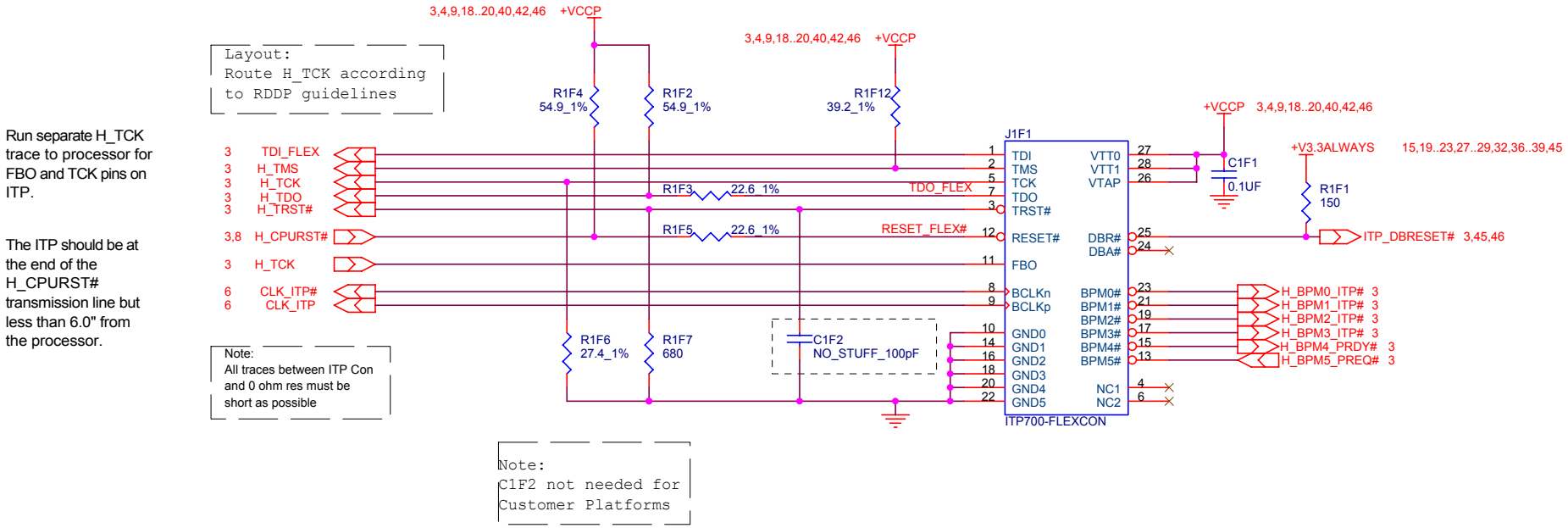
CPU Thermal Sensor





Run separate H_TCK trace to processor for FBO and TCK pins on ITP.

The ITP should be at the end of the H_CPURST# transmission line but less than 6.0" from the processor.

Place TCK pulldown resistor within 1" of ITP.

Title	CPU Thermal Sensor & ITP		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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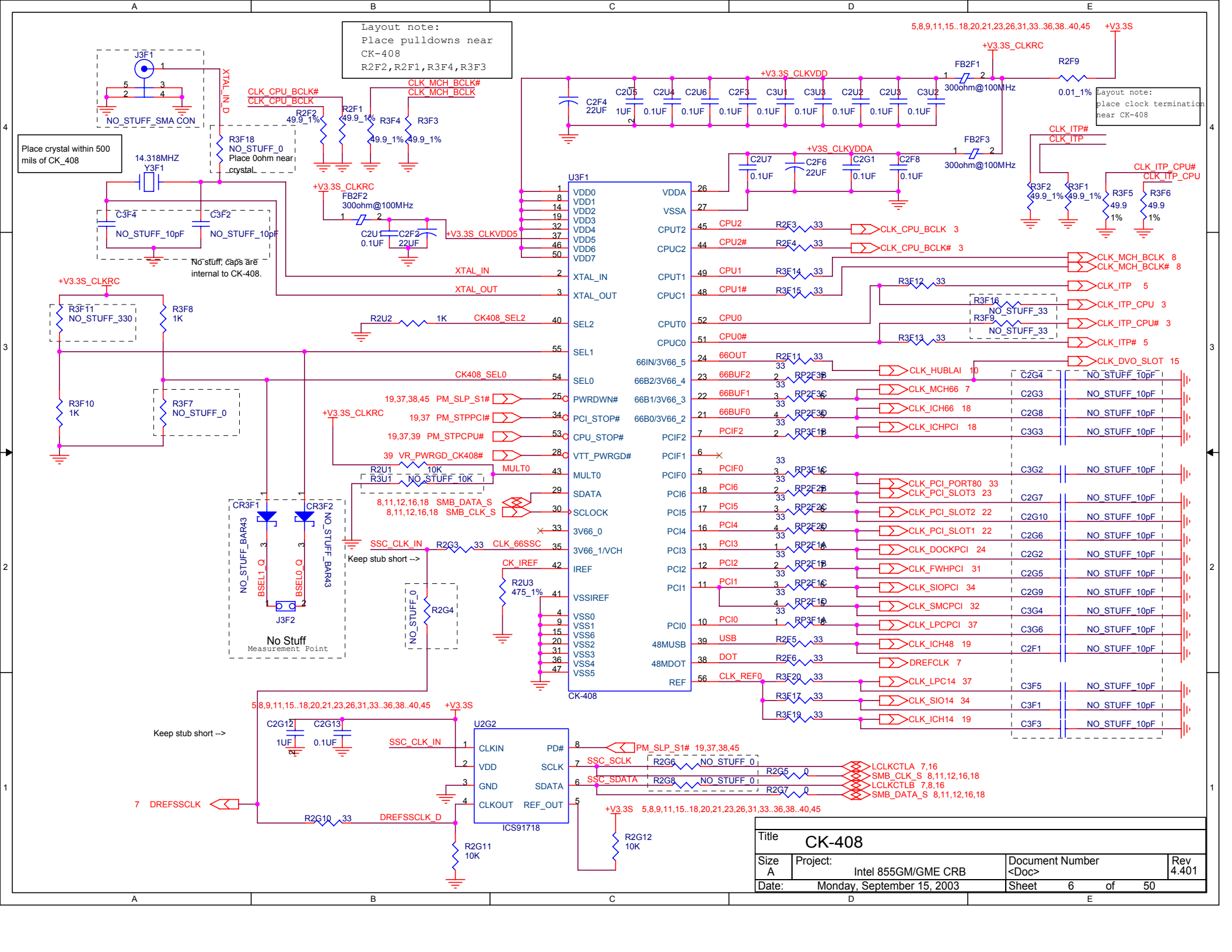
Layout note:
Place pulldowns near
CK-408
R2F2,R2F1,R3F4,R3F3
Place crystal within 500 mils of CK_408
No stuff, caps are internal to CK-408.
Keep stub short -->
Keep stub short -->
Layout note:
place clock termination near CK-408
No Stuff
Measurement Point
CK-408
ICS91718
Title
CK-408
Size A
Project: Intel 855GM/GME CRB
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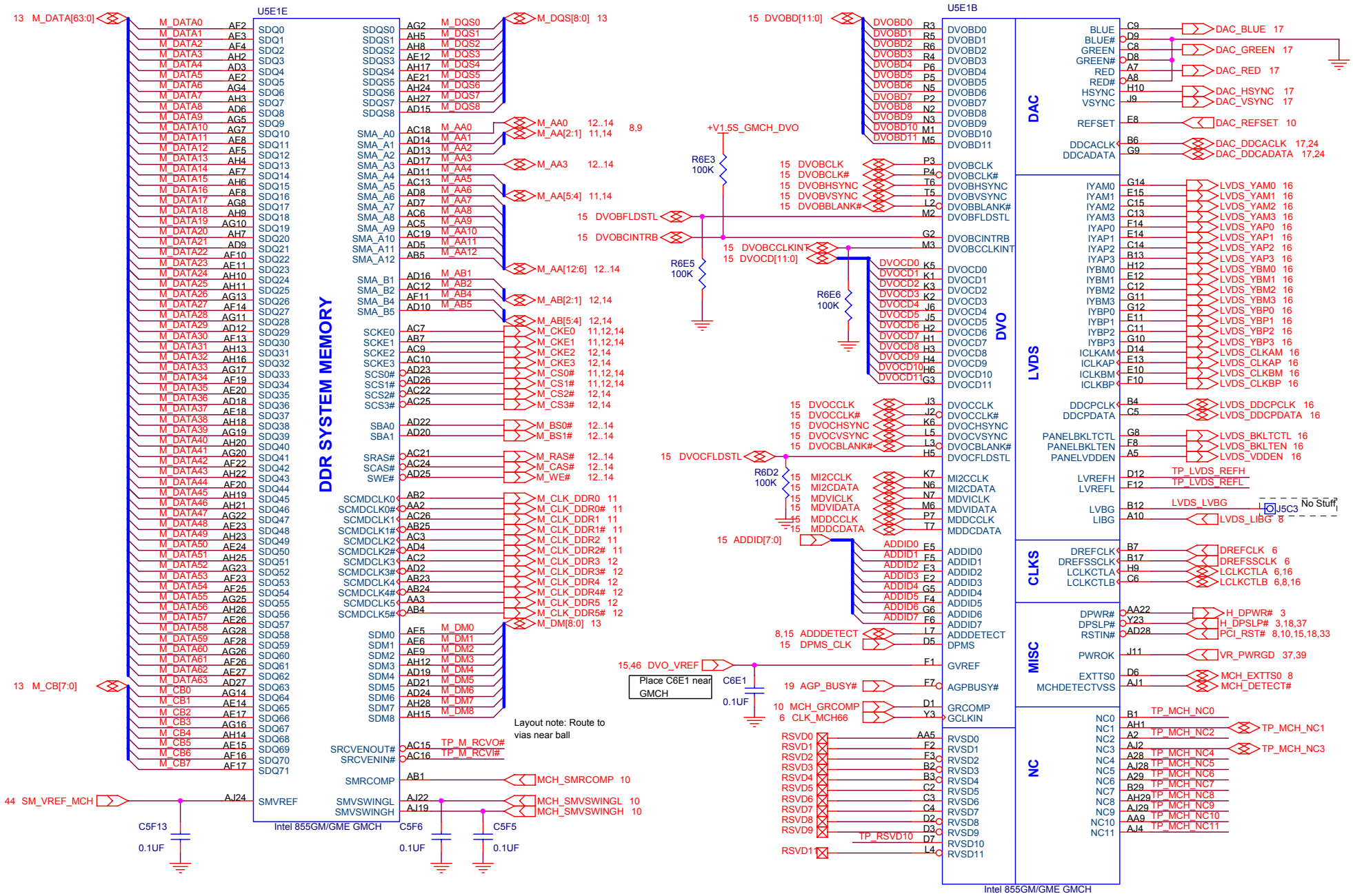
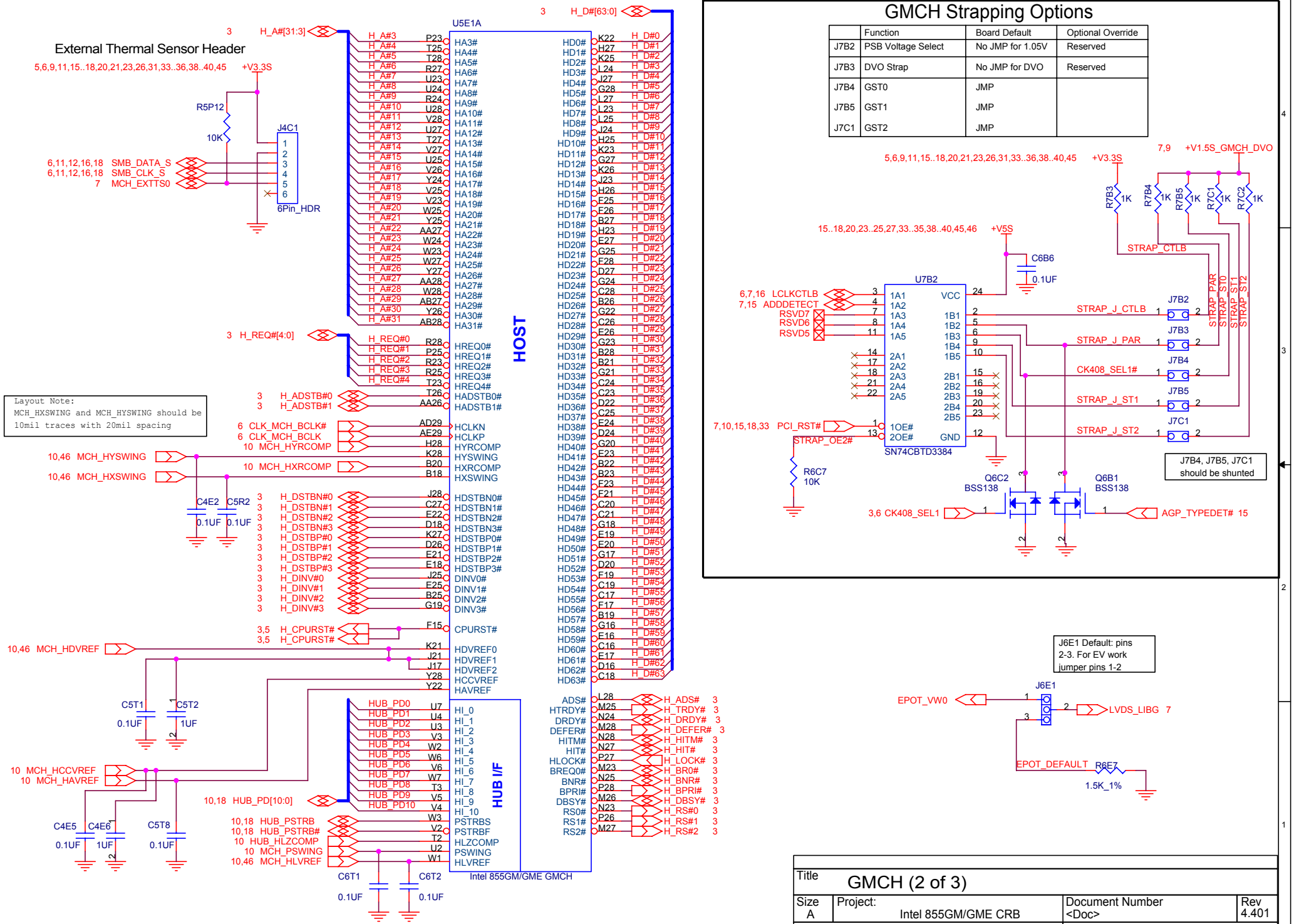
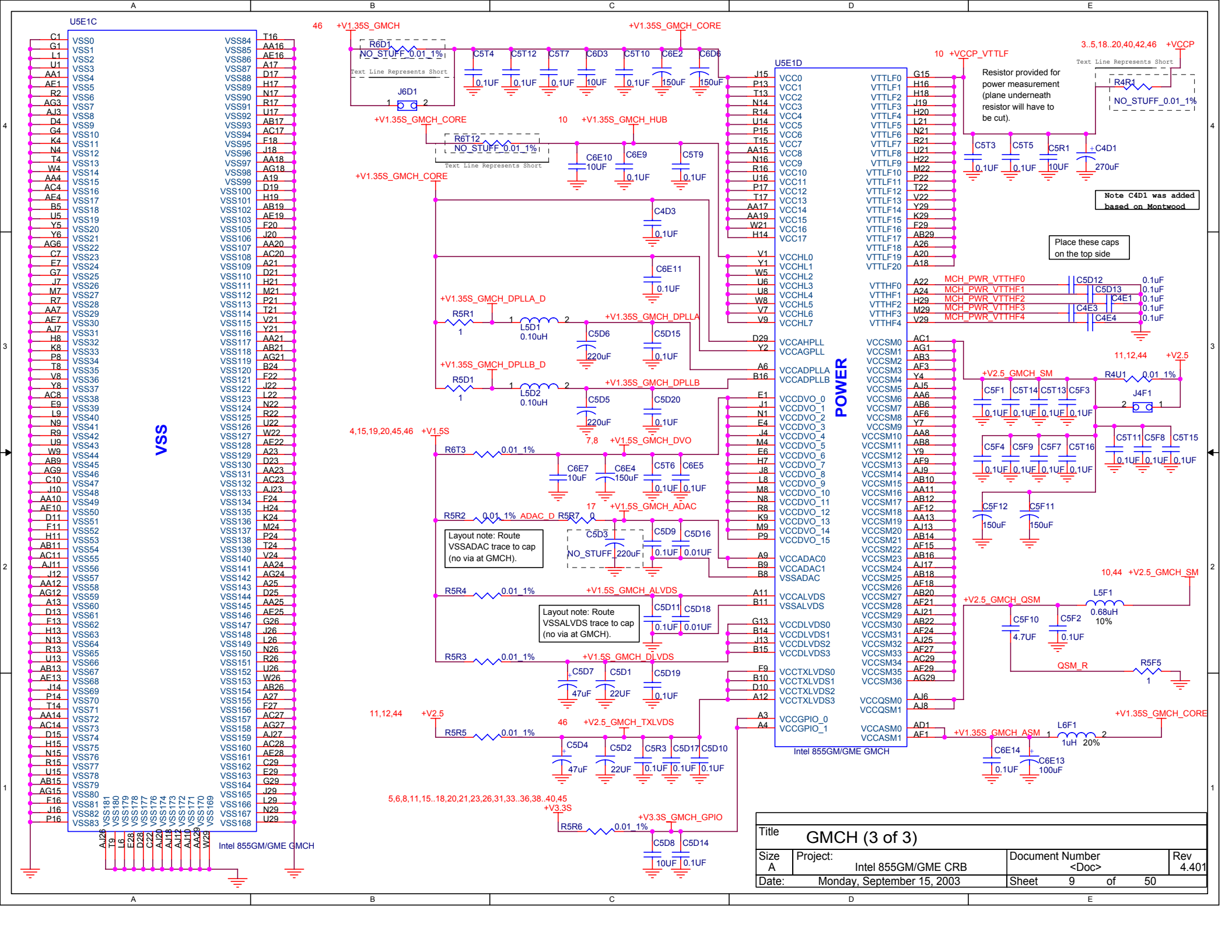
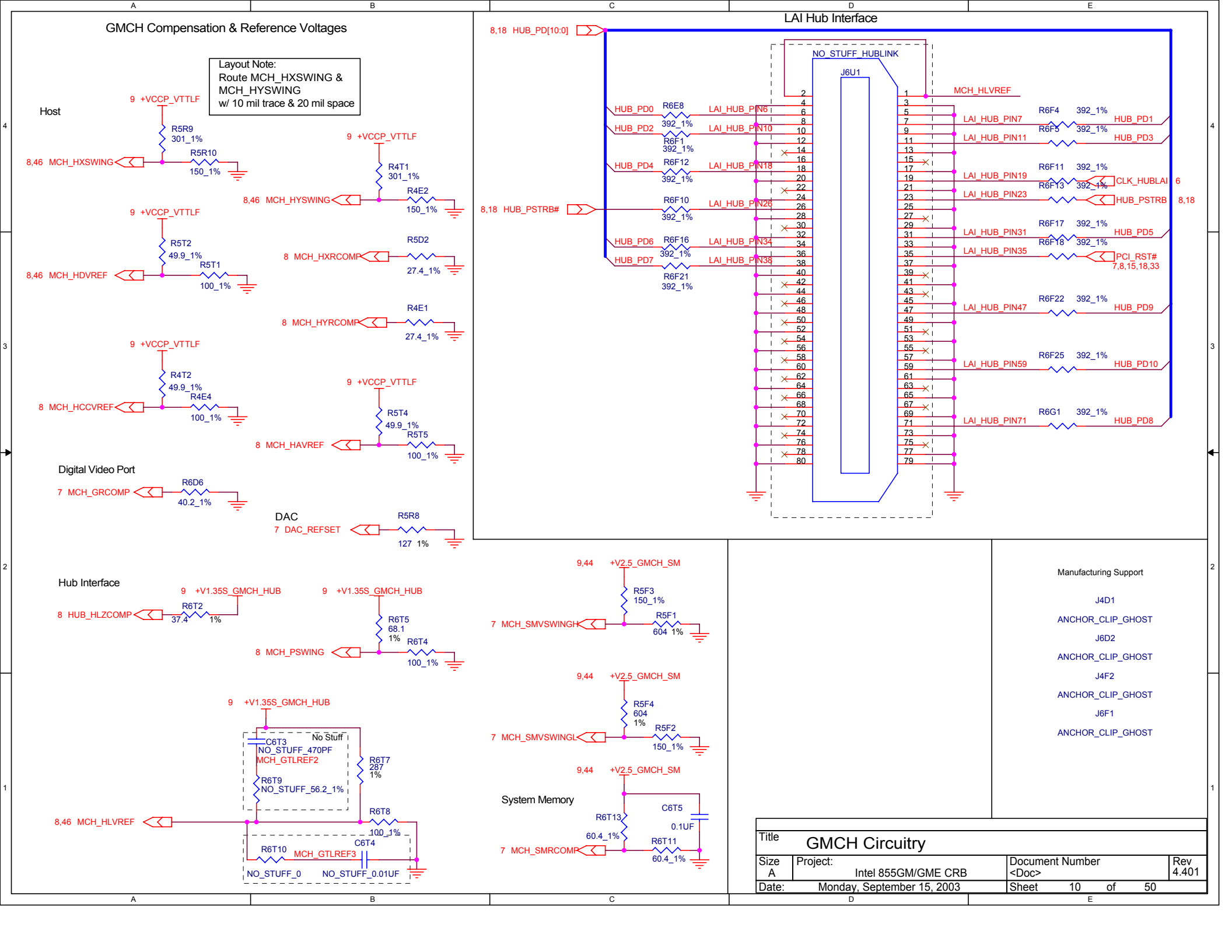


Title	GMCH (1 of 3)		
Size: A	Project: Intel 855GM/GME CRB	Document Number: <Doc>	Rev: 4.401
Date: Monday, September 15, 2003		Sheet 7 of 50	


External Thermal Sensor Header
5,6,9,11,15..18,20,21,23,26,31,33..36,38..40,45
+V3.3S
R5P12
10K
J4C1
6Pin_HDR
6,11,12,16,18 SMB_DATA_S
6,11,12,16,18 SMB_CLK_S
7 MCH_EXTTS0
U5E1A
HOST
3 H_A#[31:3]
3 H_D#[63:0]
3 H_REQ#[4:0]
3 H_ADSTB#0
3 H_ADSTB#1
6 CLK_MCH_BCLK#
6 CLK_MCH_BCLK
10 MCH_HYRCOMP
10,46 MCH_HYSWING
10 MCH_HXRCOMP
10,46 MCH_HXSWING
C4E2 0.1UF
C5R2 0.1UF
3 H_DSTBN#0
3 H_DSTBN#1
3 H_DSTBN#2
3 H_DSTBN#3
3 H_DSTBP#0
3 H_DSTBP#1
3 H_DSTBP#2
3 H_DSTBP#3
3 H_DINV#0
3 H_DINV#1
3 H_DINV#2
3 H_DINV#3
3,5 H_CPURST#
3,5 H_CPURST#
10,46 MCH_HDVREF
C5T1 0.1UF
C5T2 1UF
10 MCH_HCCVREF
10 MCH_HAVREF
C4E5 0.1UF
C4E6 1UF
C5T8 0.1UF
10,18 HUB_PD[10:0]
10,18 HUB_PSTRB
10,18 HUB_PSTRB#
10 HUB_HLZCOMP
10 MCH_PSWING
10,46 MCH_HLVREF
C6T1 0.1UF
C6T2 0.1UF
HUB I/F
Intel 855GM/GME GMCH
Layout Note:
MCH_HXSWING and MCH_HYSWING should be 10mil traces with 20mil spacing
GMCH Strapping Options
Function
Board Default
Optional Override
J7B2 PSB Voltage Select No JMP for 1.05V Reserved
J7B3 DVO Strap No JMP for DVO Reserved
J7B4 GST0 JMP
J7B5 GST1 JMP
J7C1 GST2 JMP
5,6,9,11,15..18,20,21,23,26,31,33..36,38..40,45
+V3.3S
7,9 +V1.5S_GMCH_DVO
R7B3 1K
R7B4 1K
R7B5 1K
R7C1 1K
R7C2 1K
15..18,20,23..25,27,33..35,38..40,45,46
+V5S
C6B6 0.1UF
STRAP_CTLB
U7B2
SN74CBTD3384
6,7,16 LCLKCTLB
7,15 ADDDETECT
RSVD7
RSVD6
RSVD5
7,10,15,18,33 PCI_RST#
STRAP_OE2#
R6C7 10K
STRAP_J_CTLB
STRAP_J_PAR
CK408_SEL1#
STRAP_J_ST1
STRAP_J_ST2
J7B2
J7B3
J7B4
J7B5
J7C1
STRAP_PAR
STRAP_ST0
STRAP_ST1
STRAP_ST2
J7B4, J7B5, J7C1 should be shunted
Q6C2 BSS138
Q6B1 BSS138
3,6 CK408_SEL1
AGP_TYPEDET# 15
J6E1 Default: pins 2-3. For EV work jumper pins 1-2
J6E1
EPOT_VW0
LVDS_LIBG 7
EPOT_DEFAULT R6E7 1.5K_1%
Title GMCH (2 of 3)
Size A
Project: Intel 855GM/GME CRB
Document Number <Doc>
Rev 4.401
Date: Monday, September 15, 2003
Sheet 8 of 50


U5E1C
VSS
Intel 855GM/GME GMCH
U5E1D
POWER
Intel 855GM/GME GMCH
Text Line Represents Short
Resistor provided for power measurement (plane underneath resistor will have to be cut).
Note C4D1 was added based on Montwood
Place these caps on the top side
Layout note: Route VSSADAC trace to cap (no via at GMCH).
Layout note: Route VSSALVDS trace to cap (no via at GMCH).
Title
GMCH (3 of 3)
Size A
Project: Intel 855GM/GME CRB
Document Number <Doc>
Rev 4.401
Date: Monday, September 15, 2003
Sheet 9 of 50


GMCH Compensation & Reference Voltages
Layout Note:
Route MCH_HXSWING & MCH_HYSWING
w/ 10 mil trace & 20 mil space
Host
9 +VCCP_VTTLF
R5R9 301_1%
8,46 MCH_HXSWING
R5R10 150_1%
9 +VCCP_VTTLF
R4T1 301_1%
8,46 MCH_HYSWING
R4E2 150_1%
9 +VCCP_VTTLF
R5T2 49.9_1%
8,46 MCH_HDVREF
R5T1 100_1%
R5D2
8 MCH_HXRCOMP
27.4_1%
R4E1
8 MCH_HYRCOMP
27.4_1%
9 +VCCP_VTTLF
R4T2 49.9_1%
8 MCH_HCCVREF
R4E4 100_1%
9 +VCCP_VTTLF
R5T4 49.9_1%
8 MCH_HAVREF
R5T5 100_1%
Digital Video Port
7 MCH_GRCOMP
R6D6 40.2_1%
DAC
7 DAC_REFSET
R5R8 127 1%
Hub Interface
9 +V1.35S_GMCH_HUB
8 HUB_HLZCOMP
R6T2 37.4 1%
9 +V1.35S_GMCH_HUB
R6T5 68.1 1%
8 MCH_PSWING
R6T4 100_1%
9 +V1.35S_GMCH_HUB
No Stuff
C6T3 NO_STUFF_470PF
MCH_GTLREF2
R6T9 NO_STUFF_56.2_1%
R6T7 287 1%
8,46 MCH_HLVREF
R6T8 100_1%
C6T4
R6T10 MCH_GTLREF3
NO_STUFF_0
NO_STUFF_0.01UF
LAI Hub Interface
8,18 HUB_PD[10:0]
NO_STUFF_HUBLINK
J6U1
MCH_HLVREF
HUB_PD0 R6E8 392_1% LAI_HUB_PIN6
HUB_PD2 R6F1 392_1% LAI_HUB_PIN10
HUB_PD4 R6F12 392_1% LAI_HUB_PIN18
8,18 HUB_PSTRB# R6F10 392_1% LAI_HUB_PIN26
HUB_PD6 R6F16 392_1% LAI_HUB_PIN34
HUB_PD7 R6F21 392_1% LAI_HUB_PIN38
LAI_HUB_PIN7 R6F4 392_1% HUB_PD1
LAI_HUB_PIN11 R6F5 392_1% HUB_PD3
LAI_HUB_PIN19 R6F11 392_1% CLK_HUBLAI 6
LAI_HUB_PIN23 R6F13 392_1% HUB_PSTRB 8,18
LAI_HUB_PIN31 R6F17 392_1% HUB_PD5
LAI_HUB_PIN35 R6F18 392_1% PCI_RST# 7,8,15,18,33
LAI_HUB_PIN47 R6F22 392_1% HUB_PD9
LAI_HUB_PIN59 R6F25 392_1% HUB_PD10
LAI_HUB_PIN71 R6G1 392_1% HUB_PD8
9,44 +V2.5_GMCH_SM
R5F3 150_1%
7 MCH_SMVSWINGH
R5F1 604 1%
9,44 +V2.5_GMCH_SM
R5F4 604 1%
7 MCH_SMVSWINGL
R5F2 150_1%
9,44 +V2.5_GMCH_SM
System Memory
R6T13 60.4_1%
C6T5 0.1UF
7 MCH_SMRCOMP
R6T11 60.4_1%
Manufacturing Support
J4D1
ANCHOR_CLIP_GHOST
J6D2
ANCHOR_CLIP_GHOST
J4F2
ANCHOR_CLIP_GHOST
J6F1
ANCHOR_CLIP_GHOST
Title
GMCH Circuitry
Size A
Project: Intel 855GM/GME CRB
Document Number <Doc>
Rev 4.401
Date: Monday, September 15, 2003
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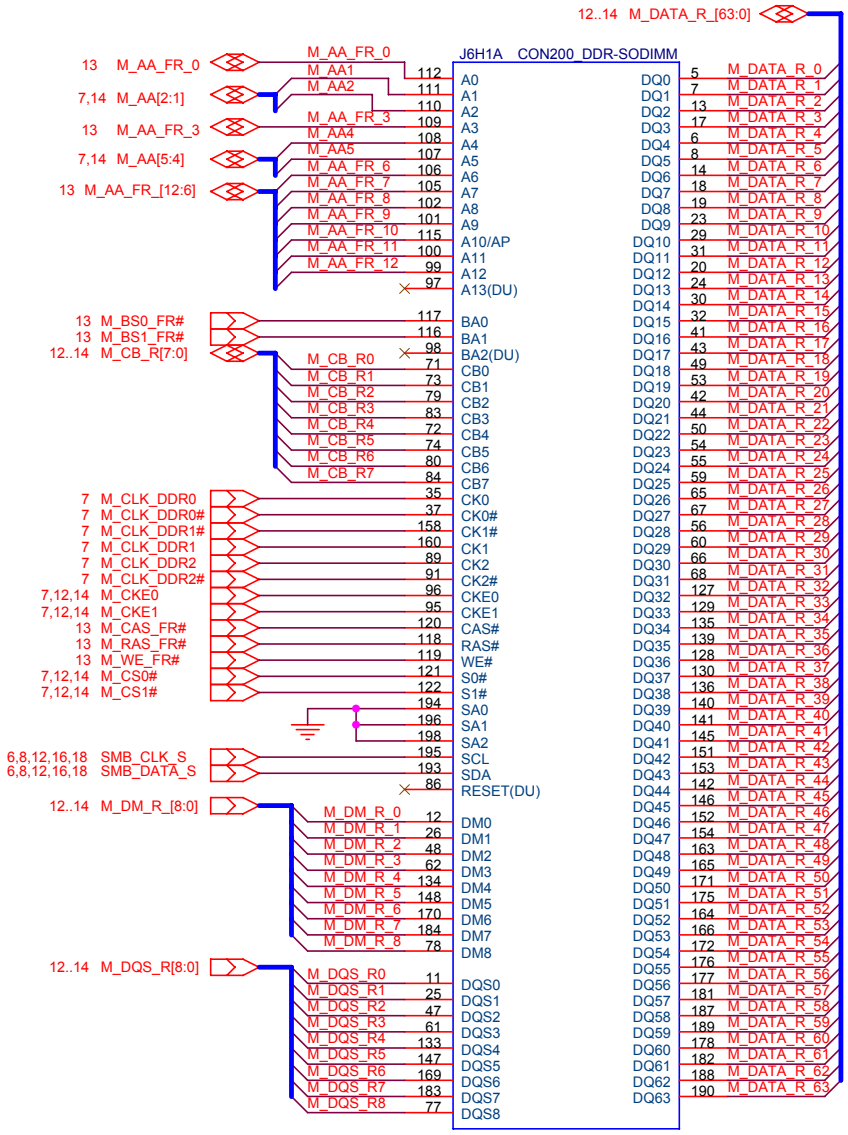
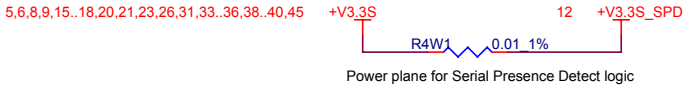
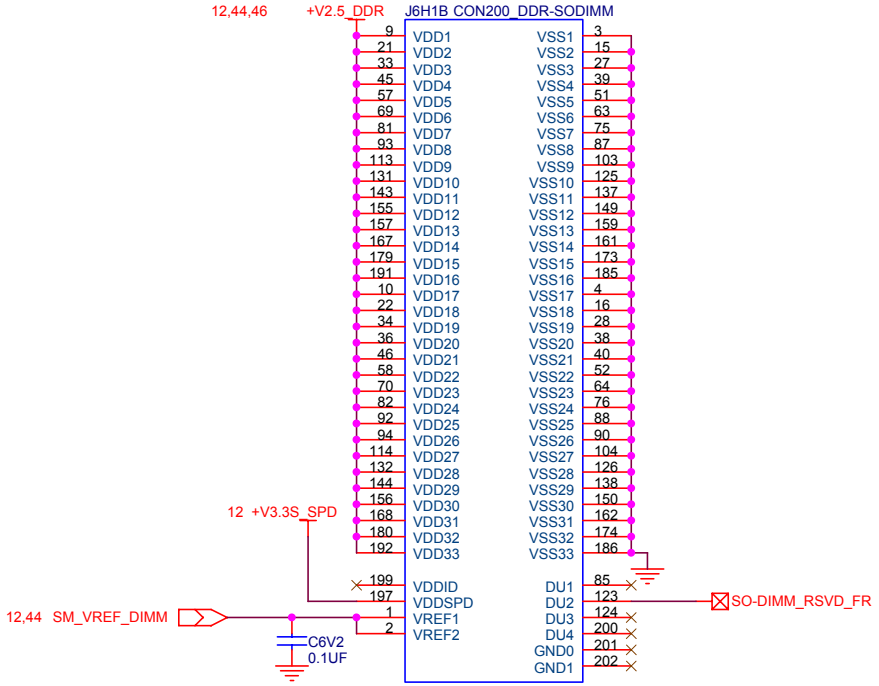
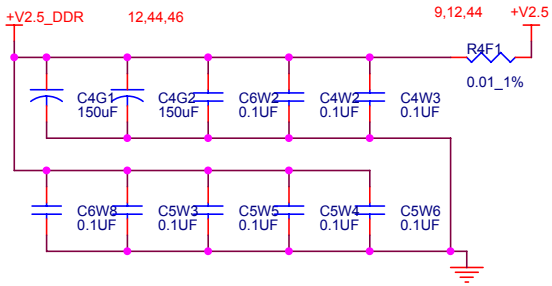


SO-DIMM 0



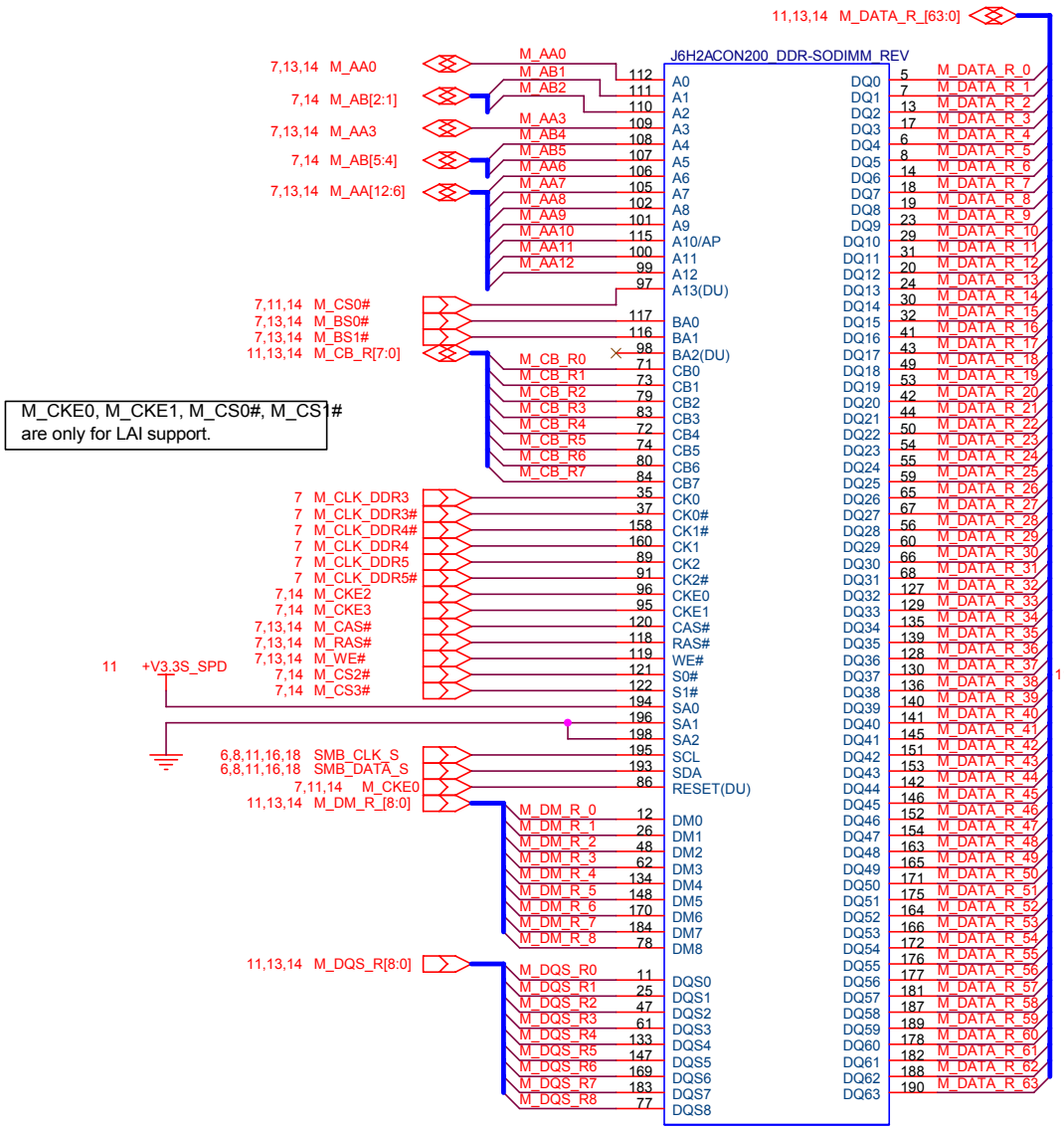
Power plane for Serial Presence Detect logic





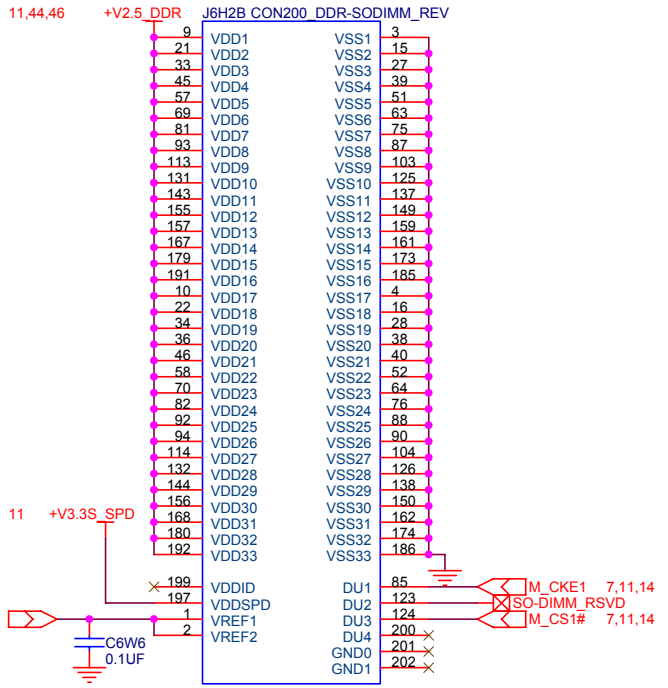
Layout note: Place capacitors between and near DDR connector if possible.

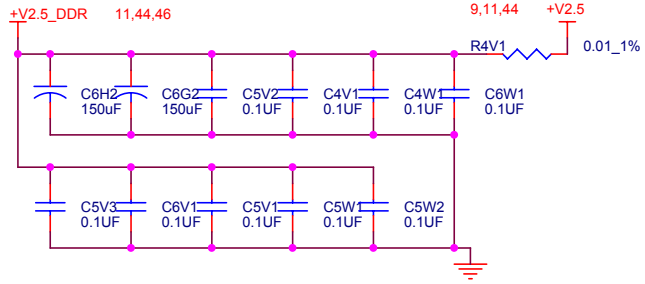
Title: DDR SO-DIMMs (1 of 2)			
Size: A	Project: Intel 855GM/GME CRB	Document Number: <Doc>	Rev: 4.401
Date: Monday, September 15, 2003		Sheet 11 of 50	



SO-DIMM 1

SO-DIMM 1 is placed farther from the GMCH than SO-DIMM 0

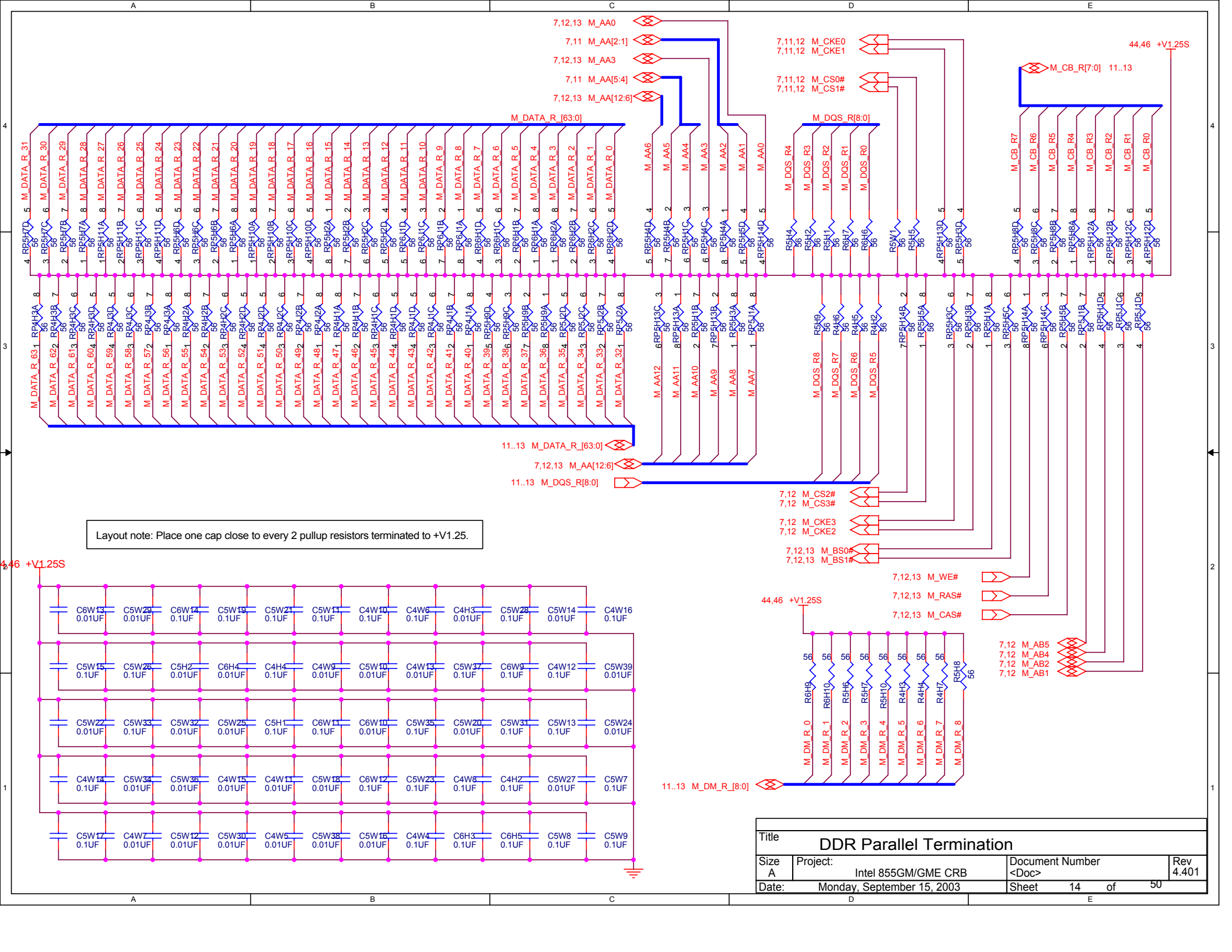




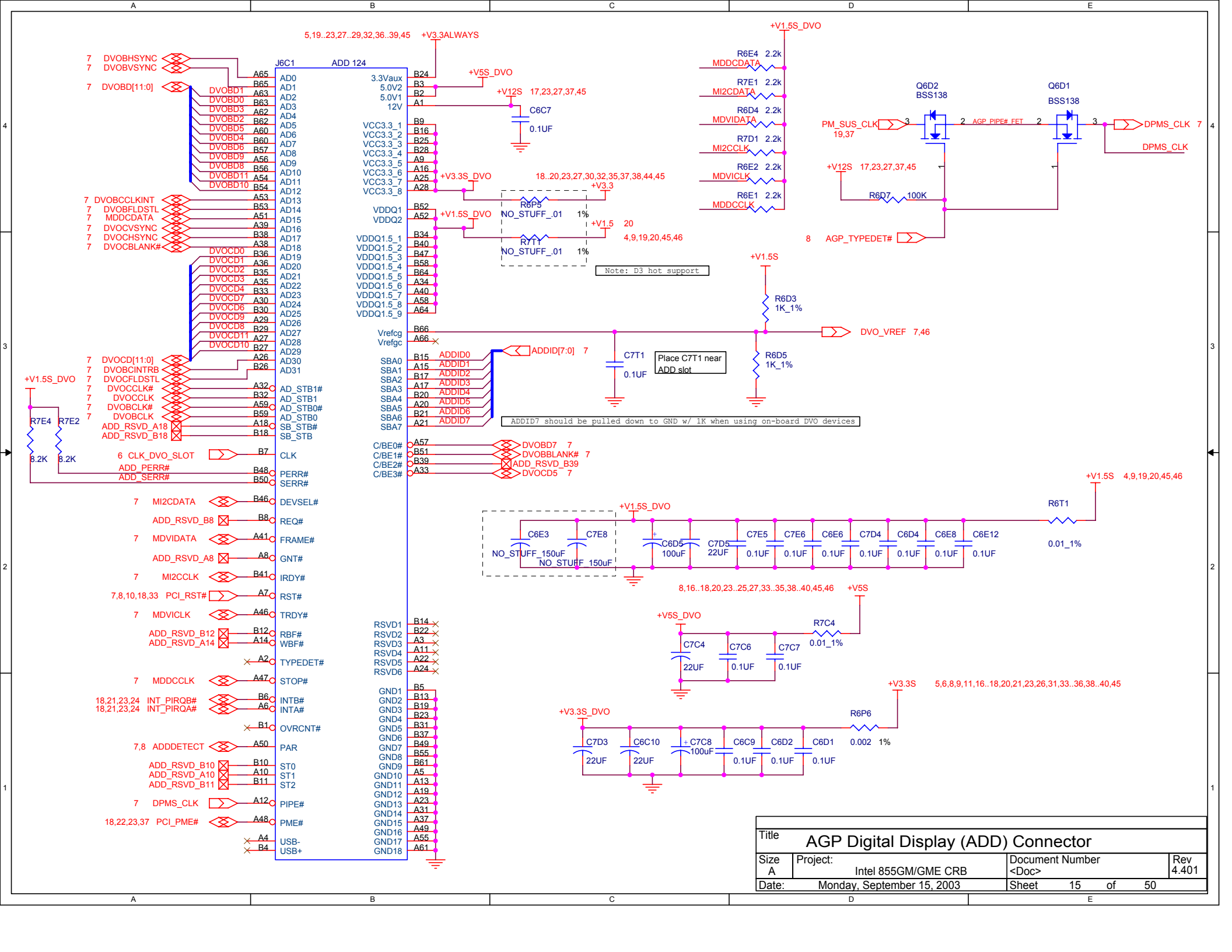
Layout note: Place capacitors between and near DDR connectors if possible.

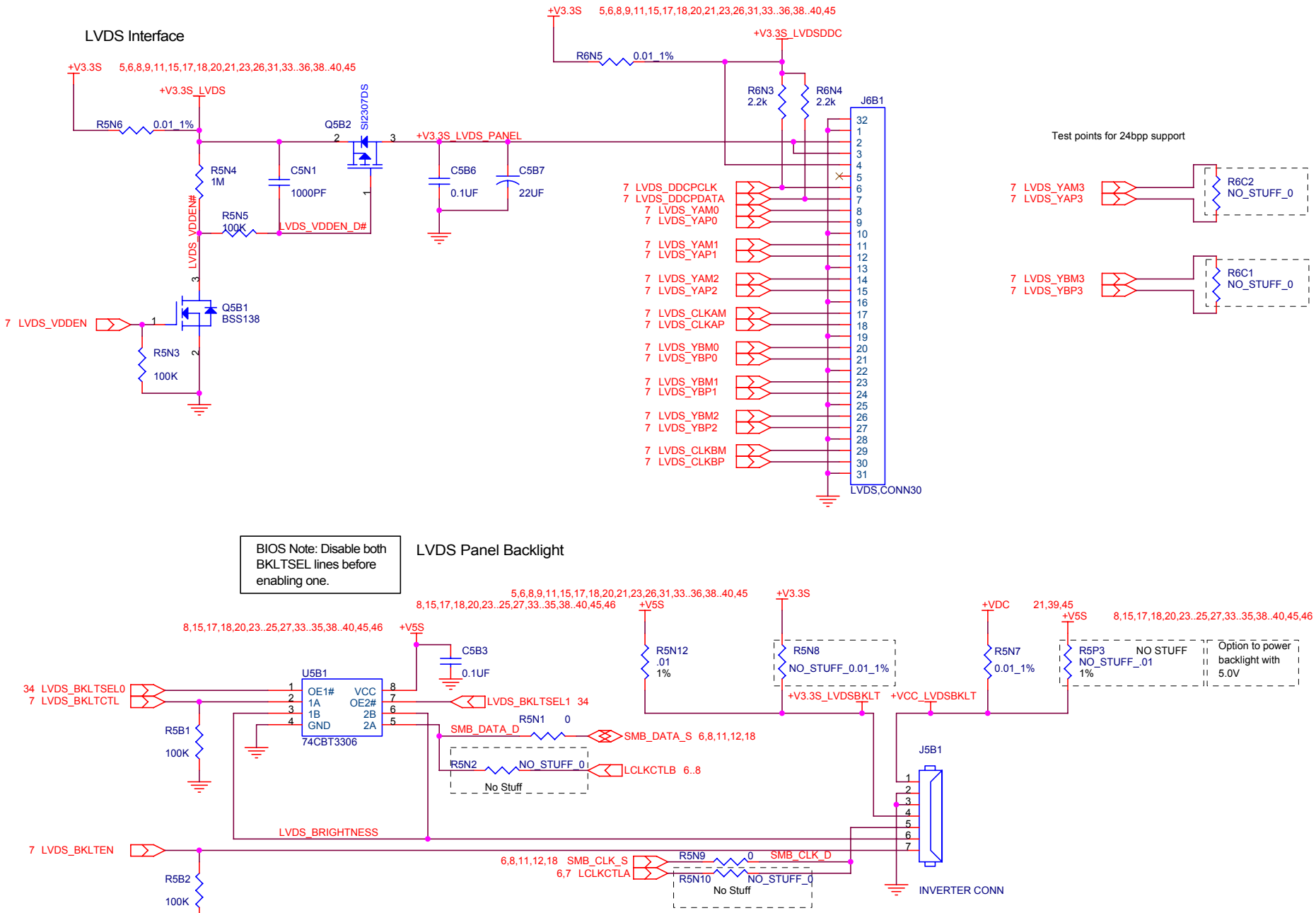
Title	DDR SO-DIMMs (2 of 2)		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
Date: Monday, September 15, 2003		Sheet 12 of 50	

Title: DDR Series Termination			
Size: Custom	Project: Intel 855GM/GME CRB	Document Number: <Doc>	Rev: 4.401
Date: Monday, September 15, 2003		Sheet 13 of 50	

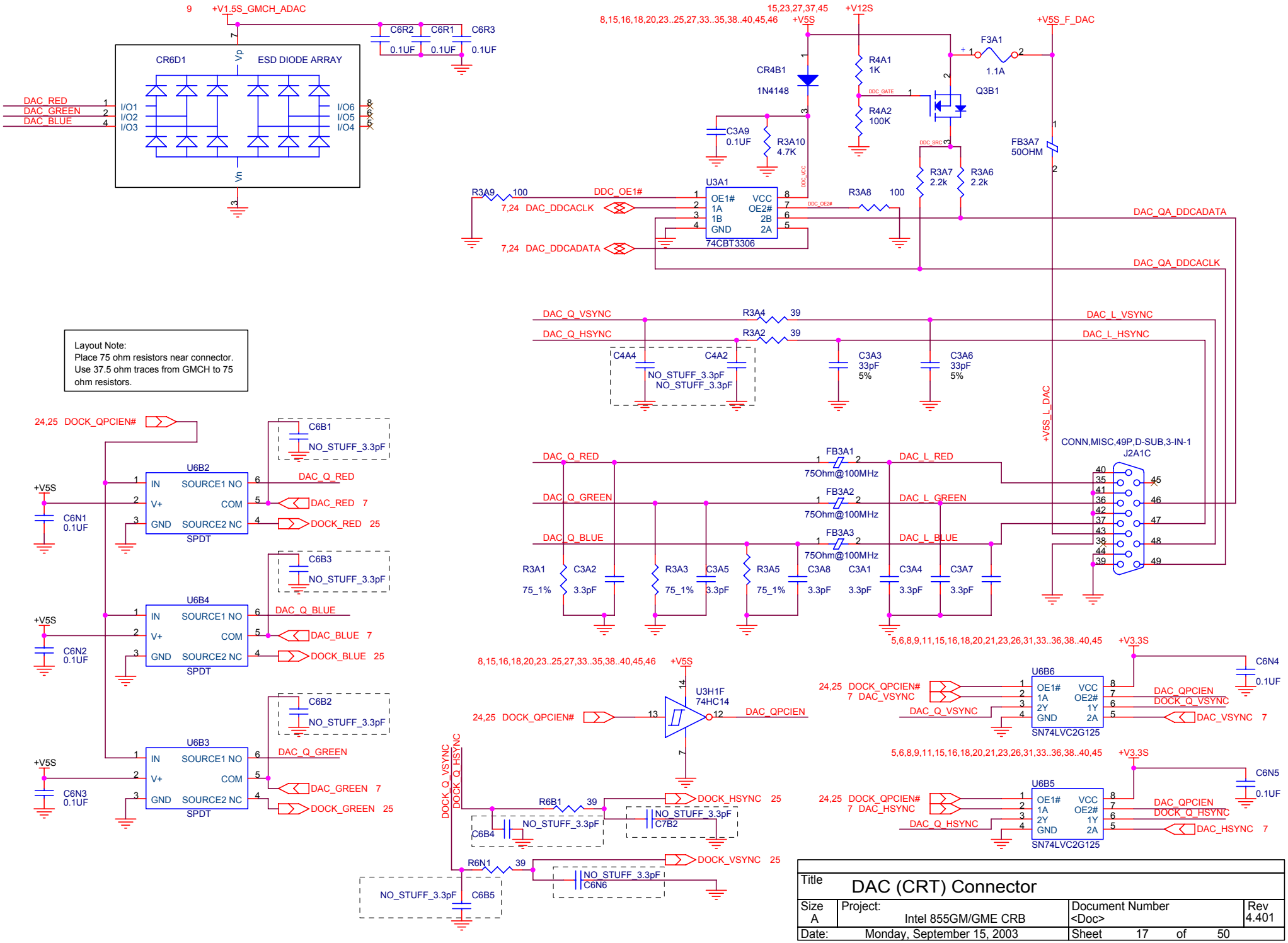


Title	DDR Parallel Termination		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
Date: Monday, September 15, 2003		Sheet 14 of 50	

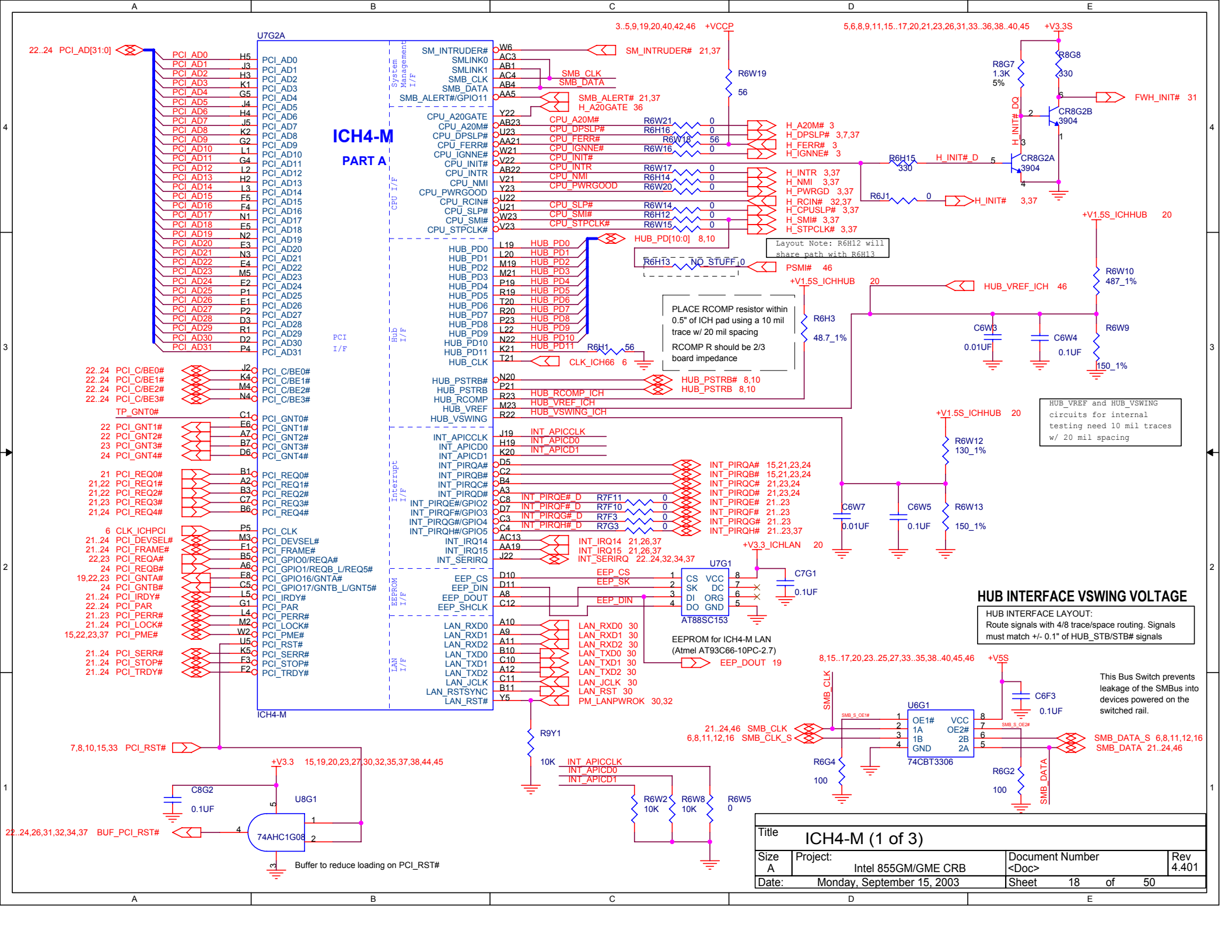

J6C1
ADD 124
7 DVOBHSYNC
7 DVOBVSYNC
7 DVOBD[11:0]
7 DVOBCCLKINT
7 DVOBFLDSTL
7 MDDCDATA
7 DVOCVSYNC
7 DVOCHSYNC
7 DVOCBLANK#
7 DVOCD[11:0]
7 DVOBCINTRB
7 DVOCFLDSTL
7 DVOCCLK#
7 DVOCCLK
7 DVOBCLK#
7 DVOBCLK
ADD_RSVD_A18
ADD_RSVD_B18
6 CLK_DVO_SLOT
ADD_PERR#
ADD_SERR#
7 MI2CDATA
ADD_RSVD_B8
7 MDVIDATA
ADD_RSVD_A8
7 MI2CCLK
7,8,10,18,33 PCI_RST#
7 MDVICLK
ADD_RSVD_B12
ADD_RSVD_A14
7 MDDCCLK
18,21,23,24 INT_PIRQB#
18,21,23,24 INT_PIRQA#
7,8 ADDDETECT
ADD_RSVD_B10
ADD_RSVD_A10
ADD_RSVD_B11
7 DPMS_CLK
18,22,23,37 PCI_PME#
USB-
USB+
AD_STB1#
AD_STB1
AD_STB0#
AD_STB0
SB_STB#
SB_STB
CLK
PERR#
SERR#
DEVSEL#
REQ#
FRAME#
GNT#
IRDY#
RST#
TRDY#
RBF#
WBF#
TYPEDET#
STOP#
INTB#
INTA#
OVRCNT#
PAR
ST0
ST1
ST2
PIPE#
PME#
5,19..23,27..29,32,36..39,45 +V3.3ALWAYS
+V5S_DVO
+V12S 17,23,27,37,45
C6C7
0.1UF
+V3.3S_DVO
18..20,23,27,30,32,35,37,38,44,45 +V3.3
R6P5
NO_STUFF_.01 1%
+V1.5S_DVO
+V1.5 20
4,9,19,20,45,46
R7T1
NO_STUFF_.01 1%
Note: D3 hot support
+V1.5S
R6D3
1K_1%
DVO_VREF 7,46
ADDID[7:0] 7
C7T1
0.1UF
Place C7T1 near ADD slot
R6D5
1K_1%
ADDID7 should be pulled down to GND w/ 1K when using on-board DVO devices
+V1.5S_DVO
R7E4 R7E2
8.2K 8.2K
DVOBD7 7
DVOBBLANK# 7
ADD_RSVD_B39
DVOCD5 7
R6E4 2.2k
MDDCDATA
R7E1 2.2k
MI2CDATA
R6D4 2.2k
MDVIDATA
R7D1 2.2k
MI2CCLK
R6E2 2.2k
MDVICLK
R6E1 2.2k
MDDCCLK
Q6D2
BSS138
Q6D1
BSS138
PM_SUS_CLK
19,37
AGP_PIPE#_FET
DPMS_CLK 7
DPMS_CLK
+V12S 17,23,27,37,45
R6D7 100K
8 AGP_TYPEDET#
+V1.5S_DVO
C6E3 NO_STUFF_150uF
C7E8 NO_STUFF_150uF
C6D5 100uF
C7D5 22UF
C7E5 0.1UF
C7E6 0.1UF
C6E6 0.1UF
C7D4 0.1UF
C6D4 0.1UF
C6E8 0.1UF
C6E12 0.1UF
+V1.5S 4,9,19,20,45,46
R6T1
0.01_1%
8,16..18,20,23..25,27,33..35,38..40,45,46 +V5S
+V5S_DVO
C7C4 22UF
C7C6 0.1UF
C7C7 0.1UF
R7C4
0.01_1%
+V3.3S 5,6,8,9,11,16..18,20,21,23,26,31,33..36,38..40,45
+V3.3S_DVO
C7D3 22UF
C6C10 22UF
C7C8 100uF
C6C9 0.1UF
C6D2 0.1UF
C6D1 0.1UF
R6P6
0.002 1%
Title
AGP Digital Display (ADD) Connector
Size A
Project: Intel 855GM/GME CRB
Document Number <Doc>
Rev 4.401
Date: Monday, September 15, 2003
Sheet 15 of 50



Title: LVDS			
Size: A	Project: Intel 855GM/GME CRB	Document Number: <Doc>	Rev: 4.401
Date: Monday, September 15, 2003		Sheet 16 of 50	



Title	DAC (CRT) Connector		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
Date: Monday, September 15, 2003		Sheet 17 of 50	


U7G2A
ICH4-M
PART A
PCI_AD[31:0]
PCI_C/BE0#
PCI_C/BE1#
PCI_C/BE2#
PCI_C/BE3#
TP_GNT0#
PCI_GNT1#
PCI_GNT2#
PCI_GNT3#
PCI_GNT4#
PCI_REQ0#
PCI_REQ1#
PCI_REQ2#
PCI_REQ3#
PCI_REQ4#
CLK_ICHPCI
PCI_DEVSEL#
PCI_FRAME#
PCI_REQA#
PCI_REQB#
PCI_GNTA#
PCI_GNTB#
PCI_IRDY#
PCI_PAR
PCI_PERR#
PCI_LOCK#
PCI_PME#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
PCI_RST#
PCI_GPIO0/REQA#
PCI_GPIO1/REQB_L/REQ5#
PCI_GPIO16/GNTA#
PCI_GPIO17/GNTB_L/GNT5#
PCI I/F
System Management I/F
SM_INTRUDER#
SMLINK0
SMLINK1
SMB_CLK
SMB_DATA
SMB_ALERT#/GPIO11
CPU I/F
CPU_A20GATE
CPU_A20M#
CPU_DPSLP#
CPU_FERR#
CPU_IGNNE#
CPU_INIT#
CPU_INTR
CPU_NMI
CPU_PWRGOOD
CPU_RCIN#
CPU_SLP#
CPU_SMI#
CPU_STPCLK#
Hub I/F
HUB_PD[10:0]
HUB_PD0
HUB_PD1
HUB_PD2
HUB_PD3
HUB_PD4
HUB_PD5
HUB_PD6
HUB_PD7
HUB_PD8
HUB_PD9
HUB_PD10
HUB_PD11
HUB_CLK
HUB_PSTRB#
HUB_PSTRB
HUB_RCOMP
HUB_VREF
HUB_VSWING
Interrupt I/F
INT_APICCLK
INT_APICD0
INT_APICD1
INT_PIRQA#
INT_PIRQB#
INT_PIRQC#
INT_PIRQD#
INT_PIRQE#/GPIO2
INT_PIRQF#/GPIO3
INT_PIRQG#/GPIO4
INT_PIRQH#/GPIO5
INT_IRQ14
INT_IRQ15
INT_SERIRQ
EEPROM I/F
EEP_CS
EEP_DIN
EEP_DOUT
EEP_SHCLK
LAN I/F
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_JCLK
LAN_RSTSYNC
LAN_RST#
ICH4-M
3..5,9,19,20,40,42,46 +VCCP
R6W19 56
SM_INTRUDER# 21,37
SMB_CLK
SMB_DATA
SMB_ALERT# 21,37
H_A20GATE 36
R6W21 0
R6H16 0
R6W18 56
R6W16 0
R6W17 0
R6H14 0
R6W20 0
R6W14 0
R6H12 0
R6W15 0
H_A20M# 3
H_DPSLP# 3,7,37
H_FERR# 3
H_IGNNE# 3
H_INTR 3,37
H_NMI 3,37
H_PWRGD 3,37
H_RCIN# 32,37
H_CPUSLP# 3,37
H_SMI# 3,37
H_STPCLK# 3,37
HUB_PD[10:0] 8,10
R6H13 NO_STUFF 0
PSMI# 46
Layout Note: R6H12 will share path with R6H13
PLACE RCOMP resistor within 0.5" of ICH pad using a 10 mil trace w/ 20 mil spacing
RCOMP R should be 2/3 board impedance
R6H3 48.7_1%
+V1.5S_ICHHUB 20
HUB_VREF_ICH 46
R6H1 56
CLK_ICH66 6
HUB_PSTRB# 8,10
HUB_PSTRB 8,10
HUB_RCOMP_ICH
HUB_VREF_ICH
HUB_VSWING_ICH
5,6,8,9,11,15..17,20,21,23,26,31,33..36,38..40,45 +V3.3S
R8G7 1.3K 5%
R8G8 330
FWH_INIT# 31
CR8G2B 3904
CR8G2A 3904
H_INIT#_DQ
H_INIT#_D
R6H15 330
R6J1 0
H_INIT# 3,37
+V1.5S_ICHHUB 20
R6W10 487_1%
R6W9 150_1%
C6W3 0.01UF
C6W4 0.1UF
HUB_VREF and HUB_VSWING circuits for internal testing need 10 mil traces w/ 20 mil spacing
+V1.5S_ICHHUB 20
R6W12 130_1%
R6W13 150_1%
C6W7 0.01UF
C6W5 0.1UF
+V3.3_ICHLAN 20
C7G1 0.1UF
U7G1
AT88SC153
INT_PIRQA# 15,21,23,24
INT_PIRQB# 15,21,23,24
INT_PIRQC# 21,23,24
INT_PIRQD# 21,23,24
INT_PIRQE# 21..23
INT_PIRQF# 21..23
INT_PIRQG# 21..23
INT_PIRQH# 21..23,37
INT_IRQ14 21,26,37
INT_IRQ15 21,26,37
INT_SERIRQ 22..24,32,34,37
EEP_CS
EEP_SK
EEP_DIN
EEP_DOUT 19
EEPROM for ICH4-M LAN
(Atmel AT93C66-10PC-2.7)
HUB INTERFACE VSWING VOLTAGE
HUB INTERFACE LAYOUT:
Route signals with 4/8 trace/space routing. Signals must match +/- 0.1" of HUB_STB/STB# signals
8,15..17,20,23..25,27,33..35,38..40,45,46 +V5S
SMB_CLK
21..24,46 SMB_CLK
6,8,11,12,16 SMB_CLK_S
U6G1
74CBT3306
C6F3 0.1UF
R6G4 100
R6G2 100
SMB_DATA_S 6,8,11,12,16
SMB_DATA 21..24,46
This Bus Switch prevents leakage of the SMBus into devices powered on the switched rail.
7,8,10,15,33 PCI_RST#
+V3.3 15,19,20,23,27,30,32,35,37,38,44,45
C8G2 0.1UF
U8G1
74AHC1G08
22..24,26,31,32,34,37 BUF_PCI_RST#
Buffer to reduce loading on PCI_RST#
R9Y1 10K
INT_APICCLK
INT_APICD0
INT_APICD1
R6W2 10K
R6W8 10K
R6W5 0
Title ICH4-M (1 of 3)
Size A
Project: Intel 855GM/GME CRB
Document Number <Doc>
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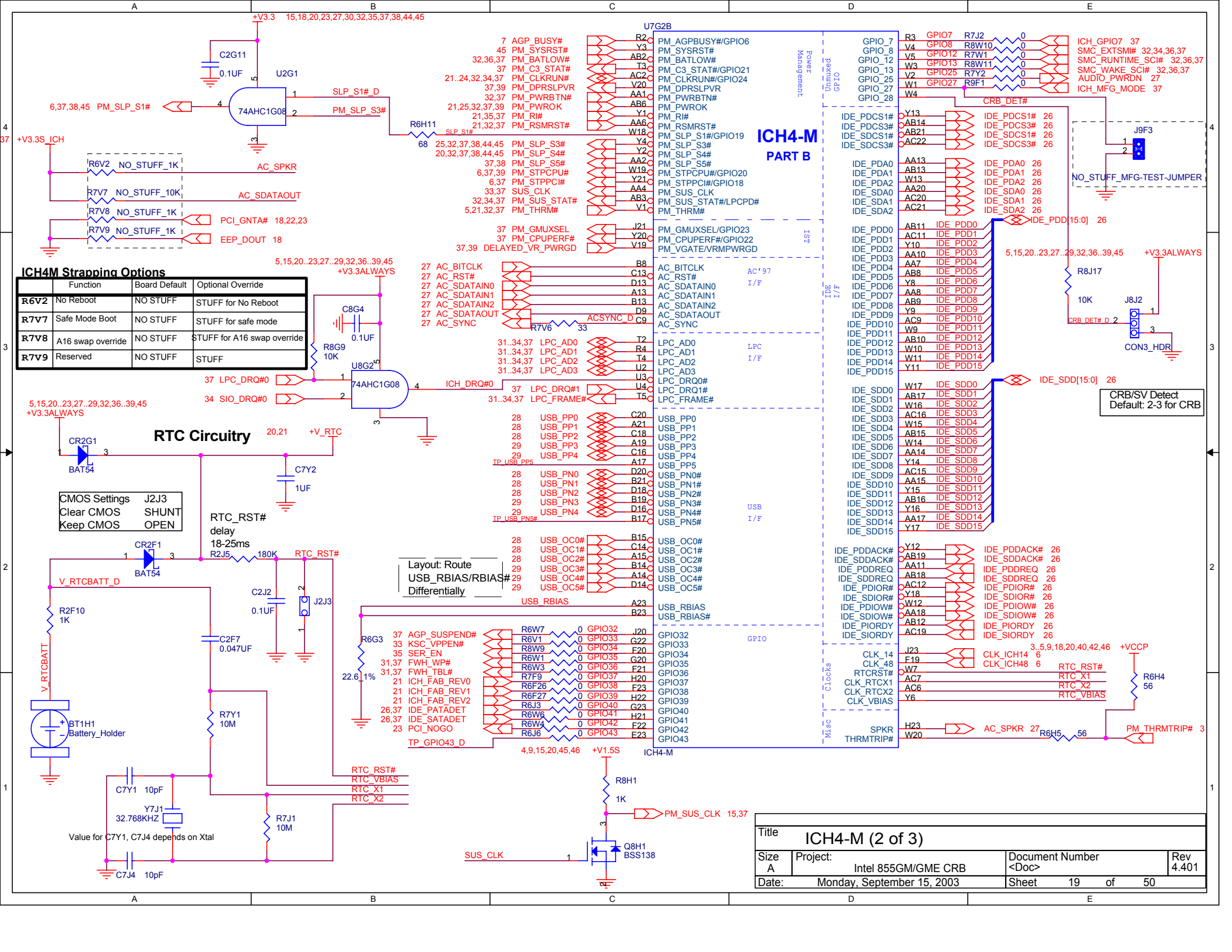
ICH4M Strapping Options
R6V2 No Reboot NO STUFF STUFF for No Reboot
R7V7 Safe Mode Boot NO STUFF STUFF for safe mode
R7V8 A16 swap override NO STUFF STUFF for A16 swap override
R7V9 Reserved NO STUFF STUFF
RTC Circuitry
CMOS Settings J2J3
Clear CMOS SHUNT
Keep CMOS OPEN
RTC_RST# delay 18-25ms
Layout: Route USB_RBIAS/RBIAS# Differentially
ICH4-M PART B
Value for C7Y1, C7J4 depends on Xtal
CRB/SV Detect Default: 2-3 for CRB
Title ICH4-M (2 of 3)
Size A
Project: Intel 855GM/GME CRB
Document Number <Doc>
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Date: Monday, September 15, 2003
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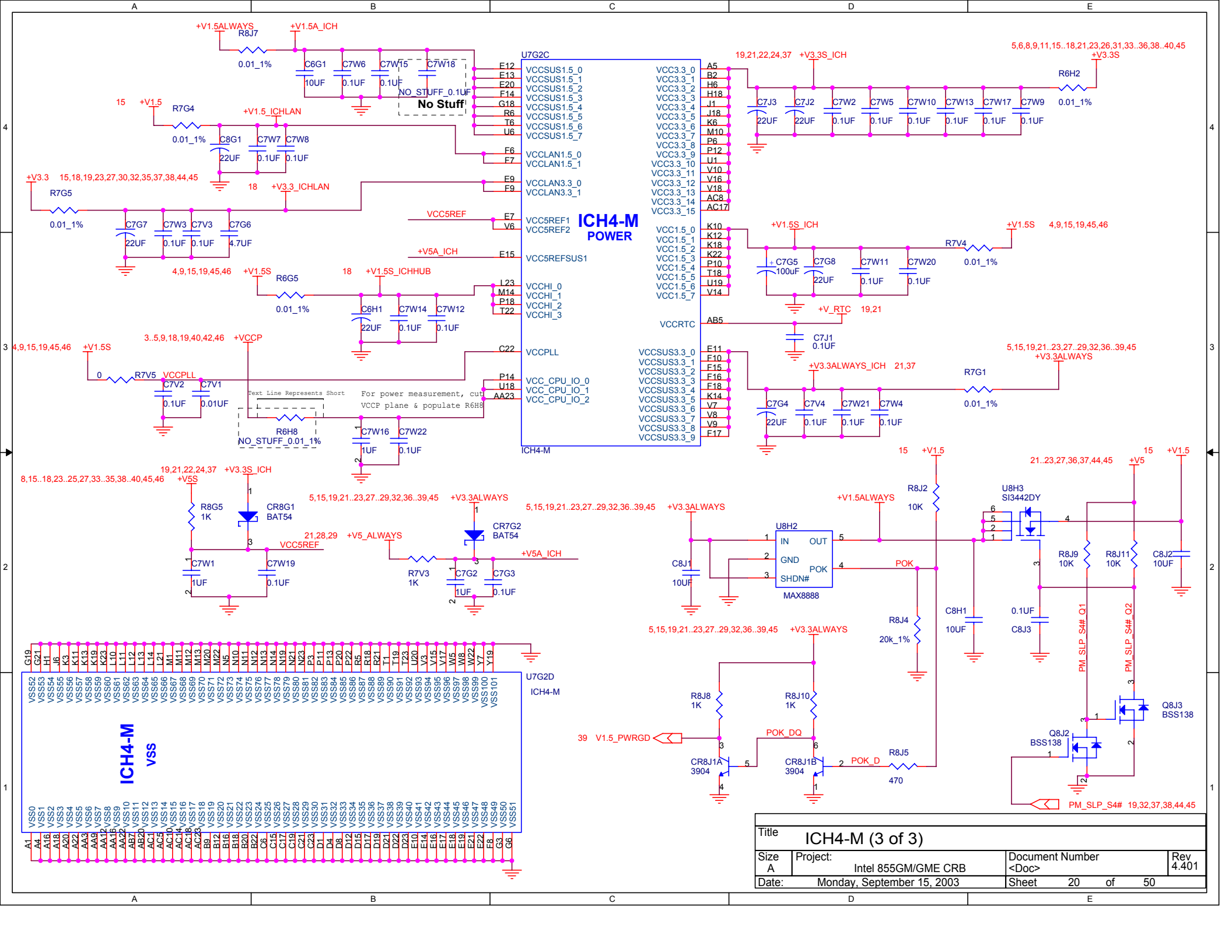
U7G2C
ICH4-M
POWER
ICH4-M
U7G2D
ICH4-M
VSS
No Stuff
Text Line Represents Short
For power measurement, cut
VCCP plane & populate R6H8
NO_STUFF_0.01_1%
NO_STUFF_0.1UF
MAX8888
U8H2
U8H3
SI3442DY
Q8J3
BSS138
Q8J2
BSS138
CR8J1A
3904
CR8J1B
3904
CR8G1
BAT54
CR7G2
BAT54
Title
ICH4-M (3 of 3)
Size
A
Project:
Intel 855GM/GME CRB
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ICH4 Pullups

20,37 +V3.3ALWAYS_ICH

19,35,37 PM_RI# — RP8H6C 3 — 6 10K
18,37 SMB_ALERT# — RP8H7B 2 — 7 10K

19,20,22,24,37 +V3.3S_ICH

18,22..24 PCI_FRAME#	RP8H2D 4	5	8.2K
18,22..24 PCI_IRDY#	RP8H3C 3	6	8.2K
18,22..24 PCI_TRDY#	RP8H2C 3	6	8.2K
18,22..24 PCI_STOP#	RP8H2B 2	7	8.2K
18,22..24 PCI_SERR#	RP8H2A 1	8	8.2K
18,22..24 PCI_DEVSEL#	RP8H3A 1	8	8.2K
18,22,23 PCI_PERR#	RP8H3D 4	5	8.2K
18,22..24 PCI_LOCK#	RP8H3B 2	7	8.2K
18 PCI_REQ0#	RP8H1C 3	6	8.2K
18,22 PCI_REQ1#	RP8G3C 3	6	8.2K
18,22 PCI_REQ2#	RP8G2A 1	8	8.2K
18,23 PCI_REQ3#	RP8H1B 2	7	8.2K
18,24 PCI_REQ4#	RP8H1D 4	5	8.2K
18,26,37 INT_IRQ14	RP7J1D 4	5	8.2K
18,26,37 INT_IRQ15	RP7J1A 1	8	8.2K
15,18,23,24 INT_PIRQA#	RP8H1A 1	8	8.2K
15,18,23,24 INT_PIRQB#	RP8G3A 1	8	8.2K
18,23,24 INT_PIRQC#	RP8G3B 2	7	8.2K
18,23,24 INT_PIRQD#	RP8G3D 4	5	8.2K
18,22,23 INT_PIRQE#	RP7F2A 1	8	8.2K
18,22,23 INT_PIRQF#	RP7F2C 3	6	8.2K
18,22,23 INT_PIRQG#	RP7F2B 2	7	8.2K
18,22,23,37 INT_PIRQH#	RP7F2D 4	5	8.2K
22,23 PCI_REQ64#	RP7E1A 1	8	10K
22,23 PCI_ACK64#	RP7E1B 2	7	10K
19,22..24,32,34,37 PM_CLKRUN#	RP8H7D 4	5	10K

19,20 +V_RTC

18,37 SM_INTRUDER# — R2J4 — 100K

5,6,8,9,11,15..18,20,23,26,31,33..36,38..40,45 +V3.3S

5,19,32,37 PM_THRM# — R8H2 — 8.2K

19,25,32,37,39 PM_PWROK — R8H4 100K
19,32,37 PM_RSMRST# — R8J6 100K

20,37 +V3.3ALWAYS_ICH

18,22..24,46 SMB_CLK — R8J1 — 2.2k
18,22..24,46 SMB_DATA — R8J3 — 2.2k

+V5_ALWAYS Generation

Vout=0.8(1+Rtop/Rbot)
Vout=0.8(1+(3.92k/750))= 4.98V
IMAX OUT = 50mV / 10mohms = 5A

+V5 20,22,23,27,36,37,44,45
+V3.3ALWAYS 5,15,19,20,22,23,27..29,32,36..39,45
R4N1 100K_1% +VDC 16,39,45

39 V5A_PWRGD

Place these caps near U4C1

R4P1 NO_STUFF_680K

U4C1 LTC1735-1

1	COSC	TG	16
2	RUN/SS	BOOST	15
3	ITH	SW	14
8	SGND	VIN	13
7	VOSENSE	INTVCC	12
5	SENSE-	BG	11
6	SENSE+	PGND	10
9	EXTVCC		
4	PGOOD		

V5A_COSC — C4C10 47pF — C4C11 3300pF
RUN_SS
V5A_ITH — R4C6 37.4k_1% — C4C12 47pF — C4C7 47pF — C4C13 330pF
V5A_ITH_D
C4C9 1000PF

Q4C1A SI4966DY
V5A_TG
C4C5 0.47uF
V5A_BOOST
V5A_SW
CR4C1 MBR0520LT1
V5A_INTVCC
Q4C1B SI4966DY
V5A_BG
C4P3 1UF — C4C8 10UF — C4P1 0.1UF

Layout:
CR4B2 needs to be placed close to U4C1 & Q4C1

L4B1 4.7uH — R4C1 0.01_1%
+V5_ALWAYS 20,28,29
CR4B2 B320A
V5A_BG_D
R4C4 10_1% — R4C5 10_1%
R4C3 3.92k_1% TOP
R4C2 750_1% BOTTOM
V5A_SENSE+
V5A_SENSE-
V5A_VOSENSE

FAB REVISION

19,20,22,24,37 +V3.3S_ICH

R6F20 NO_STUFF_10K — R6F19 10K — R7F8 10K
19 ICH_FAB_REV0
19 ICH_FAB_REV1
19 ICH_FAB_REV2
R6F24 10K — R6F23 NO_STUFF_10K — R7F5 NO_STUFF_10K

FAB ID Strapping Table

ICH_FAB_REV 2	1	0	BOARD FAB
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

+V5 20,22,23,27,36,37,44,45 — C4C4 0.1UF
Please place C4C4 near U4C1 Pin 9

+VDC 16,39,45 — C4P2 100pF 10% — C4B8 22UF
Please place C4P2 and C4B8 near Q4C1A.

+V5_ALWAYS 20,28,29 — C4C3 150UF — C4C6 0.1UF
Please place C4C3 and C4C6 near R4C1

GND_V5A — R4C7 0

Title	ICH4-M Pullups and Testpoints		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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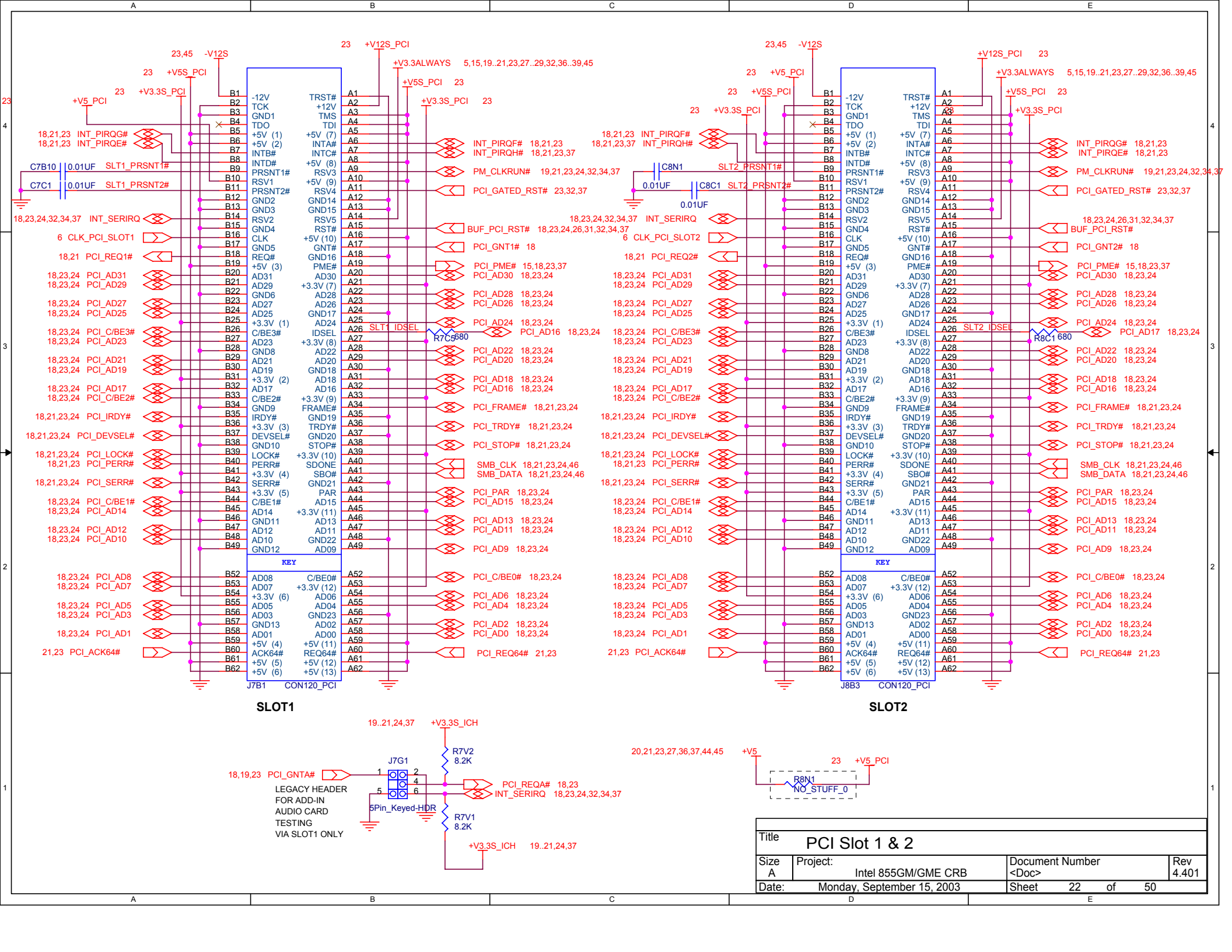
SLOT1
SLOT2
LEGACY HEADER
FOR ADD-IN
AUDIO CARD
TESTING
VIA SLOT1 ONLY
NO_STUFF_0
Title
PCI Slot 1 & 2
Size
A
Project:
Intel 855GM/GME CRB
Document Number
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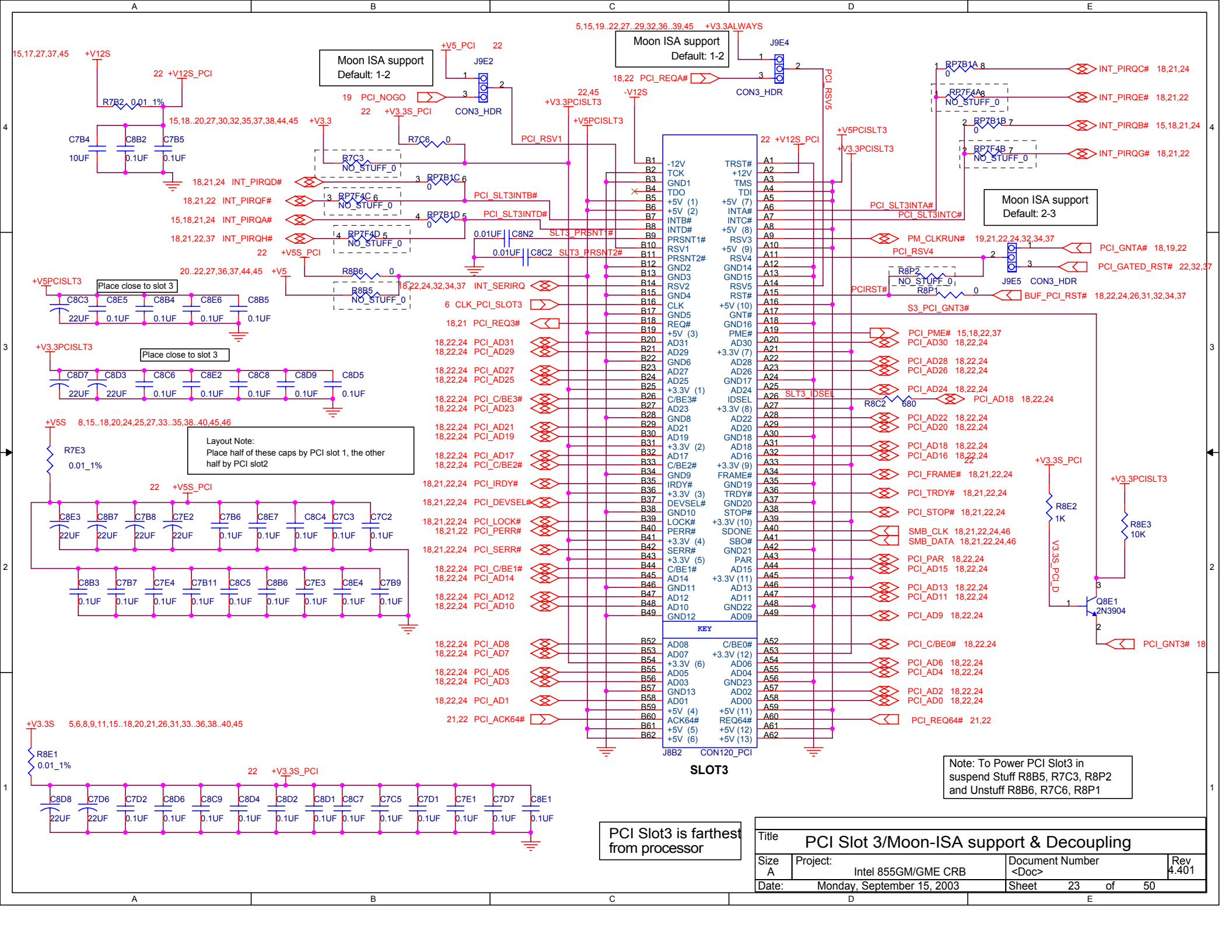
Moon ISA support
Default: 1-2
Moon ISA support
Default: 1-2
Moon ISA support
Default: 2-3
SLOT3
KEY
Place close to slot 3
Place close to slot 3
Layout Note:
Place half of these caps by PCI slot 1, the other half by PCI slot2
Note: To Power PCI Slot3 in suspend Stuff R8B5, R7C3, R8P2 and Unstuff R8B6, R7C6, R8P1
PCI Slot3 is farthest from processor
Title
PCI Slot 3/Moon-ISA support & Decoupling
Size A
Project: Intel 855GM/GME CRB
Document Number <Doc>
Rev 4.401
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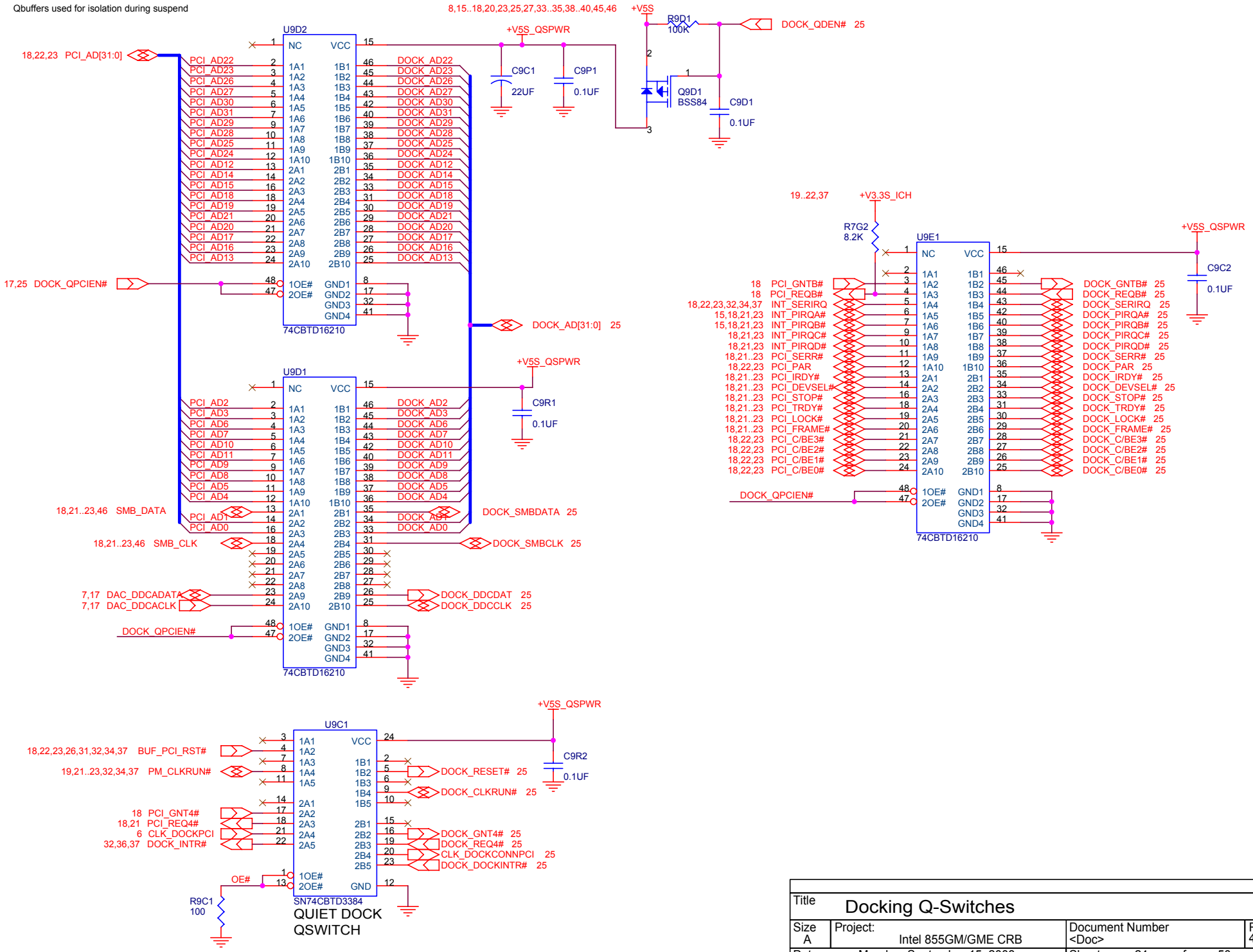
Sheet 23 of 50

Qbuffers used for isolation during suspend



Title	Docking Q-Switches		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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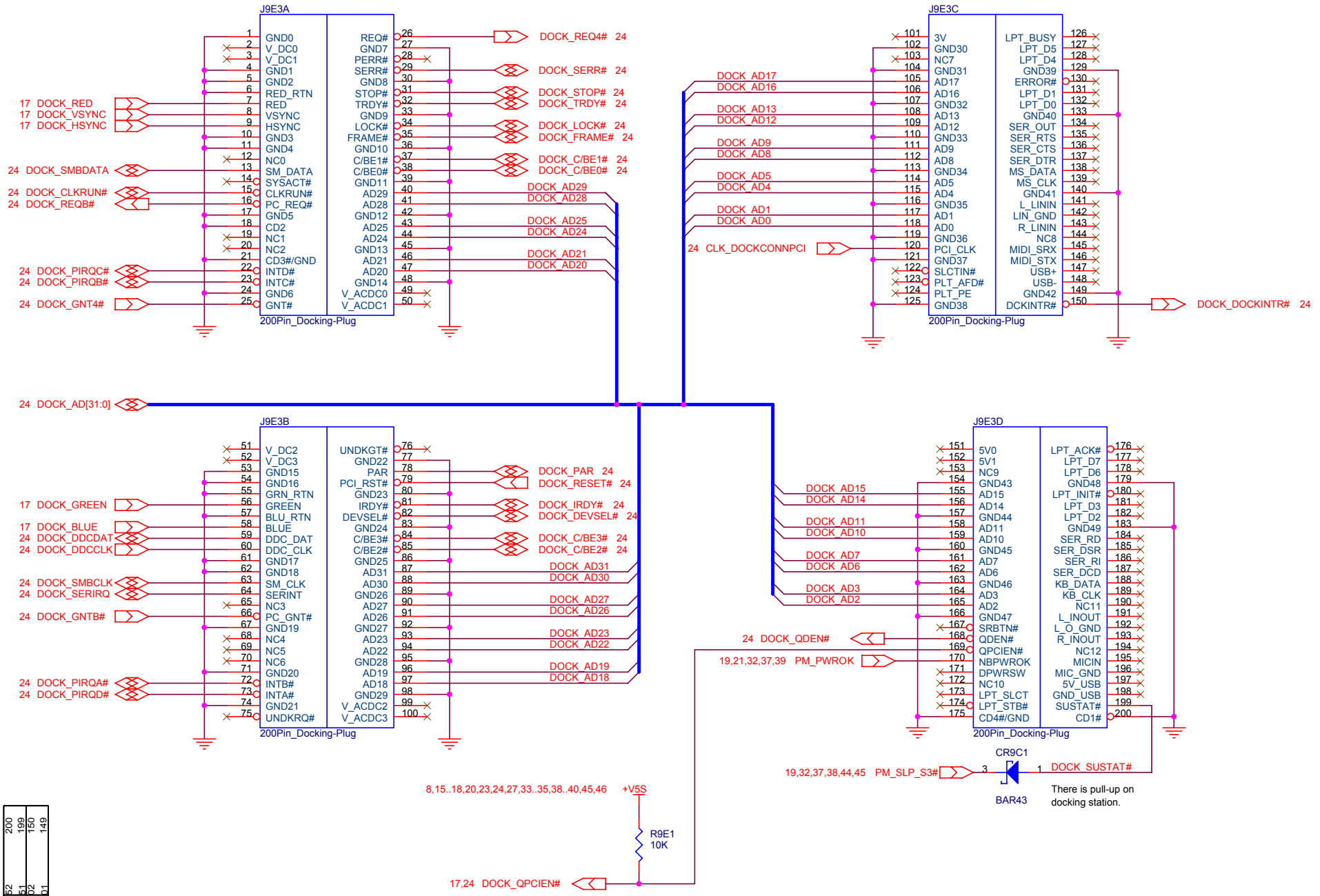
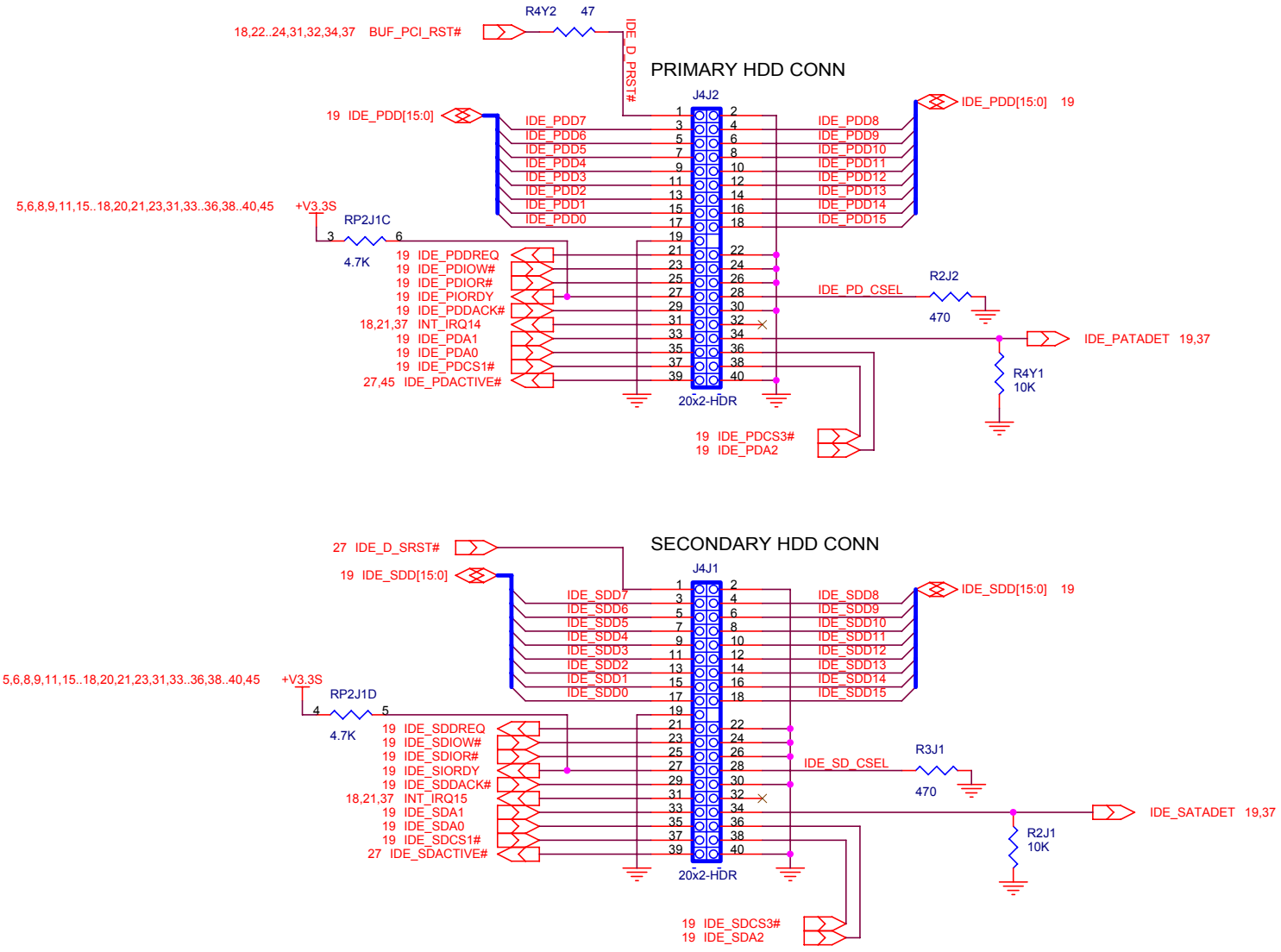


Title	Docking Connector		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
Date: Monday, September 15, 2003		Sheet 25 of 50	



Title	IDE 1 of 2		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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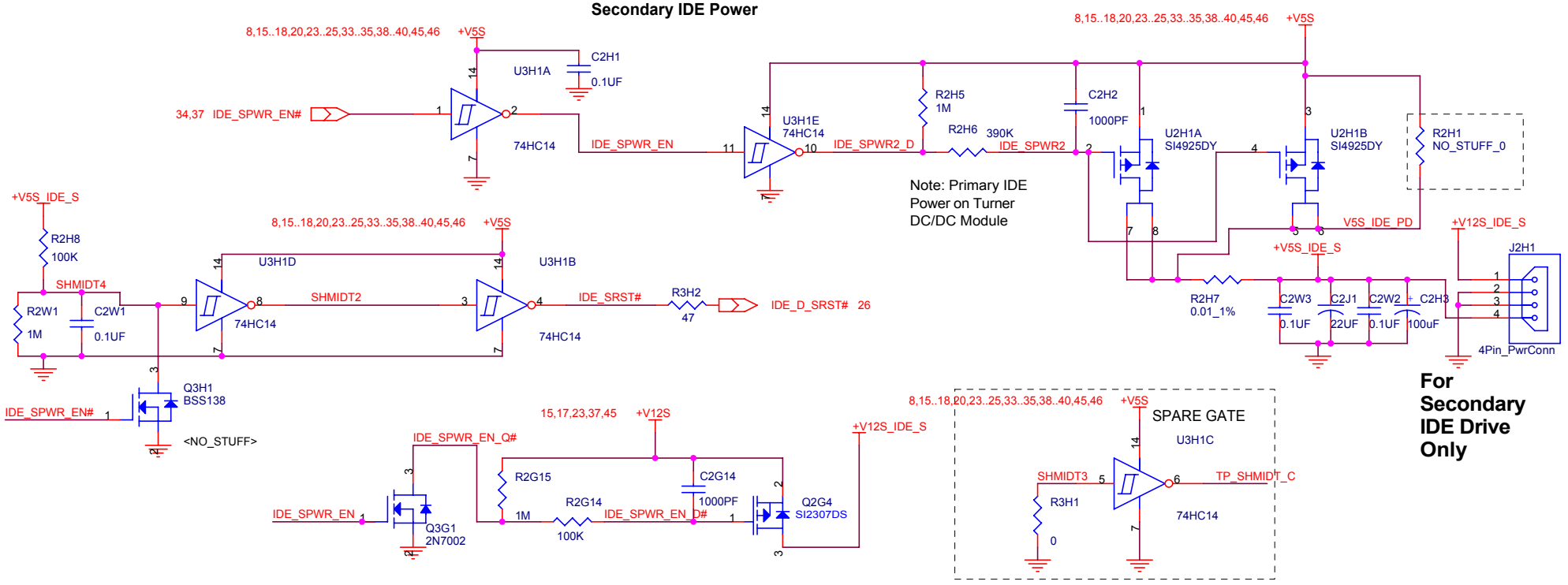
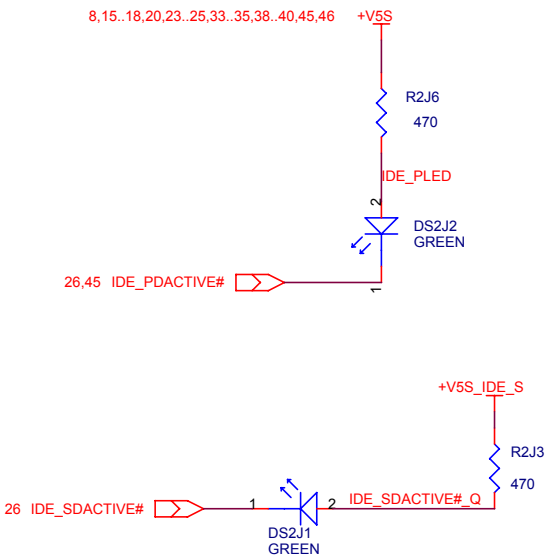
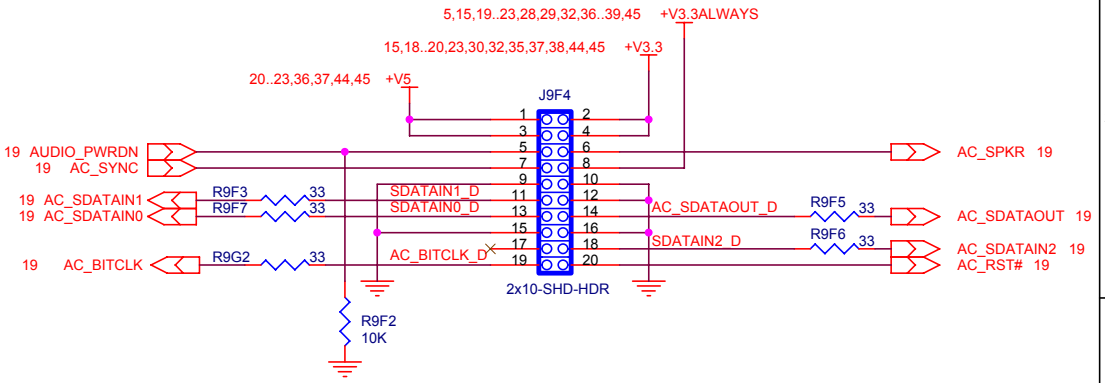
Secondary IDE Power



IDE Activity LEDs



MDC Interposer Header



Layout Note:
Place R9F3, R9F7 and R9G2 0.1 to 0.4 inches from MDC header based on topology

Title: IDE 2 of 2 / MDC INTERPOSER			
Size: A	Project: Intel 855GM/GME CRB	Document Number: <Doc>	Rev: 4.401
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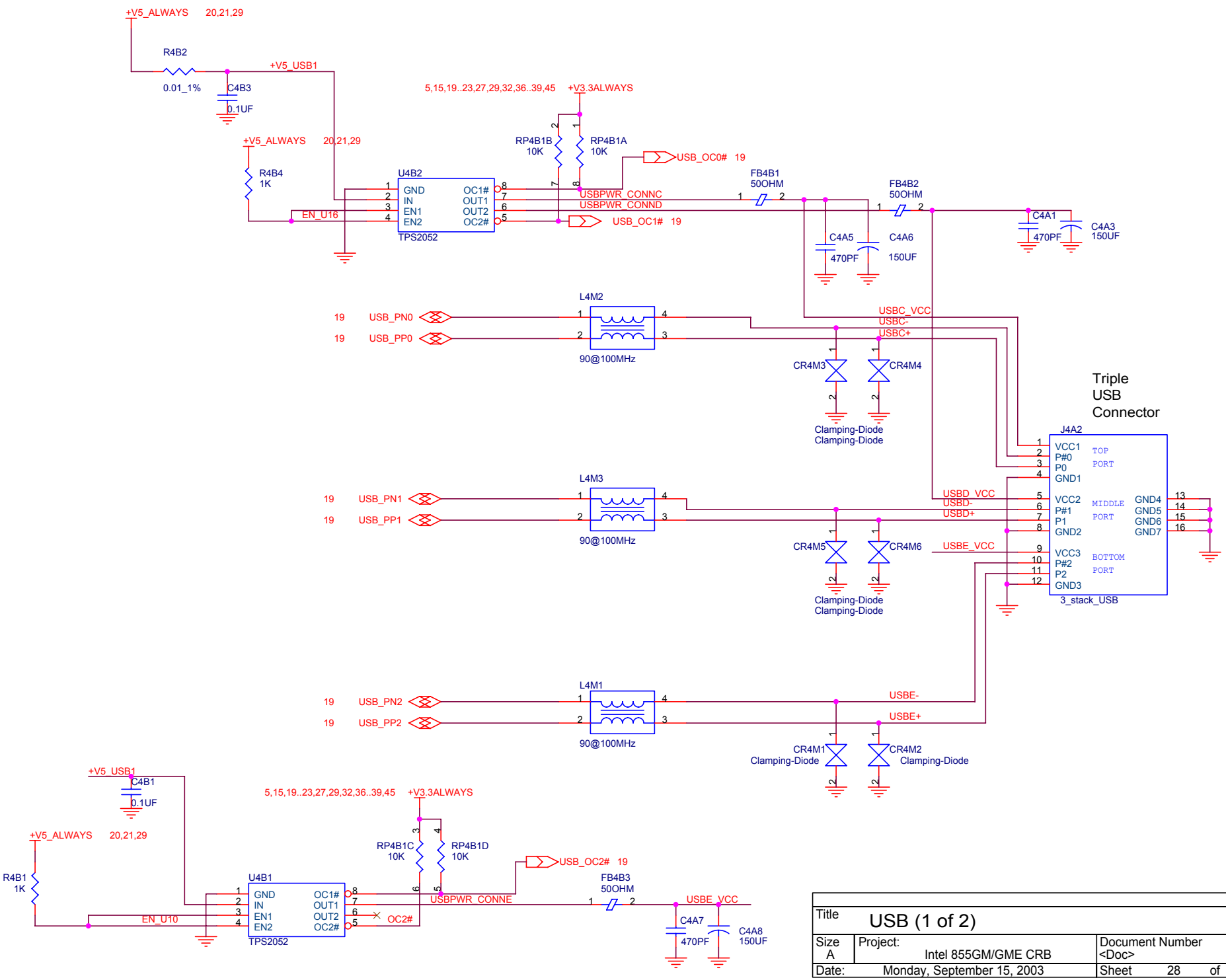

Title	USB (1 of 2)		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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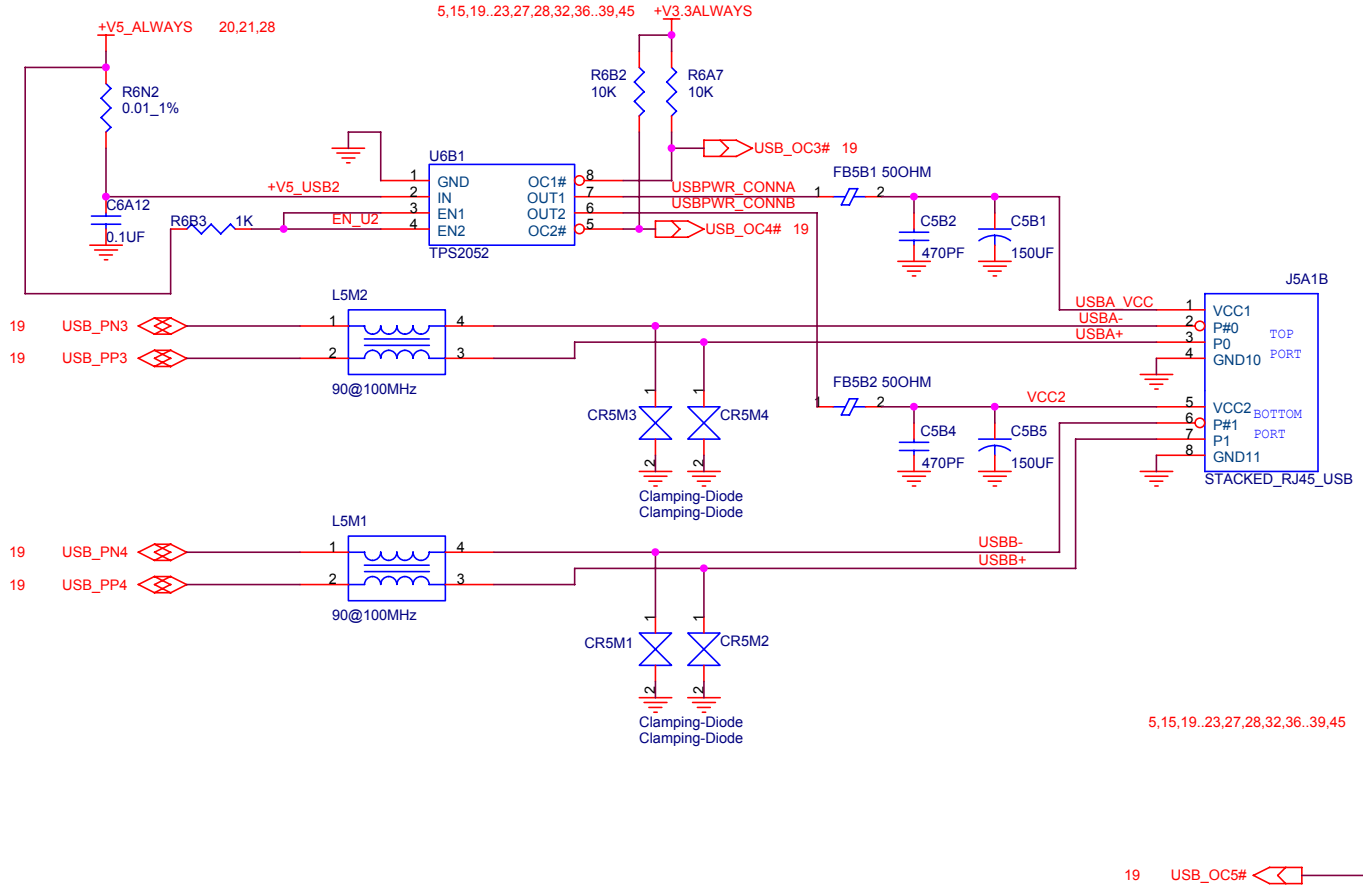
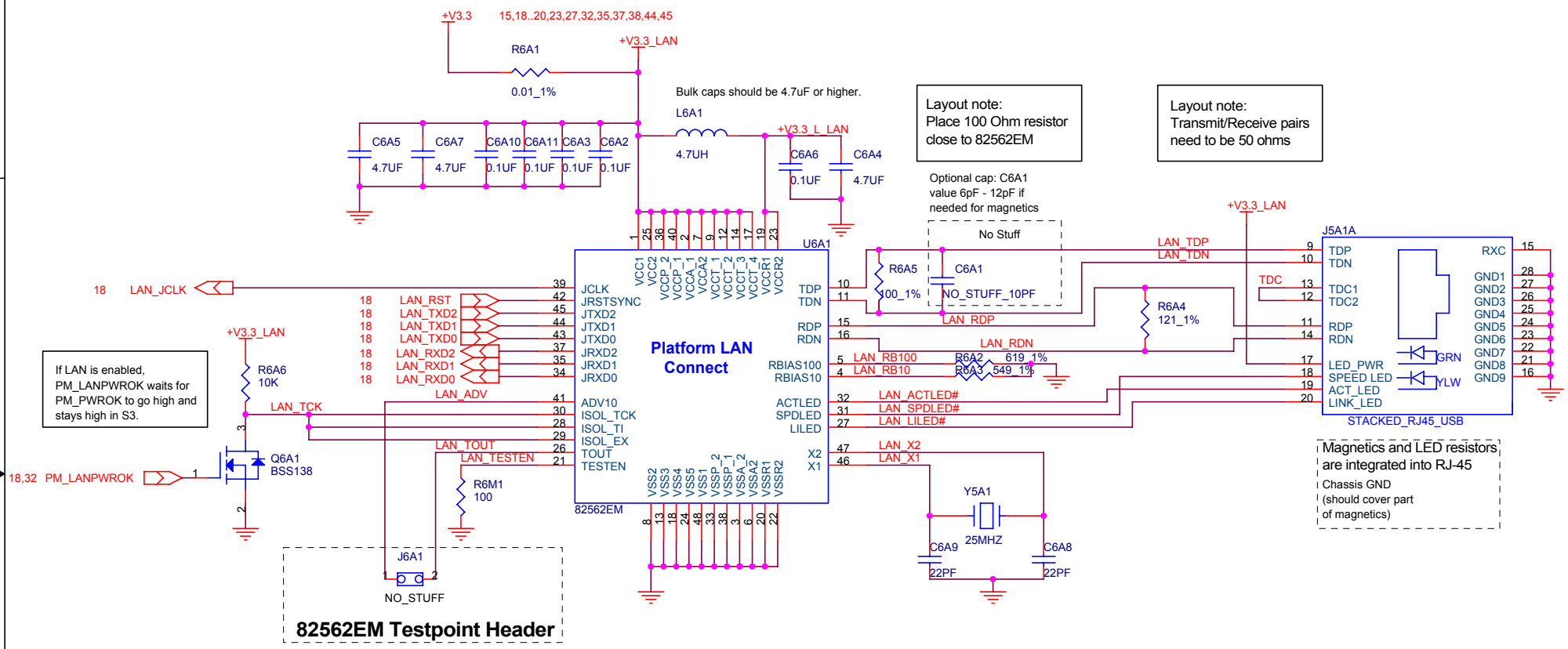


Title	USB Connector (2 of 2)		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
Date: Monday, September 15, 2003		Sheet 29 of 50	



Title	LAN Interface (82562EM)		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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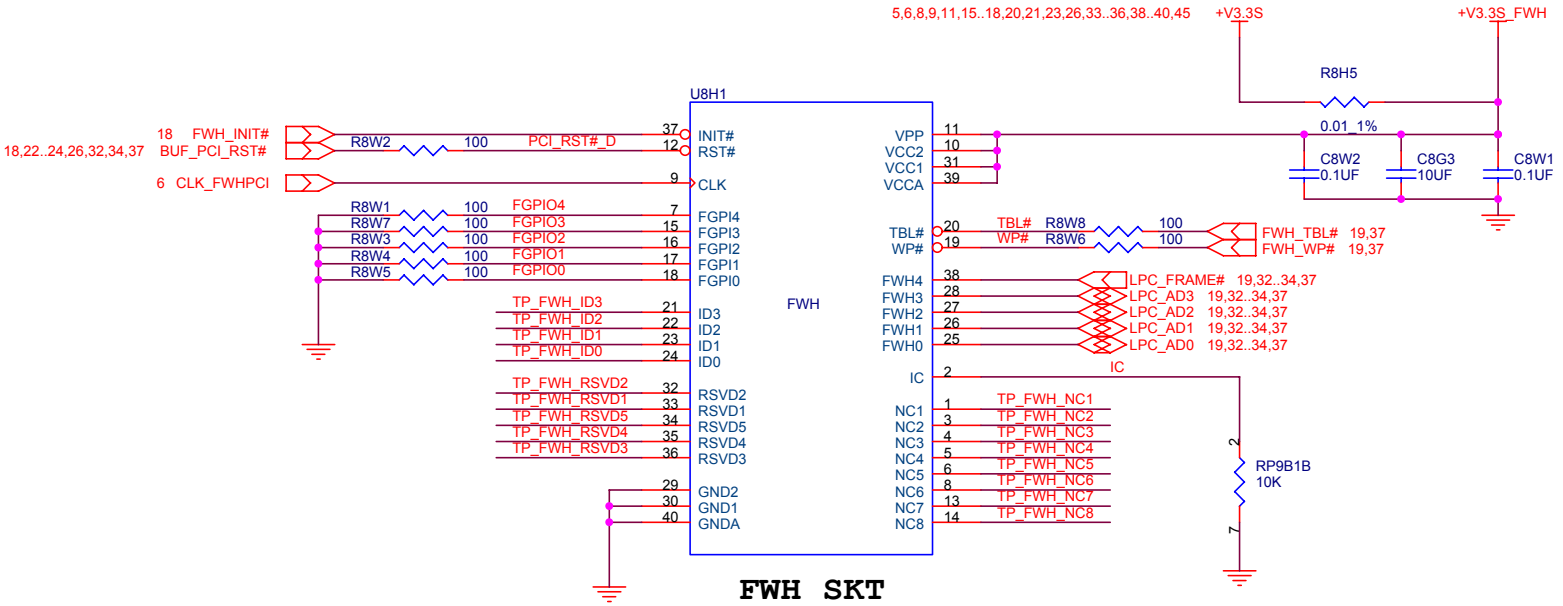

FWH SKT

FWH sits in the FWH_TSOP_Socket, Not on the board

Title: FWH			
Size: A	Project: Intel 855GM/GME CRB	Document Number: <Doc>	Rev: 4.401
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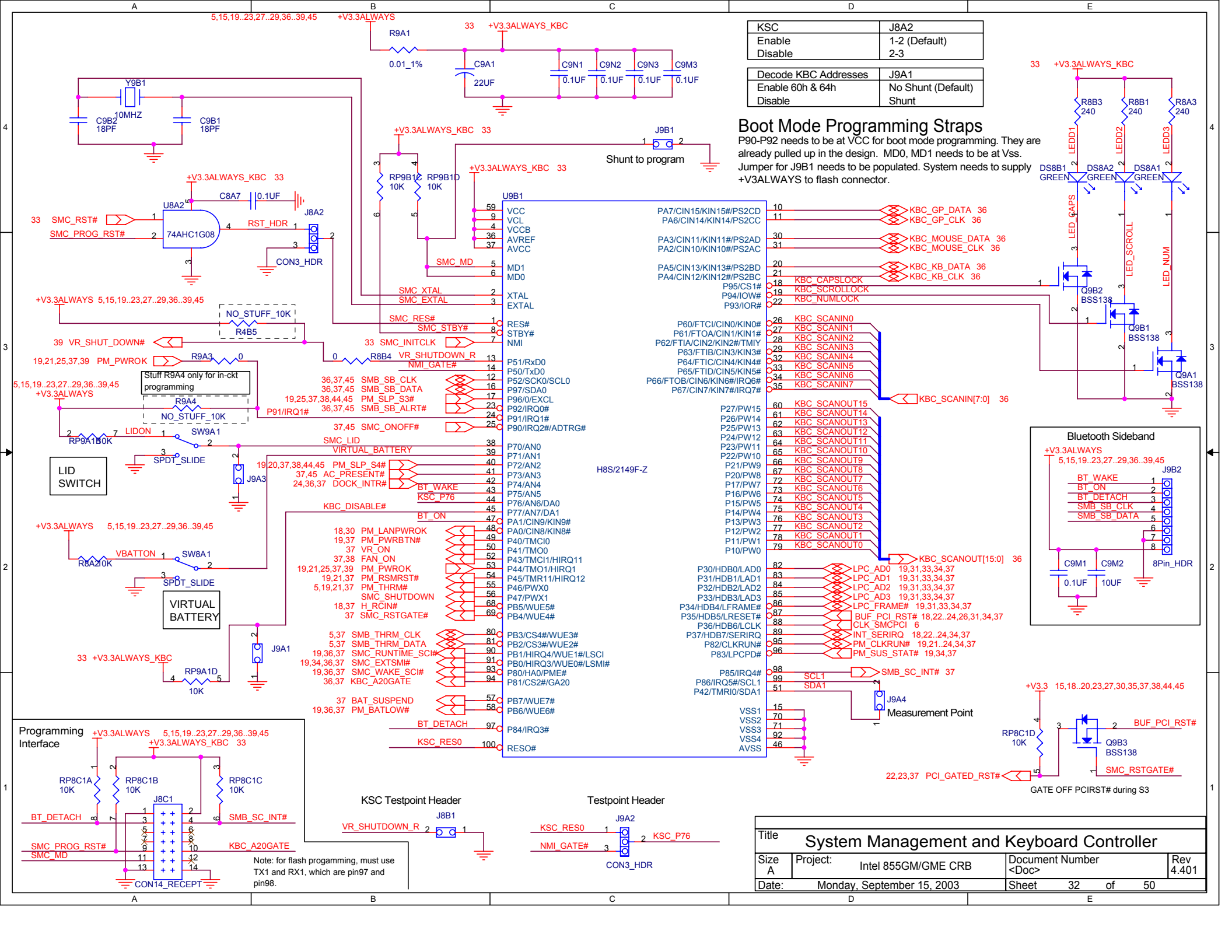
KSC | J8A2
Enable | 1-2 (Default)
Disable | 2-3
Decode KBC Addresses | J9A1
Enable 60h & 64h | No Shunt (Default)
Disable | Shunt
Boot Mode Programming Straps
P90-P92 needs to be at VCC for boot mode programming. They are already pulled up in the design. MD0, MD1 needs to be at Vss. Jumper for J9B1 needs to be populated. System needs to supply +V3ALWAYS to flash connector.
H8S/2149F-Z
U9B1
LID SWITCH
VIRTUAL BATTERY
Bluetooth Sideband
Programming Interface
KSC Testpoint Header
Testpoint Header
Measurement Point
Shunt to program
Stuff R9A4 only for in-ckt programming
Note: for flash progamming, must use TX1 and RX1, which are pin97 and pin98.
GATE OFF PCIRST# during S3
Title
System Management and Keyboard Controller
Size A
Project: Intel 855GM/GME CRB
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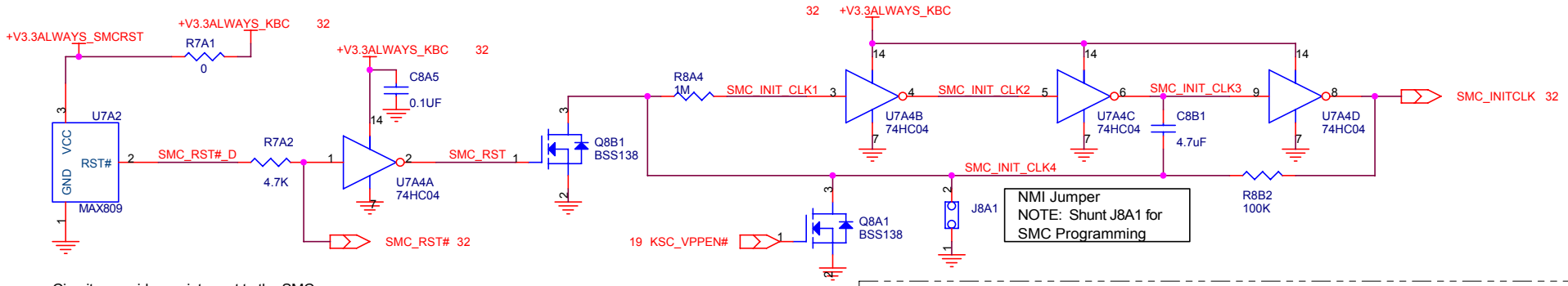
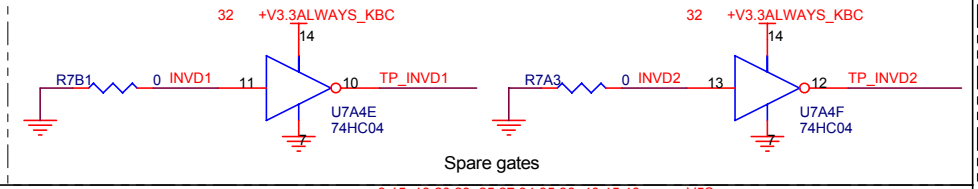
SMC SUSPEND TIMER

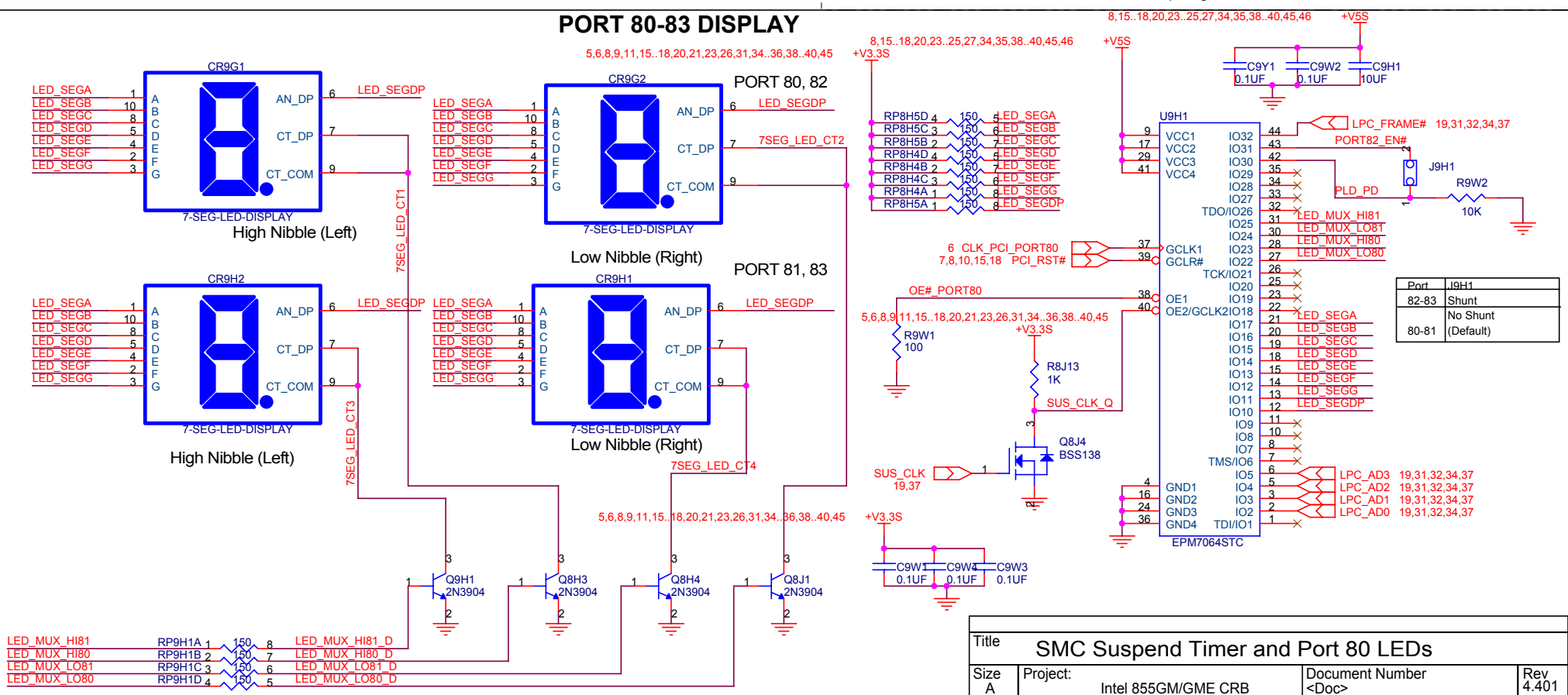


Circuitry provides an interrupt to the SMC every 1s while in suspend (this allows the SMC to complete housekeeping functions while suspended)

1Hz Clock	J8A1
Disable	Shunt (Default)
Enable	No Shunt



PORT 80-83 DISPLAY



Port	J9H1
82-83	Shunt
80-81	No Shunt (Default)

Title	SMC Suspend Timer and Port 80 LEDs		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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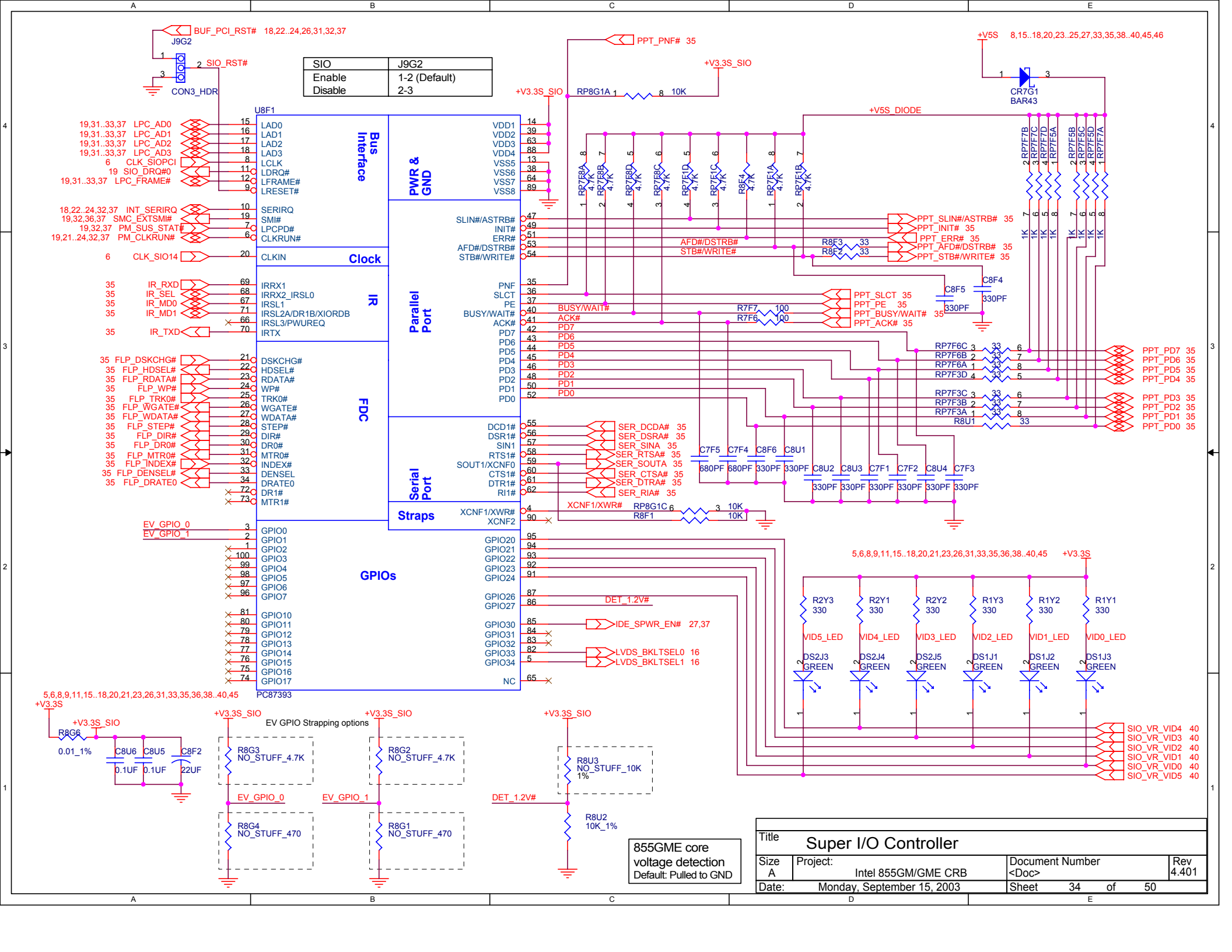
BUF_PCI_RST# 18,22..24,26,31,32,37
J9G2
SIO_RST#
CON3_HDR
SIO | J9G2
Enable | 1-2 (Default)
Disable | 2-3
U8F1
Bus Interface
LAD0
LAD1
LAD2
LAD3
LCLK
LDRQ#
LFRAME#
LRESET#
SERIRQ
SMI#
LPCPD#
CLKRUN#
Clock
CLKIN
IR
IRRX1
IRRX2_IRSL0
IRSL1
IRSL2A/DR1B/XIORDB
IRSL3/PWUREQ
IRTX
FDC
DSKCHG#
HDSEL#
RDATA#
WP#
TRK0#
WGATE#
WDATA#
STEP#
DIR#
DR0#
MTR0#
INDEX#
DENSEL
DRATE0
DR1#
MTR1#
GPIOs
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
PC87393
PWR & GND
VDD1
VDD2
VDD3
VDD4
VSS5
VSS6
VSS7
VSS8
Parallel Port
SLIN#/ASTRB#
INIT#
ERR#
AFD#/DSTRB#
STB#/WRITE#
PNF
SLCT
PE
BUSY/WAIT#
ACK#
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
Serial Port
DCD1#
DSR1#
SIN1
RTS1#
SOUT1/XCNF0
CTS1#
DTR1#
RI1#
Straps
XCNF1/XWR#
XCNF2
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO26
GPIO27
GPIO30
GPIO31
GPIO32
GPIO33
GPIO34
NC
DET_1.2V#
IDE_SPWR_EN# 27,37
LVDS_BKLTSEL0 16
LVDS_BKLTSEL1 16
+V3.3S_SIO
RP8G1A 10K
PPT_PNF# 35
+V5S 8,15..18,20,23..25,27,33,35,38..40,45,46
CR7G1
BAR43
+V5S_DIODE
PPT_SLIN#/ASTRB# 35
PPT_INIT# 35
PPT_ERR# 35
PPT_AFD#/DSTRB# 35
PPT_STB#/WRITE# 35
PPT_SLCT 35
PPT_PE 35
PPT_BUSY/WAIT# 35
PPT_ACK# 35
PPT_PD7 35
PPT_PD6 35
PPT_PD5 35
PPT_PD4 35
PPT_PD3 35
PPT_PD2 35
PPT_PD1 35
PPT_PD0 35
SER_DCDA# 35
SER_DSRA# 35
SER_SINA 35
SER_RTSA# 35
SER_SOUTA 35
SER_CTSA# 35
SER_DTRA# 35
SER_RIA# 35
XCNF1/XWR# RP8G1C 10K
R8F1 10K
EV_GPIO_0
EV_GPIO_1
5,6,8,9,11,15..18,20,21,23,26,31,33,35,36,38..40,45 +V3.3S
R2Y3 330 VID5_LED DS2J3 GREEN
R2Y1 330 VID4_LED DS2J4 GREEN
R2Y2 330 VID3_LED DS2J5 GREEN
R1Y3 330 VID2_LED DS1J1 GREEN
R1Y2 330 VID1_LED DS1J2 GREEN
R1Y1 330 VID0_LED DS1J3 GREEN
SIO_VR_VID4 40
SIO_VR_VID3 40
SIO_VR_VID2 40
SIO_VR_VID1 40
SIO_VR_VID0 40
SIO_VR_VID5 40
5,6,8,9,11,15..18,20,21,23,26,31,33,35,36,38..40,45 +V3.3S
R8G6 0.01_1%
C8U6 0.1UF
C8U5 0.1UF
C8F2 22UF
EV GPIO Strapping options
R8G3 NO_STUFF_4.7K
R8G2 NO_STUFF_4.7K
R8G4 NO_STUFF_470
R8G1 NO_STUFF_470
R8U3 NO_STUFF_10K 1%
R8U2 10K_1%
855GME core voltage detection
Default: Pulled to GND
Title
Super I/O Controller
Size A
Project: Intel 855GM/GME CRB
Document Number <Doc>
Rev 4.401
Date: Monday, September 15, 2003
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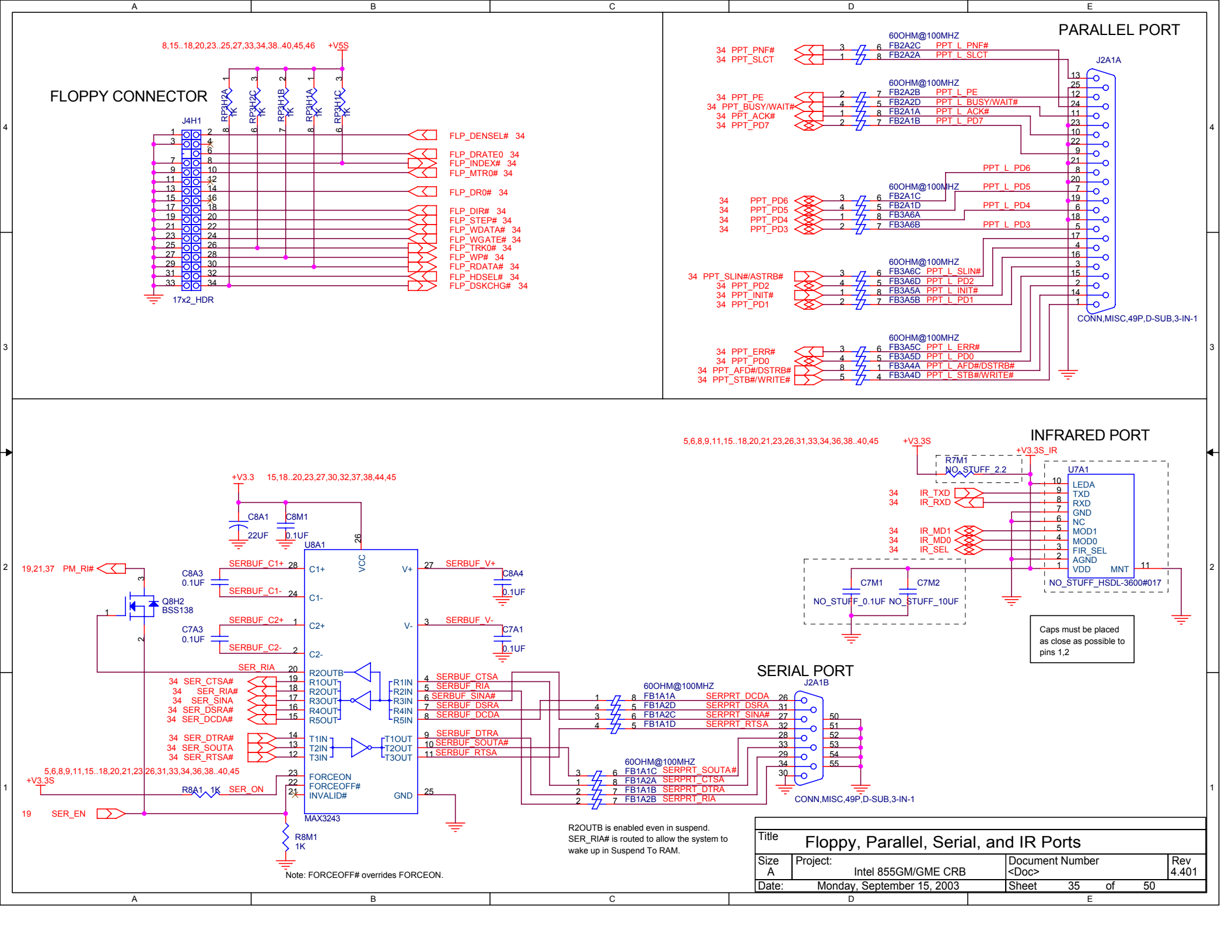
FLOPPY CONNECTOR
8,15..18,20,23..25,27,33,34,38..40,45,46
+V5S
RP3H2A 1K
RP3H2C 1K
RP3H2B 1K
RP3H1A 1K
RP3H1C 1K
J4H1
17x2_HDR
FLP_DENSEL# 34
FLP_DRATE0 34
FLP_INDEX# 34
FLP_MTR0# 34
FLP_DR0# 34
FLP_DIR# 34
FLP_STEP# 34
FLP_WDATA# 34
FLP_WGATE# 34
FLP_TRK0# 34
FLP_WP# 34
FLP_RDATA# 34
FLP_HDSEL# 34
FLP_DSKCHG# 34
PARALLEL PORT
60OHM@100MHZ
34 PPT_PNF#
34 PPT_SLCT
FB2A2C PPT_L_PNF#
FB2A2A PPT_L_SLCT
J2A1A
34 PPT_PE
34 PPT_BUSY/WAIT#
34 PPT_ACK#
34 PPT_PD7
FB2A2B PPT_L_PE
FB2A2D PPT_L_BUSY/WAIT#
FB2A1A PPT_L_ACK#
FB2A1B PPT_L_PD7
PPT_L_PD6
PPT_L_PD5
PPT_L_PD4
PPT_L_PD3
34 PPT_PD6
34 PPT_PD5
34 PPT_PD4
34 PPT_PD3
FB2A1C
FB2A1D
FB3A6A
FB3A6B
34 PPT_SLIN#/ASTRB#
34 PPT_PD2
34 PPT_INIT#
34 PPT_PD1
FB3A6C PPT_L_SLIN#
FB3A6D PPT_L_PD2
FB3A5A PPT_L_INIT#
FB3A5B PPT_L_PD1
34 PPT_ERR#
34 PPT_PD0
34 PPT_AFD#/DSTRB#
34 PPT_STB#/WRITE#
FB3A5C PPT_L_ERR#
FB3A5D PPT_L_PD0
FB3A4A PPT_L_AFD#/DSTRB#
FB3A4D PPT_L_STB#/WRITE#
CONN,MISC,49P,D-SUB,3-IN-1
INFRARED PORT
5,6,8,9,11,15..18,20,21,23,26,31,33,34,36,38..40,45
+V3.3S
+V3.3S_IR
R7M1
NO_STUFF 2.2
U7A1
34 IR_TXD
34 IR_RXD
34 IR_MD1
34 IR_MD0
34 IR_SEL
LEDA
TXD
RXD
GND
NC
MOD1
MOD0
FIR_SEL
AGND
VDD
MNT
NO_STUFF_HSDL-3600#017
C7M1
C7M2
NO_STUFF_0.1UF
NO_STUFF_10UF
Caps must be placed as close as possible to pins 1,2
+V3.3
15,18..20,23,27,30,32,37,38,44,45
C8A1 22UF
C8M1 0.1UF
U8A1
MAX3243
VCC
GND
C1+
C1-
C2+
C2-
V+
V-
19,21,37 PM_RI#
Q8H2 BSS138
C8A3 0.1UF
C7A3 0.1UF
C8A4 0.1UF
C7A1 0.1UF
SERBUF_C1+
SERBUF_C1-
SERBUF_C2+
SERBUF_C2-
SERBUF_V+
SERBUF_V-
SER_RIA
R2OUTB
R1OUT
R2OUT
R3OUT
R4OUT
R5OUT
R1IN
R2IN
R3IN
R4IN
R5IN
34 SER_CTSA#
34 SER_RIA#
34 SER_SINA
34 SER_DSRA#
34 SER_DCDA#
SERBUF_CTSA
SERBUF_RIA
SERBUF_SINA#
SERBUF_DSRA
SERBUF_DCDA
34 SER_DTRA#
34 SER_SOUTA
34 SER_RTSA#
T1IN
T2IN
T3IN
T1OUT
T2OUT
T3OUT
SERBUF_DTRA
SERBUF_SOUTA#
SERBUF_RTSA
FORCEON
FORCEOFF#
INVALID#
5,6,8,9,11,15..18,20,21,23,26,31,33,34,36,38..40,45
+V3.3S
R8A1 1K SER_ON
19 SER_EN
R8M1 1K
Note: FORCEOFF# overrides FORCEON.
SERIAL PORT
J2A1B
60OHM@100MHZ
FB1A1A SERPRT_DCDA
FB1A2D SERPRT_DSRA
FB1A2C SERPRT_SINA#
FB1A1D SERPRT_RTSA
FB1A1C SERPRT_SOUTA#
FB1A2A SERPRT_CTSA
FB1A1B SERPRT_DTRA
FB1A2B SERPRT_RIA
CONN,MISC,49P,D-SUB,3-IN-1
R2OUTB is enabled even in suspend.
SER_RIA# is routed to allow the system to wake up in Suspend To RAM.
Title
Floppy, Parallel, Serial, and IR Ports
Size A
Project: Intel 855GM/GME CRB
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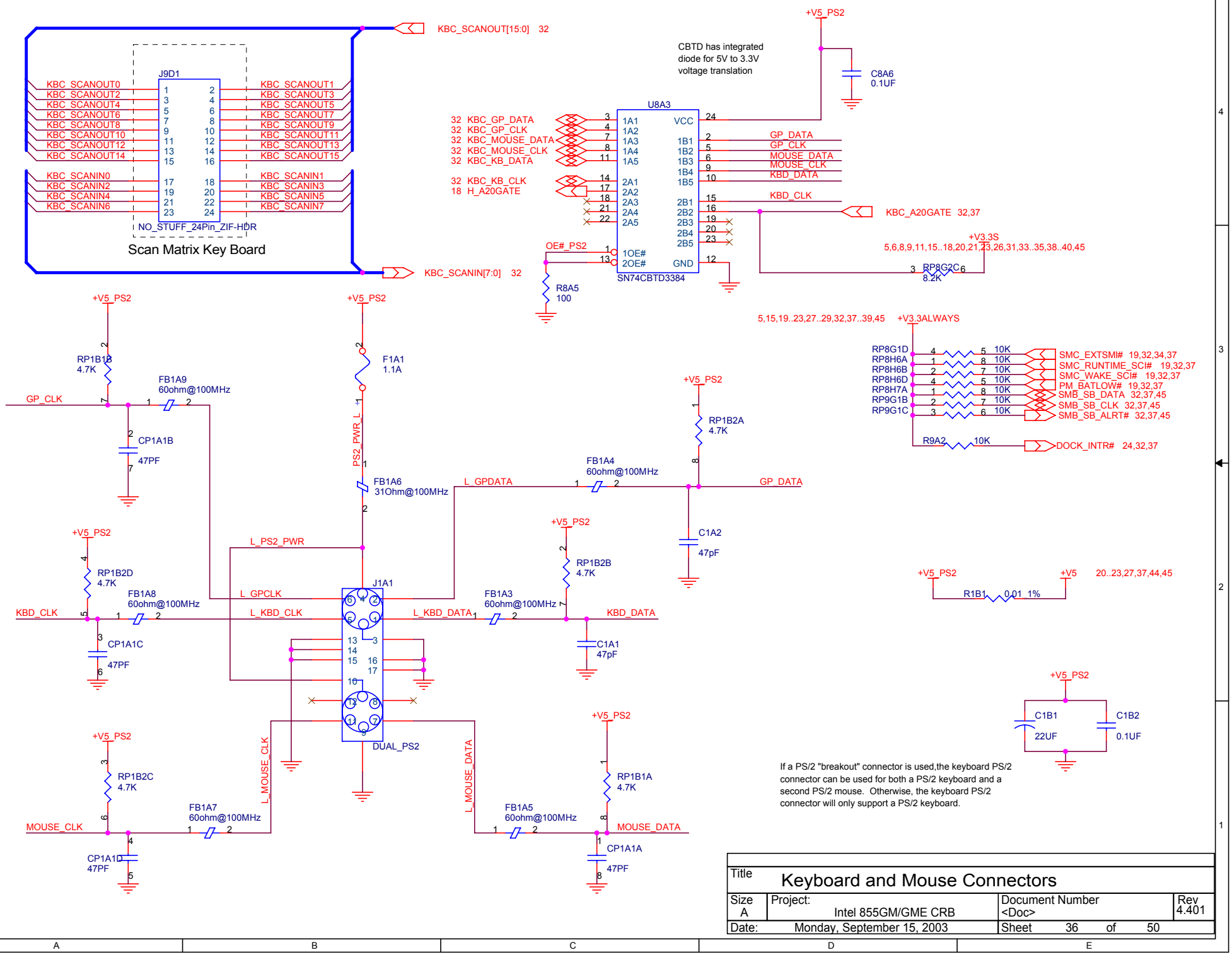

Title	Keyboard and Mouse Connectors		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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LPC POWERED ON SUSPEND RAIL FOR ADD-IN H8 CARD

LPC Debug Slot

J8F1

60Pin_CardCon

B1	12V1	12V2	A1
B2	SUSCLK	NEG_12V	A2
B3	GND1	GND2	A3
B4	LREQ	BP_CLK	A4
B5	VCC3_1	VCC3_2	A5
B6	LCNTL0	LCNTL1	A6
B7	GND3	GND5	A7
B8	LDC	LD6	A8
B9	LD5	LD4	A9
B10	GND4	GND7	A10
B11	LD3	LD2	A11
B12	LD1	LD0	A12
B13	GND6	VCC5_2	A13
B14	3V_STBY	SCLK	A14
B15	LPS	GND10	A15
B16	KBRESTE#	SERIRQ	A16
B17	A20GATE#	CLKRUN#	A17
B18	GND8	GND12	A18
B19	LSMI#	LINK_ON	A19
	KEY		
B20	VCC5_1	VCC5_3	A20
B21	LDRQ1#	LDRQ0#	A21
B22	LFRAME1#	GND14	A22
B23	GND9	LAD3	A23
B24	LAD2	LAD1	A24
B25	LAD0	GND15	A25
B26	GND11	PCICLK	A26
B27	PCIRST#	LPCPD#	A27
B28	GND13	GND16	A28
B29	OSC	PME#	A29
B30	VCC3_3	VCC3_4	A30

15,17,23,27,45 +V12S
+V3.3_LPCSLOT
+V3.3_LPCSLOT
15,17,23,27,45 +V12S
19,33 SUS_CLK
5,15,19..23,27..29,32,36,38,39,45 +V3.3ALWAYS
+V5_LPCSLOT
+V5_LPCSLOT
18,32 H_RCIN#
32,36 KBC_A20GATE
19,32,34,36 SMC_EXTSMI#
INT_SERIRQ 18,22..24,32,34
PM_CLKRUN# 19,21..24,32,34
+V5_LPCSLOT
19 LPC_DRQ#1
19,31..34 LPC_FRAME#
19,31..34 LPC_AD2
19,31..34 LPC_AD0
6 CLK_LPC14
LPC_DRQ#0 19
LPC_AD3 19,31..34
LPC_AD1 19,31..34
CLK_LPCPCI 6
PM_SUS_STAT# 19,32,34
PCI_PME# 15,18,22,23
LPC_RST#
22,23,32 PCI_GATED_RST#
R9G3 NO_STUFF_0
R9G4 0
BUF_PCI_RST# 18,22..24,26,31,32,34

Layout Note:
Line up LPC slot with PCI Slot 3

SMC Sidebands for LPC Power Management

J9D2

15x2_HDR

5,19,21,32 PM_THRM#	1	2	SMC_RUNTIME_SCI# 19,32,36
19,32 PM_PWRBTN#	3	4	SMC_WAKE_SCI# 19,32,36
32,45 SMC_ONOFF#	5	6	FAN_ON 32,38
32 VR_ON	7	8	SMB_THRM_CLK 5,32
19,21,25,32,39 PM_PWROK	9	10	SMB_THRM_DATA 5,32
	11	12	
19,21,32 PM_RSMRST#	13	14	SMB_SB_CLK 32,36,45
32,45 AC_PRESENT#	15	16	SMB_SB_DATA 32,36,45
	17	18	SMB_SB_ALRT# 32,36,45
19,25,32,38,44,45 PM_SLP_S3#	19	20	PM_BATLOW# 19,32,36
	21	22	
45 GATED_SMC_SHUTDOWN	23	24	
32 BAT_SUSPEND	25	26	
32 SMC_RSTGATE#	27	28	SMB_SC_INT# 32
24,32,36 DOCK_INTR#	29	30	

J3H1

2X8_HDR

3,18 H_PWRGD	1	2	
18,21 SM_INTRUDER#	3	4	H_INIT# 3,18
19,21,35 PM_RI#	5	6	H_INTR 3,18
3,7,18 H_DPSLP#	7	8	BUF_PCI_RST# 18,22..24,26,31,32,34
18,21 SMB_ALERT#	9	10	R4169 D
3,18 H_NMI	11	12	H_STPCLK# 3,18
3,18 H_SMI#	13	14	
	15	16	H_CPUSLP# 3,18

20..23,27,36,44,45 +V5
R3H3 1K

ICH4-M Testpoint Header

20,21 +V3.3ALWAYS_ICH
19..22,24 +V3.3S_ICH
R7J4 10K
R7J3 4.7K

J7J1

2X5-Header

19 ICH_GPIO7	1	2	IDE_PATADET 19,26
	3	4	IDE_SATADET 19,26
18,21..23 INT_PIRQH#	5	6	
19 ICH_MFG_MODE	7	8	
15,18,22,23 PCI_PME#	9	10	

J9J1

2X8_HDR

6,19,39 PM_STPCPU#	1	2	PM_STPPCI# 6,19
6,19,38,45 PM_SLP_S1#	3	4	INT_IRQ14 18,21,26
19 PM_C3_STAT#	5	6	INT_IRQ15 18,21,26
19 PM_CPUPERF#	7	8	AGP_SUSPEND# 19
7,39 VR_PWRGD	9	10	
	11	12	
	13	14	PM_CLKRUN# 19,21..24,32,34
	15	16	PM_SLP_S4# 19,20,32,38,44,45

J2J2

8Pin HDR
SIO Sidebands

27,34 IDE_SPWR_EN#	1	2	FWH_WP# 19,31
	3	4	FWH_TBL# 19,31
	5	6	
	7	8	

TEST HEADER

J2J1

8Pin HDR

19,32,34,36 SMC_EXTSMI#	1	2	DELAYED_VR_PWRGD 19,39
19,38 PM_SUS_S5#	3	4	PM_SUS_CLK 15,19
19,39 PM_DPRSLPVR	5	6	PM_GMUXSEL 19
	7	8	

NO STUFF

GROUND HEADERS

J9J4 J7E1 J7F2 J1H6 J2A2
J9J3 J7A1 J9E1 J1E2

20..23,27,36,44,45 +V5
R9G1 0.01 1%
C9G2 22UF
C9G1 0.1UF
+V5_LPCSLOT

+V3.3 15,18..20,23,27,30,32,35,38,44,45
R9G5 0.01 1%
C9G4 22UF
C8F1 0.1UF
C8F3 0.1UF
C9G3 0.1UF
+V3.3_LPCSLOT

Title	LPC Slot & Debug Headers		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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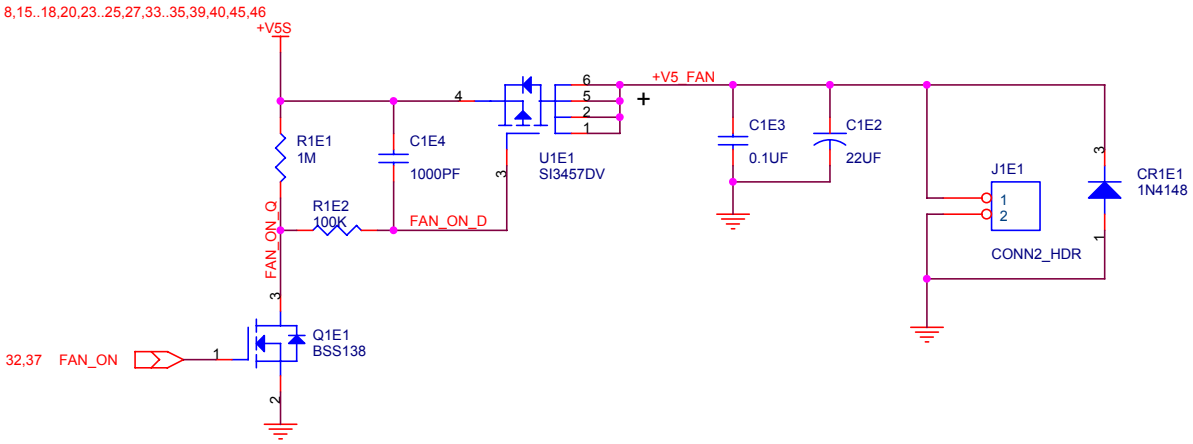
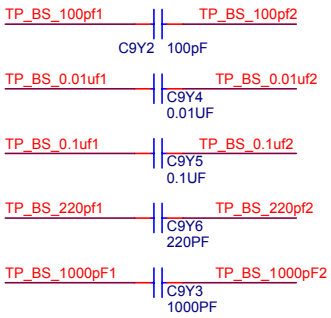
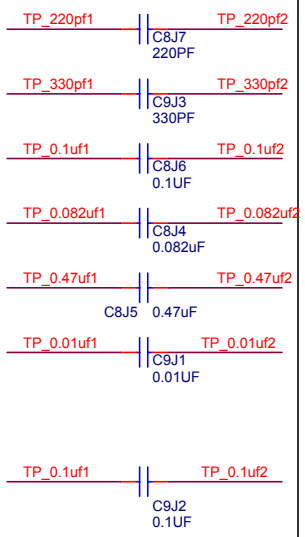
Fan Power Control



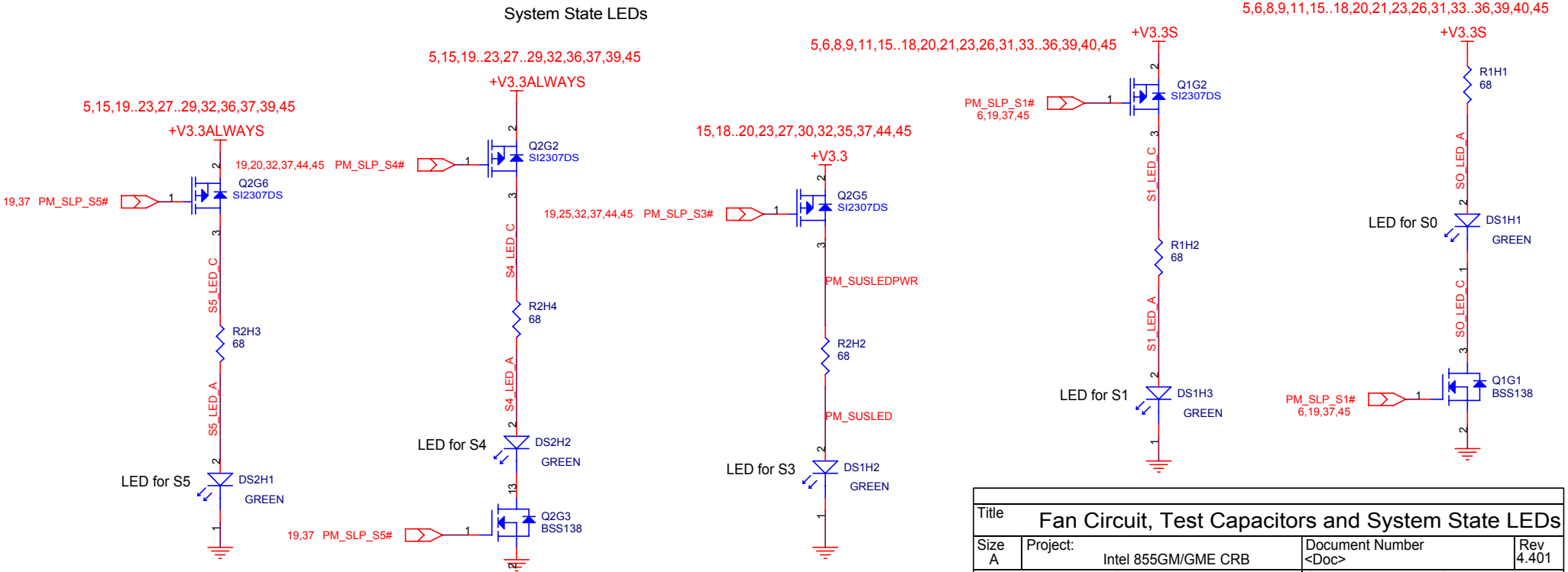
Test CAPs backside



Test CAPs



System State LEDs



Title	Fan Circuit, Test Capacitors and System State LEDs		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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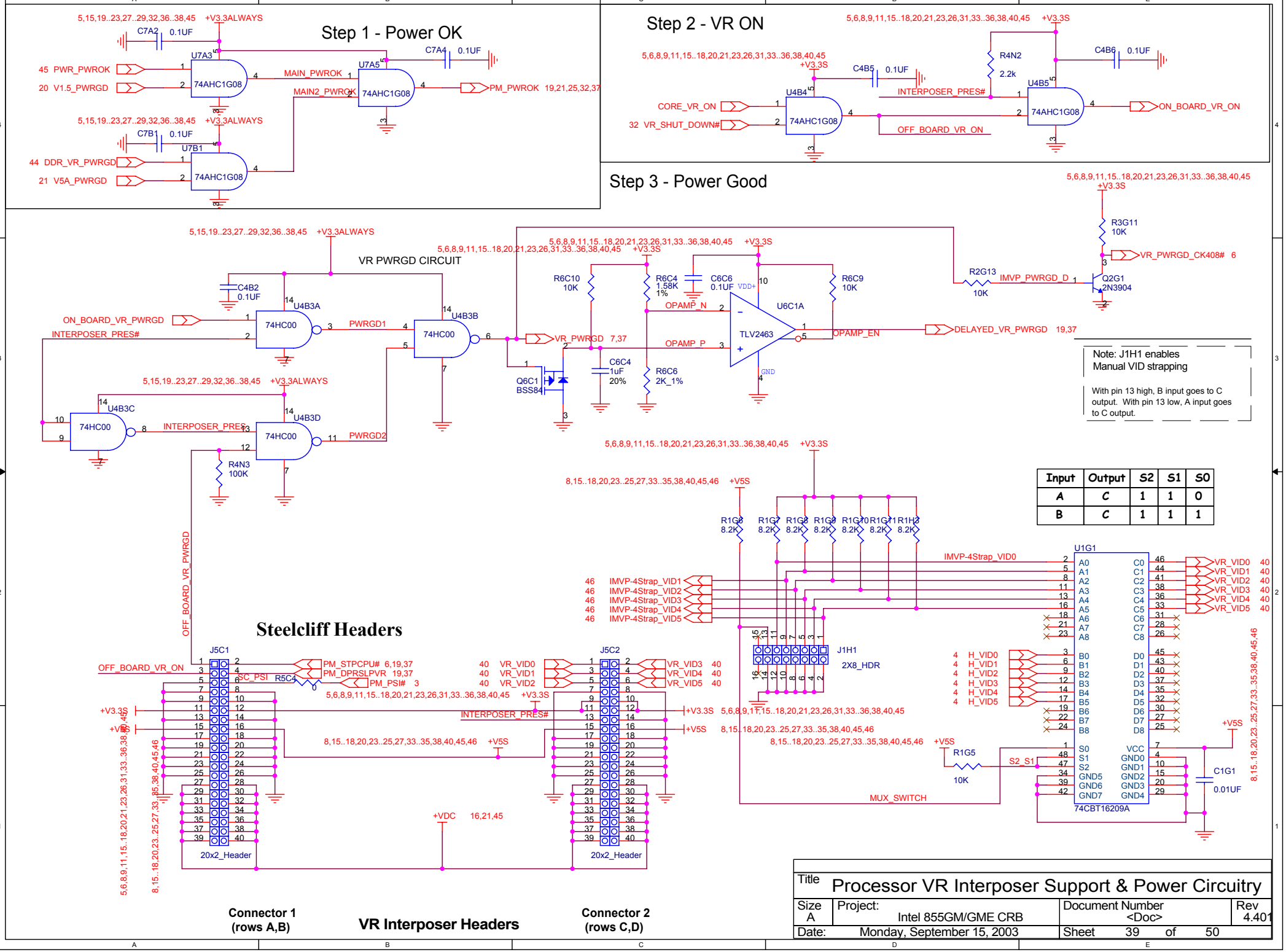
Step 1 - Power OK
Step 2 - VR ON
Step 3 - Power Good
VR PWRGD CIRCUIT
Steelcliff Headers
VR Interposer Headers
Connector 1 (rows A,B)
Connector 2 (rows C,D)
Note: J1H1 enables Manual VID strapping
With pin 13 high, B input goes to C output. With pin 13 low, A input goes to C output.
Input | Output | S2 | S1 | S0
A | C | 1 | 1 | 0
B | C | 1 | 1 | 1
Title: Processor VR Interposer Support & Power Circuitry
Size: A
Project: Intel 855GM/GME CRB
Document Number: <Doc>
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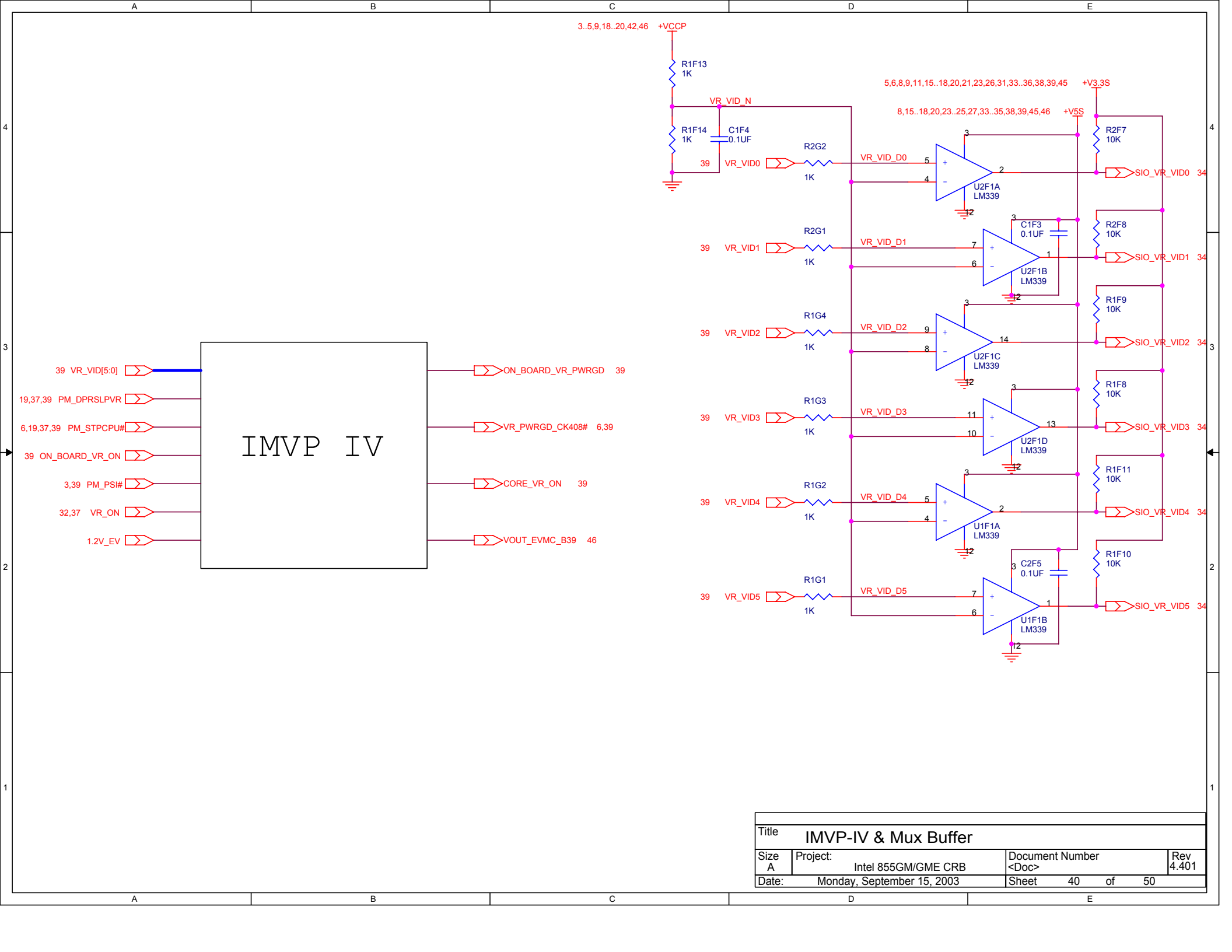

Title	IMVP-IV & Mux Buffer		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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Title: IMVP-IV VR Controller			
Size: B	Project: Intel 855GM/GME CRB	Document Number: <Doc>	Rev: 4.401
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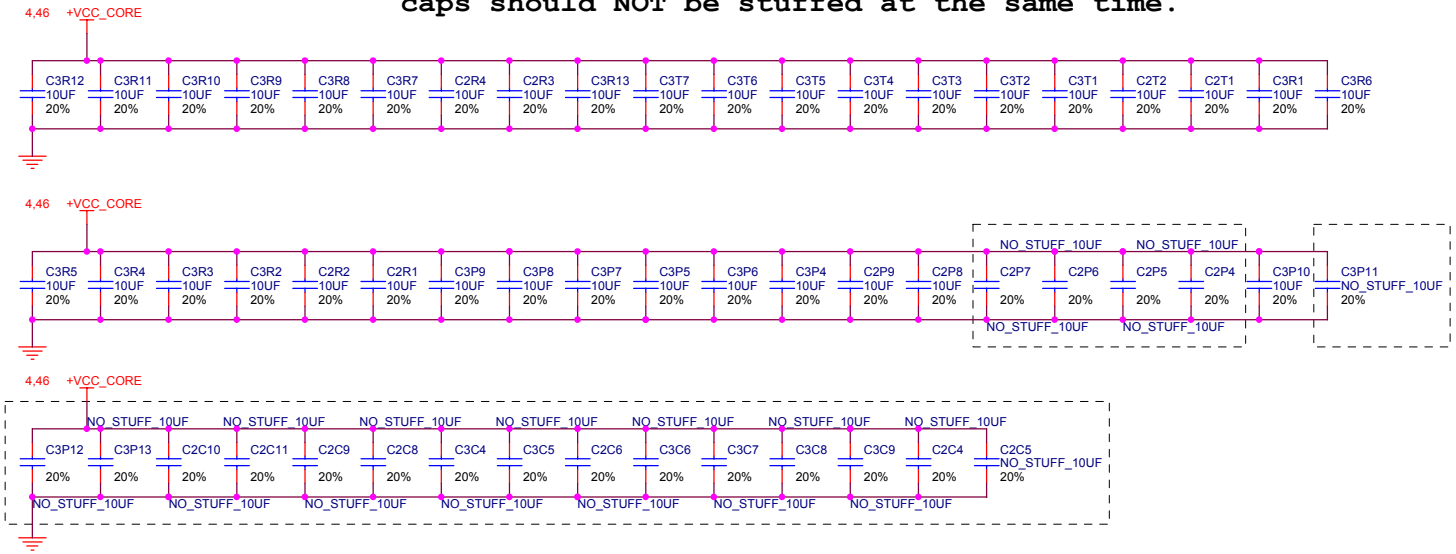
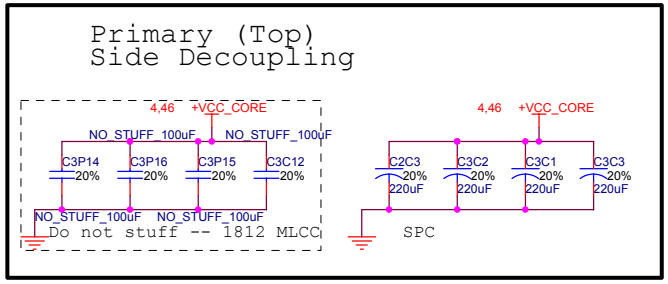
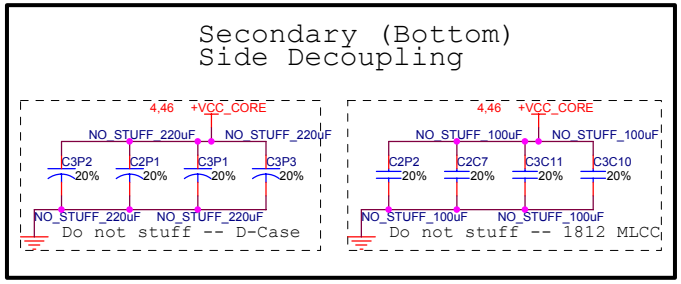
VCore HF and Bulk Decoupling

This solution will allow any of the decoupling options. All caps should NOT be stuffed at the same time.

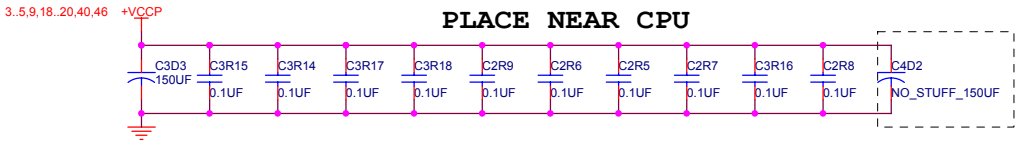






VCCP Decoupling

PLACE NEAR CPU



Title: Processor Decoupling			
Size: B	Project: Intel 855GM/GME CRB	Document Number: <Doc>	Rev: 4.401
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Title	855GME VR and VCCP		
Size B	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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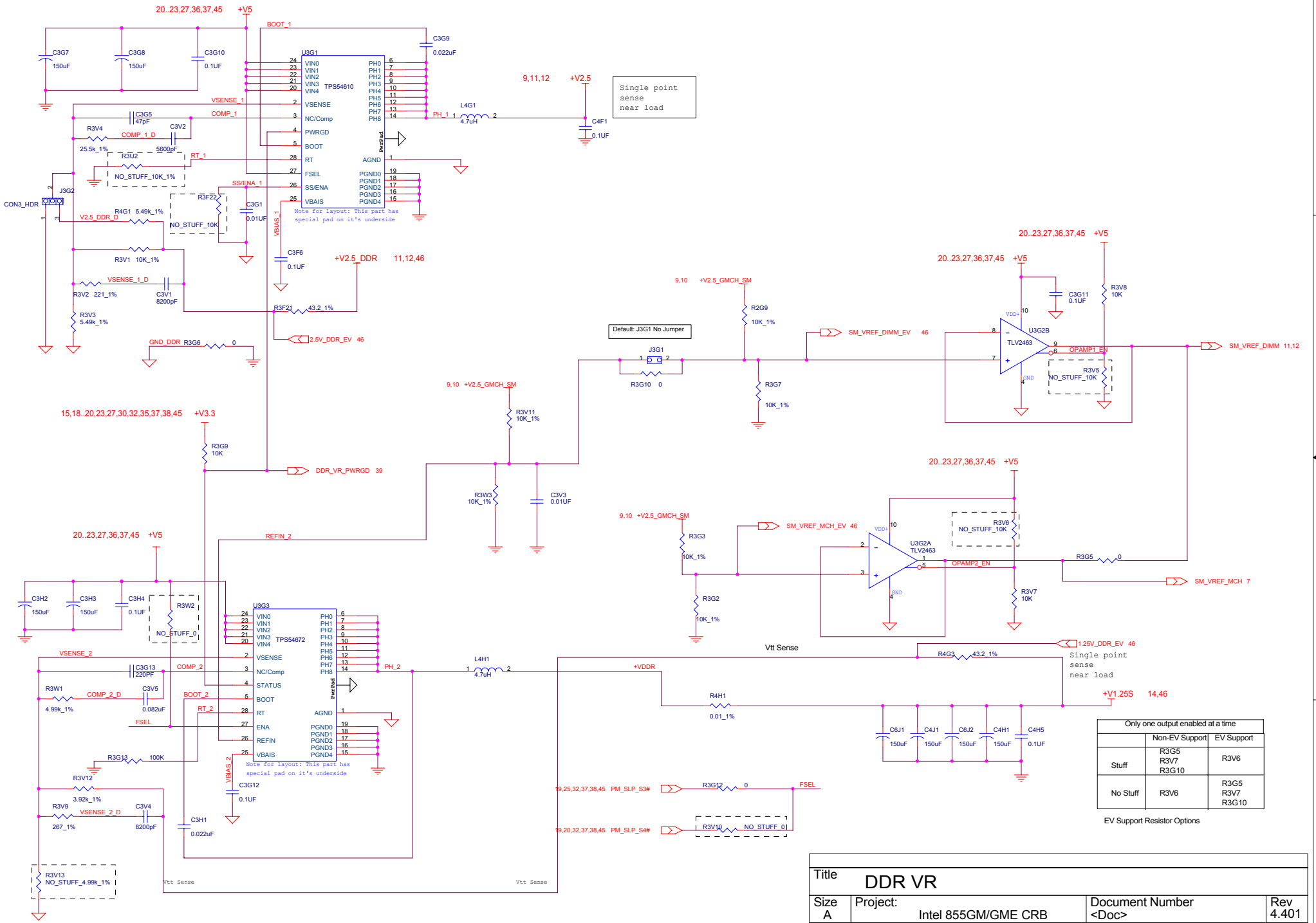
20..23,27,36,37,45 +V5
BOOT_1
C3G9 0.022uF
C3G7 150uF
C3G8 150uF
C3G10 0.1UF
U3G1
TPS54610
VIN0 VIN1 VIN2 VIN3 VIN4
PH0 PH1 PH2 PH3 PH4 PH5 PH6 PH7 PH8
VSENSE_1
VSENSE
COMP_1
NC/Comp
PWRGD
BOOT
RT
FSEL
SS/ENA
VBAIS
AGND
PGND0 PGND1 PGND2 PGND3 PGND4
PwrPad
PH_1
L4G1 4.7uH
9,11,12 +V2.5
C4F1 0.1UF
Single point sense near load
C3G5 47pF
C3V2 5600pF
R3V4 25.5k_1%
COMP_1_D
R3U2 NO_STUFF_10K_1%
RT_1
SS/ENA_1
R3F22 NO_STUFF_10K
C3G1 0.01UF
VBIAS_1
J3G2
CON3_HDR
R4G1 5.49k_1%
V2.5_DDR_D
R3V1 10K_1%
C3F6 0.1UF
+V2.5_DDR 11,12,46
VSENSE_1_D
R3V2 221_1%
C3V1 8200pF
R3V3 5.49k_1%
R3F21 43.2_1%
2.5V_DDR_EV 46
GND_DDR R3G6 0
Note for layout: This part has special pad on it's underside
20..23,27,36,37,45 +V5
C3G11 0.1UF
R3V8 10K
U3G2B TLV2463
VDD+ GND
OPAMP1_EN
R3V5 NO_STUFF_10K
SM_VREF_DIMM 11,12
9,10 +V2.5_GMCH_SM
R2G9 10K_1%
Default: J3G1 No Jumper
J3G1
R3G10 0
R3G7 10K_1%
SM_VREF_DIMM_EV 46
9,10 +V2.5_GMCH_SM
R3V11 10K_1%
15,18..20,23,27,30,32,35,37,38,45 +V3.3
R3G9 10K
DDR_VR_PWRGD 39
R3W3 10K_1%
C3V3 0.01UF
20..23,27,36,37,45 +V5
U3G2A TLV2463
R3V6 NO_STUFF_10K
OPAMP2_EN
R3G5 0
SM_VREF_MCH 7
R3V7 10K
9,10 +V2.5_GMCH_SM
R3G3 10K_1%
SM_VREF_MCH_EV 46
R3G2 10K_1%
20..23,27,36,37,45 +V5
REFIN_2
C3H2 150uF
C3H3 150uF
C3H4 0.1UF
R3W2 NO_STUFF_0
U3G3
TPS54672
VSENSE_2
C3G13 220PF
COMP_2
R3W1 4.99k_1%
COMP_2_D
C3V5 0.082uF
BOOT_2
RT_2
FSEL
R3G13 100K
R3V12 3.92k_1%
R3V9 267_1%
VSENSE_2_D
C3V4 8200pF
C3H1 0.022uF
VBIAS_2
C3G12 0.1UF
PH_2
L4H1 4.7uH
+VDDR
Vtt Sense
R4G3 43.2_1%
1.25V_DDR_EV 46
Single point sense near load
R4H1 0.01_1%
+V1.25S 14,46
C6J1 C4J1 C6J2 C4H1 150uF
C4H5 0.1UF
19,25,32,37,38,45 PM_SLP_S3#
R3G12 0
FSEL
19,20,32,37,38,45 PM_SLP_S4#
R3V10 NO_STUFF_0
R3V13 NO_STUFF_4.99k_1%
Vtt Sense
Vtt Sense
Only one output enabled at a time
Non-EV Support
EV Support
Stuff
R3G5 R3V7 R3G10
R3V6
No Stuff
R3V6
R3G5 R3V7 R3G10
EV Support Resistor Options
Title DDR VR
Size A
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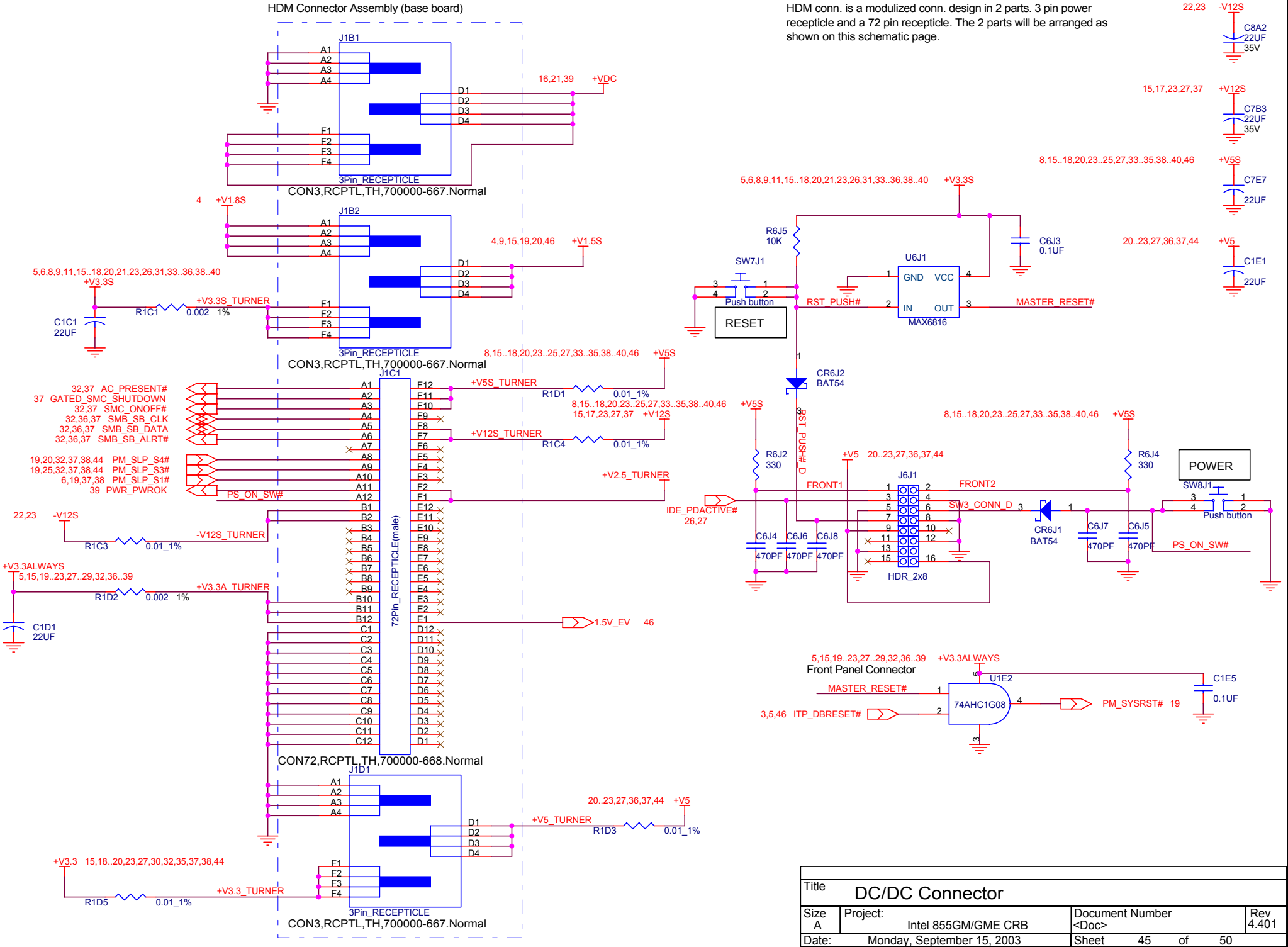
HDM Connector Assembly (base board)

HDM conn. is a modulized conn. design in 2 parts. 3 pin power recepticle and a 72 pin recepticle. The 2 parts will be arranged as shown on this schematic page.



Title	DC/DC Connector		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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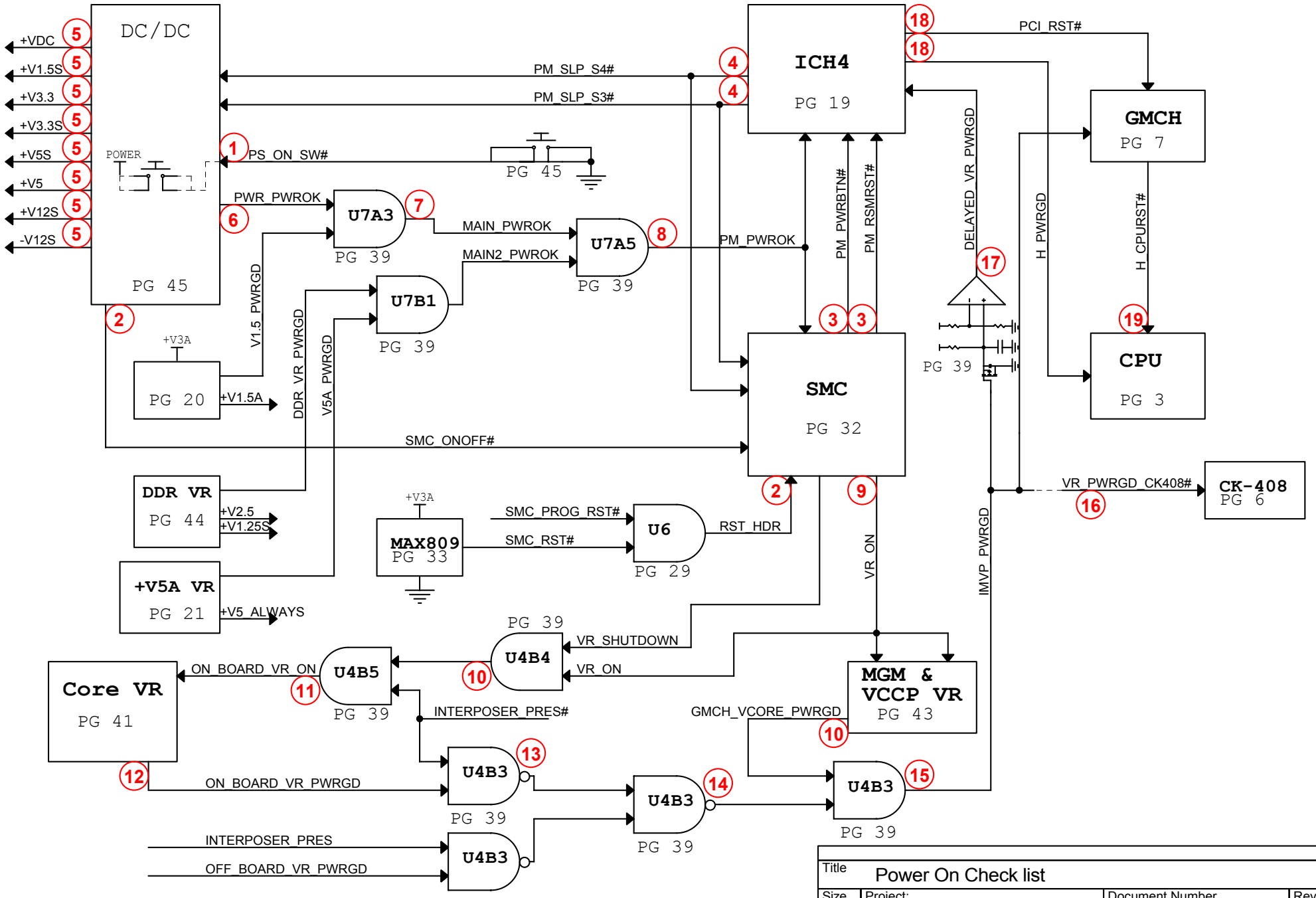
Power On Sequence



Title	Power On Check list		
Size A	Project: Intel 855GM/GME CRB	Document Number <Doc>	Rev 4.401
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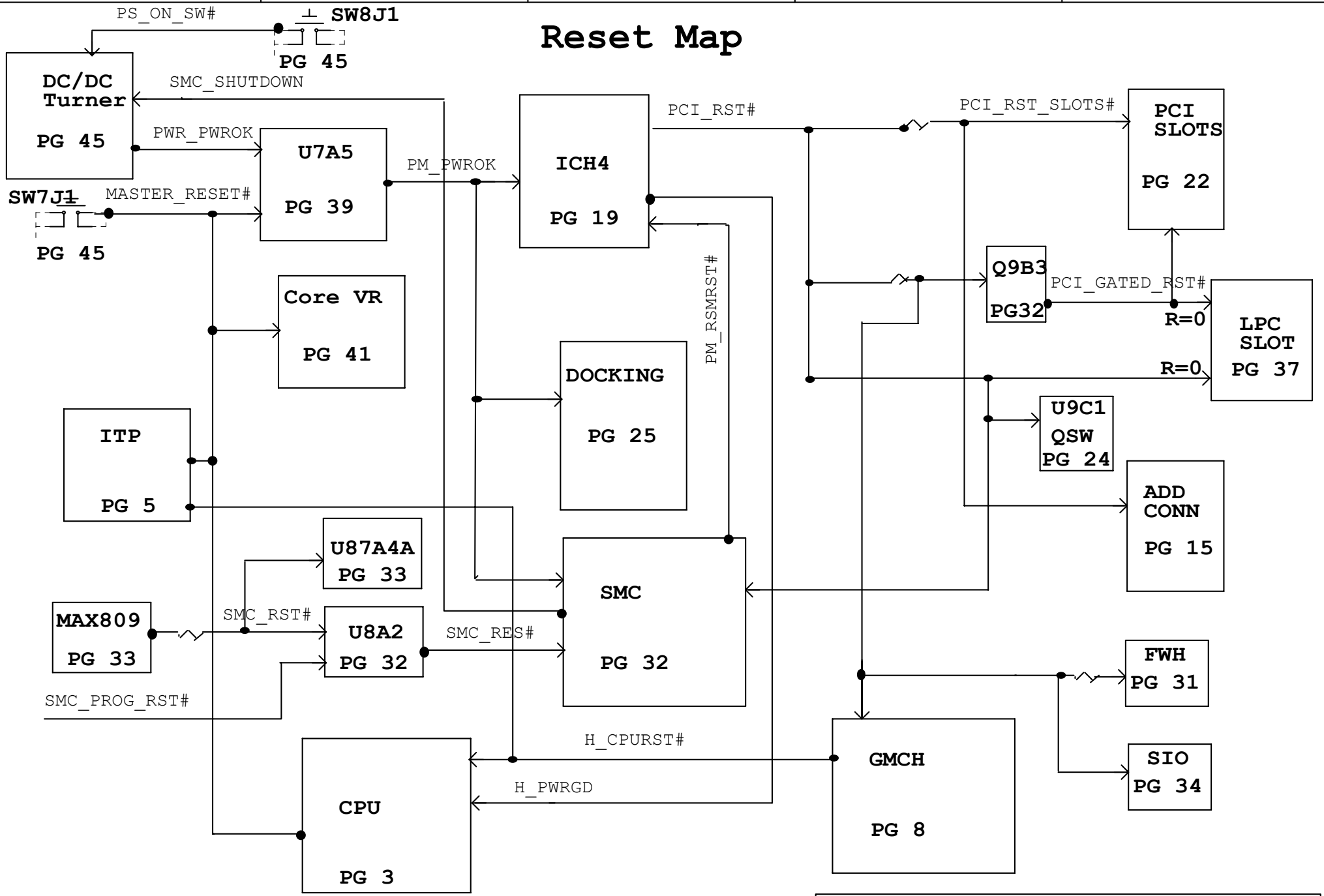
Reset Map



Title: Reset Map			
Size: A	Project: Intel 855GM/GME CRB	Document Number: <Doc>	Rev: 4.401
Date: Monday, September 15, 2003		Sheet 48 of 50	