Intel® 855PM Chipset Platform

Design Guide

For use with Intel® Pentium® M and Intel® Celeron® M Processors

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Revision History

Rev.	Order No.	Description	Date
001	252614	Initial Release	March 2003
002	252614	Updates include: Added Support for the Intel® Celeron® M processor Incorporated information from Design Guide Update 253479-002 Updated design guidelines for supporting PC2700 (333 MHz) DDR SDRAM Transition from Intel 855PM DDR 266/200 MHz Chipset to Intel 855PM DDR 200/266/333 MHz Chipset Design Guidelines System Memory SMVREF Design Update Intel® PRO/Wireless 2100 and Bluetooth* Design Requirements PSB to FSB nomenclature Change High-density Memory Support Update	January 2004
003	252614	Updates include: Added Support for the Intel Pentium® M processor on 90nm process with 2-MB L2 Cache	May 2004

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1. Introduction

This design guide organizes and provides Intel's design recommendations for systems incorporating the Intel® 855PM chipset. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The Intel 855PM chipset supports the Intel® Pentium® M Processor, Intel® Pentium® M Processor on 90nm process with 2-MB L2 Cache, and the Intel® Celeron® M Processor. Unless specifically noted, all guidelines referencing the Intel Pentium M processor and Intel Pentium M Processor on 90nm process with 2-MB L2 Cache are also applicable to the Intel Celeron M processor.

1.1. Terminology

Convention/Terminology	Definition
82801DBM ICH4-M	Refers to Intel's next generation Intel® 82801DBM Chipset I/O Controller Hub for mobile platforms. Also referred to as ICH4-M.
855PM MCH	Refers to Intel's next generation Intel 855PM Chipset Memory Controller Hub for mobile platforms. Also referred to as MCH.
855PM Chipset	Refers to the platform consists of Intel 855PM Chipset Memory Controller Hub (MCH) and Intel 82801 DBM Chipset I/O Controller Hub (ICH4-M)
Intel Pentium M Processor	Refers to the Intel Pentium M Processor and Intel Pentium M Processor on 90nm process with 2-MB L2 Cache. Intel Pentium M Processor will reference both processors unless specified
AC	Audio Codec
AGP	Accelerated Graphics Port
AGTL+	Assisted Gunning Transceiver Logic+
AMC	Audio/Modem Codec
Anti-Etch	Any plane-split, void or cutout in a VCC or GND plane is referred to as an anti-etch
ASF	Alert Standards Format
BER	Bit Error Rate
CMC	Common Mode Choke
CRB	Customer Reference Board
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge
FS	Full Speed – Refers to USB 1.1 Full Speed.
FSB	Front Side Bus – Processor to MCH interface
FWH	Firmware Hub – A non-volatile memory device used to store the system BIOS.
Future Pentium M Family Processor	Refers to Intel's future processors based on the Intel Pentium M processor micro-architecture
HS	High Speed – Refers to USB 2.0 High Speed
LPC	Low Pin Count

Convention/Terminology	Definition
LS	Low Speed – Refers to USB 1.0 Low Speed
MC	Modem Codec
MCH	Intel's next generation chipset memory controller hub for mobile platforms
PCM	Pulse Code Modulation
PLC	Platform LAN Connect
RTC	Real Time Clock
SMBus	System Management Bus – A two-wire interface through which various system components can communicate
SPD	Serial Presence Detect
S/PDIF	Sony/Phillips Digital Interface
STD	Suspend-To-Disk
STR	Suspend-To-Ram
TCO	Total Cost of Ownership
TDM	Time Division Multiplexed
TDR	Time Domain Reflectometry
UBGA	Micro Ball Grid Array
UPGA	Micro Pin Grid Array
USB	Universal Serial Bus
VRM	Voltage Regulator Module

1.2. Referenced Documents

Contact your Intel Field Representatives for the latest revisions.

Document	Location
Intel® Pentium® M Processor on 90nm process with 2-MB L2 Cache Datasheet	http://developer.intel.com
Intel® Pentium® M Processor Datasheet	http://developer.intel.com
Intel® Pentium® M Processor Specification Update	http://developer.intel.com
Intel® Celeron® M Processor Datasheet	http://developer.intel.com
Intel® 855PM Memory Controller Hub (MCH) DDR 200/266 MHz Datasheet	http://developer.intel.com
Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet	http://developer.intel.com/design/mobile/datashts/252337.htm
Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Specification Update	http://developer.intel.com/design/chipsets/specupdt
Intel® 82802AB/82802AC Firmware Hub (FWH) Datasheet	http://www.intel.com/design/chipsets/datashts/290658.htm
ITP700 Debug Port Design Guide	http://developer.intel.com/design/Xenon/guides/249679.htm
AGP Interface Specification	http://www.intel.com/technology/agp/agp_index.htm
Application Note AP-728: ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions	http://www.intel.com/design/chipsets/applnots/292276.htm
PCI Local Bus Specification	http://www.pcisig.com
JEDEC PC2100 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification	http://www.jedec.org
JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification	http://www.jedec.org/download/search/JESD79R2.pdf

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2. System Overview

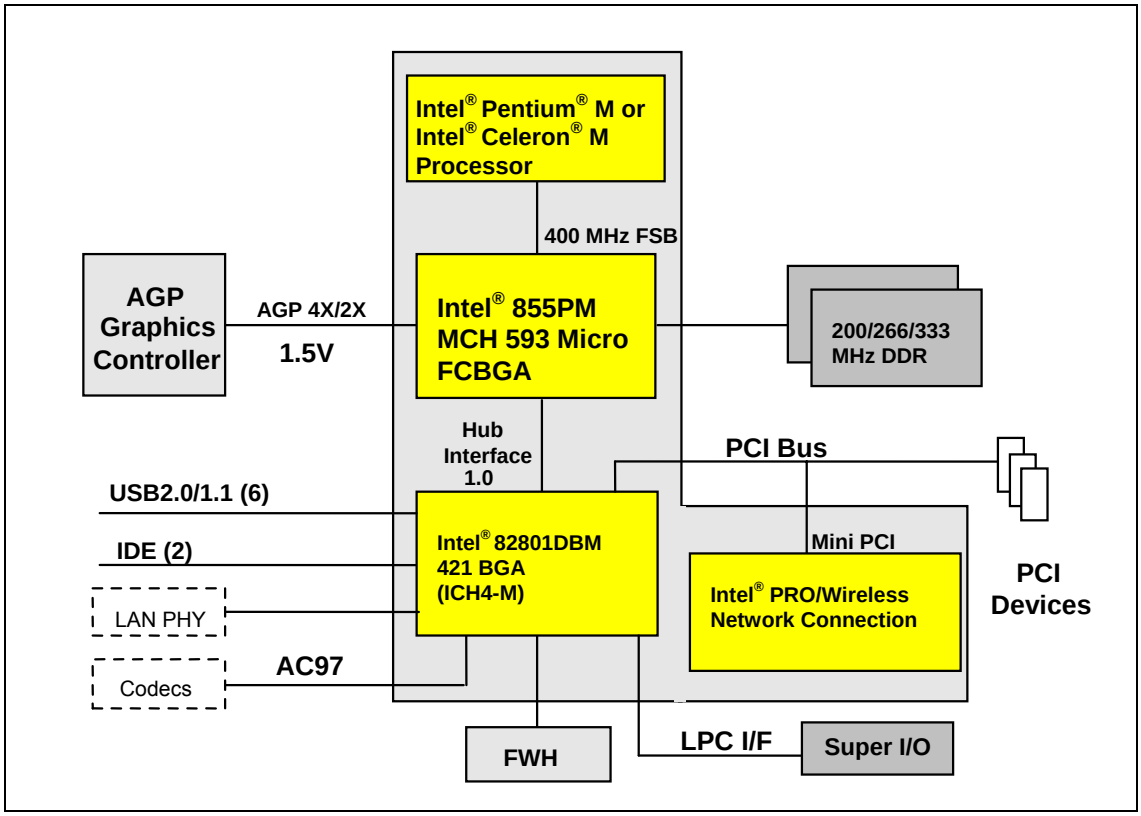
2.1. Intel® Centrino™ Mobile Technology Features

The technologies represented by the Intel Centrino brand will include an Intel Pentium M processor, Intel 855PM chipset, and 802.11 (Wi-Fi) wireless networking capability.

The integrated Wi-Fi Certified Intel PRO/Wireless Network Connection has been designed and validated to work with all of the Intel Centrino mobile technology components and is able to connect to 802.11 Wi-Fi certified access points. It also supports advanced wireless LAN security including Cisco* LEAP, 802.1X, and WEP in addition to providing software-upgradeable support for future security protocols, like WPA and full Cisco Compatible features. Finally, for comprehensive security support, the Intel PRO/Wireless Network Connection has been verified with leading VPN suppliers like Cisco, CheckPoint*, Microsoft* and Intel® NetStructure™.

Figure 1 illustrates the basic system block diagram.

Figure 1. Basic System Block Diagram



2.2. Intel® Pentium® M Processor/Intel® Celeron® M Processor

2.2.1. Architectural Features

Supports Intel Architecture with Dynamic Execution

High performance, low-power core

On-die, primary 32-kB instruction cache and 32-kB write-back data cache

On-die, second level cache with Advanced Transfer Cache Architecture

- 2-MB for Intel Pentium M Processor on 90nm process with 2-MB L2 Cache
- 1-MB for Intel Pentium M Processor
- 512-kB for Intel Celeron M Processor

Advanced Branch Prediction and Data Prefetch Logic

Streaming SIMD Extensions 2 (SSE2)

400-MHz, Source-Synchronous Front Side Bus

Advanced Power Management features including Enhanced Intel SpeedStep technology (not supported by Intel Celeron M processor)

2.2.1.1. Packaging/Power

478-pin, Micro-FCPGA and 479-ball Micro-FCBGA packages

$V_{CC\text{-}CORE}$:

- Refer to *Intel® Pentium® M Processor Datasheet*, *Intel® Pentium® M Processor on 90nm process with 2-MB L2 Cache Datasheet* and *Intel® Celeron® M Processor Datasheet for $V_{CC\text{-}CORE}$ voltages*

VCCA:

- Intel Pentium M processor and Intel Celeron M processor: 1.8 V
- Intel Pentium M processor on 90nm process with 2-MB L2 Cache: 1.8 V or 1.5 V

V_{CCP} (1.05 V)

2.3. Intel 855PM Memory Controller Hub (MCH)

2.3.1. Front Side Bus Support

Optimized for the Intel Pentium M processor / Intel Celeron M processor in 478-pin Micro-FCPGA and 479-ball Micro-FCBGA packages

AGTL+ bus driver technology with integrated GTL termination resistors (gated AGTL+ receivers for reduced power)

Supports 32-bit AGTL+ bus addressing (no support for 36-bit address extension)

Supports Uni-processor (UP) systems

400 MT/s FSB support (100 MHz)

2X Address, 4X Data

8 deep In-Order Queue

2.3.2. Integrated System Memory DRAM Controller

Supports up to two double-sided SO-DIMMs (four rows populated) with unbuffered PC1600/PC2100/2700 DDR-SDRAM (with or without ECC)

Supports 64 Mb, 128 Mb, 256 Mb, and 512 Mb technologies for x8 and x16 width devices

Maximum of 2 GB of system memory by using 512-Mb stacked memory technology devices

Supports 200 MHz, 266 MHz and 33MHz DDR devices

64-bit data interface (72-bit with ECC)

PC1600/2100 system memory interface

Supports up to 16 simultaneous open pages

Support for SO-DIMM Serial Presence Detect (SPD) scheme via SMBus interface STR power management support via self refresh mode using CKE

2.3.3. Accelerated Graphics Port (AGP) Interface

Supports AGP 2.0 data transfers

Supports a single AGP (1X/2X/4X) device (either via a connector or on the motherboard)

Only supports 1.5-V VDDQ for AGP electricals

PCI semantic (FRAME# initiated) accesses to DRAM are snooped

AGP semantic (PIPE# and SBA) traffic to DRAM is not snooped on the FSB and is therefore not coherent with the CPU caches

High priority access support

Delayed transaction support for AGP reads that cannot be serviced immediately

AGP Busy/Stop Protocol support

Support for D3 Hot and Cold Device states

AGP Clamping and Sense Amp control

2.3.4. Packaging/Power

593-pin, Micro-FCBGA package (37.5 mm x 37.5 mm)

V_{CC-MCH} (1.2 V); VCCSM (2.5 V); 1.5 V; VCCGA, VCCHA, & VCC1_8 (1.8 V); V_{CCP} (1.05 V)

2.4. Intel 82801DBM I/O Controller Hub (ICH4-M)

The Intel 82801DBM provides the I/O subsystem with access to the rest of the system:

Upstream Accelerated Hub Architecture interface for access to the MCH

PCI 2.2 interface (6 PCI Request/Grant Pairs)

Bus Master IDE controller (supports Ultra ATA 100/66/33)

USB 1.1 and USB 2.0 Host Controllers and support for USB 2.0 High Speed Debug port

I/O APIC

SMBus 2.0 Controller

FWH Interface

LPC Interface

AC'97 2.2 Interface

Alert-On-LAN*

IRQ Controller

2.4.1. Packaging/Power

421-pin, BGA package (31 mm x 31 mm)

VCC1_5 (1.5 V main logic voltage); VCCSUS1_5 (1.5 V resume logic voltage); VCCLAN1_5 (1.5 V LAN logic voltage); VCC3_3 (3.3 V main I/O voltage); VCCSUS3_3 (3.3 V resume I/O voltage); VCCLAN3_3 (3.3 V LAN I/O voltage); V5REF (5 V); V5REF_SUS (5 V); VCCRTC; VCCHI (1.8 V); V_CPU_IO/V_{CCP} (1.05 V)

2.5. Intel PRO/Wireless Network Connection

Ability to connect to 802.11 Wi-Fi Certified networks

Industry standard and extended wireless security support (WEP, 802.1X and Cisco* LEAP)

Intel® PROSet software with advanced profile management support, allows multiple setup profiles to connect to different WLAN networks

Intel PROSet software with automatic WLAN switching support enables automatic switching between wired & wireless LAN connections

Intel PROSet software supports Cisco, Check Point, Microsoft and Intel VPN connections†

Intel PROSet software with ad hoc connection wizard support provides a simple interface for setting up ad hoc networks

Intel Wireless Coexistence System support enables reduced interference between Intel PRO/Wireless & certain Bluetooth* devices

Per-packet antenna selection enables optimized WLAN performance

Intel Intelligent Scanning technology, reduces power by controlling the frequency of scanning for access points

Power saving capability with five different power settings allows users to trade off performance and battery life.

2.5.1. Packaging and Power

Mini-PCI Type 3B: (59.45 mm x 44.45 mm x 5mm)

Mini-PCI Type 3A: (59.45 mm x 50.8 mm x 5 mm)

3.3V

2.6. Firmware Hub (FWH)

An integrated hardware Random Number Generator (RNG)

Register-based locking

Hardware-based locking

Five GPIs

2.6.1. Packaging/Power

32-pin TSOP/PLCC

3.3-V core and 3.3 V/12 V for fast programming

3. General Design Considerations

This section documents motherboard layout and routing guidelines for Intel 855PM chipset platforms. It does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, Intel recommends that critical signals be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e. 55 ± 15%) is the "nominal" trace impedance for a 5-mil wide external trace and a 4-mil wide internal trace. However, some stack-ups may lead to narrower or wider traces on internal or external layers in order to meet the 55- impedance target. Note the trace impedance target assumes that the trace is not subjected to the EMI created by changing current in neighboring traces. It is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces when calculating flight times. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. Also, all high-speed, impedance controlled signals (e.g. FSB signals) should have continuous GND referenced planes and cannot be routed over or under power/GND plane splits.

3.1. Nominal Board Stack-Up

Systems incorporating the Intel 855PM chipsets requires a board stack-up yielding a target impedance of 55 ± 15%.

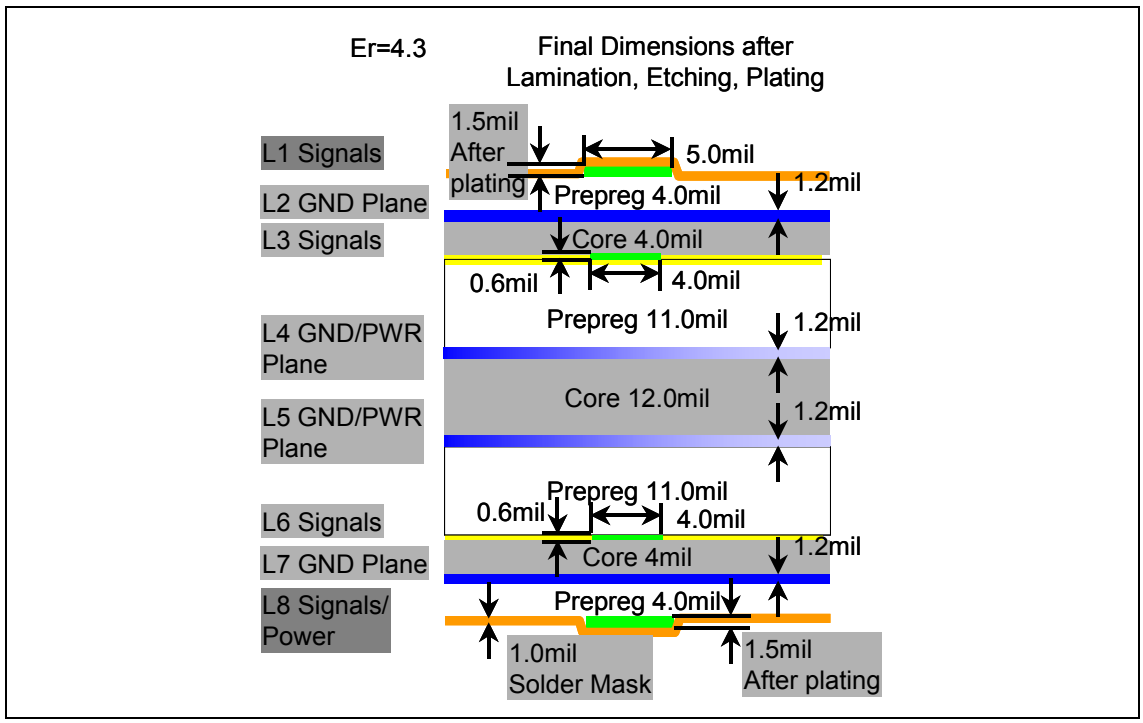
An example of an 8-layer board stack-up is shown in Figure 2. The left side of the figure illustrates the starting dimensions of the metal and dielectric material thickness as well as drawn trace width dimensions prior to lamination, conductor plating, and etching. After the motherboard materials are laminated, conductors plated, and etched, somewhat different dimensions result. Dielectric materials become thinner, under/over etching of conductors alters their trace width, and conductor plating makes them thicker. It is important to note that for the purpose of extracting electrical models from transmission line properties, the final dimensions of signals after lamination, plating, and etching should be used.

The stack-up uses 1.2-mil (1 oz) copper on power planes to reduce I*R drops and 0.6-mil copper thickness on the signal layers: primary side layer (L1), Layer 3 (L3), Layer 6 (L6), and secondary side layer (L8). After plating, the external layers become 1.2 to 2 mils thick.

To meet the nominal 55- characteristic impedance primary and secondary side layer micro-strip lines are drawn at 5-mil trace width but end up with a 5.5-mil final trace width after etching. For the same reason, the 5-mil thick prepreg between the primary side layer and Layer 2 starts at 5 mils but becomes 4 mils after lamination. This situation and result also applies to Layer 7 and the secondary side layer.

To ensure impedance control of 55 , the primary and secondary side layer micro-strip lines should reference solid ground planes on Layer 2 and Layer 7, respectively.

Figure 2. Recommended Board Stack-Up Dimensions



Internal signal traces on Layer 3 and Layer 6 are unbalanced strip-lines. To meet the nominal 55- characteristic impedance for these traces, they reference a solid ground plane on Layer 2 and Layer 7. Since the coupling to Layer 4 and Layer 5 is still significant, (especially true when thinner stack-ups use balanced strip-lines on internal layers) these layers are converted to ground floods in the areas of the motherboard where the high-speed interfaces like the FSB or DDR system memory are routed. In the remaining sections of the motherboard layout the Layer 4 and Layer 5 layers are used for power delivery.

For 55- characteristic impedance Layer 3 (Layer 6), strip-lines have a 4-mil final trace width and are separated by a core dielectric thickness of 4 mils after lamination from the Layer 2 (Layer 7) ground plane and 11-mil thickness prepreg after lamination to separate it from Layer 4 (Layer 5). The starting thickness of these core and prepreg dielectric layers before lamination is 5 mils and 12 mils, respectively.

The secondary side layer is also used for power delivery in many cases since it benefits from the thick copper plating of the external layer plating as well as referencing the close (4-mil prepreg thickness) Layer 7 ground plane. The benefit of such a stack-up is low inductance power delivery.

OEMs may choose to use different stack-ups (number of layers, thickness, trace width, etc.) from the one example outlined in Figure 2. However, the following key elements should be observed:

1. Final post lamination, post etching, and post plating dimensions should be used for electrical model extractions.
2. Power plane layers should be 1 oz thick and signal layers should be ½ oz thick.
3. External layers become 1 – 1.5 oz (1.2 – 2 mils) thick after plating

4. All high-speed signals should reference solid ground planes through the length of their routing and should not cross plane splits. To guarantee this, both planes surrounding strip-lines should be GND.
5. Intel recommends that high-speed signal routing be done on internal, strip-line layers.
6. High-speed signals transitioning between layers next to the component, signal pins should be accounted for by the GND stitching vias that would stitch all the GND plane layers in that area of the motherboard. Due to the arrangement of the Intel® Pentium® M Processor / Intel® Celeron® M Processor and Intel 855PM MCH pin-maps, GND vias placed near all GND lands will also be very close to high-speed signals that may be transitioning to an internal layer. Thus, no additional ground stitching vias (besides the GND pin vias) are required in the immediate vicinity of the processor and MCH packages to accompany the signal transitions from the component side into an internal layer.
7. High-speed routing on external layers should be minimized in order to avoid EMI. Routing on external layers also introduces different delays compared to internal layers, making it extremely difficult to do length matching if some routing is done on both internal and external layers.

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4. FSB Design Guidelines

The following layout guidelines support designs using the Intel Pentium M processor / Intel Celeron M processor and the Intel 855PM MCH chipset. Due to on-die Rtt resistors on both the processor and the chipset, additional resistors do not need to be placed on the motherboard for most FSB signals. A simple point-to-point interconnect topology is used in these cases.

4.1. FSB Design Recommendations

For proper operation of the processor and the chipset, the system designer must meet the timing and voltage specification of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions, which may be different than an OEM's system design. The most accurate way to understand the signal integrity and timing of the FSB in your platform is by performing a comprehensive simulation analysis. It is possible that adjustments to trace impedance, line length, termination impedance, board stack-up, and other parameters can be made that improve system performance.

Refer to the latest *Intel® Pentium® M Processor Datasheet*, *Intel® Pentium® M Processor on 90nm process with 2-MB L2 Cache Datasheet* or *Intel® Celeron® M Processor Datasheet* for a FSB signal list, signal types, and definitions. Below are the design recommendations for the data, address, and strobes. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate. The guidelines are derived from empirical testing with Intel 855PM chipset MCH package models.

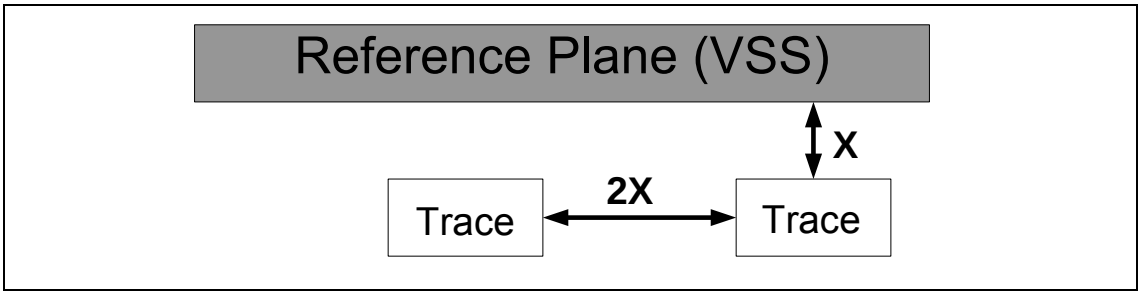
4.1.1. Recommended Stack-up Routing and Spacing Assumptions

The following section describes in more detail, the terminology and definitions used for different routing and stack-up assumptions that apply to the recommended motherboard stack-up show in Figure 2.

4.1.1.1. Trace Space to Trace – Reference Plane Separation Ratio

Figure 3 illustrates the recommended relationship between the edge-to-edge trace spacing (2X) versus the trace to reference plane separation (X). An edge-to-edge trace spacing (2X) to trace – reference plane separation (X) ratio of 2 to 1 ensures a low crosstalk coefficient. All the effects of crosstalk are difficult to simulate. The timing and layout guidelines for the Intel Pentium M/Intel Celeron M processor have been created with the assumption of a 2:1 trace spacing to trace – reference plane ratio. A smaller ratio would have an unpredictable impact due to crosstalk.

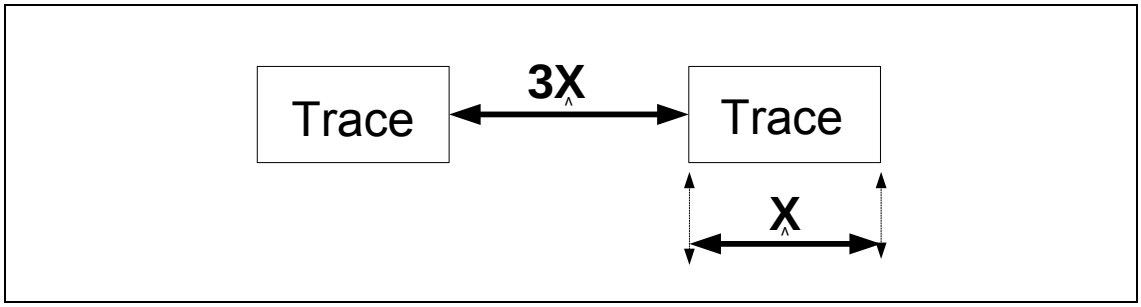
Figure 3. Trace Spacing vs. Trace to Reference Plane Example



4.1.1.2. Trace Space to Trace Width Ratio

Figure 4 illustrates the recommended relationship between the edge-to-edge trace spacing versus trace width ratio for the best signal quality results. In general, a 3:1 trace space to trace width ratio is preferred and highly recommended. In case of routing difficulties on the motherboard, using a 2:1 ratio would be acceptable **only** if additional simulations conclude that it is possible, and this may include some changes to the stack-up or routing assumptions. In the case of the FSB signals, routing recommendations for a 2:1 trace spacing to trace width ratio can be found in Topology 2 for the source synchronous signals (see Table 5).

Figure 4. Trace Spacing vs. Trace Width Example



4.1.1.3. Recommended Stack-up Calculated Coupling Model

The importance of maintaining an adequate trace space to trace width ratio is to achieve the best signal quality possible given routing constraints. The simulations performed that resulted in the recommended 3:1 trace space to trace width ratio is to keep the coupling between adjacent traces below a maximum value. For the recommended stack-up, the constants shown in Figure 5 are assumed to be constant for a **typical** stack-up. This means the mutual to self-coupling relationship given below does not take into account the normal tolerances that are allowed for in the recommended board stack-up's parameters. For the recommended stack-up shown in Figure 2, the calculated capacitive coupling maximum value is represented by the following relationship:

$$(C_{MUTUAL} / C_{SELF}) \times 100 = 8.15\%$$

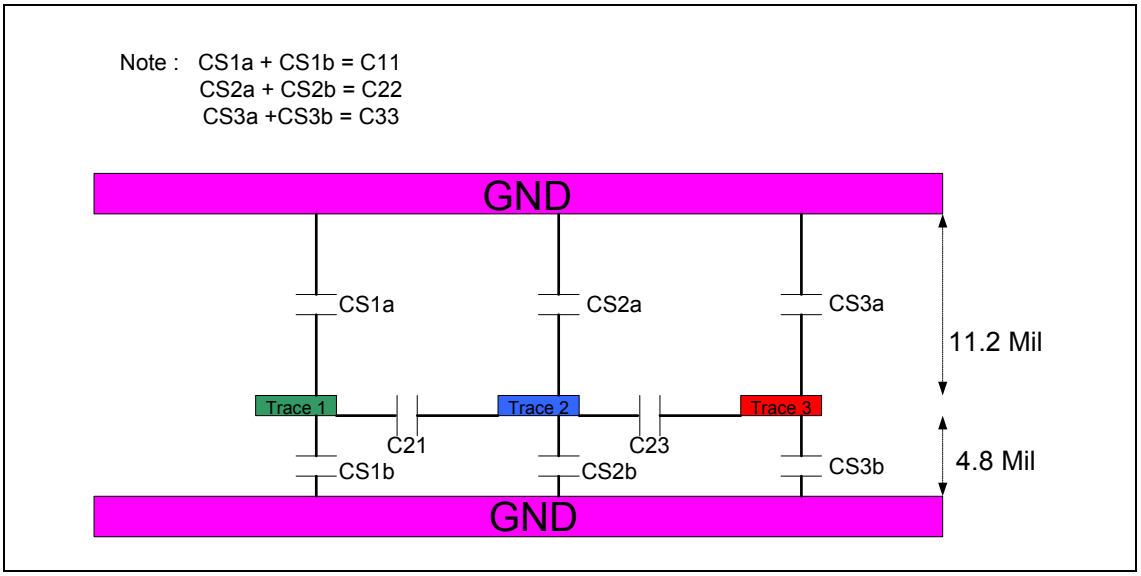
As shown in Figure 5, the coupling values are calculated based on a three-line model, represented by Trace 1, Trace 2, and Trace 3. Based on the capacitive coupling model shown, the aforementioned parameters are:

$$C_{MUTUAL} = C21 + C23$$

C_{SELF} = C22 (Trace 2, i.e. CS2a + CS2b)

If a stack-up that is employed does not adhere to the recommended stack-up, then a new extraction must be made for the stack-up using a 2D field solver program. According to the 2D field solver results, new coupling calculations must be performed to ensure that the coupling results are less than the aforementioned capacitive coupling maximum value of 8.15%. If the coupling results are greater than the maximum value, then additional system level simulations must be performed to avoid any signal quality issues due to crosstalk effects.

Figure 5. Recommended Stack-up Capacitive Coupling Model



4.1.1.4. Signal Propagation Time to Distance Relationship and Assumptions

Due to the high frequency nature of some interfaces and signals, length matching may or may not exist as part of the routing requirements for a given interface. In general, the tolerances that specific signals in a bus must be routed to will be stated as a length measured in mils or inches and is specific to the recommended motherboard stack-up (see Figure 2). However, some length matching tolerances for signals listed in this design guide may be stated as a measurement of time. In such cases, the correlation of the period of time to an actual length value will depend on board stack-up.

Based on the recommended stack-up, the signal propagation time to distance relationship, for the purpose of this design guide, is as follows:

Strip-line (internal layer) Routing: 180 ps for 1.0 inch

Micro-strip (external layer) Routing: 162 ps for 1.0 inch

For example, a length-matching requirement of ± 50 ps for routing on a strip-line (internal) layer would correlate to a trace length whose tolerance is within ± 278 mils of an associated trace. The signal propagation time to distance relationship listed above is based on a single transmission line model incorporating a **typical** stack-up. Thus, no other signals or traces are accounted for in such a model and there is an assumption of zero coupling with other traces. Also, the recommended stack-up's parameter tolerances are not taken into account in the "typical" stack-up assumptions. Finally, in cases that need to account for worst-case stack-up parameters and for even or odd mode coupling, new extractions from the stack-up model must be done to provide an accurate signal propagation time to distance relationship.

4.1.2. Common Clock Signals

All common clock signals use an AGTL+ bus driver technology with on die integrated GTL termination resistors connected in a point-to-point, Zo = 55 , controlled impedance topology between the processor and the Intel 855PM chipset MCH. No external termination is needed on these signals. These signals operate at the FSB frequency of 100 MHz.

Common clock signals should be routed on an internal or external layer while referencing solid ground planes. Common clock signal routing on internal layers implemented with complete reference to ground planes both above and below the signal layer is recommended. Based on current simulation results, routing on internal layers allows for a minimum pin-to-pin motherboard length of 1.0 inch and a maximum of 6.5 inches. Routing on external layers allows for a pin-to-pin motherboard length of 1.0 inch and a maximum of 6.5 inches. Trace length matching for the common clock signals is not required. Intel recommends routing these signals on the same internal or external layer for the entire length of the bus. If routing constraints require routing of these signals with a transition to a different layer, a minimum of one ground stitching via for every two signals should be placed within 100 mils of the signal transition vias.

Routing of the common clock signals should use a minimum of 1:2 trace spacing. This implies a 4-mil trace width with a minimum of 8-mil spacing (i.e. 12-mil minimum pitch) for routing on internal layers. For external layers, route using a 5-mil trace width and a 10-mil minimum spacing (i.e. 15-mil pitch). Practical cases of escape routing under the MCH or the processor package outline and near by vicinity may not allow the implementation of 1:2 trace spacing requirements. Although every attempt should be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the MCH and the processor package outlines and up to 200 – 300 mils outside the package outline.

Table 1 summarizes the list of common clock and key routing requirements. RESET# (CPURST# of MCH) is also a common clock signal but requires a special treatment for the case where an ITP700FLEX debug port is used. See Section 4.1.5 for further details. Figure 6 and Figure 7 illustrate an example of escape routing from the processor and the Intel 855PM chipset MCH package vicinity for the common clock signals. To allow for flat routing, DEFER#, DRDY#, HIT#, HITM#, TRDY#, and BNR# would have to have minimal routing on the primary side in the vicinity of the MCH package and then the rest of the routing continues on internal layer 6. The ground vias of the MCH pins provide the needed ground stitching vias for a layer transition for these signals. The remaining signals have standard dog bone (a land for a BGA ball followed by a short trace to a via with a 25-mil offset in the X and Y directions) vias on the primary side and continue to the processor in a simple point-to-point connection. The processor only has straightforward dog bones on the primary side for this group of signals. Figure 8 shows a global routing summary of these common clock signals as a simple point-to-point connection on Layer 6 between the processor and the Intel 855PM MCH.

Table 1. FSB Common Clock Signal Internal Layer Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance ( )	Width & spacing (mils)
CPU	MCH		Min (inches)	Max (inches)		
ADS#	ADS#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
BNR#	BNR#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
BPRI#	BPRI#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
BR0#	BREQ0#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
DBSY#	DBSY#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
DEFER#	DEFER#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
DPWR#	DPWR#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
DRDY#	DRDY#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
HIT#	HIT#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
HITM#	HITM#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
LOCK#	HLOCK#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
RS[2:0]#	RS[2:0]#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
TRDY#	HTRDY#	Strip-line	1.0	6.5	55 ± 15%	4 & 8
RESET#[1]	CPURST#	Strip-line	1.0	6.5	55 ± 15%	4 & 8

NOTE: For topologies where an ITP700FLEX debug port is implemented, see Section 4.1.5 for RESET# (CPURST#) implementation details.

Table 2. FSB Common Clock Signal External Layer Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance ( )	Width & spacing (mils)
CPU	MCH		Min (inches)	Max (inches)		
ADS#	ADS#	Micro-strip	1.0	6.5	55 ±15%	5 & 10
BNR#	BNR#	Micro-strip	1.0	6.5	55 ±15%	5 & 10
BPRI#	BPRI#	Micro-strip	1.0	6.5	55 ± 15%	5 & 10
BR0#	BREQ0#	Micro-strip	1.0	6.5	55 ± 15%	5 & 10
DBSY#	DBSY#	Micro-strip	1.0	6.5	55 ± 15%	5 & 10
DEFER#	DEFER#	Micro-strip	1.0	6.5	55 ± 15%	5 & 10
DPWR#	DPWR#	Micro-strip	1.0	6.5	55 ± 15%	5 & 10
DRDY#	DRDY#	Micro-strip	1.0	6.5	55 ±15%	5 & 10
HIT#	HIT#	Micro-strip	1.0	6.5	55 ±15%	5 & 10
HITM#	HITM#	Micro-strip	1.0	6.5	55 ±15%	5 & 10
LOCK#	HLOCK#	Micro-strip	1.0	6.5	55 ± 15%	5 & 10
RS[2:0]#	RS[2:0]#	Micro-strip	1.0	6.5	55 ± 15%	5 & 10
TRDY#	HTRDY#	Micro-strip	1.0	6.5	55 ± 15%	5 & 10
RESET#[1]	CPURST#	Micro-strip	1.0	6.5	55 ± 15%	5 & 10

NOTE: For topologies where an ITP700FLEX debug port is implemented, see Section 4.1.5 for RESET# (CPURST#) implementation details.

Figure 6. Common Clock Signals Example – Intel 855PM MCH Escape Routing

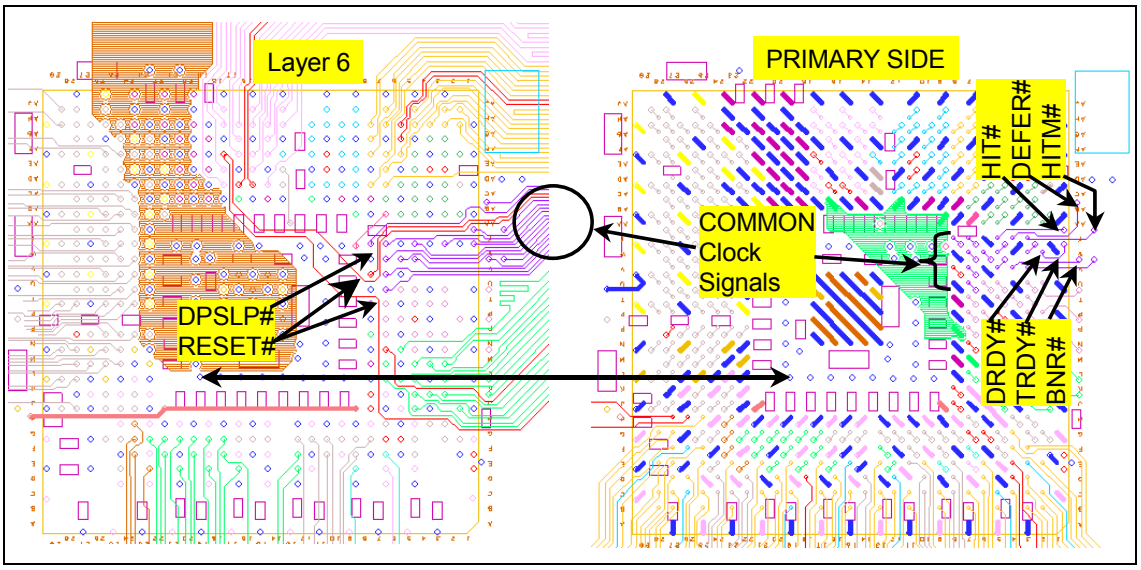


Figure 7. Common Clock Signals Example – Processor Escape Routing

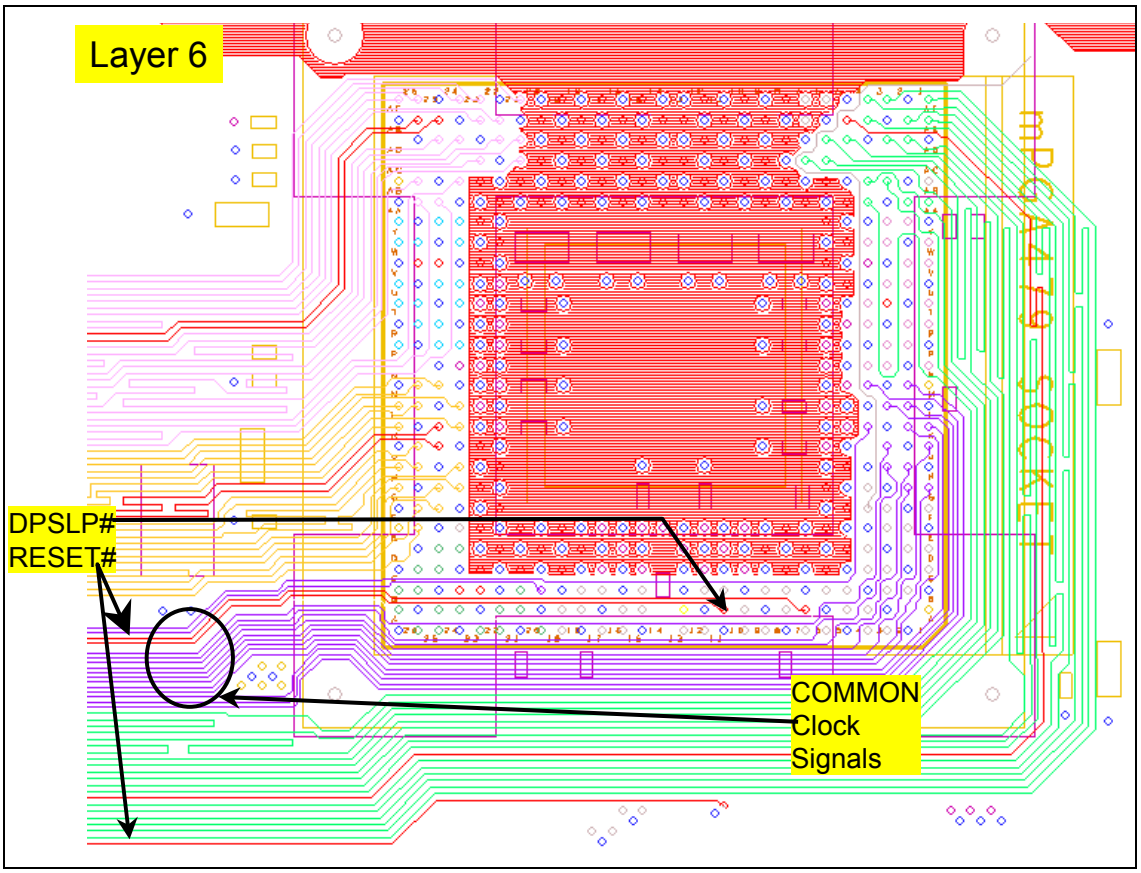
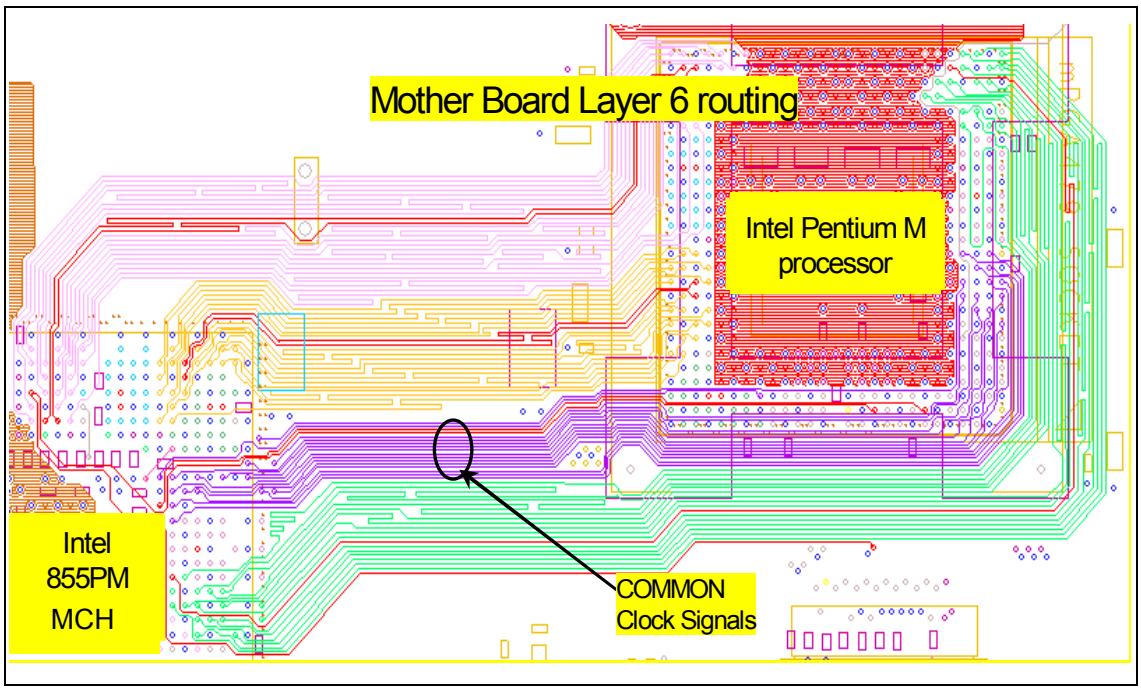


Figure 8. Common Clock Signals Example – Processor to Intel 855PM MCH Layer 6 Routing



4.1.3. Source Synchronous Signals

All source synchronous signals use an AGTL+ bus driver technology with on-die GTL termination resistors connected in a point-to-point, Zo = 55 controlled impedance topology between the Intel Pentium M/Intel Celeron M processor and the Intel 855PM MCH. No external termination is needed on these signals. Source synchronous FSB address signals operate at a double pumped rate of 200 MHz while the source synchronous FSB data signals operate at a quad pumped rate of 400 MHz. High-speed operation of the source synchronous signals requires careful attention to their routing considerations. The following guidelines should be strictly adhered to, to guarantee robust high-frequency operation of these signals.

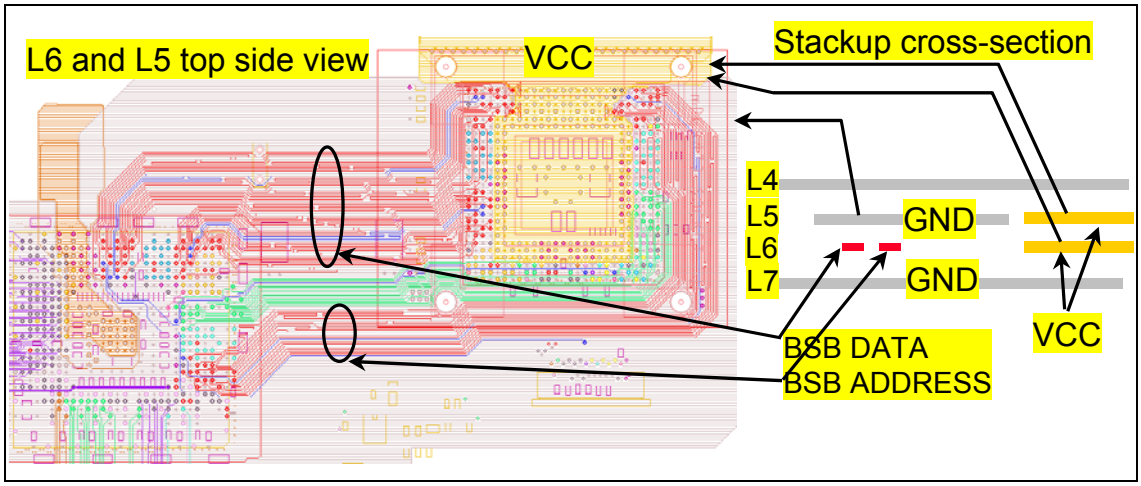
4.1.3.1. Source Synchronous General Routing Guidelines

Source synchronous data and address signals and their associated strobes are partitioned into groups of signals. Flight time skew minimization within the same group of source synchronous signals is a key parameter that allows their high frequency (400 MHz) operation. All the source synchronous signals that belong to **the same group** should be routed on **the same internal layer** for the entire length of the bus. It is acceptable to split different groups of source synchronous signals between different motherboard layers as long as all the signals that belong to that group are kept on the same layer. Grouping of FSB source synchronous signals is summarized in Table 3 and Table 6. This practice results in a significant reduction of the flight time skew since the dielectric thickness, line width, and velocity of the signals will be uniform across a single layer of the stack-up. There is no guarantee of a relationship of dielectric thickness, line width, and velocity between layers.

The source synchronous signals should be routed as a strip-line on an internal layer with complete reference to ground planes both above and below the signal layer. Routing with references to split planes or power planes other than ground is not allowed. For the recommended stack-up example as shown in Figure 2, source synchronous FSB signals are routed on Layer 3 and Layer 6. Layer 2 and Layer 7 are solid grounds across the entire motherboard. However, this is not sufficient since significant coupling exists between signal Layer 3 and power plane Layer 2 as well as signal Layer 6 and power plane Layer 5. To guarantee complete ground referencing, Layer 4 and Layer 5 are converted to ground plane floods in the areas where the source synchronous FSB signals are routed. In addition all the ground plane areas are stitched with ground vias in the vicinity of the processor and Intel 855PM MCH package outlines with the vias of the ground pins of the processor and MCH pin-map.

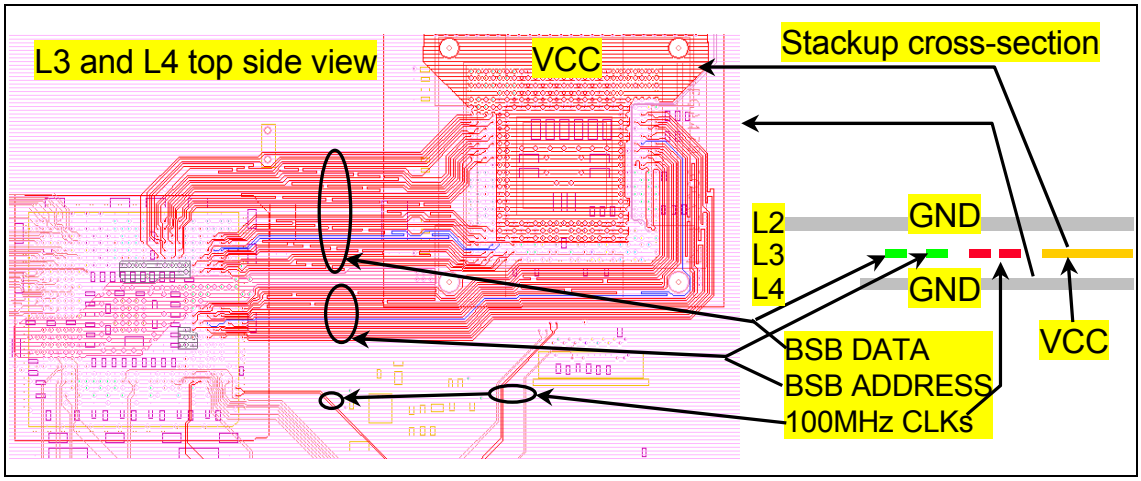
Figure 9 illustrates a motherboard layout and a cross-sectional view of the recommended stack-up of the FSB source synchronous DATA and ADDRESS signals referencing ground planes on both Layer 7 and Layer 5. Notice that in the socket cavity of the processor Layer 5 and Layer 6 layers is used for VCC core power delivery. However, outside the socket cavity Layer 6 signals are routed on top of a solid Layer 7 ground plane and also Layer 5 is converted to a ground flood under the shadow of the FSB signals routing between the processor and MCH. Stitching of all the GND planes is provided by the ground vias in the pin-map of the processor and MCH.

Figure 9. Layer 6 FSB Source Synchronous Signals GND Referencing to Layer 5 and Layer 7 Ground Planes



In a similar way, Figure 10 illustrates a recommended layout and stack-up example of how another group of FSB source synchronous DATA and ADDRESS signals can reference ground planes on both Layer 2 and Layer 4. Note that in the socket cavity of the processor, Layer 3 is used for VCC core power delivery to reduce the I*R drop. However, outside of the socket cavity Layer 3 signals are routed below a solid Layer 2 ground plane and also Layer 4 is converted to a ground flood under the shadow of the FSB signals routing between the processor and MCH.

Figure 10. Layer 3 FSB Source Synchronous Signals GND Referencing to Layer 2 and Layer 4 Ground Planes



Skew minimization requires pin-to-pin trace length matching of the FSB source synchronous signals that belong to the same group including the strobe signals of that group. Trace length matching of the processor and MCH packages does not need to be accounted for in the motherboard routing since both packages have the source synchronous signals and the strobes length matched within the group inside the package routing.

Current simulation results provide routing guidelines using 1:3 spacing (Topology 1) for the FSB source synchronous signals. This implies 4-mil trace width with a minimum of 12-mil spacing (i.e. 16-mil minimum pitch). Practical cases of escape routing under the MCH or processor package outline and near by vicinity may not even allow the implementation of 1:2 trace spacing requirements. Although every attempt should be made to maximize the signal spacing in these areas, it is allowable to have 1:1 trace spacing underneath the MCH and the processor package outlines and up to 200 – 300 mils outside the package outline.

Routing guidelines using 1:2 spacing is available and can be used wherever 1:3 spacing cannot be implemented by using Topology 2. The benefits of additional spacing include increased signal quality and voltage margining. The trace routing and length matching requirements are provided in the following sections.

4.1.3.2. Source Synchronous – Data

Robust operation of the 400-MHz, source synchronous data signals require tight skew control. For this reason, these signals are split into matched groups as outlined in Table 3. All the signals within the same group should be kept on the same layer of motherboard routing and should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. Because the processor and Intel 855PM MCH packages provide package trace equalization for signals within each data group, all signals should be routed on the system board to meet the pin-to-pin matching requirement of ± 100 mils. The two complementary strobe signals associated with each group should be length matched to each other within ± 25 mils and tuned to the average length of the data signals of their associated group. This will optimize setup/hold time margin.

Table 3. FSB Data Source Synchronous Signal Trace Length Mismatch Mapping

CPU Signal Name	Signal Matching	Strobes associated With the Group	Strobe Matching	Notes
D[15:0]#, DINV0#	± 100 mils	DSTBP0#, DSTBN0#	± 25 mils	1
D[31:16]#, DINV1#	± 100 mils	DSTBP1#, DSTBN1#	± 25 mils	1
D[47:32]#, DINV2#	± 100 mils	DSTBP2#, DSTBN2#	± 25 mils	1
D[63:48]#, DINV3#	± 100 mils	DSTBP3#, DSTBN3#	± 25 mils	1

NOTE: Strobes of the same group should be trace length matched to each other within ±25 mil and to the average length of their associated Data signal group.

Table 4 lists the source synchronous data signal general routing requirements. Due to the 400-MHz, high-frequency operation of the data signals, 1:3 spacing is strongly advised and should be limited to a pin-to-pin trace length minimum of 0.5 inches and maximum of 5.5 inches.

Table 4. FSB Source Synchronous Data Signal Routing Guidelines Topology 1

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance ( )	Width & spacing (mils)
CPU	MCH		Min (inches)	Max (inches)		
DINV[3:0]#	DBI[3:0]#	Strip-line	0.5	5.5	55 ± 15%	4 & 12
D[63:0]#	HD[63:0]#	Strip-line	0.5	5.5	55 ±15%	4 & 12
DSTBN[3:0]#	HDSTBN[3:0]#	Strip-line	0.5	5.5	55 ± 15%	4 & 12
DSTBP[3:0]#	HDSTBP[3:0]#	Strip-line	0.5	5.5	55 ±15%	4 & 12

If routing space constraints do not allow 1:3 spacing of the source synchronous data signals, Table 5 lists alternative routing requirements for some of these signals if 1:2 spacing is used. In both topologies, the pin-to-pin trace length should be limited to a minimum of 0.5 inches and a maximum of 5.5 inches. The adherence to tighter characteristic trace impedance tolerances for the alternative routing requirements allows the closer spacing of the data and bus inversion signals to be achieved. The use of ± 10% tolerance for the trace impedance in the alternative topology allows designs to maintain the same overall minimum and maximum trace lengths as the primary topology that utilizes a looser ± 15% tolerance. Although the data and bus inversion signals for the FSB can be routed with 1:2 spacing when using the tighter trace impedance tolerance, the data strobes **must** maintain 1:3 spacing. In this case, the processor's DSTBN[3:0]# and DSTBP[3:0]# strobe signals must be routed to the MCH's HDSTBN[3:0]# and HDSTBP[3:0]# strobe signals with 1:3 spacing from all signals even if ± 10% trace impedance tolerance is used.

Table 5. FSB Source Synchronous Data Signal Routing Guidelines Topology 2

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance ( )	Width & spacing (mils)
CPU	MCH		Min (inches)	Max (inches)		
DINV[3:0]#	DBI[3:0]#	Strip-line	0.5	5.5	55 ± 10%	4 & 8
D[63:0]#	HD[63:0]#	Strip-line	0.5	5.5	55 ± 10%	4 & 8
DSTBN[3:0]#	HDSTBN[3:0]#	Strip-line	0.5	5.5	55 ±10%	4 & 12
DSTBP[3:0]#	HDSTBP[3:0]#	Strip-line	0.5	5.5	55 ± 10%	4 & 12

4.1.3.3. Source Synchronous – Address

Source synchronous address signals operate at 200 MHz. Thus, their routing requirements are very similar to the data signals. Refer to Sections 4.1.3.1 and 4.1.3.2 for further details. Table 6 details the partition of the address signals into matched length groups. Due to the lower operating frequency of the address signals, pin-to-pin length matching is relaxed to ± 200 mils. Each group is associated with only one strobe signal. To maximize setup/hold time margin, the address strobes should be trace length matched to the average trace length of the address signals of their associated group. In addition, each address signal should be trace length matched within ± 200 mils of its associated strobe signal.

Table 6. FSB Address Source Synchronous Signal Trace Length Mismatch Mapping

CPU Signal Name	Signal Matching	Strobe Associated With the Group	Strobe to Assoc. Address Signal Matching	Notes
REQ[4:0]#, A[16:3]#	± 200 mils	ADSTB0#	± 200 mils	1, 2
A[31:17]#	± 200 mils	ADSTB1#	± 200 mils	1, 2

NOTES:
1. ADSTB[1:0]# should be trace length matched to the average length of their associated Address signals group.
2. Each Address signal should be trace length matched to its associated Address Strobe within ± 200 mils.

Table 7 lists the source synchronous address signals general routing requirements. Due to the 200-MHz, high frequency operation of the address signals, 1:3 spacing is strongly advised and trace lengths should be limited to a pin-to-pin trace length minimum of 0.5 inches and a maximum of 6.5 inches. The routing guidelines listed in Table 7 allows for 1:2 spacing for the address signals given a 55 ± 15% characteristic trace impedance. But if space permits, 1:3 spacing should be applied to these signals. For the address strobes, 1:3 spacing is required irrespective of the tolerance of the trace impedance. This is a change from previous recommendations where 1:2 spacing was acceptable for ± 15% impedance tolerances.

Table 7. FSB Source Synchronous Address Signal Routing Guidelines

Signal Names		Transmission Line Type	Total Trace Length		Nominal Impedance ( )	Width & Spacing (mils)
CPU	MCH		Min (inches)	Max (inches)		
A[31:3]#	HA[31:3]#	Strip-line	0.5	6.5	55 ± 15%	4 & 8
REQ[4:0]#	HREQ[4:0]#	Strip-line	0.5	6.5	55 ± 15%	4 & 8
ADSTB#[1:0]	HADSTB[1:0]#	Strip-line	0.5	6.5	55 ± 15%	4 & 12

4.1.3.4. Source Synchronous Signals Recommended Layout Example

Figure 11 illustrates escape routing of the FSB source synchronous signals in the vicinity of the Intel 855PM MCH package. The primary side has minimum length dog bones from the BGA lands that transition with vias into internal routing Layer 3 and Layer 6. Note the change in orientation of the dog bone “dipoles” as it changes from place to place to allow smooth escape routing on Layer 3 and Layer 6 later on in between the GND vias. The signals are split about half and half between Layer 3 and Layer 6. For address signals, the first group containing REQ[4:0]#, A[16:3]#, and ADSTB[0]# are routed on Layer 3. The second group of address signals containing A[31:17]# and ADSTB[1]# is routed on Layer 6. Similarly, D[15:0]#, DINV[0]#, DSTBN[0]#, DSTBP[0]# and D[47:32]#, DINV[2]#, DSTBN[2]#, DSTBP[2]# are routed on Layer 3. The remaining two data signals groups with associated strobe and DINV signals are routed on Layer 6. A vertical corridor with no routing on Layer 6 to the left of the D[63:48]# group is used to feed the 1.2-V core power plane of the MCH.

Figure 11 also illustrates how a horizontal corridor with no routing on Layer 3 in between the address and data signals allows feeding of the VCCA (1.8 V) power plane to the PLL power delivery pins VCCGA and VCCHA of the Intel 855PM MCH and continues to the VCCA[3:0] pins of the processor. Notice that this 1.8-V VCCA power plane “forks” as a separate branch from the 1.8-V decoupling capacitor while the Hub Interface (HI) 1.8-V power pins connect to a separate branch of the 1.8-V power plane flood on Layer 3. This is done to reduce noise pickup of the PLL power delivery due to HI switching activity.

Figure 12 illustrates the processor socket vicinity escape routing of the source synchronous FSB signals and their successful coexistence with robust power delivery. All source synchronous signals are connected with minimum length dog bones from the BGA lands of the socket on the primary side layer into internal layers Layer 3 and Layer 6. In Figure 11, note the changing orientation of the dog bone "dipoles" as they rotate around the sides of the pin field to guarantee smooth escape routing on Layer 3 and Layer 6.

In addition to signal routing on the primary side, Layer 3 and Layer 6 are also used to feed the core power delivery into the areas free of signals routing. VCCA (1.8 V) starts from the MCH in Figure 11 and is routed on Layer 3 and is connected with a cluster of vias to a VCCA flood on the primary side layer. This feeds the primary side "U shape" on the three sides of the processor socket that feeds the VCCA[3:0] pins. To minimize loop inductance of the VCCA (1.8 V) vias, they are accompanied by two GND stitching vias.

Figure 13 shows a global view of FSB source synchronous signal routing and its coexistence with a robust power delivery layout solution. Source synchronous signals are serpentine length matched on Layer 3 and Layer 6 in the area in between the processor and Intel 855PM MCH packages per the procedure described in Section 4.1.3.5. Also, the source synchronous address signals route around the thermal backing plate hole and utilize the space on Layer 3 and Layer 6 in the socket vicinity to perform trace length equalization.

Since GTLREF generation and the COMP[3:0] resistor connections minimize via use, there is minimal interaction between these vias with the routing of the source synchronous signals. Refer to Section 4.1.7, Figure 29, Figure 31, and Section 4.1.8.1 for further details.

Also the complete corridor flood routing of VCCA from the MCH can be seen on Figure 13 starting on Layer 3 and then transitioning to the primary side of the motherboard with the cluster of vias next to the processor socket. Figure 13 also illustrates why the 100-MHz clocks that are routed on Layer 3 can not get to the processor pins on either Layer 3 nor Layer 6. Thus, the two clocks transition to the secondary side of the motherboard (not shown in Figure 13) to obtain the shortest vertical distance to the processor's BCLK[1:0] pins and the ITP_CLK[1:0] pins of the ITP700FLEX debug port. See Section 4.3.1 for further details.

Figure 11. Intel 855PM MCH Source Synchronous Signals Recommended Escape Routing Example

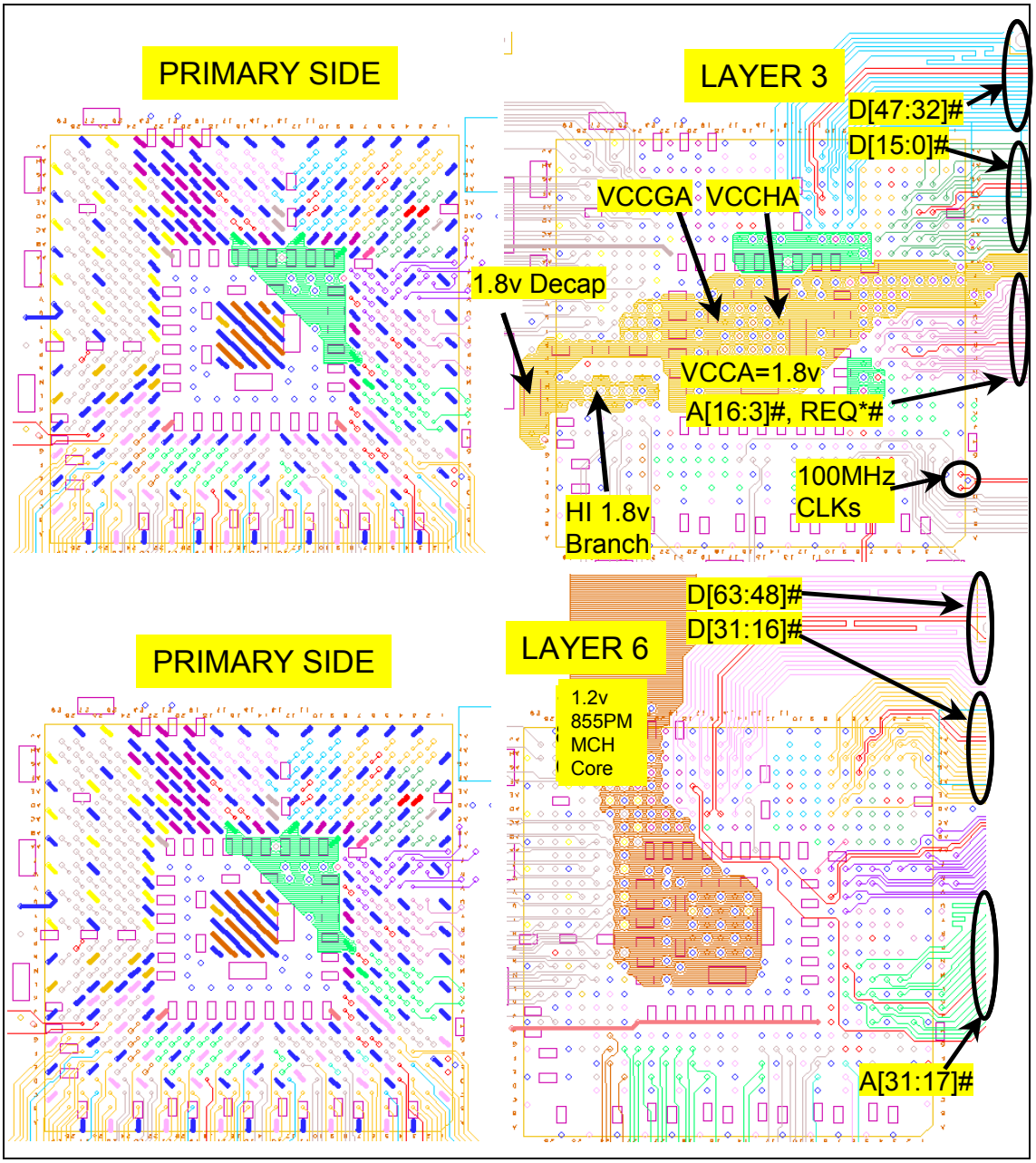


Figure 12. Processor Source Synchronous Signals Recommended Escape Routing Example

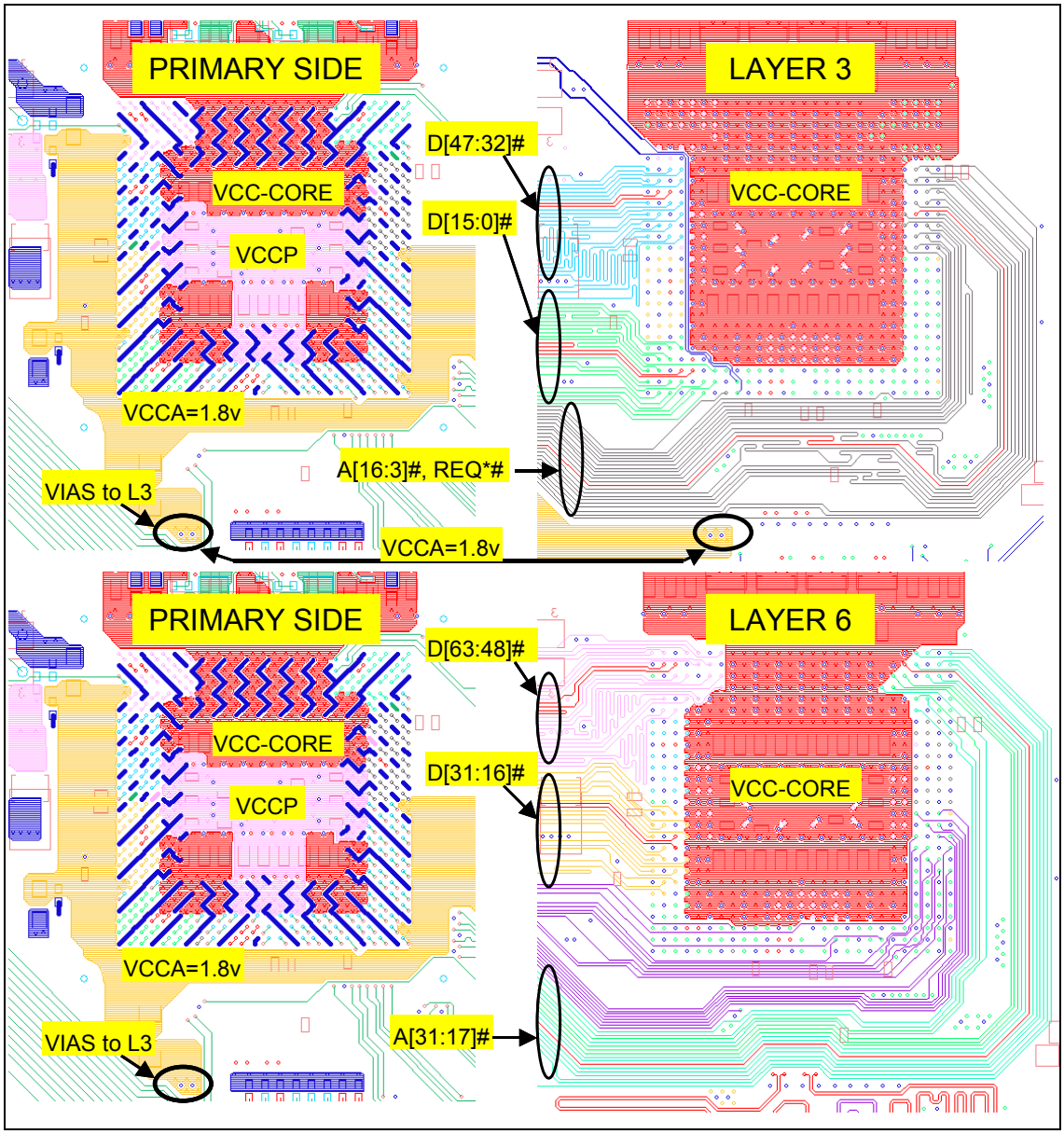
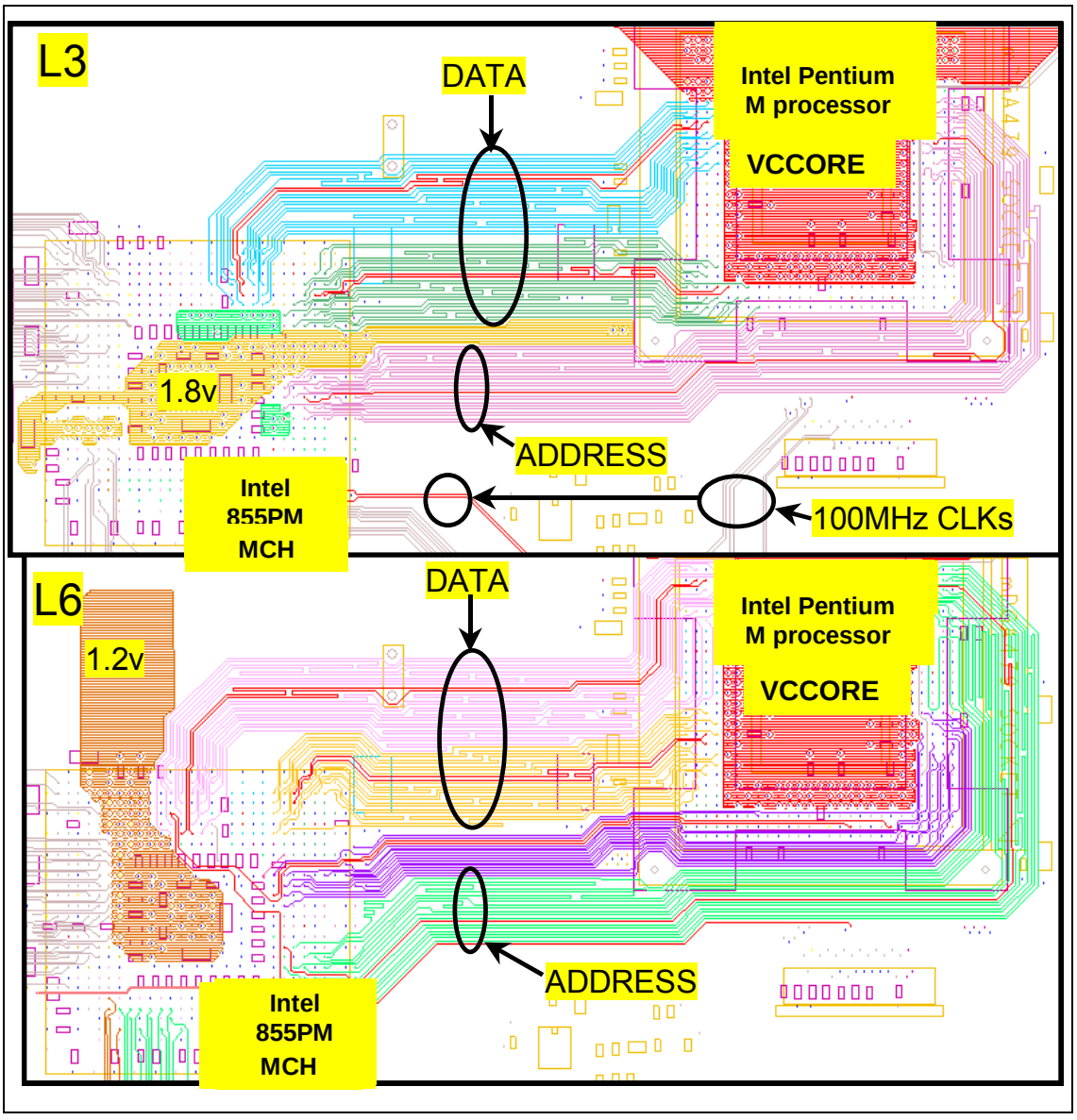


Figure 13. Processor to Intel 855PM MCH Source Synchronous Signals Routing Example

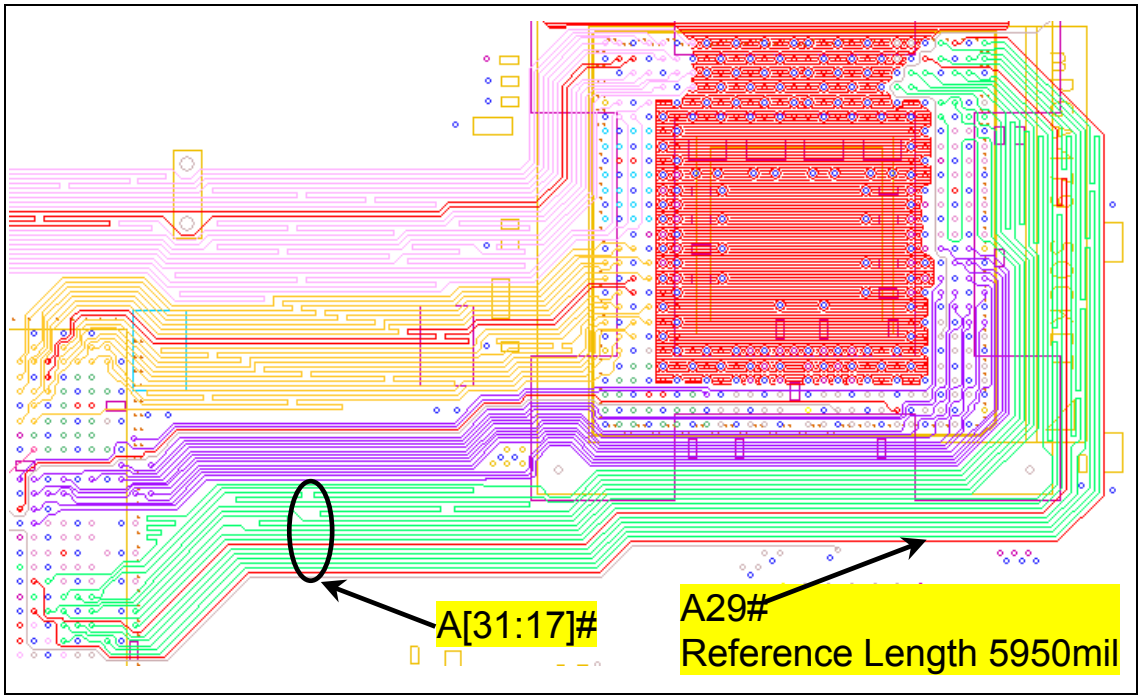


4.1.3.5. Trace Length Equalization Procedures

The following example describes how to adjust a trace so that it will be length-matched to its reference. A spreadsheet software program i.e. Microsoft* Excel* is used to facilitate the trace length matching process. The layout editor used in this example is Allegro*. Figure 15 illustrates the trace length matching procedure as described below:

1. Cell B3 in Excel is preset to calculate the , which is the difference between the starting length and reference length. This cell will calculate the function "B1 - B2."
2. Cell B4 calculates half of the which is equal to the value in Cell B3 divided by 2 This cell will calculate the function "B3 / 2."
3. Pre-route all the traces to approximately the same length using serpentines. The serpentines have to use the same 1:3 spacing as the rest of the routing. It will be useful to make the traces 16 – 32 mils longer than needed in this stage. It is also important that there should be **no** 90 angles in the serpertines.
4. Select the trace in the group of traces to be equalized that cannot be made any shorter. Taking A[31:17]# as an example, in Figure 14 the longest trace that defines the reference length turns out to be A29#. Note that there are no serpentines on this signal. Use the Allegro I (info) command to report the reference length of the longest trace in the group. Record the reference length in cell B1 of Excel*.

Figure 14. Reference Trace Length Selection



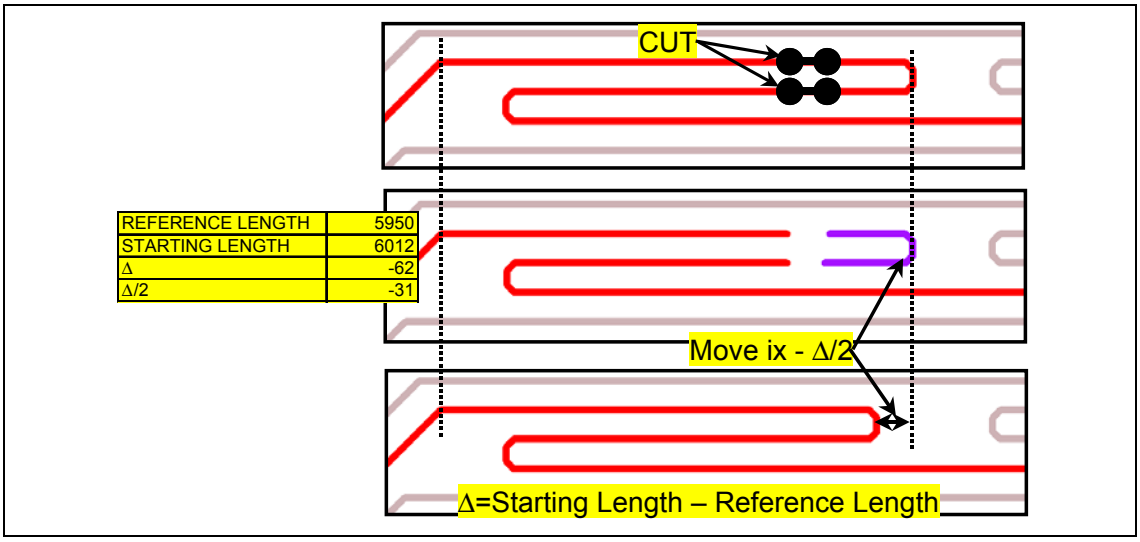
5. Use the Allegro* I (info) command to report the current length of the trace to be equalized. Record the length in cell B2 of the Excel* spreadsheet.
6. Use the Allegro* "Cut" command to cut the trace in two locations of the serpentine as shown in Figure 15. This will generate a floating section of the serpentine.

7. Use the Allegro* “Move ix” (i.e. if vertical routing) command to move the floating section by the /2 distance listed in cell B4.

8. Reconnect the floating segment if needed.

9. Repeat steps 5 through 8 for the reminder of the traces in the group

Figure 15. Trace Length Equalization Procedures with Allegro*



4.1.4. Asynchronous Signals

4.1.4.1. Topologies

The following sections describe the topologies and layout recommendations for the Asynchronous Open Drain and CMOS Signals found on the platform.

All Open Drain signals listed in the following sections below must be pulled-up to V_{CCP} (1.05 V). If any of these Open Drain signals are pulled-up to a voltage higher than V_{CCP}, the reliability and power consumption of the processor may be affected. Therefore, it is very important to follow the recommended pull-up voltage for these signals.

4.1.4.1.1. Topology 1A: Open Drain (OD) Signal Driven by the Processor – IERR#

The Topology 1A OD signal IERR# should adhere to the following routing and layout recommendations. Table 8 lists the recommended routing requirements for the IERR# signal of the processor. The routing guidelines allow the signal to be routed as either micro-strip or strip-lines using 55 ± 15% characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is V_{CCP} (1.05 V). Due to the dependencies on system design implementation, IERR# can be implemented in a number of ways to meet design goals. IERR# can be routed as a test point or to any optional system receiver.

Figure 16. Routing Illustration for Topology 1A

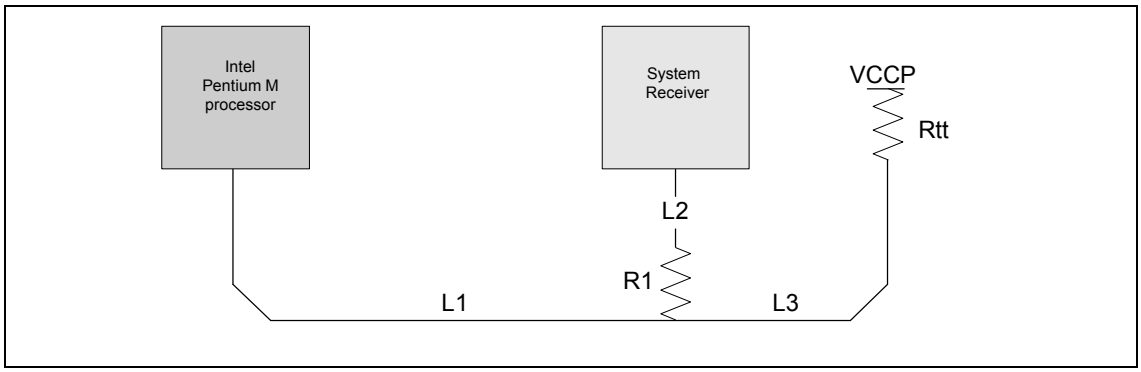


Table 8. Layout Recommendations for Topology 1A

L1	L2	L3	R1	Rtt	Transmission Line Type
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 ± 5%	56 ± 5%	Micro-strip
0.5” – 12.0”	0” – 3.0”	0” – 3.0”	56 ± 5%	56 ± 5%	Strip-line

4.1.4.1.2. Topology 1B: Open Drain (OD) Signals Driven by the Processor – FERR# and THERMTRIP#

The Topology 1B OD signals FERR# and THERMTRIP# should adhere to the following routing and layout recommendations. Table 9 lists the recommended routing requirements for the FERR# and THERMTRIP# signals of the processor. The routing guidelines allows the signals to be routed as either micro-strips or strip-lines using 55 ± 15% characteristic trace impedance. Series resistor R1 is a dampening resistor for reducing overshoot/undershoot reflections on the transmission line. The pull-up voltage for termination resistor Rtt is V_{CCP} (1.05 V).

Intel recommends that the FERR# signal of the processor be routed to the FERR# signal of the Intel 82801DBM ICH4-M. THERMTRIP# can be implemented in a number of ways to meet design goals. It can be routed to the ICH4-M or any optional system receiver. Intel recommends that the THERMTRIP# signal of the processor be routed to the THRMTRIP# signal of the ICH4-M. The ICH4-M's THRMTRIP# signal is a new signal to the I/O controller hub architecture that allows the ICH4-M to quickly put the whole system into a S5 state whenever the catastrophic thermal trip point has been reached.

If either FERR# or THERMTRIP# is routed to an optional system receiver rather than the ICH4-M and the interface voltage of the optional system receiver does not support a 1.05-V voltage swing, then a voltage translation circuit must be used. If the recommended voltage translation circuit described in Section 4.1.4.2 is used, the driver isolation resistor shown in Figure 24, Rs, should replace the series dampening resistor R1 in Topology 1B. Thus, it is important to note that R1 will no longer be required in such a topology.

Figure 17. Routing Illustration for Topology 1B

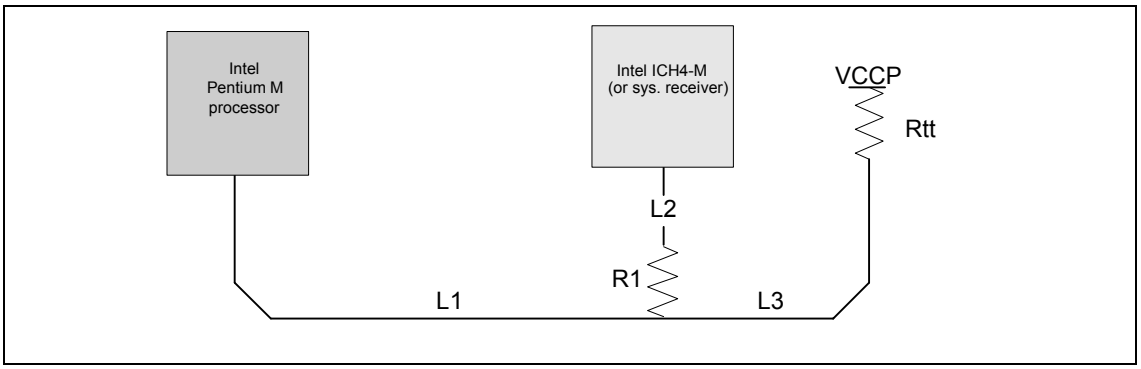


Table 9. Layout Recommendations for Topology 1B

L1	L2	L3	R1	Rtt	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	56 ± 5%	56 ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	56 ± 5%	56 ± 5%	Strip-line

4.1.4.1.3. Topology 1C: Open Drain (OD) Signals Driven by the Processor – PROCHOT#

The Topology 1C OD signal PROCHOT#, should adhere to the following routing and layout recommendations. Table 10 lists the recommended routing requirements for the PROCHOT# signal of the processor. The routing guidelines allows the signal to be routed as either a micro-strip or strip-line using 55 ± 15% characteristic trace impedance. Figure 18 shows the recommended implementation for providing voltage translation between the processor's PROCHOT# signal and a system receiver that utilizes a 3.3-V interface voltage (shown as V_IO_RCVR).

Series resistor Rs is a component of the voltage translation logic and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 24. Rs should be placed at the beginning of the T-split from the PROCHOT# signal. The pull-up voltage for termination resistor Rtt is V_{CCP} (1.05 V).

Intel recommends that PROCHOT# be routed using the voltage translation logic shown in Figure 18. The receiver at the output of the voltage translation circuit can be any system receiver that can function properly with the PROCHOT# signal given the nature and usage model of this pin. PROCHOT# is capable of toggling hundreds of times per second to signal a hot temperature condition.

Figure 18. Routing Illustration for Topology 1C

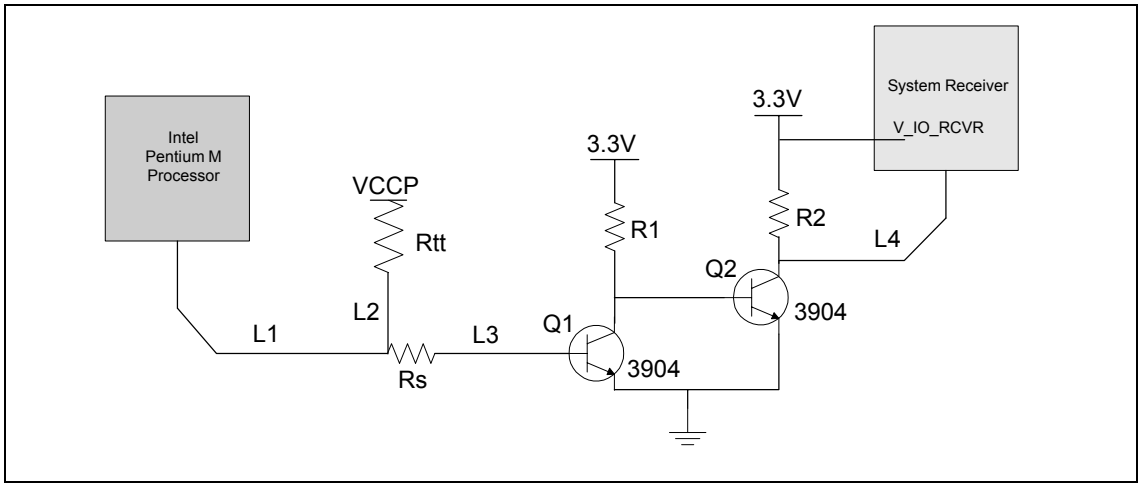


Table 10. Layout Recommendations for Topology 1C

L1	L2	L3	L4	Rs	R1	R2-	Rtt	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	0.5" – 12.0"	330 ± 5%	1.3 k ± 5%	330 ± 5%	56 ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	0" – 3.0"	0.5" – 12.0"	330 ± 5%	1.3 k ± 5%	330 ± 5%	56 ± 5%	Strip-line

4.1.4.1.4. Topology 2A: Open Drain (OD) Signal Driven by Intel 82801DBM ICH4-M – PWRGOOD

The Topology 2A OD signal PWRGOOD driven by the Intel 82801DBM ICH4-M (processor CMOS signal input) should adhere to the following routing and layout recommendations. Table 11 lists the recommended routing requirements for the PWRGOOD signal of the processor. The routing guidelines allows the signal to be routed as either micro-strip or strip-lines using 55 ± 15% characteristic trace impedance. The pull-up voltage for termination resistor Rtt is V_{CCP} (1.05 V). Note that the Intel ICH4-M's CPUPWRGD signal should be routed point-to-point to the processor's PWRGOOD signal. The routing from the processor's PWRGOOD pin should fork out to both to the termination resistor, Rtt, and the ICH4-M. Segments L1 and L2 from Figure 19 should not T-split from a trace from the processor pin.

Figure 19. Routing Illustration for Topology 2A

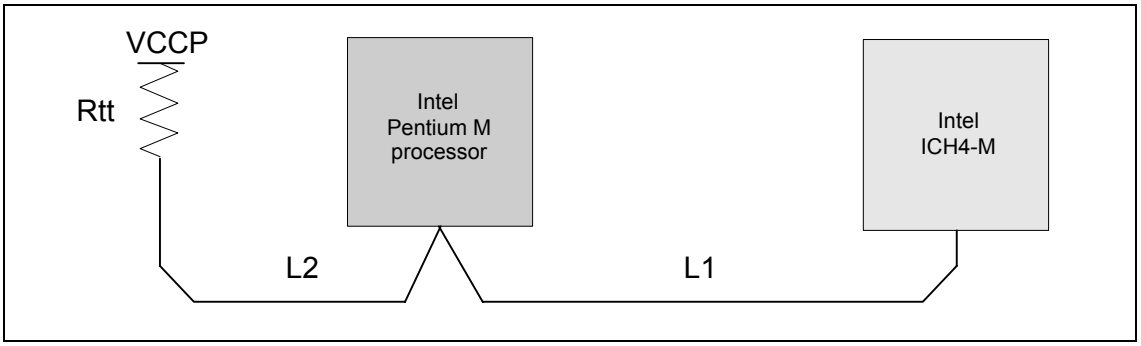


Table 11. Layout Recommendations for Topology 2A

L1	L2	Rtt	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	330 ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	330 ±5%	Strip-line

4.1.4.1.5. Topology 2B: CMOS Signals Driven by Intel 82801DBM ICH4-M – DPSLP#

The Topology 2B CMOS DPSLP# signal driven by the Intel 82801DBM ICH4-M (processor CMOS signal input) should adhere to the following routing and layout recommendations illustrated in Figure 20. As listed in Table 12, the L1 and L2 segments of the DPSLP# signal topology can be routed as either micro-strip or strip-lines using 55 ± 15% characteristic trace impedance. Note that the ICH4-M's DPSLP# signal should be routed point-to-point with the daisy chain topology shown. The routing of DPSLP# at the processor should fork out to both the ICH4-M and the Intel 855PM MCH. Segments L1 and L2 from Figure 20 should not T-split from a trace from the processor pin.

Figure 20. Routing Illustration for Topology 2B

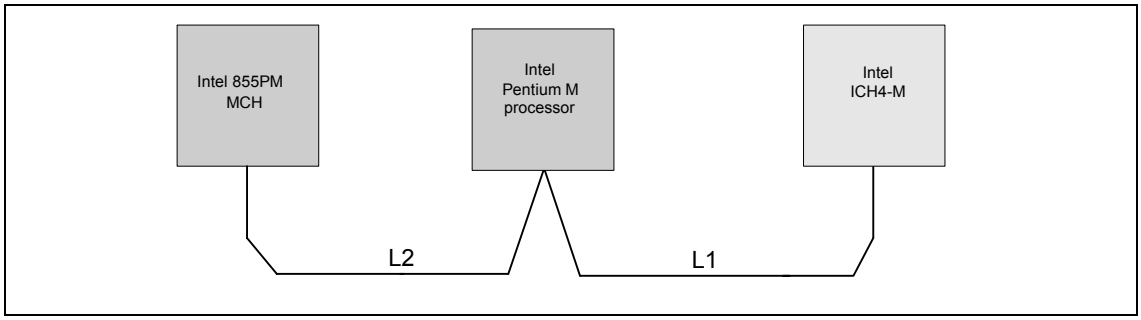
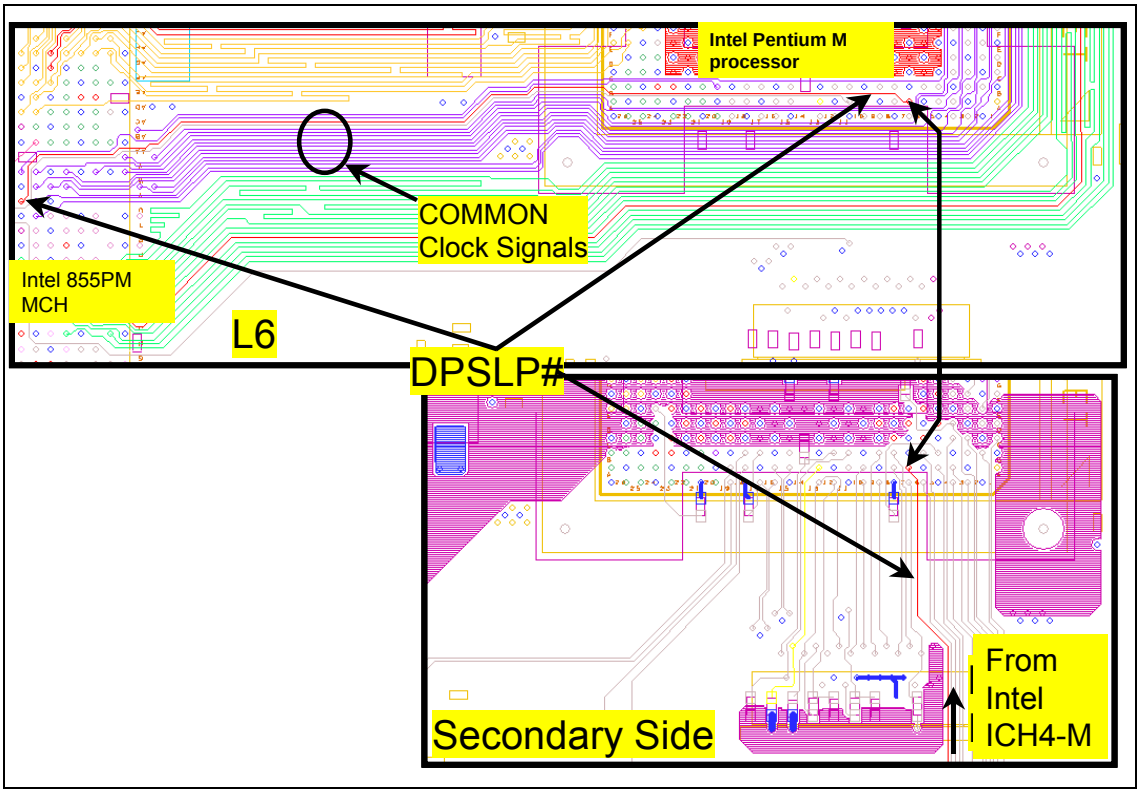


Table 12. Layout Recommendations for Topology 2B

L1	L2	Transmission Line Type
0.5" – 12.0"	0.5" – 6.5"	Micro-strip
0.5" – 12.0"	0.5" – 6.5"	Strip-line

Figure 21 illustrates a DPSLP# signal routing example to conform to Topology 2B recommendations. The routing starts from the ICH4-M's DPSLP# signal on the secondary side layer of the motherboard to the processor 's DPSLP# pin. The dog bone via allows switching of the routing layer to Layer 6 thereby allowing routing to the Intel 855PM MCH's DPSLP# pin located in the same cluster as the remaining common clock signals routed between the processor and MCH. The routing layer change from the secondary side to Layer 6 using the processor DPSLP# pin dog bone via is strongly advised to avoid any stub tapering of the CPU connection off of the ICH4-M to MCH connection to minimize transmission line effects.

Figure 21. DPSLP# Layout Routing Example



4.1.4.1.6. Topology 2C: CMOS Signals Driven by Intel 82801DBM ICH4-M – LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK#

The Topology 2C CMOS LINT0/INTR, LINT1/NMI, A20M#, IGNNE#, SLP#, SMI#, and STPCLK# signals should implement a point-to-point connection between the Intel 82801DBM ICH4-M and the processor. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 55 ± 15% characteristic trace impedance. No additional motherboard components are necessary for this topology.

Figure 22. Routing Illustration for Topology 2C

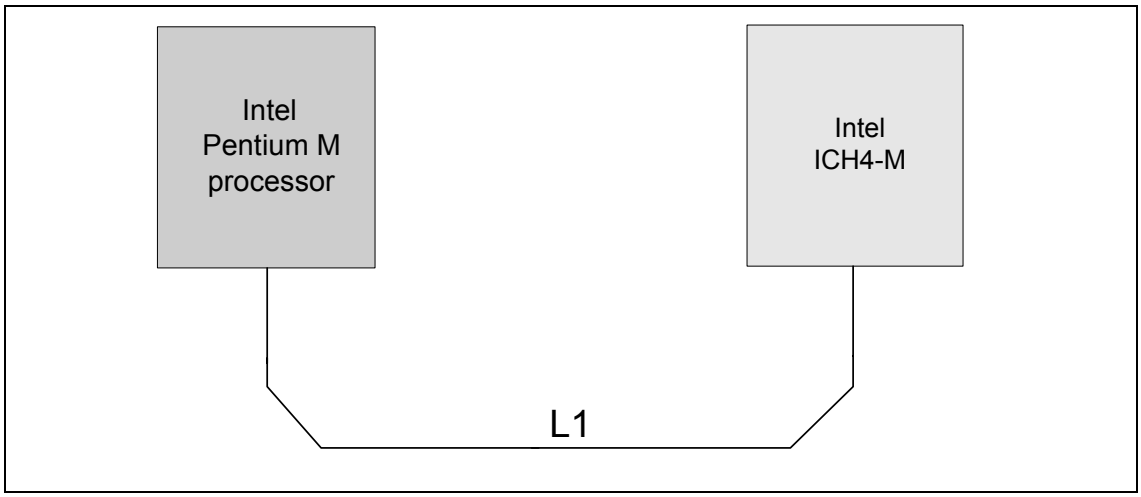


Table 13. Layout Recommendations for Topology 2C

L1	Transmission Line Type
0.5” – 12.0”	Micro-strip
0.5” – 12.0”	Strip-line

4.1.4.1.7. Topology 3: CMOS Signals Driven by Intel 82801DBM ICH4-M to Processor and FWH – INIT#

The signal INIT# should adhere to the following routing and layout recommendations. Table 14 lists the recommended routing requirements for the INIT# signal of the ICH4-M. The routing guidelines allow both signals to be routed as either micro-strip or strip-lines using 55 ± 15% characteristic trace impedance. Figure 23 shows the recommended implementation for providing voltage translation between the ICH4-M's INIT# voltage signaling level and any firmware hub (FWH) that utilizes a 3.3 V interface voltage (shown as a supply V_IO_FWH). See Section 4.1.4.2 for more details on the voltage translator circuit. For convenience, the entire topology and required transistors and resistors for the voltage translator is shown in Figure 23.

Series resistor Rs is a component of the voltage translator logic circuit and serves as a driver isolation resistor. Rs is shown separated by distance L3 from the first bipolar junction transistor (BJT), Q1, to emphasize the placement of Rs with respect to Q1. The placement of Rs a distance of L3 before the Q1 BJT is a specific implementation of the generalized voltage translator circuit shown in Figure 24. The routing recommendations of transmission line L3 in Figure 23 is listed in Table 14 and Rs should be placed at the beginning of the T-split of the trace from the ICH4-M's INIT# pin.

Figure 23. Routing Illustration for Topology 3

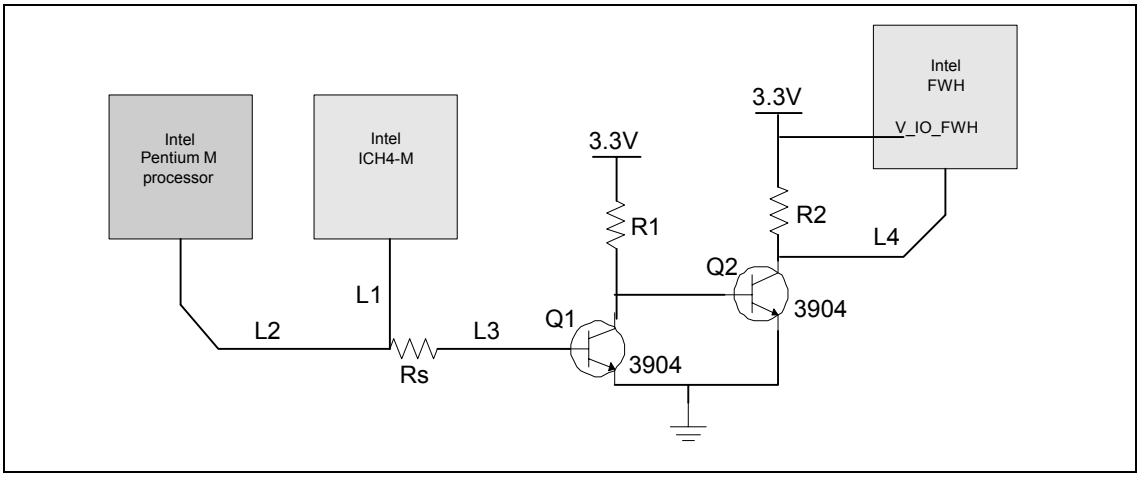


Table 14. Layout Recommendations for Topology 3

L1 + L2	L3	L4	Rs	R1	R2	Transmission Line Type
0.5" – 12.0"	0" – 3.0"	0.5" – 6.0"	330 ± 5%	1.3 k ± 5%	330 ± 5%	Micro-strip
0.5" – 12.0"	0" – 3.0"	0.5" – 6.0"	330 ± 5%	1.3 k ± 5%	330 ± 5%	Strip-line

For details on INIT# assertion/deassertion timings, see Section 9.7.5 for more details.

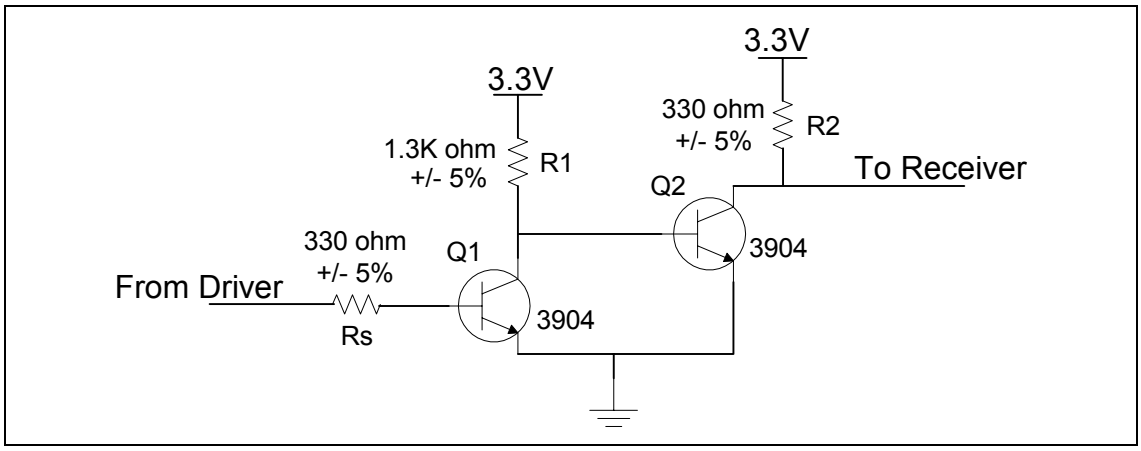
4.1.4.2. Voltage Translation Logic

A voltage translation circuit or component is required on any signals where the voltage signaling level between two components connected by a transmission line may cause unpredictable signal quality. The recommended voltage translation circuit for the platform is shown in Figure 24. For the INIT# signal (Section 4.1.4.1.7), a specialized version of this voltage translator circuit is used where the driver isolation resistor, Rs, is place at the beginning of a transmission line that connects to the first bipolar junction transistor, Q1. Though the circuit shown in Figure 24 was developed to work with signals that require translation from a 1.05-V to a 3.3-V voltage level, the same topology and component values, in general, can be adapted for use with other signals as well provided the interface voltage of the receiver is also 3.3 V. Any component value changes or component placement requirements for other signals must be simulated in order to guarantee good signal quality and acceptable performance from the circuit.

In addition to providing voltage translation between driver and receiver devices, the recommended circuit also provides filtering for noise and electrical glitches. A larger first-stage collector resistor, R1, can be used on the collector of Q1, however, it will result in a slower response time to the output falling edge. In the case of the INIT# signal, resistors with values as close as possible to those listed in Figure 24 should be used without exception.

With the low 1.05-V signaling level of the FSB, the voltage translation circuit provides ample isolation of any transients or signal reflections at the input of transistor Q1 from reaching the output of transistor Q2. Based on simulation results, the voltage translation circuit can effectively isolate transients as large as 200 mV and that last as long as 60 ns.

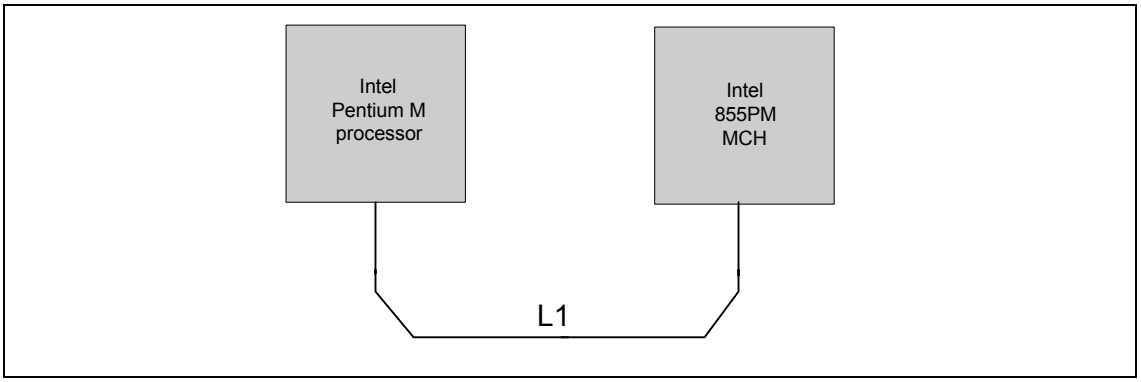
Figure 24. Voltage Translation Circuit



4.1.5. Processor RESET# Signal

The RESET# signal is a common clock signal driven by the Intel 855PM MCH CPURST# pin. In a production system where no ITP700FLEX debug port is implemented, a simple point-to-point connection between the CPURST# pin of the MCH and processor's RESET# pin is recommended (see Figure 25). On-die termination of the AGTL+ buffers on both the processor and the MCH provide proper signal quality for this connection. This is the same case as for the other common clock signals listed in Section 4.1.2. Length L1 of this interconnect should be limited to minimum of 1 inch and maximum of 6.5 inches.

Figure 25. Processor RESET# Signal Routing Topology with NO ITP700FLEX Connector



For a system that implements an ITP700FLEX debug port a more elaborate topology is required in order to guarantee proper signal quality at both the processor signal pad and the ITP700FLEX input receiver. In this case the topology illustrated in Figure 26 should be implemented. The CPURST# signal from the MCH should fork out (do not route one trace from MCH pin and then T-split) towards the processor's RESET# pin as well as towards the Rtt and Rs resistive termination network placed next to the ITP700FLEX debug port connector. Rtt (54.9 ± 1%) pulls-up to the V_{CCP} voltage and is placed at the end of the L2 line that is limited to a 12-inch maximum length. Rs (22.6 ± 1%) should be placed right next to Rtt to minimize the routing between them in the vicinity of the ITP700FLEX connector to limit the L3 length to less than 0.5 inches. ITP700FLEX operation requires the matching of L2 + L3 - L1 length to the length of the BPM[4:0]# signals length within ± 50 ps. Refer to Section 4.3.1 for more details on ITP700FLEX signal routing and Section 4.1.1.4 for more details on signal propagation time to distance correlation. See Table 15 for routing length summary and termination resistor values.

Currently 1% tolerance resistors are recommended for Rs and Rtt. The use of 5% tolerant resistors for these resistors and whether it could provide adequate signal quality performance is under investigation.

Figure 26. Processor RESET# Signal Routing Topology With ITP700FLEX Connector

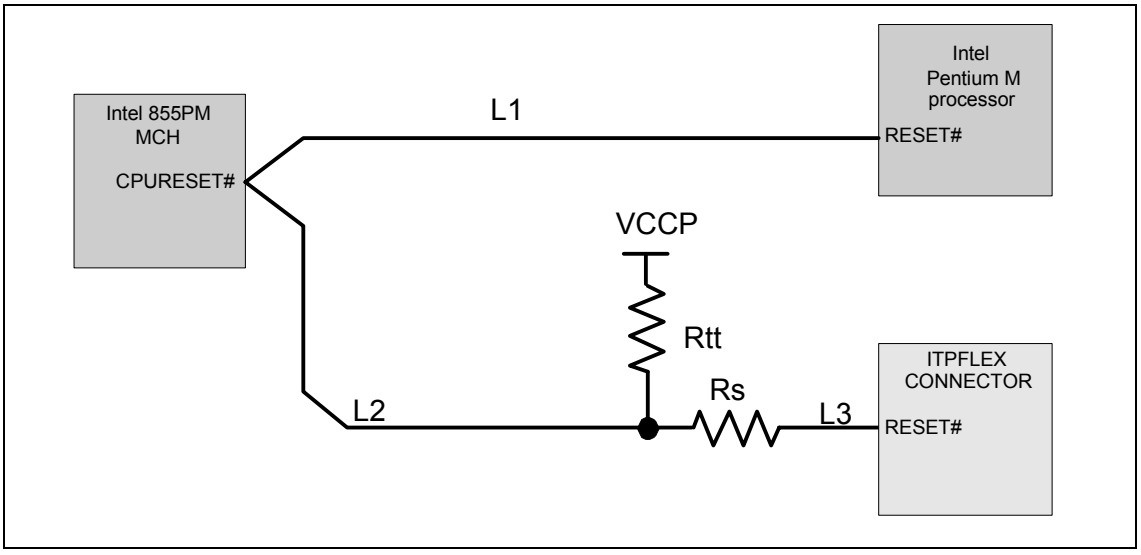


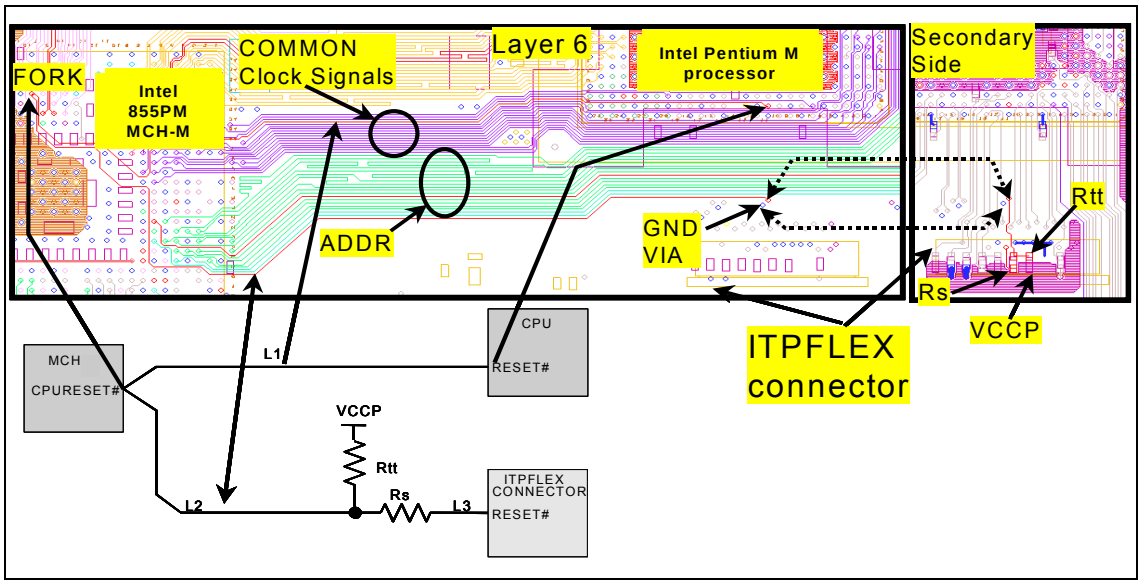
Table 15. Processor RESET# Signal Routing Guidelines with ITP700FLEX Connector

L1	L2 + L3	L3	Rs	Rtt
1.0” – 6.0”	12.0” max	0.5” max	Rs = 22.6 ± 1%	Rtt = 54.9 ± 1%

4.1.5.1. Processor RESET# Routing Example

Figure 27 illustrates a board routing example for the RESET# signal with an ITP700FLEX debug port implemented. Figure 27 illustrates how the CPURST# pin of Intel 855PM MCH forks out into two branches on Layer 6 of the motherboard. One branch is routed directly to the processor’s RESET# pin amongst the rest of the common clock signals. Another branch routes below the address signals and vias down to the secondary side that route to the Rs and Rtt resistors. These resistors are placed in the vicinity of the ITP700FLEX debug port. Note the placement of Rs and Rtt next to each other to minimize the routing between Rs and Rtt as well as the minimal routing between Rs and the ITP700FLEX connector. Also, since a transition between Layer 6 and the secondary side occurs, a GND stitching via is added to guarantee continuous ground reference of the secondary side routing of the RESET# signal to ITP700FLEX connector.

Figure 27. Processor RESET# Signal Routing Example with ITP700FLEX Debug Port

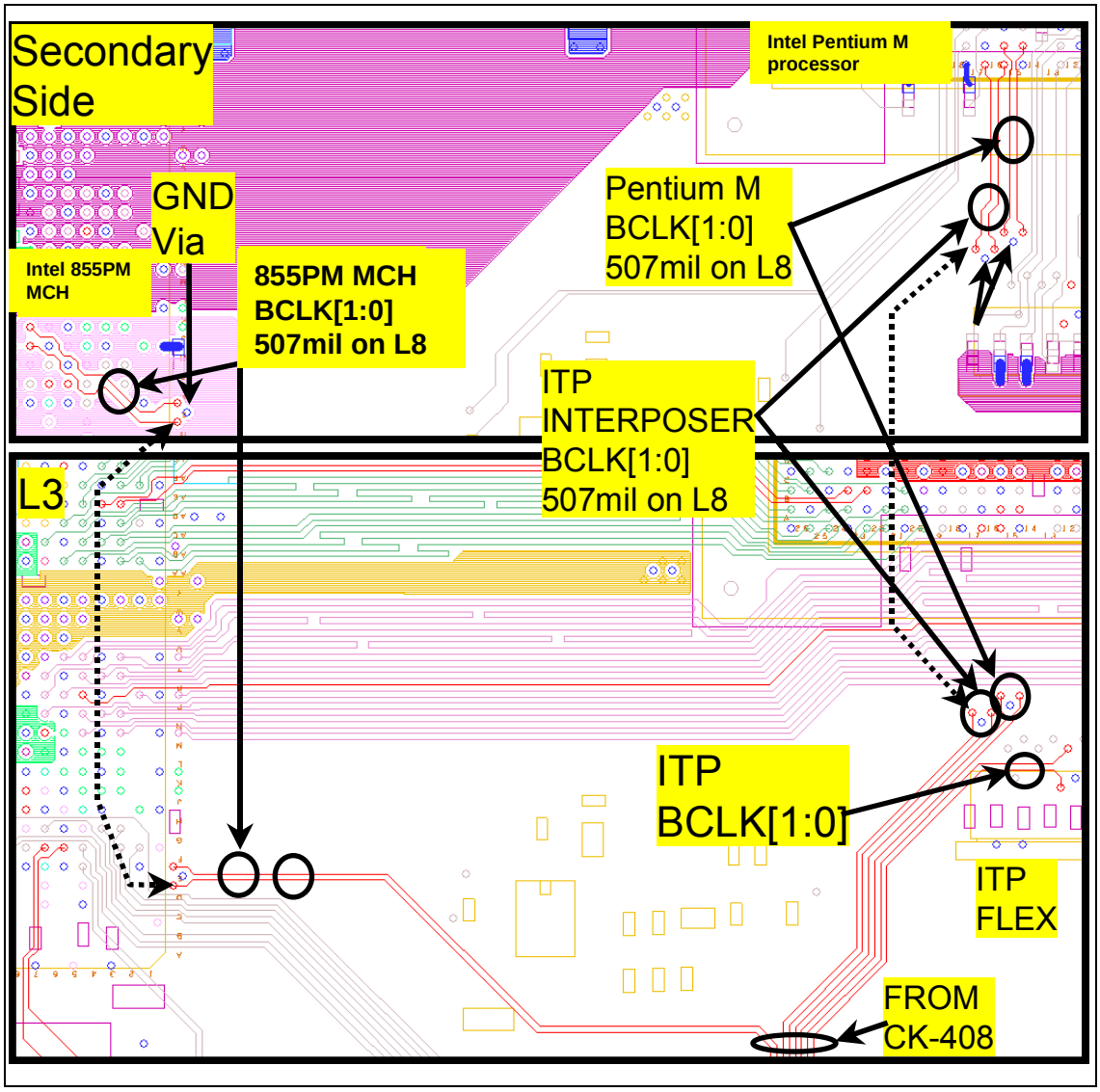


4.1.6. Processor and Intel 855PM MCH Host Clock Signals

Figure 28 illustrates processor and Intel 855PM MCH host clock signal routing. Both the processor and the MCH's BCLK[1:0] signals are initially routed from the CK-408 clock generator on Layer 3. Figure 13 shows how vertical routing on both Layer 3 and Layer 6 is blocked by the FSB address signals' horizontal routing. Thus, a transition to secondary side layer routing is needed to complete the BCLK[1:0] routing to the processor's pins. In the recommended routing example (Figure 28) secondary side layer routing of BCLK[1:0] is 507 mils long. To meet length-matching requirements between the processor and MCH's BCLK[1:0] signals, a similar transition from Layer 3 to the secondary side layer is done next to the MCH package outline. Routing of the MCH's BCLK[1:0] signals on the secondary side is also trace tuned to 507 mils. BCLK[1:0] layer transition vias are accompanied by GND stitching vias. For similar reasons, routing for the ITP interposer's BCLK[1:0] signals also transition from Layer 3 to the secondary side layer and have 507-mil long traces on this layer. Throughout the routing length on Layer 3, BCLK[1:0] signals should reference a solid GND plane on Layer 2 and Layer 4 as shown in Figure 10. See Section 10.2.1 for more details on host clock topologies and routing recommendations.

If a system supports either the on-board ITP700FLEX connector or ITP Interposer only, then differential host clock routing to either the ITP700FLEX connector or CPU socket but not both, is required.

Figure 28. Processor and Intel 855PM MCH Host Clock Layout Routing Example

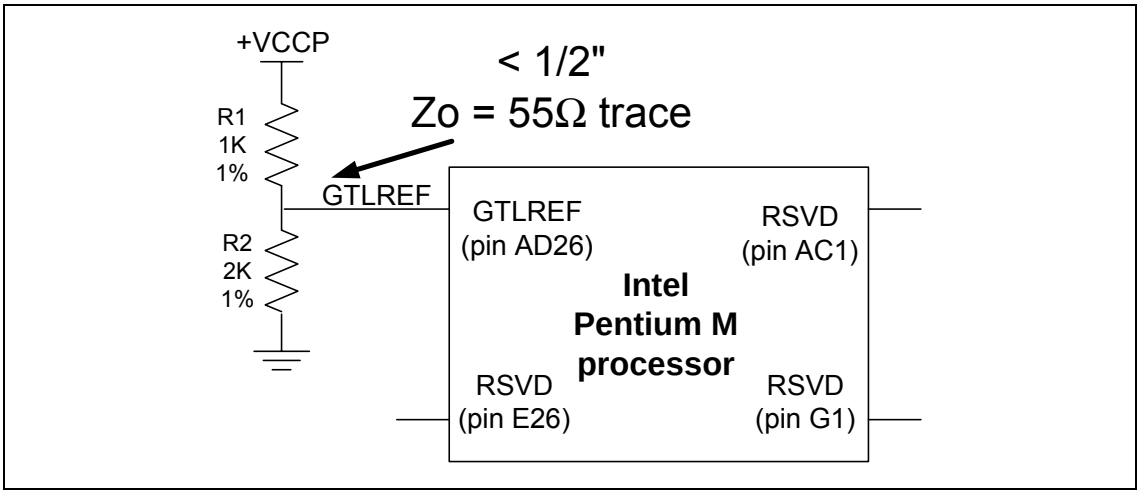


4.1.7. GTLREF Layout and Routing Recommendations

There is one AGTL+ reference voltage pin on the processor, GTLREF, which is used to set the reference voltage level for the AGTL+ signals (GTLREF). The reference voltage must be supplied to the GTLREF signal, pin AD26 of the processor pin-map. The voltage level that needs to be supplied to GTLREF must be equal to 2/3 * V_{CCP} ± 2%. The Intel 855PM MCH also requires a reference voltage (MCH_GTLREF) to be supplied to its HVREF[4:0] pins. The GTLREF voltage divider for both the processor and MCH cannot be shared. Thus, both the processor and MCH must have their own locally generated GTLREF networks. Figure 29 shows the recommended topology for generating GTLREF for Intel Pentium M processor using a R1 = 1 k ± 1% and R2 = 2 k ± 1% resistive divider.

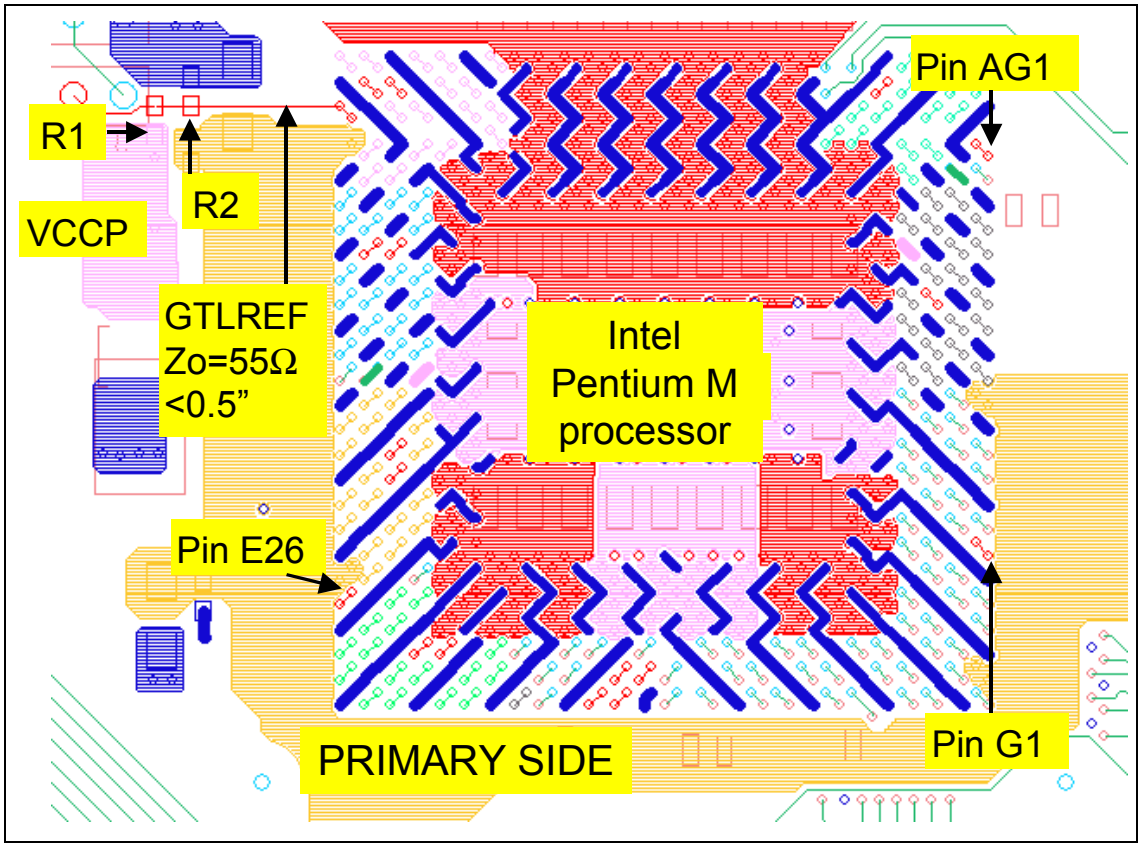
Since the input buffer trip point is set by the 2/3* V_{CCP} on GTLREF and to allow tracking of V_{CCP} voltage fluctuations, **no** decoupling should be placed on the GTLREF pin. The node between R1 and R2 (GTLREF) should be connected to the GTLREF pin of processor with a Zo = 55 trace shorter than 0.5 inches. Space any other switching signals away from GTLREF with a minimum separation of 25 mils. Do not allow signal lines to use the GTLREF routing as part of their return path (i.e. do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals).

Figure 29. Processor GTLREF Voltage Divider Network



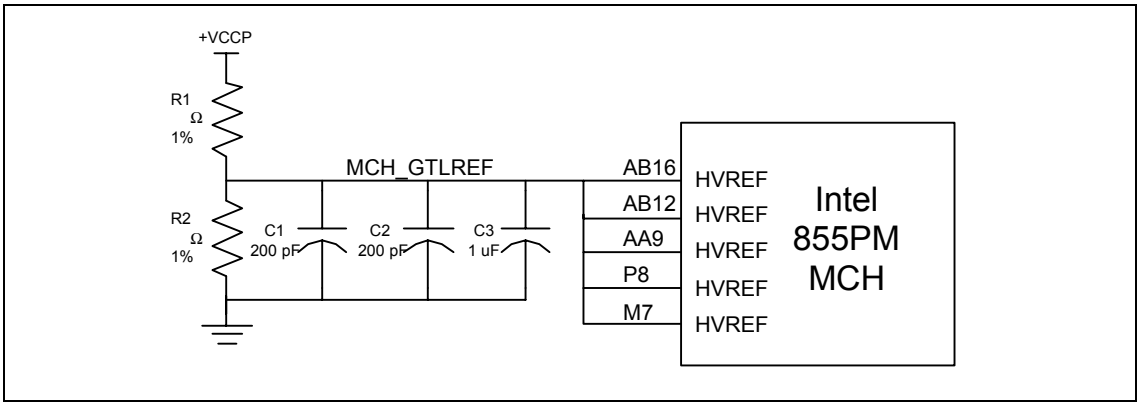
A recommended layout of GTLREF for the processor is shown in Figure 30. To avoid interaction with FSB routing and power delivery, GTLREF's R1 and R2 components are placed next to each other on the primary side of the motherboard and connected with a Zo = 55 370-mil long trace to the GTLREF pin on processor, which meets the 0.5-inch maximum length requirement. The BGA ball lands on the primary side for the RSVD signal pins E26, G1, and AC1 are shown for illustrative purposes and are not routed.

Figure 30. Processor GTLREF Motherboard Layout



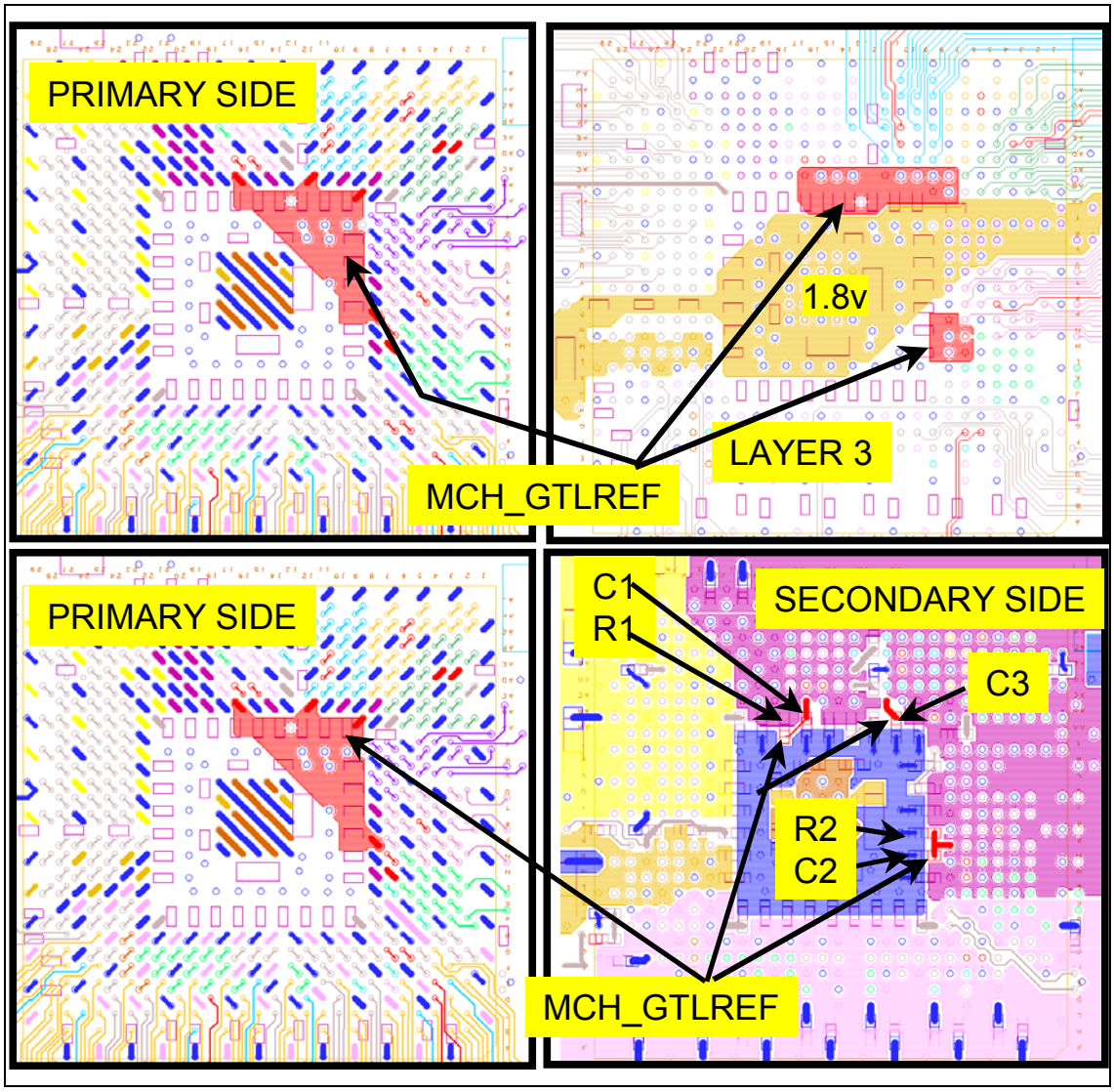
A recommended MCH_GTLREF generation circuit for the Intel 855PM MCH is shown in Figure 31. The circuit includes a resistive divider network with R1 = 49.9 ± 1% and R2 = 100 ± 1% and three decoupling capacitors C1 = C2 = 200 pF and C3 = 1 F all bypassed to GND. The MCH_GTLREF voltage connects to five Intel 855PM MCH HVREF pins: AB16, AB12, AA9, P8, and M7.

Figure 31. Intel 855PM MCH HVREF[4:0] Reference Voltage Generation Circuit



A recommended layout for the MCH_GTLREF generation circuit is shown in Figure 32. The MCH_GTLREF generation circuit components are located on the secondary side to minimize motherboard space usage and optimize robustness of the connection. Each of the AB16, AB12, and P8 HVREF pins has a decoupling capacitor (C1, C2, and C3) next to them. GND side of the C1, C2, and C3 capacitors is connected to the GND flood on the secondary side and stitched with vias to internal GND planes. R1 is placed next to pin AB16 and R2 is placed next to pin P8. Layer 3 of the motherboard shorts the two clusters of HVREF pins P8, M7, AB16, AB12, and AA9. The two clusters are further shorted on the primary side layer.

Figure 32. Intel 855PM MCH HVREF[4:0] Motherboard Layout



4.1.8. AGTL+ I/O Buffer Compensation

The processor has four pins, COMP[3:0], and the Intel 855PM MCH has two pins, HRCOMP[1:0], that require compensation resistors to adjust the AGTL+ I/O buffer characteristics to specific board and operating environment characteristics. Also, the MCH requires two special reference voltage generation circuits to pins HSWNG[1:0] for the same purpose described above. Refer to the *Intel® Pentium M Processor Datasheet, Intel® Celeron M Processor Datasheet, Intel® Pentium® M Processor on 90nm process with 2-MB L2 Cache Datasheet,* and *Intel® 855PM Memory Controller Hub (MCH) DDR200/266MHz Datasheet* for details on resistive compensation.

4.1.8.1. Processor AGTL+ I/O Buffer Compensation

For the processor, the COMP[2] and COMP[0] pins must each be pulled-down to ground with 27.4 ± 1% resistors and should be connected to the processor with a Zo = 27.4 trace that is less than 0.5 inches from the processor pins. The COMP[3] and COMP[1] pins must each be pulled-down to ground with 54.9 ± 1% resistors and should be connected to the processor with a Zo = 55 trace that is less than 0.5 inches from the processor pins.. COMP[3:0] traces should be at least 25 mils (> 50 mils preferred) away from any other toggling signal.

The recommended layout of the processor COMP[3:0] resistors is illustrated in Figure 33. To avoid interaction with FSB routing on internal layers and VCCA power delivery on the primary side, Layer 1, COMP[1:0] resistors are placed on the secondary side. Ground connections to the COMP[1:0] resistors use a small ground flood on the secondary side layer and connect only with a single GND via to stitch the GND planes. The compact layout as shown in Figure 33 should be used to avoid excessive "perforation" of the V_{CCP} plane power delivery. Figure 33 illustrates how a 27.4- resistor connects with an ~18-mil wide (Zo = 27.4) and 160-mil long trace to COMP0. Necking down to 14 mils is allowed for a short length to pass in between the dog bones. The 54.9- resistor connects with a regular 5-mil wide (Zo = 55) and 267-mil long trace to COMP1.

Placement of COMP[1:0] on the primary side is possible as well. An alternative placement implementation is shown if Figure 34.

To minimize motherboard space usage and produce a robust connection, the COMP[3:2] resistors are also placed on the secondary side (Figure 33, right side). A 27.4- resistor connects with an 18-mil wide (Zo = 27.4) and 260-mil long trace to COMP2. Necking down to 14 mils is allowed for a short length to pass in between the dog bones. Notice that the COMP2 (Figure 33, left side) dog bone trace connection on the primary side is also widened to 14 mils to meet the Zo = 27.4- characteristic impedance target. The right side of Figure 33 also illustrates how the 54.9 ± 1% resistor connects with a regular 5-mil wide (Zo = 55) and 100-mil long trace to COMP3. The ground connection of COMP[3:2] is done with a small flood plane on the secondary side that connects to the GND vias of pins AA1 and Y2 of the processor pin-map. This is done to avoid via interaction with the FSB routing on Layer 3 and Layer 6.

For COMP2 and COMP0, it is extremely important that 18-mil wide dog bone connections on the primary side and 18-mil wide traces on the secondary sides be used to connect the signals to compensation resistors on the secondary side. The use of 18-mil wide dog bones and traces is used to achieve the Zo = 27.4 target to ensure proper operation of the FSB. See Figure 35 for more details.

Figure 33. Processor COMP[3:0] Resistor Layout

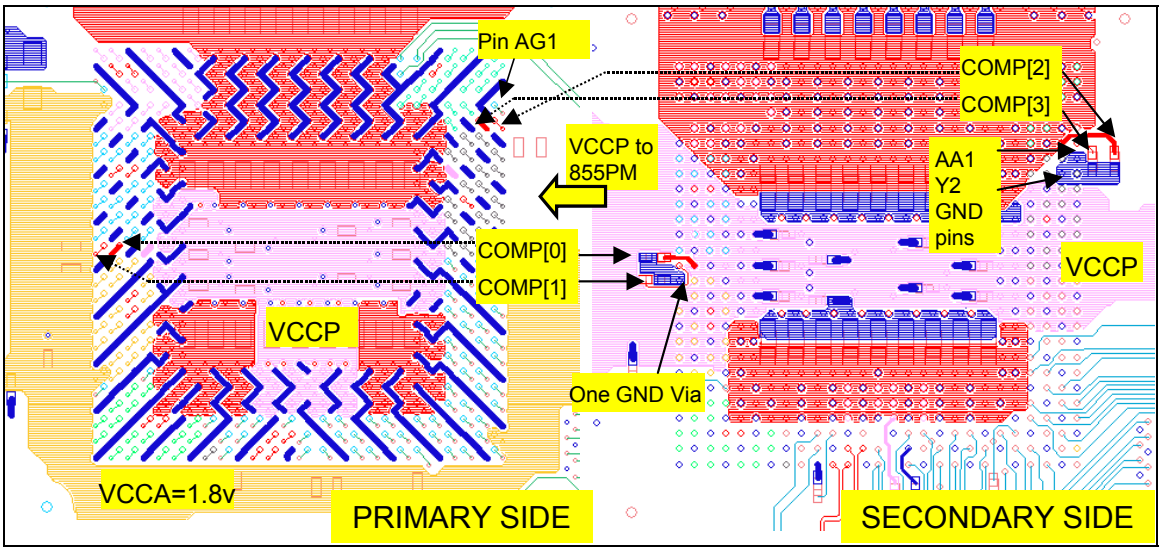


Figure 34. Processor COMP[1:0] Resistor Alternative Primary Side Layout

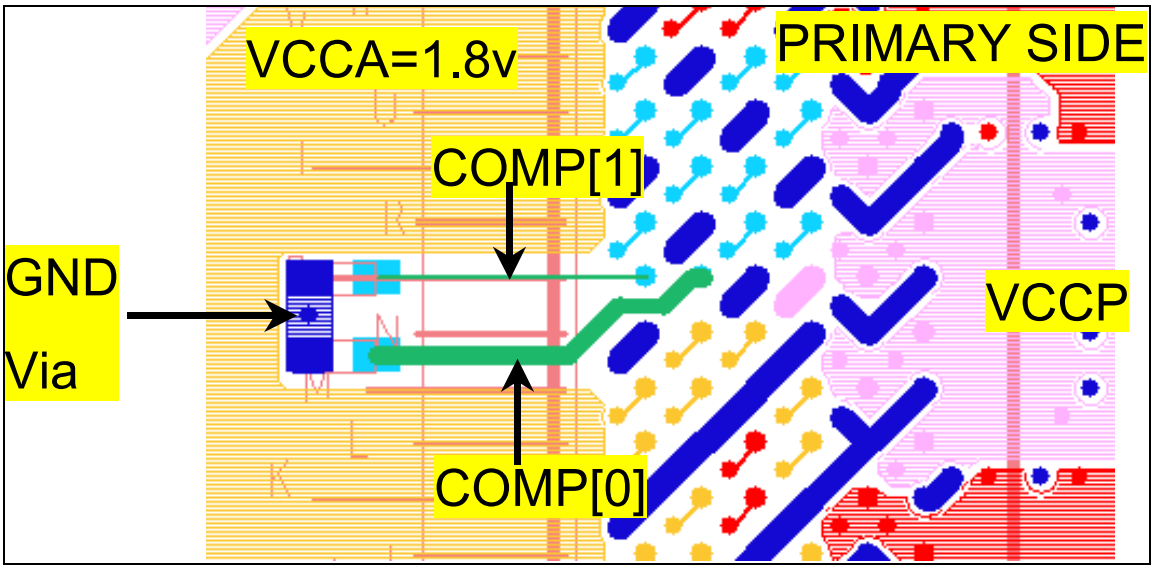
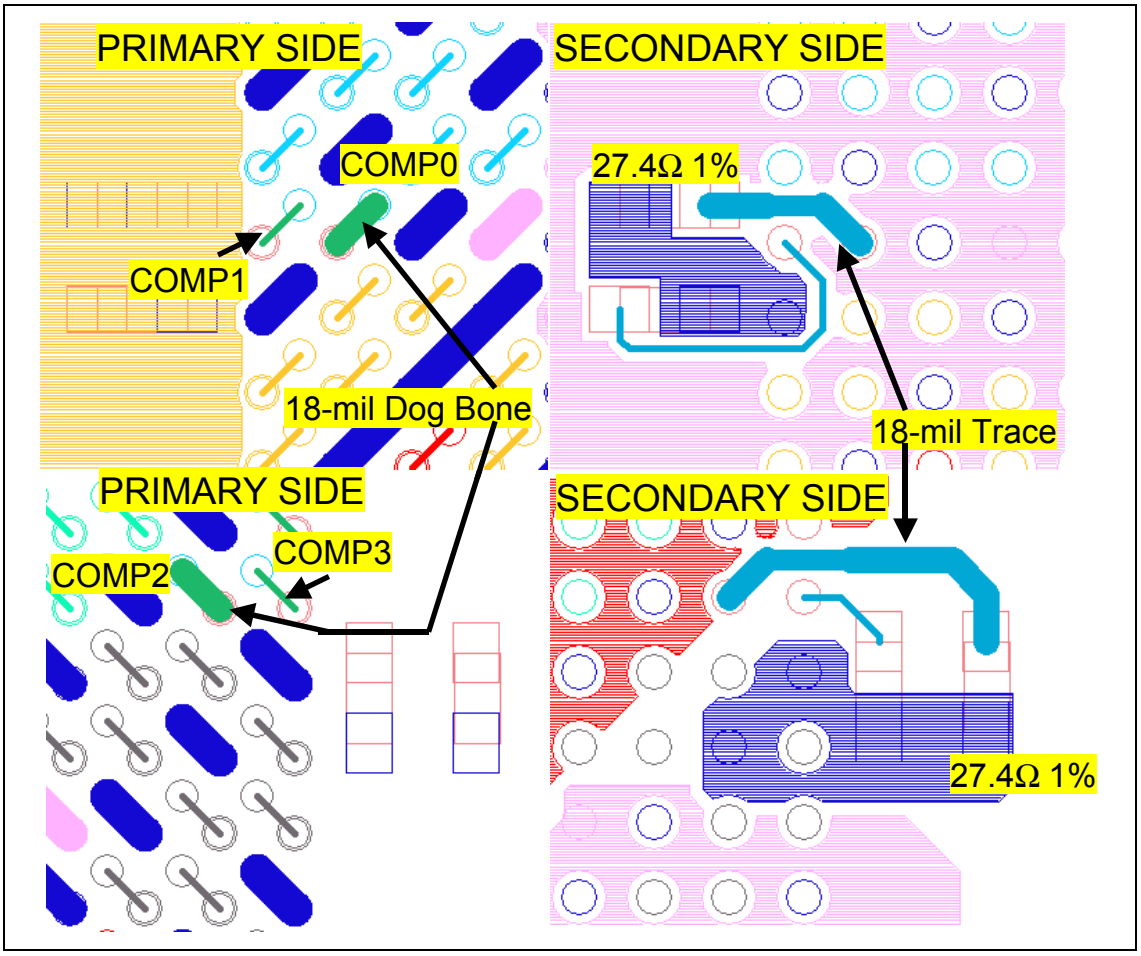


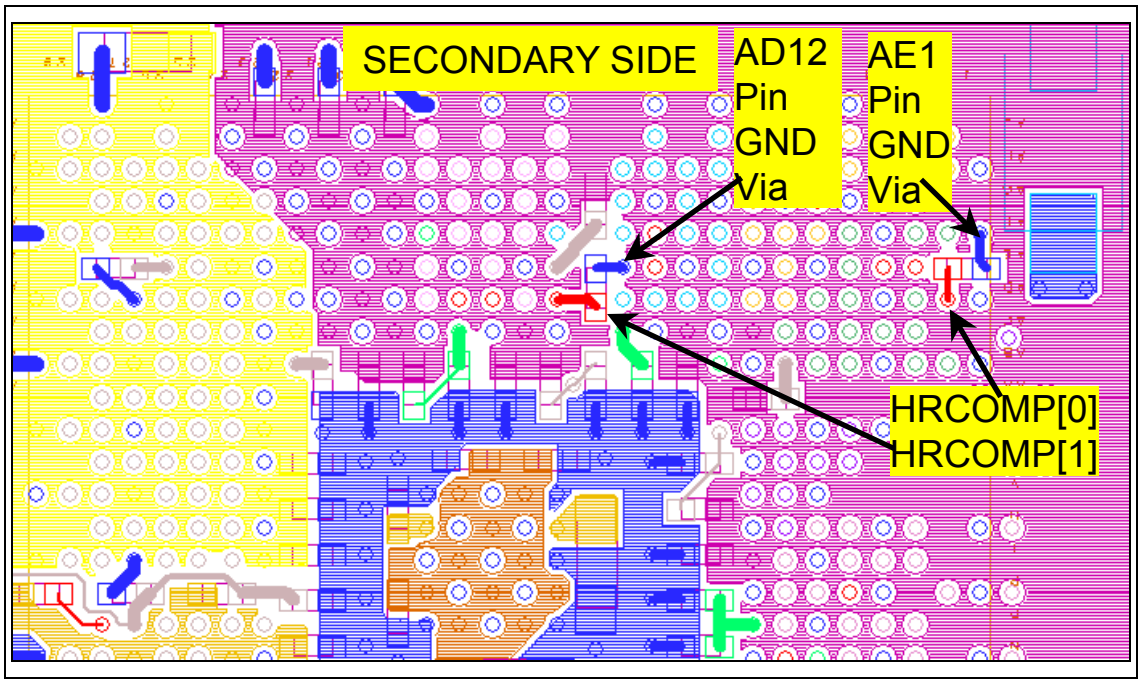
Figure 35. Processor COMP[2] and COMP[0] 18-Mil Wide Dog Bones and Traces



4.1.8.2. Intel 855PM MCH AGTL+ I/O Buffer Compensation

The Intel 855PM MCH AGTL+ I/O buffer resistive compensation signals pins of the MCH, HRCOMP[1:0], should each be pulled-down to ground with a 27.4 ± 1% resistor. The maximum trace length from pin to resistor should be less than 0.5 inches long and includes the dog bone connection on the primary side from the BGA land to the dog bone via. This < 0.5 inch long connection should be 18 mils wide to achieve the Zo = 27.4 target. Also, the routing for HRCOMP should be at least 25 mils away from any switching signal. Figure 36 illustrates the recommended layout for the Intel 855PM MCH HRCOMP[1:0] resistors that are placed on the motherboard's secondary side to save space as well as to make the shortest possible connection without interacting with FSB routing. To avoid GND via interaction of the HRCOMP[1:0] resistors, each should share the ground pin vias of the MCH's AE1 and AD12 ground pins to make the ground connection.

Figure 36. Intel 855PM MCH HRCOMP[1:0] Resistor Layout



The MCH's AGTL+ I/O buffer resistive compensation mechanism also requires the generation of reference voltages to the HSWNG[1:0] pins with a value of 1/3* V_{CCP}. The schematics for HSWNG[1:0] voltage generation is illustrated in Figure 37. Two resistive dividers with R1a = R1b = 301 ± 1% and R2a = R2b = 150 ± 1% generate the HSWNG[1:0] voltages. C1a = C1b = 0.01 µF act as decoupling capacitors and connect HSWNG[1:0] to V_{CCP}. HSWNG components should be placed within 0.5 inches of their respective pins and connected with a 15-mil wide trace. To avoid coupling with any other signals, maintain a minimum of 25 mils of separation to other signals.

Figure 37. Intel 855PM MCH HSWNG[1:0] Reference Voltage Generation Circuit

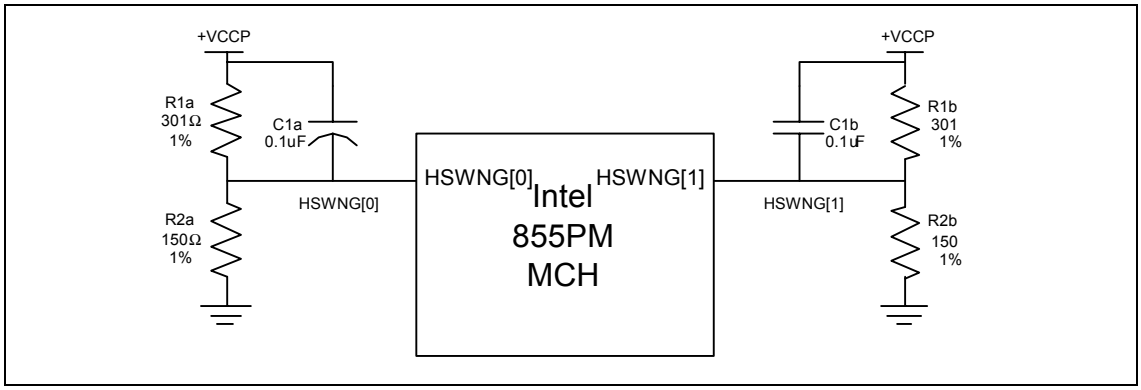
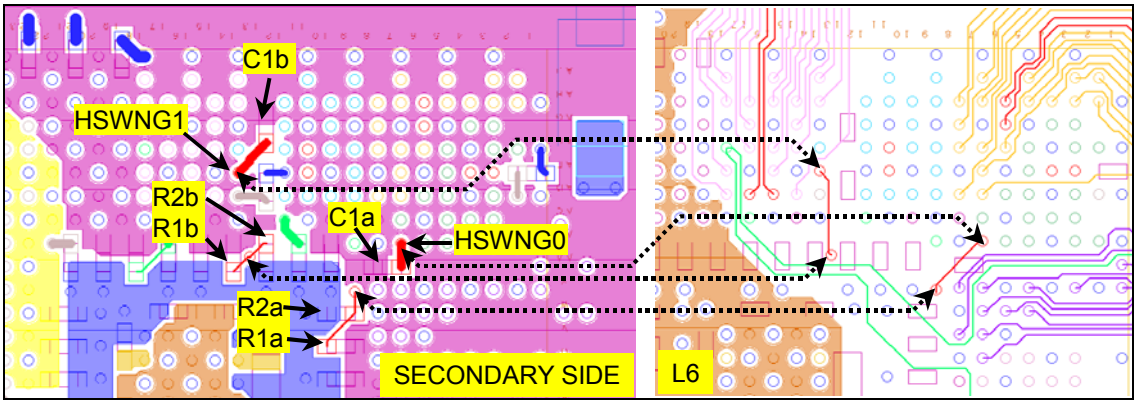


Figure 38 illustrates recommended layout for the HSWNG[1:0] components that are placed on the secondary side to minimize their interconnect length and space they occupy. In the example, C1a and C1b are placed closer to HSWNG pins than R1a, R1b, R2a, and R2b. It is important to keep only the connection of C1a and C1b to the HSWNG[1:0] with a 15-mil wide trace. The R1a (R1b) to R2a (R2b) connection can be done with a narrow trace as well as the connection to the pin that in the layout

example below is done by means of a via to Layer 6 and a short trace from the via to the dog bone via of HSWNG[1:0] pin as illustrated on the right side of Figure 38.

Figure 38. Intel 855PM MCH HSWNG[1:0] Layout



4.1.9. Processor FSB Strapping

The Intel Pentium M processor / Intel Celeron M processor and Intel 855PM MCH both have pins that require termination for proper component operation.

1. For the processor, a stuffing option should be provided for the TEST[3:1] pins to allow a 1-k ± 5% pull-down to ground for testing purposes. For proper processor operation, the resistor should not be stuffed. Resistors for the stuffing option on these pins should be placed within 2.0 inches of the processor. Figure 39 illustrates the recommended layout for the stuffing options. For normal operation, these resistors should not be stuffed.
2. For the MCH, the ST[1] signal does not require an external pull-up for normal operation. This signal has an internal pull-up that straps the FSB for 100-MHz operation. However, a stuffing option for a 1-k ± 5% pull-up to a 1.5-V source can be provided for testing purposes. For details on the ST[0] signal, refer to Section 6.3.
3. The processor's ITP signals, TDI, TMS, TRST and TCK should assume default logic values even if the ITP debug port is not used. The TDO signal may be left open or no connect in this case. Table 16 summarizes the default strapping resistors for these signals. These resistors should be connected to the processor within 2.0 inches from their respective pins. It is important to note that Table 16 is applicable only when neither the onboard ITP nor ITP interposer are planned to be used. See Section 4.2 on cautions against designs with lack of debug tools support. Intel does not recommend use of the ITP interposer debug port if there is a dependence only on the motherboard termination resistors. The signals below should be isolated from the motherboard via specific termination resistors on the ITP interposer itself per interposer debug port recommendations. For the case where the onboard ITP700FLEX debug port is used refer to Section 4.3 for default termination recommendations.

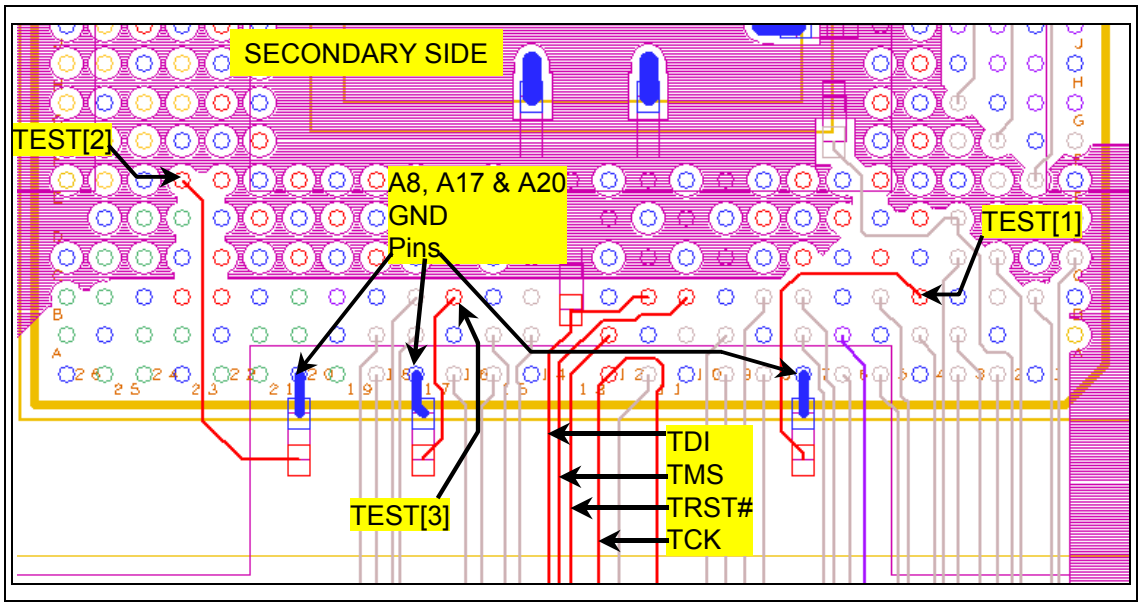
Table 16. ITP Signal Default Strapping When ITP Debug Port Not Used

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ± 5%	V_{CCP}	Within 2.0" of the CPU
TMS	39 ± 5%	V_{CCP}	Within 2.0" of the CPU
TRST#	680 ± 5%	GND	Within 2.0" of the CPU
TCK	27 ± 5%	GND	Within 2.0" of the CPU
TDO	Open	NC	N/A

Figure 39 illustrates the recommended layout for the processor's strapping resistors. To avoid interaction with FSB routing, the TEST[3:1] signal resistors are placed on the secondary side of the motherboard. To avoid GND via interaction with the FSB routing, the resistors share GND via connections with the A8, A17, and A20 ground pins of the processor.

The 150- pull-up resistor to V_{CCP} (1.05 V) for TDI is shown in Figure 39 on the secondary side of the board. The placement of the strapping resistors for TDI, TMS, TRST#, and TCK is not critical.

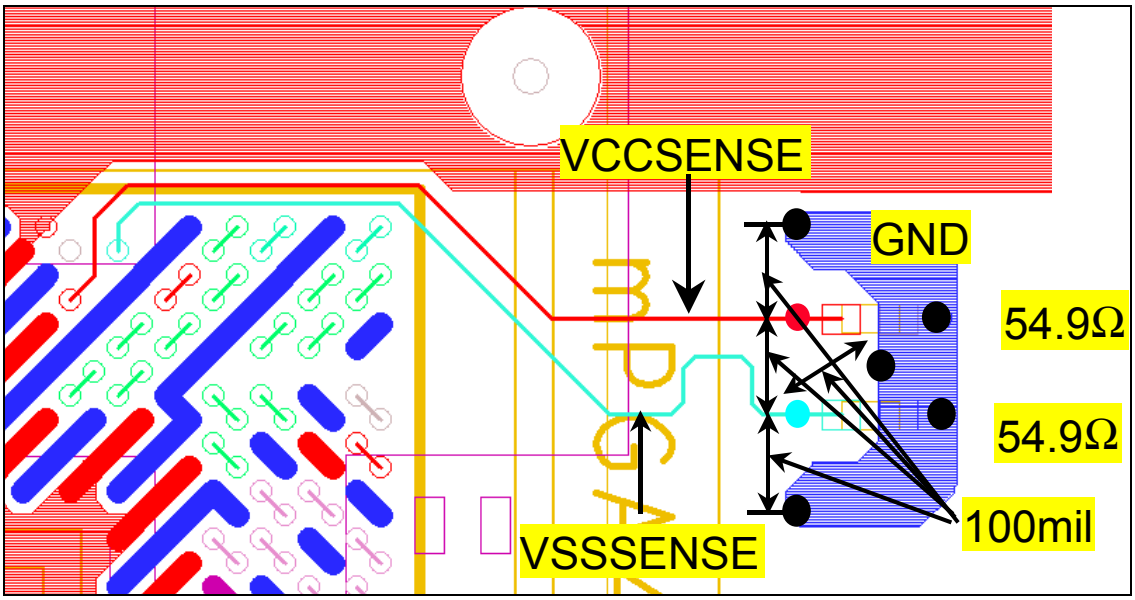
Figure 39. Processor Strapping Resistor Layout



4.1.10. Processor $V_{CCSENSE}/V_{SSSENSE}$ Design Recommendations

The VCCSENSE and VSSSENSE signals of the processor provide isolated, low impedance connections to the processor's core power (VCC) and ground (VSS). These pins can be used to sense or measure power (VCC) or ground (VSS) near the silicon with little noise. To make them available for measurement purposes, it is recommended that VCCSENSE and VSSSENSE both be routed with a Zo = 55 ± 15% trace of equal length. Use 3:1 spacing between the routing for the two signals and all other signals should be a minimum of 25 mils (preferably 50 mils) from VCCSENSE and VSSSENSE routing. Terminate each line with an optional (default is No Stuff) 54.9 ± 1% resistor. Also, a ground via spaced 100 mils away from each of the test point vias for VCCSENSE and VSSSENSE should be added. A third ground via should also be placed in between them to allow for a differential probe ground. See Figure 40 for the recommended layout example.

Figure 40. $V_{CCSENSE}/V_{SSSENSE}$ Routing Example



4.2. Intel System Validation Debug Support

In any PC design, it is critical to enable industry-standard tools to allow for debug of a wide range of issues that arise in the normal design cycle. In a mobile design, electrical/logic visibility is very limited, and often making progress on debugging such issues is very time consuming. In some cases progress is not possible without board redesign or extensive rework. Two topics in particular are very important to general system debug capabilities: ITP support and processor logic analyzer support (FSB LAI)

4.2.1. In Target Probe (ITP) Support

4.2.1.1. Background and Justification

The In Target Probe (ITP) is needed to debug BIOS, logic, signal integrity, general software, and general hardware issues involving CPUs, chipsets, SIOs, PCI devices, and other hardware in a design. The ITP is widely used by validation, test, and debug groups within Intel (as well as by third party BIOS vendors, OEMs, and other developers).

Note: Any Intel 855PM chipset based systems designed without ITP support may prevent assistance from various Intel validation, test, and debug groups. For this reason, it is critical piece that ITP support is provided. This can be done with zero additional BOM cost, and very minimal layout/footprint costs.

However, the cost for not providing this support can be anywhere from none (if there are no blocking issues found in the system design) to schedule slips of a month or more. The latter scenario represents the time needed to spin a board design and required assembly time to add an ITP port when it is absolutely required and other mechanical and routing issues prevent the use of an ITP interposer, if one exists.

4.2.1.2. Implementation

To minimize the ITP connector footprint, the ITP700FLEX alternative is a better option for mobile designs. Note that the termination values do not need to be stuffed (thus zero additional BOM cost). However, standard signal connection guidelines for the CPU's TAP logic signals for the non-ITP case still need to be followed. In other words, only the traces and component **footprints** need to be added to the design, with all previous "non-ITP" guidelines followed otherwise. This way, when ITP support is needed, the termination values and connector can be populated as needed for debug support. Note also that if the ITP700FLEX footprint cannot be followed due to mechanical, routing, or footprint reasons, it is acceptable to have a simple via grouping in lieu of the connector to allow for "blue-wiring" of the ITP. This assumes that all signal topology and routing guidelines are still adhered to on the motherboard and the "blue-wiring" from the signal vias to the ITP700FLEX connector is as short as possible.

4.2.2. Processor Logic Analyzer Support (FSB LAI)

4.2.2.1. Background and Justification

The second key tool that is needed to debug BIOS, logic, signal integrity, general software, and general hardware issues involving CPUs, chipsets, SIOs, PCI devices, and other hardware in platform design is the FSB Logic Analyzer probe (FSB LAI). This critical tool is widely used by various validation, test,

and debug groups within Intel (as well as by third party BIOS vendors, OEMs, and other developers). For the Intel Pentium M and Intel Celeron M processors, Agilent* Corporation will develop this tool and will likely be the only visibility to this critical system bus.

Note: Any Intel 855PM chipset based systems designed without FSB LAI support may severely limit the ability of various Intel validation, test, and debug groups from debugging various issues in a reasonable amount of time.

For this reason, it is critical that FSB LAI support is provided. There are two primary pieces to providing this support:

1. Providing a motherboard with a processor socket. The FSB LAI is an interposer that plugs into the CPU socket, and the CPU then plugs into the LAI. The use of non-standard sockets may also prohibit the LAI from working as the locking mechanism may become inaccessible. It is important to check the LAI design guidelines to ensure a particular socket will work. Note that the LAI was designed to accommodate the most common (and at the time the only known) Intel Pentium M processor sockets on the market.

2. Observing FSB LAI keepout requirements. There are several options to achieving this. Removing the motherboard from the case is typically the first step to meeting keepout requirements. If any components that would otherwise be in the keepout area can be relocated for debug purposes (i.e. axial lead devices that can be de-soldered and re-soldered to the other side of the board, parts that can be removed and blue-wired further away, etc.) that is also an acceptable method of meeting keepout requirements. If keepouts still can not be met, Intel strongly recommends that a separate debug motherboard be built which has the same bill of material (BOM) and Netlist, but with FSB LAI keepout requirements met (this also gives the opportunity to add other test-points).

4.2.2.2. Implementation

Details from Agilent* Corporation on the FSB LAI mechanicals (i.e. design guide with keepout volume info) are currently available for ordering. Please contact your local Intel field representative on how to obtain the latest design info. See Section 4.3.1.4 for more details.

4.2.3. Intel Pentium M Processor and Intel Celeron M Processor On-Die Logic Analyzer Trigger Support (ODLAT)

The Intel Pentium M and Intel Celeron M processor provides support for three address/data recognizers on-die for setting on-die logic analyzer triggers (ODLAT) or breakpoints. Details from American Arium* on the ODLAT are currently available for ordering.

4.3. Onboard Debug Port Routing Guidelines

For systems incorporating the Intel Pentium M and Intel Celeron M processors, the debug port should be implemented as either an onboard debug port or via an interposer. Please reference the document *ITP700 Debug Port Design Guide*, which can be found on http://www.intel.com/design/Xeon/guides/24967912.pdf, for the most up to date information.

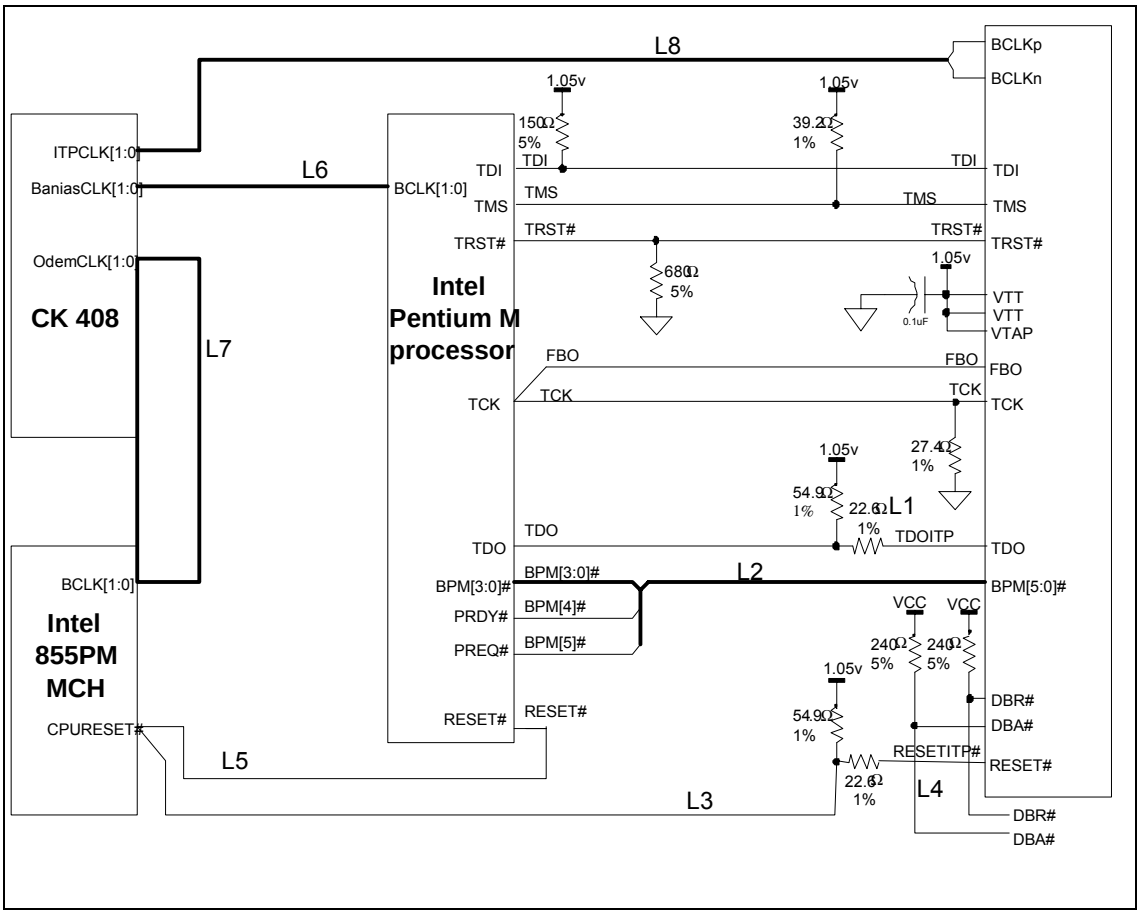
4.3.1. Recommended Onboard ITP700FLEX Implementation

4.3.1.1. ITP Signal Routing Guidelines

Figure 41 illustrates recommended connections between the onboard ITP700FLEX debug port, processor, Intel 855PM MCH, and CK-408 clock chip in the cases where the debug port is used.

For the purpose of this discussion on ITP700FLEX signal routing, refer to Section 4.1.1.4 for more details on the signal propagation time to distance relationships for the length matching requirements listed as periods of time below. It is understood that the time to distance relationships mentioned in Section 4.1.1.4 apply to the specific assumptions made only and it is the responsibility of the system designer to determine what is the appropriate length that correlates to the listed time periods as length matching requirements.

Figure 41. ITP700FLEX Debug Port Signals



To connect to the debug port, follow the steps below:

Route the TDI signal between the ITP700FLEX connector and the processor. A 150- ± 5% pull-up to V_{CCP} (1.05 V) should be placed within ± 300 ps of the TDI pin.

Route the TMS signal between ITP700FLEX connector and the processor. A 39.2- ± 1% pull-up to V_{CCP} should be placed within ± 200 ps of the ITP700FLEX connector pin.

Route the TRST# signal between ITP700FLEX connector and the processor. A 510- to 680- ± 5% pull-down to ground should be placed on TRST#. Placement of the pull down resistor is not critical. Avoid having any trace stub from the TRST# signal line to the termination resistor.

Route the TCK signal from the ITP700FLEX connector's TCK pin to the processor's TCK pin and then fork back from the processor's TCK pin and route back to ITP700FLEX connector's FBO pin. A 27.4- ± 1% pull-down to ground should be placed within ± 200 ps of the ITP700FLEX connector pin.

Route the TDO signal from the processor to a 54.9- ± 1% pull-up resistor to V_{CCP} that should be placed close to ITP700FLEX connector's TDO pin. Then insert a 22.6- ± 1% series resistor to connect the 54.9- pull-up and "TDOITP" net (see Figure 41). Limit the L1 segment length of the TDOITP net to be less than 1.0 inch.

The processor drives the BPM[4:0]# signals to the ITP700FLEX at a 100-MHz clock rate. Route the BPM[4:0]# as a Zo=55 point-to-point transmission line connection between the processor and the ITP700FLEX connector. Connect the ITP700FLEX connector's BPM[3:0]# pins to processor's BPM[3:0]# pins. Connect the ITP700FLEX's BPM[4]# signal to processor's PRDY# pin. The ITP700FLEX's integrated far-end terminations as well as the processor's AGTL+ integrated on-die termination guarantee proper signal quality for the BPM[4:0]# signals. Due to the length of the ITP700FLEX cable, the length L2 of the BPM[4:0]# signals on the motherboard should be limited to be shorter than 6.0 inches. The BPM[4:0]# signals' length L2 should be length matched to each other within ± 50 ps. The BPM[4:0]# signal trace lengths are matched inside the processor package, thus motherboard routing does **not** need to compensate for any processor package trace length mismatch.

Due to the processor's AGTL+ on-die termination for BPM[3:0]# and PRDY#, there is no issue or concern if the BPM[4:0]# pins of the ITP700FLEX connector are left floating when the ITP is not being used and the ITP700FLEX cable is unplugged.

Route the ITP700FLEX connector's BPM[5]# signal as a Zo = 55 point-to-point connection to the processor's PREQ# pin. Integrated on the ITP700FLEX BPM[5]# driver signal is a resistive pull-up that guarantees proper signal quality at the processor's PREQ# input pin. The processor has an integrated, weak, on-die pull-up to V_{CCP} for the PREQ# signal to guarantee a proper logic level when the ITP700FLEX port connector is not plugged in. There is no need for any external termination on the motherboard for the BPM[5]# = PREQ# signal. The maximum length of BPM[5]#/PREQ# should not exceed 6.0 inches.

As explained in Sections 4.1.5 and 4.1.5.1, the RESET# signal forks (see Figure 26) out from the Intel 855PM MCH's CPURST# pin and is routed to the processor and ITP700FLEX debug port. One branch from the fork connects to the processor's RESET# pin and the second branch connects to a 54.9 ± 1% termination pull-up resistor to V_{CCP} placed close to the ITP700FLEX debug port. A series 22.6 ± 1% resistor is used to continue the path to the ITP700FLEX RESET# pin with the RESETITP# net in Figure 41. The length of the RESETITP# net (labeled as net L4) should be limited to be less than 0.5 inches

There is no need for pull-up termination on the processor side of the RESET# net due to presence of AGTL+ on-die termination on the processor and the MCH.

The ITP700FLEX debug port's BCLKp/BCLKn inputs are driven with a 100-MHz differential clock from the CK-408 clock chip. The CK-408 also feeds another two pairs of 100-MHz differential clocks to the processor BCLK[1:0] and MCH BCLK[1:0] input pins. Common clock signal timing requirements of the MCH and the processor requires matching of processor and MCH BCLK[1:0] nets L6 and L7, respectively. To guarantee correct operation of ITP700FLEX, the BCLKp/BCLKn net L8 should be tuned to be within ± 50 ps to the sum of length L6 of the BCLK[1:0] lines and the additional length L2 of the BPM#[4:0] signals.

i.e. L6 + L2 = L8 (within ± 50 ps)

The timing requirements for the BPM[5:0]#, RESET#, and BCLKp/BCLKn signals of the ITP700FLEX debug port requires careful attention to their routing. Standard high frequency bus routing practices should be observed.

1. Keep a minimum of 2:1 spacing in between these signals and to other signals.
2. Reference these signals to ground planes and avoid routing across power plane splits.
3. The number of routing layer transitions should be minimized. If layout constraints require a routing layer transition, any such transition should be accompanied with ground stitching vias placed within 100mils of the signal via with at least one ground via for every two signals making a layer transition.

   DBR# should be routed to the system reset logic (e.g. the SYSRST# signal of the ICH4-M) and initiate the equivalent of a front panel reset commonly found in desktop systems. The 150- to 240- pull-up resistor should be placed within 1 ns of the ITP700FLEX connector. Note that the CPU should **not** be power cycled when DBR# is asserted.

   DBA# is an optional system signal that can be used to indicate to the system that the ITP/TAP port is being used. If not implemented, this signal can be left as no connect. If implemented, it should be routed with a 150- to 240- pull-up resistor placed within 1ns of the ITP700FLEX connector. See the *ITP700 Debug Port Design Guide* for more details on DBA# usage.

   The ITP700FLEX VTT and VTAP pins should be shorted together and connected to the V_{CCP} (1.05 V) plane with a 0.1-µF decoupling capacitor placed within 0.1 inch of the VTT pins.

Table 17 summarizes termination resistors values, placement, and voltages the ITP signals need to connect to for proper operation for onboard ITP700FLEX debug port.

Table 17. Recommended ITP700FLEX Signal Terminations

Signal	Termination Value	Termination Voltage	Termination/Decap Location	Notes
TDI	150 ± 5%	V_{CCP} (1.05 V)	Within ± 300 ps of the processor TDI pin	5
TMS	39.2 ± 1%	V_{CCP} (1.05 V)	Within ± 200 ps of the ITP700FLEX connector TMS pin	5
TRST#	510 – 680 ± 5%	GND	Anywhere between processor and ITP700FLEX connector	5
TCK	27.4 ± 1%	GND	Within ± 200 ps of the ITP700 FLEX connector TCK pin	5
TDO	54.9 ± 1% pull-up and 22.6 ± 1% series resistor	V_{CCP} (1.05 V)	Within 1" of the ITP700FLEX connector TDO pin	1, 5
BCLK(p/n)				2
FBO	Connect to TCK pin of CPU	N/A	N/A	1
RESET#	54.9 ± 1% pull-up and 22.6 ± 1% series resistor	V_{CCP} (1.05 V)	Within 0.5" of the ITP700FLEX connector RESET# pin	1
BPM[5:0]#	Not Required			3
DBA#	150-240 ± 5%	VCC of target system recovery circuit.	Within 1 ns of the ITP700FLEX connector DBA# pin	4
DBR#	150-240 ± 5%	VCC of target system recovery circuit	Within 1 ns of the ITP700FLEX connector DBR# pin	
VTAP	Short to V_{CCP} plane	V_{CCP} (1.05 V)		
VTT	Short to V_{CCP} plane	V_{CCP} (1.05 V)	Add 0.1-µF decap within 0.1 inch of VTT pins of ITP700FLEX connector	

NOTES:
1. See Figure 41.
2. Refer to Section 4.3.1.1.
3. All the needed terminations to guarantee proper signal quality are integrated inside the processor AGTL+ buffers or inside the ITP700FLEX debug port. No need for any external components for the BPM[5:0]# signals.
4. Only required if DBA# is used with any target system circuitry. This signal may be left unconnected if unused.
5. In cases where a system is designed to utilize the ITP700FLEX debug port for debug purposes but the ITP700FLEX connector may or may not be populated at all times although the signal routing and termination or decoupling components are implemented, the component placement guidelines should adhere to the ones listed in Table 17. However, for signals where the termination component placement guidelines for non-ITP700FLEX supported systems (see Table 16) are more restrictive or conservative than the component placement guidelines for the ITP700FLEX supported case, then the more conservative/restrictive guidelines should be followed.

4.3.1.2. ITP Signal Routing Example

Figure 43 illustrates a recommended layout example for the ITP700FLEX signals. The ITP700FLEX connector is placed on the primary side of the motherboard and results in a smooth, straight-forward routing solution.

Note that the V_{CCP} (1.05 V) power delivery continues from the processor socket cavity on the secondary side of the motherboard through the pin field as shown on the right side of Figure 43. Three V_{CCP} vias in conjunction with three ground stitching vias allow a transition to the primary side to connect to the VTT and VTAP pins of the ITP700FLEX connector and also a transition back to the secondary side of the

motherboard. A small V_{CCP} flood is created on the secondary side under the body of the ITP700FLEX connector with a 0.1-µF decoupling capacitor. This also provides a convenient connection for the two 54.9- pull-ups for RESET# and TDO signals as well as the 39.2- pull-up for the TMS signal.

Notice the very short trace from the 22.6- series resistors for the RESET# and TDO signals to the ITP700FLEX pins. See also Section 4.1.5.1 for more details of RESET# signal routing.

The 150- pull-up resistor for TDI is connected to the V_{CCP} (1.05 V) flood on the secondary side close to processor pin.

The ITP700FLEX TCK pin has a 27.4- pull-down to ground very close to the ITP700FLEX connector and also routes to the processor's TCK pin and loops back with no stub to the FBO pin of the ITP700FLEX connector.

BCLKp/BCLKn are routed in this example on Layer 3. For more BCLKp/BCLKn routing details, refer to Figure 28 in Section 4.1.6.

All other signals incorporate a straight forward routing methodology between the ITP700FLEX and processor pins.

4.3.1.3. ITP_CLK Routing to ITP700FLEX Connector

A layout example for ITP_CLK/ITP_CLK# routing to an ITP700FLEX connector is shown in Figure 42. The CK-408 clock chip is mounted on the primary side of the motherboard and the differential clock pair also breaks out on the same side. The differential ITP clock pair routing requires the use of a pair of 33- ± 5% series resistors placed within 0.5 inches of the clock chip output pins followed by a pair of 49.9- ± 1% termination resistors to ground. The ITP_CLK/ITP_CLK# signals route as a differential pair with a 4-mil trace width on 7-mil spacing from the junction of the 33- and 49.9- ± 5% resistors across the internal Layer 6 through an open channel to the ITP700FLEX connector. Serpentining of the ITP_CLK traces is also performed in order to meet the ± 50 ps length matching requirement between ITP_CLK and the sum of length L6 of the BCLK[1:0] lines and the additional length L2 of the BPM#[5:0] signals in Figure 41. The ITP_CLK pair routing then switches back to the primary side layer through a via near the ITP700FLEX connector.

Figure 42. ITP_CLK to ITP700FLEX Connector Layout Example

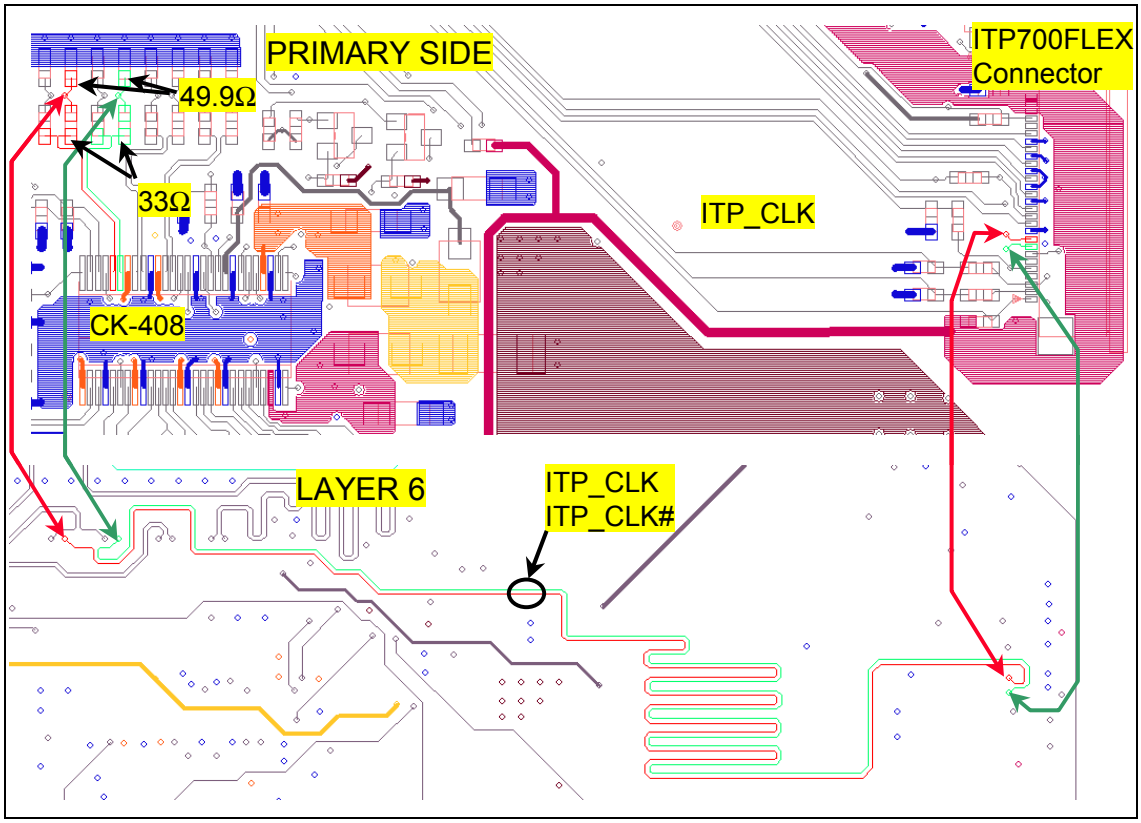
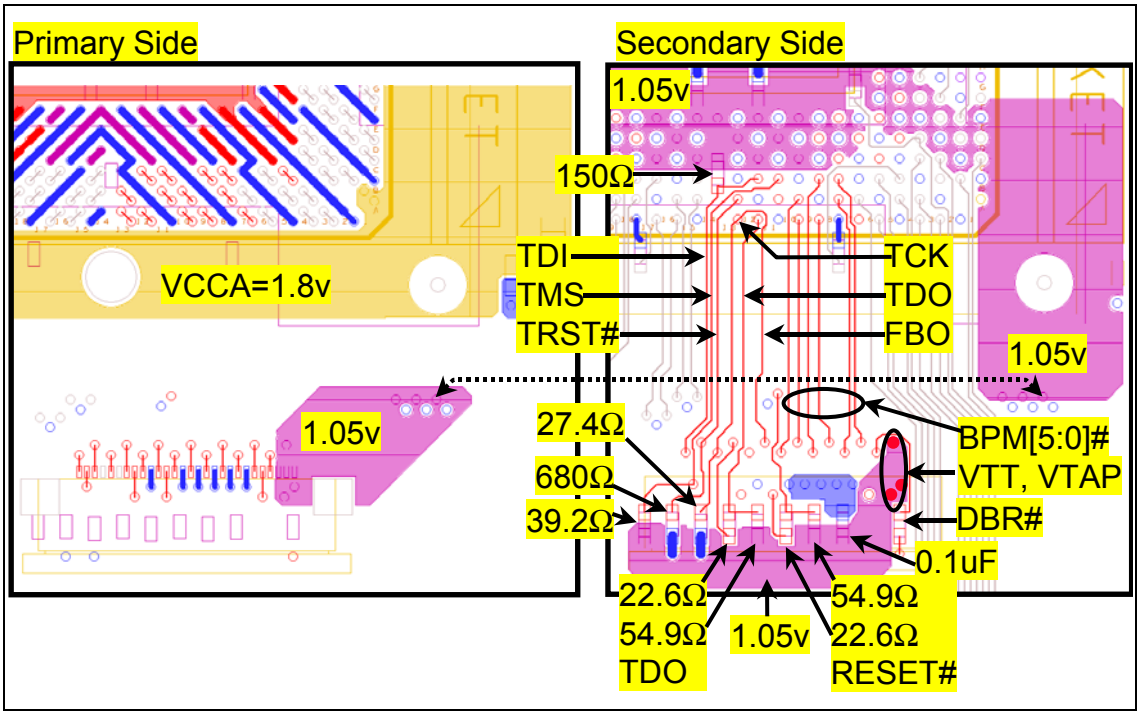


Figure 43. ITP700FLEX Signals Layout Example



4.3.1.4. ITP700FLEX Design Guidelines for Production Systems

For production systems that do not populate the onboard ITP700FLEX debug port connector, the following guidelines should be followed to ensure that all necessary signals are terminated properly.

Table 16 summarizes all the signals that require termination when a system does not populate the ITP700FLEX connector but still implements the routing for all the signals. This includes TDI, TMS, TRST#, and TCK. Based on the recommended values in this table, the resistor tolerances for TMS and TCK can be relaxed from ± 1% to ± 5% to reduce cost. Also, TDO can be left as a no connect, thus the 54.9 ± 1% pull-up and 22.6 ± 1% series resistors can be removed.

For the ITP700FLEX connector's RESET# input signal, it is only possible to depopulate the 22.6 ± 1% series resistor. The 54.9 ± 1% pull-up resistor is required for termination purposes if the routing for RESET# is not modified. RESET# would be a long, unterminated transmission line if the 54.9 ± 1% is not populated and could affect CPURST# signal quality and performance at the Intel 855PM MCH and the processor. If the routing for RESET# is removed or disconnected at the output of the MCH's CPURST# pin, then it is possible to also remove the 54.9 ± 1% resistor.

The series 33- and 49.9- ± 1% parallel termination resistors on the ITP_CLK/ITP_CLK# differential host clock inputs to the ITP700FLEX connector can also be depopulated for production systems. The only requirement is that the BIOS should disable the third differential host clock pair routed from the CK-408 clock chip to the ITP700FLEX connector.

Finally, the 150- to 240- pull-up resistor for the DBR# output signal from the ITP700FLEX connector may or may not be depopulated depending on how it affects the system reset logic that it is connected to. Thus, it is the responsibility of the system designer to determine whether termination for DBR# is required or not for a given system implementation. The same is also true for DBA#, if

implemented. It is the responsibility of the system designer to determine whether termination for DBA# is required or not.

4.3.2. Recommended ITP Interposer Debug Port Implementation

Intel is working with American Arium* to provide ITP interposer cards for use in debugging Intel Pentium M and Intel Celeron M processor based systems as an alternative to the onboard ITP700FLEX in cases where the onboard connector cannot be supported. The ITP interposer card is an additional component that integrates a processor socket along with ITP700 connector on a single interposer card that is compatible with the 478-pin Intel Pentium M processor / Intel Celeron M processor socket.

Table 16 summarizes all the signals that require termination for a system designed for use with the ITP interposer. This includes TDI, TMS, TRST#, and TCK. Also, TDO can be left as a no connect.

DBR# should be routed to the system reset logic (e.g. the SYSRST# signal of the ICH4-M) and initiate the equivalent of a front panel reset commonly found in desktop systems. The 150- to 240- pull-up resistor should be placed within 1ns of the ITP connector. Note that the processor should **not** be power cycled when DBR# is asserted.

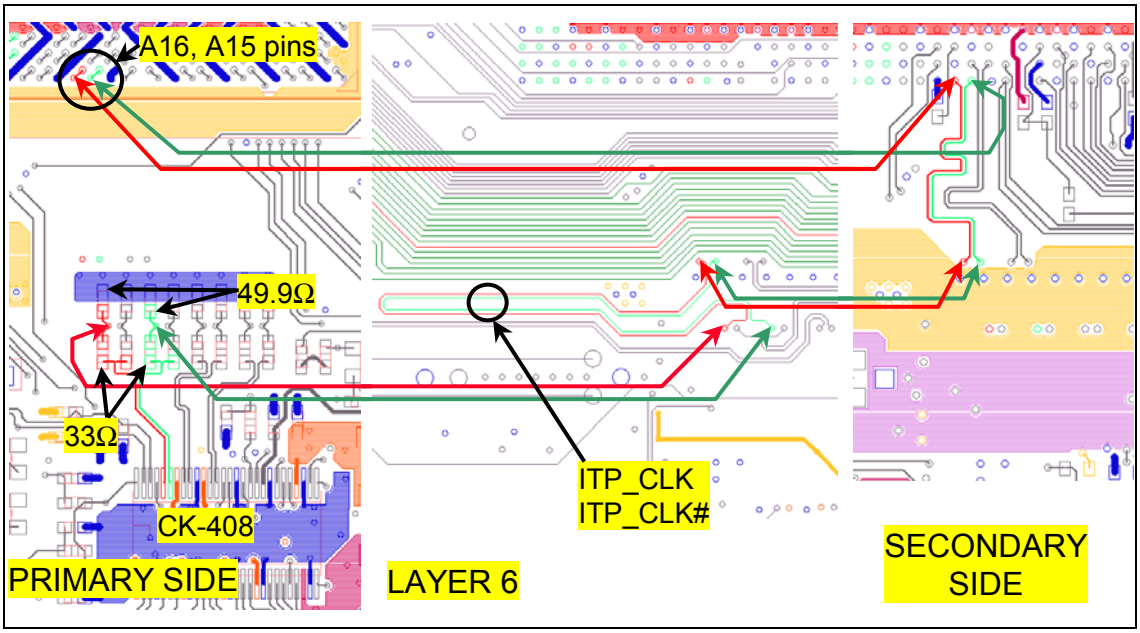
DBA# is an optional system signal that can be used to indicate to the system that the ITP/TAP port is being used. If not implemented, this signal can be left as no connect. If implemented, it should be routed with a 150- to 240- pull-up resistor placed within 1 ns of the ITP connector. See the *ITP700 Debug Port Design Guide* for more details on DBA# usage.

4.3.2.1. ITP_CLK Routing to ITP Interposer

A layout example for ITP_CLK/ITP_CLK# routing to the processor socket for supporting an ITP interposer is shown in Figure 44. The CK-408 clock chip is mounted on the primary side layer of the motherboard and the differential clock pair also breaks out on the same side. The differential ITP clock pair routing also requires the use of a pair of 33- ± 5% series resistors placed within 0.5 inches of the clock chip output pins and followed by a pair of 49.9- ± 1% termination resistors to ground. ITP_CLK/ITP_CLK# signals connect as a differential pair with 4-mil trace width on 7-mil spacing from the junction of the 33- and the 49- resistors. The majority of the ITP_CLK differential serpentine routing takes place on internal Layer 6 below the FSB address signal routing.

Completion of ITP_CLK routing on Layer 6 is not possible due to FSB routing on Layer 6. Therefore, the ITP_CLK differential pair then is routed to the secondary side layer to complete routing to the ITP_CLK (pin A16) and ITP_CLK# (pin A15) pins of the processor while matching the BCLK[1:0] routing on the secondary side for a 507-mil length (see Figure 28 and description in Section 4.1.6). Routing to the processor socket on the primary side layer is not possible because of the presence of the VCCA 1.8-V plane flood along the A signal side row of the pin-map. ITP_CLK routing to the ITP interposer should achieve the ± 50 ps length matching requirement of the BCLK[1:0] lines.

Figure 44. ITP_CLK to CPU ITP Interposer Layout Example



4.3.2.2. ITP Interposer Design Guidelines for Production Systems

For production systems that do not use the ITP interposer, the following guidelines should be followed to ensure that all necessary signals are terminated properly.

Table 16 summarizes all the signals that require termination when a system does not utilize the ITP interposer. This includes TDI, TMS, TRST#, and TCK. TDO can be left as a no connect.

The series 33 and 49.9 ±1% parallel termination resistors on the ITP_CLK/ITP_CLK# differential host clock inputs to the processor socket can also be depopulated for production systems. The only requirement is that the BIOS should disable the third differential host clock pair routed from the CK-408 clock chip to the Intel Pentium M processor / Intel Celeron M processor socket.

Finally, the 150- to 240- pull-up resistor for the DBR# output signal from processor socket may or may not be depopulated depending on how it affects the system reset logic that it is connected to. Thus, it is the responsibility of the system designer to determine whether termination for DBR# is required or not for a given system implementation. The same is also true for DBA#, if implemented. It is the responsibility of the system designer to determine whether termination for DBA# is required or not.

4.3.3. Logic Analyzer Interface (LAI)

Intel is working with Agilent* Corporation to provide logic analyzer interfaces (LAIs) for use in debugging Intel Pentium M/Intel Celeron M processor-based systems. LAI vendors should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of an Intel Pentium M/Intel Celeron M processor-based system, the LAI is critical in providing the ability to probe and capture FSB signals. There are two sets of considerations to keep in mind when designing an Intel Pentium M/Intel Celeron M processor-based system that can make use of an LAI: mechanical and electrical.

4.3.3.1. Mechanical Considerations

The LAI is installed between the processor socket and the Intel Pentium M/Intel Celeron M processor. The LAI pins plug into the socket, while the processor in the 478-pin package plugs into a socket on the LAI. Cabling this part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keep-out volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include space normally occupied by the processor heat sink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

4.3.3.2. Electrical Considerations

The LAI will also affect the electrical performance of the FSB. Therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications as load models for the LAI solution they provide.

4.4. Intel Pentium M Processor / Intel Celeron M Processor and Intel 855PM MCH FSB Signal Package Lengths

Table 18 lists the package trace lengths of the Intel Pentium M processor / Intel Celeron M processor and the Intel 855PM MCH for the source synchronous data and address signals. All the signals within the same group are routed to the same length as listed below with ± 0.1-mil accuracy. As a result of this package trace length matching, no motherboard trace length compensation is needed for these signals. Refer to Section 4.1.3 for further details. The processor and MCH package traces are routed as micro-strip lines with a nominal characteristic impedance of 55 ± 15%.

Table 18. Processor and MCH FSB Signal Package Trace Lengths

Signal Group	CPU Signal Name	Processor Package Trace Length (mils)	MCH Signal Name	MCH Package Trace Length (mils)
SOURCE SYNCHRONOUS – DATA & ADDRESS SIGNALS				
Data Group 1	D[15:0]#	722	HD[15:0]#	851
	DINV[0]#	722	DBI[0]#	851
	DSTBP[0]#	722	HDSTBP[0]#	851
	DSTBN[0]#	722	HDSTBN[0]#	851
Data Group 2	D[31:16]#	564	HD[31:16]#	958
	DINV[1]#	564	DBI[1]#	958
	DSTBP[1]#	564	HDSTBP[1]#	958
	DSTBN[1]#	564	HDSTBN[1]#	958
Data Group 3	D[47:32]#	661	HD[47:32]#	760
	DINV[2]#	661	DBI[2]#	760
	DSTBP[2]#	661	HDSTBP[2]#	760
	DSTBN[2]#	661	HDSTBN[2]#	760
Data Group 4	D[63:48]#	758	HD[63:48]#	709
	DINV[3]#	758	DBI[3]#	709
	DSTBP[3]#	758	HDSTBP[3]#	709
	DSTBN[3]#	758	H DSTBN[3]#	709
Address Group 1	REQ[4:0]#	616	HREQ[4:0]#	662
	A[16:3]#	616	HA[16:3]#	662
	ADSTB[0]#	616	HADSTB[0]#	662
Address Group 2	A[31:17]#	773	HA[31:17]#	686
	ADSTB[1]#	773	HADSTB[1]#	686
COMMON CLOCK SIGNALS				
	ADS#	454	ADS#	338
	BNR#	506	BNR#	536
	BPRI#	424	BPRI#	425
	BR0#	336	BREQ0#	329
	DBSY#	445	DBSY#	440

Signal Group	CPU Signal Name	Processor Package Trace Length (mils)	MCH Signal Name	MCH Package Trace Length (mils)
	DEFER#	349	DEFER#	544
	DPWR#	506	DPWR#	365
	DRDY#	529	DRDY#	627
	HIT#	420	HIT#	533
	HITM#	368	HITM#	611
	LOCK#	499	HLOCK#	611
	RS[0]#	576	RS[0]#	350
	RS[1]#	524	RS[1]#	467
	RS[2]#	451	RS[2]#	442
	TRDY#	389	HTRDY#	494
	RESET#	455	CPURST#	499
DIFFERENTIAL HOST CLOCKS				
Host Clocks	BCLK0	447	BCLK0	503
	BCLK1	447	BCLK1	503

5. Platform Power Requirements

5.1. General Description

The Intel Pentium M processor supports Enhanced Intel® SpeedStep® technology, which enables real-time dynamic switching of the voltage and frequency between multiple performance modes. This occurs by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system. With Enhanced Intel® SpeedStep® technology, there will be more than two modes of operation. The processor will be able to operate in more than two voltage levels. Although this specification addresses the highest processor core frequency and the lowest processor core frequency, there will be other modes where the voltage command may be different than that of these two modes. The Intel Celeron M processor does not support Enhanced Intel SpeedStep technology.

Terminology used to reference the names of the voltage rails are defined below.

$V_{CC-CORE}$ is the core rail of the processor

V_{CCP} is the FSB rail of the processor and MCH. Also used for CPU signals of ICH4-M chipset and CPU ITP700FLEX debug port if used

V_{CC-MCH} is the core rail of the MCH

5.2. Intel 855PM MCH Phase Lock Loop Power Delivery Design Guidelines

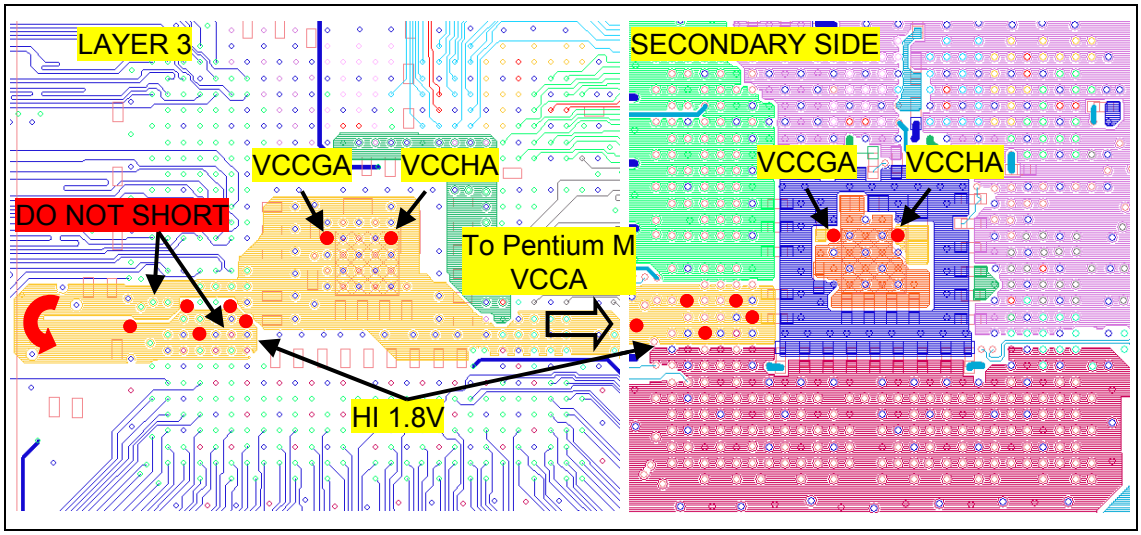
5.2.1. Intel 855PM MCH PLL Power Delivery

V_{CCGA} and V_{CCHA} are two pins on the Intel 855PM MCH that supply power to the PLL clock generators on the MCH silicon. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system; it degrades external I/O timings as well as internal core timings (i.e. maximum frequency). Traditionally these supply pins are low-pass filtered to prevent any performance degradation. The MCH has an internal super filter for the 1.8-V analog supply. Thus, the MCH does not require any external low-pass filtering for these power pins. However, one 10-nF 0603 form factor and one 10- F 1206 form factor decoupling capacitor should be placed as close as possible to the VCCGA and VCCHA pins. It is acceptable to share one of the capacitors from each of the listed types above for the two pins as long as a robust connection between the two pins is made. An example of such a connection is shown below. The VCCGA and VCCHA pins will share the 1.8-V power plane of the Hub Interface. However, it is advisable to connect the VCCGA and VCCHA pins with a separate flood that will “fork out” from the bulk decoupling capacitors of the HI 1.8 V power supplies and will route as a separate flood plane to the VCCGA and VCCHA pins without sharing the power delivery pins of the MCH Hub Interface’s 1.8 V. To minimize inductance and resistance parasitics, a flood with maximal width should be used along with 25-mil wide dog bone connections to vias that connect BGA lands on the primary side.

In Figure 45, the recommended power delivery layout and decoupling for VCCGA and VCCHA is shown. Notice on the left side of Figure 45 how the 1.8-V supply that powers the Hub Interface forks

from the bulk decoupling capacitor via on the secondary side layer also routes through Layer 3 as a separate branch to the 1.8-V flood that shorts the MCH VCCGA and VCCHA pins. The Hub Interface 1.8-V power delivery pin vias do not connect to the Layer 3 branch of the flood that feeds the VCCGA and VSSGA pins. The flood continues to the processor's VCCA[3:0] pins (1.8 V) on Layer 3, routing between the common clock and source synchronous address signal routing corridor as explained in Section 4.1.3.4, Figure 11, Figure 12, and Figure 13. The right side of Figure 45 illustrates that the VCCGA pin is connected with a small flood on the secondary side to a 10-nF 0603 form factor capacitor while the VCCHA pin with anther flood connects to a 1206 form factor 10-µF capacitor. Each of the capacitors connect through a via to a robust, wide 1.8 V flood of Layer 3 shown on the left side of Figure 45. The Layer 1 dog bone connection (not shown in Figure 45) should have a width of 25 mils for each of the VCCGA and VCCHA pins.

Figure 45. Intel 855PM MCH 1.8 V V_{CCGA} and V_{CCHA} Recommended Power Delivery



5.2.2. Intel 855PM MCH PLL Voltage Supply Power Sequencing

See Section 11.4.2 for more details on the platform power sequencing requirements for the 1.8-V supply to the processor and Intel 855PM MCH's PLLs.

5.3. Processor Phase Lock Loop Power Delivery Design Guidelines

5.3.1. Processor PLL Power Delivery

V_{CCA}[3:0] is a power source required by the PLL clock generators on the processor silicon. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e. maximum frequency). Traditionally this supply is low-pass filtered to prevent any performance degradation. The processor has an internal PLL super filter for the 1.8-V supply to the VCCA [3:0] pins that dispenses with the need for any external low-pass filtering. However, one 0603 form factor 10-nF and one 1206 form factor 10- F decoupling capacitor should be placed as close as possible to each of the four VCCA pins (i.e. a pair of capacitors consisting of one 10-nF and one 10- F should be used for each VCCA pin). VCCA power delivery should meet the 1.8 V ± 5% tolerance at the VCCA pins. As a result, to meet the current

demand of the processor and future Intel Pentium M/Intel Celeron M family processor, it is strongly recommended that the VCCA feed resistance from the 1.8 V power supply up to the VCCA shorting scheme described below be less than **0.1** . Intel recommends that the main VCCA feed be connected to the processor VCCA0 pin.

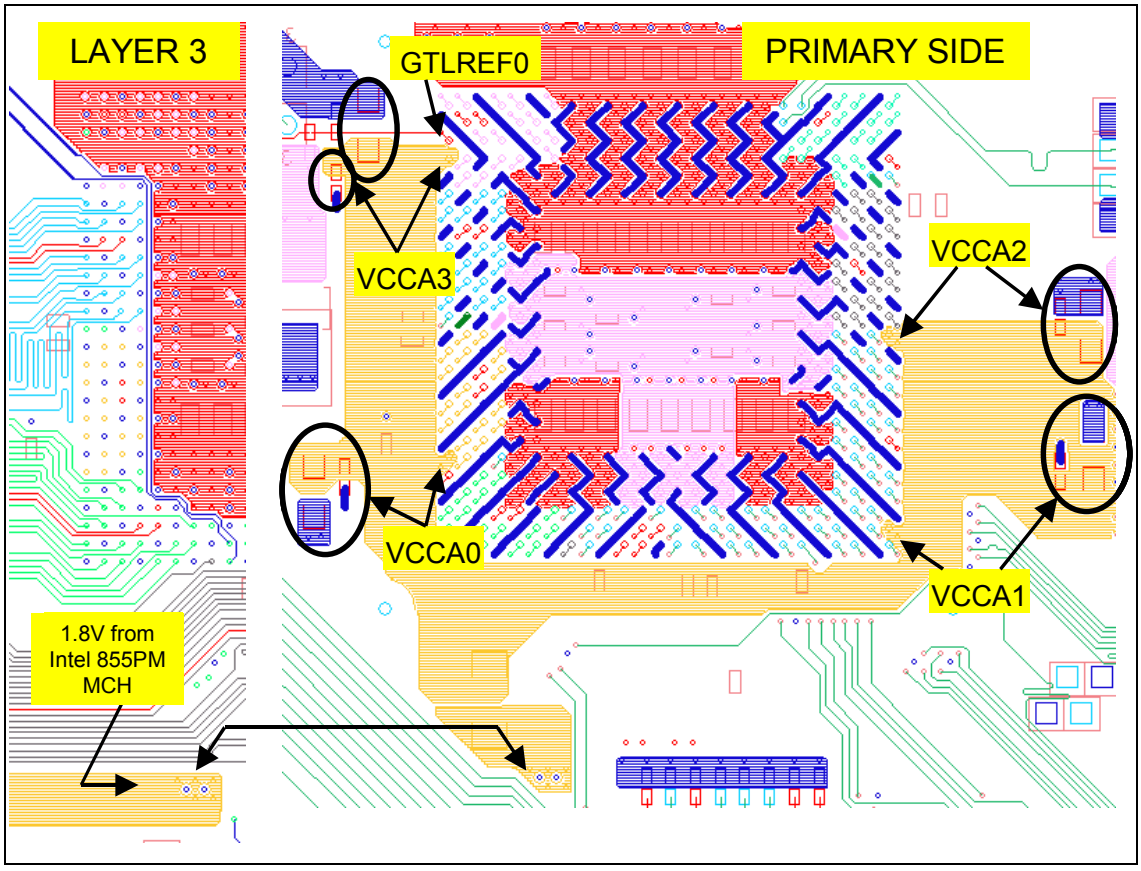
Figure 46 illustrates the recommended layout example of the VCCA[3:0] pins feed and decoupling. The 1.8-V flood on Layer 3 from Intel 855PM MCH is via'ed up to the primary side layer with a cluster of five 1.8-V vias and two GND stitching vias as shown on the left and middle side of Figure 46. On the primary layer side, a wide flood in a "U-Shape" shorts the four VCCA[3:0] pins of the processor. To minimize resistance and inductance of the "U-Shaped" VCCA flood shorting the VCCA[3:0] pins, the flood should be at least 100 mils wide and be spaced at least 25 mils from any switching signals. If possible, a flood wider than the 100-mil minimum should be implemented and should reference a ground plane only. Do not reference any switching signals or split planes. The recommended wide flood on the primary side benefits from low inductance connections to the VCCA[3:0] pins due to the close proximity of the Layer 2 solid ground plane 4 mils below the primary side 1.8-V flood. (Refer to the stack-up description in Figure 2.) Decoupling capacitors for pin VCCA3 are placed on the primary side in the vicinity of the GTLREF circuit (refer to Figure 30). No via is required to connect the VCCA3 side of the capacitors to the VCCA3 pin. The groundside of the VCCA3 capacitors has a small ground flood that is shared with the GTLREF circuit and connects to internal ground plane with two vias.

VCCA0 capacitors are also placed on the primary side. No via is needed on the VCCA0 side of the capacitors that connect to the VCCA0 pin. A small ground flood on the primary side shorts the ground side of the 1206 form factor 10- F VCCA0 decoupling capacitor via two GND stitching vias to minimize interaction with FSB routing. The 0603 form factor 10-nF VCCA0 decoupling capacitor connects to internal ground planes via a single GND stitching via.

VCCA1 decoupling capacitors are placed on the primary side on the bottom right corner of the processor socket. No via is required to connect the VCCA1 side of the decoupling capacitors to the VCCA1 pin. A small, ground plane connects the groundside of the 1206 form factor 10- F VCCA1 capacitors with a pair of vias to an internal ground plane. The 10- F decoupling capacitor connects to internal ground planes via a single GND stitching via.

The decoupling capacitors for VCCA2 are placed on the primary side on the right side of the processor socket. A small ground flood on the primary side is shared by the GND-side of the two required decoupling capacitors for VCCA2. Both the 10-nF and 10- F capacitors are placed in a vertical orientation on the primary side to avoid interaction with FSB routing and do not require vias on the VCCA2 side to connect to the VCCA2 pin.

Figure 46. Processor 1.8 V VCCA[3:0] Recommended Power Delivery and Decoupling



5.3.2. Processor PLL Voltage Supply Power Sequencing

See Section 11.4.2 for more details on platform power sequencing requirements for the 1.8-V supply to the processor and Intel 855PM MCH's PLLs.

5.3.2.1. Voltage Identification for Intel Pentium M/Intel Celeron M Processor

There are six voltage identification pins on the Intel Pentium M/Intel Celeron M processor. These signals can be used to support automatic selection of $V_{CC\text{-}CORE}$ voltages. They are needed to cleanly support voltage specification variations on current and future processors. VID[5:0] is defined in Table 19 below.

The VID[5:0] signals are 1.05-V CMOS level outputs. Intel recommends that 1:2 spacing and routing with a trace impedance of 55 ± 15% be used. No external termination is required for VID[5:0]. To guarantee signal quality, a point-to-point routing between the Intel processor and the VRM should be used. Figure 47 illustrates a signal escape routing example in the vicinity of the processor package outline. To allow for the coexistence of $V_{CC\text{-}CORE}$ and V_{CCP} power delivery routing as well as FSB signal routing, the VID[5:0] signals should utilize the remainder of the routing channels on Layer 3 (for VID2 and VID0), Layer 6 (for VID4), and Layer 8 (for VID1, VID3, and VID5).

Figure 47. Intel® Pentium® M Processor / Intel® Celeron® M Processor VID[5:0] Escape Routing Layout Example

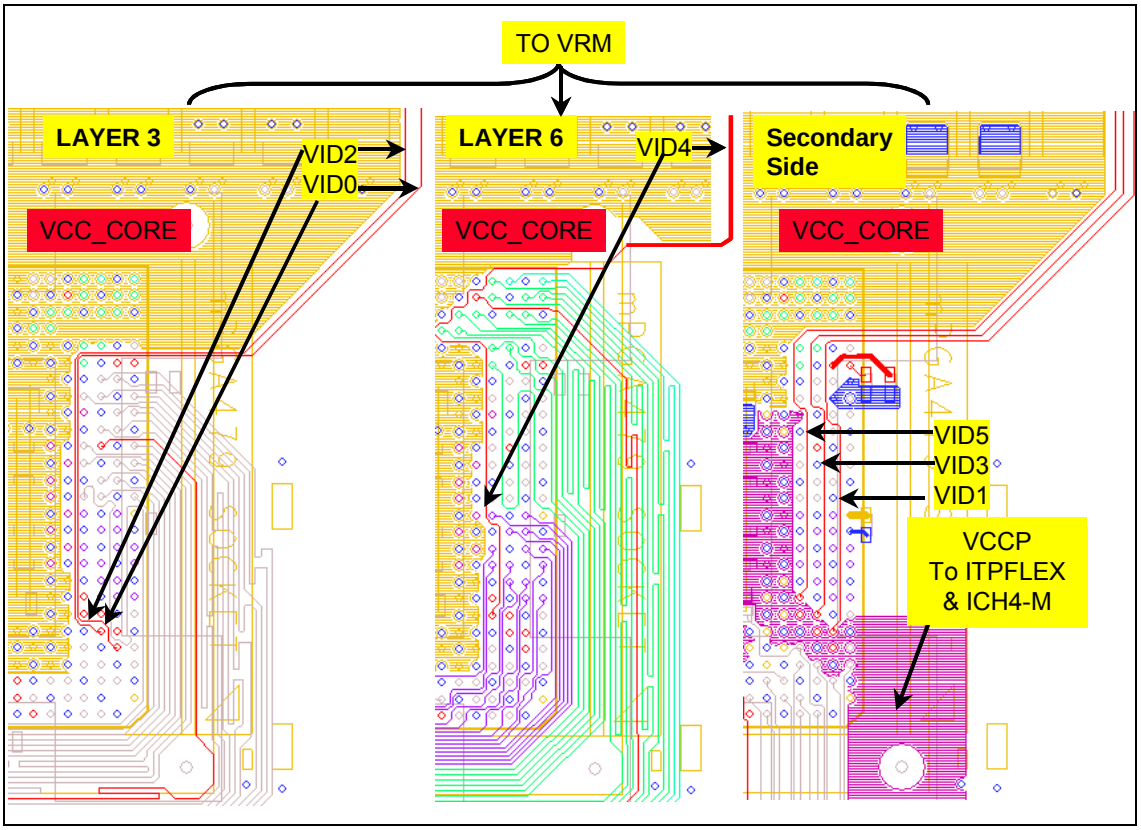


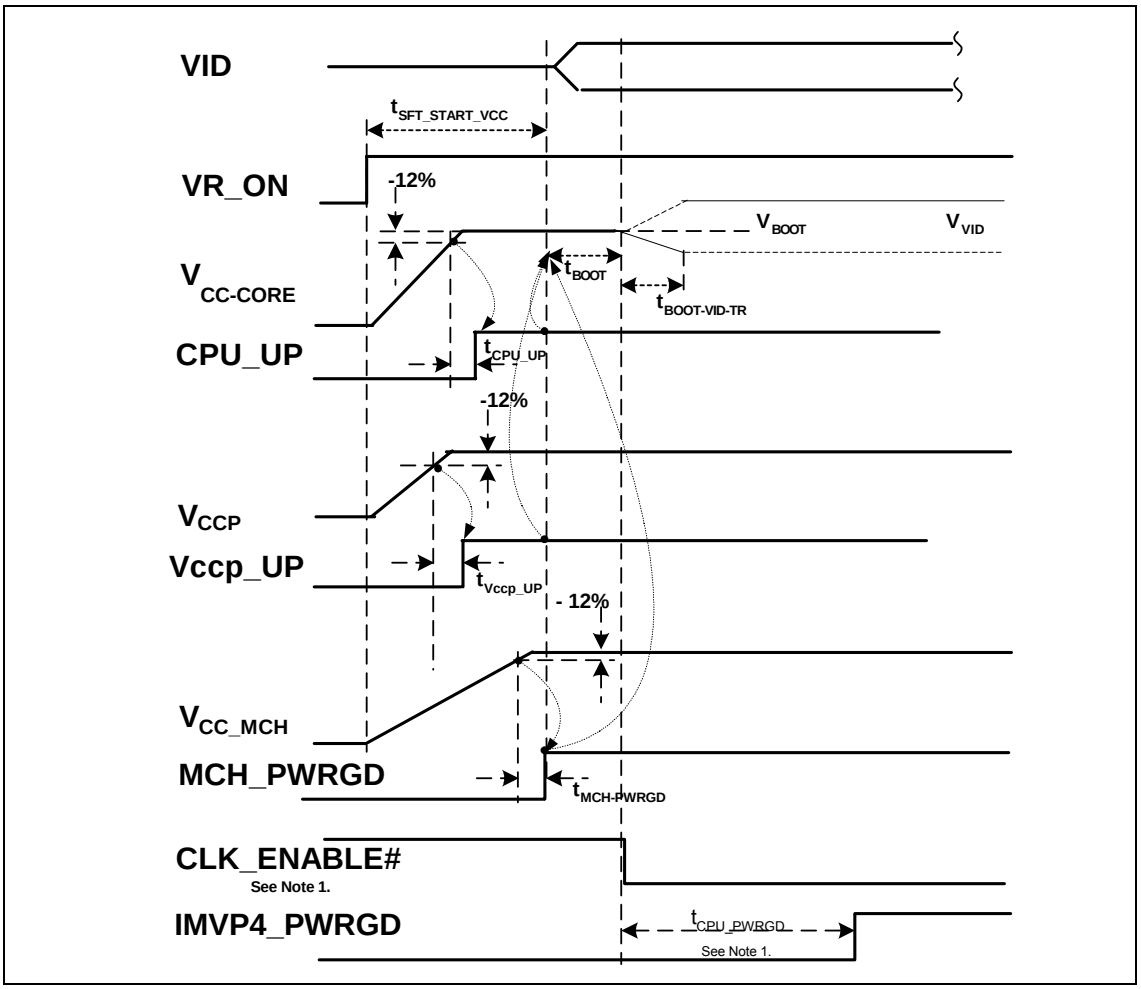
Table 19. VID vs. $V_{CC\text{-}CORE}$ Voltage

VID						$V_{CC\text{-}CORE}$	VID						$V_{CC\text{-}CORE}$
5	4	3	2	1	0	V	5	4	3	2	1	0	V
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

5.3.2.2. $V_{CC-CORE}$ Power Sequencing

There is only one enable pin, VR_ON, used to enable the outputs of the voltage regulator. When VR_ON is low, all output voltage rails ($V_{CC-CORE}$, V_{CCP}, and V_{CC_MCH}) are driven to a 0-V state. When VR_ON is high, V_{CCP}, V_{CC_MCH} and $V_{CC-CORE}$ are commanded ramp up at the same time. Figure 48 illustrates the power on sequencing timing.

Figure 48. Power On Sequencing Timing Diagram



NOTES:

1. Desired, but not required feature of a processor and chipset regulator controller. If not implemented by the controller, both the CLK_ENABLE# and the $t_{CPU-PWRGD}$ timer must be implemented by platform control logic.
2. Figure 48 depicts a number of signals that may or may not be platform visible.

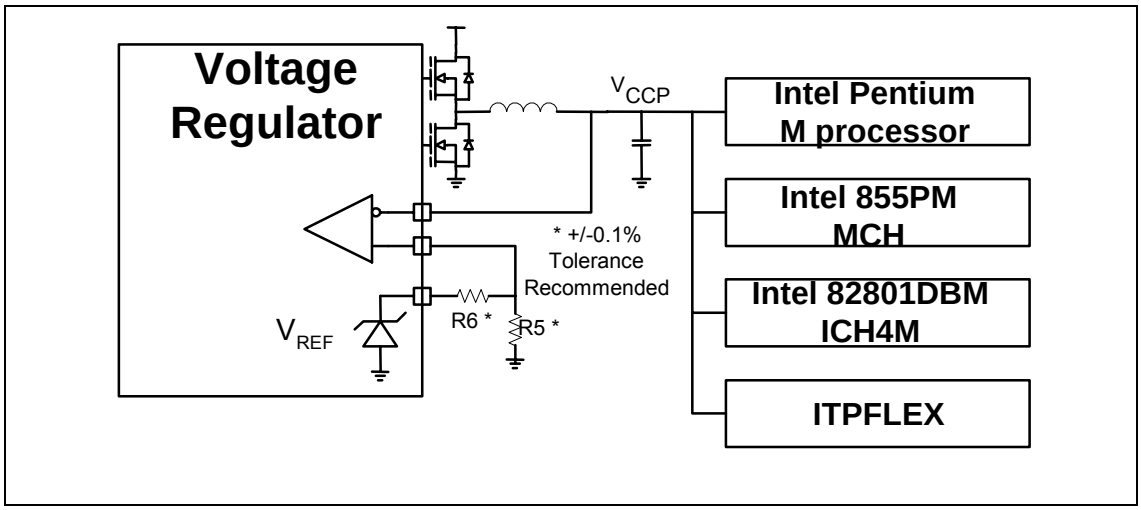
See Section 11.4 for platform power sequencing details and timing requirements.

5.4. V_{CCP} Output Requirements

The V_{CCP} output voltage rail provides power to the FSB rail for the Intel Pentium M/Intel Celeron M processor, the Intel 855PM MCH, the 82801DBM ICH4-M, and ITP700FLEX debug port if it is used. For the ICH4-M, this rail is known as V_{CPU_IO}. The voltage regulator can be programmed via an external

resistor network. See Figure 49. V_{REF} is used to set the highest output voltage in conjunction with the selection of R5 & R6 in the resistor network.

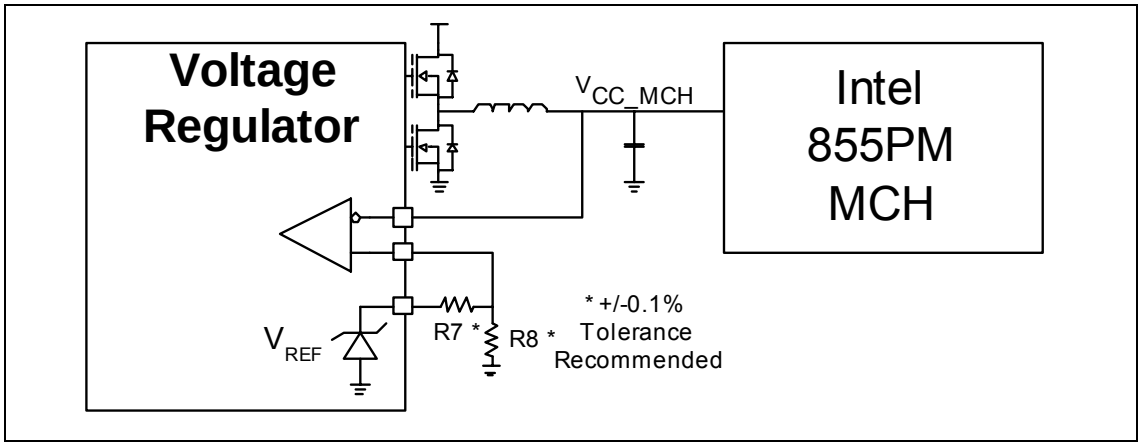
Figure 49. V_{CCP} Block Diagram



5.5. V_{CC-MCH} Output Requirements

The V_{CC-MCH} output rail provides power to the core of the Intel 855PM MCH. The nominal voltage of V_{CC-MCH} is 1.2 V. The voltage regulator can be programmed via an external resistor network. See Figure 50. V_{REF} is used to set the highest output voltage in conjunction with the selection of R7 and R8 in the resistor network..

Figure 50. V_{CC-MCH} Block Diagram



5.6. Thermal Power Dissipation

Power dissipation has traditionally been a thermal/mechanical challenge for mobile system designers. The amount of current required from the processor power delivery circuit and the heat generated by processors has increased as processor frequencies go up and the silicon process geometry shrinks. The package of any integrated device can only dissipate so much heat into the surrounding environment. The

temperature of a device, such as a processor power delivery circuit-switching transistor, is a balance of heat being generated by the device and its ability to shed heat either through radiation into the surrounding air or by conduction into the circuit board. Increased power will effectively raise the temperature of the processor power delivery circuits. Switching transistor die temperatures can exceed the recommended operating value if the heat cannot be removed from the package effectively.

As the current demands for higher frequency and performance processors increases, the amount of power dissipated, *i.e.*, heat generated, in the processor power delivery circuit has become of concern for mobile system, thermal, and electrical design engineers. The high input voltage, low duty factor inherent in mobile power supply designs leads to increasing power dissipation losses in the output stage of the traditional buck regulator topology used in the mobile industry today.

These losses can be attributed to three main areas of the processor power delivery circuit. The switching MOSFET dissipates a significant amount of power during switching of the top control MOSFET, power dissipation resulting from drain to source resistance ($R_{DS(ON)}$) DC losses across the bottom synchronous MOSFET, and the power dissipation generated through the magnetic core and windings of the main power inductor.

There has been significant improvement in the switching MOSFET technology to lower gate charge of the control MOSFET allowing them to switch faster thus reducing switching losses. Improvements in lowering the $R_{DS(ON)}$ parametric of the synchronous MOSFET have resulted in reduced DC losses. The Direct Current Resistance (DCR) of the power inductor has been reduced, as well, to lower the amount of power dissipation in the circuit's magnetic.

These technology improvements by themselves are not sufficient to effectively remove the heat generated during the high current demand and tighter voltage regulation required by today's mobile processors. There are several mechanisms for effectively removing heat from the package of these integrated devices. Some of the most common methods are listed below.

- Attaching a heat spreader or heat pipe to the package with a low thermal co-efficient bonding material
- Adding and/or increasing the copper fill area attached to high current carrying leads
- Adding or re-directing air flow to flow across the device
- Utilize multiple devices in parallel, as allowed, to reduce package power dissipation
- Utilizing newer/enhanced technology and devices to lower heat generation but with equal or better performance.

For the mobile designer, these options are not always available or economically feasible. The most effective method of thermal spreading and heat removal, from these devices, is to generate airflow across the package AND add copper fill area to the current carrying leads of the package.

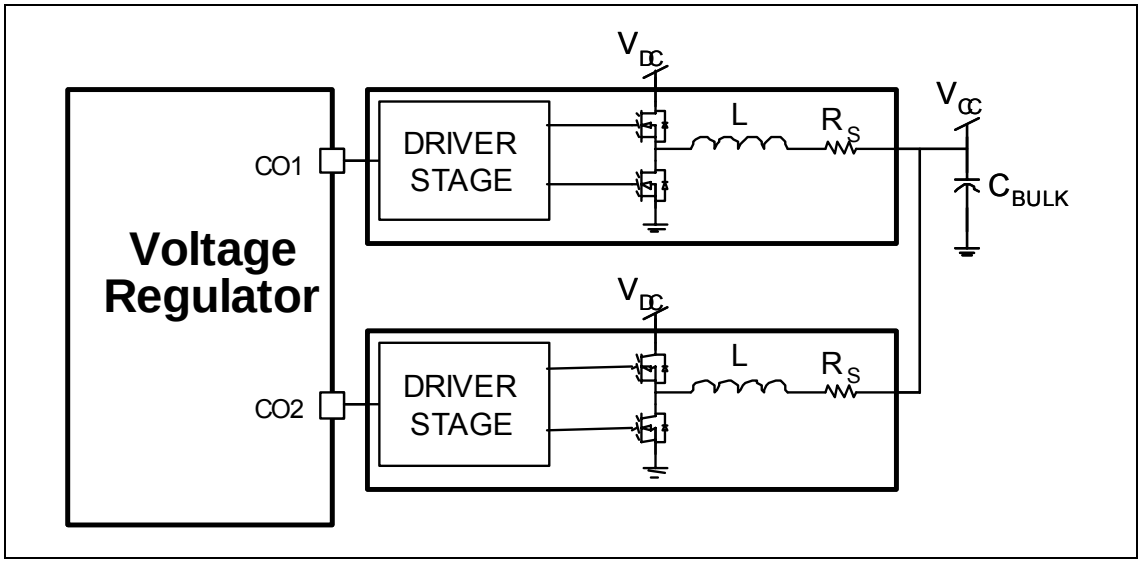
The processor power delivery topology can also be modified to improve the thermal spreading characteristic of the circuit and dramatically reduce the power dissipation requirements of the switching MOSFET and inductor. This topology referred to as multi-phase, provides an output stage of the processor regulator consisting of several smaller buck inductor phases that are summed together at the processor. Each phase can be designed to handle and source a much smaller current. This can reduce the size, quantity, and rating of the components needed in the design. This can also decrease the cost and PCB area needed for the total solution. The implementation options for this topology are discussed in the next section.

5.7. Voltage Regulator Topology

In a single-phase topology, the duty cycle of the Control (top) MOSFET is roughly the ratio of the output voltage and the input voltage. Due to the small ratio between $V_{CC\text{-}CORE}$ and V_{DC}, the duty cycle of the Control MOSFET is very small. The main power loss in the Control MOSFET is therefore due to the transition or switching loss as it switches on and off. To minimize the transition loss in the Control MOSFET, its transition time must be minimized. This is usually accomplished with the use of a small-size MOSFET. Or similarly, the duty cycle of the Synchronous MOSFET is very large; hence, to minimize the DC loss of the Synchronous MOSFET, its $R_{DS\text{-}ON}$ must be small. This is usually accomplished with the use of a large-size MOSFET or several small-size MOSFETs connected in parallel, but this solution usually leads to shoot-through current as it is quite difficult to minimize the effect of the Gate-Glitch phenomenon in the Synchronous MOSFET due to C_{GD} charge coupling effect. It is, therefore, necessary to go to multi-phase topology. In a multi-phase topology, the output load current is sourced from multiple sources or output stages. The term multi-phase implies that the phases or stages are out of phase with respect to each other. For example, in a dual-phase topology, the stages are exactly 180 output of phase.

Refer to Figure 51 for a block diagram for a dual-phase topology.

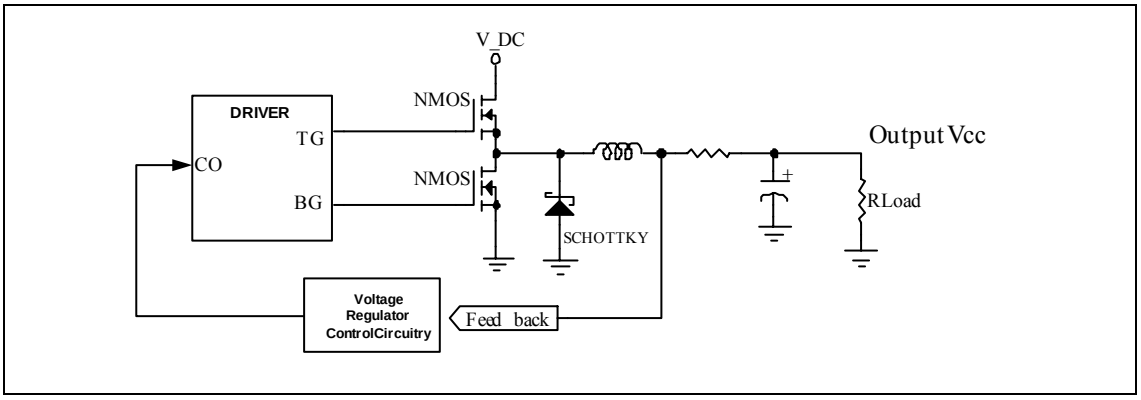
Figure 51. Voltage Regulator Multi-Phase Topology Example



5.8. Voltage Regulator Design Recommendations

When laying out the processor power delivery circuit using a traditional Buck Voltage Regulator on a printed circuit board, the following checklist should be followed.

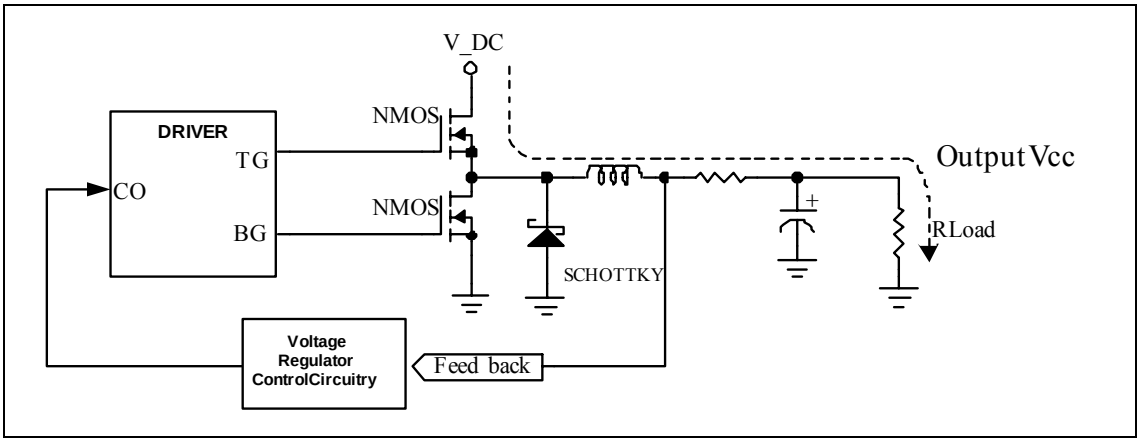
Figure 52. Buck Voltage Regulator Example



5.8.1. High Current Path, Top MOSFET Turned ON

The dashed/arrow line in Figure 53 indicates the high current path when the top MOSFET is ON. Current flows from the V_DC power source, through the top MOSFET (There may be more than one of these.), through the inductor and sense resistor and finally through the processor, R_{Load}, to ground. The components and current paths shown must be able to not only carry the high current through the processor, but the power source and ground must also be adequate.

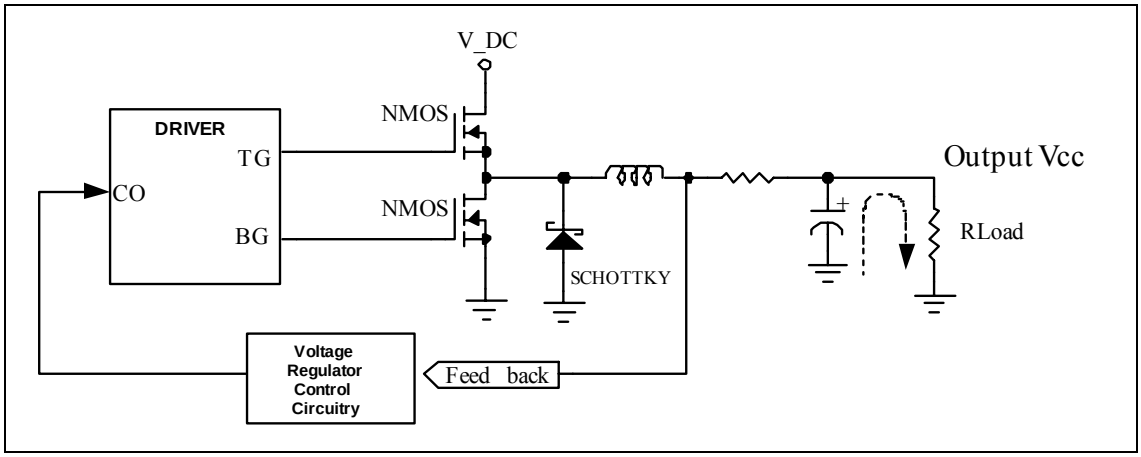
Figure 53. High Current Path With Top MOSFET Turned ON



5.8.2. High Current Paths During Abrupt Load Current Changes

During abrupt changes in the load current, the bulk and decoupling capacitors must supply current for the brief period before the regulator circuit can respond. The dashed/arrow line in Figure 54 illustrates this current path. Stray inductance and resistance become a major concern and if they are not minimized, they can compromise the effectiveness of the capacitors. Bulk capacitors for Vcc should be located at the highest current density points. These high-density points are located along the shortest route between the processor core and the sense resistor. Using short, fat traces or planes can minimize both stray inductance and resistance.

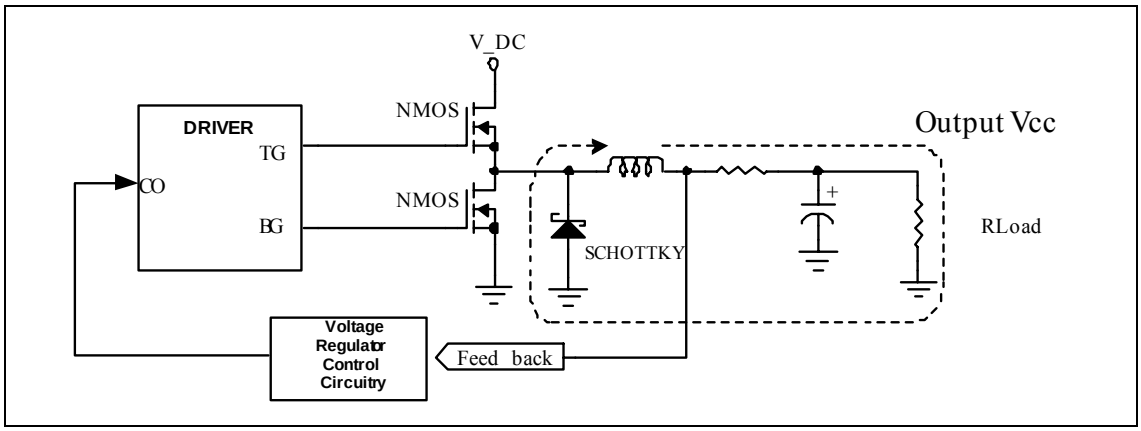
Figure 54. High Current Path During Abrupt Load Current Changes



5.8.3. High Current Paths During Switching Dead Time

When the top MOSFET turns OFF and before the bottom MOSFET (again there may be more than one of these.) is turned ON, The pattern of current flow changes. The inductor is no longer being supplied current through the top MOSFET starts to collapse its magnetic field. The inductor literally becomes a generator, at this point. The dashed/arrow line in Figure 55 shows the current path during the time that both top and bottom MOSFETs are OFF. This is termed "Dead Time." During Dead Time there is a high current flow through the inductor, processor, ground, and the Schottky diode. The diode and its traces must be laid out in such as to minimize both stray inductance and resistance with short, fat traces or planes.

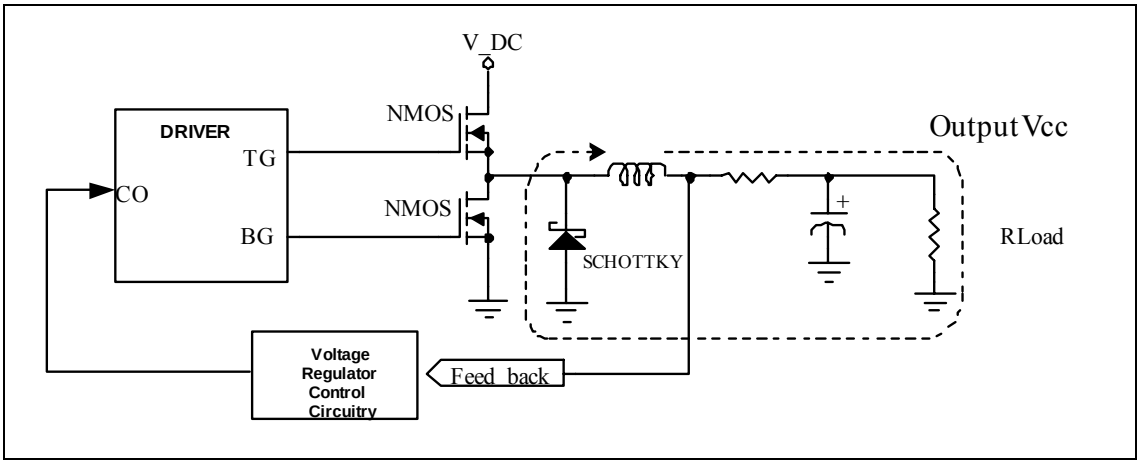
Figure 55. High Current Path with Top and Bottom MOSFETs Turned Off (Dead Time)



5.8.4. High Current Path with Bottom MOSFET(s) Turned ON

A few nanoseconds after the top MOSFET is turned OFF, the bottom MOSFET(s) is turned ON. The high current path now switches from the Schottky diode to the bottom MOSFET(s), the current path shown by the dashed/arrow line in Figure 56. Minimize stray inductance and resistance with short, fat traces or planes.

Figure 56. High Current Path With Bottom MOSFET(s) Turned ON



5.8.5. General Layout Recommendations

All the components in the high current paths dissipate some power, i.e., they get warm when current runs through them. To minimize temperature rise and facilitate thermal spreading, large copper fill areas connecting the high current components is imperative. For example, the MOSFET manufacturers recommend that each MOSFET be mounted on one square inch of two-ounce copper. While this may not be possible in the mobile environment, this recommendation serves to illustrate the importance of thermal considerations in the Switching Regulator layout.

Bulk capacitors for Vcc need three vias per pad if vias are not shared. Clusters of bulk and bypass capacitors may be clustered along the high current paths between the sense resistor and the processor. Clusters may have copper fill areas between capacitors. This provides additional opportunities for vias – do not stop at three.

Some controllers sense the load on Vcc by monitoring the voltage drop across the sense resistor with a Kelvin connection. The two feedback traces do not handle a high current, but must be of equal lengths to get an accurate load measurement. Connect the feedback signal traces as close as possible to both ends of the sense resistor. While the feedback traces do not handle high current, they are high impedance and susceptible to interference from electrical and magnet noise. Avoid routing these traces near the power inductor and avoid routing through vias.

The sense resistor is to be placed as close to the inductor as possible, followed by the first two bulk capacitors.

The lead frame in the power MOSFETs is used to dissipate heat. To do this each of the power MOSFETs requires 1 square inch of copper.

Avoid ground loops as they pick up noise. Use star or single point grounding. The source of the lower (Synchronous bottom MOSFET) is an ideal point where the input and output ground planes can be connected.

Keep the inductor-switching node small by placing the output inductor, switching top MOSFET and synchronous Bottom MOSFETs close together on the same copper fill.

The MOSFET enable/gate traces to the Driver must be as short (less than 1 inch), straight, and wide as possible (20 to 25 mils). Ideally, the driver has to be placed right next to the MOSFETs. Circuits using multiple top or bottom MOSFETs need to have the gate traces serpentined so the all

the traces going to the top MOSFETs Gates and most especially the bottom MOSFETs gates are the same length.

Use the bulk capacitors and use multiple layer traces with heavy copper to keep the parasitic resistance low. Use a minimum of three vias per connection on each bulk capacitor.

Place the top MOSFET drains as close to the VDC-input capacitors as possible.

The sense resistor has to be wide enough to carry the full load current. A minimum of 1 via per Amp to the Vcc plane should be used. Use more if space permits.

Use solid 2-oz. copper fill under Drain and Source connections of the Top and Bottom MOSFETs.

The voltage regulator is usually left to the last moment. Often the allocated area is too small, a narrow strip and the location poor. These factors combine so that the design flow, described above usually cannot be followed.

General Rule: Copper Fill is Good. Fill the PCB with metal. There should be no large areas of the board without metal. Widen the Grounds, Vcc and other power rails to fill any blank spots. Large metal fill areas allow the voltage regulator to improve its heat radiation thus run cooler. Large copper fill areas have other benefits too, including reducing stray resistance and inductance, capturing and dissipating RF energy by allowing eddy currents to flow.

5.9. Processor Decoupling Recommendations

Intel recommends proper design and layout of the system board bulk and high frequency decoupling capacitor solution to meet the transient tolerance at the processor package balls. To meet the transient response of the processor, it is necessary to properly place bulk and high frequency capacitors close to the processor power and ground pins.

5.9.1. Transient Response

The inductance of the motherboard power planes slows the voltage regulator's ability to respond quickly to a current transient. Decoupling a power plane can be partitioned into several independent parts. The closer to the load the capacitor is placed, the more stray inductance is bypassed. By bypassing the inductance of leads, power planes, etc., less capacitance is required. However, areas closer to the load have less room for capacitor placement and therefore, tradeoffs must be made.

The processor causes very large switching transients. These sharp surges of current occur at the transition between low power states and the normal operating states. The system designer must provide adequate high frequency decoupling to manage the highest frequency components of the current transients. Larger bulk storage capacitors supply current during longer lasting changes in current demand.

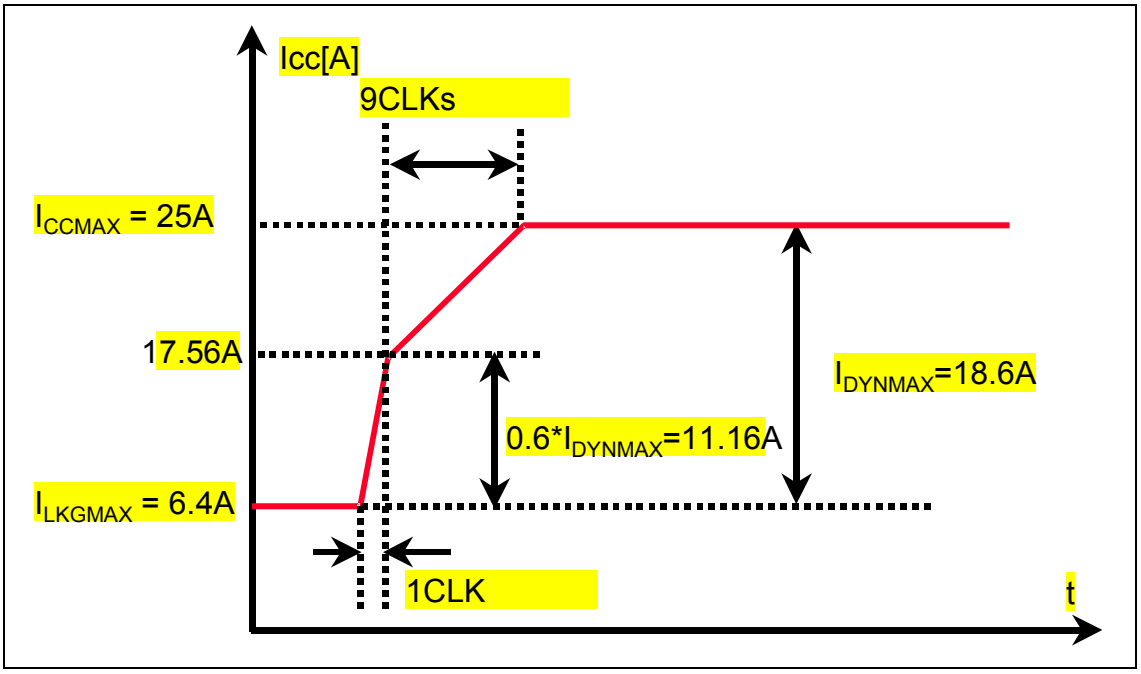
All of this power bypassing is required due to the relatively slow speed at which a DC-to-DC converter can respond. A typical voltage converter has a reaction time on the order of 1 to 100 s while the processor's current steps can be at shorter than 1 ns. High Frequency decoupling is typically done with ceramic capacitors with a very low ESR. Because of their low ESR, these capacitors can act very quickly to supply current at the beginning of a transient event. However, because the ceramic capacitors are small, i.e. they can only store a small amount of charge, thus Bulk capacitors are needed too. Bulk capacitors are typically polarized with high capacitance values and unfortunately higher ESLs and ESRs. The higher ESL and ESR of the Bulk capacitor limit how quickly it can respond to a transient event. The Bulk and high frequency capacitors working together can supply the charge needed to stay in regulator before the regulator can react during a transient.

A load change transient occurs when coming out of or entering a low power state. These are not only quick changes in current demand, but also long lasting average current requirements. This occurs when the processor enters different power modes by stopping and starting it's internal clock. The processor current requirements can change by as much as 60% of the maximum current very quickly.

The estimated Intel® Pentium® M Processor / Intel® Celeron® M Processor worst-case current consumption change waveform is illustrated in Figure 57. This figure illustrates the expected waveform seen at the die bumps of the CPU. Due to the presence of decoupling capacitors, it is expected that the ramp rates of the current would slow down as seen by the motherboard's high frequency and bulk decoupling capacitors.

In Figure 57, worst-case leakage current is estimated to be 6.4 A. When the clock starts to toggle, current consumption in one clock may change instantaneously, up to 60% of the estimated dynamic current consumption of 18.6 A; thus, reaching a current of 17.56 A. After that initial step, the current may ramp continually within 9 clocks; thus, reaching an estimated I_{CCMAX} of 25 A. It should be noted that current consumption of Intel Pentium M processor and Intel Celeron products may be lower than what is shown in Figure 57. However, to guarantee the suitability of the motherboard and VRM design for future, higher frequency products the $V_{CC\text{-}CORE}$ design should be able to meet the current requirements of Figure 57.

Figure 57. Estimated Processor Current Consumption Change During STPCLK Exit



5.9.2. High Frequency, Mid Frequency, and Bulk Decoupling

System motherboards should include high and mid frequency and bulk decoupling capacitors as close to the socket power and ground pins as possible. Decoupling should be arranged such that the lowest ESL devices (0612 reverse geometry type, if used for some of the recommended options below) are closest to the processor power pins followed by the 1206 devices (if used), and finally, bulk electrolytics (organic covered tantalum or aluminum covered capacitors). System motherboards should include bulk-decoupling capacitors as close to the processor socket power and ground pins as possible. The layout example shown in Section 5.9.3 should be followed closely. Table 20 lists the recommended decoupling

solutions for $V_{CC-CORE}$, while Table 21 and Table 22 list the recommended decoupling solutions for the V_{CCP} and V_{CC_MCH} supply rails, respectively. Also, see decoupling solutions for the $V_{CC-CORE}$ (section 5.9.3), V_{CCP} (section 5.9.4) , and V_{CC_MCH} (section 5.9.5) supply rails in the design guide. .

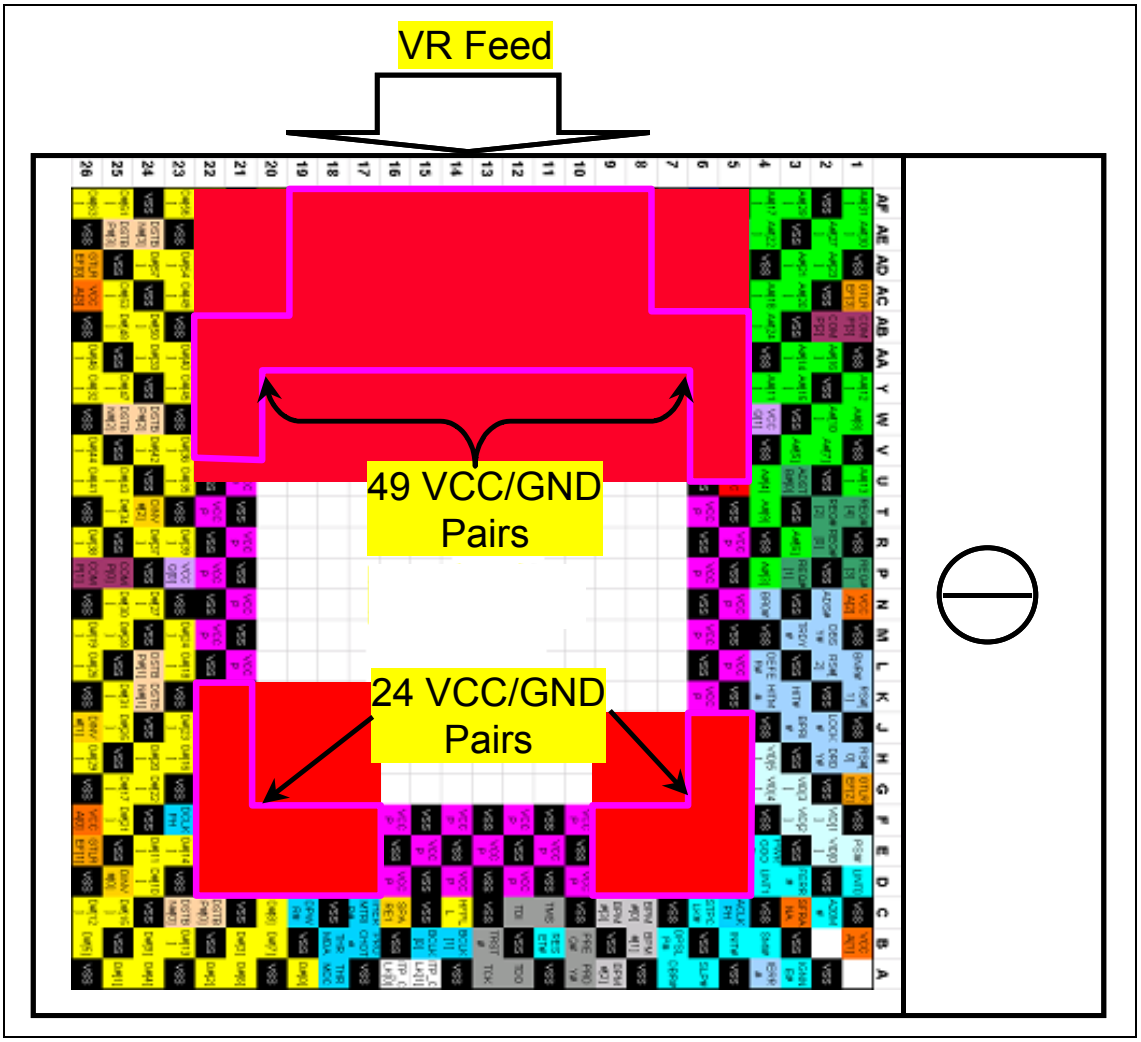
5.9.3. Processor Core Voltage Plane and Decoupling

Due to the high current (up to 25 A) requirements of the processor core voltage, the $V_{CC-CORE}$ is fed from the VRM by means of multiple power planes that provide both low resistance and low inductance paths between the voltage regulator, decoupling capacitors, and processor $V_{CC-CORE}$ pins. To meet the $V_{CC-CORE}$ transient tolerance specifications for the worst-case stimulus shown in Figure 57, the maximum Equivalent Series Resistance (ESR) of the decoupling solution should be equal to or less than 3 m .

Figure 2 (see Section 3.1) shows an example of a motherboard power plane stack-up that allows for both robust, high frequency signals routing and robust $V_{CC-CORE}$ power delivery.

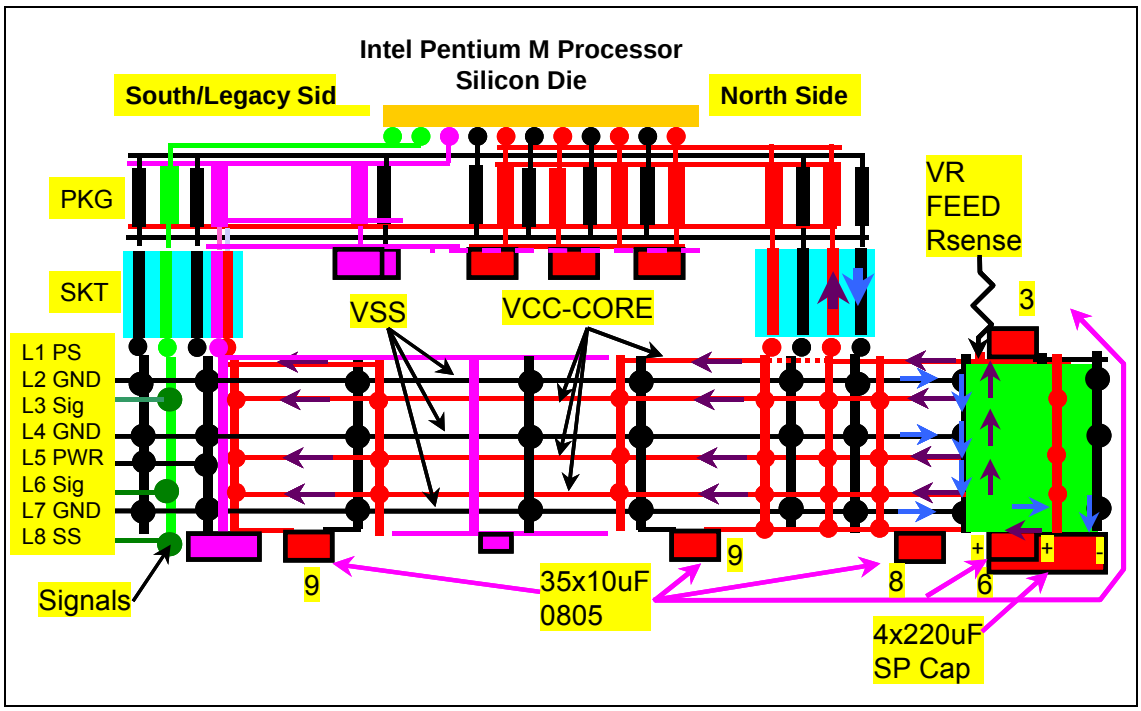
The processor pin-map is shown in Figure 58 for reference in the discussion below. Note the highlighted $V_{CC-CORE}$ power delivery corridor pins concentrated on the north side of the pin-map that contains forty-nine $V_{CC-CORE}$/GND pin pairs while the south side of the socket contains only 24 $V_{CC-CORE}$/GND pin pairs. Since access to the 24 south side pin pairs is blocked by the legacy signals, the only option available for providing robust core power delivery to the processor is by placing the VRM and most of the decoupling capacitors to the north of the core power delivery corridor (found on the north side of the forty-nine $V_{CC-CORE}$/GND pin pairs). It is advised to not feed the VR from any other side other than this $V_{CC-CORE}$ corridor on the north side of the processor socket. Due to the high current demand, all the $V_{CC-CORE}$ and ground vias of the processor pin-map should have vias that are connected to both internal and external power planes. Sharing of vias between several $V_{CC-CORE}$ pins or ground pins is not allowed.

Figure 58. Intel Pentium M Processor and Intel Celeron M ProcessorSocket Core Power Delivery Corridor



A conceptual diagram of this $V_{CC\text{-}CORE}$ power delivery scheme is shown in Figure 59.

Figure 59. Processor Core Power Delivery and Decoupling Concept



In this example, bulk-decoupling 220- F SP capacitors (according to $V_{CC\text{-}CORE}$ recommended decoupling guidelines) are placed on the north side of the secondary side layer in the processor $V_{CC\text{-}CORE}$ power delivery corridor. Notice the VRM feed point (sense resistor connection) is on the positive terminal side of the 220- F SP capacitors. Both $V_{CC\text{-}CORE}$ and ground vias are used on both sides of the SP capacitors' positive terminal side in order to reduce the inductance of the capacitor connection as illustrated by the current flow loop area in Figure 59. If the VR feed is on the negative side of the SP capacitors then both $V_{CC\text{-}CORE}$ and GND stitching vias will be needed on both the positive and negative terminals of the capacitor to reduce the effective inductance of the capacitor.

Layers 1 (primary side layer), 3, 5, 6, and (secondary side layer) 8 are used for $V_{CC\text{-}CORE}$ current feeding while referencing Layers 2, 4, and 7 (ground planes) with a small dielectric separation (see Figure 2 in Section 3.1). These layers are solid ground planes in the areas under the processor package outline and where the decoupling capacitors are placed. This results in a reduction in effective loop inductance. For the recommended layout examples shown in Figure 59, Figure 60, Figure 61, and Figure 62, a low inductance value of ~41 pH is achieved. Bulk decoupling capacitors respond too slowly to handle the fast current transients of the processor. For this reason, 0805 mid frequency decoupling capacitors are added on the primary and secondary side. Some are placed under the package outline of the processor while the rest are placed in the periphery of the processor along the AF signal row of the pin-map where a majority of the $V_{CC\text{-}CORE}$ power pins are found. A 4-mil power plane separation between the secondary side power plane flood and Layer 7 ground while using the 0805 capacitors significantly reduces the inductance of these capacitors. Results from a 3D field solver simulation suggest that an ESL of 600-pH per capacitor can be used to help achieve the specific layout style described above. The ESL of the 0805 capacitors is a very critical parameter, thus the layout style shown in the recommendation below should be closely followed. To stress the importance of 0805 capacitors that result in an ESL of 600 pH, it can be compared to ~1.2 nH ESL for 1206 form factor capacitors. Please note that the 0805 capacitors have $V_{CC\text{-}CORE}$ and ground vias on both negative and positive terminals similar to the 220- F SP capacitors in order to achieve a low inductance connection.

The motivation for concentrating the majority of the 0805 mid/high frequency decoupling capacitors and all of the SP-type bulk decoupling capacitors on the secondary side layer is to take advantage of the $V_{CC-CORE}$ corridor that establishes a robust connection from the VRM feed to the decoupling capacitors. On the primary side, the dog bone via connections for the $V_{CC-CORE}$ pins and ground pins effectively separate the $V_{CC-CORE}$ plane flood into multiple, relatively narrow strips separated by alternating Vss dogbones. These narrow floods that feed the inner $V_{CC-CORE}$ pins of the processor are non-ideal and for this reason, robust connections to capacitors are performed on the secondary side. Only three of the mid-frequency decoupling capacitors need to be placed on the primary side.

Table 20 lists the decoupling solutions recommended by Intel for the processor's $V_{CC-CORE}$ voltage rail. The solution offers the benefits of robust electrical performance, comparable efficiency, minimal cost, minimal motherboard surface area requirements, and lowest acoustic noise. It is a polymer-covered aluminum and ceramic-decoupling capacitor based solution that implements 4 polymer covered aluminum (SP type) capacitors that have a low ESR of 12 m each. It also uses 35 x 10 µF 0805 MLCC mid frequency decoupling capacitors. Substitution of the 0805 capacitors with 1206 or other capacitors with higher inductance is not allowed.

Table 20. $V_{CC-CORE}$ Decoupling Guidelines[1]

Description	Cap (µF)	ESR (m	ESL (nH)
Low Frequency Decoupling (Polymer Covered Aluminum – SP Cap, AO Cap	4 x 220 µF	12 m (max) / 4	2.5 nH / 4
Mid Frequency Decoupling (0805 MLCC, >= X6R)	35 x 10 µF	5 m (typ) / 35	0.6 nH / 35

NOTES:

1. $V_{CC-CORE}$ decoupling guidelines are recommended to be used with small footprint (100 mm^2 or less) 0.36 H ± 20% inductors.

An example layout implementation of the recommended VCC_{-CORE} decoupling guidelines is illustrated in Figure 60, Figure 61, and Figure 62 below. Figure 60 and Figure 61 show how the four, low frequency SP decoupling capacitors are placed on the secondary side and connected to the AF signal row of the processor pins with a solid $V_{CC-CORE}$ flood area along with eight of the mid frequency 0805 ceramic decoupling capacitors that are in between. To minimize the inductance of the SP capacitor connection for the layout style shown, the sense resistors' VRM feed is on the positive terminal side of the SP capacitors. In this case each of the SP capacitors are connected to two pairs of $V_{CC-CORE}$/GND vias on the positive terminal. See Figure 61 for more details. If the VRM sense resistors connect from the negative side of the SP capacitors, then two pairs of $V_{CC-CORE}$/GND vias will be needed on both positive and negative terminals of the SP capacitors.

Thirty-two, 10-µF, 0805 capacitors are placed on the secondary side (Layer 8) while the remaining three are placed on the primary side (Layer 1). Six of the 10-µF capacitors are placed outside the socket outline with a 90-mil (or closer) pitch (see Figure 61) and are divided evenly on either side for the four, 220-µF bulk capacitors (three to the left and three to the right of the SP capacitors). Each of these six 0805 capacitors have a pair of $V_{CC-CORE}$ and GND stitching vias next to both positive and negative terminals of the capacitors. The stitching vias connect to the internal ground and $V_{CC-CORE}$ planes, respectively.

The eight, 10-µF, 0805 capacitors (see Figure 61) that are located in between the SP capacitors and the processor $V_{CC-CORE}$ "north corridor" pins also have a pair of $V_{CC-CORE}$ and GND stitching vias on both sides of their terminals. The negative terminals share $V_{CC-CORE}$ and GND stitching via connections with the six 0805 ceramic and SP capacitors mentioned above. The positive terminal $V_{CC-CORE}$ and GND stitching connections are shared with the "north corridor" and ground pins of the AF signal row of the

processor socket. To allow good current flow from the SP capacitors to the north side of the $V_{CC-CORE}$ corridor pins, Intel recommends that these eight, 10- F 0805 capacitors be spaced 100 mils apart from each other even if the motherboard design rules allow tighter spacing. The 100-mil horizontal spacing allows some $V_{CC-CORE}$ flood in between the capacitor ground pads (as illustrated in Figure 61) as well as additional connections to internal Layers 3, 5, and 6 as illustrated in Figure 62. An additional nine, 10-µF, 0805 capacitors are placed along the Y signal row of the processor pins on the secondary side below the $V_{CC-CORE}$ "north corridor" pins under the shadow of the socket cavity. These nine capacitors are spaced 90 mils apart. Each of these nine 0805 capacitors have a pair of $V_{CC-CORE}$ and GND stitching vias next to both their positive and negative terminals. The stitching vias connect to the internal ground and $V_{CC-CORE}$ planes respectively. The positive terminal $V_{CC-CORE}$ and GND stitching vias are shared with the AA signal row of the processor's $V_{CC-CORE}$ and ground pins. A wide $V_{CC-CORE}$ power delivery corridor flood on the secondary side of the motherboard connects the 0805 ceramic and SP capacitors that are placed to the north of the processor socket and the nine capacitors that are placed under the shadow of the socket cavity on the secondary side. The flood is as wide as the whole AF signal row and should connect to all the $V_{CC-CORE}$ pins in signal rows Y, W, V, and U as illustrated in Figure 61.

The remaining nine (out of thirty-two) 10- F, 0805 (see Figure 60) capacitors are on the secondary side are used to decouple the remainder of the twenty-four $V_{CC-CORE}$/GND pin pairs on the south side of the processor socket. These capacitors are placed along signal row G of the processor pins with a 90-mil (or smaller) pitch. Each of the nine capacitors has a pair of $V_{CC-CORE}$ and GND stitching vias on both sides of their terminals. Five out of nine capacitors share positive terminals with $V_{CC-CORE}$ and GND stitching via connections with signal row F's $V_{CC-CORE}$ and GND pins. The remaining four capacitors are placed next to the V_{CCP} pins of signal row F and have their own $V_{CC-CORE}$ vias but do share GND stitching vias.

As shown on the secondary side of Figure 60, a wide $V_{CC-CORE}$ flood connects the positive terminal of these nine capacitors to all twenty-four $V_{CC-CORE}$ pins of the processor pin-map on the south side including the $V_{CC-CORE}$ pins of signal rows K, J, H, and G. The reason for interruption of the $V_{CC-CORE}$ flood on the secondary side between the north and south sides is to allow the V_{CCP} corridor connection between the DATA and ADDR sides of the processor socket.

The primary side view in Figure 60 depicts two wide $V_{CC-CORE}$ floods that connect from the $V_{CC-CORE}$ stitching vias of the nine capacitors next to their negative terminal to the $V_{CC-CORE}$ pins of the two clusters of the twenty-four $V_{CC-CORE}$ pins in rows K, J, H, G, F, E, and D of the processor pin-map. Note the specific arrangement of the vias for the $V_{CC-CORE}$ dog bones to allow connection of all $V_{CC-CORE}$ BGA balls in this cluster of twenty-four pins to the $V_{CC-CORE}$ flood shapes on the primary.

As described above in Figure 60, the $V_{CC-CORE}$ floods are isolated between the north and south sides of the $V_{CC-CORE}$ pins of the processor socket on both the primary and secondary sides. The reason for the discontinuity of the $V_{CC-CORE}$ floods on the primary and secondary sides is to facilitate V_{CCP} power delivery. Consequently, this allows the V_{CCP} corridor connections between the DATA and ADDR sides of the processor socket on the secondary side and the V_{CCP} flood for all DATA, ADDR, and Legacy side V_{CCP} pins on the primary side (see Figure 60). In reality, the north and south sides of the $V_{CC-CORE}$ floods are bridged by means of $V_{CC-CORE}$ planes in Layers 3, 5, and 6 as illustrated in Figure 62. Layers 3, 5, and 6 connect the $V_{CC-CORE}$ stitching vias next to the negative terminals of the nine capacitors on the north side with the $V_{CC-CORE}$ stitching vias next to the negative terminals of the nine capacitors on the south side. Layers 3, 5, and 6 $V_{CC-CORE}$ corridors utilize the fact that there are no FSB signals routed under the shadow of the processor socket cavity. All the $V_{CC-CORE}$ pins of the processor pin-map should connect to the internal $V_{CC-CORE}$ planes of Layers 3, 5, and 6. Special attention should be give to not route any of the FSB or any other signal in a way that would block $V_{CC-CORE}$ connections to all the $V_{CC-CORE}$ power pins of the processor socket in Layers 3, 5, and 6. Figure 62 also shows how the $V_{CC-CORE}$ planes on Layers 3, 5, and 6 make an uninterrupted connection all the way from the SP capacitors and sense resistors in the north side of the $V_{CC-CORE}$ corridor up to the south side of the twenty-four $V_{CC-CORE}$ pins of the processor socket. This continuous connection is imperative on all three internal layers since

neither the primary nor the secondary side $V_{CC-CORE}$ floods make one continuous, robust connection from "north to south."

The remaining three, 10-µF, 0805 capacitors are placed on the primary side immediately above the shadow of the three 0805 capacitors on the secondary side and are placed at the same pitch (90 mils) as shown in Figure 60 and Figure 61. Two are on the side closest to the signal column 24 and 25 of the processor pins while one is on the side closest to signal column 2. The area in between these three capacitors can be efficiently used for VRM sense resistor connections as illustrated in the primary side zoom in view in Figure 61.

Special care should be taken to provide a robust connection on the $V_{CC-CORE}$ floods on the primary side from the sense resistors to the $V_{CC-CORE}$ corridor pins on the north side of the processor socket. This robust connection is needed due to the presence of the GND dog bones on the primary side. The specific arrangement of $V_{CC-CORE}$ and GND vias as shown in Figure 61 should be closely followed to provide a robust connection to the $V_{CC-CORE}$ floods for **ALL** $V_{CC-CORE}$ BGA balls and vias on the primary side in the AF, AE, AD, AC, AB, AA, Y, W, V, and U signal rows of the processor socket connecting all the way up to $V_{CC-CORE}$ stitching vias next to negative terminals of the nine 0805 capacitors placed under the socket cavity shadow.

Figure 63 shows a magnified view of the recommended layout for the SP capacitor connections to minimize their inductance on the secondary side (Layer 8) of the motherboard. The $V_{CC-CORE}$ pin side of the capacitor has two $V_{CC-CORE}$ vias placed 82 mils above the $V_{CC-CORE}$ pad of the SP capacitor within the shadow of the SP capacitor. These two $V_{CC-CORE}$ vias are paired with two GND vias with a 50-mil offset to reduce the inductance of the connection between the capacitor and the plane. An additional pair of GND vias are placed 82 mils below the ground pad of the SP capacitor (also under the shadow of the SP capacitor body) to allow efficient stitching of ground planes on Layers 1, 2, 4, 7, and 8 in this area. Outside the shadow of the SP capacitors, the $V_{CC-CORE}$/GND via pairs of the SP capacitors are shared with the $V_{CC-CORE}$/GND via pairs of the 0805 capacitors. The placement of additional vias is not advised since this will result in excessive perforation of the internal power planes due to the antipad voids. The pitch between the SP caps is 220 mils (or closer).

The layout concepts described in Figure 58 through Figure 63 result in an estimated $V_{CC-CORE}$ effective resistance of 0.58 m and an effective inductance of ~41 pH. Despite the use of multiple power planes, this is still significant compared to the 3-m load line target resistance and compared to the 17.1 pH (600 pH / 35) inductance of the thirty-five 0805 decoupling capacitors. If alternative layout solutions are used, they should be implemented with a level of robustness greater than or equal to that in the example above. In terms of robustness, this refers to creating a low resistance and inductance connection between the bulk and mid frequency capacitors and the processor pins.

Figure 60. $V_{CC-CORE}$ Power Delivery and Decoupling Example – (Primary and Secondary Side Layers)

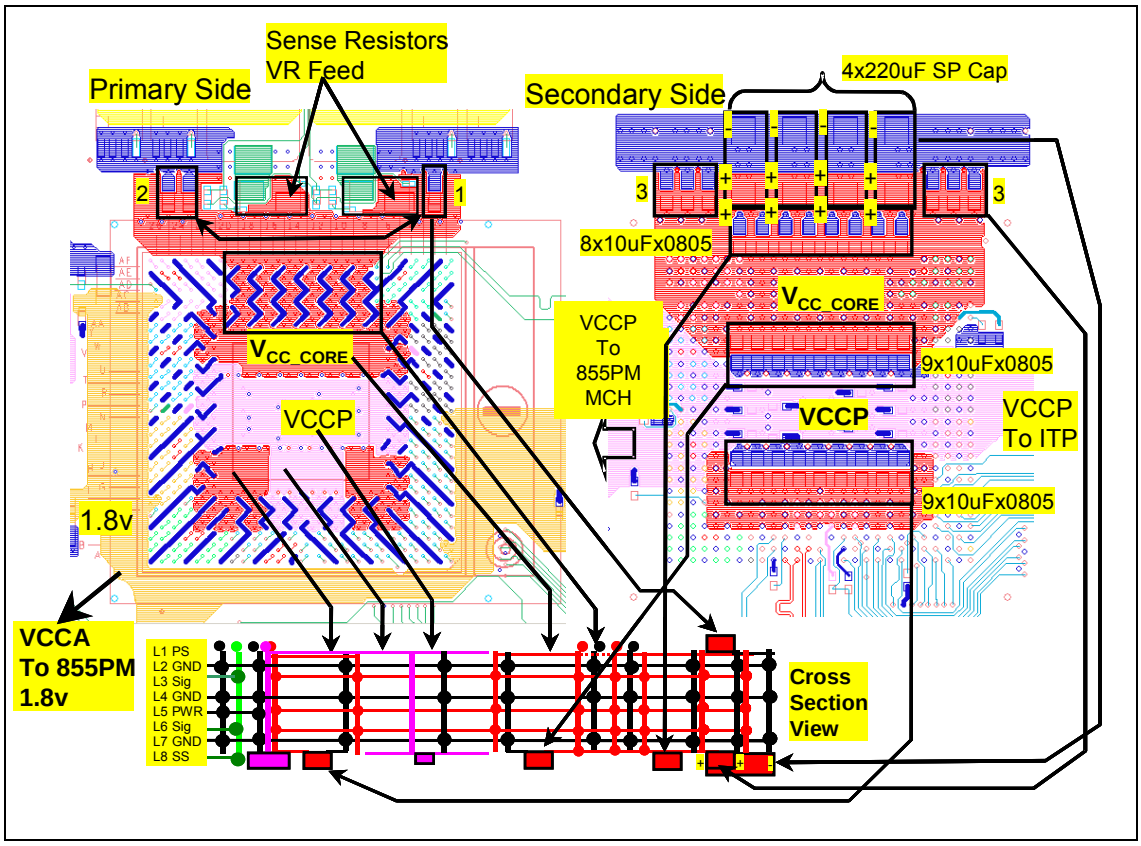


Figure 61. Processor Core Power Delivery "North Corridor" Zoom In View

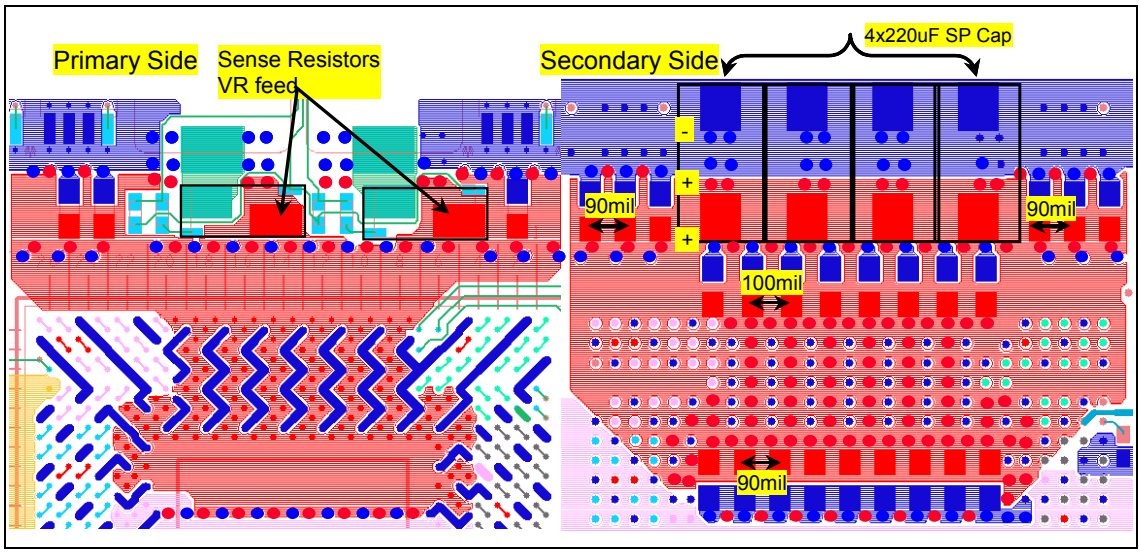


Figure 62. $V_{CC-CORE}$ Power Delivery and Decoupling Example (Layers 3, 5, and 6)

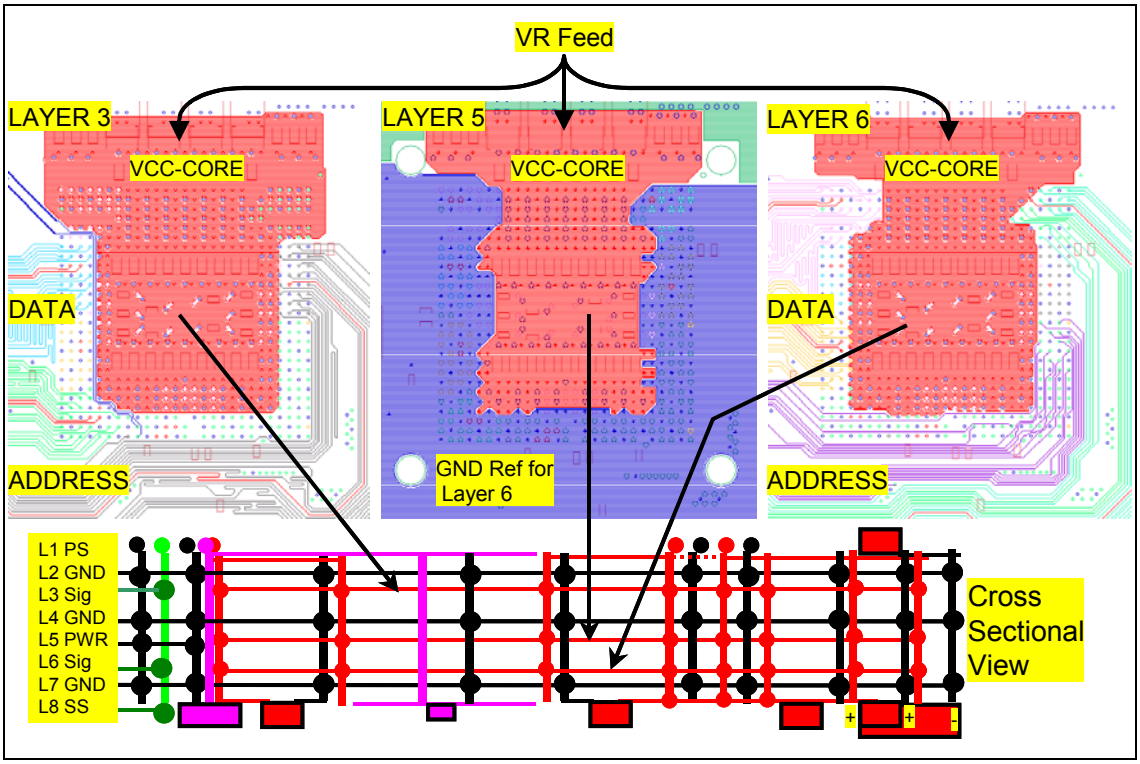
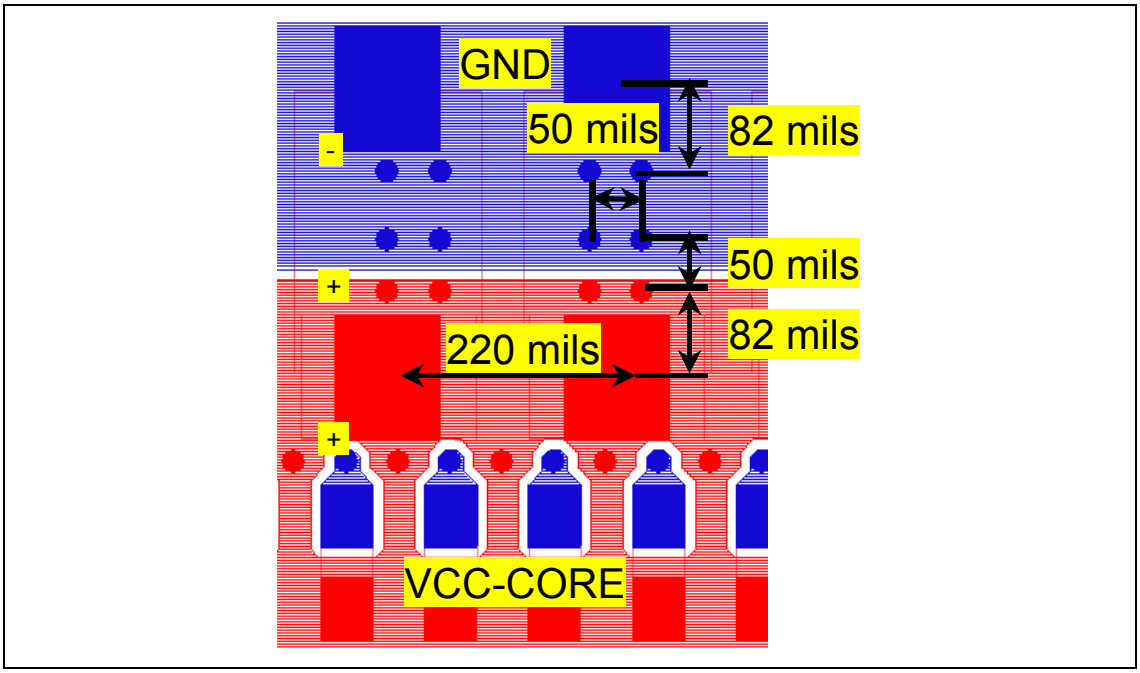


Figure 63. Recommended SP Cap Via Connection Layout (Secondary Side Layer)



5.9.4. Intel Pentium M Processor / Intel Celeron M Processor and Intel 855PM MCH V_{CCP} Voltage Plane and Decoupling

The 400-MHz high frequency operation of the Intel Pentium M/Intel Celeron M and Intel 855PM MCH's FSB requires careful attention to the design of the power delivery for V_{CCP} (1.05 V) to the processor and MCH. Table 21 summarizes the V_{CCP} (1.05 V) voltage rail decoupling requirements. Two 150-µF POSCAPs with an ESR of 36 m (typ) should be used for bulk decoupling. One capacitor should be placed next to the processor socket and one capacitor in close proximity to the MCH package. The current layout example recommends the placement of each POSCAP on the secondary side of the motherboard to minimize inductance. In addition, ten 0.1-µF X7R capacitors in a 0603 form factor should be placed on the secondary side of the motherboard under the processor socket cavity next to the V_{CCP} pins of the processor. Five capacitors should be spread out near the Data signal side and five capacitors near the Address signal side of the processor socket's pin-map. Eight more 0.1-µF X7R capacitors in a 0603 form factor should be placed on the secondary side of the motherboard next to the V_{CCP} pins of the MCH. The processor and MCH V_{CCP} pins should be shorted with a wide, V_{CCP} plane preferably on the secondary side such that it will extend across the whole "shadow" of the FSB signals routed between the processor and MCH. The 1.05-V, VR feed point into the V_{CCP} plane should be roughly in between the processor and MCH.

Table 21. V_{CCP} Decoupling Guidelines

Description	Cap (µF)	ESR (m	ESL (nH)	Notes
Low Frequency Decoupling (Polymer Covered Tantalum – POSCAP, Neocap, KO Cap)	2 x 150 µF	36 m (typ) / 2	2.5 nH / 2	1
High Frequency Decoupling (0603 MLCC, >= X7R) Place next to the processor	10 x 0.1 µF	16 m (typ) / 10	0.6 nH / 10	
High Frequency Decoupling (0603 MLCC, >= X7R) Place next to the Intel 855PM MCH	8 x 0.1 µF	16 m (typ) / 8	0.6 nH / 8	

NOTES:
1. Place one capacitor close to processor and one capacitor close to the Intel 855PM MCH.

5.9.4.1. Processor V_{CCP} Voltage Plane and Decoupling

Figure 64 illustrates a conceptual cross sectional view of the recommended processor V_{CCP} power delivery layout. Due to the presence of the Layer 7 GND plane that is 4 mils above Layer 8 (see Figure 2), the secondary side layer (Layer 8) V_{CCP} plane creates a low inductance short between the 0603 form factor 0.1-µF capacitors and the 150-µF, POSCAP capacitor. At the same time, the V_{CCP} plane on the secondary side efficiently connects the capacitors to the processor V_{CCP} pin vias. Ten, 0603 capacitors are placed on the secondary side under the socket cavity shadow while the 150- F, POSCAP capacitor is placed to the processor socket shadow close to the DATA side pins of the secondary side. Figure 65 shows a conceptual cross sectional view (left side of Figure 65) of the V_{CCP} power delivery and how it translates into an actual layout on the primary and secondary sides of the motherboard as shown on the right side of Figure 65. The secondary side of Figure 65 utilizes a wide V_{CCP} plane coming from the MCH that shorts the V_{CCP} pins of the DATA and ADDR side of the processor pin-map with the ten, 0603 form factor 0.1-µF decoupling capacitors that are placed on the secondary side in the shadow of the processor socket cavity. These capacitors provide decoupling for the V_{CCP} pins of the processor.

Placement and layout of the ten, 0.1-µF capacitors should be strictly adhered to in order to minimize the effective loop inductance of these capacitors. All the capacitors should be placed within 45 mils (center-to-center) of the V_{CCP} pin rows. Ground vias for the 0.1-µF capacitors should also be placed within 45 mils of the capacitor pads and shorted with a 25-mil wide trace to the ground via.

In Figure 65, the secondary side shows one of the 150- F POSCAPs being placed next to the processor socket close to the DATA pins. Notice that the ground pin connection of the POSCAP is extended towards the V_{CCP} pad of the capacitor with two ground vias placed under the body of the POSCAP. This is done in order to minimize the inductance of the POSCAP connection by minimizing the loop area of current flow.

Figure 65 also shows that a connection on the secondary side to the Legacy side V_{CCP} pins of the processor pin-map is not possible because it is blocked by the secondary side $V_{CC-CORE}$ flood that connects the south side 0805 capacitors with the twenty-four $V_{CC-CORE}$ pins on the south side of the processor pin-map (see secondary side of Figure 60 in Section 5.9.3). Thus, the primary side of Figure 65 illustrates a V_{CCP} flood shape that shorts the DATA, ADDR, and Legacy V_{CCP} pins of the processor pin-map. The very specific arrangement of the V_{CCP}/GND vias illustrated on the primary side of Figure 65 should be strictly followed to guarantee that each V_{CCP} BGA ball of the processor pin-map connects to the V_{CCP} shape flood on the primary side. To guarantee robust connection to the ground balls around the V_{CCP} pins, 25-mil wide dog bones should be used while the V_{CCP} BGA balls of the processor socket are advised to use the wide V_{CCP} flood in between the Vss dog bones as illustrated on the primary side of Figure 65.

A V_{CCP} flood “channel” should pass through the processor pin field on the bottom right side of the processor socket to continue the V_{CCP} feed to the ITP700FLEX debug port. A V_{CCP} flood “channel” to the ICH4-M is provided from the main V_{CCP} flood plane of the MCH and circumvents the 1.5-V and 1.8-V plane floods to the MCH by routing around the AGP bus signal quadrant (not shown in figures). Refer to Figure 65 for more details.

Figure 64. Processor V_{CCP} Power Delivery and Decoupling Concept

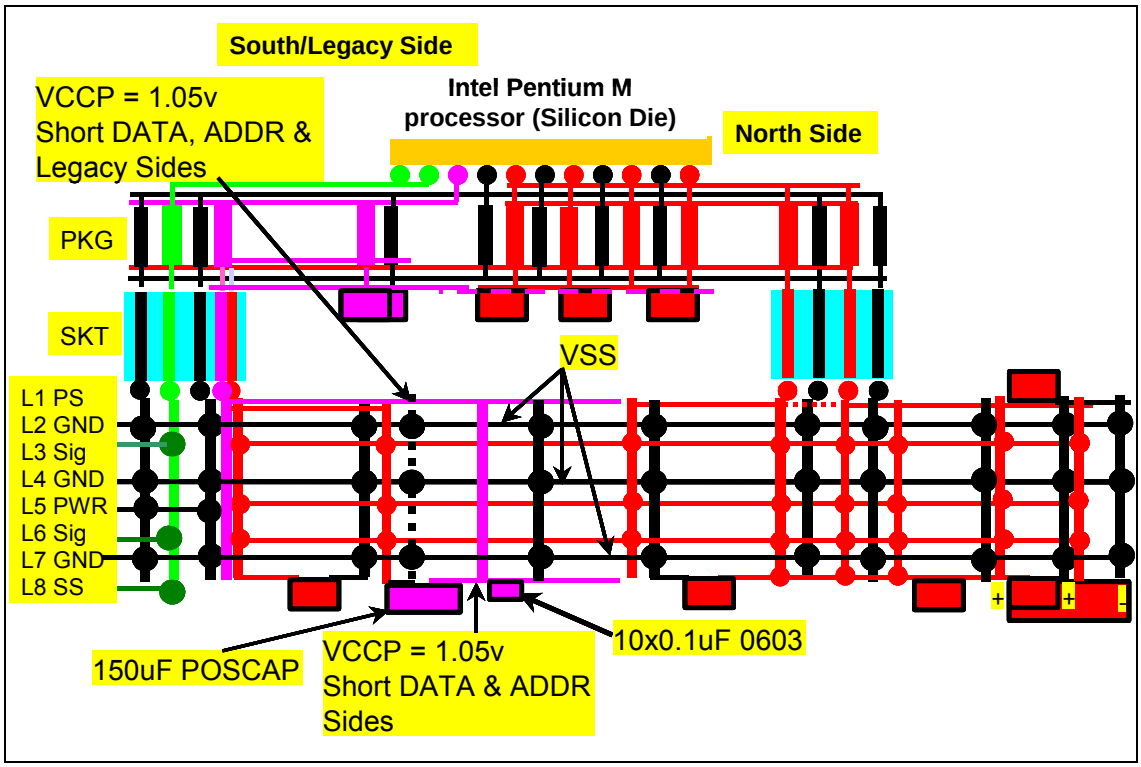
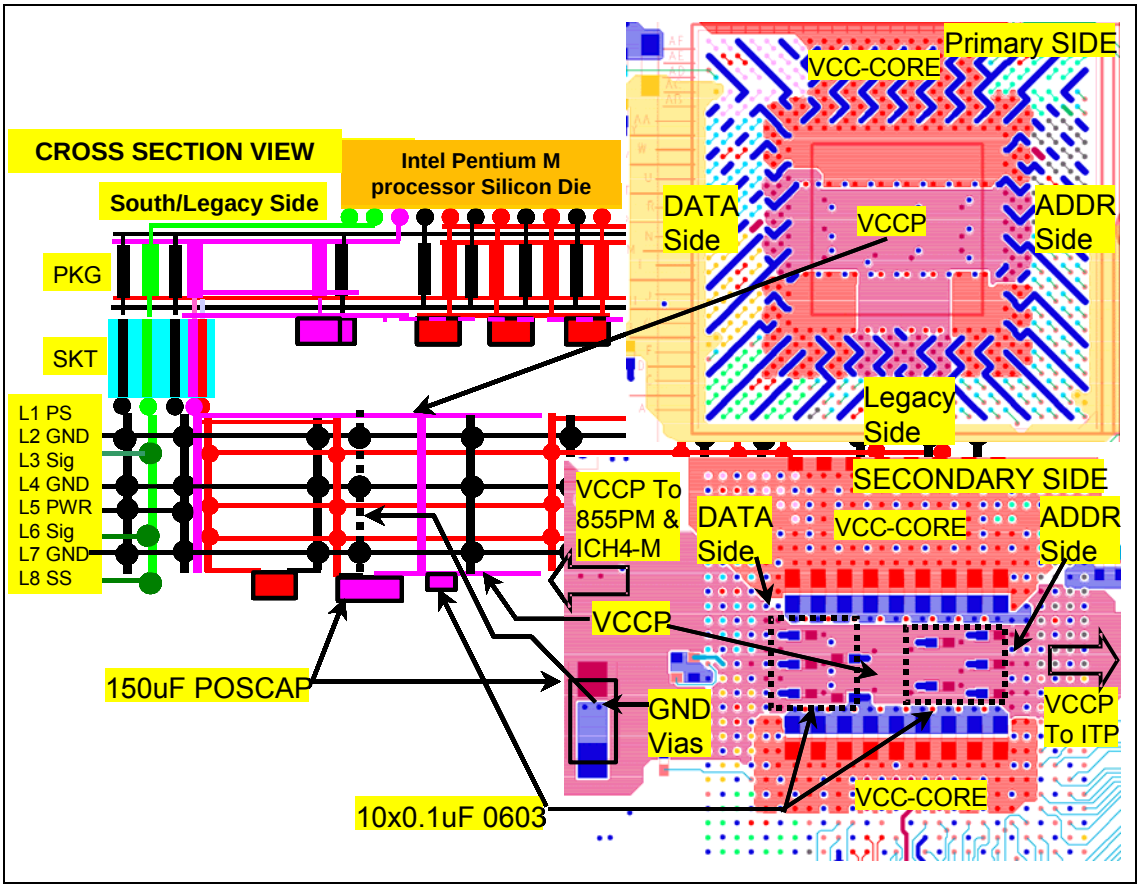


Figure 65. Processor V_{CCP} Power Plane and Decoupling Example



5.9.4.2. Intel 855PM MCH V_{CCP} Voltage Plane and Decoupling

The Intel 855PM MCH conceptual V_{CCP} (1.05 V) power delivery cross section is illustrated in Figure 66. Similar to the concept for the processor, the secondary side layer (Layer 8) that references the solid ground plane on Layer 7 located 4 mils above (see Figure 2) creates a low inductance short between the 150-µF POSCAPs and the 0.1 µF 0603 form factor capacitors placed inside and outside of the package shadow of the MCH on the secondary side.

Figure 66. Intel 855PM MCH V_{CCP} Power Plane and Decoupling Concept

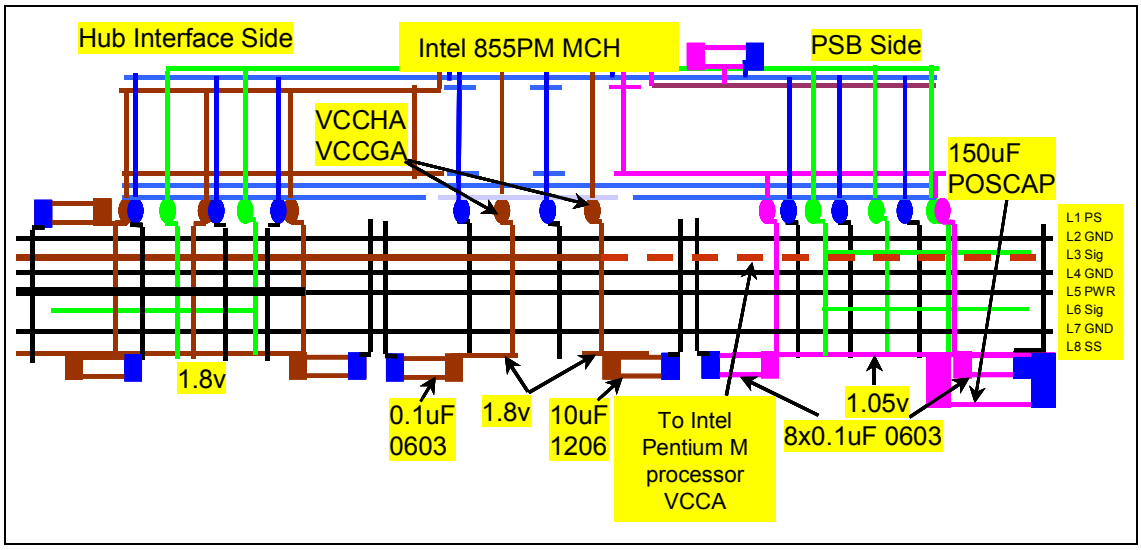
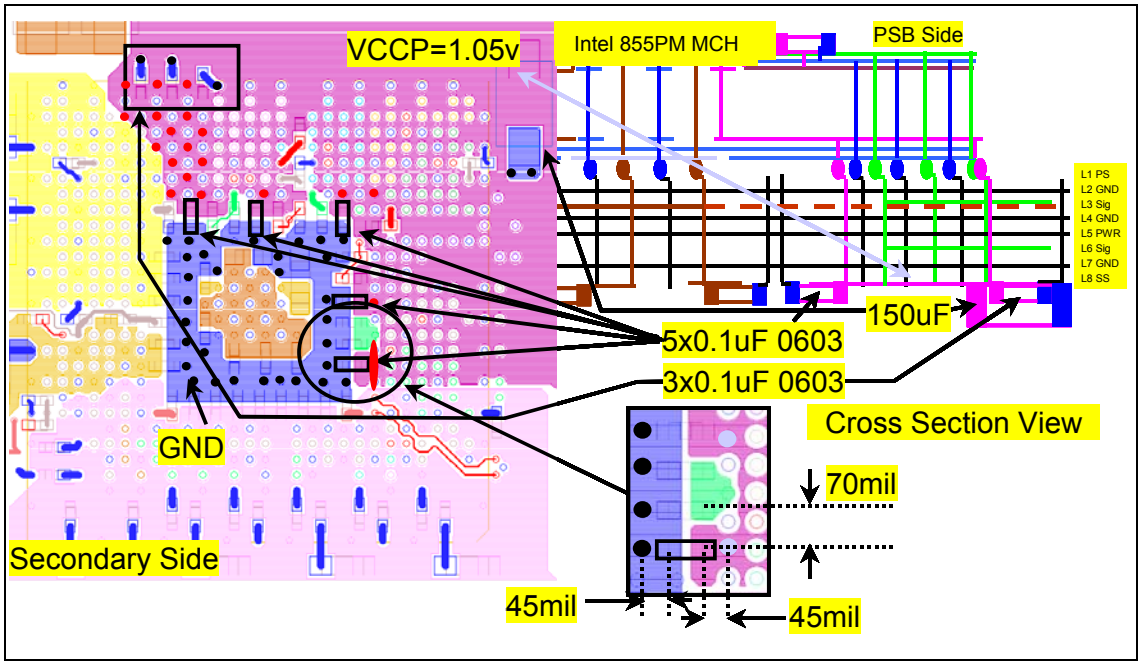


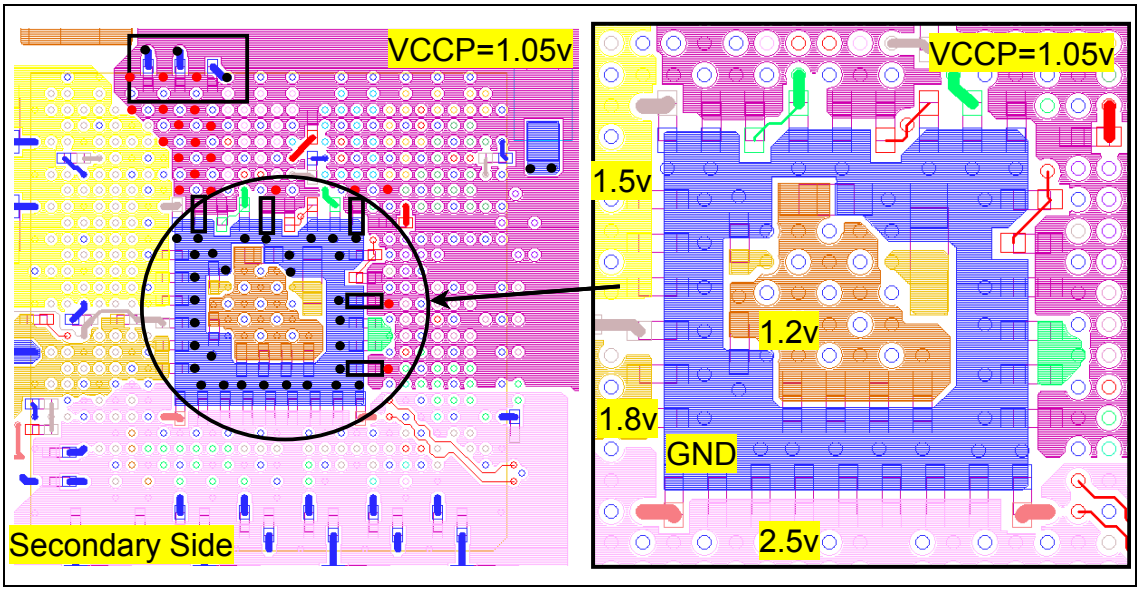
Figure 67. Intel 855PM MCH V_{CCP} Power Plane and Decoupling Recommended Layout Example



The left side of Figure 67 illustrates how the conceptual cross section (right side of Figure 67) of the V_{CCP} (1.05 V) plane for power delivery for the Intel 855PM MCH translates into an actual layout. The entire section of the MCH pin-map related to the FSB signals is a flood with a V_{CCP} plane on the secondary side (Layer 8). Five 0603 form factor 0.1-µF capacitors are placed next to each of the V_{CCP} pins of the MCH pin-map on the inner rows. The V_{CCP} pad of the capacitor is placed within (center-to-center) 45 mils of the inner row of V_{CCP} pins on the MCH pin-map. All the capacitors in the MCH's inner row of power pins are to be spaced 70 mils from each other to allow adequate spacing and placement of the capacitors. The groundsides of the 0.1-µF capacitors are shorted with a "ring" shaped ground flood. The groundside vias are within 45 mils of each of the ground pads of the capacitors. See the "Zoom In View" in Figure 67. Three, 0.1-µF 0603 form factor capacitors are placed outside the MCH cavity on the secondary side. It is important that the layout style and placement of the 0603 form factor capacitors for V_{CCP} as explained above in Figure 67 are closely followed to guarantee the 0.6 nH ESL for these capacitors. For clarity, refer to the "Zoom In View" picture of the capacitor placement on the MCH's secondary side on the inner row pin field as illustrated on the right side of Figure 68.

One, 150-µF POSCAP placed on the secondary side (top right corner of Figure 67) close to the MCH package body outline should also be used.

Figure 68. Intel 855PM MCH V_{CCP} Power Delivery Recommended Layout (Zoom In View)



5.9.5. Intel 855PM MCH Core Voltage Plane and Decoupling

The V_{CC-MCH} (1.2 V) plane feeds the internal core logic of the 855PM MCH. V_{CC-MCH} does not employ on package decoupling. Thus, in order to guarantee an accurate V_{CC-MCH} voltage on the MCH die, the specific decoupling guidelines listed in Table 22 should be closely adhered to. The specific component form factors, the layout style, and the decoupling capacitor values should also be used with no deviation from recommendations.

The decoupling for V_{CC-MCH} should utilize two, 150-µF POSCAPs acting as bulk decoupling capacitors and should be placed (preferably) on the secondary side of the motherboard in the vicinity of the MCH package shadow. The mid frequency decoupling should include a 2.2-µF, 10% 0805 form factor X7R MLCC decoupling capacitor placed within 50 mils of the MCH's U16 V_{CC-MCH} pin. High frequency decoupling consists of the careful tuning of five 0603 form factor X7R capacitors with different values each: One, 0.22-µF, 10% capacitor; one, 47-nF, 10% capacitor; one, 22-nF, 10% capacitor; one, 15 nF,

10% capacitor; and one, 10-nF, 10% capacitor. All five capacitors should be placed on the secondary side of the motherboard within 45 mils of the P17, N16, and N14 V_{CC-MCH} pins. All the V_{CC-MCH} power delivery pin vias should be shorted on the secondary side of the motherboard with a solid flood and shorted to the mid and high frequency decoupling capacitors. The primary side of the V_{CC-MCH} should use a flood plane to short the V_{CC-MCH} vias while allowing some perforation due to ground and VCCHA and VCCGA dog bones. Refer to specific layout examples below for more details.

Table 22. V_{CC-MCH} Decoupling Guidelines

Description	Cap (µF)	ESR (m	ESL (nH)	Notes
Low Frequency Decoupling (Polymer Covered Tantalum – POSCAP, Neocap, KO Cap)	2 x 150 µF	42 m (typ) / 2	2.5 nH / 2	
Mid Frequency Decoupling (0805 MLCC, >= X7R 10%)	1 x 2.2 µF	2 m (typ)	730 pH	
High Frequency Decoupling (0603 MLCC, >= X7R 10%)	1 x 220 nF	9 m (typ)	0.6 nH	1
High Frequency Decoupling (0603 MLCC, >= X7R 10%)	1 x 47 nF	24 m (typ)	0.6 nH	1
High Frequency Decoupling (0603 MLCC, >= X7R 10%)	1 x 22 nF	40 m (typ)	0.6 nH	1
High Frequency Decoupling (0603 MLCC, >= X7R 10%)	1 x 15 nF	49 m (typ)	0.6 nH	1
High Frequency Decoupling (0603 MLCC, >= X7R 10%)	1 x 10 nF	66 m (typ)	0.6 nH	1

NOTE: To achieve the 0.6 nH ESL, the recommended layout should be followed.

Figure 69 illustrates the conceptual cross sectional view for the MCH's V_{CC-MCH} (1.2 V) power delivery layout. V_{CC-MCH} vias connect a flood on the primary side to Layer 5 and Layer 6 that are parallel connection floods that feed the inner row of V_{CC-MCH} pins from the voltage regulator. The vias also continue to the secondary side flood plane under the die shadow to provide a low inductance short between the 0805 and 0603 form factor high and mid frequency decoupling capacitors with to the V_{CC-MCH} power delivery pins. Low inductance is achieved due to a 4.5-mil separation (see Figure 2) of the secondary side V_{CC-MCH} flood from the Layer 7 ground plane.

The feed connections of the Layer 5 and Layer 6 V_{CC-MCH} floods also benefit from low inductance due to the use of the Layer 4 and Layer 7 ground planes, respectively, as reference planes with a small dielectric separation (see Figure 2). The use of the two layers, Layer 5 and Layer 6, as feeds is required since one of them becomes too narrow when crossing the pin-field antipads to carry the needed amount of current without compromising voltage drop. Once Layer 5 and Layer 6 get outside the MCH package outline, two, 150-µF POSCAPs are connected with V_{CC-MCH} and ground vias to the Layer 5 and Layer 6 planes floods. Notice that the V_{CC-MCH} and the ground vias are placed under the body of the POSCAPs capacitors with about 35 mils of spacing to minimize the inductance of the capacitor connection vias. Refer to Figure 70, which illustrates how the conceptual power delivery cross sectional view of the V_{CC-MCH} in Figure 69 translates into an actual, recommended layout as implemented on the primary side layer (Layer 1), Layer 4, Layer 5, and the secondary side layer (Layer 8). The top left side of Figure 70 shows how the BGA balls and the vias are shorted with a small V_{CC-MCH} plane flood on the primary side. Notice the orientation of the dog bones on the primary side layer (Layer 1) since this is critical to fit all the required components on the secondary side.

The top right side of Figure 70 shows how most of Layer 5 under the MCH package outline is a ground plane except for a narrow corridor that allows escape of the V_{CC-MCH} out of the pin field. This is possible since Layer 5 does not need to be ground in this area since there are no signals routed on Layer 6 in this area that needs to be ground referenced to Layer 5. However, due to the via antipads the V_{CC-MCH} corridor is fairly narrow. Thus, another somewhat wider V_{CC-MCH} plane flood corridor is created in between the FSB and AGP signals for escape routing on Layer 6 as illustrated on the bottom right side of Figure 70. Both Layer 5 and Layer 6 V_{CC-MCH} floods get connected to a VR feed point.

The bottom left side of Figure 70 illustrates how the V_{CC-MCH} flood on the secondary side is shorted to the four 0603 and one 2.2 µF 0805 form factor capacitors to the V_{CC-MCH} pins. As the Layer 5 and Layer 6 V_{CC-MCH} floods continue to the VR feed point, they are also via'ed down with the four pairs of V_{CC-MCH} and ground vias to connect the two, 150-µF POSCAPs placed on the secondary side layer (Layer 8). Notice that the vias are placed under the body of the POSCAPs and connect to two small V_{CC-MCH} and ground floods on the secondary side that connect the vias to the POSCAP pads. This is done to minimize the ESL of the POSCAPs in this connection.

In Figure 70 and Figure 71, placement of the POSCAPs on the secondary side is recommended since Layer 5 and Layer 6 are much closer to the secondary side thus lower ESL will result for this connection.

Figure 69. V_{CC-MCH} Power Delivery and Decoupling Concept

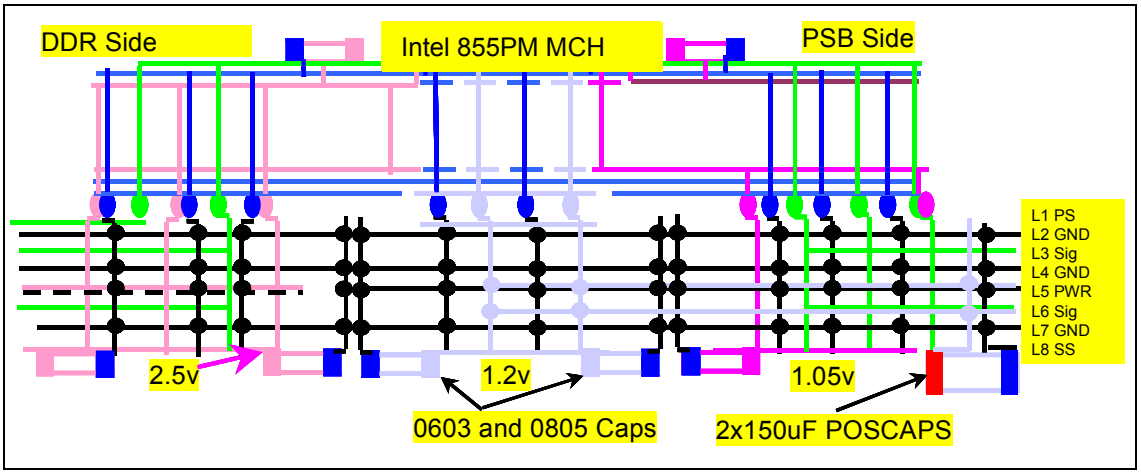


Figure 70 illustrates how the conceptual cross section of the V_{CC-MCH} power delivery in Figure 69 translates into an actual recommended layout as implemented on the primary side layer (Layer 1), Layer 4, Layer 5, and secondary side layer (Layer 8). The top left side of Figure 70 shows how the BGA balls and the vias are shorted with a small V_{CC-MCH} plane flood on the primary side. Notice the orientation of the dog bones since this is critical to fit all the required components on the secondary side.

The top right side of Figure 70 shows how most of Layer 5 under the Intel 855PM MCH package outline shadow is a ground plane except for a narrow corridor that allows for the escape routing of the V_{CC-MCH} out of the pin field. This is possible since Layer 5 does not need to be ground in this area since there are no signals routed on Layer 6 in this area that needs to use Layer 5 for ground referencing. However, due to the via antipads, the V_{CC-MCH} corridor is fairly narrow. Thus, another somewhat wider V_{CC-MCH} plane flood corridor is created in between the FSB and AGP signals for escape routing on Layer 6 as illustrated in bottom right side of Figure 70. Both Layer 5 and Layer 6 V_{CC-MCH} floods get connected to a VR feed point.

The bottom left side of Figure 70 illustrates the V_{CC-MCH} flood on the secondary side shorted to the five, 0603 form factor capacitors and one, 2.2-µF 0805 form factor capacitor to the V_{CC-MCH} pins. As the

Layer 5 and Layer 6 V_{CC-MCH} floods continue to the VR feed point, they also are via'ed down with the four pairs of V_{CC-MCH} and ground vias to connect to the two, 150-µF POSCAPs placed on the secondary side (Layer 8). Notice that the vias are placed under the body of the POSCAPs and connect to two small V_{CC-MCH} and ground floods on the secondary side that connect the vias to the POSCAP pads. This is done to minimize the ESL of the POSCAPs in this connection.

In Figure 70 and Figure 71, placement of the POSCAPs on the secondary side is recommended since Layer 5 and Layer 6 are much closer to the secondary side, thus lower ESL will result from this connection.

Figure 70. V_{CC-MCH} Power Planes and Decoupling Example

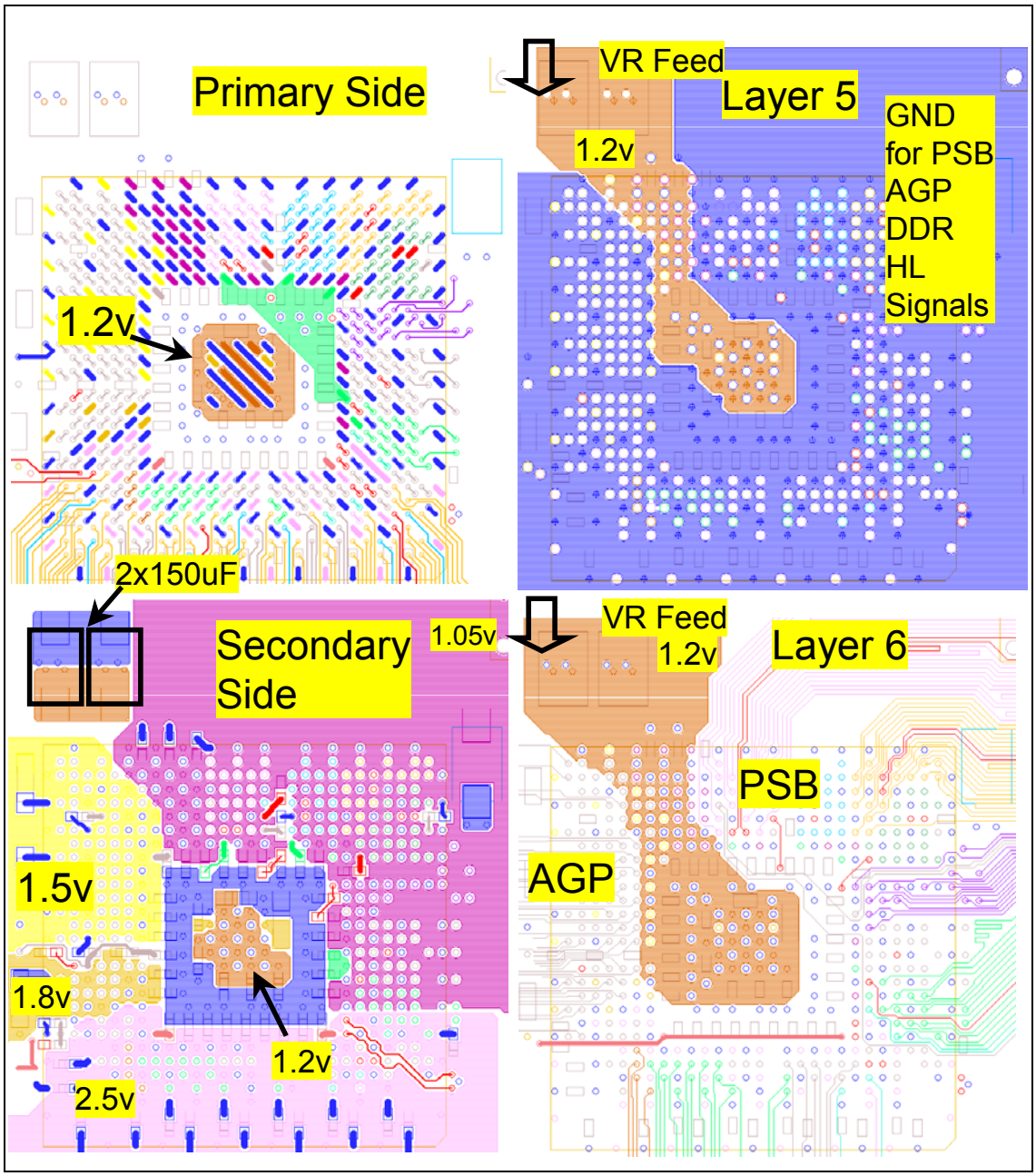
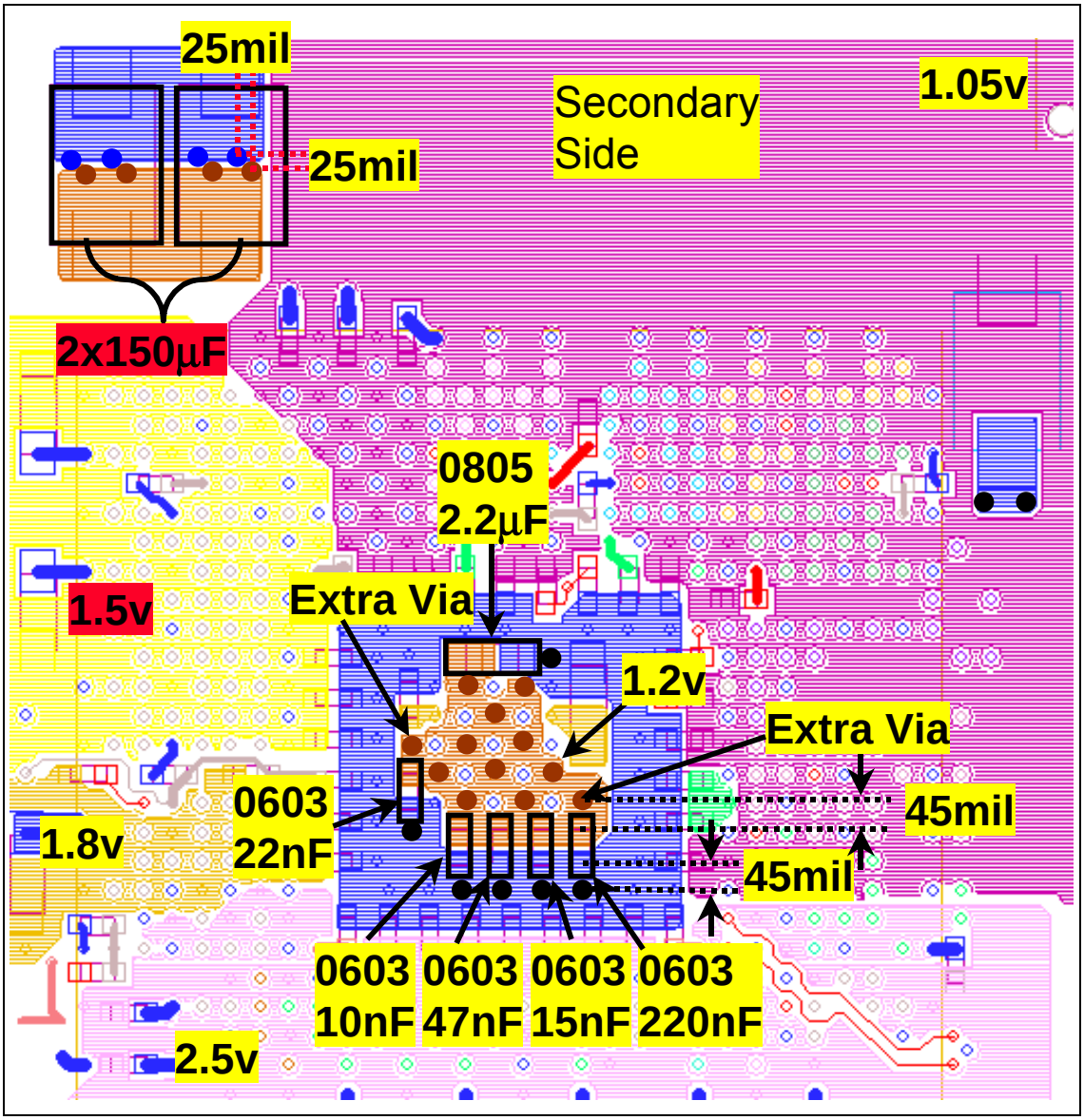


Figure 71 further illustrates a "Zoom In View" of the secondary side layout that was shown on the bottom left side of Figure 70. Notice the specific locations of the 0805, 2.2-µF mid frequency capacitor and the 0603 form factor 10 nF, 15 nF, 22 nF, 47 nF, and 220 nF high frequency decoupling capacitors. The 0603 capacitors' V_{CC-MCH} side pads are placed within 45 mils of their respective row of V_{CC-MCH} vias. All these capacitors are shorted with the V_{CC-MCH} flood on the secondary side plane to the V_{CC-MCH} vias of the pin field and the two extra vias that were added to effectively stitch the primary side, Layer 5, Layer 6, and the secondary side V_{CC-MCH} floods to the decoupling capacitors. The groundside of the 0603 form factor 10 nF, 15 nF, 22 nF, 47 nF, and 220 nF capacitors connect to a ground ring on the secondary side and a stitching ground via is placed within 45 mils of the ground pad of the capacitor.

On the top left corner of Figure 71 four pairs of the V_{CC-MCH} and ground vias connect the two small V_{CC-MCH} and ground floods for the two 150-µF bulk decoupling POSCAPs to internal layers. The V_{CC-MCH} vias are offset 25 x 25 mils in the X and Y directions from the ground vias. This cluster of vias is placed symmetrically under the middle of the body of the POSCAPs.

Figure 71. V_{CC-MCH} Secondary Layer Decoupling Capacitor Placement (Zoom in View)



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6. System Memory Design Guidelines (DDR-SDRAM)

The Intel 855PM chipset Double Data Rate (DDR) SDRAM system memory interface consists of 121 CMOS signals. These CMOS signals have been divided into several signal groups: Data, Command, Control, Feedback, and Clock signals. Table 23 summarizes the different signal grouping. Refer to the *Intel® 855PM Memory Controller Hub (MCH) DDR 200/266/MHz Datasheet* for details on the signals listed.

Table 23. Intel 855PM Chipset DDR Signal Groups

Group	Signal Name	Description
Data	SDQ[63:0]	Data Bus
	SDQ[71:64]	Check Bits for ECC Function
	SDQS[8:0]	Data Strobes
Command	SMA[12:0]	Memory Address Bus
	SBS[1:0]	Bank Select
	SRAS#	Row Address Select
	SCAS#	Column Address Select
	SWE#	Write Enable
Control	SCKE[3:0]	Clock Enable - (One per Device Row)
	SCS#[3:0]	Chip Select - (One per Device Row)
Feedback	RCVENOUT#	Output Feedback Signal
	RCVENIN#	Input Feedback Signal
Clocks	SCK[5:0]	DDR-SDRAM Differential Clocks - (3 per SO-DIMM)
	SCK#[5:0]	DDR-SDRAM Inverted Differential Clocks - (3 per SO-DIMM)

6.1. DDR 200/266/333 MHz System Memory Topology and Layout Design Guidelines

The Intel 855PM chipset's Double Data Rate (DDR) SDRAM system memory interface implements the low swing, high-speed, terminated SSTL_2 topology.

This section contains information and details on the DDR topologies, the DDR layout and routing guidelines, and the DDR power delivery requirements that will provide for a robust DDR solution on an system incorporating the Intel 855PM chipset.

Caution: DDR System Memory Topologies for all signal groups have a relatively high via usage, please take this into consideration for the board layout as the vias and the anti-pad for the via could restrict power delivery to the SO-DIMMs.

Note: Simulations performed for motherboard strip-line, simulations account for different propagation delays in strip-line only and **not** accounted for in micro-strip. The simulated motherboard r was 3.8 and 4.5.

Note: Intel has conducted simulations for 2x8 SO-DIMMs that are based on the 1x8 raw card B populated with Dual Die Package (DDP) SDRAM parts based on 512-Mbit devices (two 256-Mbit dies within the same package). For platform design details for supporting this memory type, see Section 6.1.6.

Note: In the *JEDEC PC2100 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Rev 1.0*, it is noted that pin 89 and pin 91 (CK2 and CK2#) of the SO-DIMM connector are reserved for x72 modules or registered modules. By default, the Intel 855PM MCH does not drive 3rd SCK pair to non-ECC memory modules. Therefore, it is important to make sure that the memory modules are not expected to use all clock pairs. Intel design guidelines for non-ECC memory modules assume that only 2 of 3 SCK differential clock pairs available on the MCH are used. Intel design guidelines assume that only ECC memory modules utilize three SCK differential clock pairs.

6.1.1. Data Signals – SDQ[71:0], SDQS[8:0]

The Intel 855PM MCH data signals are source synchronous signals that include a 64-bit wide data bus, 8 check bits for Error Checking and Correction (ECC), and 9 data strobe signals. There is an associated data strobe (DQS) for each data (DQ) and check bit (CB) group. This section summarizes the DQ/CB to DQS matching.

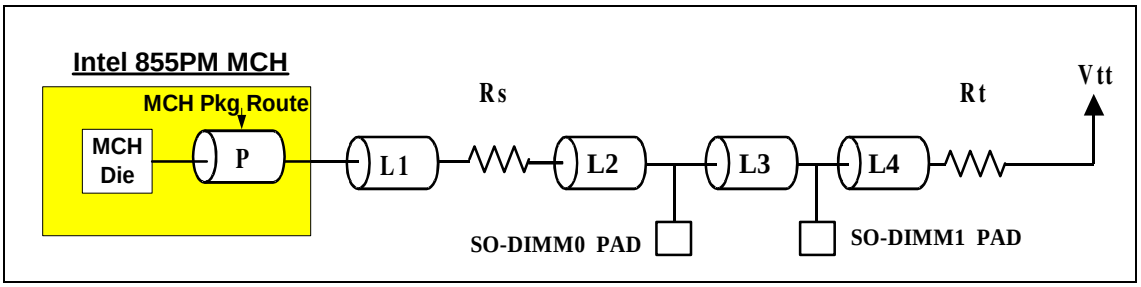
The data signals include SDQ[71:0] and SDQS[8:0]. The data signal group routing starting from the MCH is as follows. The data signals should transition immediately from an external layer to an internal signal layer under the MCH. Keep to the same internal layer until transitioning back to an external layer at the series resistor. If the series resistor is on the same side of the board as SO-DIMM0 then stay on external layer and route to appropriate pad of SO-DIMM0. If it is necessary to return to an internal layer return to same internal layer and then return to external layer immediately prior to appropriate pad of SO-DIMM0. If the series resistor is on the opposite side of the board then either transition to same external layer as SO-DIMM0 and route to appropriate pad of SO-DIMM0 or return to the same internal layer and then return to external layer immediately prior to the appropriate pad of SO-DIMM0. Continue the route for the SO-DIMM0 pad by returning to same internal layer and transition to an external layer immediately prior to the appropriate pad of SO-DIMM1. To connect the parallel termination resistor either remain on same external layer as SO-DIMM1 and connect the parallel termination resistor, transition to external layer on opposite of the board as the SO-DIMM1 and connect the parallel

termination resistor, or transition to same internal layer and then return to external layer and connect to the parallel termination resistor.

The data signal group byte lane and associated strobe needs to be routed on the same inner signal layer. The data signal groups and associated strobe may be routed on different internal layers provided that the byte lane are all routed on same internal layer. For example SDQ[7:0] and SDQS0 may be routed on one internal layer and SDQ[15:8] and SDQS1 may be routed on a different internal layer. In addition, match routing topology and via placement for all signals in a given byte lane including the associated strobe. External trace lengths should be minimized. To facilitate simpler routing, swapping of the byte lane and the associated strobe is allowed for SDQ[63:0] only. Bit swapping within the byte lane is allowed for SDQ[63:0] only. The CB group, SDQ[71:64], cannot be byte lane swapped with another DQ byte late. Also, bit swapping within the SDQ[71:64] byte lane is not allowed. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series (Rs) and parallel (Rt) data and strobe termination resistors, but data and strobe signals can't be placed within the same R pack as the command or control signals. The table and diagrams below depict the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Figure 72. Data Signal Routing Topology



The data signals should be routed using 1:2 trace to space ratio for signals within the data group. There should be a minimum of 20 mils of spacing to non-DDR related signals and DDR clock pairs SCK/SCK#[5:0]. Data signals should be routed on inner layers with minimized external trace lengths.

Table 24. Data Signal Group Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	Data – SDQ[71:0], SDQS[8:0]		1
Motherboard Topology	Daisy Chain with Parallel Termination		
Reference Plane	Ground Referenced		
Characteristic Trace Impedance (Zo)	55 ±15%		
Trace Width	Inner layers: 4 mils Outer layers: 5 mils		
Trace to Space ratio	1:2 (e.g. 4 mil trace to 8 mil space)		6
Group Spacing	Isolation spacing for non-DDR related signals = 20 mils minimum		
Trace Length L1 – MCH Signal Ball to Series Termination Resistor Pad	Min = 0.5" Max = 3.75"	Figure 74	3, 5
Trace Length L2 – Series Termination Resistor	Max = 0.75"	Figure 74	3

Pad to First SO-DIMM Pad			
Trace Length L3 – First SO-DIMM Pad to Last SO-DIMM Pad	Max = 1.0”	Figure 74	3
Trace Length L4 – Last SO-DIMM Pad to Parallel Termination Resistor Pad	Max = 0.80”	Figure 74	
Overall routing length from 855PM MCH to last SO-DIMM Pad– L1+Rs+L2+L3 (required for DDR333 support)	Min = 0.5” Max= 4.5”		
Series Termination Resistor (Rs)	10 ± 5%		
Parallel Termination Resistor (Rt)	56 ± 5%		
Maximum Recommended Motherboard Via Count Per Signal	6		2, 4
Length Matching Requirements	SDQ[71:0] to SDQS[8:0] SDQS[8:0] to SCK/SCK#[5:0] See Section 6.2.1for details		

NOTES:

1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using 4 vias if trace length L2 is routed on same external layer as SO-DIMM0 and a via is shared between SO-DIMM1 and parallel termination resistor.
5. L1 trace length does not include MCH-M package length and should not be used when calculating L1 length.
6. Implementing a space to trace ratio of 3:1 (e.g. 12-mil space to 4-mil trace) for DQS[8:0] will produce a design with increased timing margins.

6.1.1.1. Data to Strobe Length Matching Requirements

The data and check bit signals, SDQ[71:0], are grouped by byte lanes and associated with a data strobe, SDQS[8:0]. The data signals and check bit signals must be length matched to their associated strobe within ± 25 mils provided that individual trace lengths (i.e. L1, L2, and L3) specifications are not violated. For SO-DIMM0 this length matching includes the motherboard trace length to the pads of the SO-DIMM0 connector (L1 + Rs Length + L2). For SO-DIMM1, the motherboard trace length to the pads of the SO-DIMM1 connector (L1 + Rs Length + L2 + L3).

For associated SDQS Length = X and SDQ Byte Group Length = Y, the following must be met:

$$(X - 25 \text{ mils}) \quad Y \quad (X + 25 \text{ mils})$$

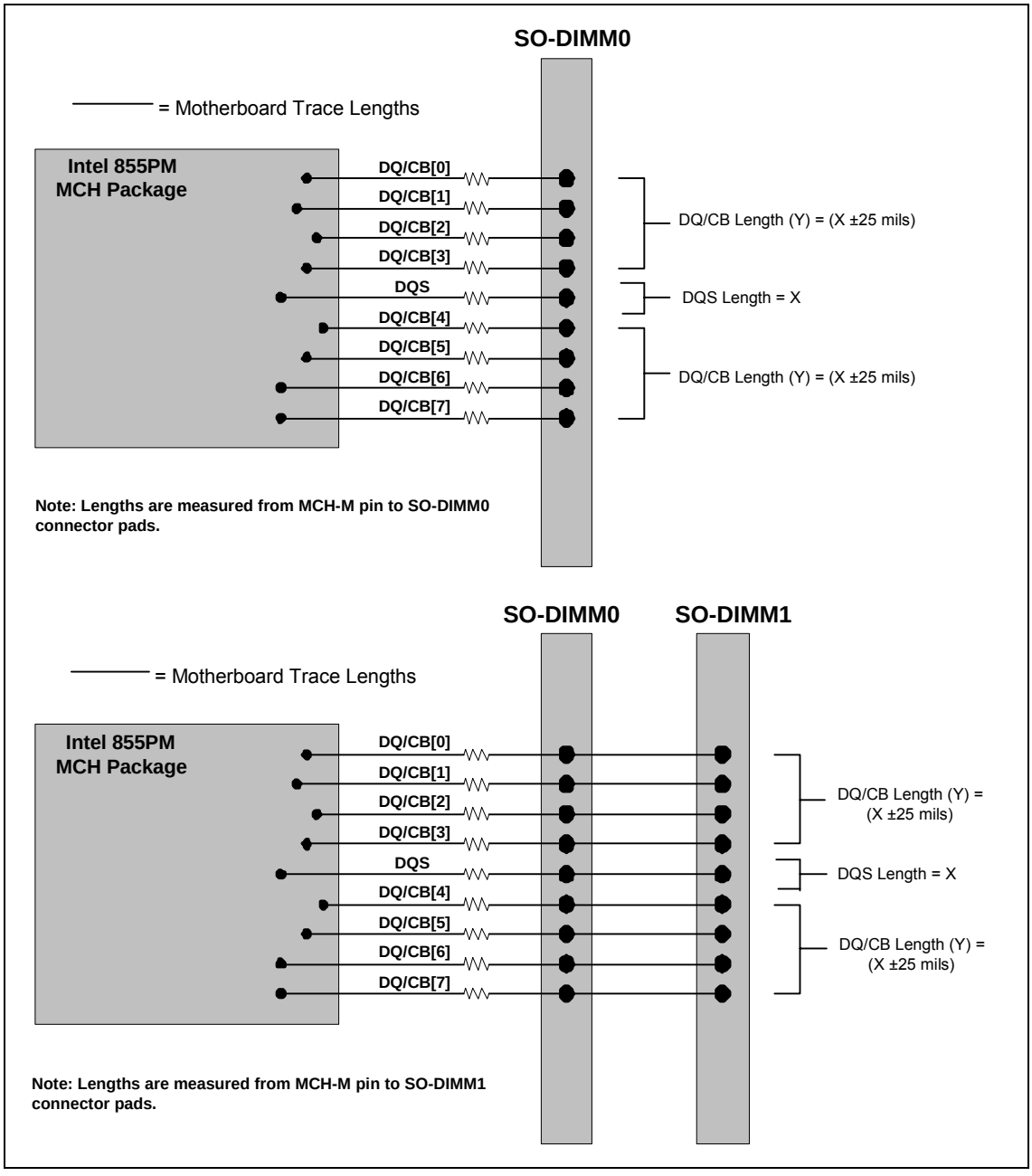
No length matching is required from the SO-DIMM1 to the parallel termination resistors. Table 25 and Figure 73 below depict the length matching requirements between the DQ, CB, and DQS signals.

Table 25. SDQ[71:0] to SDQS[8:0] Length Mismatch Mapping

Signal	Mismatch	Relative To
SDQ[7:0]	± 25 mils	SDQS0
SDQ[15:8]	± 25 mils	SDQS1
SDQ[23:16]	± 25 mils	SDQS2
SDQ[31:24]	± 25 mils	SDQS3
SDQ[39:32]	± 25 mils	SDQS4
SDQ[56:40]	± 25 mils	SDQS5
SDQ[55:48]	± 25 mils	SDQS6
SDQ[63:56]	± 25 mils	SDQS7
SDQ[71:64]	± 25 mils	SDQS8

Note: The recommended individual trace lengths (i.e. L1, L2, and L3) specifications can not be violated when the signal lengths are tolerance by ± 25 mils.

Figure 73. DQ/CB to DQS Trace Length Matching Requirements



6.1.1.2. Strobe to Clock Length Matching Requirements

The data strobe signals may be up to 1.0 inches shorter or up to 0.5 inches longer than their associated differential clock pairs.

Note: Using this formula is made simpler by routing all clocks to the associated SO-DIMM the same length, for example SCK/SCK#[2:0] all being the same length.

Length matching equation for SO-DIMM0:
X_1 = SCK/SCK#[2:0] = MCH package + L1 of Figure 72
Y_1 = SDQS[8:0] = MCH package + L1 + Rs Length + L2 of Figure 72 where:

$$(Y_1 – 0.5”) \quad X_1 \quad (Y_1 + 1.0”)$$

Length matching equation for SO-DIMM1:
X_2 = SCK/SCK#[5:3] = MCH package + L1 of Figure 72
Y_2 = SDQS[8:0] = MCH package + L1 + Rs Length + L2 + L3 of Figure 72 where:

$$(Y_2 – 0.5”) \quad X_2 \quad (Y_2 + 1.0”)$$

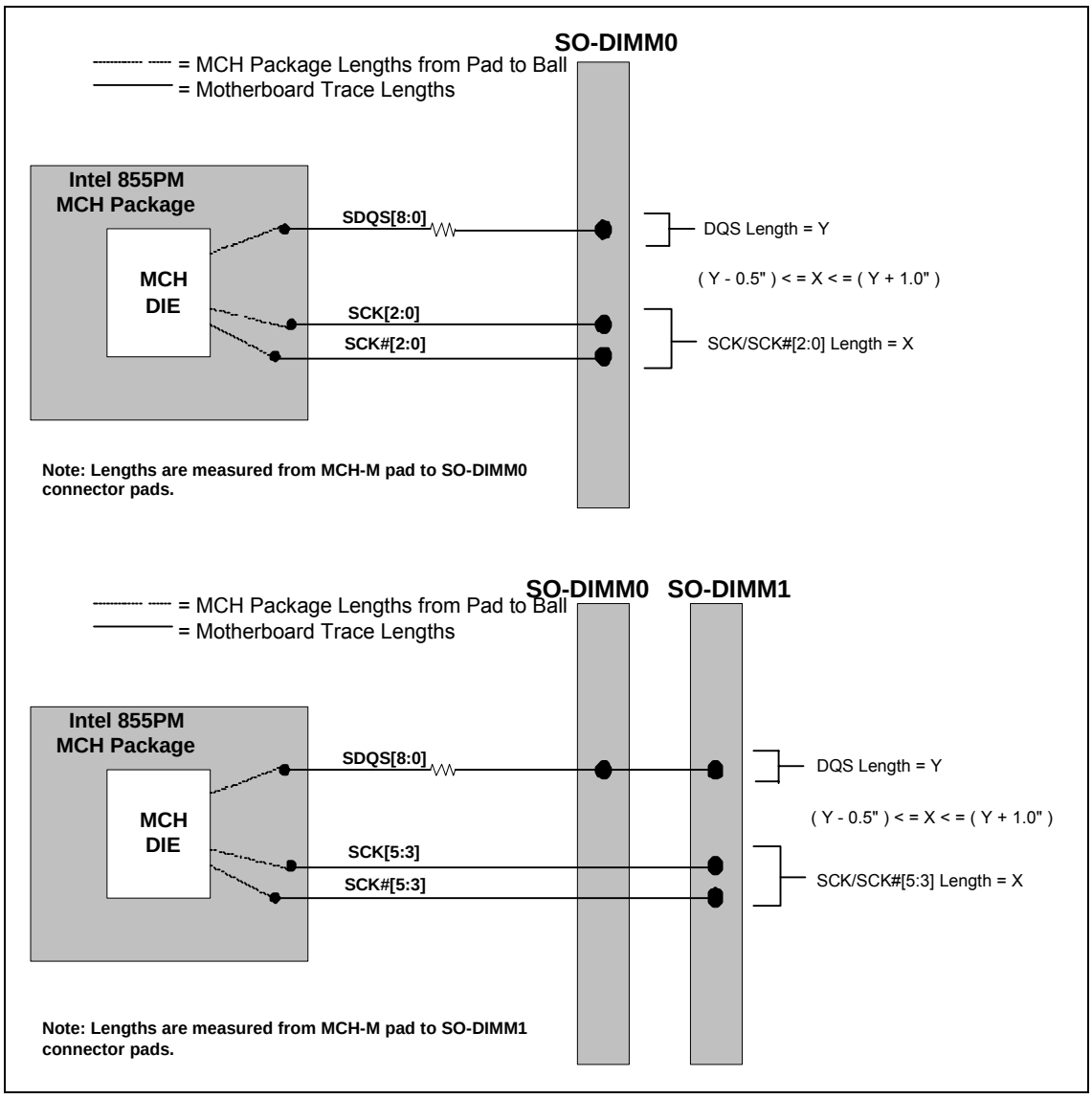
For example if the total clock length of SCK/SCK#[2:0](X_1) is 3.5 inches then the length of all data strobe signal routing to SO-DIMM0 must be between 2.5 inches to 4.0 inches, if SCK/SCK#[5:3](X_2) is 4.5 inches then the length of all control signal route to SO-DIMM1 must be between 3.5 inches to 5.0 inches. Figure 74 depicts the length matching requirements between the DQS and clock signals.

The MCH package lengths for clocks and strobes **must** be taken into account for routing length matching.

If clocks to each SO-DIMM are routed to different lengths due to allowable tolerance, then the strobe to clock length requirement must be met for all clock lengths. For example if the clock pairs to SO-DIMM0 are routed at 1.975 inches for CLK0/CLK0#, 2.000 inches for CLK1/CLK1#, and 2.025 inches for CLK2/CLK2# then the strobes length (DQS) to SO-DIMM0 must be routed between 1.025 inches to and 2.475 inches. If the CLK to one SO-DIMM is all equal in length, 2.00 inches for example then the strobes (DQS) can be routed between 1.00 inches to 2.50 inches.

Refer to Section 4.4 for package trace length data.

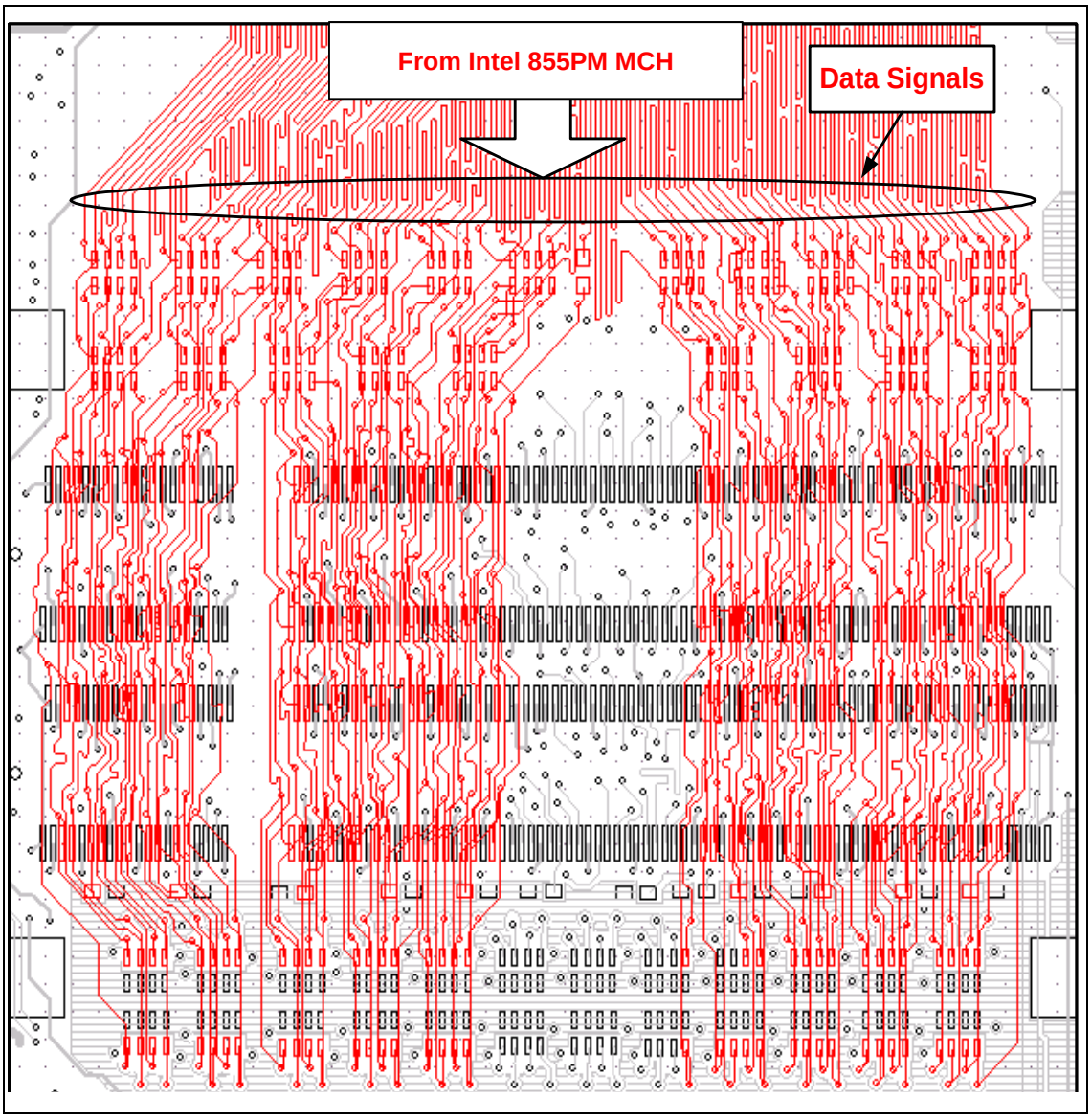
Figure 74. SDQS to SCK/SCK# Trace Length Matching Requirements



6.1.1.3. Data Routing Example

Figure 75 is an example of a board routing for the Data signal group. Data routing is shown in red. The majority of the Data signal route is on an internal layer, both external layers can used for parallel termination R-pack placement.

Figure 75. Data Signals Group Routing Example



6.1.1.4. Support for Small Form Factor Design DDR Data Bus Routing

The layout and routing guidelines for the system memory interface of the Intel 855PM MCH have been optimized to address the requirements of small form factor designs (i.e., mini-note, sub-note, and tablet PCs). The design guidelines allow the routing of SDQ[71:0] and SDQS[8:0] from the MCH pin to the series resistor (Rs) to be as short as 0.5 inches.

6.1.2. Control Signals – SCKE[3:0], SCS#[3:0]

The Intel 855PM MCH control signals, SCKE[3:0] and SCS#[3:0], are common clocked signals. They are "clocked" into the DDR-SDRAM devices using clock signals SCK/SCK#[5:0]. The MCH drives the control and clock signals together, with the clocks crossing in the valid control window. The MCH provides one chip select (CS) and one clock enable (CKE) signal per SO-DIMM physical device row. Two chip select and two clock enable signals will be routed to each SO-DIMM. Refer to Table 26 for the CKE and CS# signal to SO-DIMM mapping.

Table 26. Control Signal to SO-DIMM Mapping

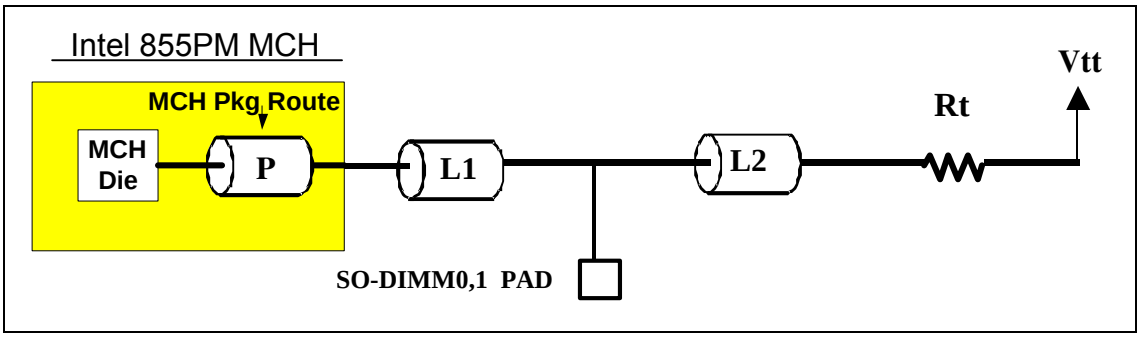
Signal	Relative To	SO-DIMM Pin
SCS#[0]	SO-DIMM0	121
SCS#[1]	SO-DIMM0	122
SCS#[2]	SO-DIMM1	121
SCS#[3]	SO-DIMM1	122
SCKE[0]	SO-DIMM0	96
SCKE[1]	SO-DIMM0	95
SCKE[2]	SO-DIMM1	96
SCKE[3]	SO-DIMM1	95

The control signal group routing starting from MCH is as follows. The control signal routing should transition immediately from an external layer to an internal signal layer under the MCH. Keep to the same internal layer until transitioning back to an external layer and connect to the appropriate pad of the SO-DIMM connector and the parallel termination resistor. If the layout requires additional routing before the termination resistor, return to the same internal layer and transition back out to an external layer immediately prior to parallel termination resistor.

External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground reference to keep the path of return current continuous. Intel suggests that all control signals be routed on the same internal layer.

Resistor packs are acceptable for the parallel (Rt) control termination resistors, but control signals can not be placed within the same R pack as the data or command signals. The table and diagrams below depict the recommended topology and layout routing guidelines for the DDR-SDRAM control signals.

Figure 76. Control Signal Routing Topology



The control signals should be routed using 1:2 trace to space ratio for signals within the control group. There should be a minimum of 20-mils of spacing to non-DDR related signals and DDR clocks SCK/SCK#[5:0]. Control signals should be routed on inner layers with minimized external trace lengths.

Table 27. Control Signal Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	Control – SCKE[3:0], SCS#[3:0]		1
Motherboard Topology	Point-to-Point with Parallel Termination		
Reference Plane	Ground Referenced		
Characteristic Trace Impedance (Zo)	55 ±15%		
Trace Width	Inner layers: 4 mils Outer layers: 5 mils		
Trace to Space ratio	1:2 (e.g. 4 mil trace to 8 mil space)		
Group Spacing	Isolation spacing for non-DDR related signals = 20 mils minimum		
Trace Length L1 – MCH Control Signal Ball to SO-DIMM Pad	Min = 0.5 inches Max = 5.0 inches	Figure 76	4, 5
Trace Length L2 – SO-DIMM Pad to Parallel Termination Resistor Pad	Max = 2.0 inches	Figure 76	
Parallel Termination Resistor (Rt)	56 ± 5%		
Maximum Recommended Motherboard Via Count Per Signal	3		2, 3, 4
Length Matching Requirements	Control Signals to SCK/SCK#[5:0] See Section 6.1.2.1 for details		

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. It is possible to route using 2 vias if one via is shared that connects to the SO-DIMM pad and parallel termination resistor.
4. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
5. L1 trace length does not include MCH package length and should not be used when calculating L1 length.

6.1.2.1. Control to Clock Length Matching Requirements

The control signals must be 0.5 inches shorter to 1.0 inches longer than their associated differential clock pairs.

Length matching equation for SO-DIMM0:
X_1 = SCK/SCK#[2:0]
Y_1 = SCS#[1:0] and SCKE[1:0] = L1of Figure 76 where:

$$(Y_1 – 1.0”) \quad X_1 \quad (Y_1 + 0.5”)$$

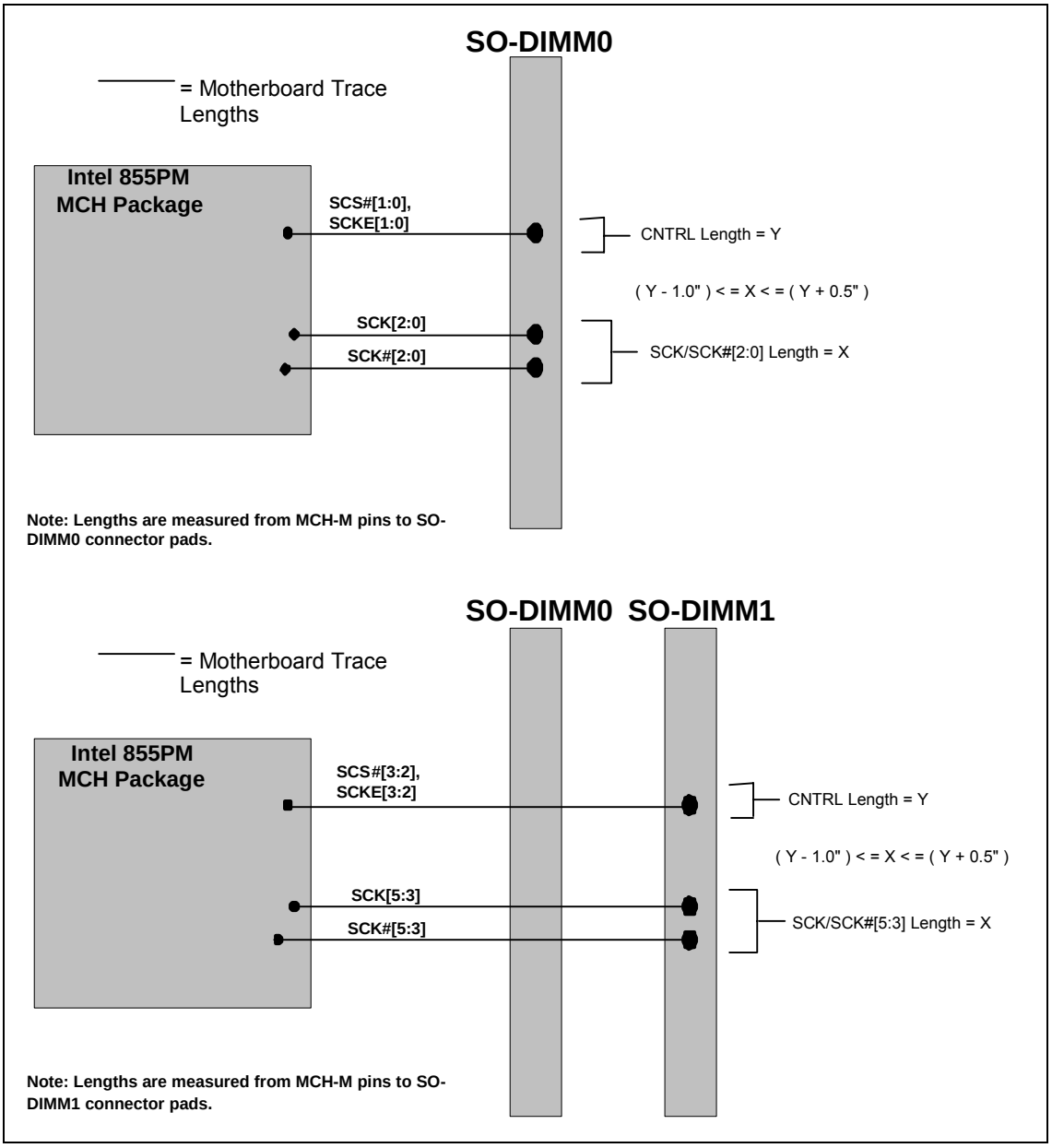
Length matching equation for SO-DIMM1:
X_2 = SCK/SCK#[5:3]
Y_2 = SCS#[3:2] and SCKE[3:2] = L1of Figure 76 where:

$$(Y_2 – 1.0”) \quad X_2 \quad (Y_2 + 0.5”)$$

For example if the clock length of SCK/SCK#[2:0](X_1) is 3.5 inches then the length of all control signal routing to SO-DIMM0 must be between 3.0 inches to 4.5 inches, if SCK/SCK#[5:3](X_2) is 4.5 inches then the length of all control signal route to SO-DIMM1 must be between 4.0 inches to 5.5 inches. Figure 77 depicts the length matching requirements between the control and clock signals.

The MCH package lengths do not need to be taken into account for routing length matching purposes.

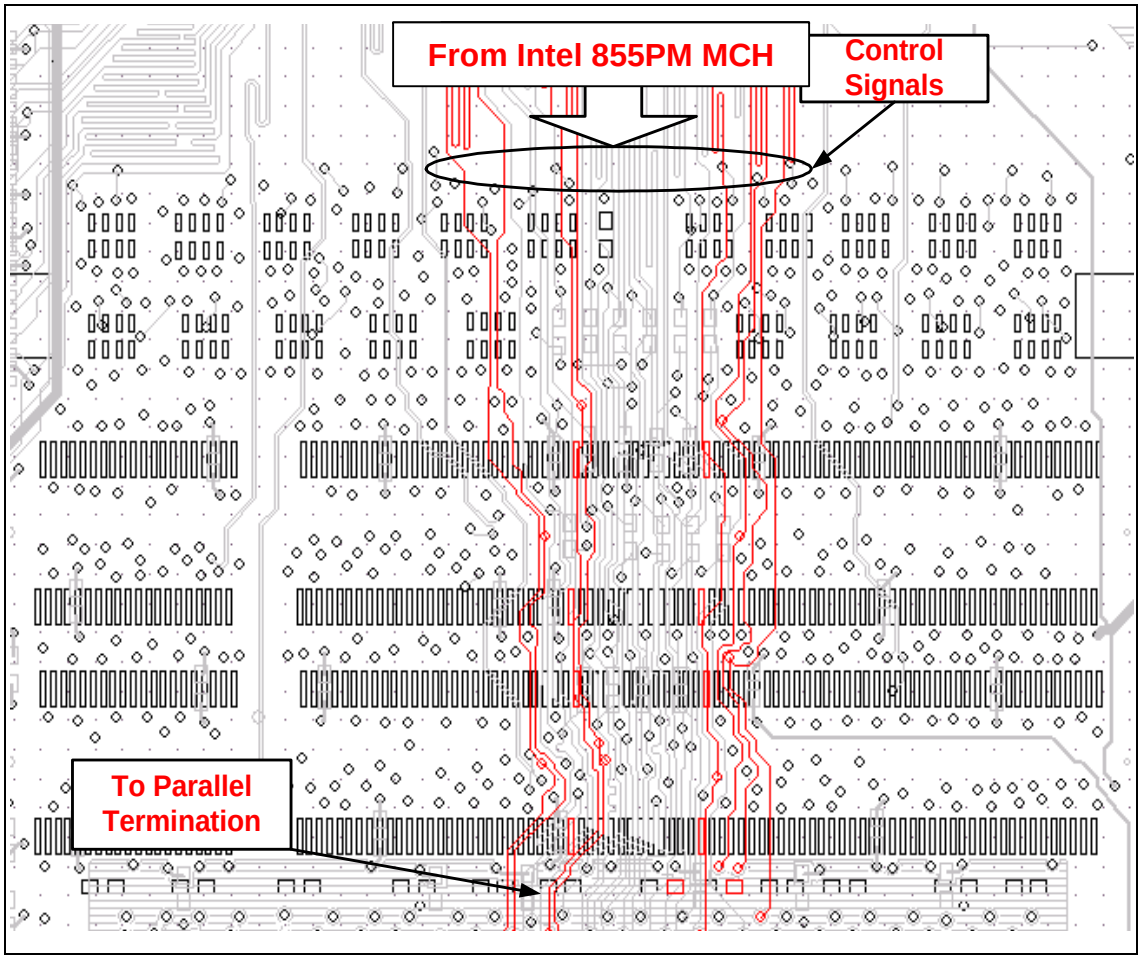
Figure 77. Control Signal to SCK/SCK# Trace Length Matching Requirements



6.1.2.2. Control Routing Example

Figure 78 is an example of a board routing for the Control signal group. Control routing is shown in red.

Figure 78. Control Signals Group Routing Example



6.1.3. Command Signals – SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#

The Intel 855PM MCH command signals, SMA[12:0], SBS[1:0], SRAS#, SCAS#, and SWE# are common clocked signals. They are "clocked" into the DDR-SDRAMs using the clock signals SCK/SCK#[5:0]. The MCH drives the command and clock signals together, with the clocks crossing in the valid command window. There are two supported topologies for the command signal group. Section 6.1.3 is divided into two subsections; Topology 1 and Topology 2. Topology 1 is a daisy chain topology. Topology 2 implements a T routing topology. Both topologies place a series resistor between the two SO-DIMMs to damp SO-DIMM-to-SO-DIMM resonance. Topology 2 is the topology that best allows for placement of the SO-DIMMs back to back in the butterfly configuration, thus minimizing the SO-DIMM footprint area.

6.1.3.1. Command Topology 1 Solution

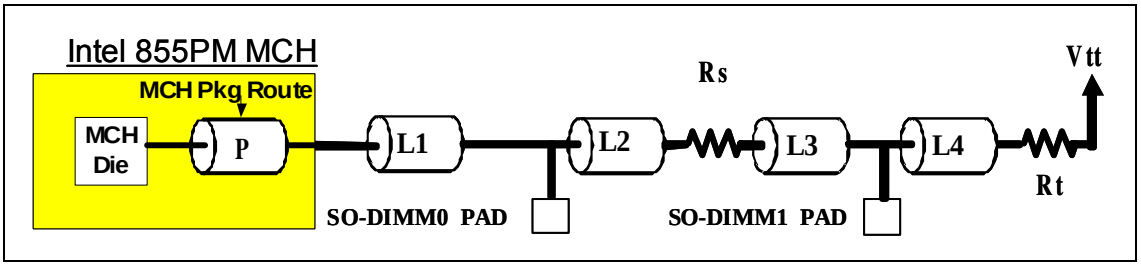
6.1.3.1.1. Routing Description for Command Topology 1

The command signal group routing starting from Intel 855PM MCH is as follows. The command signal routing should transition immediately from an external layer to an internal signal layer under the MCH. Keep to the same internal layer until transitioning back to an external layer immediately prior to connecting the SO-DIMM0 connector pad. At the via transition for SO-DIMM0, continue the signal route on the same internal layer to the series termination resistor (Rs), collocated to SO-DIMM1. At this resistor the signal should transition to an external layer immediately prior to the pad of Rs. After the series resistor, Rs, continue the signal route on the external layer landing on the appropriate connector pad of SO-DIMM1, or if necessary return to the same internal layer and return to external layer immediately prior to the connector pad of SO-DIMM1. After SO-DIMM1, transition to the same internal layer or stay on the external layer and route the signal to Rt.

It is suggested that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors but command signals can't be placed within the same R-packs as data, strobe, or control signals. The diagrams and tables below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1. Collocating the series resistor, Rs, and SO-DIMM1 allows for the elimination of one via from the signal route.

Figure 79. Command Signal Routing for Topology 1



The command signals should be routed using a 1:2 trace to space ratio for signals within the command group. There should be a minimum of 20 mils spacing to non-DDR related signals and DDR clock pairs SCK/SCK#[5:0]. Command signals should be routed on inner layers with minimized external traces.

Table 28. Command Topology 1 Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	Command – SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#		1
Motherboard Topology	Daisy Chain with Parallel Termination		
Reference Plane	Ground Referenced		
Characteristic Trace Impedance (Zo)	55 ± 15%		
Trace Width	Inner layers: 4 mils Outer layers: 5 mils		
Trace to Space ratio	1:2 (e.g. 4 mil trace to 8 mil space)		
Group Spacing	Isolation spacing for non-DDR related signals = 20 mils minimum		
Trace Length L1 – MCH Command Signal Ball to First SO-DIMM Pad	Min = 1.0 inch Max = 4.0 inches	Figure 79	3, 5
Trace Length L2 – First SO-DIMM Pad to Series Resistor Pad	Max = 1.1 inches	Figure 79	3
Trace Length L3 – Series Resistor Pad to Second SO-DIMM Pad	Max = 0.2 inches	Figure 79	3
Trace Length L4 – Second SO-DIMM Pad to Parallel Resistor Pad	Max = 0.8 inches	Figure 79	
Series Termination Resistor (Rs)	10 ± 5%		
Parallel Termination Resistor (Rt)	56 ± 5%		
Maximum Recommended Motherboard Via Count Per Signal	6		2, 4
Length Matching Requirements	Command Signals to SCK/SCK#[5:0] See Section 6.1.3.1.2 for details		

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using 4 vias if one via is shared that connects to the SO-DIMM1 pad and parallel termination resistor.
5. L1 trace length does not include MCH package length and should not be used when calculating L1 length.

6.1.3.1.2. Command Topology 1 to Clock Length Matching Requirements

The command signals must be 0.5 inches shorter to 1.0 inches longer than their associated differential clock pairs.

Length matching equation for SO-DIMM0:
X_1 = SCK/SCK#[2:0]
Y_1 = Command Signals = L1 of Figure 79 where:

$$(Y_1 – 1.0”) \quad X_1 \quad (Y_1 + 0.5”)$$

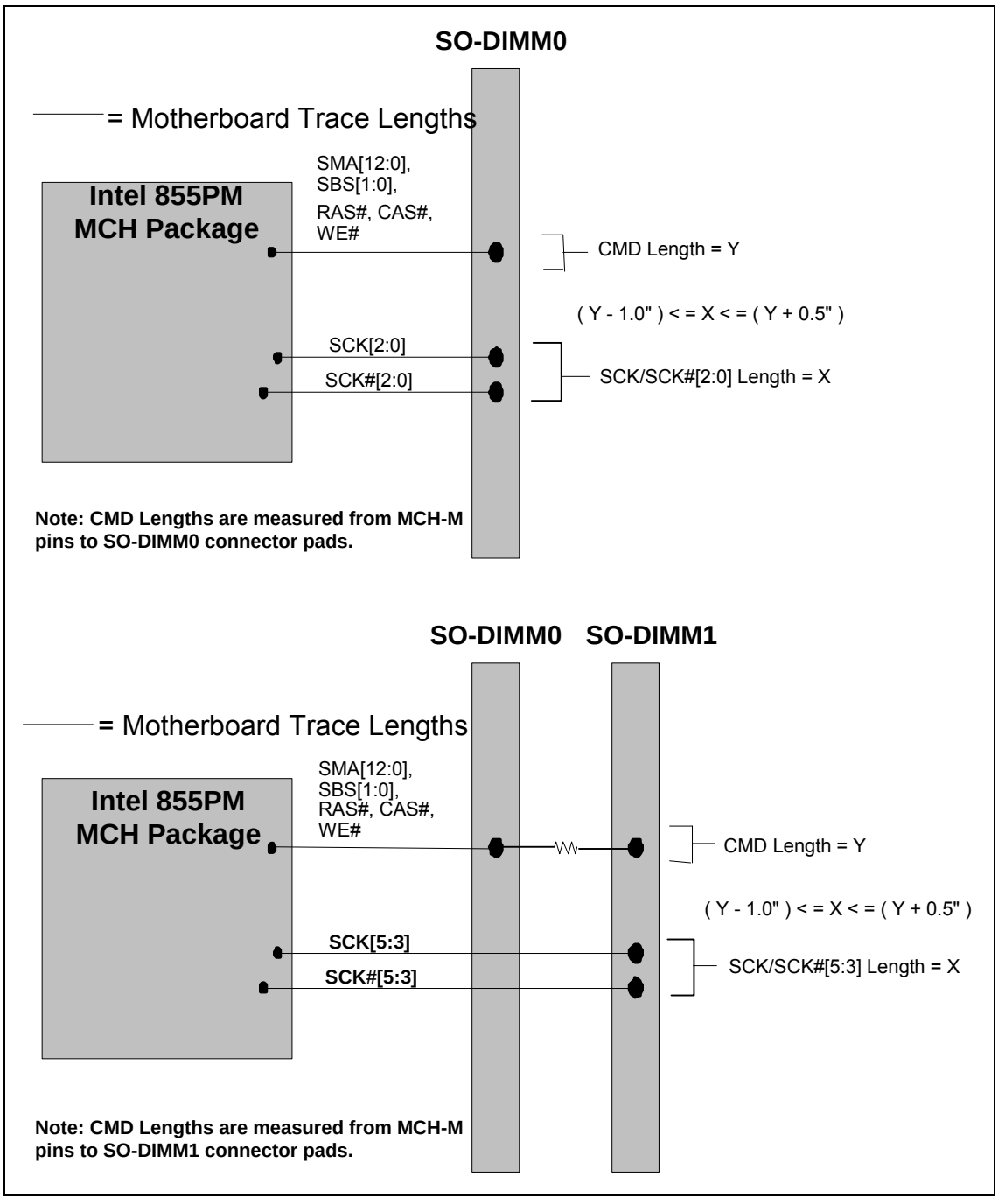
Length matching equation for SO-DIMM1:
X_2 = SCK/SCK#[5:3]
Y_2 = Command Signals = L1 + L2 + Rs Length + L3 of Figure 79 where:

$$(Y_2 – 1.0”) \quad X_2 \quad (Y_2 + 0.5”)$$

For example if the clock length of SCK/SCK#[2:0](X1) is 5.0 inches then the lengths of all command signal routing to SO-DIMM0 must be between 4.5” to 6.0”, if SCK/SCK#[5:3](X2) is 5.5 inches then the length of command signal routing to SO-DIMM1 must be between 5.0 inches to 6.5 inches. Figure 80 depicts the length matching requirements between the command and clock signals.

The MCH package lengths do not need to be taken into account for routing length matching purposes.

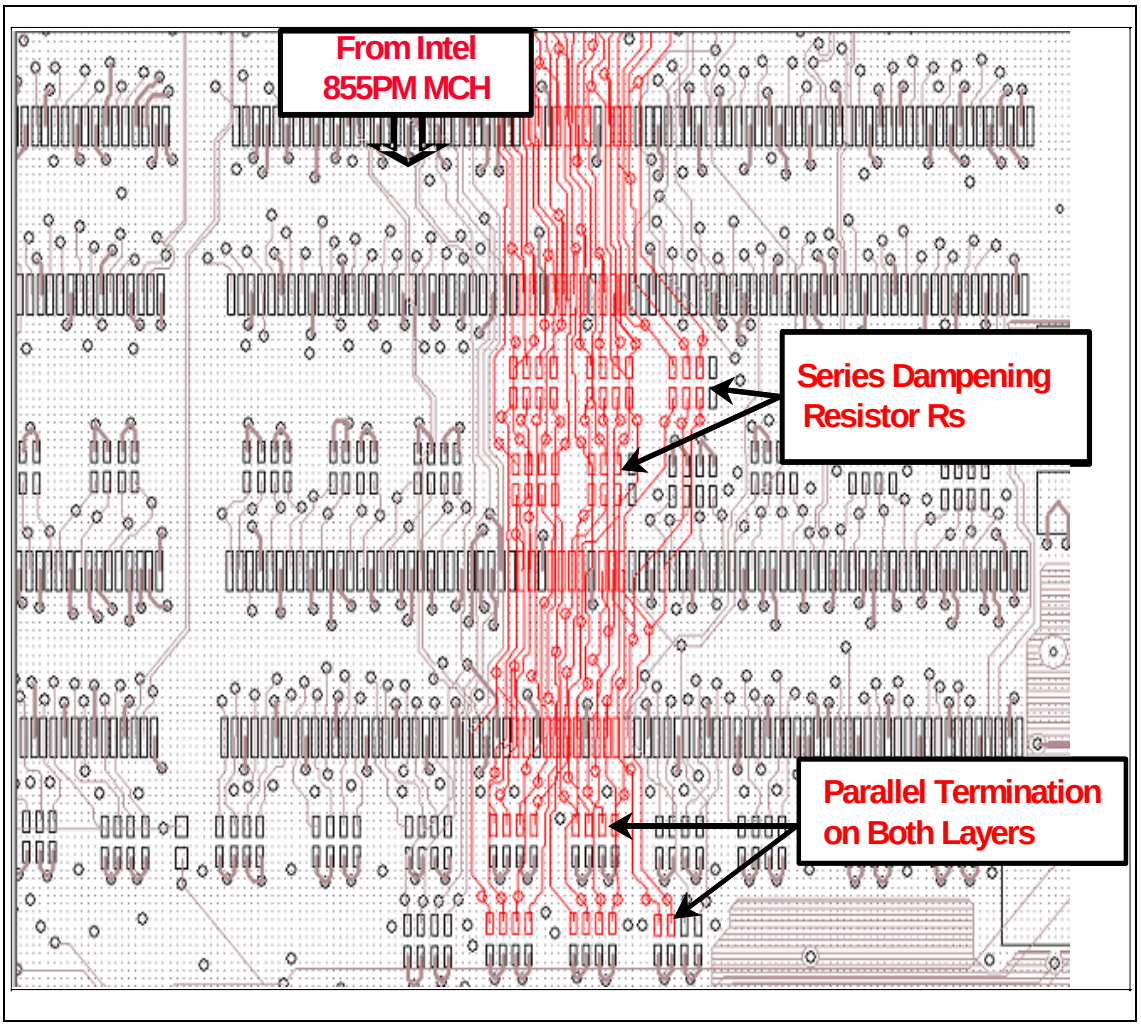
Figure 80. Command Signal to SCK/SCK# Trace Length Matching Requirements



6.1.3.1.3. Command Topology 1 Routing Example

Figure 81 is an example of a board routing for the Command signal group. Command routing is shown in red.

Figure 81. Command Signals Topology 1 Routing Example



6.1.3.2. Command Topology 2 Solution

6.1.3.2.1. Routing Description for Command Topology 2

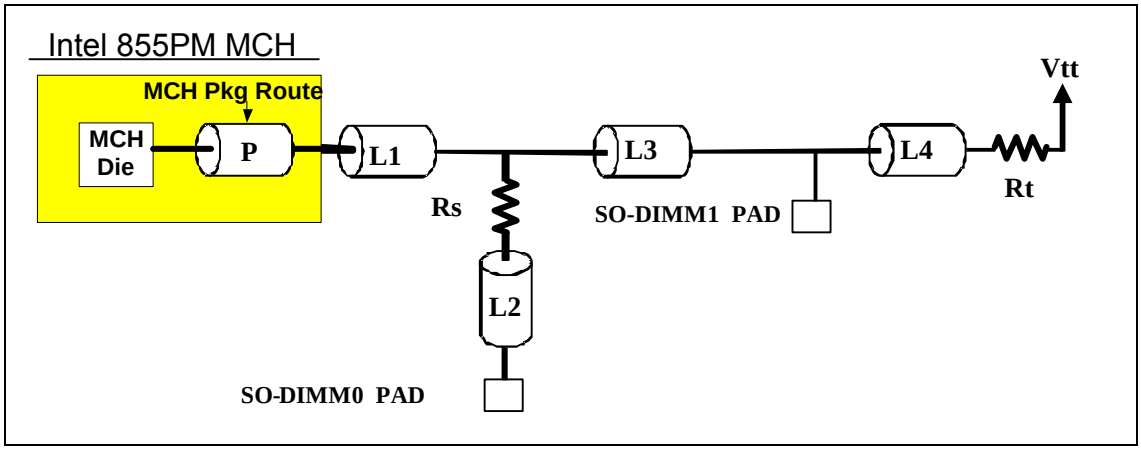
The command signal group routing starting from Intel 855PM MCH is as follows. The command signal routing should transition immediately from an external layer to an internal signal layer under the MCH. Keep to the same internal layer until transitioning back to an external layer at the series resistor Rs. At this point there is a T in the topology. One leg of the T will route through Rs and either transition back to the same internal layer or stay external and landing on the appropriate connector pad of SO-DIMM0. If it was necessary to return to the internal layer from Rs the signal should return to the external layer immediately prior to landing on the appropriate connector pad of SO-DIMM0. The other leg of the T will continue on the same internal layer and return to the external layer immediately prior to landing on the appropriate connector pad of SO-DIMM1. If possible stay on the external layer and connect to the parallel termination resistor or if the parallel termination resistor is on the opposite side of the board from the SO-DIMM1 connector then share the via and route to the parallel termination resistor. If sharing the via or using the opposite side of the board is not possible, continue on the same internal layer and route to the external layer immediately prior to the termination resistor.

External trace lengths should be minimized. Intel suggests that the parallel termination be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous. It is recommended that command signal group be routed on same internal layer.

It is suggested that the parallel termination (Rt) be placed on both sides of the board to simplify routing and minimize trace lengths. All internal and external signals should be ground referenced to keep the path of the return current continuous.

Resistor packs are acceptable for the series and parallel command termination resistors, but command signals can not be placed within the same R-packs as data, strobe or control signals. The diagrams and tables below depict the recommended topology and layout routing guidelines for the DDR-SDRAM command signals routing to SO-DIMM0 and SO-DIMM1.

Figure 82. Command Signal Routing for Topology 2



The command signals should be routed using 1:2 trace to space ratio for signals within the command group. There should be a minimum of 20 mils of spacing to non-DDR related signals and DDR clock

pairs SCK/SCK#[5:0]. Command signals should be routed on inner layers with minimized external trace lengths.

Table 29. Command Topology 2 Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	Command – SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#		1
Motherboard Topology	Daisy Chain with Parallel Termination		
Reference Plane	Ground Referenced		
Characteristic Trace Impedance (Zo)	55 ± 15%		
Trace Width	Inner layers: 4 mils Outer layers: 5 mils		
Trace to Space ratio	1:2 (e.g. 4 mil trace to 8 mil space)		
Group Spacing	Isolation spacing for non-DDR related signals = 20 mils minimum		
Trace Length L1 – MCH Command Signal Ball to Series Resistor 1 Pad	Min = 0.5 inches Max = 5.0 inches	Figure 82	3, 5
Trace Length L2 – Series Resistor Pad to First SO-DIMM Pad	Max = 1.0 inches	Figure 82	3
Trace Length L3 – Series Resistor Load to Second SO-DIMM Pad	Min = 0.4 inches Max = 1.75 inches	Figure 82	3
Trace Length L4 – Second SO-DIMM Pad to Parallel Resistor Pad	Max = 0.25 inches	Figure 82	
Series Termination Resistor (Rs)	10 ± 5%		
Parallel Termination Resistor (Rt)	56 ± 5%		
Maximum Recommended Motherboard Via Count Per Signal	6		2, 4
Length Matching Requirements	Command Signals to SCK/SCK#[5:0] See Section 6.1.3.2.2 for details		

NOTES:

1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. Power distribution vias from Rt to Vtt are not included in this count.
3. The overall maximum and minimum length to the SO-DIMM must comply with clock length matching requirements.
4. It is possible to route using 3 vias if one via is shared that connects L1, L3, and series termination and if one via is shared that connects to the SO-DIMM1 pad and parallel termination resistor.
5. L1 trace length does not include MCH package length and should not be used when calculating L1 length.

6.1.3.2.2. Command Topology 2 to Clock Length Matching Requirements

The command signals must be 0.5 inches shorter to 1.0 inches longer than their associated differential clock pairs.

Length matching equation for SO-DIMM0:
X_1 = SCK/SCK#[2:0]
Y_1 = Command Signals = L1 + Rs Length + L2 of Figure 82 where:

$$(Y_1 – 1.0”) \quad X_1 \quad (Y_1 + 0.5”)$$

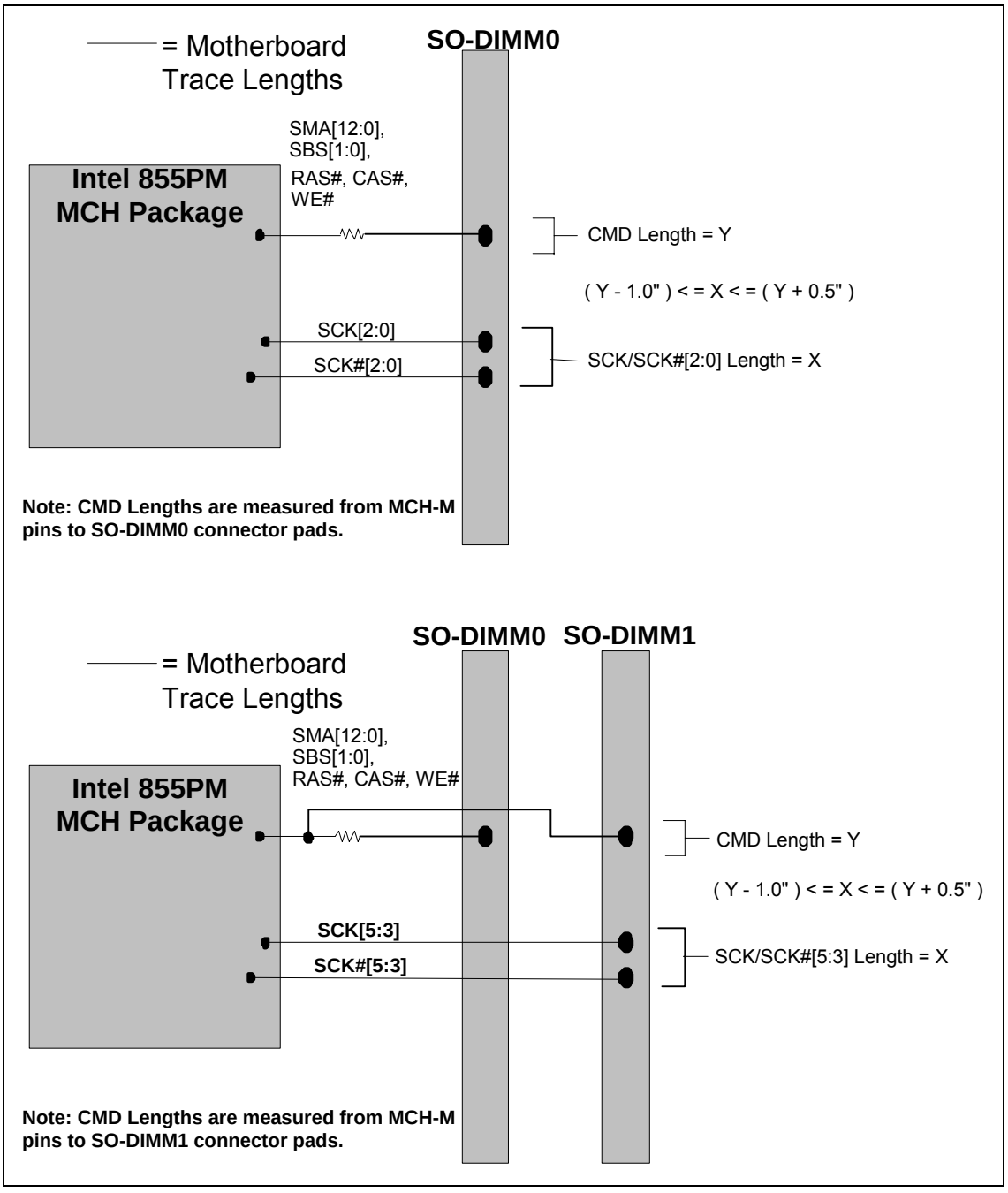
Length matching equation for SO-DIMM1:
X_2 = SCK/SCK#[5:3]
Y_2 = Command Signals = L1 + L3 of Figure 82 where:

$$(Y_2 – 1.0”) \quad X_2 \quad (Y_2 + 0.5”)$$

For example if the clock length of SCK/SCK#[2:0](X_1) is 5.0 inches then the length of all command signal routing to SO-DIMM0 must be between 4.5 inches to 6.0 inches, if SCK/SCK#[5:3](X_2) is 5.5 inches then the length of command signal routing to SO-DIMM1 must be between 5.0 inches to 6.5 inches. Figure 83 depicts the length matching requirements between the command and clock signals.

The MCH package lengths do not need to be taken into account for routing length matching purposes.

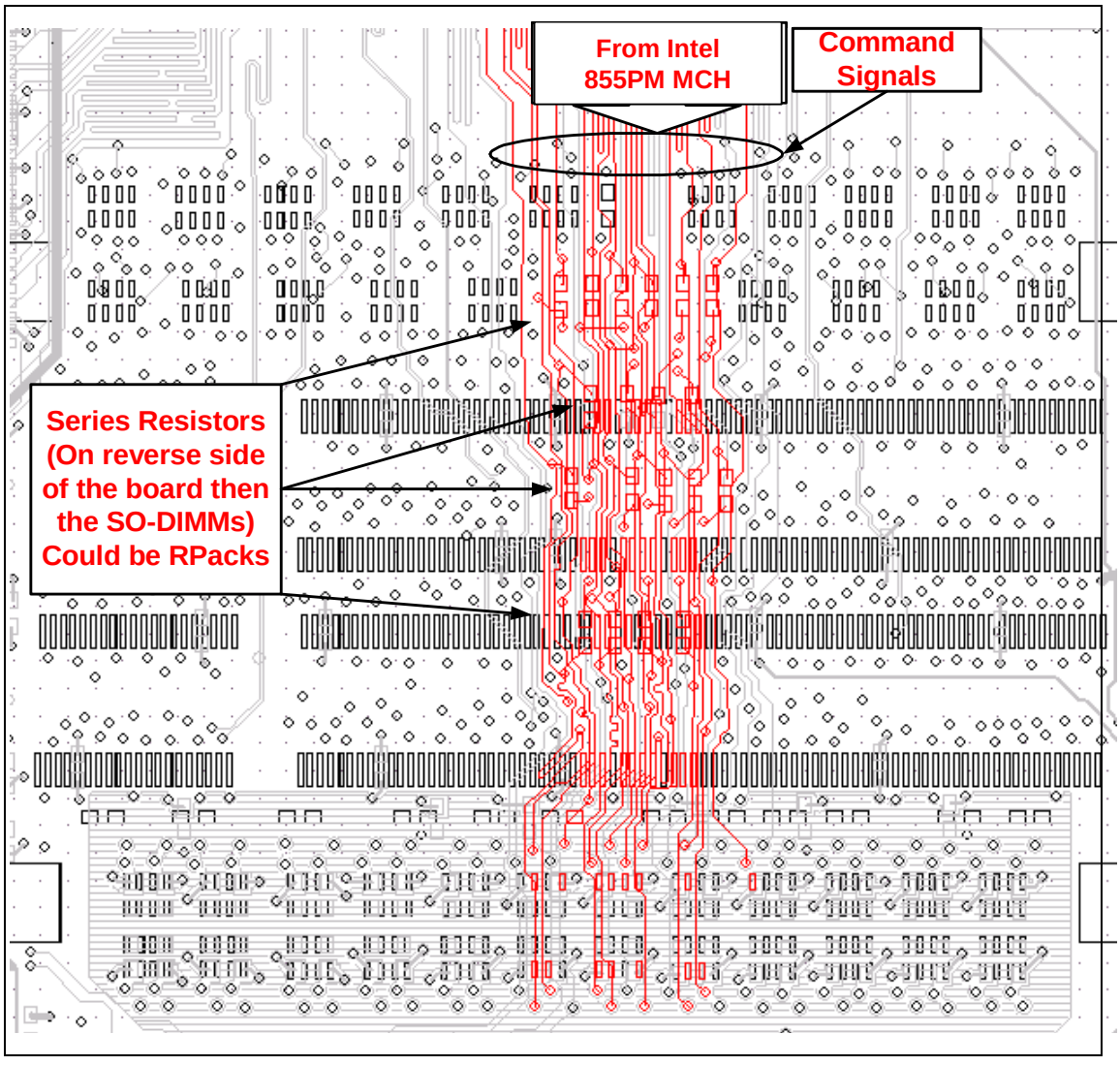
Figure 83. Command Signal to SCK/SCK# Trace Length Matching Requirements



6.1.3.2.3. Command Topology 2 Routing Example

Figure 84 is an example of a board routing for the Command signal group. Command routing is shown in red.

Figure 84. Command Signals Topology 2 Routing Example



6.1.4. Clock Signals – SCK[5:0], SCK#[5:0]

The clock signal group includes the differential clock pairs SCK[5:0] and SCK#[5:0]. The Intel 855PM MCH generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. The MCH only supports unbuffered DDR SO-DIMMs, three differential clock pairs are routed to each SO-DIMM connector. Table 30 summarizes the clock signal mapping.

Table 30. Clock Signal Mapping[1]

Signal	Relative To
SCK[2:0], SCK#[2:0]	SO-DIMM0
SCK[5:3], SCK#[5:3]	SO-DIMM1

NOTE: Assummes no clock pair swapping between SO-DIMMs and actual implementation may vary.

The one to one mapping of the clocks from the MCH to the SO-DIMM is not required. For example, it is not necessary that the SCKn/SCK#n clock pair from the MCH route to the same number clock on the SO-DIMM0 connector, which is CKn/CK#n in the *PC2100 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification*. This changing of clock numbering from MCH to SO-DIMMs may require additional BIOS setting changes. Swapping SCK and SCK# within a differential pair is not allowed. e.g. SCK1 and SCK1# may not be swapped at the SO-DIMM connector.

The clock differential pair routing starting from MCH is as follows. The clock differential pair routing should transition immediately from an external layer to an internal signal layer under the MCH and route as a differential pair referenced to ground for the entire length to their associated SO-DIMM connector pads. Immediately prior to the SO-DIMM connector the signals should transition to the same external layer as the SO-DIMM and connect the appropriate pad of the SO-DIMM connector.

External trace lengths should be minimized. All internal and external signal routing should be ground referenced to keep the path of the return current continuous. The diagrams and table below depict the recommended topology and layout routing guidelines for the DDR-SDRAM differential clocks.

Figure 85. DDR Clock Routing Topology (SCK/SCK#[5:0])

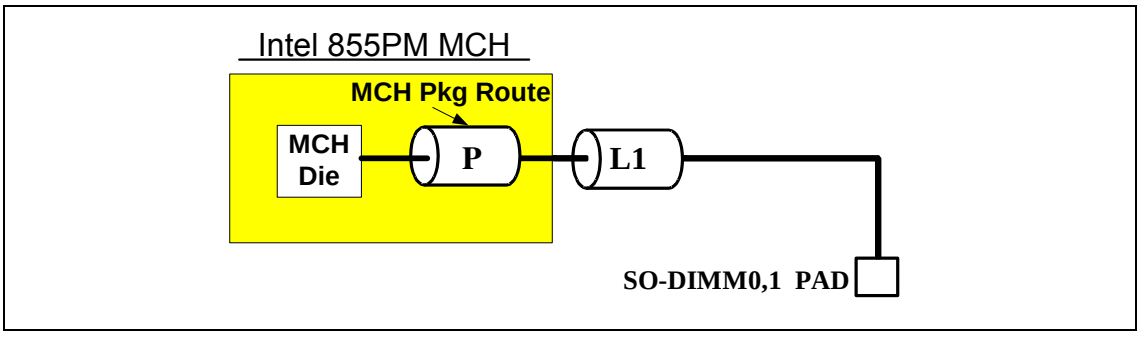


Table 31. Clock Signal Group Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	Clock – SCK[5:0], SCK#[5:0]		1
Motherboard Topology	Differential Pair Point-to-Point		
Reference Plane	Ground Referenced		
Characteristic Trace Impedance (Zo)	55 ± 15% (single ended)		
Trace Width (Option 1)	Inner layers: 4 mils Outer layers: 5 mils		5, 6
Trace Width (Option 2)	Inner layers: 7 mils Outer layers: 8 mils		5, 6
Differential Trace Spacing	Inner layers: 4 mils Outer layers: 5 mils		2
Group Spacing	Isolation spacing from another DDR signal group = 20 mils minimum Isolation spacing for non-DDR related signals = 20 mils minimum		
Trace Length L1 – MCH Clock Signal Ball to SO-DIMM Pad	Min = 0.5” Max = 5.5”	Figure 85	3, 4
Maximum Recommended Motherboard Via Count Per Signal	2		
Length Matching Requirements	SCK/SCK#[5:0] The 3 SO-DIMM0 clock pairs are equal in length plus tolerance and the 3 SO-DIMM1 clock pairs are equal in length plus tolerance See Section 6.1.4.1 for details		
Clock Pair-to-Pair tolerance	± 25 mils		
SCK to SCK# tolerance	± 10 mils		

NOTES:
1. Recommended trace lengths may change in a later revision of the design guide.
2. Spacing between SCK and SCK# within each differential pair should be implemented as follows with the following clock trace widths: for microstrips use 4-mil spacing, 4-mil or 7-mil trace width; for striplines use 5-mil spacing, 5-mil or 8-mil trace width.
3. The overall maximum and minimum length to the SO-DIMM must comply with DDR signal length matching requirements.
4. L1 trace length does not include MCH package length and should not be used when calculating L1 length.
5. Routing SCK/SCK# to a 7-mil trace width with 4-mil spacing is included as a design enhancement option. Simulations show improved timing margin resulting from use of a 7-mil clock trace width.
6. Option 1 **OR** Option 2 must be implemented for all SCK/SCK# pairs for a given design. The two options should not be combined within one design.

6.1.4.1. Clock Signal Length Matching Requirements

The Intel 855PM MCH provides three differential clock pair signals for each SO-DIMM. A differential clock pair is made up of a SCK signal and its complement signal SCK#.

The differential pairs for one SO-DIMM are:

SCK[0] / SCK#[0]
SCK[1] / SCK#[1]
SCK[2] / SCK#[2]

The differential pairs for the second SO-DIMM are:

SCK[3] / SCK#[3]
SCK[4] / SCK#[4]
SCK[5] / SCK#[5]

The differential clock pairs' motherboard routing must be matched to ± 25 mils. Each SCK to SCK# pair motherboard routing must be matched to ± 10 mils. Figure 86 and Figure 87 depict the length matching requirement between SCK/SCK# and clock pairs, respectively.

For information covering the data and data strobe to clock length matching requirements reference Section 6.1.1.2, for information covering the control signal to clock length matching requirements reference Section 6.1.2.1, and for information covering the command signal to clock length matching requirements reference Section 6.1.3.1.2 for Topology 1 and Section 6.1.3.2.2 for Topology 2. Refer Section 6.1.5.1 for package trace length data.

Figure 86. SCK/SCK# Trace Length Matching Requirements

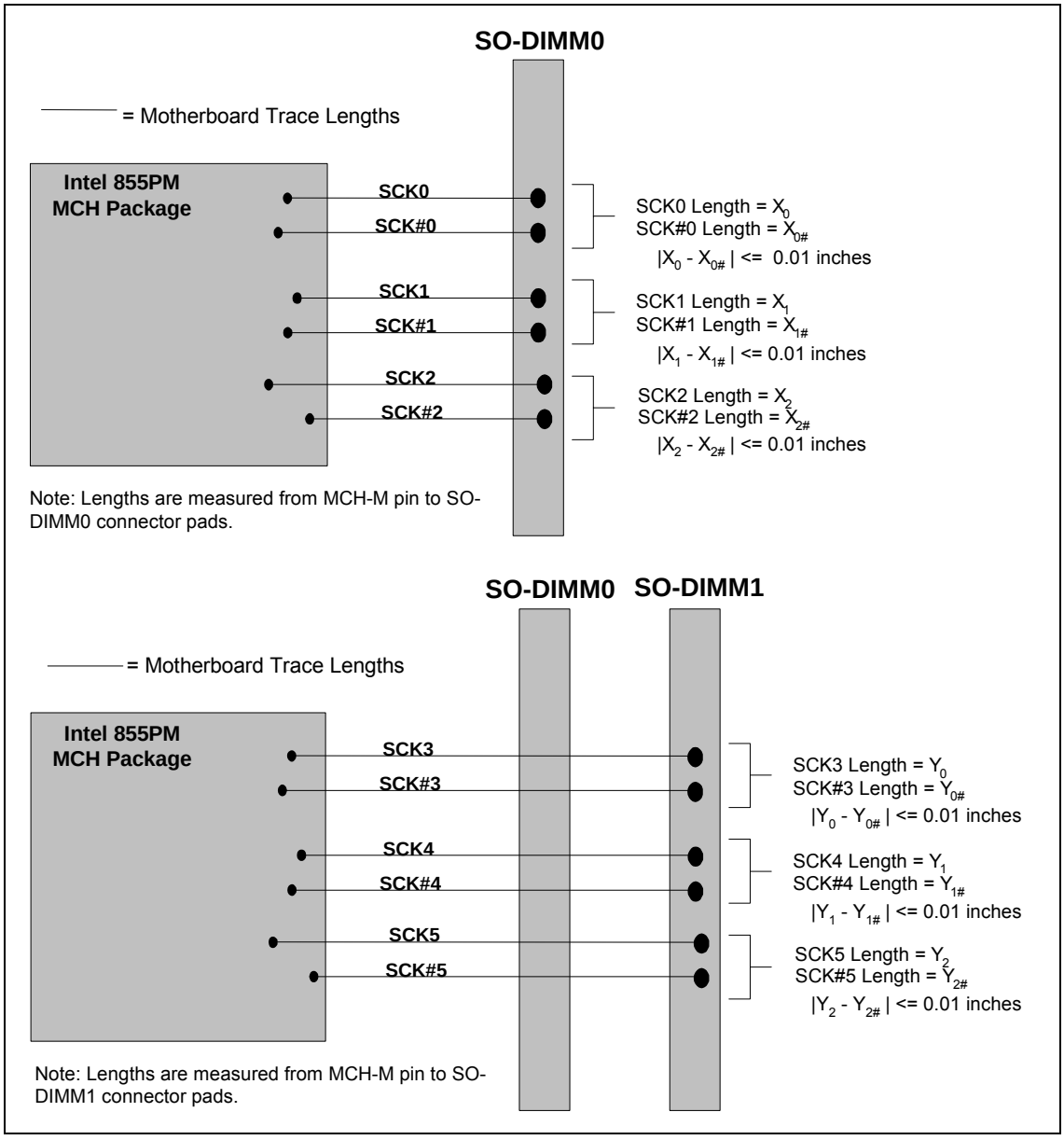
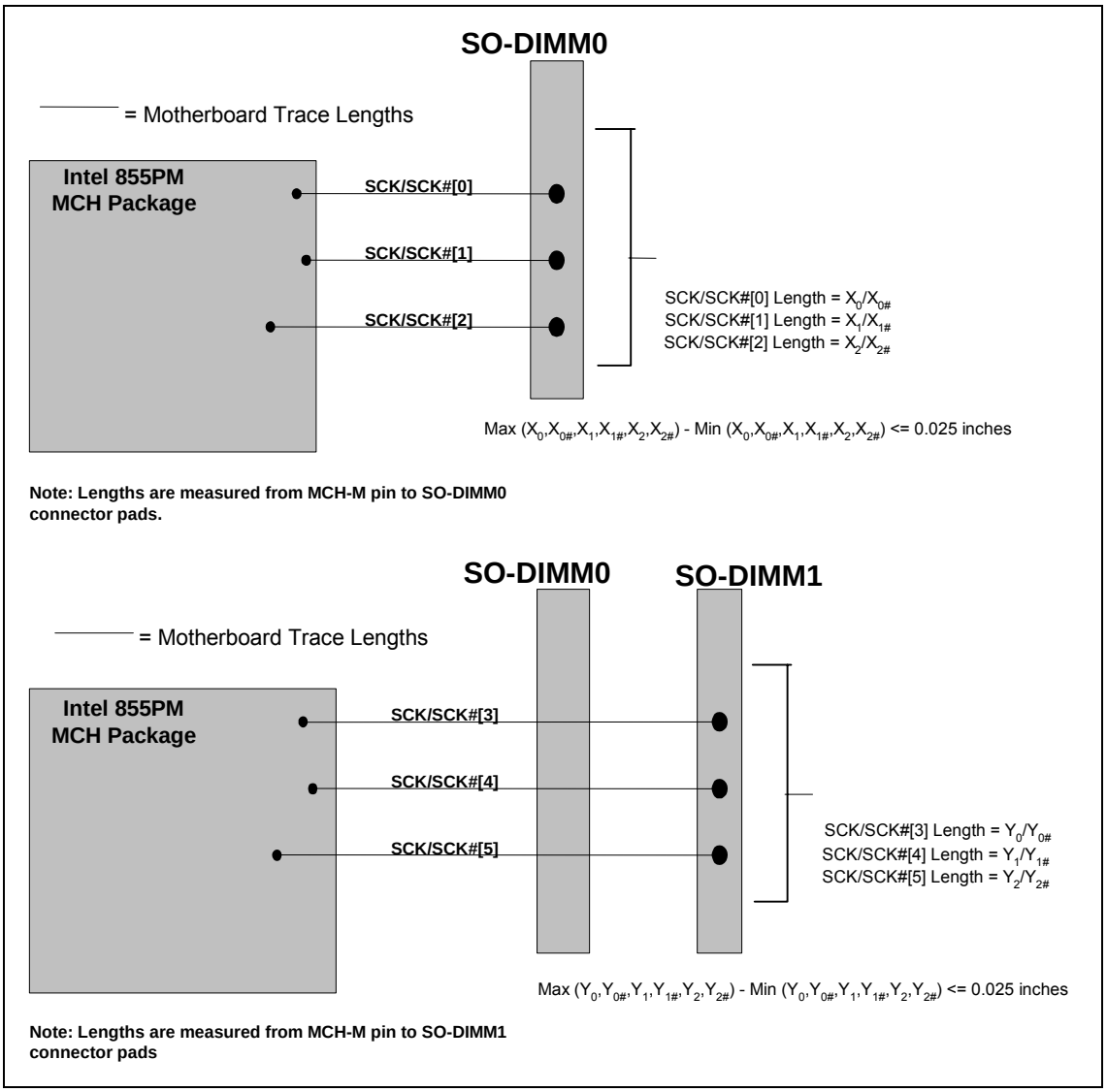


Figure 87. Clock Pair Trace Length Matching Requirements[1]

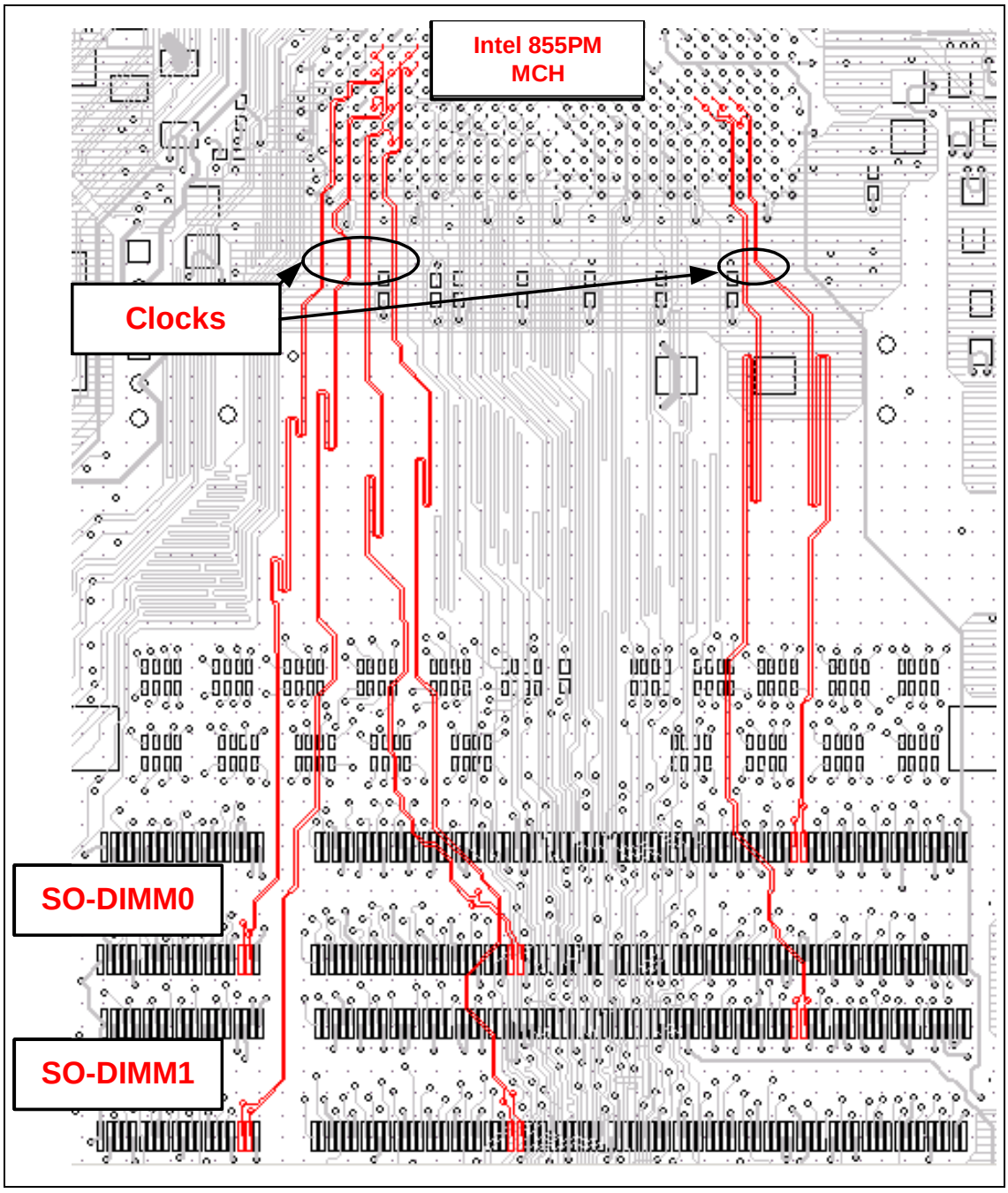


NOTE: Length matching between DQS and Clock pairs must include package length.

6.1.4.1.1. Clock Routing Example

Figure 88 is an example of a board routing for the Clock signal group. Clock routing is shown in red.

Figure 88. Clock Signal Routing Example



6.1.4.2. Intel 855PM Chipset High Density Memory Support

The 855PM chipset architecture supports 2-GB of system memory. This memory capacity can be achieved using "high-density" memory devices of various package types. Intel has done only limited simulation and bench testing on these high-density SO-DIMM memory modules and has not seen any functional or analog inspection failures using existing layout guidelines. Due to a lack of JEDEC standard for high density memory; however, Intel has not done complete simulation nor validation with all the available package configurations. Customers are strongly encouraged to perform complete validation on their platforms based on the particular high-density memory package of their choice.

6.1.5. Feedback – RCVENOUT#, RCVENIN#

The Intel 855PM MCH provides a feedback signal called "receive enable" (RCVEN#), which is used to gate the strobe inputs for read data. There are two pins on the MCH to facilitate the use of RCVEN#. The RCVENOUT# pin is an output of the MCH and the RCVENIN# pin is an input to the MCH. RCVENOUT# must connect directly to RCVENIN#.

The diagrams and table below depict the recommended topology and layout routing guidelines for the DDR-SDRAM feedback signal**. The RCVEN# signal must be routed on the same layer as the system memory clocks**. The RCVEN# routing starting from MCH is as follows. RCVEN# should transition immediately from the same external signal layer as MCH to the same internal signal layer as memory clocks under the MCH, routed referenced to ground for the entire length. RCVEN# should then transition from the internal signal layer back to the same external layer as MCH and connect the RCVENIN# of MCH. External trace lengths should be minimized. All internal (segment L2) and external layer signal routing (segments L1 and L3) should be ground referenced to keep the path of the return current continuous.

Figure 89. DDR Feedback (RCVEN#) Routing Topology

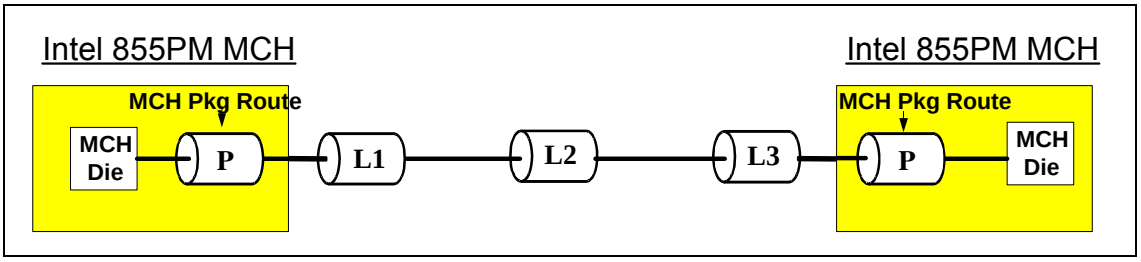


Table 32. Feedback Signal Routing Guidelines

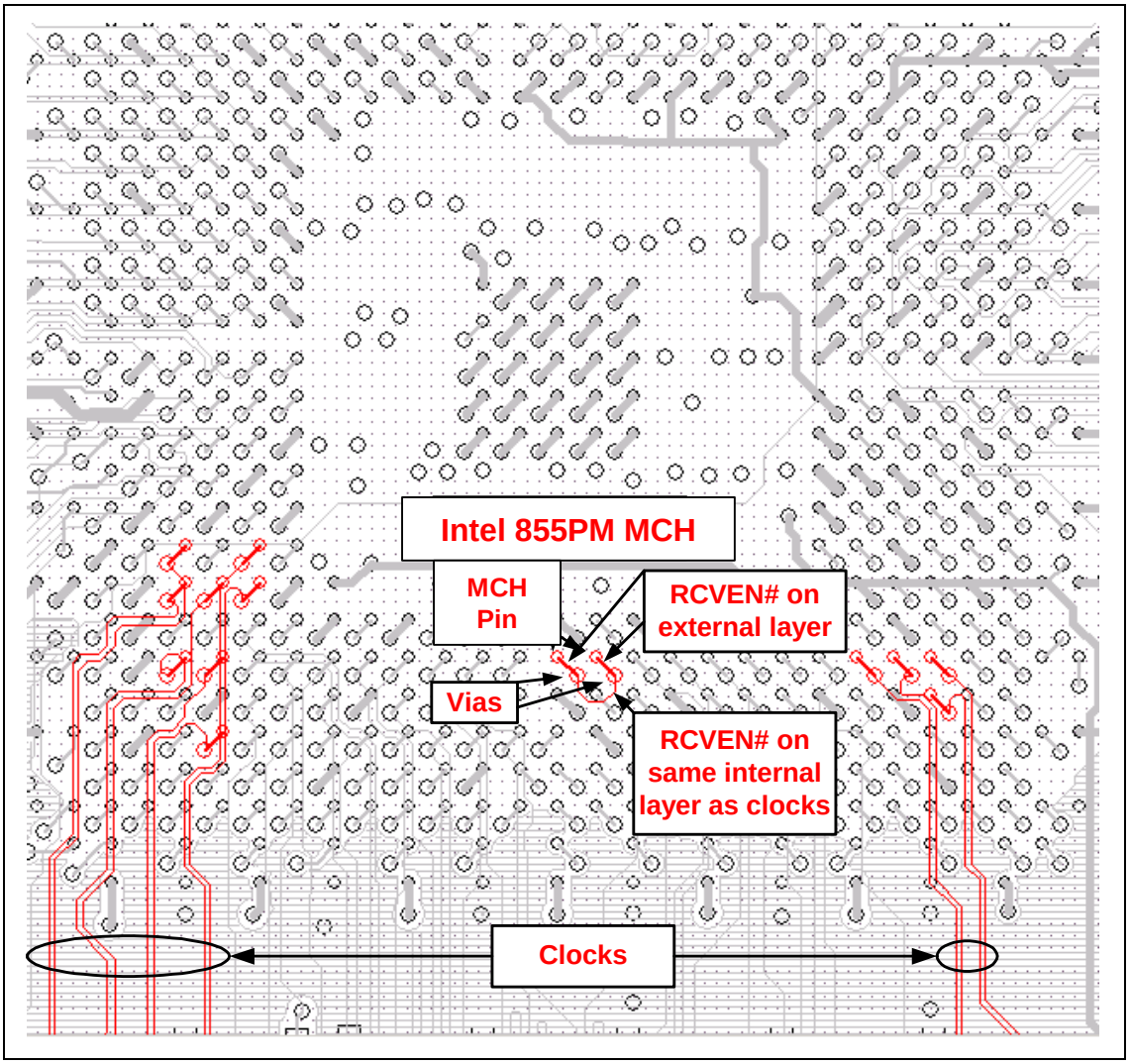
Parameter	Routing Guidelines	Figure	Notes
Signal Group	Feedback – RCVENOUT#, RCVENIN#		1
Motherboard Topology	Point-to-Point		
Reference Plane	Ground Referenced		
Characteristic Trace Impedance (Zo)	55 ± 15% (single ended)		
Trace Width	Inner layers: 4 mils Outer layers: 5 mils		
Group Spacing	Isolation spacing from another DDR signal group = 20 mils minimum Isolation spacing for non-DDR related signals = 20 mils minimum		
Trace Length L1 – MCH Feedback Signal Pin to Signal Via	Max = 40 mils	Figure 89	2
Trace Length L2 – MCH RCVENOUT# Signal Via to RCVENIN# Signal Via	Must = 100 mils ± 5mils	Figure 89	
Trace Length L3 – Signal Via to MCH Feedback Signal Pin	Max = 40 mils	Figure 89	3
Maximum Recommended Motherboard Via Count Per Signal	2		
Length Matching Requirements	None		

NOTES:
1. Recommended trace lengths may change in a later revision of the design guide.
2. L1 trace length does not include MCH package length and should not be used when calculating L1 length.
3. L3 trace length does not include MCH package length and should not be used when calculating L3 length.

6.1.5.1. RCVEN# Routing Example

Figure 90 is an example of a board routing implementation for the RCVEN# signal. Clock routing is show in red.

Figure 90. RCVEN# Signal Routing Example



6.1.6. Support for "DDP Stacked" SO-DIMM Modules

Simulations have been performed to verify the suitability of the DDR layout and routing guidelines to support the use of 512-Mbit technology-based (two 256-Mbit dies within the same package), "DDP stacked", 2x8 SO-DIMM memory modules on Intel 855PM chipset based platforms. For the purpose of this discussion, the term "DDP stacked" is used to refer to DDP SDRAM based 2x8 SO-DIMM memory modules. Based on these simulations, the current routing guidelines can support this type of stacked memory device. Other stacked devices have not been simulated and therefore cannot be recommended. Please see Section 6.1.4 for clock signal group related routing updates.

6.1.7. Recommended Design Option to Support PC2700 DDR SDRAM with Existing PC1600 and PC2100 Intel 855PM Platforms

The following sections document the currently available design option for enabling PC2700 DDR SDRAM support based on existing platform layouts.

6.1.7.1. Shortened Data Signal Group Trace Length

Modifications to current platforms to support PC2700 are possible by reducing the overall motherboard trace length for the data signal group if current trace lengths exceed the PC2700 trace length guidelines. This includes all DDR data signals, SDQ[71:0], and data strobe signals, SDQS[8:0].

Design guidelines for supporting PC2700 based on an existing PC1600 and PC2100 layout are presented in Section 6.2.7.1.1. A list of general design considerations for adapting current platforms to support PC2700 is summarized in Section 6.2.7.1.2.

6.1.7.1.1. Supporting PC2700 Based on an Existing PC Platform Layout

While the maximum length of L1, L2, L3, and L4 remains unchanged from previous revisions of this design guide, the maximum overall length allowed from the MCH-M to the second SO-DIMM (L1 + Rs + L2 + L3) for PC2700 support is limited to 4.5 inches. This represents a reduction of 1.0 inches compared to that allowed for PC2100 and PC1600 design guidelines. As a result, platforms based on current PC2100 and PC1600 layout guidelines may require a reduction in trace lengths of up to 1.0 inches, in order to meet the PC2700 maximum data signal group length requirements.

Figure 91. Data Signal Group (SDQ[71:0], SDQS[8:0]) Routing Topology – PC2700, PC2100 and PC1600 Compliant

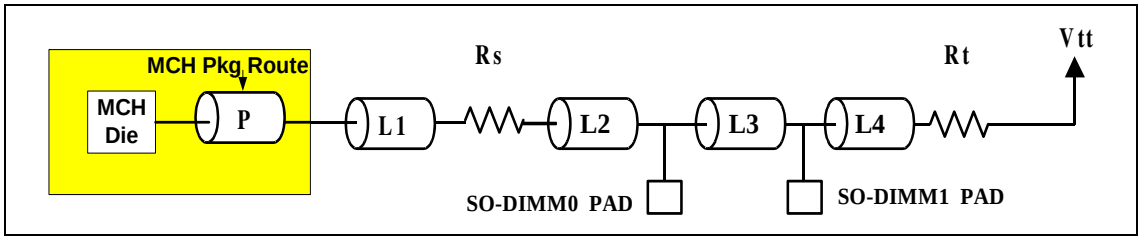


Table 33. Data Signal Group (SDQ[71:0], SDQS[8:0]) Routing Guidelines – PC2700, PC2100 and PC1600 Compliant

	L1	L2	L3	L4	Rs	Rt	L1 + Rs + L2 + L3
DDR Data Signal Group (for platform supporting PC2700, PC2100, PC1600 DDR SDRAM)	Min = 0.5” Max = 3.75”	Min = 0” Max = 0.75”	Min = 0” Max = 1.0”	Min = 0” Max = 0.8”	22.6 ± 1%	54.9 ± 1%	**Min = 0.5”** **Max = 4.5**”
DDR Data Signal Group (for platform supporting PC2100 and PC1600 DDR SDRAM)	Min = 0.5” Max = 3.75”	Min = 0” Max = 0.75”	Min = 0” Max = 1.0”	Min = 0” Max = 0.8”	22.6 ± 1%	54.9 ± 1%	Min = 0.5” Max =5.5”

6.1.7.1.2. Additional Design Considerations for Adapting Intel 855PM DDR 200/266 MHz Platforms To Support PC2700

In addition to meeting the updated routing length requirements specified in Section 6.2.7.1, future DDR 333-MHz platforms must also adhere to all other existing design guidelines for the DDR 200-MHz and 266-MHz platforms. Table34 contains section references to all other existing design guidelines that need to be followed for the different signal groups.

Table 34. Existing PC2100/PC1600 DDR SDRAM Design Guidelines Required for PC2700 Support

Group	Signal	Section Reference
Data	SDQ[71:0]; SDQS[8:0]	6.2.1
Control	SCKE[3:0]; SCS#[3:0]	6.2.2
Command	SMA[12:0]; SBS[1:0]; SRAS#; SCAS#; SWE#	6.2.3
Clock	SCK[5:0]; SCK#[5:0]	6.2.4
Feedback	RCVENOUT#; RCVENIN#	6.2.5

6.2. Intel 855PM MCH DDR Signal Package Lengths

The signals listed in Table 35 are routed with 55 ± 15% micro-strip transmission lines. Signals within the same group are trace length matched within 0.1 mils inside the package. Thus, motherboard routing does not need to compensate for trace length mismatch in the package for these signals.

Table 35. Intel 855PM Chipset DDR Signal Package Lengths

Data Signal Name	Intel 855PM MCH Package Trace Length (mils)	Data Signal Name	Intel 855PM MCH Package Trace Length (mils)
DATA GROUP 1		**DATA GROUP 6**	
SDQ[7:0]	945	SDQ[47:40]	732
SDQS[0]	945	SDQS[5]	732
DATA GROUP 2		**DATA GROUP 7**	
SDQ[15:8]	873	SDQ[55:48]	850
SDQS[1]	873	SDQS[6]	850
DATA GROUP 3		**DATA GROUP 8**	
SDQ[23:16]	765	SDQ[63:56]	950
SDQS[2]	765	SDQS[7]	950
DATA GROUP 4		**DATA GROUP 9**	
SDQ[31:24]	658	SDQ[71:64]	646
SDQS[3]	658	SDQS[8]	646
DATA GROUP 5			
SDQ[39:32]	649		
SDQS[4]	649		
DIFFERENIAL CLOCKS			
SCK[5:0]	661	SCK[5:0]#	661
COMMAND – SMA			
SMA[0]	462	SMA[7]	515
SMA[1]	441	SMA[8]	446
SMA[2]	481	SMA[9]	523
SMA[3]	537	SMA[10]	404
SMA[4]	434	SMA[11]	536
SMA[5]	548	SMA[12]	538
SMA[6]	510		
COMMAND – SBS			
SBS[0]	423	SBS[1]	398

Data Signal Name	Intel 855PM MCH Package Trace Length (mils)	Data Signal Name	Intel 855PM MCH Package Trace Length (mils)
COMMAND – Misc			
SCAS#	491	SRAS#	447
SWE#	401		
CONTROL – SCKE			
SCKE[0]	557	SCKE[2]	506
SCKE[1]	600	SCKE[3]	573
CONTROL – SCS#			
SCS#[0]	516	SCS#[2]	516
SCS#[1]	539	SCS#[3]	610
RECEIVE ENABLE			
RCVENOUT#	661	RCVENIN#	348

6.3. DDR System Memory Interface Strapping

The Intel 855PM MCH has pins that require termination for proper component operation.

For the MCH, the ST[0] pin does not require any strapping for normal operation. This signal has an internal pull-up that straps the MCH for DDR memory during reset. However, a stuffing option for a 1-k ± 5% pull-up to a 1.5-V source can be provided for testing purposes.

6.4. ECC Disable Guidelines

The Intel 855PM MCH can be configured to operate in an ECC data integrity mode that allows for multiple bit error detection and single bit error correction. This option to design for and support ECC DDR memory modules is dependent on design objectives. By default, ECC functionality is disabled on the platform. For designs that support ECC memory, see Sections 6.1.1 and 6.1.4 for details on signal topologies and routing guidelines.

6.4.1. Intel 855PM MCH ECC Functionality Disable

If non-ECC memory modules are to be the only supported memory type on the platform, then the eight DDR check bits signals, associated strobe, and differential clock pairs associated with the ECC device for each SO-DIMM can be left as no connects on the Intel 855PM MCH. This includes SDQ[71:64], SDQS8, and the two differential clock pairs that are not routed to the SO-DIMMs. The following discussion mentions details for the MCH system memory registers.

The DRAM Data Integrity Mode (DDIM) bit of the DRC register (Device 0; Offset 7C-7Fh; bit 21) provides the option to enable or disable ECC operation mode in the MCH. By default, this bit is set to ‘0’ and ECC functionality is disabled. In such a case, the SDQ[71:64] and SDQS eight pins of the MCH can be left as no connects.

The DRAM Clock Control Disable Register (DCLKDIS: I/O Address 2E-2Fh) provides the capability to enable and disable the CS/CKE and SCK signals to unpopulated SO-DIMMs. Although DDR SO-DIMM connectors may provide motherboard lands for three clock pairs, Intel design recommendations only support non-ECC SO-DIMMs that require two pairs. The MCH provides the flexibility to route any differential clock pair to any SCK clock pair on the SO-DIMMs provided that the BIOS enables/disables these clocks appropriately (e.g. the MCH's SCK0 pair can be routed either to the SO-DIMM's SCK0 pair or any other pair such as SCK1 or SCK2, etc.). By default, the enable/disable bits for the clock pairs are set to '1' and are disabled or tri-stated. To further reduce EMI/noise and save power, the SCK clock pair pins of the MCH that are normally routed to ECC devices on ECC memory modules can be left as no connects.

On platforms where ECC memory is supported, it is important that all relevant SDQ, SDQS, and SCK signals to the SO-DIMMs be disabled when the system is populated with only non-ECC or a combination of ECC and non-ECC memory. In such cases, the registers mentioned above must be programmed appropriately.

6.4.2. DDR Memory ECC Functionality Disable

It is imperative that systems that do not support ECC memory ensure the SCK clock pairs that are normally sent to ECC SO-DIMMs be disabled. If the SCK clock pairs associated with the check bit signals were left floating in a non-ECC memory only system and ECC memory was used in one or more of the SO-DIMM slots, this could cause the ECC device on the SO-DIMM to be enabled. If SDQ[71:64] is disabled/tri-stated or not routed, then these floating inputs can cause the ECC device to draw current and potentially compromise the ECC device.

Previous revisions of this design guide provided guidelines that required additional hardware termination to address the potential issue of floating inputs on an ECC SO-DIMM when populated in a non-ECC memory only system. Since then, further analysis has been done and the new recommendation is that **no hardware termination is required** on the SDQ[71:64], SDQS8, and SCK clock pair inputs of the SO-DIMM connector.

This simplifies and provides the most reasonable hardware design recommendation that offers tradeoffs between protecting any ECC memory inadvertently populated into the system vs. utilizing all physical memory available in a system while incurring no power penalty.

6.5. System Memory Compensation

See Section 11.5.4 for details.

6.6. SMVREF Generation

See Section 11.5.3.1 for details.

6.7. DDR Power Delivery

See Section 11.5 for details.

6.8. External Thermal Sensor Based Throttling (ETS#)

The Intel 855PM MCH's ETS# input pin is an active low input that can be used with an external thermal sensor to monitor the temperature of the DDR SO-DIMMs for a possible thermal condition. Assertion of ETS# will result in the limiting of DRAM bandwidth on the DDR memory interface to reduce the temperature in the vicinity of the system memory.

By default, the functionality and input buffer associated with ETS# are disabled. Also, the MCH can be programmed to send an SERR, SCI, or SMI message to the ICH4-M upon the assertion of this signal. External thermal sensors that are suitable for the purpose described above would need to have a small form factor and be able to accurately monitor the ambient temperature in the vicinity of the DDR system memory.

Intel is currently in the process of enabling this feature on the MCH and is actively engaging with thermal sensor vendors to ensure compatibility and suitability of vendors' products with the ETS# pin. This includes electrical design guidelines for the ETS# pin and usage/placement guidelines of the thermal sensors for maximum effectiveness. Current third party vendor product offerings that may be suitable for the ETS# pin application include ambient temperature thermal sensors and remote diode thermal sensors. Also, thermal sensors that implement an open-drain output for signaling a thermal event would provide the most flexibility from an electrical and layout design perspective.

6.8.1. ETS# Usage Model

The thermal sensors targeted for this application with the Intel 855PM MCH's ETS# are planned to be capable of measuring the ambient temperature only and should be able to assert ETS# if the preprogrammed thermal limits/conditions are met or exceeded. Because many variables within a mobile system can affect the temperature measured at any given point in a system, the expected usage and effectiveness of ETS# is also very focused. Because of factors such as thermal sensor placement, airflow within a mobile chassis, adjacent components, thermal sensor sensitivity, and thermal sensor response time, ETS# can effectively be used for controlling skin temperatures. However, due to the location of the thermal sensor ETS# should not be used for measuring or controlling the Tj or Tcase parameters of DDR-SDRAM devices since it cannot respond quickly enough to dynamic changes in DRAM power.

6.8.2. ETS# Design Guidelines

ETS#, as implemented in the Intel 855PM MCH, is an active low signal and does **not** have an integrated pull-up to maintain a logic '1'. As a result of this, a placeholder for an external 8.2-k to 10-k pull-up resistor should be provided near the ETS# pin. Electrical details on output characteristics of suitable thermal sensors for use with the MCH are currently not finalized. The recommended pull-up voltage for this external pull-up is 2.5 V (VCCSM). Ideally, the thermal sensor should implement an open drain type output buffer to drive ETS#. A system is expected to have one thermal sensor per SO-DIMM connector on the motherboard. As a result, routing guidelines for the output of these thermal sensors to the ETS# pin will also be important.

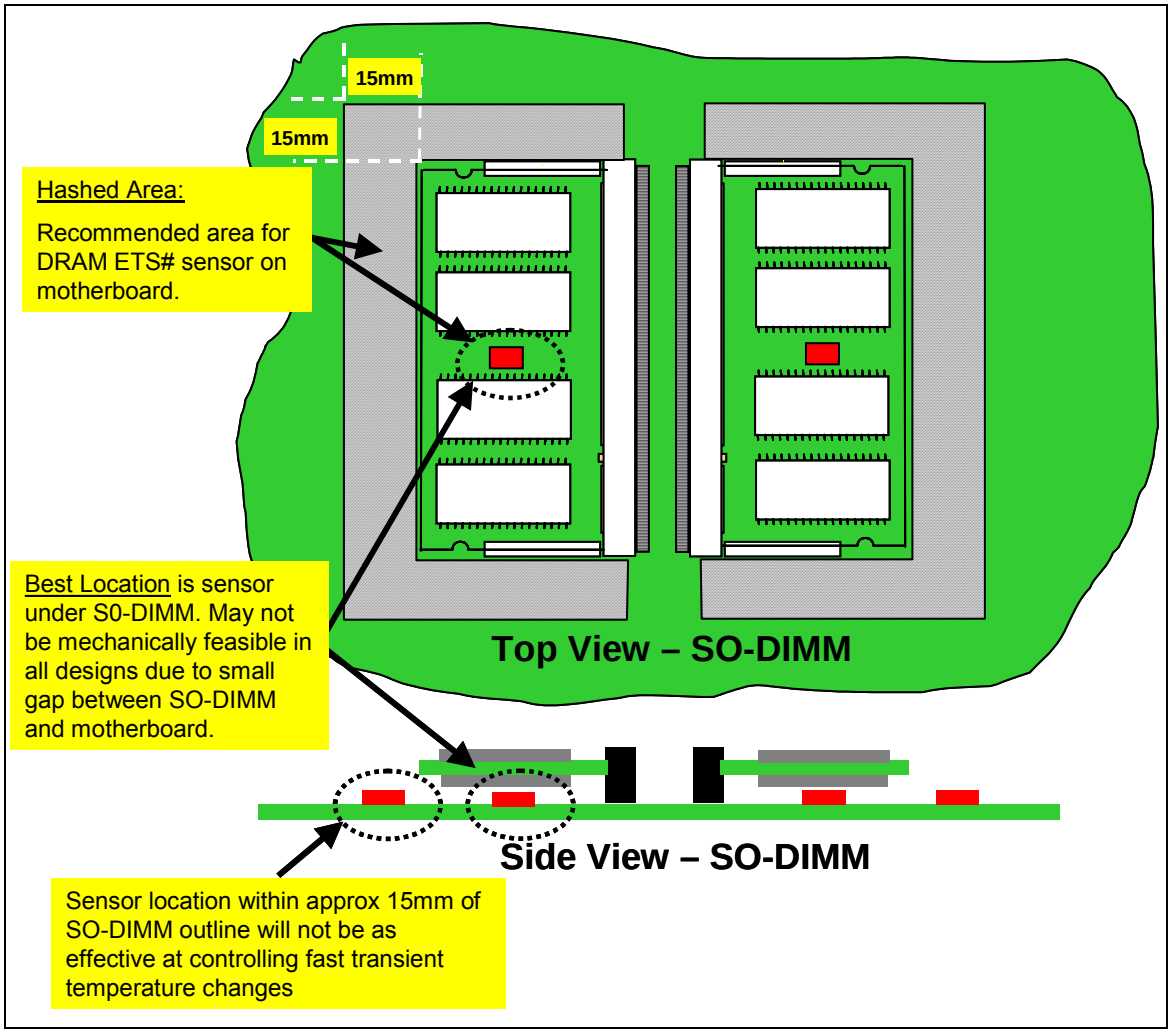
Routing guidelines and other special, motherboard design considerations will vary with the vendor and type of thermal sensor chosen for this ETS# application. As a result, vendor specific design guidelines should also be followed closely to ensure proper operation of this feature. As a general rule, system designers should follow good design practices in ensuring good signal integrity on this signal as well as achieving adequate isolation from adjacent signals. Also, any thermal design considerations (e.g. proper ground flood placement underneath the external thermal sensor; proper isolation of the differential signal routing for thermal diode applications, etc.) for the external thermal sensor itself should also be met.

6.8.3. Thermal Sensor Placement Guidelines

The many factors that can affect the accuracy of ambient temperature measurements by thermal sensors make the placement of them a very critical and especially challenging task. Ideally, one thermal sensor should be placed near each SO-DIMM in a system. The thermal sensor should be located in an area where the effects of airflow and effects of conduction from adjacent components are minimized. This allows for the best correlation of thermal sensor temperature to chassis or notebook surface temperature. Refer to Figure 92 for details.

Assuming airflow is negligible within a system, the optimal placement of the thermal sensor is on the surface of the motherboard directly beneath the shadow of an SO-DIMM module centered longitudinally and laterally in relation to the outline of the SO-DIMM. The thermal sensor should have a form factor small enough to allow it to fit beneath double-sided memory modules (i.e. modules with memory devices on both sides of a module). If placement within the outline of an SO-DIMM is not possible, then the next best option is to locate it within approximately 15 mm (0.6 inches) of the outline/SO-DIMM shadow. Again, this assumes negligible effects from airflow.

Figure 92. DDR Memory Thermal Sensor Placement



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7. AGP Port Design Guidelines

For detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to the latest *AGP Interface Specification*, *Revision 2.0*, which can be obtained from http://www.agpforum.org. This design guide focuses only on specific Intel 855PM chipset platform recommendations.

7.1. AGP Interface

The *AGP Interface Specification Revision 2.0* enhances the functionality of the original AGP Interface Specification (revision 1.0) by allowing 4X data transfers (4 data samples per clock) and 1.5-volt operation. In addition to these major enhancements, additional performance enhancement and clarifications, such as *fast write* capability, are included in Revision 2.0 of the *AGP Interface Specification*.

The 4X operation of the AGP interface provides for "quad-sampling" of the AGP AD (Address/Data) and SBA (Side-band Addressing) buses. That is, the data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of a 15 ns period (66-MHz clock) or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, the data is sampled twice during a 66-MHz clock cycle. Therefore, the data cycle time is 7.5 ns.

In order to allow for these high-speed data transfers, the 2X mode of AGP operation uses source synchronous data strobing. During 4X operation, the AGP interface uses differential source synchronous data strobing. However, differential source synchronous data strobing is not strictly required by the AGP specification.

With data cycle times as small as 3.75 ns, and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great, or there is noise on the interface, incorrect data will be sampled.

The low-voltage operation on AGP (1.5 V) requires even more noise immunity. For example, during 1.5-V operation, V_{ilmax} is 570 mV. Without proper isolation, crosstalk could create signal integrity issues.

A single AGP controller is supported by the Intel 855PM MCH AGP interface. LOCK# and SERR#/PERR# are not supported. The AGP buffers operate in only one mode:

AGP 4X, 2X and 1X operate at 1.5 V *only*.

AGP semantic cycles to DRAM are not snooped on the host bus.

The MCH supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization.

The AGP interface is clocked from the 66-MHz clock input to the MCH, 66IN. The AGP interface is synchronous to the host and system memory interfaces with a clock ratio of 2:3 (66 MHz: 100 MHz) and to the hub interface with a clock ratio of 1:1 (66 MHz: 66 MHz).

7.2. AGP 2.0 Spec

7.2.1. AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: 1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals. Each group has different routing requirements. In addition, within the 2X/4X timing domain signals, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. The signal groups are documented in the following table.

Table 36. AGP 2.0 Signal Groups

1X timing domain	CLK (3.3 V) RBF# WBF# ST[2:0] PIPE# REQ# GNT# PAR FRAME# IRDY# TRDY# STOP# DEVSEL#
2X / 4X timing domain	Set #1 AD[15:0] C/BE[1:0]# AD_STB0 AD_STB0#[1] Set #2 AD[31:16] C/BE[3:2]# AD_STB1 AD_STB1#[1] Set #3 SBA[7:0] SB_STB SB_STB#[1]

Miscellaneous, Asynchronous	USB+ USB- OVRCNT# PME# TYPDET# PERR# SERR# INTA# INTB#

NOTE: These signals are used in 4X AGP mode ONLY.

Table 37. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

Throughout this section, the term data refers to AD[31:0], C/BE[3:0]#, and SBA[7:0]. The term strobe refers to AD_STB[1:0], AD_STB#[1:0], SB_STB, and SB_STB#. When the term data is used, it refers to one of the three sets of data signals, as in Table 37. When the term strobe is used, it refers to one of the strobes as it relates to the data in its associated group.

The routing guidelines for each group of signals (1X timing domain signals, 2X/4X timing domain signals, and miscellaneous signals) will be addressed separately.

7.3. AGP Routing Guidelines

7.3.1. 1x Timing Domain Routing Guidelines

7.3.1.1. Trace Length Requirements for AGP 1X

This section contains information on the 1X-timing domain routing guidelines. The AGP 1X timing domain signals (refer to Table 36) have a maximum trace length of 10 inches. The target impedance is 55- ± 15%. This maximum applies to ALL of the signals listed as 1X timing domain signals in Table 36. In addition to this maximum trace length requirement (refer to Table 38 and Table 39) these signals must meet the trace spacing and trace length mismatch requirements in Sections 7.3.1.2 and 7.3.1.3.

Table 38. Layout Routing Guidelines for AGP 1X Signals

1X signals	Max. Length (inches)	Width (mils)	Space (mils)
CLK_AGP_SLT	10	4	4
AGP_PIPE#	10	4	4
AGP_RBF#	10	4	4
AGP_WBF#	10	4	4
AGP_ST[2:0]	10	4	4
AGP_FRAME#	10	4	4
AGP_IRDY#	10	4	4
AGP_TRDY#	10	4	4
AGP_STOP#	10	4	4
AGP_DEVSEL#	10	4	4
AGP_REQ#	10	4	4
AGP_GNT#	10	4	4
AGP_PAR	10	4	4

7.3.1.2. Trace Spacing Requirements

AGP 1X timing domain signals (refer to Table 36) can be routed with 4-mil minimum trace separation.

7.3.1.3. Trace Length Mismatch

There are no trace length mismatch requirements for 1X timing domain signals. These signals must meet minimum and maximum trace length requirements.

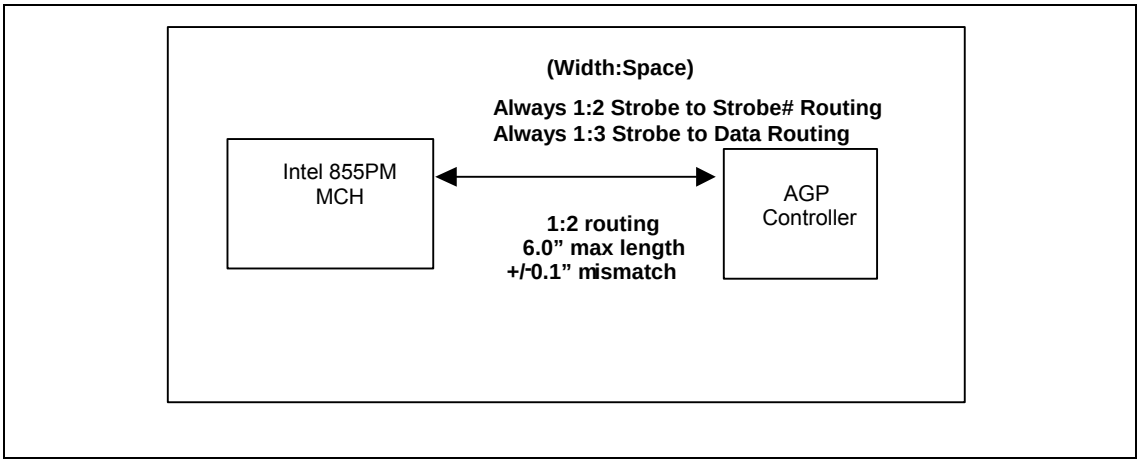
7.3.2. 2X/4X Timing Domain Routing Guidelines

7.3.2.1. Trace Length Requirements for AGP 2X/4X

These trace length guidelines apply to ALL of the signals listed as 2X/4X timing domain signals in Table 36. In addition to these maximum trace length requirements, these signals must meet the trace spacing and trace length mismatch requirements in Sections 7.3.2.2 and 7.3.2.3.

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. These routing rules are divided by trace spacing. In 1:2 spacing, the distance between the traces is two times the width of traces. Simulations in a mobile environment support this rule.

Figure 93. AGP Layout Guidelines



If the AGP interface is less than 6.0 inches, 1:2 trace spacing is required for 2X/4X lines. These 2X/4X signals must be matched to their associated strobe within ± 0.1 inches. This is for designs that require less than 6 inches between the graphics device and the Intel 855PM MCH. See Figure 93 for details.

Reduce line length mismatch to ensure added margin. In order to reduce trace to trace coupling (cross talk), separate the traces as much as possible.

7.3.2.2. Trace Spacing Requirements

AGP 2X/4X timing domain signals (refer to Table 36) must be routed as documented in Table 39. They should be routed using 4-mil traces. Additionally, the signals can be routed with 5-mil spacing when breaking out of the Intel 855PM MCH. The routing must widen to the requirement in Table 40 within 0.3 inches of the MCH package.

Since the strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source synchronous AGP interface, special care should be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g. AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 4-mil traces with 8 mils of space (1:2) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 15 mils (1:3). The strobe pair must be length matched to less than ± 0.1 inches (that is, a strobe and its compliment must be the same length within ± 0.1 inches).

Table 39. Layout Routing Guidelines for AGP 2X/4X Signals

Signal	Maximum Length (inch)	Trace Space (mils) (4 mil traces)	Length Mismatch (inch)	Relative To	Notes
2X/4X Timing Domain Set#1	6	8	± 0.1	AGP_ADSTB0 and AGP_ADSTB0#	AGP_ADSTB0, AGP_ADSTB0# must be the same length (±10 mils)
2X/4X Timing Domain Set#2	6	8	± 0.1	AGP_ADSTB1 and AGP_ADSTB1#	AGP_ADSTB1, AGP_ADSTB1# must be the same length (±10 mils)
2X/4X Timing Domain Set#3	6	8	± 0.1	AGP_SBSTB and AGP_SBSTB #	AGP_SBSTB, AGP_SBSTB# must be the same length (±10 mils)

7.3.2.3. Trace Length Mismatch Requirements

Table 40. AGP 2.0 Data Lengths Relative to Strobe Length

Max Trace Length	Trace Spacing	Strobe Length	Min Trace Length	Max Trace Length
< 6 in	1:2	X	X – 0.1 in	X + 0.1 in

The trace length minimum and maximum (relative to strobe length) should be applied to each set of 2X/4X timing domain signals **independently**. That is, if AD_STB0 and ADSTB0# are 5 inches, then AD[15:0] and C/BE[1:0] must be between 4.9 inches and 5.1 inches. However AD_STB1 and ADSTB1# can be 3.5 inches (and therefore AD[31:16] and C/BE#[3:2] must be between 3.4 inches and 3.6 inches). In addition, all 2X/4X timing domain signals must meet the maximum trace length requirements.

All signals should be routed as strip lines (inner layers).

All signals in a signal group should be routed on the same layer. Routing studies have shown that these guidelines can be met. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to 0 inches as possible to provide optimal timing margin.

Table 41 shows the AGP 2.0 routing summary.

Table 41. AGP 2.0 Routing Guideline Summary

Signal	Maximum Length	Trace Spacing (4 mil traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	10 in	4 mils	No Requirement	N/A	None
2X/4X Timing Domain Set#1	6 in	8 mils	± 0.1 in	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	6 in	8 mils	± 0.1 in	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	6 in	8 mils	± 0.1 in	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length
Miscellaneous	10 in	8 mils	No Requirement	N/A	PCI_PME#, AGP_PERR#, AGP_SERR#

Each strobe pair must be separated from other signals by at least 15 mils.

7.3.3. AGP Clock Skew

The maximum total AGP clock skew, between the Intel 855PM MCH and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter, which originates on the motherboard, add-in module (if used), and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but also at all points on the clock edge that falls in the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew (the motherboard designer shall determine how the 0.9 ns is allocated between the board and the synthesizer).

7.3.4. AGP Signal Noise Decoupling Guidelines

The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the Intel 855PM MCH. The following guidelines are not intended to replace thorough system validation on Intel 855PM chipset-based products.

A minimum of six 0.01-µF capacitors are required and must be as close as possible to the MCH. These should be placed within 70 mils of the outer row of balls on the MCH for VDDQ decoupling. Ideally, this should be as close as possible.

The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.

Intel recommends that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.

In order to add the decoupling capacitors within 70 mils of the MCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1.0 inch max.).

In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. One extra 0.01-±F capacitor per 10 vias is required. The capacitor should be placed as close as possible to the center of the via field.

7.3.5. AGP Routing Ground Reference

Intel strongly recommends that at least the following critical signals be referenced to ground from the MCH to an AGP controller connector using a minimum number of vias on each net: AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_TRDY#, G_IRDY#, G_GNT#, and ST[2:0].

In addition to the minimum signal set listed previously, Intel strongly recommends that half of all AGP signals be referenced to ground, depending on the board layout. In an ideal design, the complete AGP interface signal field would be referenced to ground. This recommendation is not specific to any particular PCB stack-up, but should be applied to all systems incorporating the Intel 855PM chipset.

7.3.6. Pull-ups

The *AGP 2.0 Specification* requires AGP control signals to have pull-up resistors to VDDQ to ensure they contain stable values when no agent is actively driving the bus. Also, the AD_STB[1:0]# and ST_STB# strobes require pull-down resistors to GND. The Intel 855PM MCH has integrated many of these pull-up/pull-down resistors on the AGP interface and a few other signals not required by the AGP 2.0 Specification. Pull-ups are allowed on any signal except AD_STB[1:0]# and ST_STB#.

The MCH has no support for the PERR# and SERR# pins of an AGP graphics controller that supports PERR# and SERR#. Pull-ups to a 1.5-V source are required down on the motherboard in such cases.

Table 42. AGP Pull-Up/Pull-Down Requirements and Straps

Signal	AGP 2.0 Signal Pull-Up/Pull-Down Requirements	Intel 855PM MCH Integrated Pull-Up/Pull-Down	State During RSTIN# Assertion	Notes
DEVSEL#	Pull-Up	4.5 k Pull-Up		
FRAME#	Pull-Up	4.5 k Pull-Up		
GNT#		4.5 k Pull-Up	Pull-Up (Strap)	6
INTA#	Pull-Up			3, 5
INTB#	Pull-Up			3, 5
IRDY#	Pull-Up	4.5 k Pull-Up		
PERR#	Pull-Up			2
PIPE#	Pull-Up	4.5 k Pull-Up		
RBF#	Pull-Up	4.5 k Pull-Up	Pull-Up (Strap)	6
REQ#		4.5 k Pull-Up		1
SERR#	Pull-Up			2
ST[2:0]		4.5 k Pull-Up	Pull-Up (Strap)	4, 6
STOP#	Pull-Up	4.5 k Pull-Up		
TRDY#	Pull-Up	4.5 k Pull-Up		
WBF#		4.5 k Pull-Up	Pull-Up (Strap)	6
AD_STB[1:0]	Pull-Up	4.5 k Pull-Up		
AD_STB[1:0]#	Pull-Down	4.5 k Pull-Down		
SB_STB	Pull-Up	4.5 k Pull-Up		
SB_STB#	Pull-Down	4.5 k Pull-Down		
SBA[7:0]		4.5 k Pull-Up	Pull-Up (Strap)	1, 6

NOTES:

1. The Intel 855PM MCH has integrated pull-ups to ensure that these signal do not float when there is no add-in card in the connector.
2. The Intel 855PM MCH does not implement the PERR# and SERR# signals. Pull-ups on the motherboard are required for AGP graphics controllers that implement these signals.
3. The AGP graphics controller's INTA# and INTB# signals must but routed to the system PCI interrupt request handler where the pull-up requirement should be met. For Intel 855PM chipset-based systems, they can be routed to the ICH4-M's PIRQ signals that are open drain and require pull-ups on the motherboard.
4. ST[1:0] provide the strapping options for 100-MHz FSB operation and DDR memory, respectively.
5. INTA# and INTB# should be pulled to 3.3 V, not VDDQ.
6. Refer to the *Intel® 855PM Memory Controller Hub (MCH) DDR 200/266 MHz Datasheet* for more details on straps.

The pull-up/pull-down resistor value requirements are shown in Table 43.

Table 43. AGP 2.0 Pull-up Resistor Values

Rmin	Rmax
4 k	16 k

The recommended AGP pull-up/pull-down resistor value is 8.2 k .

7.3.7. AGP VDDQ and VREF

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller. VDDQ is the interface voltage. The external graphics controller may **ONLY** power the Intel 855PM MCH AGP I/O buffers with 1.5-V VDDQ power pins.

7.3.8. VREF Generation for AGP 2.0 (2X and 4X)

7.3.8.1. 1.5-V AGP Interface (2X/4X)

In order to account for potential differences between VDDQ and GND at the Intel 855PM MCH and graphics controller, both devices use **source generated Vref**. That is, the Vref signal is generated at the graphics controller and *sent* to the MCH and another Vref is generated at the MCH and *sent* to the graphics controller.

Both the graphics controller and the MCH are required to generate Vref. The voltage divider networks consist of AC and DC elements. The reference voltage that should be supplied to the Vref pins of the MCH and the graphics controller is ½ * VDDQ. Two 1-k ± 1% resistors can be used to divide VDDQ down to the necessary voltage level.

The Vref divider network should be placed as close to the AGP interface as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the Vref signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity.

7.3.9. AGP Compensation

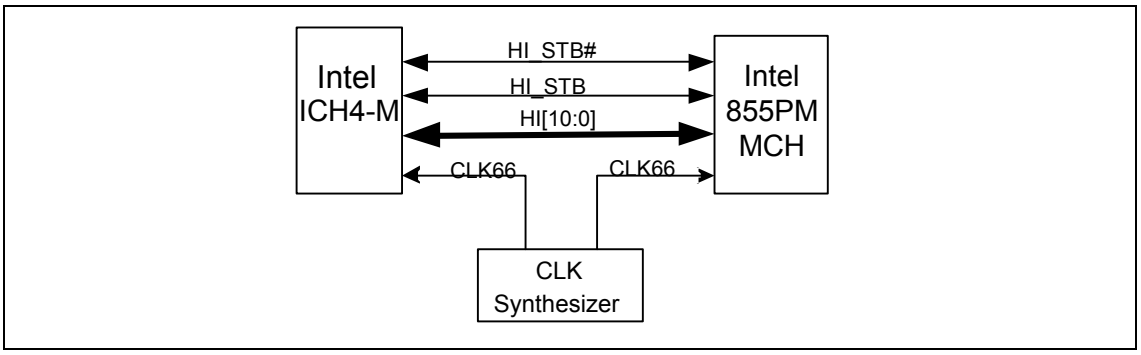
The Intel 855PM MCH AGP interface supports resistive buffer compensation. For Printed Circuit Boards with characteristics impedance of 55 , tie the GRCOMP pin to a 36.5 ± 1% pull-down resistor (to ground) via a 10-mil wide, very short (0.5 inches) trace.

8. Hub Interface

The Intel 855PM MCH and Intel 82801DBM ICH4-M pin-map assignments have been optimized to simplify the hub interface routing between these devices. Intel recommends that the hub interface signals be routed directly from the MCH to the ICH4-M with all signals referenced to VSS. Layer transitions should be kept to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer.

The hub interface signals are broken into two groups: data signals (HI) and strobe signals (HI_STB). For the 11-bit hub interface, HI[10:0] are associated with the data signals while HI_STB and HI_STB# are associated with the strobe signals.

Figure 94. Hub Interface Routing Example



8.1. Hub Interface Compensation

This hub interface connects the 82801DBM ICH4-M and the Intel 855PM MCH. The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires resistive compensation (RCOMP).

The trace impedance must equal 55- ± 15%

Table 44. Hub Interface RCOMP Resistor Values

Component	Trace Impedance	HICOMP Resistor Value	HICOMP Resistor Tied to
ICH4-M	55 ± 15%	36.5 ± 1%	VSS
MCH	55 ± 15%	36.5 ± 1%	Vcc1_8

8.2. Hub Interface Data HI[7:0] and Strobe Signals

The hub interface HI[7:0] data signals should be routed on the same layer as hub interface strobe signals. There are two options for routing and include either an external layer or an internal layer.

8.2.1. Internal Layer Routing

Traces should be routed 4 mils wide with 8 mils trace spacing (4 on 8) and 20 mils spacing from other signals. In order to break out of the Intel 855PM MCH and Intel 82801DBM ICH4-M packages, the HI[7:0] signals can be routed 4 on 4. The signal must be separated to 4 on 8 within 300 mils from the package.

The maximum HI[7:0] signal trace length is 6 inches. The HI[7:0] signals must be matched within ± 100 mils of the HI_STB differential pair. There is no explicit matching requirement between the individual HI[7:0] signals.

The hub interface strobe signals should be routed as a differential pair, 4 mils wide with 8 mils trace spacing (4 on 8). The maximum length for strobe signals is 6 inches. Each strobe signal must be the same length and each HI[7:0] signal must be matched to within ± 100 mils of the strobe signals.

Table 45. Hub Interface Signals Internal Layer Routing Summary

Signal	Max length (inch)	Width (mils)	Space (mils)	Mismatch length (mils)	Relative To	Space with other signals (mils)	Notes
HI_[7:0]	6	4	8	± 100	Differential HI_STB pair	20	
HI_STB and HI_STB#	6	4	8	±100	Data lines	20	HI_STB and HI_STB# must be the same length (± 10 mils)

8.2.2. External Layer Routing

Traces should be routed 5 mils wide with 10 mils trace spacing (5 on 10) and 20 mils spacing from other signals. In order to break out of the Intel 855PM MCH and Intel 82801DBM ICH4-M packages, the HI[7:0] signals can be routed 5 on 5. The signals must be separated to 5 on 10 within 300 mils from the package.

The hub interface strobe signals should be routed as a differential pair, 5 mils wide with 10 mils trace spacing (5 on 10). The maximum length for the strobe signals is 6 inches. Each strobe signal must be the same length, and each HI[7:0] signal must be matched to within ± 100 mils of the strobe signals.

Table 46. Hub Interface Signals External Layer Routing Summary

Signal	Max length (inch)	Width (mils)	Space (mils)	Mismatch length (mils)	Relative To	Space with other signals (mils)	Notes
HI_[7:0]	6	5	10	± 100	Differential HI_STB pair	20	
HI_STB and HI_STB#	6	5	10	± 100	Data lines	20	HI_STB and HI_STB# must be the same length (± 10 mils)

8.3. Hub Interface Data HI[10:8] Signals

The maximum length for the hub interface data signals, HI[10:8] is 8 inches. They should be routed on the same layer with Hl[7:0].

8.3.1. Internal Layer Routing

Traces should be routed 4 mils wide with 8 mils trace spacing (4 on 8) and 20 mils spacing from other non-hub interface related signals. In order to break out of the Intel 855PM MCH and Intel 82801DBM ICH4-M packages, the HI[10:8] signals can be routed 4 on 4. The signal must be separated to 4 on 8 within 300 mils from the package.

8.3.2. External Layer Routing

Traces should be routed 5 mils wide with 10 mils trace spacing (5 on 10) and 20 mils spacing from other non-hub interface signals. In order to break out of the Intel 855PM MCH and Intel 82801DBM ICH4-M packages, the HI[10:8] signals can be routed 5 on 5. The signal must be separated to 4 on 8 within 300 mils from the package.

8.3.3. Terminating HI[11]

The HI[11] signal exists on the Intel 82801DBM ICH4-M but not the Intel 855PM MCH and is not used on the platform. It can be left as a no connect.

8.4. HIREF/HI_VSWING Generation/Distribution

HIREF is the hub interface reference voltage used on both the Intel 855PM MCH and the Intel 82801DBM ICH4-M. Depending on the buffer mode, the HIREF voltage requirement must be set appropriately for proper operation. The ICH4-M uses HI_VSWING to control voltage swing and impedance strength of the hub interface buffers. See the table below for the HIREF and HI_VSWING voltage specifications and the associated resistor recommendations for the voltage divider circuit.

Table 47. Hub Interface HIREF/HI_VSWING Generation Circuit Specifications

HI_VSWING Voltage Specification (V)[1]	HIREF Voltage Specification (V)[1]	Recommended Resistor Values for the HIREF Divider Circuit (Ohm)
1/2 VCC1_8 ± 7%	1/2 VCC1_8 ± 7%	R1 = R2 = (100 – 150) ± 1% C1 = 0.01 µF C2 = 0.1 µF

NOTE: 7% tolerance includes static and transient tolerances. HIREF and HI_VSWING must track VCC1_8 and to this end must be ± 2% relative to the instantaneous value of VCC1_8.

The single HIREF divider should not be located more than 3 inches away from either the MCH or ICH4-M. If the single HIREF divider is located more than 3 inches away, locally generated hub interface reference voltage dividers should be used instead. The reference voltage generated by a single HIREF divider should be bypassed to ground with a 0.1-µF capacitor (C2) and at each component with a 0.01-µF capacitor (C1) located close to the component HIREF pin. If the reference voltage is generated locally, the bypass capacitor (0.01 µF) needs to be close to the component HIREF pin.

Figure 95. Hub Interface with Single Reference Voltage Divider Circuit

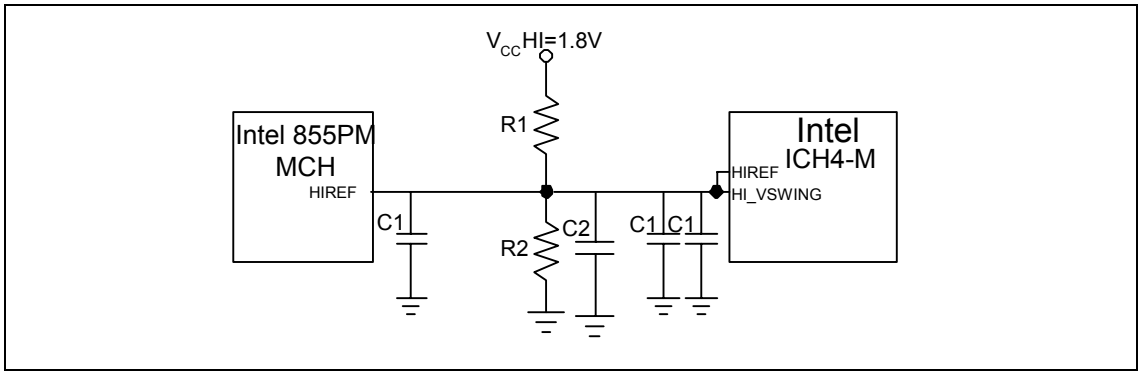
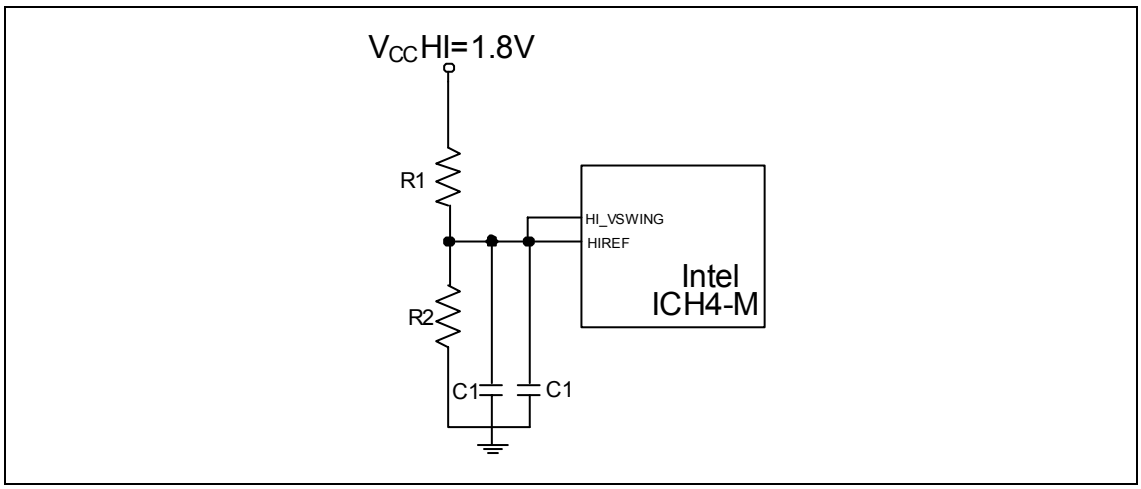


Figure 96. Hub Interface with Locally Generated Reference Voltage Divider Circuit



8.5. Hub Interface Decoupling Guidelines

The main focus of these guidelines is to minimize signal integrity problems on the hub interface of the Intel 855PM MCH. To improve I/O power delivery, use two 0.1-µF capacitors per each component (i.e. the ICH4-M and MCH). These capacitors should be placed within 150 mils from each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1_8 side of the capacitors to the VCC1_8 power balls. Similarly, if layout allows, metal fingers running on the VCC1_8 side of the board should connect the GND side of the capacitors to the VSS power balls.

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9. I/O Subsystem

9.1. IDE Interface

This section contains guidelines for connecting and routing the Intel 82801DBM ICH4-M IDE interface. The ICH4-M has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH4-M has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0- resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5-mil traces on 7-mil spaces, and must be less than 8 inches long (from ICH4-M to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inches.

9.1.1. Cabling

Length of cable: Each IDE cable must be equal to or less than 18 inches.

Capacitance: Less than 35 pF.

Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).

Grounding: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

Intel 82801DBM ICH4-M Placement: The ICH4-M must be placed equal to or less than 8 inches from the ATA connector(s).

9.1.2. Primary IDE Connector Requirements

Figure 97. Connection Requirements for Primary IDE Connector

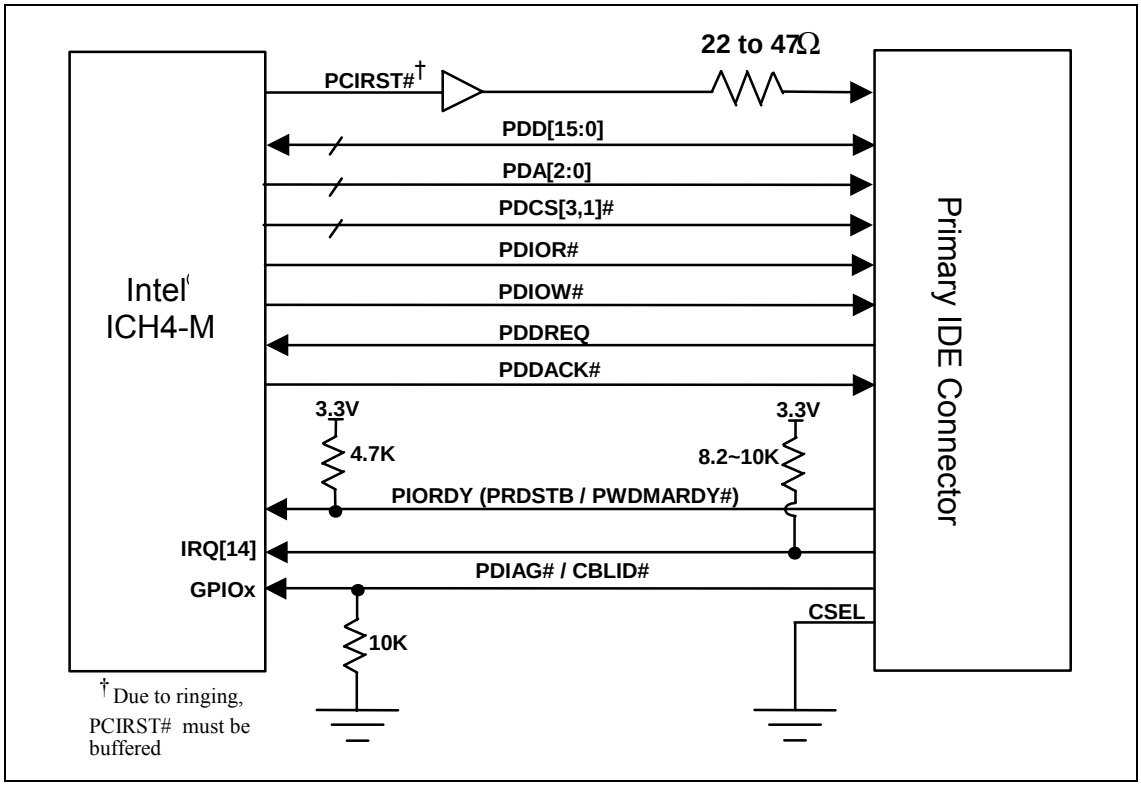


Figure 96 highlights the requirements for routing the ICH4-M IDE interface to the primary IDE connector.

22 - 47 series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.

An 8.2 k - 10 k pull-up resistor is required on IRQ14 to VCC3_3.

A 4.7-k pull-up resistor to VCC3_3 is required on PIORDY and SIORDY.

Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.

The 10-k resistor to ground on the PDIAG#/CBLID# signal is required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

9.1.3. Secondary IDE Connector Requirements

Figure 98. Connection Requirements for Secondary IDE Connector

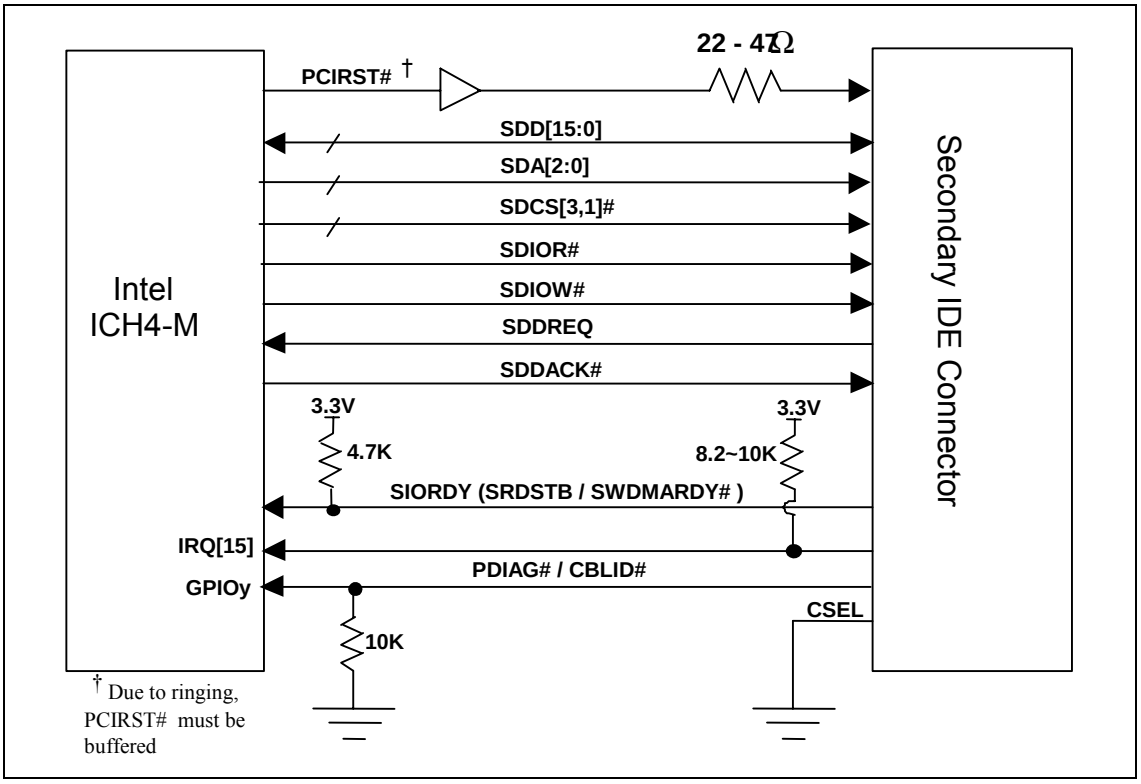


Figure 97 highlights the requirements for routing ICH4-M IDE interface to the secondary IDE connector.

22 - 47 series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.

An 8.2 k - 10 k pull-up resistor is required on IRQ15 to VCC3_3.

A 4.7-k pull-up resistor to VCC3_3 is required on PIORDY and SIORDY.

Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.

The 10-k resistor to ground on the PDIAG#/CBLID# signal is required on the Secondary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

9.1.4. Mobile IDE Swap Bay Support

Systems that require the support for an IDE "hot" swap drive bay can be designed to utilize the Intel 82801DBM ICH4-M's IDE interface disable feature to achieve this functionality. To support a mobile "hot" swap bay, the ICH4-M allows the IDE output signals to be tri-stated or driven low and input buffers to be turned off. This requires certain hardware and software requirements to be met for proper operation.

From a hardware perspective, the equivalent of two spare control signals (e.g. GPIO's) and a FET are needed to properly utilize the IDE tri-state feature. An IDE drive must have a reset signal (i.e. first additional control signal) driving its reset pin and a power supply that is isolated from the rest of the IDE interface. To isolate the power supplied to the IDE drive bay, a second additional control signal is needed to control the enabling/disabling of a FET that supplies a separate plane flood powering the IDE drive and its interface.

Although actual hardware implementations may vary, the isolated reset signal and power plane are strict requirements. Systems that connect the IDE swap bay drive to the same power plane and reset signals of the ICH4-M should not use this IDE tri-state feature. Many IDE drives use the control and address lines as straps that are used to enter test modes. If the IDE drive is powered up along with the ICH4-M while the IDE interface is tri-stated rather than being driven to the default state, then the IDE drive could potentially enter a test mode. To avoid such a situation, the aforementioned hardware requirements or equivalent solution should be implemented.

9.1.4.1. Intel 82801DBM ICH4-M IDE Interface Tri-State Feature

The new IDE interface tri-state capabilities of the Intel 82801DBM ICH4-M also include a number of configuration bits that must be programmed accordingly for proper system performance. The names of the critical registers, their location, and brief description are listed below.

1. B0:D31:F0 Offset D5h (BACK_CNTL – Backed Up Control Register) bits [7:6] need to be set to '1' in order to enable the tri-stating of the primary and secondary IDE pins when the interfaces are put into reset. By default both bits are set to '1.'
2. B0:D31:F0 Offset D0-D3h (GEN_CNTL – General Control Register) bit [3] should be set to '1' in order to lock the state of bits [7:6] at B0:D31:F0 Offset D5h. This prevents any inadvertent reprogramming of the IDE interface pins to a non-tri-state mode during reset by a rogue software program. By default this bit is set to '0' and BIOS should set this bit to '1.' This is a write once bit only and requires a PCIRST# to reset to '0.' Thus, this bit also needs to be set to '1' after resume from S3-S5.
3. B0:D31:F1 Offset 54h (IDE_CONFIG – IDE I/O Configuration Register) bits [19:18] (SEC_SIG_MODE) and bits [17:16] (PRIM_SIG_MODE) control the reset states of the secondary and primary IDE channels, respectively. The values in SEC_SIG_MODE and PRIM_SIG_MODE are tied to the values set by the BACK_CNTRL register bits [7:6], respectively. When bits [7:6] are set to '1,' the PRIM_SIG_MODE and SEC_SIG_MODE will be set to '01' for tri-state when the either IDE channel is put in reset.
4. B0:D31:F1 Offset 40-41h (Primary) and 42-23h (Secondary) bit [5] and bit [1] (IDE_TIM – IDE Timing Register) are the IORDY Sample Point Enable bits for drive 1 and 0 of the primary and secondary IDE channels, respectively. By default, these bits are set to '0' and during normal power up, should be set to '1' by the BIOS to enable IORDY assertion from the IDE device when an access is requested.

9.1.4.2. S5/G3 to S0 Boot Up Procedures for IDE Swap Bay

The procedures listed below summarize the steps that must be followed during power up of an IDE swap bay drive.

1. ICH4-M powers up, IDE interface is tri-stated, disk drive is not powered up. IDE drive is recognized as being on a separate power plane and its reset is different from the ICH4-M.
2. BIOS powers on the IDE drive. e.g. GPIO is used to switch on a FET on the board.
3. Once the IDE drive and interface is powered up, the ICH4-M exits from tri-state mode and begins to actively drive the interface.
4. Once ready, the BIOS can de-assert the reset signal to the IDE drive. e.g. GPIO routed to the IDE drive's reset pin.

9.1.4.3. Power Down Procedures for Mobile Swap Bay

The procedures listed below summarize the steps that must be followed in order to remove an IDE device from the mobile swap bay.

1. User indicates to the system that removal of IDE device from the mobile swap bay should begin. Once the system recognizes that all outstanding IDE accesses have completed, the reset signal to the swap device should be asserted.
2. The IDE channel (primary or secondary) that the device resides on should then be set to drive low mode rather than the default tri-state mode. This requires setting the IDE_CONFIG register (B0:D31:F0 Offset 54h) bits [19:18] or [17:16] to '10' (10b). This will cause all IDE outputs to the IDE drive to drive low rather than the default tri-state (which is useful during boot up to prevent any IDE drives from entering a test mode).
3. The IORDY Sample Point Enable bit of the IDE_TIM register for the appropriate IDE device should then be set to '0' to disable IORDY sampling by the ICH4-M. This ensures that zeros will always be returned if the OS attempts to access the IDE device being swapped.
4. Power to the isolated power plane of the IDE device can then be removed and the system can indicate to the user that the mobile swap bay can be removed and the IDE device replaced.

9.1.4.4. Power Up Procedures After Device "Hot" Swap Completed

The procedures listed below summarize the steps that must be followed after a new IDE device has been added to the mobile swap bay and the swap bay must be powered back up.

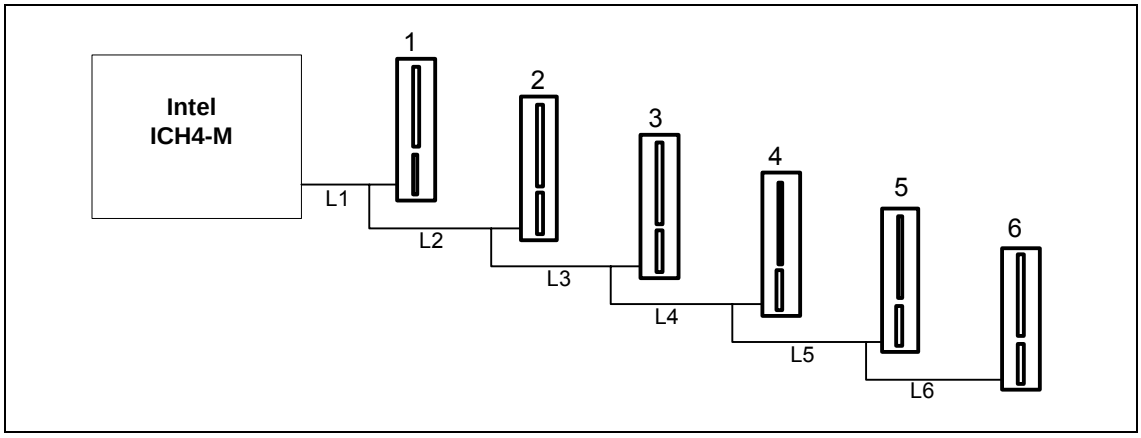
1. Once the IDE swap bay is replaced into the system, the power plane to the device should be enabled once again.
2. The IORDY Sample Point Enable bit of the IDE_TIM register for the appropriate IDE device should then be set to '1' to enable IORDY sampling by the Intel 82801DBM ICH4-M. This allows the OS to access the IDE device once again and waits for the assertion of IORDY in response to an access request.
3. Once the system IDE interface is configured for normal operation once again, the reset signal to the swap device should be de-asserted to allow the drive to initialize.

9.2. PCI

The Intel 82801DBM ICH4-M provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high performance data streaming when the ICH4-M is acting as either the target or the initiator in the PCI bus.

The ICH4-M supports six PCI Bus masters (excluding the ICH4-M), by providing six REQ#/GNT# pairs. In addition, the ICH4-M supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 99. PCI Bus Layout Example



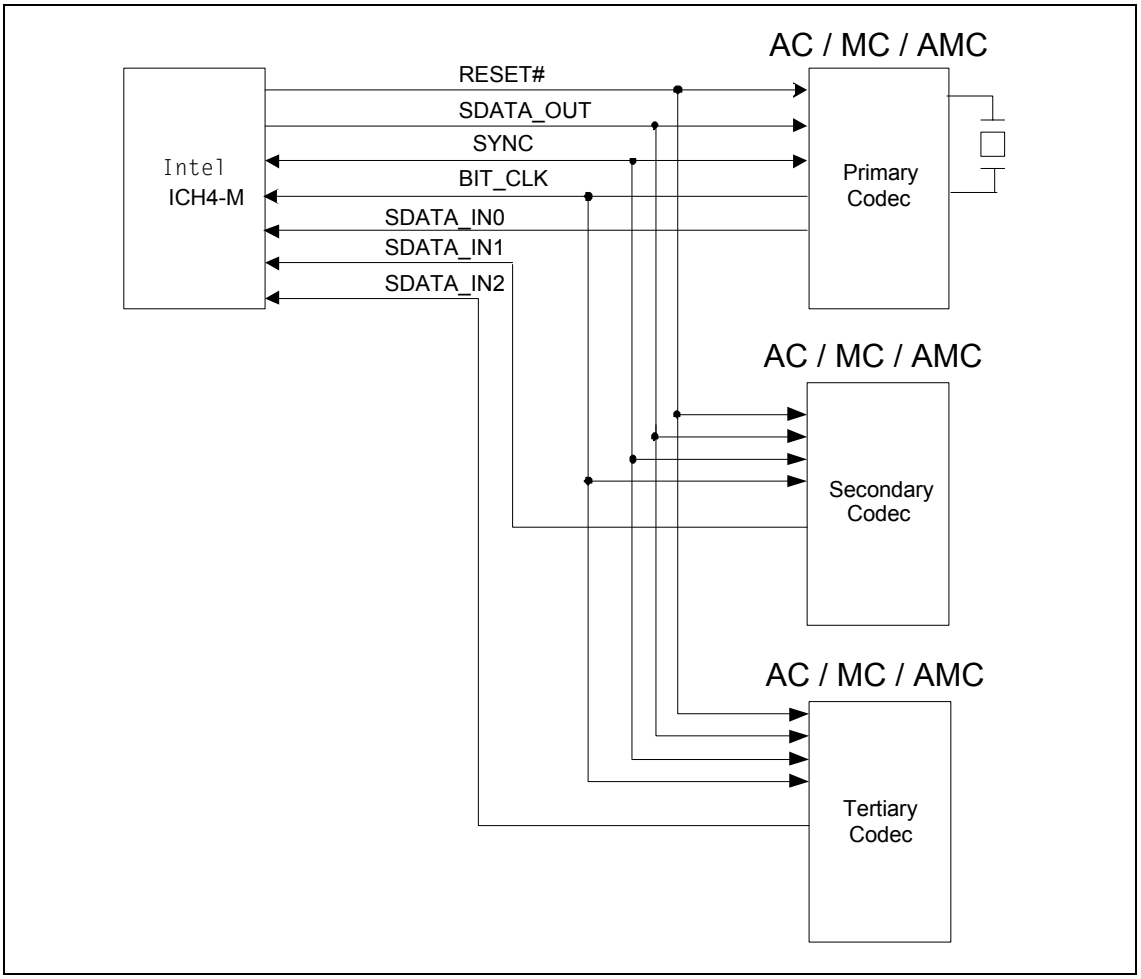
9.3. AC'97

The Intel 82801DBM ICH4-M implements an AC'97 2.1, 2.2, and 2.3 compliant digital controller. Please contact your codec IHV (Independent Hardware Vendor) for information on 2.2 compliant products. The AC'97 2.2 specification is on the Intel website:

http://developer.intel.com/ial/scalableplatforms/audio/index.htm - 97spec/

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH4-M AC-link allows a maximum of three codecs to be connected. Figure 100 shows a three-codec topology of the AC-link for the ICH4-M.

Figure 100. Intel 82801DBM ICH4-M AC'97 – Codec Connection



Note: If a modem codec is configured as the primary AC-link Codec, there should not be any Audio Codecs residing on the AC-link. The primary codec may be connected to AC_SDIN0 as documented in the *Intel® 82801DBM I/O Controller Hub 4 Mobile Datasheet*.

Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576-MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH4-M) and to any other codec present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK directly off the CK-408 clock chip's 14.31818 MHz output is not supported.**

The ICH4-M supports wake-on-ring from S1M-S5 via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4-M has weak pull-down/pull-ups that are always enabled. This will keep the link from floating when the AC-link is off or there are no codecs present.

If the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT will be driven by the codec and the ICH4-M respectively. However, AC_SDIN0,

AC_SDIN1, and AC_SDIN2 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

Figure 101. Intel 82801DBM ICH4-M AC'97 – AC_BIT_CLK Topology

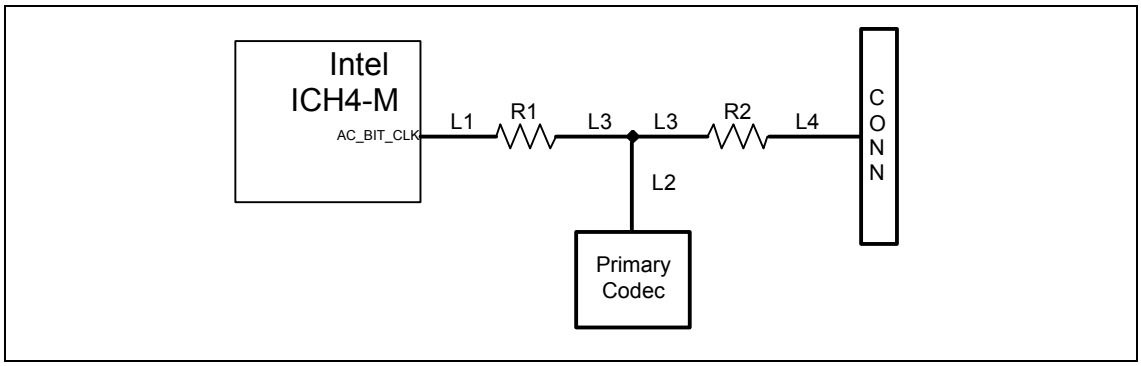


Table 48. AC'97 AC_BIT_CLK Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_BIT_CLK Signal Length Matching
5 on 5	L1 = (1 to 8) – L3 L2 = 0.1 to 6 L3 = 0.1 to 0.4 L4 = (1 to 6) – L3	R1 = 33 - 47 R2 = Option 0 resistor for debugging purposes	N/A

NOTES:
1. Simulations were performed using Analog Device's* Codec (AD1885) and the Cirrus Logic's* Codec (CS4205b). Results showed that if the AD1885 codec was used a 33- resistor was best for R1 and if the CS4205b codec was used a 47- resistor for R1 was best.
2. Bench data shows that a 47- resistor for R1 is best for the Sigmatel* 9750 codec.

Figure 102. Intel 82801DBM ICH4-M AC'97 – AC_SDOUT/AC_SYNC Topology

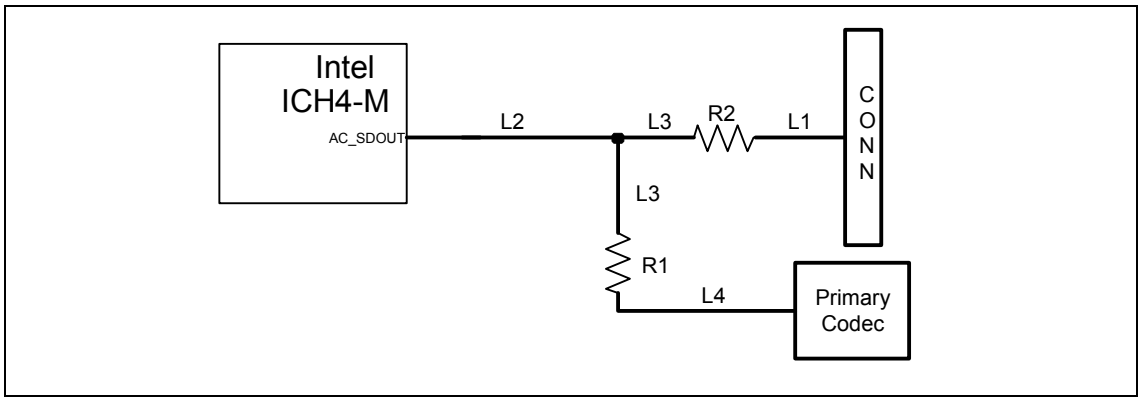


Table 49. AC'97 AC_SDOUT/AC_SYNC Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_SDOUT/AC_SYNC Signal Length Matching
5 on 5	L1 = (1 to 6) – L3 L2 = 1 to 8 L3 = 0.1 to 0.4 L4 = (0.1 to 6) – L3	R1 = 33 - 47 R2 = R1 if the connector card that will be used with the platform does not have a series termination on the card. Otherwise R2 = 0	N/A

NOTES:
1. Simulations were performed using Analog Device's* Codec (AD1885) and the Cirrus Logic's* Codec (CS4205b). Results showed that if the AD1885 codec was used a 33- resistor was best for R1 and if the CS4205b codec was used a 47- resistor for R1 was best.
2. Bench data shows that a 47- resistor for R1 is best for the Sigmatel* 9750 codec.

Figure 103. Intel 82801DBM ICH4-M AC'97 – AC_SDIN Topology

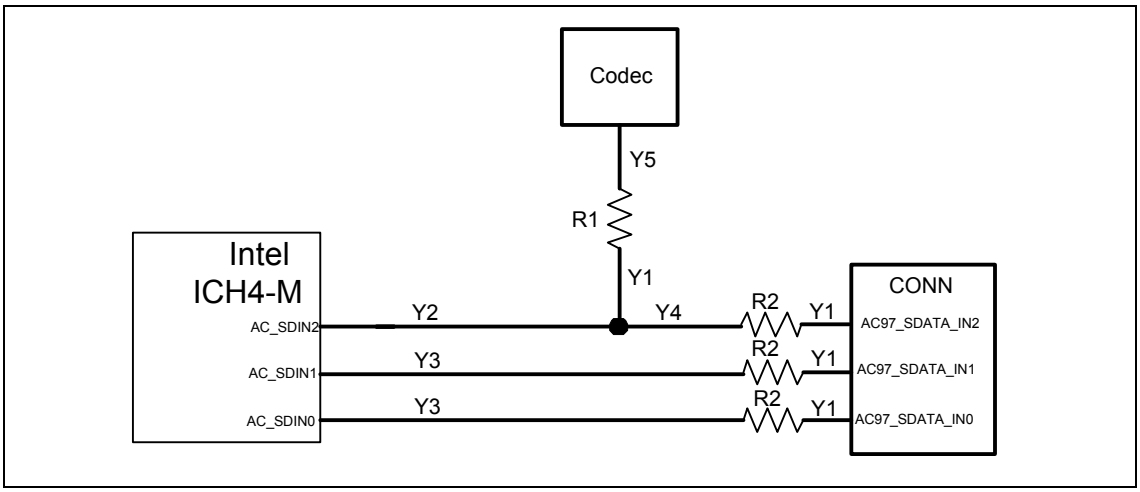


Table 50. AC'97 AC_SDIN Routing Summary

AC'97 Routing Requirements	Maximum Trace Length (inches)	Series Termination Resistance	AC_SDIN Signal Length Matching
5 on 5	Y1 = 0.1 to 0.4 Y2 = (1 to 8) – Y1 Y3 = (1 to 14) – Y1 Y4 = (1 to 6) – Y1 Y5 = (0.1 to 6) – Y1	R1 = 33 - 47 R2 = R1 if the connector card that will be used with the platform does not have a series termination on the card. Otherwise R2 = 0	N/A

NOTES:
1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33- resistor was best for R1 and if the CS4205b codec was used a 47- resistor for R1 was best.
2. Bench data shows that a 47- resistor for R1 is best for the Sigmatel 9750 codec.

9.3.1. AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground plane, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

Special consideration must be given for the ground return paths for the analog signals.

Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.

Partition the board with all analog components grouped together in one area and all digital components in another.

Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.

Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.

Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.

Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.

Analog power and signal traces should be routed over the analog ground plane.

Digital power and signal traces should be routed over the digital ground plane.

Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.

All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.

Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.

Locate the crystal or oscillator close to the codec.

9.3.2. Motherboard Implementation

The following design considerations are provided for the implementation of an Intel 82801DBM ICH4-M platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH4-M platform.

Active components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.

The ICH4-M supports wake-on-ring from S1M-S5 states via the AC'97 link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.

PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

9.3.2.1. Valid Codec Configurations

Table 51. Supported Codec Configurations

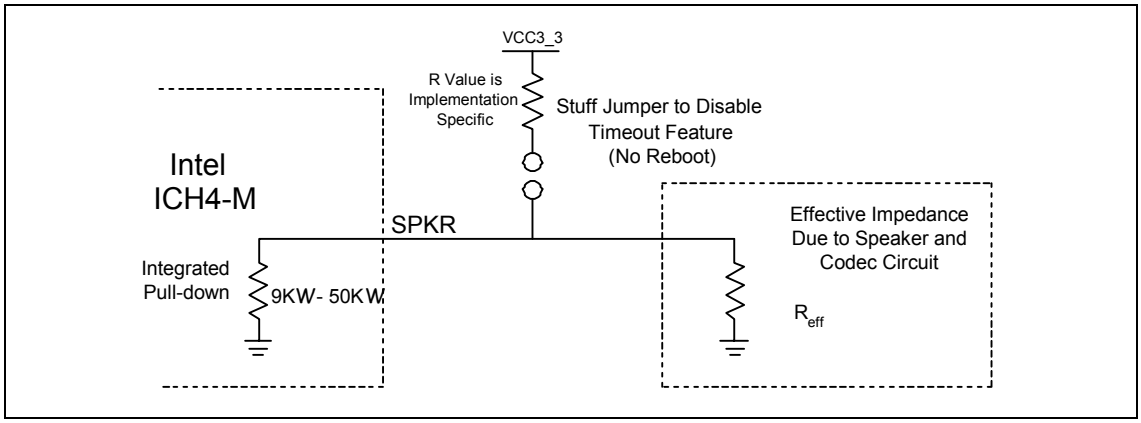
Option	Primary Codec	Secondary Codec	Tertiary Codec	Notes
1	Audio	Audio	Audio	1
2	Audio	Audio	Modem	1
3	Audio	Audio	Audio/Modem	1
4	Audio	Modem	Audio	1
5	Audio	Audio/Modem	Audio	1
6	Audio/Modem	Audio	Audio	1

NOTES:
1. For power management reasons, codec power management registers are in audio space. As a result, if there is an audio codec in the system it must be Primary.
2. There cannot be two modems in a system since there is only one set of modem DMA channels.
3. The ICH4-M supports a codec on any of the AC_SDIN lines, however the modem codec ID must be either 00 or 01.

9.3.3. SPKR Pin Configuration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4-M sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see Figure 104). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{eff}), and the ICH4-M's integrated pull-down resistor will be read as logic high (0.5 * VCC3_3 to VCC3_3 + 0.5 V).

Figure 104. Example Speaker Circuit



9.4. USB 2.0 Guidelines and Recommendations

9.4.1. Layout Guidelines

9.4.1.1. General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems. The USB 2.0 validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second plane is power, the third plane is ground and the fourth is a signal layer. This results in the placement of most of the routing on the fourth plane (closest to the ground plane), allowing a higher component density on the first plane.

1. Place the ICH4-M and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e. I/O connectors, control and signal headers, or power connectors).
2. USB 2.0 signals should be ***ground referenced*** (on recommended stack-up this would be the bottom signal layer).
3. Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities. (As shown in Figure 124.)
5. Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
6. Stubs on high-speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs for a particular signal line should not exceed 200 mils.
7. Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0

traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 9.4.2.

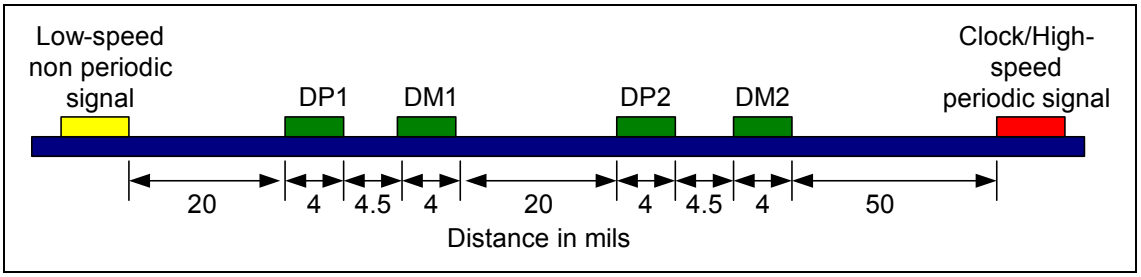
8. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
9. Keep USB 2.0 USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
10. Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

9.4.1.2. USB 2.0 Trace Separation

Use the following separation guidelines.

1. Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90- differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. 4-mil traces with 4.5-mil spacing results in approximately 90- differential trace impedance.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to high-speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
4. Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

Figure 105. Recommended USB Trace Spacing



9.4.1.3. USBRBIAS Connection

The USBRBIAS pin and the USBRBIAS# pin can be shorted and routed 5 on 5 to one end of a 22.6 ±1% resistor to ground. Place the resistor within 500 mils of the Intel 82801DBM ICH4-M and avoid routing next to clock pins.

Figure 106. USBRBIAS Connection

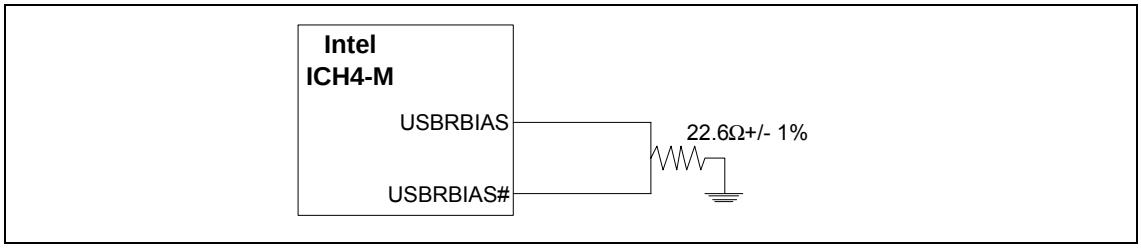


Table 52. USBRBIAS/USBRBIAS# Routing Summary

USBRBIAS/ USBRBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
5 on 5	500 mils	N/A	N/A

9.4.1.4. USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See Section 9.4.4 for details.

9.4.1.5. USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should be no greater that 150 mils.

9.4.1.6. USB 2.0 Trace Length Guidelines

Table 53. USB 2.0 Trace Length Guidelines (With Common-mode Choke)

Configuration	Signal Referencing	Signal Matching	Motherboard Trace Length	Card Trace Length	Maximum Total Length
Back Panel	Ground	The max mismatch between data pairs should not be greater than 150 mils	17 inches	N/A	17 inches

NOTES:
1. These lengths are based upon simulation results and may be updated in the future.
2. All lengths are based upon using a common-mode choke (see Section 9.4.4.1 for details on common-mode choke).

9.4.2. Plane Splits, Voids, and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cutouts.

9.4.2.1. VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the V_{CC} plane.

1. Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the Full-speed Single Ended Zero is common mode).
2. Avoid routing of USB 2.0 signals 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 F or lower in value) that bridge voltage plane splits close to where high-speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates $V_{CC}5$ and $V_{CC}3\_3$ planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to $V_{CC}5$ and the other side should tie to $V_{CC}3\_3$. Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

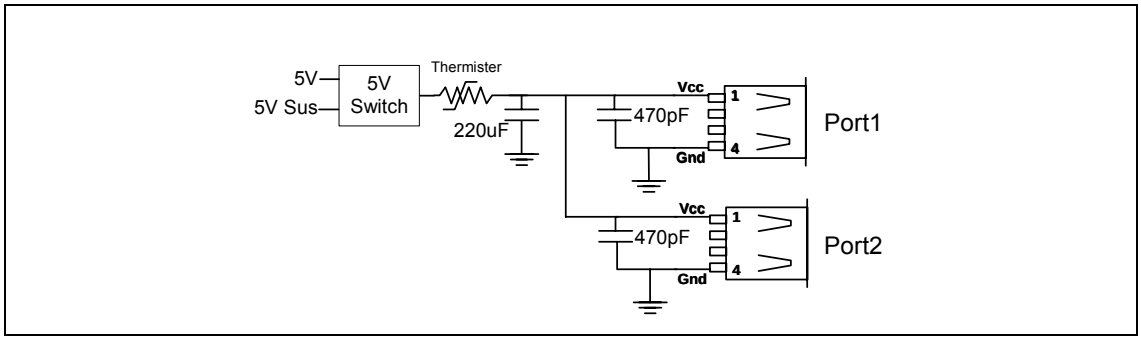
9.4.2.2. GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

9.4.3. USB Power Line Layout Topology

The following is a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach fly-back protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach fly-back voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port and the power carrying traces should be as wide as possible, preferably, a plane. A good "rule-of-thumb" is to make the power carrying traces wide enough that the system fuse will blow on an over current event. If the system fuse is rated at 1amps then the power carrying traces should be wide enough to carry at least 1.5 amps.

Figure 107. Good Downstream Power Connection



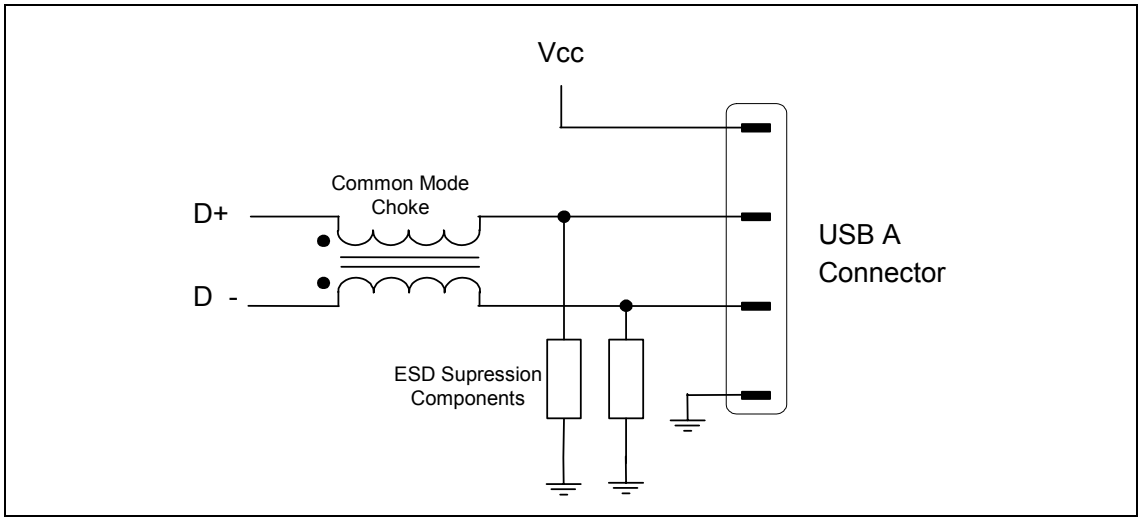
9.4.4. EMI Considerations

The following guidelines apply to the selection and placement of common-mode chokes and ESD protection devices.

9.4.4.1. Common Mode Chokes

Testing has shown that common-mode chokes can provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option **in the event** the choke is needed to pass EMI testing. Figure 108 shows the schematic of a typical common-mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins.

Figure 108. Common Mode Choke Schematic



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality. Common mode chokes with a target impedance of 80 to 90 at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
2. Once you have a part that gives passing EMI results the second step is to test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed and high-speed USB operation.

9.4.5. ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 108. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, Intel recommends including footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

9.5. I/O APIC (I/O Advanced Programmable Interrupt Controller)

The Intel 82801DBM ICH4-M is designed to be backwards compatible with a number of the legacy interrupt handling mechanisms as well as to be compliant with the latest I/O (x) APIC architecture. In addition to implementing two 8259 interrupt controllers (PIC), the ICH4-M also incorporates an Advanced Programmable Interrupt Controller (APIC) that is implemented via the 3-wire serial APIC bus that connects all I/O and local APICs. An advancement in the interrupt delivery and control architecture of the ICH4-M is represented by support for the I/O (x) APIC specification where PCI devices deliver interrupts as write cycles that are written directly to a register that represents the desired interrupt. These are ultimately delivered via the serial APIC bus or FSB. Furthermore, on Intel Pentium M/Intel Celeron M processor-based systems, the ICH4-M has the option to let the integrated I/O APIC behave as an I/O (x) APIC. This allows the ICH4-M to deliver interrupts in a parallel manner rather than just a serial one. This is accomplished by I/O APIC writes to a region of memory that is snooped by the processor and thereby knows what interrupt goes active.

On Intel Pentium M/Intel Celeron M processor-based platforms, the serial I/O APIC bus interface of the ICH4-M should be disabled. I/O (x) APIC is supported on the platform and the servicing of interrupts is accomplished via a FSB interrupt delivery mechanism.

The serial I/O APIC bus interface of the ICH4-M should be disabled as follows.

Tie APICCLK directly to ground.

Tie APICD0, APICD1 to ground through a 10-k resistor. (Separate pull-downs are required if using XOR chain testing)

The Intel® Pentium® M Processor / Intel® Celeron® M Processor does not have pins dedicated for a serial I/O APIC bus interface and thus, no hardware change is necessary. However, it is strongly encouraged to enable I/O APIC support in the BIOS and operating system on the processor based systems rather than the legacy 8259 interrupt controller due to the performance benefits and efficiencies that the I/O (x) APIC architecture enjoys over the older PIC architecture.

9.6. SMBus 2.0/SMLink Interface

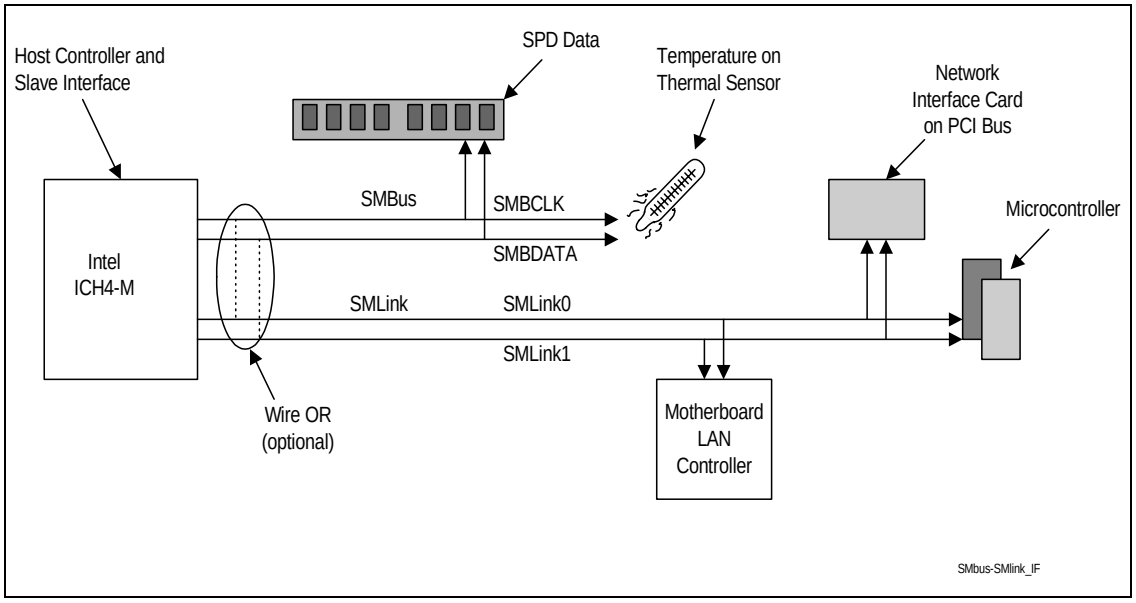
The SMBus interface on the Intel 82801DBM ICH4-M uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH4-M.

The ICH4-M incorporates an SMLink interface supporting Alert-on-LAN*, Alert-on-LAN2*, and a slave functionality. It uses two signals SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert-on-LAN* functionality, the ICH4-M transmits heartbeat and event messages over the interface. When using the Intel® 82562EM Platform LAN Connect Component, the ICH4-M's integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert-on-LAN2*-enabled LAN Controller (i.e. Intel 82562EM 10/100 Mbps Platform LAN Connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4-M SMBus Slave Interface. The slave interface function allows an external micro-controller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'ed together to allow an external management ASIC (such as Intel 82562EM 10/100 Mbps Platform LAN Connect) to access targets on the SMBus as well as the ICH4-M Slave Interface. Additionally, the ICH4-M supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, in order to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals **must** be tied together externally. This is done by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA.

Figure 109. SMBUS 2.0/SMLink Protocol



Note: Intel does not support external access of the ICH4-M's Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH4-M's SMBus Slave Interface by the ICH4-M's SMBus Host Controller. Refer to the *Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet* functionality descriptions of the SMLink and SMBus interface.

9.6.1. SMBus Architecture and Design Considerations

9.6.1.1. SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

1. Device class (High/Low power). Most designs use primarily high power devices.
2. Are there devices that must run in S3?
3. Amount of $V_{CC\_SUSPEND}$ current available, i.e. minimizing load of $V_{CC\_SUSPEND}$.

9.6.1.2. General Design Issues/Notes

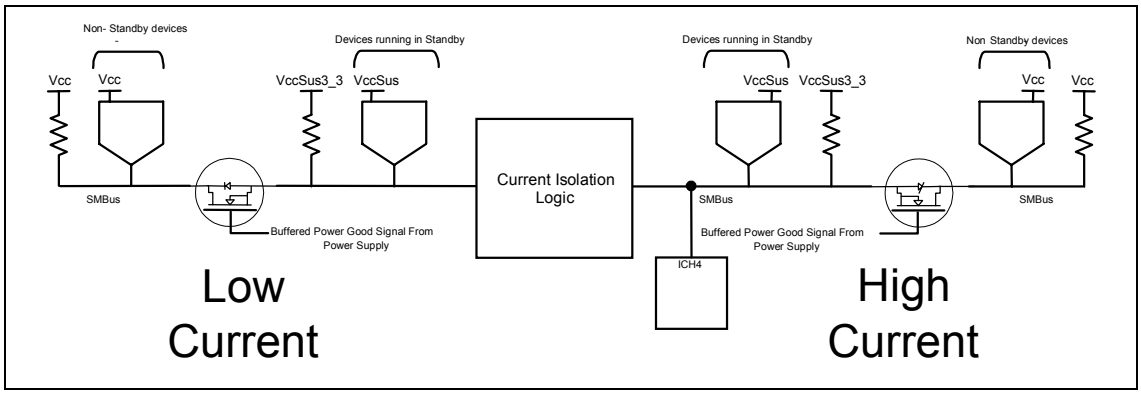
Regardless of the architecture used, there are some general considerations.

1. The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and fall time specification.
2. The maximum bus capacitance that a physical segment can reach is 400 pF.
3. The Intel ICH4-M does not run SMBus cycles while in S3.
4. SMBus devices that can operate in S3 must be powered by the $V_{CC\_SUSPEND}$ supply.

9.6.1.3. High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices while also allowing SMBus devices to communicate during the S3 state. $V_{CC\_SUSPEND}$ leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of a "FET" to isolate the devices powered by the core and suspend supplies. See Figure 110.

Figure 110. High Power/Low Power Mixed $V_{CC\_SUSPEND}$/V_{CC_CORE} Architecture



Added Considerations for mixed architecture:

1. The bus switch must be powered by $V_{CC\_SUSPEND}$.
2. Devices that are powered by the $V_{CC\_SUSPEND}$ well must not drive into other devices that are powered off. This is accomplished with the "bus switch."
3. The bus bridge can be a device like the Phillips PCA9515.

9.6.1.4. Calculating the Physical Segment Pull-Up Resistor

The following tables are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. If any physical bus segment exceeds 400 pF, then a bus bridge device like the Phillips* PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 54. Bus Capacitance Reference Chart

Device	# of Devices/ Trace Length	Capacitance Includes	Cap (pF)
ICH4-M	1	Pin Capacitance	12
CK408	1	Pin Capacitance	10
SO-DIMMS	2	Pin Capacitance (10 pF) + 1 inch worth of trace capacitance (2 pF/inch) per SO-DIMM and 2 pF connector capacitance per SO-DIMM	28
	3		42
PCI Slots	2	Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector	86
	3		129
	4		172
	5		215
	6		258
Bus Trace Length in inches	≥24	2 pF per inch of trace length	48
	≥36		72
	≥48		96

Table 55. Bus Capacitance/Pull-Up Resistor Relationship

Physical Bus Segment Capacitance	Pull-Up Range (For Vcc = 3.3 V
0 to 100 pF	8.2 k to 1.2 k
100 to 200 pF	4.7 k to 1.2 k
200 to 300 pF	3.3 k to 1.2 k
300 to 400 pF	2.2 k to 1.2 k

9.7. FWH

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the *Intel® 82802AB/82802AC Firmware Hub (FWH) Datasheet* or equivalent.

9.7.1. FWH Decoupling

A 0.1-µF capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7-µF capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the V_{CC} supply pins.

9.7.2. In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The Intel 82801DBM ICH4-M hub interface to PCI Bridge will put all CPU boot cycles out on PCI (before sending them out on the FWH interface). If the ICH4-M is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. In order to boot from a PCI card, it is necessary to keep the ICH4-M in subtractive decode mode. If a PCI boot card is inserted and the ICH4-M is programmed for positive decode, there will be two devices positively decoding the same cycle.

9.7.3. FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the Intel 82801DBM ICH4-M INIT# signal needs to be at a value slightly higher than the V_{IH} min FWH INIT# pin specification. The inactive state of this signal is typically governed by the formula V_CPU_IO(min) – noise margin. Therefore, if the V_CPU_IO(min) of the processor is 1.60 V, the noise margin is 200 mV and the V_{IH} min spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because 1.6 V – 0.2 V = 1.40 V which is greater than the 1.35 V minimum of the FWH. If the V_{IH} min of the FWH was 1.45 V, then there would be an incompatibility and logic translation would need to be used. The examples above do not take into account any noise that may be encountered on the INIT# signal. Care must be taken to ensure that the V_{IH} min specification is met with ample noise margin. In applications where it is necessary to use translation logic, refer to Section 4.1.4.1.7.

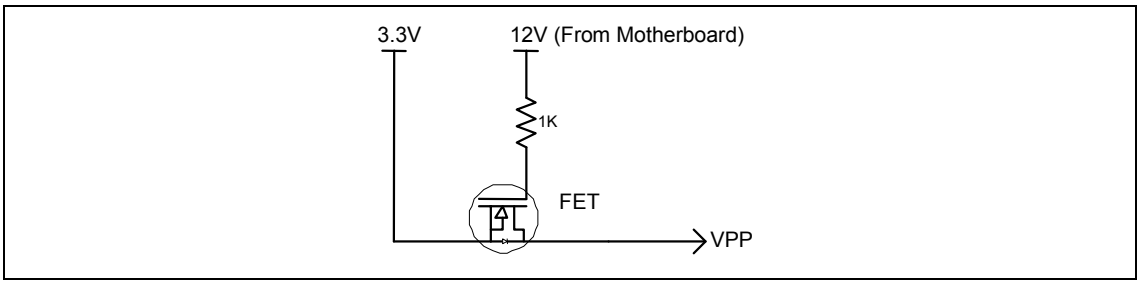
The solution assumes that level translation is necessary. Figure 23 in Section 4.1.4.1.7 implements a solution for the ICH4-M FWH signal INIT#. Trace lengths and resistor values can be found in Table 14. The Voltage Translator circuitry is shown in Figure 24. It is strongly recommended that any system that implements a FWH should have its INIT# input connected to the ICH4-M.

9.7.4. FWH V_{PP} Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports V_{PP} of 3.3 V or 12 V. If V_{PP} is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12-V V_{PP} for 80 hours (3.3 V on Vpp does not affect the life of the device). The 12-V V_{PP} would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3-V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 111. FWH VPP Isolation Circuitry



9.7.5. FWH INIT# Assertion/Deassertion Timings

Due to the large routing solution space and necessity of a voltage translator in the design of a FWH on Intel® Pentium® M Processor / Intel® Celeron® M Processor and Intel 82801DBM ICH4-M based platforms, the following timing requirements must be met to ensure proper system operation.

For INIT# assertion timings, a conservative analysis of the worst case signal propagation times shows that no timing concerns exist because the ICH4-M asserts INIT# for 16 PCI clocks (485 ns) before deasserting. This provides adequate time for INIT# to propagate to both the processor and FWH.

For the INIT# deassertion event, the critical timing is the minimum period of time before the processor is ready to begin fetching code from the FWH after the INIT# based reset begins. This minimum period is conservatively set at 1 CPU clock (10 ns). This also represents the maximum allowed propagation time for the INIT# signal from the ICH4-M to the FWH.

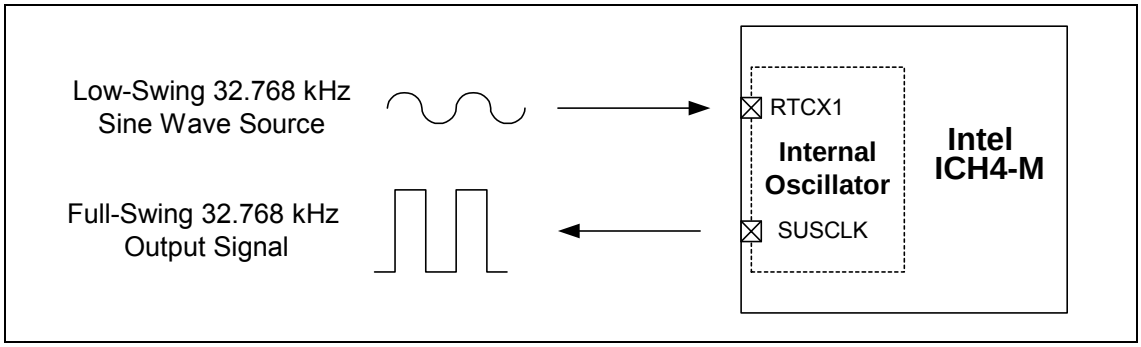
Systems that use alternative devices (i.e. not a FWH) to store the firmware may or may not require the use of INIT#. If INIT# is not used, an analysis should be done to ensure there is no negative impact to system operation. If INIT# is implemented on such a device, voltage translation may be necessary, and the assertion/deassertion timings noted above still apply.

9.8. RTC

The Intel 82801DBM ICH4-M contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH4-M uses a crystal circuit to generate a low-swing, 32 -kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4-M, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the ICH4-M is called SUSCLK. This is illustrated in Figure 112.

Figure 112. RTCX1 and SUSCLK Relationship in Intel 82801DBM ICH4-M

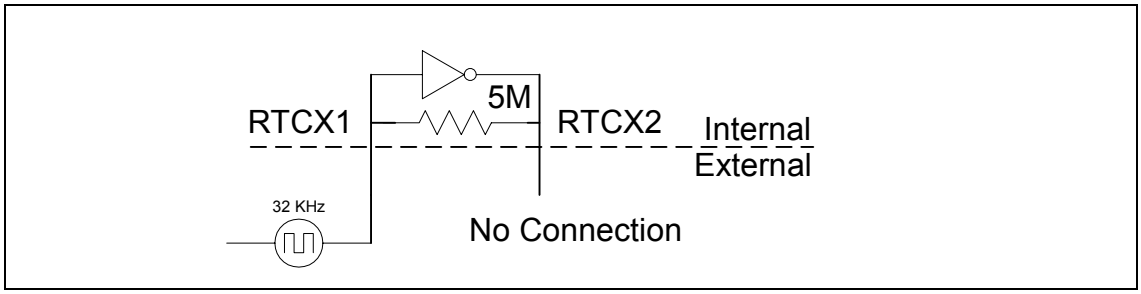


For further information on the RTC, please consult Application Note AP-728 *ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*. This application note is valid for the ICH4-M.

Even if the ICH4-M internal RTC is not used, it is still necessary to supply a clock input to RTCX1 of the ICH4-M because other signals are gated off that clock in suspend modes. However, in this case, the frequency accuracy (32.768 kHz) of the clock inputs is not critical; a cheap crystal can be used or a single clock input can be driven into RTCX1with RTCX2 left as no connect. Figure 113 illustrates the connection.

Note: This is not a validated feature on the ICH4-M. The peak-to-peak swing on RTCX1 cannot exceed 1.0 V.

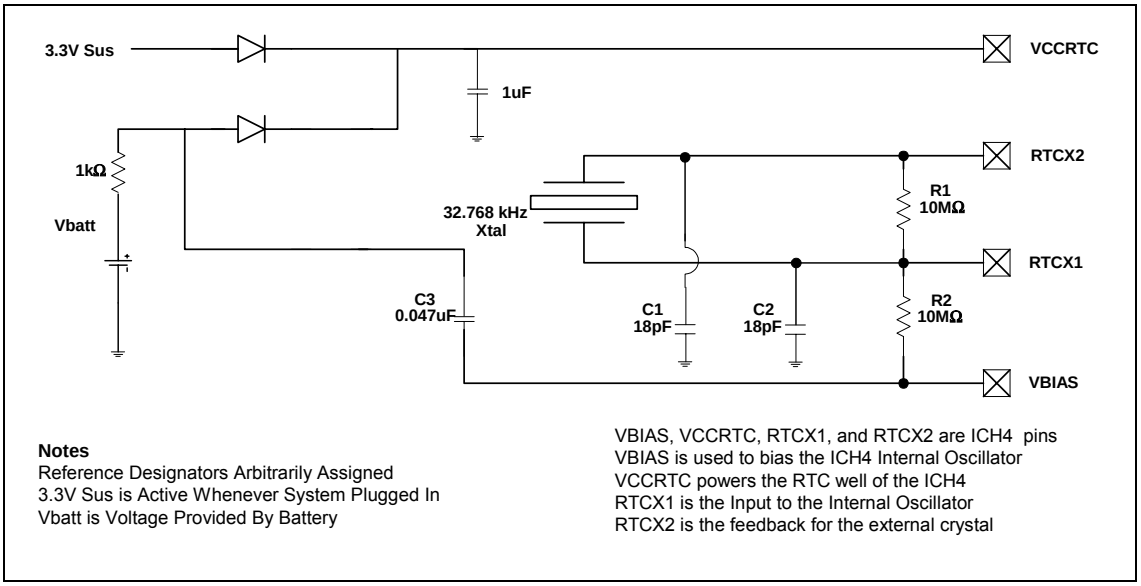
Figure 113. External Circuitry for Intel 82801DBM ICH4-M Where the Internal RTC is Not Used



9.8.1. RTC Crystal

The Intel 82801DBM ICH4-M RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 114 documents the external circuitry that comprises the oscillator of the ICH4-M RTC.

Figure 114. External Circuitry for the Intel 82801DBM ICH4-M RTC



NOTES:

1. The exact capacitor value needs to be based on what the crystal maker recommends. (Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.)
2. V_{CCRTC}: Power for RTC Well
3. RTCX2: Crystal Input 2 – Connected to the 32.7 68 kHz crystal
4. RTCX1: Crystal Input 1 – Connected to the 32.7 68 kHz crystal
5. V_{BIAS}: RTC BIAS Voltage – This ball is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.
6. V_{SS}: Ground

Table 56. RTC Routing Summary

RTC Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, R2, C1, and C2 tolerances	Signal Referencing
5 mil trace width (results in ~2 pF per inch)	1 inch	NA	R1 = R2 = 10 M ± 5% C1 = C2 = (NPO class) See Section 9.8.2 for calculating a specific capacitance value for C1 and C2	Ground

9.8.2. External Capacitors

To maintain the RTC accuracy, the external capacitor C_3 needs to be 0.047 µF and capacitor values C_1 and C_2 should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})]/[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

C_{load} = Crystal's load capacitance. This value can be obtained from Crystal's specification.

C_{in1}, C_{in2} = input capacitances at RTCX1, RTCX2 balls of the ICH4-M. These values can be obtained in the *Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet*.

C_{trace1}, C_{trace2} = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to :

$$C_{trace} = \text{trace length} * 2 \text{ pF/inch}$$

$C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of 2 electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C_1, C_2 can be chosen such that $C_1 = C_2$. Using the equation of C_{load} above, the value of C_1, C_2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C_2 can be chosen such that $C_2 > C_1$. Then C_1 can be trimmed to obtain the 32.768 kHz.

In certain conditions, both C_1, C_2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C_1, C_2 values are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example will illustrates the use of the practical values C_1, C_2 in the case that theoretical values cannot guarantee the accuracy of the RTC in low temperature condition:

Example 1:

According to a required 12-pF load capacitance of a typical crystal that is used with the ICH4-M, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25°C) to yield a 32.768 kHz oscillation.

At 0°C the frequency stability of crystal gives – 23 ppm (assumed that the circuit has 0 ppm at 25°C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C_1, C_2 are chosen to be 6.8 pF instead of 10 pF, the RTC will oscillate at a higher frequency at room temperature (+23 ppm) but this configuration of C_1 / C_2 makes the circuit oscillate closer to 32.768 kHz at 0°C. The 6.8-pF value of C1 and 2 is the **practical value**.

Note that the temperature dependency of crystal frequency is a parabolic relationship (ppm / degree square). The effect of changing the crystal's frequency when operating at 0°C (25°C below room temperature) is the same when operating at 50°C (25°C above room temperature).

9.8.3. RTC Layout Considerations

Since the RTC circuit is very sensitive and requires high accuracy oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

1. Reduce trace capacitance by minimizing the RTC trace length. The Intel 82801DBM ICH4-M requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.
2. Trace signal coupling must be limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1, RTCX2, and VBIAS.
3. Ground guard plane is highly recommended.
4. The oscillator V_{CC} should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

9.8.4. RTC External Battery Connections

The RTC requires an external battery connection to maintain its functionality and its RAM while the Intel 82801DBM ICH4-M is not powered by the system.

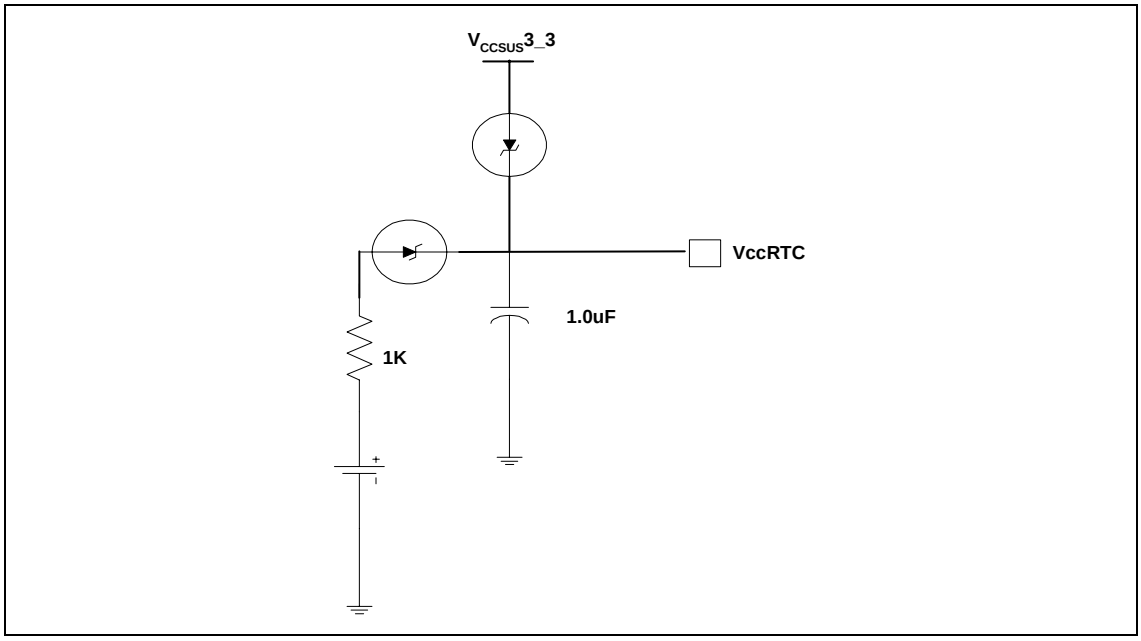
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 5 µA, the battery life will be at least:

170,000 µAh / 5 µA = 34,000 h = 3.9 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH4-M via a Schottky diode circuit for isolation. The Schottky diode circuit allows the ICH4-M RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 115 is an example of a diode circuit that is used.

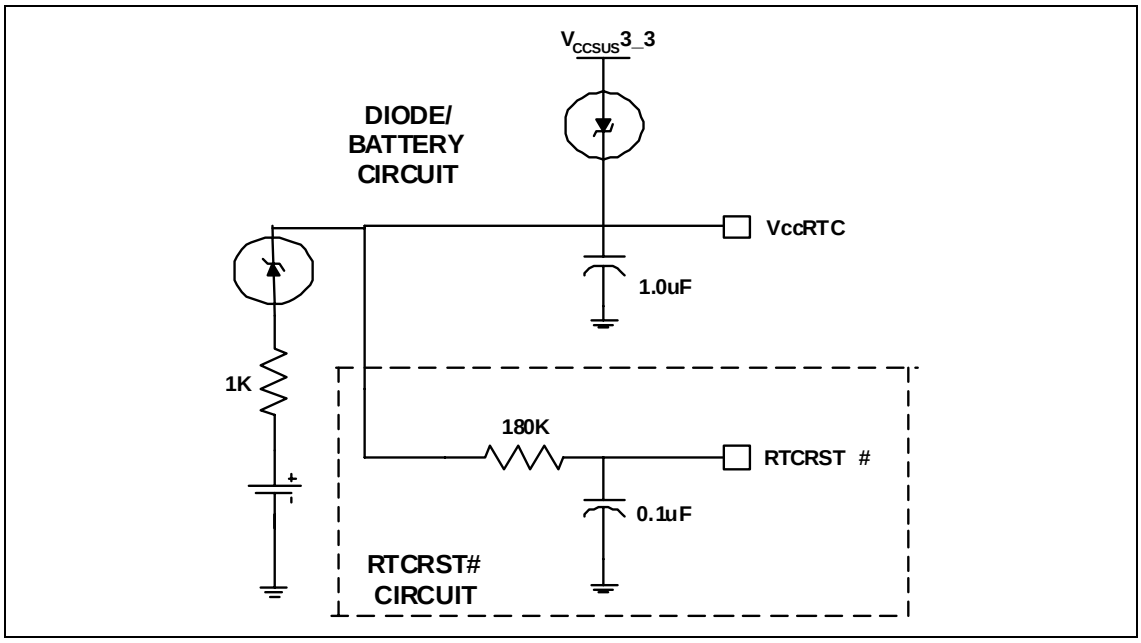
Figure 115. Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

9.8.5. RTC External RTCRST# Circuit

Figure 116. RTCRST# External Circuit for the ICH4-M RTC



The Intel 82801DBM ICH4-M RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some

time after the battery voltage is valid. The RC time delay should be in the range of 18 ms - 25 ms. Any resistor and capacitor combination that yields the proper time constant is acceptable. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 115) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 116 is an example of this circuitry that is used in conjunction with the external diode circuit.

9.8.6. V_{BIAS} DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC network of R2 and C3 (see Figure 114). Therefore, it is a self-adjusting voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200 mV DC. The RC network of R2 and C3 will filter out most of AC signal noise that exists on this ball. However, the noise on this ball should be kept minimal in order to guarantee the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details on measuring techniques.

Note that VBIAS is also very sensitive to environmental conditions.

9.8.7. SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30-70%. If the SUSCLK duty cycle is beyond 30-70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50- input impedance probe) and it is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH4-M's RTC Clock (see Application Note AP-728 for further details).

9.8.8. RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to V_{CC}RTC or pulled-down to ground while in the G3 state. RTCRST# when configured as shown in Figure 116 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to V_{CC}RTC. This will prevent these nodes from floating in G3, and correspondingly will prevent I_{CC}RTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

9.9. Internal LAN Layout Guidelines

The Intel 82801DBM ICH4-M provides several options for LAN capability. The platform supports several components depending upon the target market. Available LAN components include the Intel® 82540EP Gigabit Ethernet Controller, Intel® 82551QM Fast Ethernet Controller, Intel® 82562ET, and Intel® 82562EM Platform LAN Connect components.

Table 57. LAN Component Connections/Features

LAN Component	Interface to ICH4-M	Connection	Features
Intel 82540EP (196 BGA)	PCI	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible
Intel 82551QM (196 BGA)	PCI	Performance 10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible
Intel 82562EM (48 Pin SSOP)	LCI	Advanced 10/100 Ethernet	Ethernet 10/100 connection, Alert on LAN* (AoL)
Intel 82562ET (48 Pin SSOP)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

Design guidelines are provided for each required interface and connection.

9.9.1. Footprint Compatibility

The Intel 82540EP Gigabit Ethernet Controller and the Intel 82551QM Fast Ethernet Controller are all manufactured in a footprint compatible 15 mm x 15 mm (1-mm pitch), 196-ball grid array package. Many of the critical signal pin locations on the 82540EP and the 82551QM are identical, allowing designers to create a single design that accommodates any one of these parts. Because the usage of some pins on the 82540EP differ from the usage on the 82551QM, the parts are not referred to as “pin compatible.” The term “footprint compatible” refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design.

Design guidelines are provided for each required interface and connection. Refer to the following figures and the subsequent table for the corresponding section of this design guide.

Figure 117. Intel 82801DBM ICH4-M/Platform LAN Connect Section

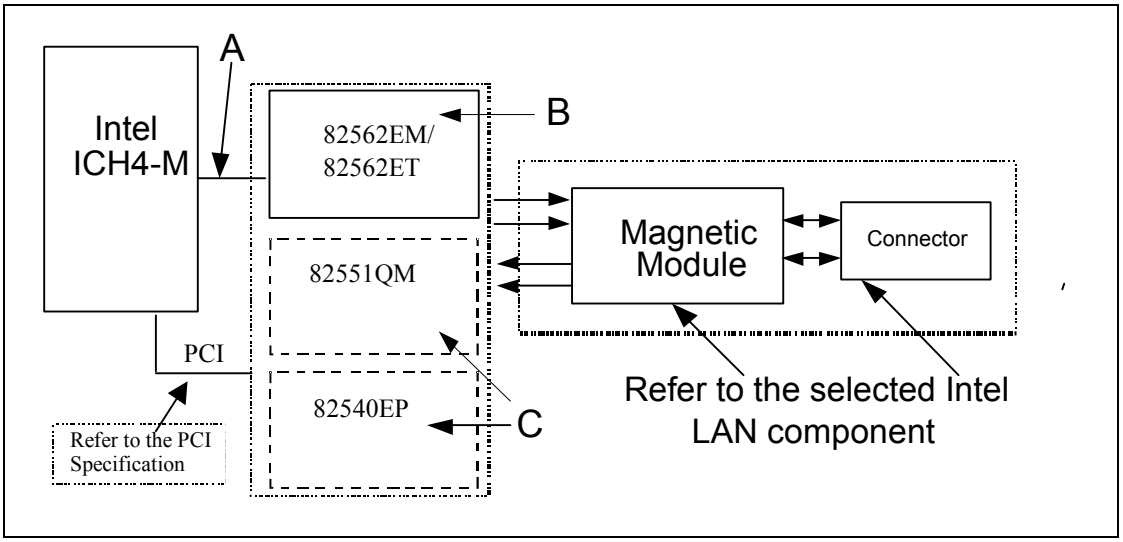


Table 58. LAN Design Guide Section Reference

Layout Section	Figure 117 Reference	Design Guide Section
Intel® ICH4-M – LAN Connect Interface (LCI)	A	Reference Section 9.9.2
Intel® 82562ET / Intel 82562EM	B	Reference Section 9.9.3
Intel® 82551QM / Intel 82540EP	C	Reference Section 9.9.5

9.9.2. Intel 82801DBM ICH4-M – LAN Connect Interface Guidelines

This section contains guidelines on how to implement a platform LAN Connect device on a system motherboard. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the Intel 82801DBM ICH4-M to LAN Connect Interface. The following signal lines are used on this interface:

LAN_CLK

LAN_RSTSYNC

LAN_RXD[2:0]

LAN_TXD[2:0]

This interface supports Intel 82562ET and Intel 82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by all components.

9.9.2.1. Bus Topologies

The Platform LAN Connect Interface can be configured in several topologies:

Direct point-to-point connection between the ICH4-M and the LAN component

LOM Implementation

9.9.2.1.1. LOM (LAN On Motherboard) Point-To-Point Interconnect

The following are guidelines for a single solution motherboard. Either Intel 82562EM or Intel 82562ET are uniquely installed.

Figure 118. Single Solution Interconnect

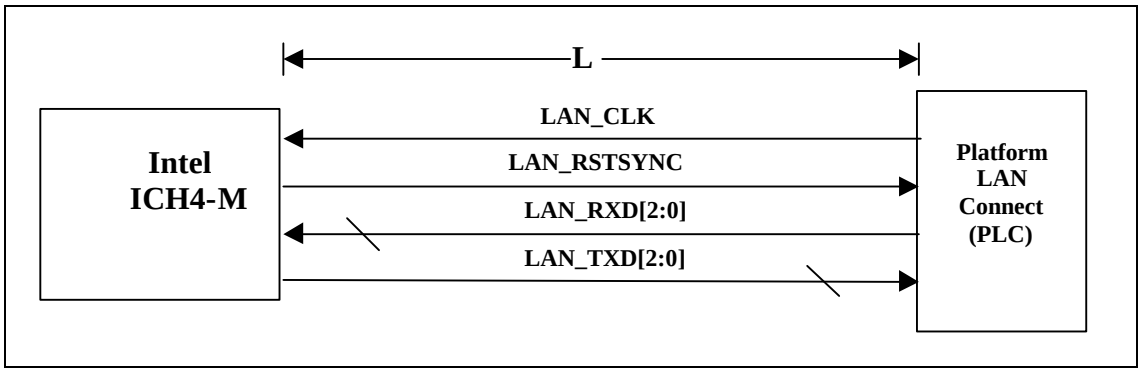


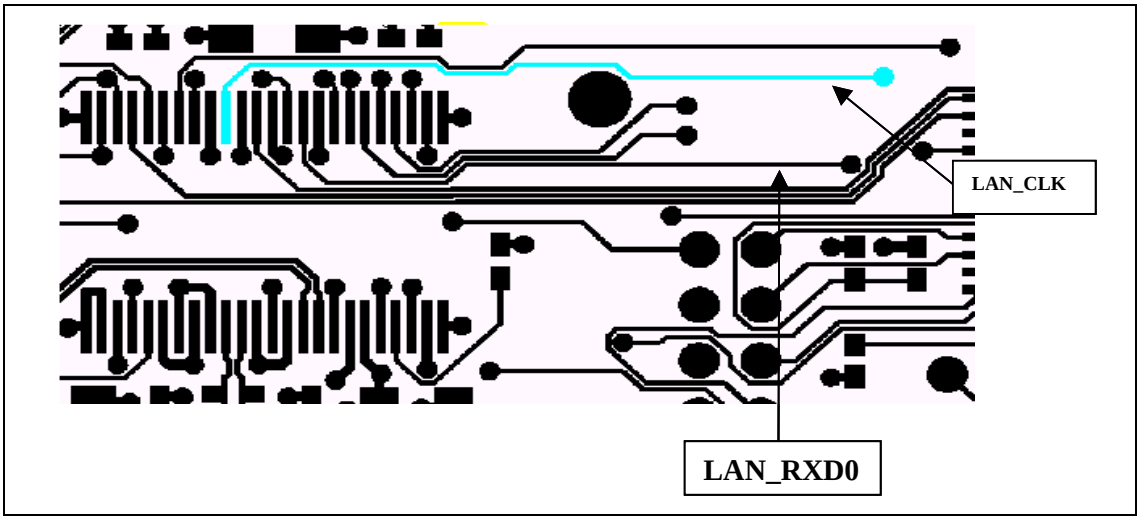
Table 59. LAN LOM Routing Summary

Trace Impedance	LAN Routing Requirements	Maximum Trace Length	Signal Referencing	LAN Signal Length Matching
55 ± 15%	5 on 10	4.5 to 12 inches	Ground	Data signals must be equal to or no more than 0.5 inches (500 mils) shorter than the LAN clock trace.

9.9.2.2. Signal Routing and Layout

Platform LAN Connect Interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. Intel recommends that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 119. LAN_CLK Routing Example



9.9.2.3. Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter. t_{RMATCH} is the sum of the trace length mismatch between LAN_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

9.9.2.4. Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard. An impedance of 55 ± 15% is strongly recommended; otherwise, signal integrity requirements may be violated.

9.9.2.5. Line Termination

Line termination mechanisms are not specified for the LAN Connect Interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 0- to 33- series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

9.9.2.6. Terminating Unused LAN Connect Interface Signals

The LAN Connect Interface on the ICH4-M can be left as a no-connect if it is not used.

9.9.3. Intel 82562ET / Intel 82562 EM Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 9.9.6. Additional guidelines for implementing an Intel 82562ET or Intel 82562EM Platform LAN Connect component are provided below.

9.9.3.1. Guidelines for Intel 82562ET / Intel 82562EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC and IEEE test specifications.

Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.9.3.2. Crystals and Oscillators

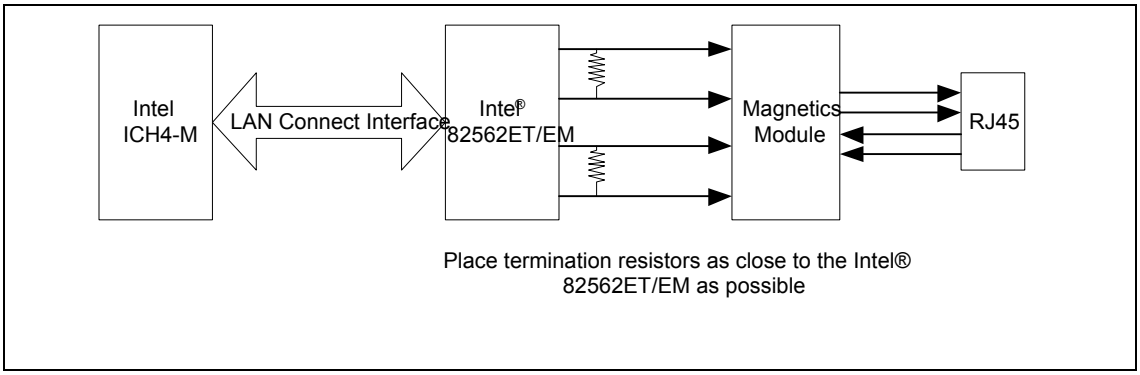
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent the possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discrete components as close as possible to the Intel 82562ET/EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

9.9.3.3. Intel 82562ET / Intel 82562EM Termination Resistors

The 100 ± 1% resistor used to terminate the differential transmit pairs (TDP/TDN) and the 121 ± 1% receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN connect component (Intel 82562ET or Intel 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e. Intel 82562ET), including the wire impedance reflected through the transformer.

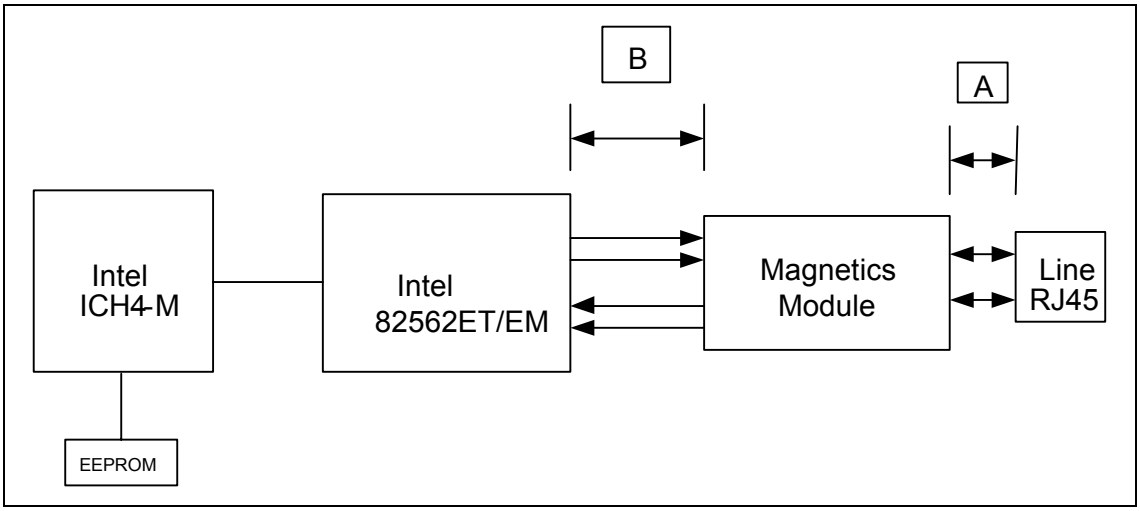
Figure 120. Intel 82562ET / Intel 82562EM Termination



9.9.3.4. Critical Dimensions

There are two dimensions to consider during layout. Distance 'A' from the line RJ-45 connector to the magnetics module and distance 'B' from the Intel 82562ET or Intel 82562EM to the magnetics module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches). See Figure 121.

Figure 121. Critical Dimensions for Component Placement



Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

9.9.3.4.1. Distance from Magnetics Module to RJ-45 (Distance A)

The distance A in Figure 121 above should be given the highest priority in board layout. The distance between the magnetics module and the RJ-45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

Differential Impedance: The differential impedance should be 100 . The single ended trace impedance will be approximately 50 ; however, the differential impedance can also be affected by the spacing between the traces.

Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the Intel 82562ET must be placed further than a couple of inches from the RJ-45 connector, distance B can be sacrificed. Keeping the total distance between the Intel 82562ET and RJ-45 will as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 to 110 should compensate for second order effects.

9.9.3.4.2. Distance from Intel 82562ET / 82562ET to Magnetics Module (Distance B)

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100- differential value. These traces should also be symmetric and equal length within each differential pair.

9.9.3.5. Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible because signals with fast rise and fall times contain many high frequency harmonics that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

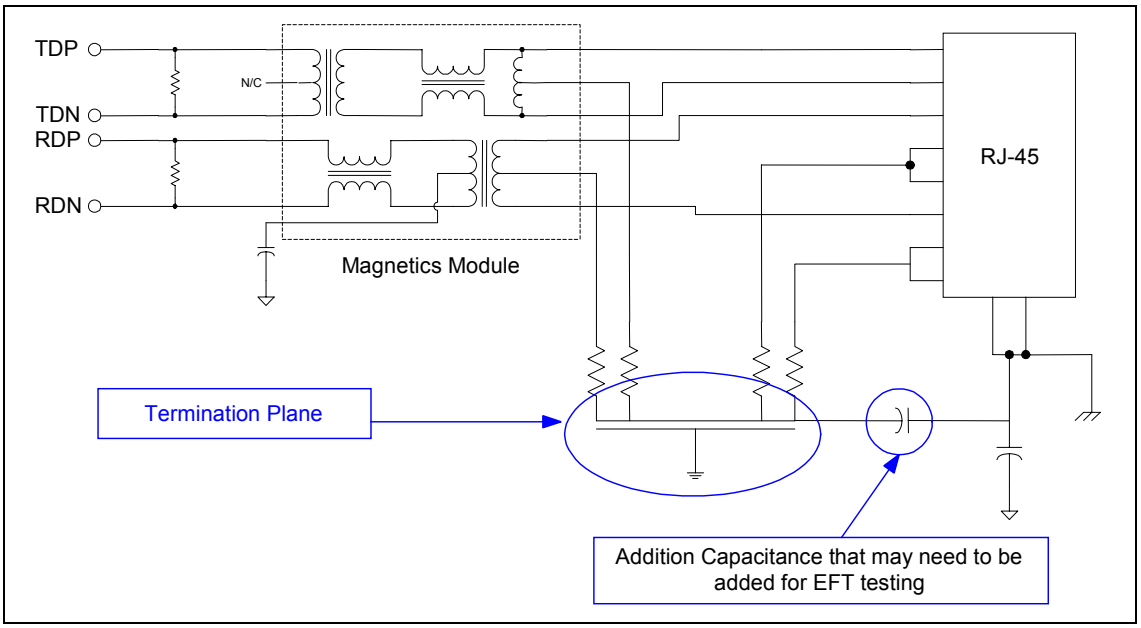
9.9.3.5.1. Terminating Unused Connections

In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the "Bob Smith" Termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75- resistors to the plane. Stray energy on unused pins is then carried to the plane.

9.9.3.5.2. Termination Plane Capacitance

Intel recommends that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ-45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

Figure 122. Termination Plane

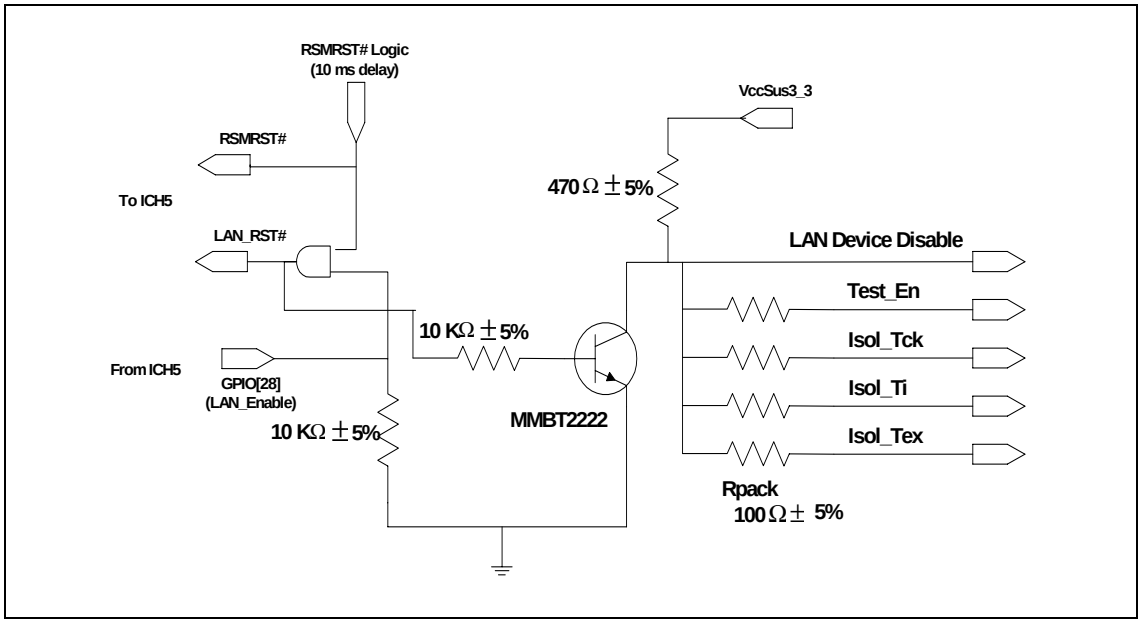


9.9.4. Intel 82562ET/EM Disable Guidelines

To disable the Intel 82562ET/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. The BIOS controlling the GPIO can disable the LAN micro-controller.

Note: LAN_RST# needs to be held low for 10 ms after power is stable. It is assumed that RSMRST# logic will provide this delay. Because GPIO28 will default to high during power up, an AND gate has been implemented to ensure the required delay for LAN_RST# is met.

Figure 123. Example Intel 82562ET/EM Disable and Power Down Circuitry



There are four pins which are used to put the Intel 82562ET/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. The table below describes the operational/disable features for this design.

The four control signals shown in the below table should be configured as follows: Test_En should be pulled-down through a 100- resistor. The remaining three control signals should each be connected through 100- series resistors to the common node “Intel 82562ET/EM _Disable” of the disable circuit.

Table 60. Intel 82562ET/EM Control Signals

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

In addition, if the LAN Connect Interface of the Intel 82801DBM ICH4-M is not used, the VccLAN1_5 and the VccLAN3_3 are still required to be powered during normal operating states. It is acceptable to power the VccLAN1_5 and VccLAN3_3 power pins by the same voltage source that supplies power to

the Vcc1_5 and Vcc3_3 power pins. Also, the LAN_RST# pin of the ICH4-M should be pulled-down to GND with a 10-k resistor to keep the interface disabled.

9.9.5. Design and Layout Consideration for Intel 82540EP / 82551QM

For specific design and layout considerations for the Intel 82540EP Gigabit Ethernet Controller and the Intel 82551QM Faster Ethernet Controller, please refer to the following documents:

82551QM / 82540EM Interchangeable LOM Design Application Note (AP 432) (Reference #10565)

82540EP Gigabit Ethernet Controller Networking Silicon Product Preview Datasheet

82540EP Gigabit Ethernet Controller Specification Update

82540EP/82541EI & 82562EZ(EX) Dual Footprint Design Guide Application Note (AP-444) (Reference# 12504)

9.9.6. General Intel 82562ET / 82562EM / 82551QM / 82540EP Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance.

Note: Some suggestions are specific to a 4.3-mil stack-up.

Maintain constant symmetry and spacing between the traces within a differential pair.

Keep the signal trace lengths of a differential pair equal to each other.

Keep the total length of each differential pair under 4 inches. (Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).)

Do not route the transmit differential traces closer than 100 mils to the receive differential traces.

Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).

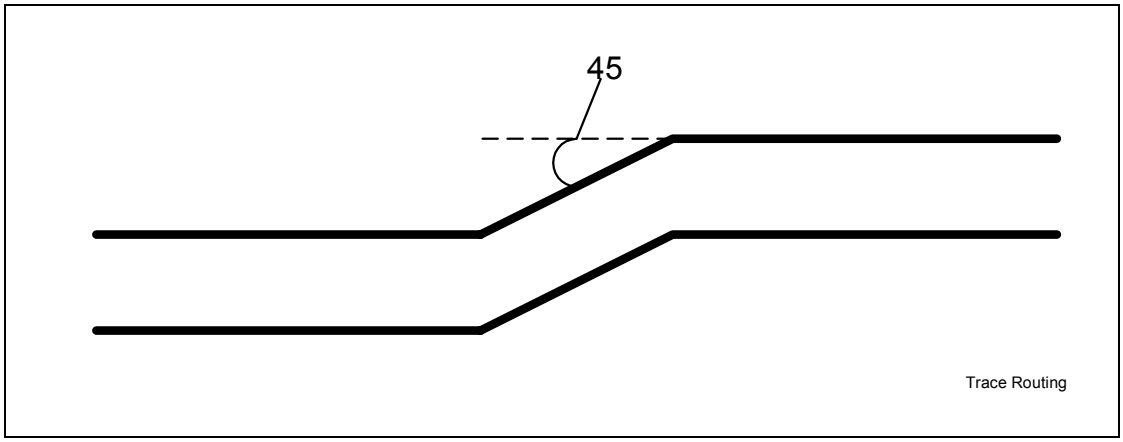
Keep maximum separation between differential pairs to 7 mils.

For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, Intel recommends using two 45° bends instead. Refer to Figure 124.

Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.

Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 124. Trace Routing



9.9.6.1.1. Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 . It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 , when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

9.9.6.1.2. Signal Isolation

Some rules to follow for signal isolation:

Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. NOTE: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.

Physically group together all components associated with one clock trace to reduce trace length and radiation.

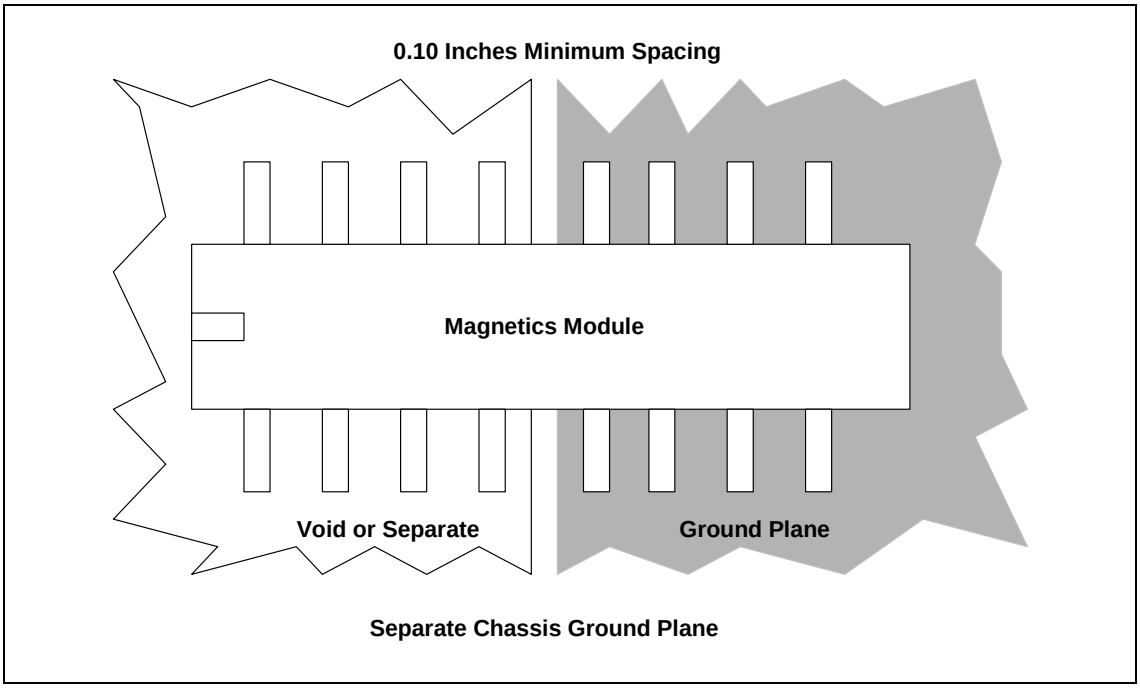
Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.

Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

9.9.6.1.3. Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum

Figure 125. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both back planes and motherboards.

Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.

Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.

All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.

Physically locate grounds between a signal path and its return. This will minimize the loop area.

Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.

The ground plane beneath the filter/transformer module should be split. The RJ-45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

9.9.6.2. Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN on motherboard designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. (Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (≤ one inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45, and the PLC.
6. Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
7. Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Please follow the appropriate reference schematic or Application Note.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have ~100- impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 and 85 , even when the designers think they've designed for 100 . (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close† to each other, the edge coupling can lower the effective differential impedance by 5 - 20 . A 10- - 15- drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.
10. Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the Intel 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail

at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These caps are not necessary, unless there is some overshoot in 100 Mbps mode.

Note: It is important to keep the two traces within a differential pair close† to each other. Keeping them close† helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e. FCC compliance) from the transmit traces, and better receive BER for the receive traces.

† Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

9.10. Power Management Interface

9.10.1. SYS_RESET# Usage Model

The System Reset signal (SYS_RESET#) of the Intel 82801DBM ICH4-M can be connected directly to a reset button or any other equivalent driver in the system where the desired effect is to immediately put the system into reset. If an Intel® Pentium® M Processor / Intel® Celeron® M Processor ITP700FLEX debug port is implemented on the system, Intel recommends that the DBR# signal of the ITP interface be connected to SYS_RESET# as well. If SYS_RESET# is implemented, a weak pull-up resistor pulled-up to the 3.3-V standby rail (VccSUS3_3) should also be implemented to ensure that no potential floating inputs to SYS_RESET# cause a system reset. The ICH4-M will debounce signals on this pin (16 ms) and allow the SMBus to go idle before resetting the system. This delay to allow all outstanding SMBus cycles to complete first and to prevent a slave device on the SMBus from “hanging” by resetting in the middle of an SMBus cycle.

9.10.2. PWRBTN# Usage Model

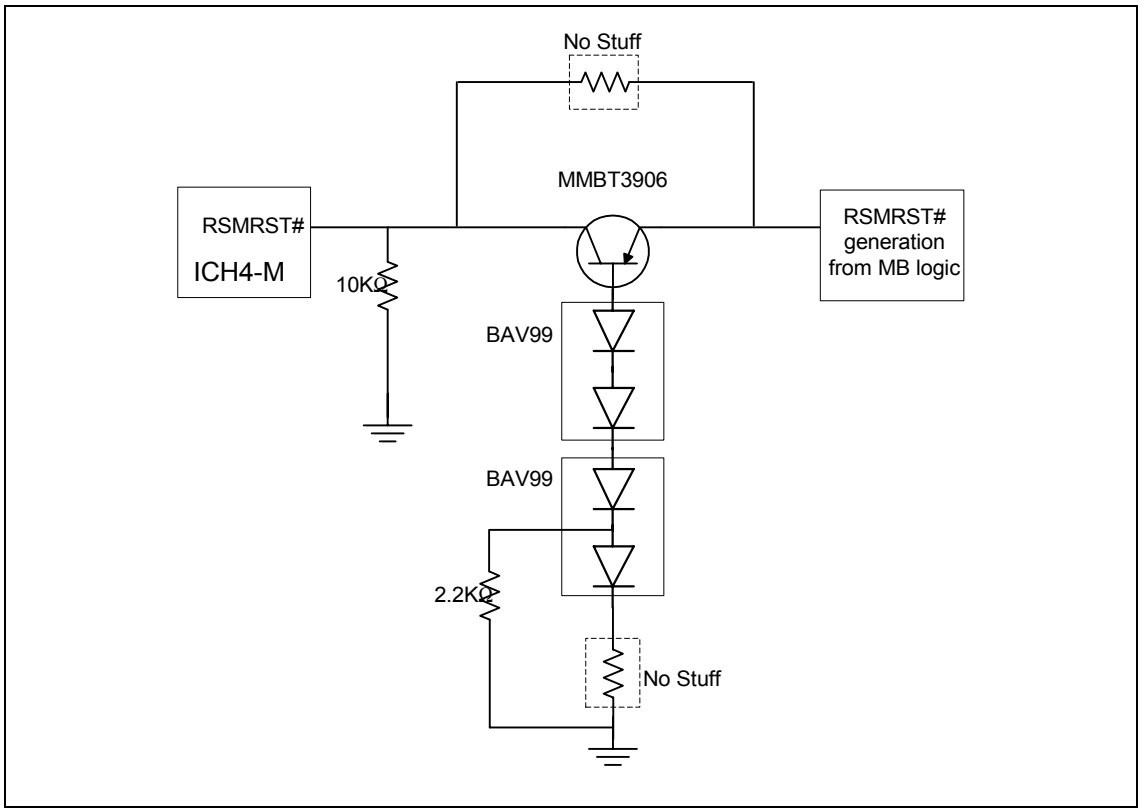
The Power Button signal (PWRBTN#) of the Intel 82801DBM ICH4-M can be connected directly to a power button or any other equivalent driver (e.g. power management controller) where the desired effect is to indicate a system request to go to a sleep state (if in a normal operating mode) or to cause a wake event (if in a sleep state already). This signal is internally pulled-up in the ICH4-M to the 3.3-V standby rail (VccSUS3_3) through a weak pull-up resistor (20 k nominal). The ICH4-M has 16 ms of internal debounce logic on this pin.

9.10.3. Power Well Isolation Control Strap Requirements

The RSMRST# signal of the ICH4-M must transition from 20% signal level to 80% signal level and vice-versa in 50us. Slower transitions may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node can potentially cause the CMOS to be cleared or corrupted, the RTC to loose time after several AC power cycles, or the intruder bit might assert erroneously.

The circuit shown in the figure below can be implemented to control well isolation between the VccSUS3_3 and RTC power-wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail or does not meet the above rise/fall time

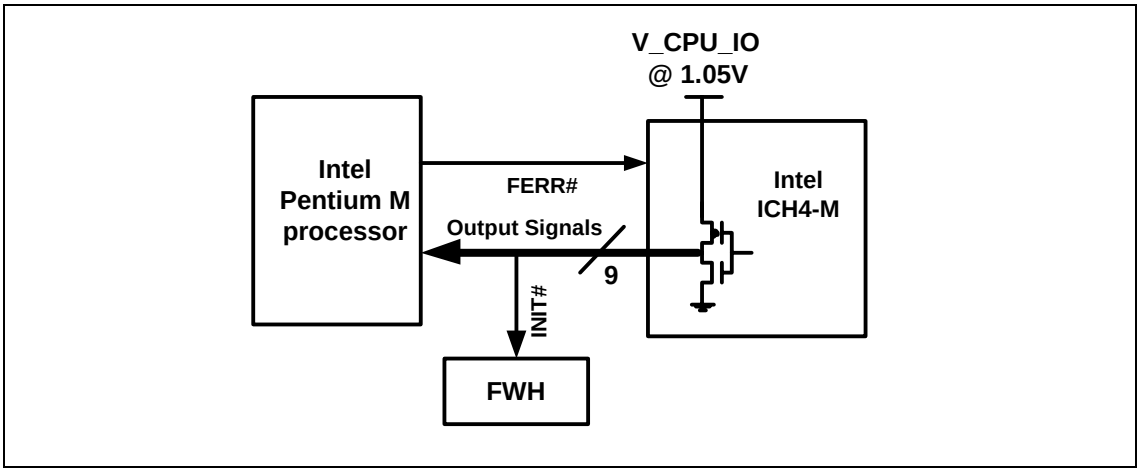
Figure 126. RTC Power Well Isolation Control



9.11. CPU I/O Signals Considerations

The Intel 82801DBM ICH4-M has been designed to be voltage compatible with the CMOS signals of the processor. For Intel Pentium M/Intel Celeron M processor-based systems, the ICH4-M's V_CPU_IO rail uses the same 1.05-V voltage as the V_{CCP} rails for the processor and Intel 855PM chipset. It is important to verify that the voltage requirements of all processor and ICH4-M signals are compatible with the FWH as well. See Section 9.7 for FWH details. Figure 127 shows a typical interface between the ICH4-M, CPU, and FWH. See Section 4.1.4 for recommended topologies and routing guidelines.

Figure 127. Intel 82801DBM ICH4-M CPU CMOS Signals with CPU and FWH



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10. Platform Clock Routing Guidelines

10.1. Clock Routing Guidelines

Only one clock generator component is required in an Intel 855PM chipset based system. Clock synthesizers that meet the *Intel® CK-408 Clock Synthesizer/Driver Specification* are suitable for an Intel 855PM chipset based system. For more information on CK-408 compliance, refer to the *CK-408 Clock Synthesizer/Driver Specification*. The following tables and figure list and detail the Intel 855PM MCH clock groups, the platform system clock cross-reference, and the platform clock distribution.

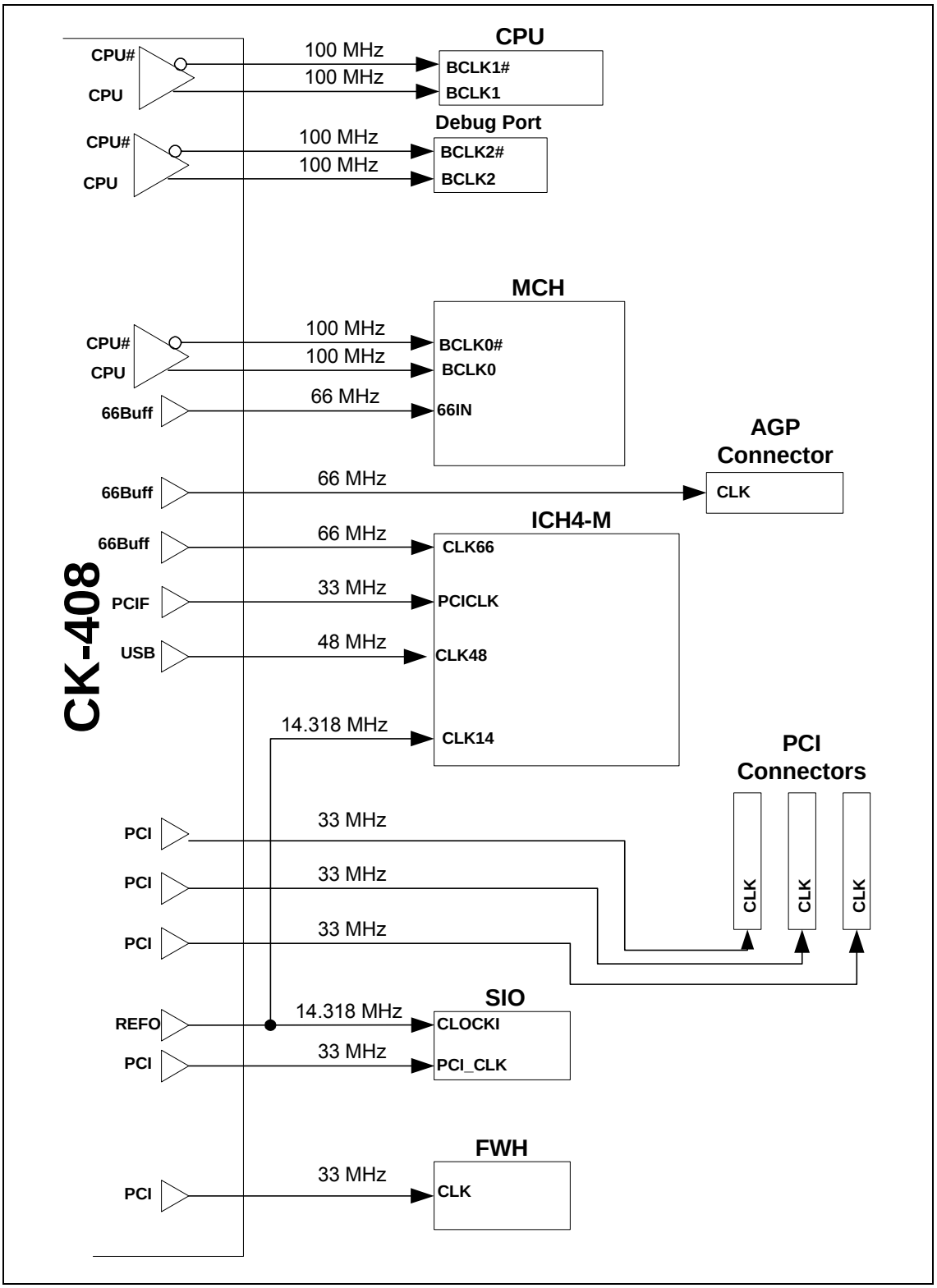
Table 61. Intel 855PM Chipset Clock Groups

Clock Name	Frequency	Receiver
HOST_CLK	100 MHz	CPU, Debug Port, and MCH
CLK66	66 MHz	Intel MCH and ICH4-M
AGPCLK	66 MHz	AGP Connector or AGP Device
CLK33	33 MHz	Intel ICH4-M, SIO, and FWH
CLK14	14.318 MHz	Intel ICH4-M and SIO
PCICLK	33 MHz	PCI Connector
USBCLK	48 MHz	Intel ICH4-M

Table 62. Platform System Clock Cross-reference

Clock Group	CK-408 Pin	Component	Component Pin Name
HOST_CLK	CPU	CPU	BCLK[0]
	CPU#	CPU	BCLK[1]
	CPU	Debug Port	BCLK[0]
	CPU#	Debug Port	BCLK[1]
	CPU	MCH	BCLK[0]
	CPU#	MCH	BCLK[1]
CLK66	3V66	MCH	66IN
		ICH4-M	CLK66
AGPCLK	3V66	AGP Connector or AGP Device	CLK
CLK33	PCIF	ICH4-M	PCICLK
	PCI	SIO	PCI_CLK
		FWH	CLK
CLK14	REF0	ICH4-M	CLK14
		SIO	CLOCKI
PCICLK	PCI	PCI Connector or PCI Device #1	CLK
		PCI Connector or PCI Device #2	CLK
		PCI Connector or PCI Device #3	CLK
USBCLK	USB	ICH4-M	CLK48

Figure 128. Platform Clock Topology Diagram



10.2. Clock Group Topology and Layout Routing Guidelines

10.2.1. HOST_CLK Clock Group

The clock synthesizer provides three pairs of 100-MHz differential clock outputs utilizing a 0.7-V voltage swing. The 100-MHz differential clocks are driven to the Intel Pentium M/Intel Celeron M processor, the Intel 855PM MCH, and the processor debug port with the topology shown in the figure below.

The clock driver differential bus output structure is a “Current Mode Current Steering” output which develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedances or to accommodate future load requirements.

The recommended termination for the differential bus clock is a “Source Shunt termination.” Refer to Figure 129 for an illustration of this terminology scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver’s output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be selected to match the characteristic impedance of the system board and Rs should be 33 ± 5%. Simulations have shown that Rs values above 33 provide no benefit to signal integrity but only degrade the edge rate.

The MULT0 pin (CK-408 pin #43) should be pulled-up through a 10 k to VCC – setting the multiplication factor to 6.

The IREF pin (CK-408 pin # 42) should be tied to ground through a 475 ± 1 % resistor – making the IREF 2.32 mA.

Figure 129. Source Shunt Termination Topology

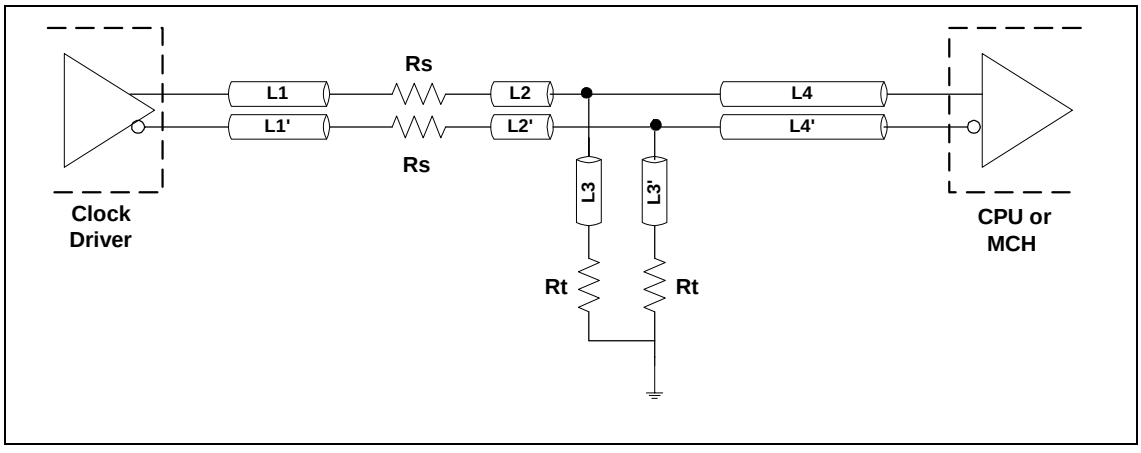


Table 63. BCLK/BCLK#[1:0] Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	HOST_CLK		1
Motherboard Topology	Source Shunt Termination		
Reference Plane	Ground Referenced (Contiguous over entire length)		
BCLK Skew Between Agents	500 ps Total Budget: 250 ps for Flight Skew; 100 ps for Pin-to-Pin Skew; 150 ps for Jitter	Figure 130	2, 3, 4, 5
Differential Pair Spacing	7 mils		6, 7
Trace Width	4 mils		8
Spacing to Other Traces	Min = 25 mils		
System Board Impedance – Differential	100 ± 15%		9
System Board Impedance – Odd Mode	50 ± 15%		10
Processor Routing Length – L1, L1': Clock Driver to Rs	Max = 0.50 inches	Figure 129	14
Processor Routing Length – L2, L2': Rs to Rt Node	Min = 0 inches Max = 0.20 inches	Figure 129	14
Processor Routing Length – L3, L3': Rt Node to Rt	Min = 0 inches Max = 0.50 inches	Figure 129	14
Processor Routing Length – L4, L4': Rt Node to Receiver	Min = 2.0 inches Max = 8.0 inches	Figure 129	
MCH Routing Length – L1, L1': Clock Driver to Rs	Max = 0.50 inches	Figure 129	14
MCH Routing Length – L2, L2': Rs to Rt Node	Min = 0 inches Max = 0.20 inches	Figure 129	14
MCH Routing Length – L3, L3': Rt Node to Rt	Min = 0 inches Max = 0.50 inches	Figure 129	14
MCH Routing Length – L4, L4': Rt Node to Receiver	Min = 2.0 inches Max = 8.0 inches	Figure 129	
Processor L1/L1' and MCH L1/L1' Length Matching	± 10 mils		16
Clock Driver-to-Processor and Clock Driver-to-MCH Length Matching (L1 + L2 + L4)	- 400 mils ± 50 mils		11
Processor BCLK (L1 + L2 + L4) and BCLK# (L1' + L2' + L4') Length Matching	± 10 mils		
MCH BCLK (L1 + L2 + L4) and BCLK# (L1' + L2' + L4') Length Matching	± 10 mils		
Series Termination Resistor (Rs)	33 ± 5%	Figure 129	12
Parallel Termination Resistor (Rt)	49.9 ± 1% (for 55 MB impedance)	Figure 129	13

NOTES:

1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. This number does not include clock driver common mode.
3. The skew budget includes clock driver output pair to output pair jitter (differential jitter), and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
4. The interconnect portion of the total budget for this specification assumes clock pairs are routed on multiple routing layers and routed no longer than the maximum recommended lengths.
5. Skew measured at the load between any two, bus agents. Measured at the crossing point.
6. Edge-to-edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
7. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.
8. Set the line width to meet correct system board impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack-up.
9. The differential impedance of each clock pair is approximately 2*Z single-ended*(1-2*Kb) where Kb is the backwards crosstalk coefficient. For the recommended trace spacing, Kb is very small and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
10. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the BCLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.
11. Values are based on socket dimensions/tolerances/parasitics outlined in the *Intel® Mobile Processor Micro-FCPGA Socket (mPGA479M) Design Guidelines (Order number: 298520)*. Or in general terms, a 4mm ± 5% socket with lumped parasitics model. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the system board trace length for the chipset will be longer than that for the processor. e.g. If Clock Driver-to-MCH = 4.0” then Clock Driver-to-Processor = 3.6” ± 50 mils.
12. Rs value of 33Ω has shown to be an effective solution.
13. Rt shunt termination value should match the system board impedance.
14. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ring back.
15. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in Er and the impedance variations due to physical tolerances of circuit board material.
16. Minimize the trace length difference between L1/L1’ of the processor and MCH BCLK/BCLK# pair to minimize skew. Length matching of L1/L1’ within 10 mils should be between the shortest BCLK/BCLK# signal of one pair to the longest BCLK/BCLK# signal of the other pair.

10.2.1.1. BCLK Length Matching Requirements

To compensate for the extra delay introduced by the processor socket dimensions/tolerances/parasitics as well as the package parasitics, the Clock Driver-to-MCH (L1 + L2 + L4) motherboard routing will be longer than Clock Driver-to-Processor (L1 + L2 + L4) motherboard routing. **Clock Driver-to-MCH routing should be 400 mils ± 50 mils longer than Clock Driver-to-Processor routing**. i.e. the following relationship should be adhered to:

Clock Driver-to-Processor (L1 + L2 + L4) = Clock Driver-to-MCH (L1 + L2 + L4) – 400 mils ± 50 mils

In order to minimize the clock skew between the processor and the MCH, the L1/L1’ segments of the two FSB agents should be exactly trace length matched if possible. The routing should be done such that the shortest L1/L1’ segment of the processor is matched within ± 10 mils of the longest L1/L1’ segment of the MCH. i.e. the following relationship should be adhered to:

Processor shortest(L1/L1’) = MCH longest(L1/L1’) ± 10 mils.

Additionally, the routing of each half of the host clock pair for the processor and MCH should be trace length matched within ± 10 mils of its complement’s routing. i.e. the following relationships should be adhered to:

Processor (L1 + L2 + L4) = Processor (L1’ + L2’ + L4’) ± 10 mils

and

MCH (L1 + L2 + L4) = MCH (L1' + L2' + L4') ± 10 mils

10.2.1.2. BCLK General Routing Guidelines

Below is the general guidelines for routing the BCLK:

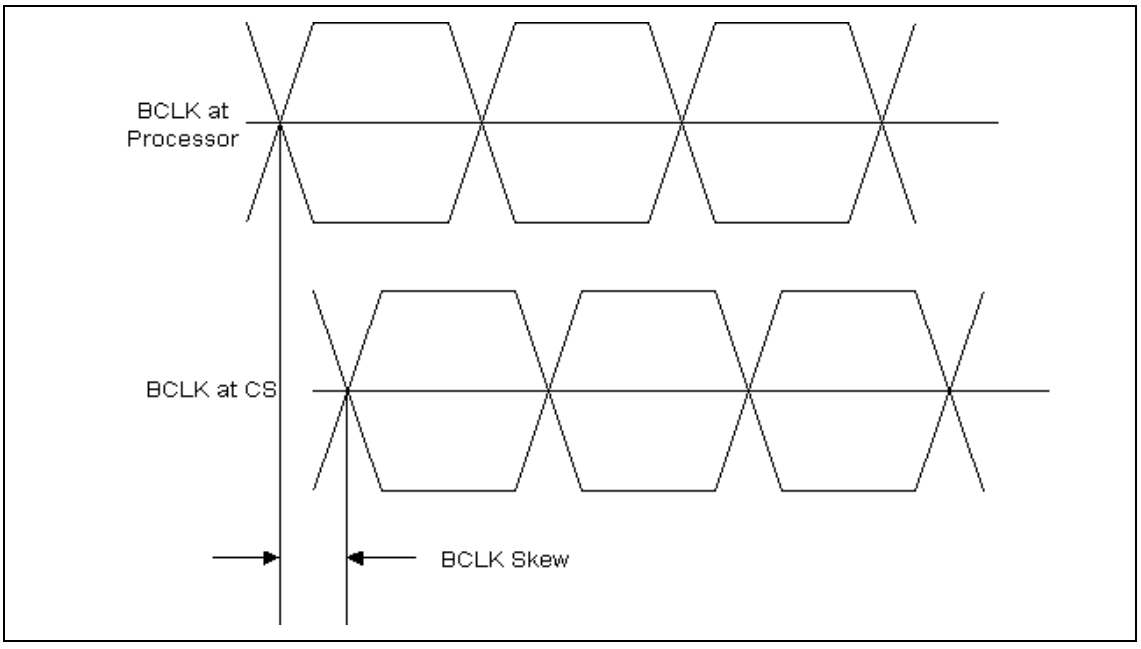
1. When routing the 100-MHz differential clocks, do not split up the two halves of a differential clock pair between layers and route to all agents on the same physical routing layer referenced to ground.
2. If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
3. Do not place vias between adjacent complementary clock traces and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

10.2.1.3. EMI constraints

Clocks are a significant contributor to EMI and should be treated with care. The following recommendations can aid in EMI reduction:

1. Maintain uniform spacing between the two halves of differential clocks.
2. Route clocks on physical layer adjacent to the VSS reference plane only.

Figure 130. Clock Skew as Measured from Agent-to-Agent



10.2.2. CLK66 Clock Group

The driver is the clock synthesizer 66-MHz clock output buffer and the receiver is the 66-MHz clock input buffer at the Intel 855PM MCH and the Intel 82801DBM ICH4-M. Note that the goal is to have as little skew between the clocks within this group as possible.

Figure 131. CLK66 Group Topology

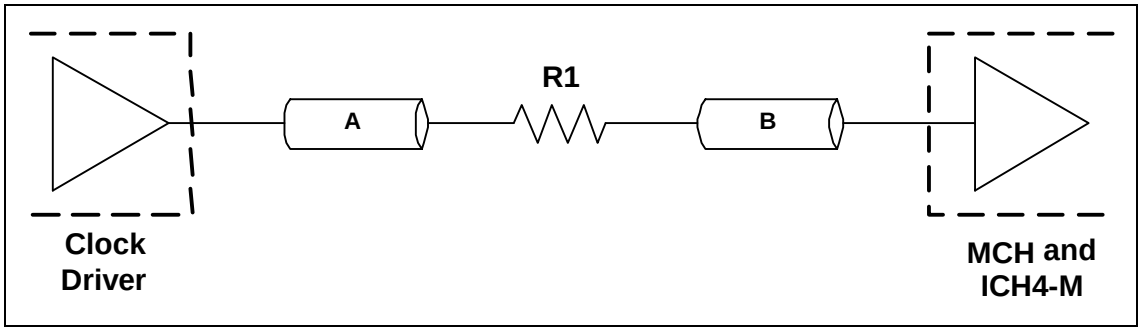


Table 64. CLK66 Group Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	CLK66		1
Motherboard Topology	Point-to-Point		
Reference Plane	Ground Referenced (Contiguous over entire length)		
Characteristic Trace Impedance (Zo)	55 ± 15%		
Trace Width	4 mils		
Trace to Space Ratio	1:5 (e.g. 4 mils trace 20 mils space)		
Group Spacing	Isolation spacing from non-Clock signals = 20 mils minimum		
Trace Length – A	Min = 0 inches Max = 0.50 inches	Figure 131	
Trace Length – B	Min = 4.0 inches Max = 8.50 inches	Figure 131	
Series Termination Resistor (R1)	33 ± 5%	Figure 131	
Skew Requirements	Minimal skew (~ 0) between clocks within the CLK66 group		
Clock Driver MCH	X		2
Clock Driver to ICH4-M	X ± 100 mils		2

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. If the trace length from clock driver to MCH is X, then the trace length from clock driver to ICH4-M must be length matched within 100 mils.

10.2.3. AGPCLK Clock Group

The driver is the clock synthesizer 66-MHz clock output buffer and the receiver is the 66-MHz clock input buffer at the AGP device. Note that the goal is to have minimal (~ 0) skew between this clock and the clocks in the clock group CLK66.

Figure 132. AGPCLK to AGP Connector Topology

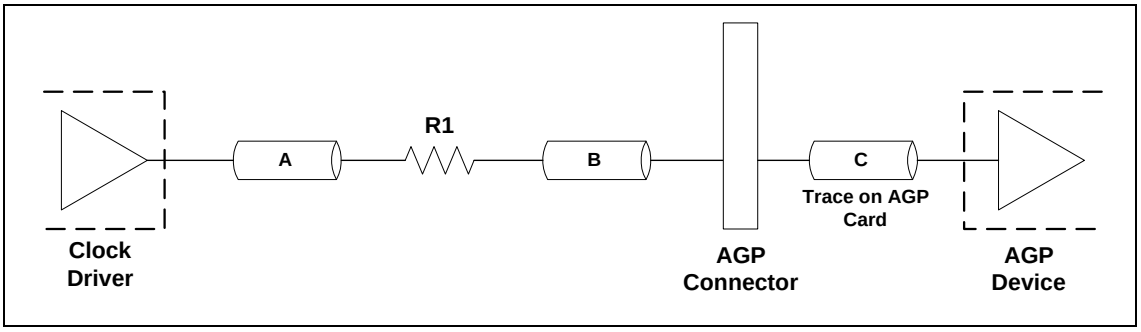


Figure 133. AGPCLK to AGP Device Down Topology

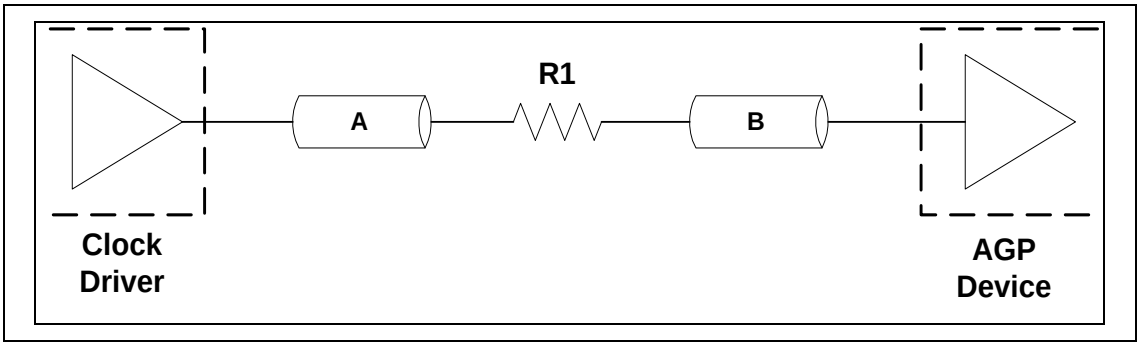


Table 65. AGPCLK Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	AGPCLK		1
Motherboard Topology	Point-to-Point		
Reference Plane	Ground Referenced (Contiguous over entire length)		
Characteristic Trace Impedance (Zo)	55 ± 15%		
Trace Width	4 mils		
Trace to Space Ratio	1:5 (e.g. 4 mils trace 20 mils space)		
Group Spacing	Isolation spacing from non-Clock signals = 20 mils minimum		
Trace Length – A	Trace length matched to CLK66 Trace A	Figure 132, Figure 133	2
Trace Length – B (Option #1)	Must be exactly trace length matched to CLK66 Trace B	Figure 133	3
Trace Length – B (Option #2)	Must be exactly trace length matched to [(CLK66 Trace B) - 4.0 inches]	Figure 132	4
Trace Length – C	Routed 4.0 inches per the AGP Specification	Figure 132	
Series Termination Resistor (R1)	33 ± 5%	Figure 133	
Skew Requirements	Minimal skew (~ 0) between AGPCLK and CLK66 group		

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.
2. AGPCLK Trace A should be trace length matched to CLK66 Trace A as closely as possible.
3. To achieve minimal skew for AGP device down topologies, AGPCLK Trace B should be matched as closely to CLK66 Trace B as possible.
4. To achieve minimal skew for AGP connector topologies, AGPCLK Trace B should be matched as closely to CLK66 Trace B as possible. Note that Trace C is assumed to be 4.0 inches on the AGP card and should be subtracted from the AGPCLK Trace B length when matching to CLK66 Trace B.

10.2.4. CLK33 Clock Group

The driver is the clock synthesizer 33-MHz clock output buffer and the receiver is the 33-MHz clock input buffer at the ICH4-M, FWH, and SIO.

Note: The goal is to have minimal (~ 0) skew between the clocks within this group, and also minimal (~ 0) skew between the clocks of this group and that of group CLK66.

Figure 134. CLK33 Group Topology

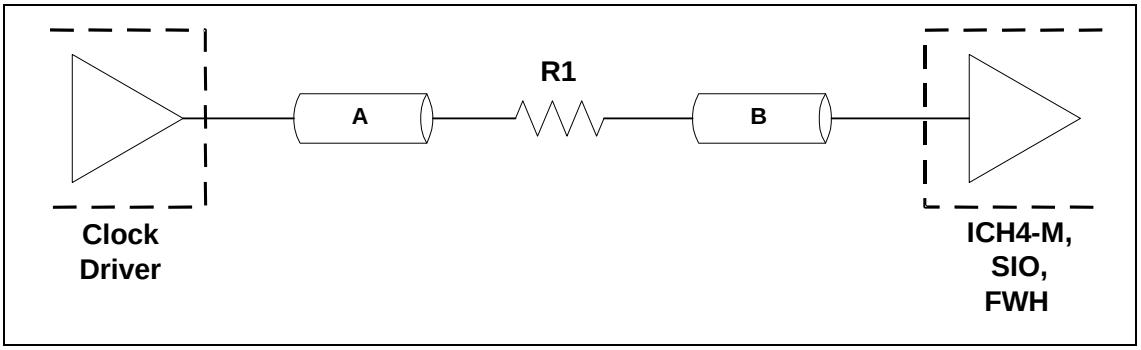


Table 66. CLK33 Group Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	CLK33		1
Motherboard Topology	Point-to-Point		
Reference Plane	Ground Referenced (Contiguous over entire length)		
Characteristic Trace Impedance (Zo)	55 ± 15%		
Trace Width	4 mils		
Trace to Space Ratio	1:5 (e.g. 4 mils trace 20 mils space)		
Group Spacing	Isolation spacing from non-Clock signals = 20 mils minimum		
Trace Length – A	Must be exactly trace length matched to CLK66 Trace A	Figure 134	
Trace Length – B	Must be exactly trace length matched to CLK66 Trace B	Figure 134	
Series Termination Resistor (R1)	33 ± 5%	Figure 134	
Skew Requirements	Minimal skew (~ 0) between CLK33 group and CLK66 group		

NOTES:
1. Recommended resistor values and trace lengths may change in a later revision of the design guide.

10.2.5. PCICLK Clock Group

The driver is the clock synthesizer 33-MHz clock output buffer and the receiver is the 33-MHz clock input buffer at the PCI devices on the PCI cards. Note that the goal is to have a maximum of ±1 ns skew between the clocks within this group, and also a maximum of ± 1 ns skew between the clocks of this group and that of group CLK33.

Figure 135. PCICLK Group to PCI Device Down Topology

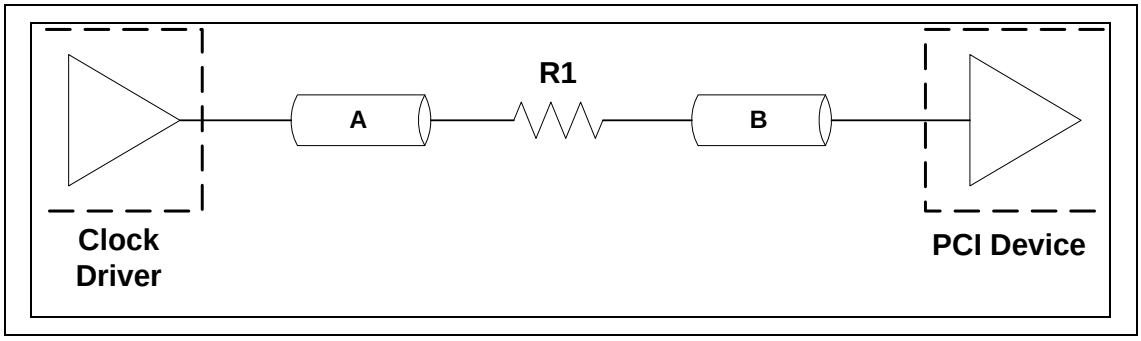


Table 67. PCICLK Group Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	PCICLK		1
Motherboard Topology	Point-to-Point		
Reference Plane	Ground Referenced (Contiguous over entire length)		
Characteristic Trace Impedance (Zo)	55 ±15%		
Trace Width	5 mils		
Trace to Space Ratio	1:4 (e.g. 5 mils trace 20 mils space)		
Group Spacing	Isolation spacing from non-Clock signals = 20 mils minimum		
Trace Length – A	Must be exactly trace length matched to CLK33 Trace A	Figure 135	
Trace Length – B	Must be exactly trace length matched to CLK33 Trace B	Figure 135	
Series Termination Resistor (R1)	33 ± 5%	Figure 135	
Skew Requirements	Maximum of ± 1 ns of skew between clocks within the PCICLK group and a maximum of ± 1 ns of skew between the clocks of this group and those of CLK33		

NOTE: Recommended resistor values and trace lengths may change in a later revision of the design guide.

Figure 136. PCICLK Group to PCI Slot Topology

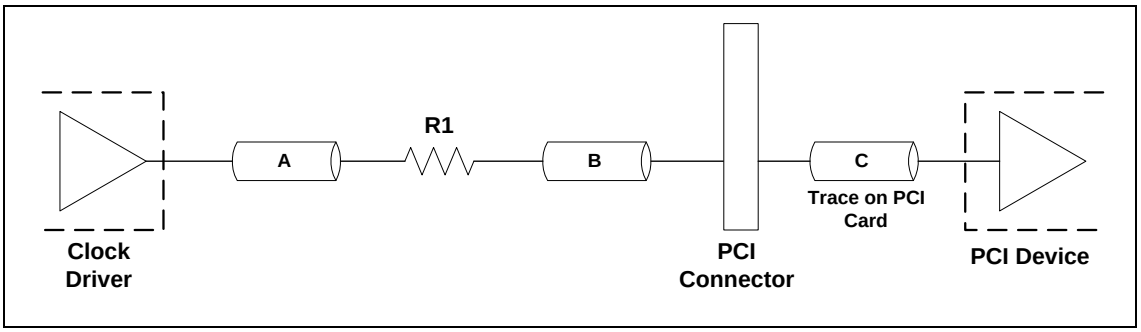


Table 68. PCICLK Group Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	PCICLK		1
Motherboard Topology	Point-to-Point		
Reference Plane	Ground Referenced (Contiguous over entire length)		
Characteristic Trace Impedance (Zo)	55 ± 15%		
Trace Width	5 mils		
Trace to Space Ratio	1:2 (e.g. 5 mils trace 10 mils space)		
Group Spacing	Isolation spacing from non-Clock signals = 10 mils minimum		
Trace Length – A	Must be exactly trace length matched to CLK33 Trace A	Figure 136	
Trace Length – B	(CLK33 Trace B) – 2.5”	Figure 136	
Trace Length – C	Routed 2.5” per the PCI Specification	Figure 136	
Series Termination Resistor (R1)	33 ± 5%	Figure 136	
Skew Requirements	Maximum of ± 1 ns of skew between clocks within the PCICLK group and a maximum of ± 1 ns of skew between the clocks of this group and those of CLK33		

NOTE: Recommended resistor values and trace lengths may change in a later revision of the design guide.

10.2.6. USBCLK Clock Group

The driver is the clock synthesizer USB clock output buffer and the receiver is the USB clock input buffer at the ICH4-M. Note that this clock is asynchronous to any other clock on the board.

Figure 137. USBCLK Group Topology

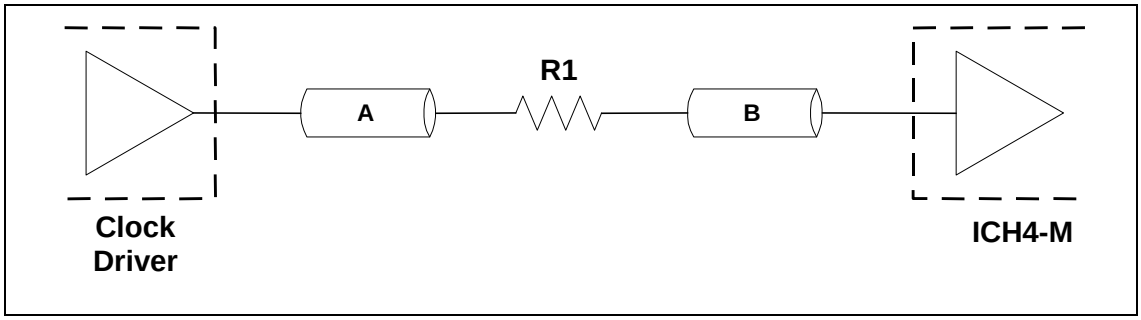


Table 69. USBCLK Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	USBCLK		1
Motherboard Topology	Point-to-Point		
Reference Plane	Ground Referenced (Contiguous over entire length)		
Characteristic Trace Impedance (Zo)	55 ± 15%		
Trace Width	5 mils		
Trace to Space Ratio	1:2 (e.g. 5 mils trace 10 mils space)		
Group Spacing	Isolation spacing from non-Clock signals = 20 mils minimum		
Trace Length – A	Min = 0 inches Max = 0.50 inches	Figure 137	
Trace Length – B	Min = 3.0 inches Max = 12.0 inches	Figure 137	
Series Termination Resistor (R1)	33 ± 5%	Figure 137	
Skew Requirements	None – USBCLK is asynchronous to any other clock on the platform		

NOTE: Recommended resistor values and trace lengths may change in a later revision of the design guide.

10.2.7. CLK14 Clock Group

The driver is the clock synthesizer 14.318-MHz clock output buffer and the receiver is the 14.318-MHz clock input buffer at the ICH4-M and SIO. Note that the clocks within this group should have minimal skew (~ 0) between each other, however each of the clocks in this group is asynchronous to clocks of any other group.

Figure 138. CLK14 Group Topology

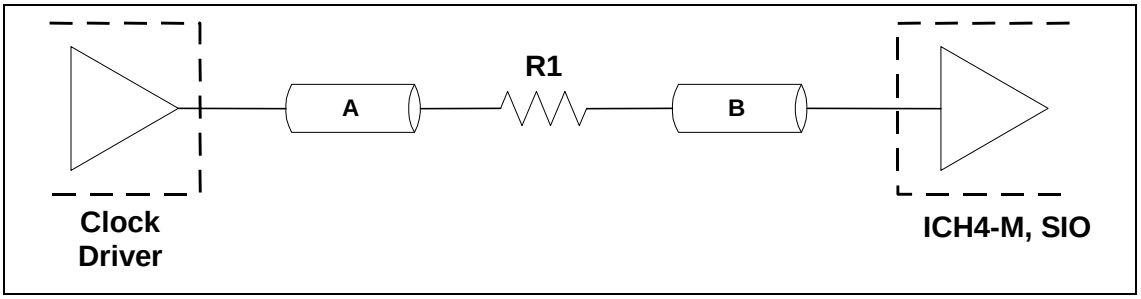


Table 70. CLK14 Group Routing Guidelines

Parameter	Routing Guidelines	Figure	Notes
Signal Group	CLK14		1
Motherboard Topology	Point-to-Point		
Reference Plane	Ground Referenced (Contiguous over entire length)		
Characteristic Trace Impedance (Zo)	55 ± 15%		
Trace Width	5 mils		
Trace to Space Ratio	1:2 (e.g. 5 mils trace 10 mils space)		
Group Spacing	Isolation spacing from non-Clock signals = 10 mils minimum		
Trace Length – A	Min = 0 inches Max = 0.50 inches	Figure 138	
Trace Length – B	Min = 4.0 inches Max = 8.50 inches	Figure 138	
Series Termination Resistor (R1)	33 ± 5%	Figure 138	
Skew Requirements	Minimal skew (~ 0) between CLK14 group and other groups, however the CLK14 group is asynchronous to all other groups		

NOTE: Recommended resistor values and trace lengths may change in a later revision of the design guide.

10.2.8. CK-408 Clock Chip Decoupling

See Section 11.7.9 for details.

10.3. CK-408 Updates for Systems based on Intel Pentium M Processor / Intel Celeron M Processor and Intel 855PM Chipset

To maximize the power savings on systems based on Intel Pentium M processor / Intel Celeron M processor and Intel 855PM chipset, additional registers have been added to the CK-408 clock generator to allow option to tri-state the CPU[2:0] host clocks during CPU_STOP# or PWRDWN assertion. The option to have CPU[2:0] driven (default) or tri-stated can be programmed via the serial I^2C bus interface to the CK-408 clock driver. If the tri-state feature on the CPU[2:0] signals is chosen, it is recommended that the STP_CPU# signal from the ICH4-M drive the CK-408's CPU_STOP# signal. Also, it is recommended that the ICH4-M's DPSLP# signal be connected to the DPSLP# pin of the processor and MCH. Functionally, the ICH4-M's STP_CPU# and DPSLP# signals are equivalent. However, STP_CPU# is powered by the main I/O well (3.3 V) and is sent to the CK-408 whereas DPSLP# is driven to the processor interface voltage (1.05 V).

10.4. CK-408 PWRDWN# Signal Connections

For Intel Pentium M processor / Intel Celeron M processor based systems that support the S1M state, the PWRDWN# input of the CK-408 clock chip is **required** to be driven by **both** the SLP_S1# and SLP_S3# signals from the Intel 82801DBM ICH4-M, i.e. the PWRDWN# pin of the CK-408 should be driven by the output of the logical AND of the SLP_S1# and SLP_S3# signals. This configuration best allows CPU[2:0] to be tri-stated during S1-M or lower (numerically higher) states.

For systems that do not support S1M but do support the S3 state, the PWRDWN# input of the CK-408 clock chip should be connected to the SLP_S3# output of the ICH4-M. It is **not** recommended that PWRDWN# be pulled-up to the CK-408's 3.3-V power supply if the S3 state is the second highest, power consuming state supported by the platform (i.e., S1M and S2 not supported). The advantage of using SLP_S3# rather than the 3.3-V supply to qualify PWRDWN# is that it reduces the likelihood of the CK-408 clocks driving into unpowered components and potentially damaging the clock input buffers. Also SLP_S3# can help reduce power consumption because it will be asserted before the 3.3-V supply will be shut off, thus minimizing the amount of time that the clocks will be left toggling.

11. Platform Power Delivery Guidelines

11.1. Definitions

S0 / Full-On operation:

During *Full-On* operation, all components on the motherboard are powered and the system is fully functional.

S1-M / Power-On-Suspend (POS, Mobile):

In the mobile implementation of the *Power-On-Suspend* state, the outputs of the clock chip stopped in order to save power. All components remain powered but may or may not be in a low power state.

S3 / Suspend-To-RAM (STR):

In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered.

S4 / Suspend-To-Disk (STD):

In the STD state, the system state is stored in non-volatile secondary storage (e.g. a hard disk) and all unnecessary system logic is turned off. Only logic required to *wake* the system remain powered. Standby power rails may or may not be powered depending on system design and the presence of AC or battery power.

S5 / Soft-Off:

The *Soft-Off* state corresponds to the G2 state. Restart is only possible with the power button.

Full-Power operation:

During *Full-Power* operation, all components remain powered. *Full-power* operation includes both *Full-On* and the S1M (CPU Stop-Grant state).

Suspend operation:

During *suspend* operation, power is removed from some components on the motherboard. Intel® 855PM chipset-based systems can be designed to support a number of suspend states such as *Power-On-Suspend* (S1M), *Suspend-to-RAM* (S3), *Suspend-to-Disk* (S4), and *Soft-Off* (S5).

Core power rail:

A power rail that is only on during *full-power* operation. These power rails are on when the PSON signal is asserted to the ATX power supply.

Standby power rail:

A power rail that in on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby

power rail that is distributed *directly* from the ATX power supply is: 5 V_{SB} (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.

Derived power rail:

A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3 V_{SB} is usually derived (on the motherboard) from 5 V_{SB} using a voltage regulator.

Dual power rail:

A *dual* power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation. Note that the voltage on a *dual* power rail may be misleading.

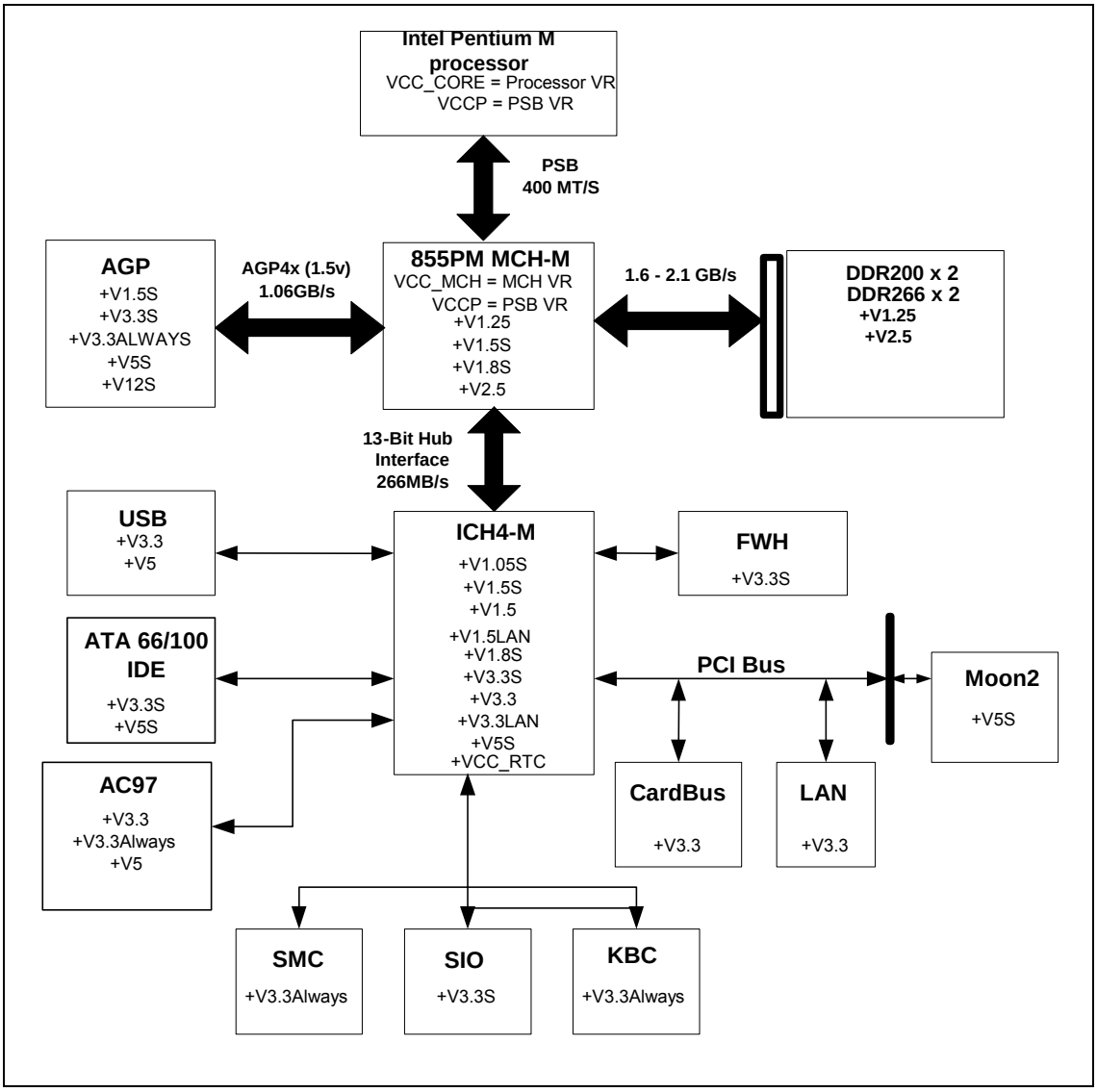
11.2. Platform Power Requirements

The following figure shows the power delivery architecture for an example Intel 855PM chipset platform. This power delivery architecture supports the "Instantly Available PC Design Guidelines" via the S3 system state. To ensure that enough power is available during S3, a thorough power budget should be completed. The power requirements should include each device's power requirements, both in *suspend* and in *Full-On*. The power requirements should be compared against the power budget supplied by the power supply. Due to the requirements of main memory and PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a *dual* power rail.

The solutions given in this document are only examples. There are many power distribution methods that achieve similar results. It is critical, when deviating from these examples, to consider the effect of the change.

11.2.1. Platform Power Delivery Architectural Block Diagram

Figure 139. Platform Power Delivery Map



11.3. Voltage Supply

11.3.1. Power Management States

Table 71. Power Management States

Signal	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*	+V*S	Clocks
FULL ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M (POS)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (STR)	LOW	LOW	HIGH	HIGH	ON	ON/OFF	OFF	OFF
S4 (STD)	LOW	LOW	LOW	HIGH	ON	ON/OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	LOW	ON	ON/OFF	OFF	OFF

11.4. Intel 855PM MCH / 82801DBM ICH4-M Platform Power-Up Sequence

Figure 140 describes the power-on timing sequence for an Intel 855PM/82801DBM-based platform.

Figure 140. Intel® 855PM/82801DBM Platform Power-Up Sequence

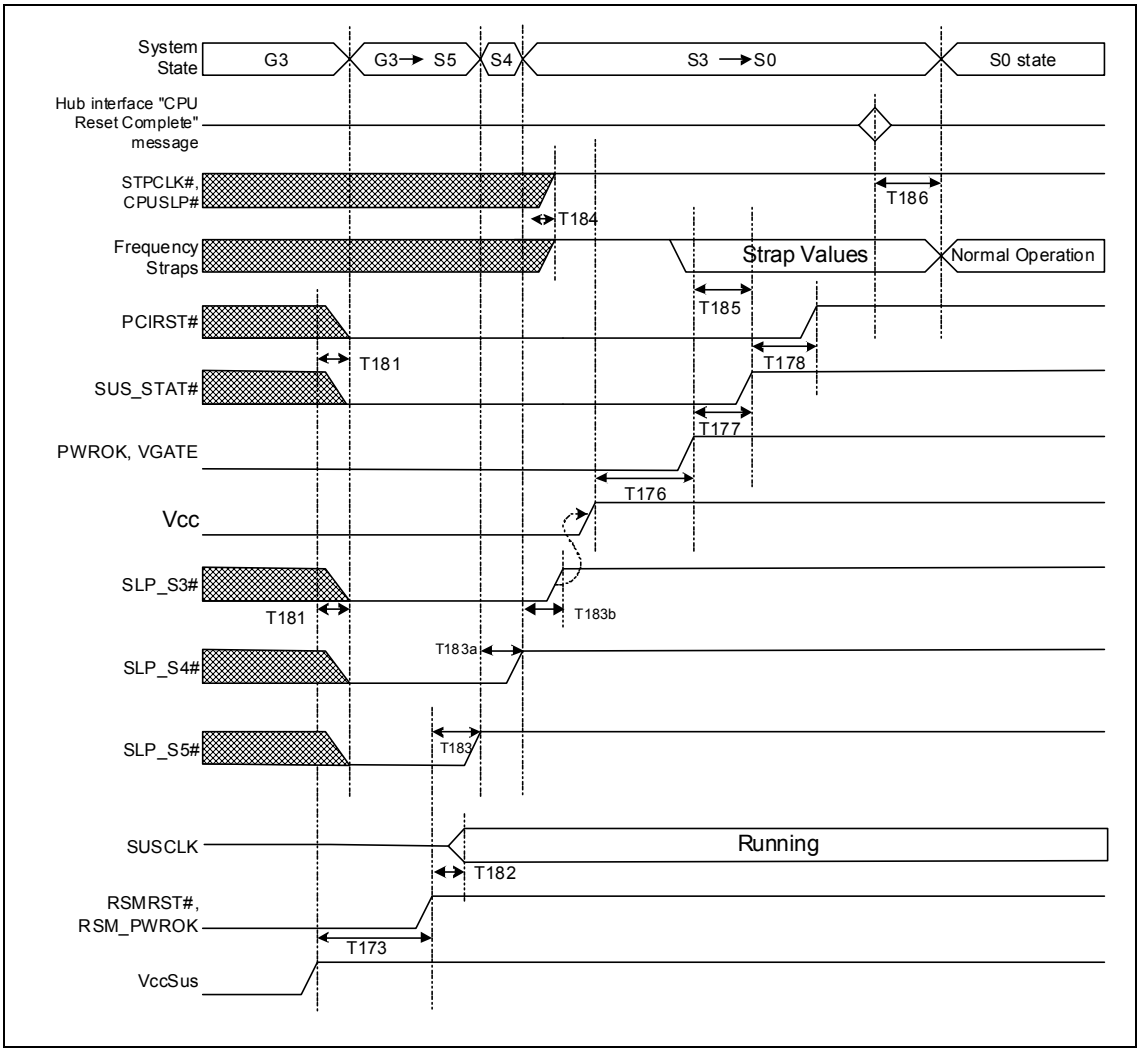


Table 72. Timing Sequence Parameters for Figure 140

Sym	Description	Min	Max	Units	Notes	Fig
T173	VccSus supplies active to RSMRST# inactive	5	-	ms		139
T175b	VccLAN supplies active to LAN_RST# active	10	-	ms		139
T176	Vcc supplies active to PWROK, VGATE active	10	-	ms		139
T177	PWROK and VGATE active and SYS_RESET# inactive to SUS_STAT# inactive	32	38	RTCCLK		139
T178	SUS_STAT# inactive to PCIRST# inactive	1	3	RTCCLK		139
T181	VccSus active to SLP_S5#, SUS_STAT# and PCIRST# active		50	ns		139
T182/T183	RSMRST# inactive to SUSCLK running, SLP_S5# inactive		110	ms	1	139
T183a	SLP_S5# inactive to SLP_S4# inactive	1	2	RTCCLK		139
T183b	SLP_S4# inactive to SLP_S3# inactive	1	2	RTCCLK		139
T184	Vcc active to STPCLK#, CPUSLP#, STP_CPU#, STP_PCI#, SLP_S1#, C3_STAT# inactive, and CPU Frequency Strap signals high		50	ns		139
T185	PWROK and VGATE active and SYS_RESET# inactive to SUS_STAT# inactive and CPU Frequency Straps latched to strap values	32	38	RTCCLK	2	139
T186	CPU Reset Complete to Frequency Straps signals unlatched from strap values	7	9	CLK66	3	139

NOTES:
1. If there is no RTC battery in the system, so VccRTC and the VccSus supplies come up together, the delay from RTCRST# and the RSMRST# inactive to SUSCLK toggling may be as much as 1000 ms.
2. These transitions are clocked off the internal RTC. One RTC clock is approximately 32 µs.
3. This transition is clocked off the 66-MHz CLK66. One CLK66 is approximately 15 ns.

11.4.1. Intel 82801DBM ICH4-M Power Sequencing Requirements

11.4.1.1. 3.3/1.5 V and 3.3/1.8 V Power Sequencing

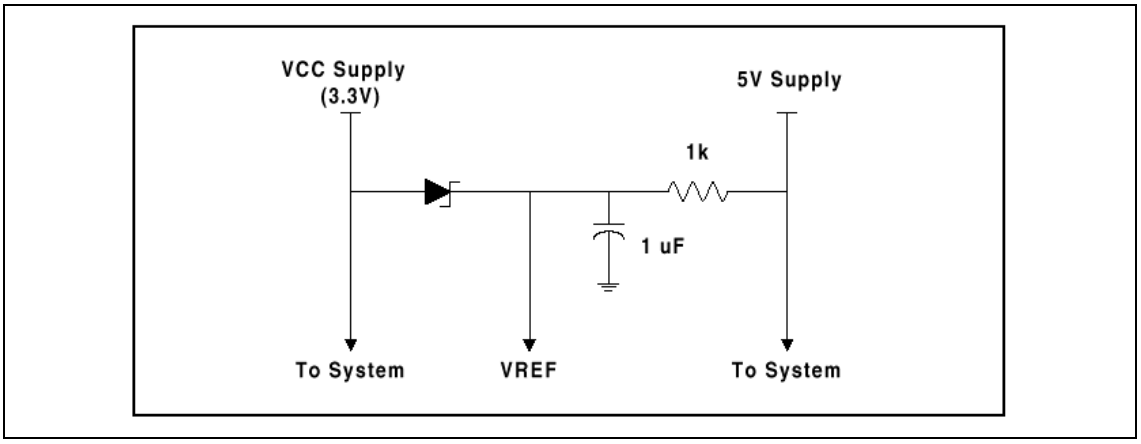
No power sequencing requirements exist for the associated 3.3 V/1.5 V rails or the 3.3 V/1.8 V rail of the ICH4-M. It is generally good design practice to power up the core before or at the same time as the other rails.

11.4.1.2. V_{5REF}/ 3.3 V Sequencing

V_{5REF} is the reference voltage for 5 V tolerance on inputs to the Intel 82801DBM ICH4-M. V_{5REF} must be powered up before V_{CC3_3}, or after V_{CC3_3} within 0.7 V. Also, V_{5REF} must power down after V_{CC3_3}, or before V_{CC3_3} within 0.7 V. It must also power down after or simultaneous to V_{CC3_3}. These rules must be followed in order to ensure the proper functionality of the ICH4-M. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the V_{CC3_3} rail. Figure 141 shows a sample implementation of how to satisfy the V_{5REF}/ 3.3 V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the V_{CCSUS3_3} rail is derived from the V_{CCSUS5} and therefore, the V_{CCSUS3_3} rail will always come up after the V_{CCSUS5} rail. As a result, V_{5REF_SUS} will always be powered up before V_{CCSUS3_3}. In platforms that do not derive the V_{CCSUS3_3} rail from the V_{CCSUS5} rail, this rule must be comprehended in the platform design.

Figure 141. Example V_{5REF} / 3.3 V Sequencing Circuitry



11.4.1.3. V_{5REF_SUS} Design Guidelines

The aforementioned rule for V_{5REF} also applies to the V_{5REF_SUS} input pin. However, in some platforms, the V_{CCSUS3_3} rail is derived from the V_{CCSUS5} and therefore, the V_{CCSUS3_3} rail will always come up after the V_{CCSUS5} rail. As a result, V_{5REF_SUS} will always be powered up before V_{CCSUS3_3}. In platforms where the V_{CCSUS3_3} rail is not derived from the V_{CCSUS5} rail, the V_{5REF} sequencing rule must be comprehended in the platform design.

In order to meet reliability and testing requirements for the USB interface, the following design recommendations for the V_{5REF_SUS} pins of the ICH4-M should be followed. Changes to the USB specification regarding continuous short conditions must be addressed. The USB 1.1 specification

requires host controllers to withstand a continuous short between the USB 5-V connector supply to a USB signal at the connector for an unspecified duration of time. Also, the USB 2.0 specification requires a host controller to withstand a short between the USB 5 V connector supply to a USB signal at the connector for 24 hours. The recommendation is to provide a 5V_ALWAYS (active S0-S5) supply to the V_{5REF_SUS} pins if available (see Figure 142). If such a supply rail is not readily available on the platform, then an alternative implementation using a 3.3V_ALWAYS (active S0-S5) and a V_{CC5} (active S0-S1M) or V_{CCSUS5} (active S0-S3) rail can be used instead (see Figure 143).

Figure 142. V5REF_SUS With 5V_ALWAYS Connection Option

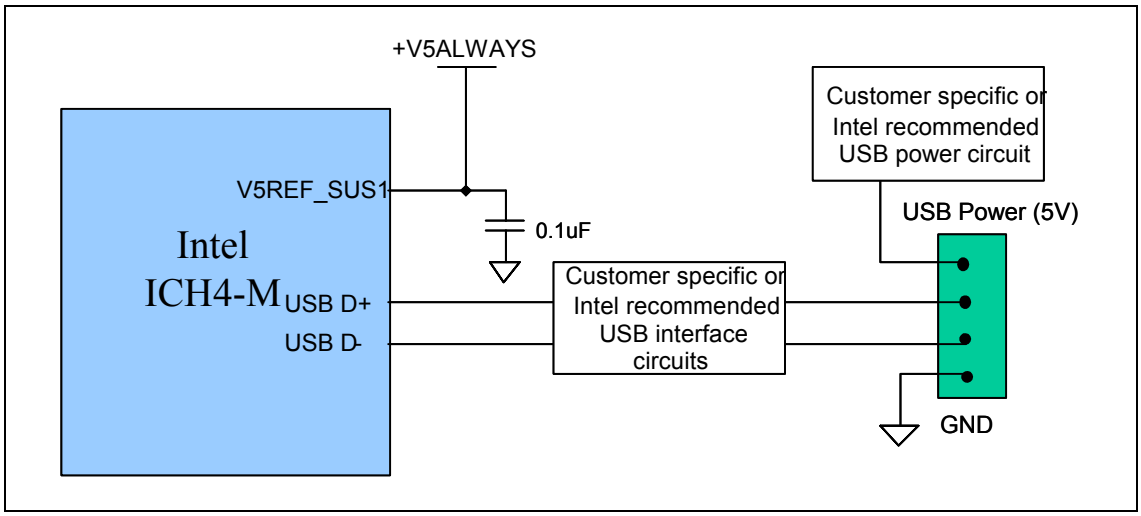
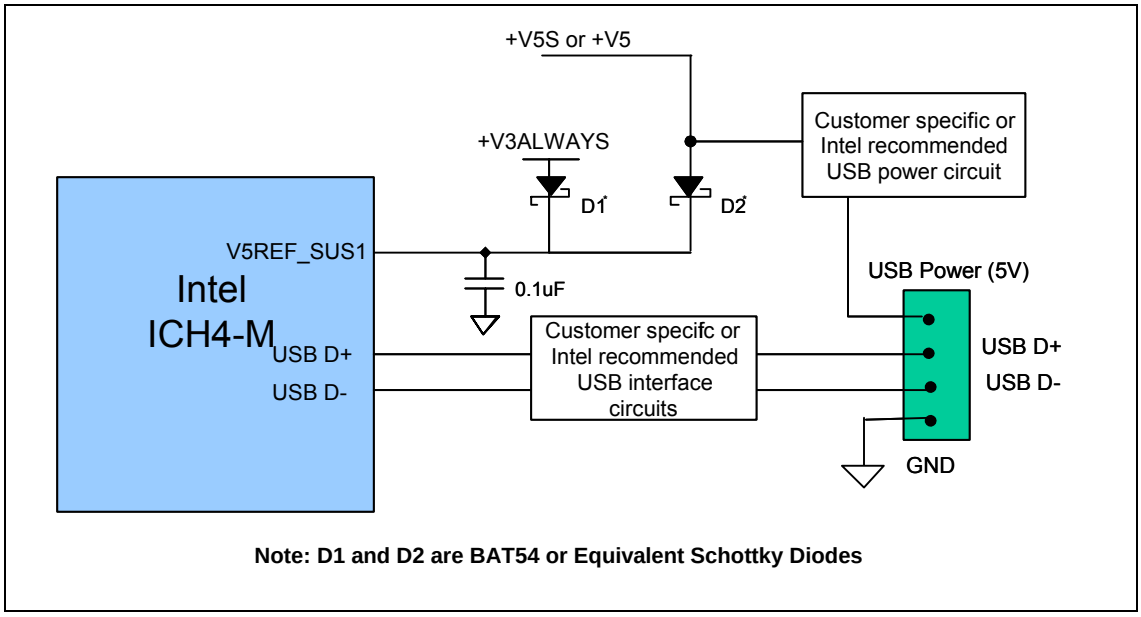


Figure 143. V5REF_SUS With 3.3V_ALWAYS and VCC5 or VCC5_SUS Connection Option



Note: D1 and D2 are BAT54 or Equivalent Schottky Diodes

11.4.2. Intel 855PM MCH Power Sequencing Requirements

No Intel 855PM MCH power sequencing requirements exist for the system incorporating the Intel 855PM chipset. All MCH power rails should be stable before de-asserting reset, but the power rails can be brought up in any order desired. Good design practice would have all MCH power rails come up as close in time as practical, with the core voltage (1.2 V) coming up first.

Although no power sequencing requirements between any of the MCH's rails exist, there are timing requirements that must be met with respect to other control signals that indicate the status of platform power rails. The 1.8-V supply rail that powers the Hub Interface of the MCH also powers the isolated, analog supply pins for the PLLs on the processor (VCCA[3:0]) and MCH (VCCGA and VCCHA). The 1.8-V supply to the processor must be stable for a minimum of 4 s **before** the ICH4-M's CPUPWRGOOD signal can be asserted to the processor's PWRGOOD input. Similarly, the RSTIN# input of the MCH must be asserted by the Intel 82801DBM ICH4-M's PCIRST# signal for a minimum of 4 s **after** the 1.8-V supply is stable.

11.4.3. DDR Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements are specified during power up or power down if the following criteria are met:

VDD and VDDQ are driven from a single power converter output

VTT is limited to 1.44 V (reflecting VDDQ(max)/2 + 50 mV VREF variation + 40 mV VTT variation)

VREF tracks VDDQ/2

A minimum resistance of 42 (22 series resistor + 22 parallel resistor ± 5% tolerance) limits the input current from the VTT supply into any pin

If the above criteria cannot be met by the system design, then the following Table 73 must be adhered to during power up.

Table 73. DDR Power-Up Initialization Sequence

Voltage Description	Sequencing	Voltage Relationship to Avoid Latch-up
VDDQ	After or with VDD	< VDD + 0.3 V
VTT	After or with VDDQ	< VDDQ + 0.3 V
VREF	After or with VDDQ	< VDQ + 0.3 V

11.5. DDR Power Delivery Design Guidelines

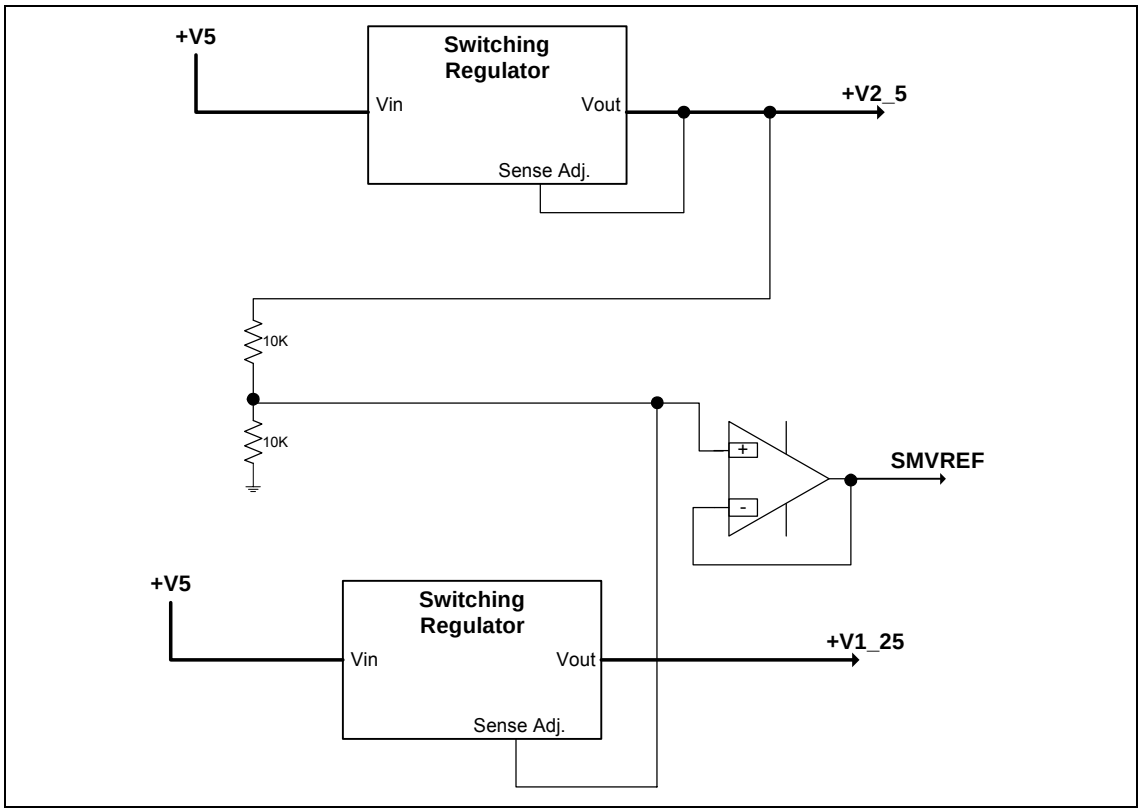
The main focus of these Intel 855PM MCH guidelines is to minimize signal integrity problems and improve the power delivery to of the MCH system memory interface and the DDR SO-DIMMs. Some sections summarize the DDR system voltage and current requirements as of publishing for this document. This document is not the original source for these specifications. Refer to the following documents for the latest details on voltage and current requirements found in this design guide.

JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification

Intel DDR 200 JEDEC Spec Addendum Rev 0.9 or later

Intel® 855PM Memory Controller Hub (MCH) DDR 200/266 MHz Datasheet

Figure 144. DDR Power Delivery Block Diagram



11.5.1. DDR Interface Decoupling Guidelines

The following is the recommended decoupling guidelines for the DDR system memory interface.

11.5.1.1. Intel 855PM MCH VCCSM Decoupling Guidelines

Every Intel 855PM MCH ground and VCCSM power ball in the system memory interface should have its own via. For the VCCSM pins of the MCH, a minimum of fifteen 0603 form factor 0.1- F high frequency capacitors is required and must be placed within 150 mils of the MCH package. The fifteen capacitors should be evenly distributed along the MCH DDR system memory interface and must be placed perpendicular to the MCH with the power (2.5 V) side of the capacitors facing the MCH. The trace from the power end of the capacitor should be as wide as possible and it must connect to a 2.5-V power ball on the outer row of balls on the MCH. Each capacitor should have their 2.5-V via placed directly over and connected to a separate 2.5-V copper finger, and they should be as close to the capacitor pad as possible, within 25 mils. The ground end of the capacitors must connect to the ground flood and to the ground plane through a via. This via should be as close to the capacitor pad as possible, within 25 mils with as thick a trace as possible.

11.5.1.2. DDR SO-DIMM System Memory Decoupling Guidelines

Discontinuities in the DDR signal return paths will occur when the signals transition between the motherboard and the SO-DIMMs. To account for this ground to 2.5-V discontinuity, a minimum of nine 0603 form factor 0.1-µF high frequency bypass capacitors is required between the SO-DIMMs to help minimize any anticipated return path discontinuities that will be created. The bypass capacitors should be connected to 2.5 V and ground. The ground trace should connect to a via that transitions to the ground plane. The ground via should be placed as close to the ground pad as possible. The 2.5-V trace should connect to a via that transitions to the 2.5-V copper flood and it should connect to the closet 2.5-V SO-DIMM pin on either the first or second SO-DIMM connector, with a wide trace. The capacitors' 2.5-V traces should be distributed as evenly as possible amongst the two SO-DIMMs. Finally, the 2.5-V via should be placed as close to the 2.5-V pad as possible.

11.5.2. 2.5-V Power Delivery Guidelines

The 2.5-V power for the Intel 855PM MCH system memory interface and the DDR SO-DIMMs is delivered around the DDR command, control, and clock signals. Special attention must be paid to the 2.5-V copper flooding to ensure proper MCH and SO-DIMM power delivery. This 2.5-V flood must extend from the MCH 2.5-V power vias all the way to the 2.5-V DDR voltage regulator and its bulk capacitors, located at the end of the DDR channel beyond the second SO-DIMM connector. The 2.5-V DDR voltage regulator must connect to the 2.5-V flood with a minimum of six vias, and the SO-DIMM connector 2.5-V pins as well as the MCH 2.5-V power vias must connect to the 2.5-V copper flood. The copper flooding to the MCH should include at least seven fingers to allow for the routing of the DDR signals and for optimal MCH power delivery. The copper fingers must be kept as wide as possible in order to keep the loop inductance path from the 2.5-V voltage regulator to the MCH at a minimum. In the areas where the copper flooding necks down around the MCH make sure to keep these neck down lengths as short as possible. The 2.5-V copper flooding under the SO-DIMM connectors must encompass all the SO-DIMM 2.5-V pins and must be solid except for the small areas where the clocks are routed within the SO-DIMM pin field where they connect to their specified SO-DIMM pins.

Additionally, a small 2.5-V copper flood shape should be placed under the MCH to encompass and increase the copper flooding to the back row of the 2.5-V MCH pins. This flood must not be placed under any of the DDR signals. In order to maximize the copper flooding, these signals should be kept as short as possible in order to reduce the amount of serpentining needed in this area on the bottom layer. Also, a minimum of 12-mil isolation spacing should be maintained between the copper flooding and the DDR signals. Finally, the six, MCH 2.5-V high frequency decoupling capacitors located on the top signal layer should have their 2.5-V vias placed directly over and connected to a separate 2.5-V copper finger.

11.5.3. DDR Reference Voltage

Table 75 through Table 77 below have grouped the voltage and current specifications together for each the Intel 855PM MCH, memory, and termination voltages. There are seven voltages/power rails specified here for a DDR VR system. Although, there are only two unique voltage regulators for 2.5 V and 1.25 V nominal, each specific power rail described here has a unique specification. Described below are the memory components themselves first (the top three listed) and the MCH requirements (next row of 3) and finally the termination voltage and current requirements.

For convenience, tolerances are given in both % and Volts though validation should be done using the specification exactly as it is written. The voltage specs are clearly defined under “Specification Definition”. If this states a tolerance in terms of volts (e.g. VREF says ± 0.050 V) then that specific voltage tolerance should be used, not a percentage of the measured value. Likewise, percentages should be used where stated. If not stated then either way is fine.

Voltage specifications are defined as either “Absolute” or “Relative”. These are described in Table 74.

Table 74. Absolute vs. Relative Voltage Specification

Type of Specification	Description
Absolute Specification	This is a standard specification most commonly used. This means that the voltage limits are based on a fixed nominal voltage and have a symmetric ± tolerance added to determine the acceptable voltage range. For example, a VDD specification does not depend on any other voltage levels. It is simply 2.5 V ± 8%.
Relative Specification	This is a specification whose nominal value is not fixed but is relative to or is a function of another voltage. This means that the other voltage must be measured to know what the nominal value is and then the symmetrical ± tolerance added to that measured value. For example, a VREF specification depends on the actual value of VDD to determine VDD/2 and then tolerance ± 0.050 V from this calculated value.

From the Table 75, it can be seen that only the 2.5-V supply is a fixed, absolute specification, whereas all of the 1.25-V nominal supplies are relative to the 2.5-V supply directly or another 1.25-V supply which is then relative to the 2.5 V supply. Due to these 1.25-V relative specifications, it becomes very important that the 1.25 V supply can track the variations in the 2.5-V supply and respond according to the 2.5-V rail variations. This can be implemented as shown in the block diagram in Figure 144 where the 2.5-V output is divided in half and used to generate the 1.25 V reference into the 1.25-V VR controller design. In this manner, the 1.25-V VR will respond proportionally to variations in the 2.5-V supply, improving the voltage margin of the relative supply requirements and overall memory system stability.

Table 75. DDR SDRAM Memory Supply Voltage and Current Specification

Name	"VDD"	"VDDQ"	"VREF"	Description
Purpose	Core Supply Voltage, Static	I/O Supply Voltage, Static	I/O Reference Supply Voltage, Static	
Specification Definition	VDD	VDDQ	VREF = (Vdd/2) ± 0.050 V	((2.5 V ± 8%)/2) ± 0.050 V
Voltage Nominal (V)	*2.500*	2.500	1.250	
Tolerance (±%)	8.0%	8.0%	4.0%	
Tolerance (±V)	0.200	0.200	0.050	
Max Absolute Spec Value (V)	2.700	2.700	1.400	((2.5V + 8%)/2) + 0.050 V
Min Absolute Spec Value (V)	2.300	2.300	1.100	((2.5 V - 8%)/2) - 0.050 V
MAX RELATIVE SPEC (calculated from measured "Vdd" value)	NA	NA	(measured Vdd/2) + 0.050 V	
MIN RELATIVE SPEC (calculated from measured "Vdd" value)	NA	NA	(measured Vdd/2) - 0.050 V	
	I_{DD} (max)	**I_{DDQ} (max)**	**I_{REF} (max)**	
Absolute Maximum Current Requirements (A)	*5.000*	0.920	0.001 (1mA)	

Table 76. MCH System Memory Supply Voltage and Current Specification

Name	"VCCSM"	"SMVREF"	"VTT"= "SMRCOMP"	Description
Purpose	MCH DDR Supply Voltage (I/O), Static	MCH Reference Supply Voltage, Static	SMRCOMP Termination Supply Voltage, Static	
Definition	VCCSM	SMVREF = (VCCSM/2) ± 2%	VTT = ("Vref") ± 0.040 V	(((2.5 V ± 5%)/2) ± 0.050 V) ± 0.040)
Voltage Nominal (V)	2.500	1.250	1.250	
Tolerance (+/-%)	5.0%	2.0%	3.2%	
Tolerance (+/-V)	0.125	0.025	0.040	
Max Absolute Spec Value (V)	2.625	1.339	1.440	(((2.5 V + 5%)/2) + 0.050 V) + 0.040)
Min Absolute Spec Value (V)	2.375	1.164	1.060	(((2.5 V - 5%)/2) - 0.050 V) - 0.040)
Max Relative Spec (calculated from measured "VCCSM" value)	NA	(measured VCCSM/2) + 2%	(measured Vref) + 0.04 V	
Min Relative Spec (calculated from measured "VCCSM" value)	NA	(measured VCCSM/2) - 2%	(measured Vref) - 0.040 V	
	I_{VCCSM} (max)	I_{SMVREF} (max)	I_{TTRC} (max)	
Absolute Maximum Current Requirements (A)	1.900	0.00005 (50uA)	0.080 (80mA)	

Table 77. Termination Voltage and Current Specifications

Name	"VTT"	Description
Purpose	Termination Supply Voltage, Static	
Definition	Vtt = ("Vref") ± 0.040 V	(((2.5 V ± 8%)/2) ± 0.050 V) ± 0.040V
Voltage Nominal (V)	1.250	
Tolerance (+/-%)	3.2%	
Tolerance (+/-V)	0.040	
Max Absolute Spec Value (V)	1.440	(((2.5 V + 8%)/2) + 0.050 V) + 0.040V
Min Absolute Spec Value (V)	1.060	(((2.5 V - 8%)/2) – 0.050 V) – 0.040V
Max Relative Spec (calculated from measured "VCCSM" value)	(Measured Vref) + 0.040 V	
Min Relative Spec (calculated from measured "VCCSM" value)	(Measured Vref) - 0.040 V	
	I_{TT} (max)	
Absolute Maximum Current Requirements (A)	2.400	

11.5.3.1. SMVREF Design Recommendations

There are two SMVREF pins on the Intel 855PM MCH that are used to set the reference voltage level for the DDR system memory signals (SMVREF). The reference voltage must be supplied to both SMVREF pins. The voltage level that needs to be supplied to these pins must be equal to VCCSM/2. Note in Figure 144 that although SMVREF is generated from the 2.5-V supply, a buffer is used as well. A buffer has also been used to provide this reference to the system for the MCH and memory. This is the "VREF" signals to the DDR memory devices and the "SMVREF" signals (SMVREF[1:0]) to the MCH. The reference design utilizes this buffer to provide the necessary current to these devices, which a simple voltage divider is not capable of providing. The reference voltage supplied to SMVREF[1:0] has the tightest tolerance in the memory system of ± 2%. Using common 1% resistors consumes 1% of this 2% tolerance. This means SMVREF must now be controlled to a 1% tolerance (i.e. be able to divide VCCSM/2 within 1%). A simple resistor divider is not a voltage regulator and is most definitely not a current source. Any current drawn across the resistor divider used to generate this 1.25-V reference will cause a voltage drop across the top resistor, which distorts or biases this reference to a lower voltage.

The clarification below summarizes SMVREF.

Table 78. Intel 855PM MCH System Memory I/O

Name	VCCSM[1]	SMVREF
Purpose	MCH DDR Supply Voltage (I/O), Static	MCH Reference Supply Voltage, Static
Definition	VCCSM	SMVREF = ((VCCSM ± 5%) / 2) ± 2%
Voltage Nominal (V)	2.500	1.250
Tolerance (+/-%)	± 5%	± 2%
Tolerance (±V)	0.125	0.025
Vmax(V)	2.625	1.275
Vmin(V)	2.375	1.225
	I_{VCCSM} (max)	I_{SMVREF} (max)
Imax (A)	1.400	0.00005 (50 µA)

NOTE: Intel 855PM MCH VREF REQUIREMENTS: the MCH core is called "VCCSM" = +2.5 V ± 5%. SMVREF is ("VCCSM" ± 5%)/2 ± 2%. This means that whether the 2.5 V is 5% high or low, we need to be able to divide that voltage by 2 within 2% accuracy. This basically means to use 1% resistors, or better.

As shown in Table 78, the max current required by the MCH for the SMVREF input is 0.00005A (50 µA). Although the current requirements for the MCH's SMVREF inputs can be met with a resistor divider, it is strongly recommended that a buffer be used. The use of a buffer can be shared between the 1.25-V VREF inputs of both the MCH and the DDR memory devices and may be necessary to provide voltage regulation within 2%. Some sample calculations are shown in Table 79, it is not possible to maintain regulation within 2% using a resistive divider without using a resistor so small that the 2.5 V current requirement becomes prohibitive. Hence, a buffer is required due to the 10 mA current requirement of the MCH SMVREF.

Table 79. Effects of Varying Resistor Values in the Divider Circuit

Rdivider ( )	Leakage (A)	Rtop Vdroop (V)	I(2.5) total = 2.5 V/2R (A)
1	0.01	0.01	1.25
10	0.01	0.1	0.125
100	0.01	1	0.0125
1000	0.01	10	0.00125
10000	*0.01*	*100*	0.000125
100000	0.01	1000	1.25E-05
1000000	0.01	10000	1.25E-06

NOTES:

1. Rdivider: This is the resistor value selected to form the divider. Assumes both top and values are equal as required for divide by 2.
2. Leakage: This is the amount of leakage current which needs to sourced from the 2.5-V supply, across the divider's top resistor (Rtop) and out to the Intel 855PM MCH SMVREF input or the DDR VREF input. This current does not go across the bottom resistor.
3. Rtop Vdroop: This is the resulting voltage droop across Rtop as a result of the leakage current.
4. I(2.5) total = 2.5 V/2R. This is the total current through divider. This is calculated to consider the amount of current and power used as a DC current through the divider.

11.5.3.2. DDR VREF Requirements

Making the same calculations for the DDR loading, results to find the max VREF load of 1 mA, a divider is STILL NOT feasible here as the load of 1mA causes unacceptable drop across even a small Rs, which wastes power.

Table 80. DDR VREF Calculation

Name	Vdd	Vref
Purpose	Core Supply Voltage, Static	I/O Reference Supply Voltage, Static
	Vdd	*Vref = (Vdd +/- 8%) / 2*
VOLTAGE Nominal (V)	*2.500* (± 8%)	*1.250*
TOLERANCE (+/-V)	0.200	0.050
Vmax(V)	2.700	1.300
Vmin(V)	2.300	1.200
	I_{DD}	I_{REF}
Design Guide	*5.000*	*0.001*

NOTE: The DDR core is called "Vdd" =+2.5 V ± 8% (= ± 0.2 V). VREF is ("Vdd" ± 8%)/2 ± 50 mV. This means that whether the 2.5 V is 8% high or low, Platform designers need to be able to divide ***that voltage*** by 2 within an accuracy of 50 mV. This basically means to use 1% resistors, or better.

Table 81. Reference Distortion Due to Load Current

R( )	I(A)	Vdroop(V)	I(2.5) total=2.5 V/2R(A)
1	0.001	0.001	1.25
10	0.001	0.01	0.125
100	0.001	0.1	0.0125
1000	0.001	1	0.00125
10000	0.001	*10*	0.000125
100000	0.001	100	1.25E-05
1000000	0.001	1000	1.25E-06

NOTE: As for the MCH, a calculation can be made for the DDR. This shows that even with the slight load of 1 mA by the DDR it is still not feasible to use a simple resistor divider. Using the max leakage specs provided today and trying to maintain an error of less than 1% (12.5 mV) one needs to decrease the resistor values such that the current just to source the divider becomes unacceptable. A divider alone does not become an acceptable solution until current requirements are in the 100-µA range. Today, it is not possible to guarantee this type of current requirement for these applications. Therefore, the use of a buffer is highly recommended for these reference voltage requirements.

11.5.4. DDR SMRCOMP Resistive Compensation

The Intel 855PM MCH requires a system memory compensation resistor, SMRCOMP, to adjust buffer characteristics to specific board and operation environment characteristics. Refer to the *Intel® 855PM Memory Controller Hub (MCH) DDR 200/266 MHz Datasheet* for details on resistive compensation. Tie the SMRCOMP pin of the MCH to a 30.1- ± 1% pull-up resistor to the DDR termination voltage (1.25 V). Also, one 0603 0.1-µF decoupling capacitor to ground should be used. Place the resistor and capacitor within 1.0 inch of the MCH. The decoupling capacitor **must** be placed on the VTT powered side of the SMRCOMP resistor. The SMRCOMP signal and VTT trace should be routed with as wide a trace as possible. It should be a minimum of 12 mils wide and be isolated from other signals with a minimum of 10 mils spacing.

11.5.5. DDR VTT Termination

The recommended topology for DDR-SDRAM Data, Control, and Command signal groups requires that all these signals to be terminated to a 1.25-V source, VTT, at the end of the memory channel opposite the Intel 855PM MCH. It is recommended that VTT be generated from the same source as that used for VCCSM, and do not be shared with the MCH and DDR SMVREF. SMVREF has a much tighter tolerance and VTT can vary more easily depending on signal states. A solid 1.25-V termination island should be used to for this purpose. The VTT termination island should be placed on the top signal layer, just beyond the last SO-DIMM connector and must be at least 50 mils wide. The Data and Command signals should be terminated using one resistor per signal. Resistor packs and ± 5% tolerant resistors are acceptable for this application. Only signals from the same DDR signal group can share a resistor pack. See Section 11.5.1 and 11.7.1 for details on high frequency and bulk decoupling requirements.

11.5.6. DDR SMRCOMP, SMVREF, VTT 1.25-V Supply Disable in S3/Suspend

The DDR interface of the Intel 855PM MCH requires that several 1.25-V voltage sources be supplied to different parts the system memory interface for proper operation. In addition to providing the DDR VTT termination voltage at the end of the DDR bus for the Data, Control, and Command signal groups, 1.25-V supplies are also used to provide the reference voltages SMVREF of the MCH, the VREF of the DDR memory devices on the SO-DIMMs, and the termination voltage of the 30.1 ± 1% SMRCOMP resistor of the MCH.

SMRCOMP and VTT 1.25-V supplies can be disabled during the S3 suspend state to further save power on the platform. This is possible because the MCH does not require resistive compensation during suspend. However, the 2.5-V VCCSM power pins of the MCH, the **SMVREF** pin of the MCH, and the VDD power pins of the DDR memory devices are required to be on in S3 state.

Note: Some DDR memory devices require a valid reference voltage during suspend. It is the responsibility of the system designer to ensure that requirements of the DDR memory devices are met. Intel recommends following VREF design on Intel CRB.

11.5.6.1. VTT Rail Power Down Sequencing During Suspend

The VTT termination voltage for the DDR bus must not be turned off until all populated rows of memory have been placed into power down mode through the deassertion of the SCKE signals. Once all

rows of memory are powered off, the VTT termination voltage can be removed. During entry into suspend and during suspend, VTT must not glitch.

The voltage supplied to VREF (see Notes in 11.5.6), and SMRCOMP can be removed once all rows of memory are powered off and SCKE must not glitch during entry into suspend and during suspend.

Consult *JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification* for more details.

11.5.6.2. VTT Rail Power Up Sequencing During Resume

During resume from the S3 state, the reverse sequencing of the power rails and control signals must happen to ensure a smooth exit from suspend. The VTT termination voltage must be supplied and steady for a minimum of 10 ms before the system begins exit from suspend. VTT must not glitch during resume.

VREF (see NOTES in 11.5.6)), and SMRCOMP also need to be supplied and valid before the assertion of the SCKE signals. These reference voltages and resistive compensation are necessary in order for the Intel 855PM MCH and the memory devices to recognize the valid assertion of SCKE to a logic '1'. SCKE must not glitch during resume and must rise monotonically.

VTT and VREF to the SO-DIMMs and SMVREF and SMRCOMP to the MCH must all be up and stable for a minimum of 10 ms before the deassertion of PCIRST#.

Consult *JEDEC Standard, JESD79, Double Data Rate (DDR) SDRAM Specification* for more details.

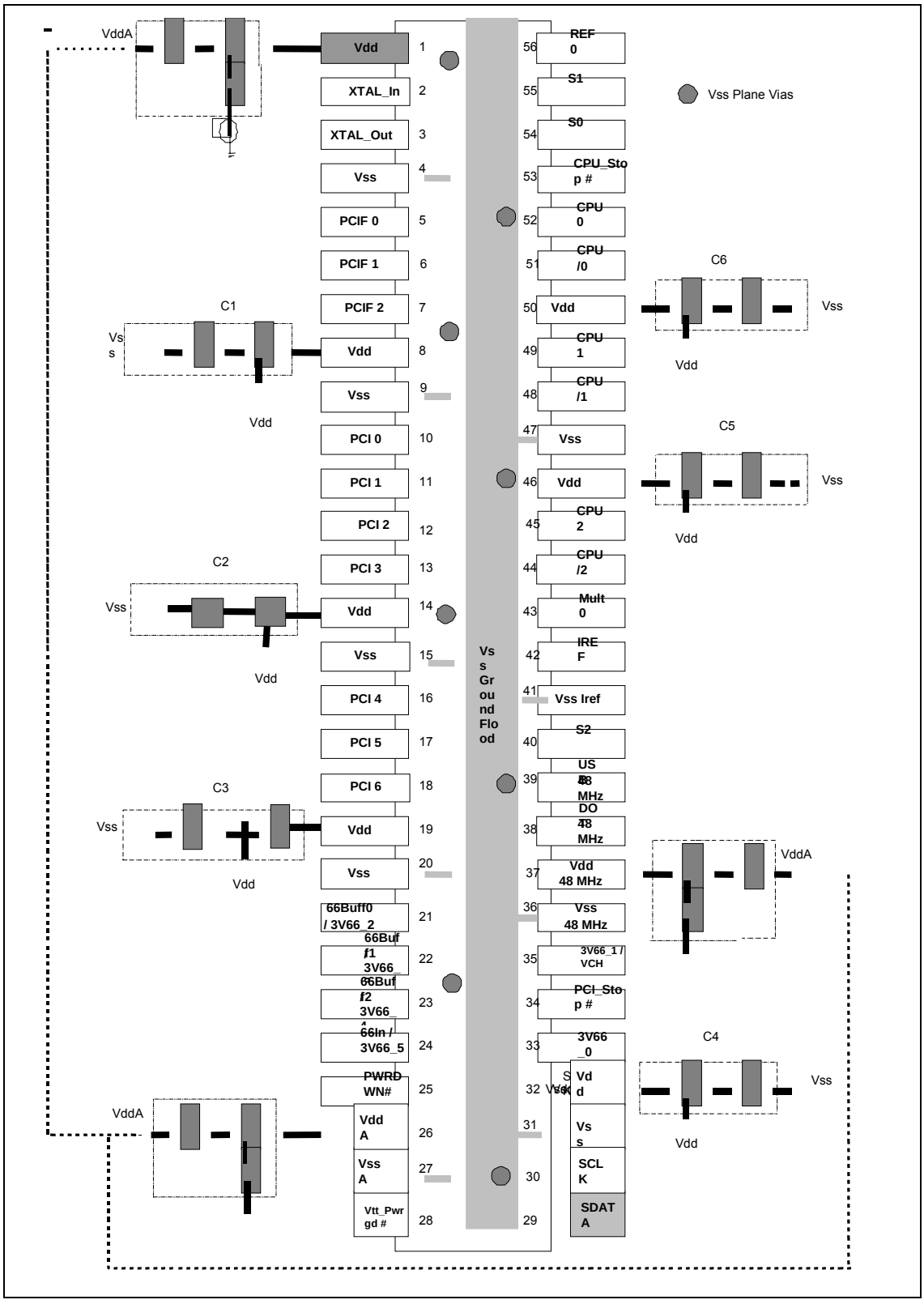
11.6. Clock Driver Power Delivery Guidelines

Special care must be taken to provide a quiet VDDA supply to the Ref VDD, VDDA, and the 48 MHz VDD. These VDDA signals are especially sensitive to switching noise induced by the other VDDs on the cock chip. They are also sensitive to switching noise generated elsewhere in the system such as the CPU VRM. The CLC pi-filter should be designed to provide the best reasonable isolation. It is recommended that a solid ground plane be underneath the clock chip on Layer 2 (assuming top trace is Layer 1). Intel also recommends that a ground flood be placed directly under the clock chip to provide a low impedance connection for the VSS pins.

For ALL power connections to planes, decoupling capacitors and vias, the MAXIMUM trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance. The decoupling capacitors should be connected as shown in the illustration taking care to connect the VDD pins directly to the VDD side of the capacitors. However, the VSS pins should not be connected directly to the VSS side of the capacitors. Instead they should be connected to the ground flood under the part that is via'ed to the ground plane. This is done to avoid VDD glitches propagating out, getting coupled through the decoupling capacitors to the VSS pins. This method has been shown to provide the best clock performance.

The ground flood should be via'ed through to the ground plane with no less than 12-16 vias under the part. It should be well connected. For all power connections, heavy duty and/or dual vias should be used. It is imperative that the standard signal vias and small traces not be used for connecting decoupling capacitors and ground floods to the power and ground planes. VDDA should be generated by using a CLC pi-filter. This VDDA should be connected to the VDD side of the three capacitors that require it using a hefty trace on the top layer. This trace should be routed from the CLC pi-filter using a star topology.

Figure 145. Decoupling Capacitors Placement and Connectivity



11.7. Decoupling Recommendations

Intel recommends proper design and layout of the system board bulk and high frequency decoupling capacitor solution to meet the transient tolerances for each component. To meet the component transient load steps, it is necessary to properly place bulk and high frequency capacitors close to the component power and ground pins.

11.7.1. Processor Decoupling Guidelines

See Section 5.9.2 for details on recommended $V_{CC\text{-}CORE}$ decoupling solutions.

11.7.2. Intel 855PM MCH Decoupling Guidelines

Table 82. Decoupling Requirements for the Intel 855PM MCH

Pin	Decoupling Requirements	Decoupling Type (Pin type)	Decoupling Placement
VCC_MCH	See Section 5.9.5	Decoupling Cap: See Table 22	Place near balls: See Figure 69
VCC1_5	See Section 7.3.4	Decoupling Cap: See Section 7.3.4	Place near balls: See Section 7.3.4
VCC1_8	(2) 0.1 µF	Decoupling Cap: See Section 8.5	Place near balls: See Section 8.5
VCCGA, VCCHA	(2) 10 µF (2) 10 nF	Decoupling Cap: See Section 5.2	Place near balls: T13, T17; See Section 5.2
VCCSM	See Section 11.5.1.1	Decoupling Cap: See Section 11.5.1.1	Place near balls: See Section 11.5.1
V_{CCP}	See Section 5.9.4	Decoupling Cap: See Table 21	Place near balls: See Figure 64 & Figure 66

11.7.3. Intel 82801DBM ICH4-M Decoupling Guidelines

The Intel 82801DBM ICH4-M is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. Intel recommends that the developer use the amount of decoupling capacitors specified in

Table 83 to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible (100 mils nominal). Rotate caps that set over power planes so that the loop inductance is minimized (see Figure 146). The basic theory for minimizing loop inductance is to consider which voltage is on Layer 2 (power or ground) and spin the decoupling cap with the opposite voltage towards the BGA (Ball Grid Array). This greatly minimizes the total loop inductance. Intel recommends that for prototype board designs, the designer should include pads for extra power plane decoupling caps.

Figure 146. Minimized Loop Inductance Example

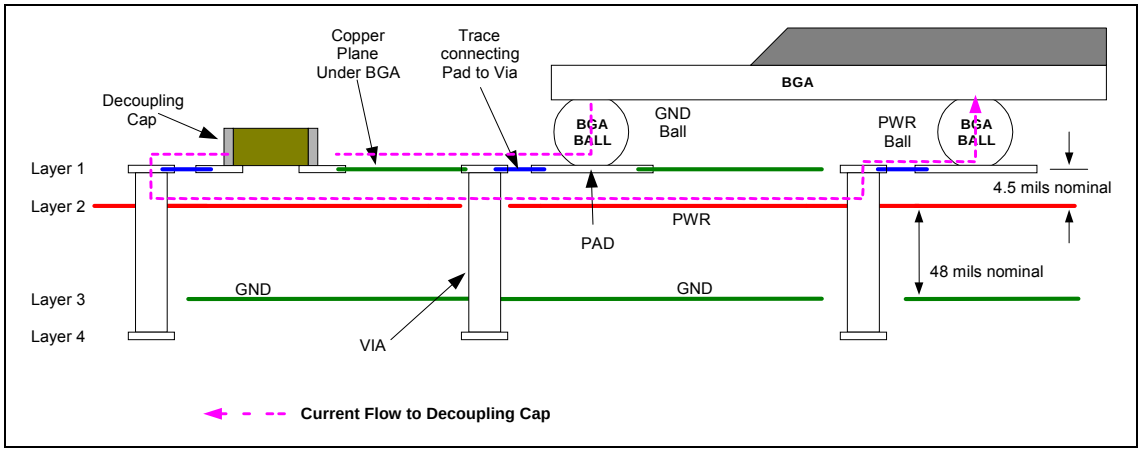


Table 83. Decoupling Requirements for the Intel 82801DBM ICH4-M

Pin	Decoupling Requirements	Decoupling Type (Pin type)	Decoupling Placement
VCC3_3	(6) 0.1 µF	Decoupling Cap (Vss)	Place near balls: A4, A1, H1, T1, AC10, and AC18
VCCSUS3_3	(2) 0.1 µF	Decoupling Cap (Vss)	Place near balls: A22 and AC5
VCCLAN3_3	(2) 0.1 µF	Decoupling Cap (Vss)	Place near balls: E9 and F9
V_CPU_IO	(1) 0.1 µF	Decoupling Cap (Vcc)	Place near ball: AA23
VCC1_5	(2) 0.1 µF	Decoupling Cap (Vss)	Place near balls: K23 and C23
VCCSUS1_5	(2) 0.1 µF	Decoupling Cap (Vss)	Place near balls: A16 and AC1
VCCLAN1_5	(2) 0.1 µF	Decoupling Cap (Vss)	Place near balls: F6 and F7
V5REF	(1) 0.1 µF	Decoupling Cap (Vcc)	Place near ball: E7
V5REF_SUS	(1) 0.1 µF	Decoupling Cap (Vss)	Place near ball: A16
VCCRTC	(1) 0.1 µF	Decoupling Cap (Vcc)	Place near ball: AB5
VCCHI	(2) 0.1 µF	Decoupling Cap (Vss)	Place near balls: T23 and N23
VCCPLL	(1) 0.1 µF (1) 0.01 µF	Decoupling Cap (Vcc)	Place near ball: C22

NOTES:
1. Capacitors should be placed less than 100 mils from the package.
2. ICH4-M balls listed in the “Decoupling Placement” guidelines column may not necessarily correlate to a VCC power ball and may include signal balls from different interfaces.

11.7.4. DDR VTT High Frequency and Bulk Decoupling

The VTT Island must be decoupled using high-speed bypass capacitors, one 0603, 0.1-µF capacitor per two DDR signals. These decoupling capacitors connect directly to the VTT island and to ground, and must be spread out across the termination island so that all the parallel termination resistors are near high frequency capacitors. The capacitor ground via should be as close to the capacitor pad as possible, within 25 mils with as thick a trace as possible. The ground end of the capacitors must connect to the ground flood on Layer 2 and to the ground plane on Layer 3 through a via. Finally, the distance from any DDR termination resistor pin to a VTT capacitor pin must not exceed more then 100 mils.

11.7.5. AGP Decoupling

See Section 7.3.4 for details.

11.7.6. Hub Interface Decoupling

See Section 8.5 for details.

11.7.7. FWH Decoupling

A 0.1-µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7-µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

11.7.8. General LAN Decoupling

All VCC pins should be connected to the same power supply.

All VSS pins should be connected to the same ground plane.

Four to six decoupling capacitors, including two 4.7-µF capacitors are recommended

Place decoupling as close as possible to power pins.

11.7.9. CK-408 Clock Driver Decoupling

The decoupling requirements for a CK-408 compliant clock synthesizer are often dependent on vendor design and implementation. The appropriate decoupling guidelines in terms of type, quantity, form factor, and usage of decoupling capacitors should come from the respective clock synthesizer component vendor.

If clock synthesizer specific decoupling guidelines from a vendor are not available, the general guidelines below can be used.

The decoupling caps should be connected taking care to connect the VDD pins directly to the VDD side of the caps. However, the VSS pins should not be connected directly to the VSS side of the caps. Instead, they should be connected to the ground flood under the part that is via'ed to the ground plane. This is done to avoid VDD glitches propagating out and getting coupled through the decoupling caps to the VSS pins. This method has been shown to provide the best clock performance.

The decoupling requirements for a CK-408 compliant clock synthesizer are as follows:

One 10-µF bulk decoupling cap in a 1206 package placed close to the VDD generation circuitry.

Six 0.1-µF high frequency decoupling caps in a 0603 package placed close to the VDD pins on the CK-408.

Three 0.1-µF high frequency decoupling caps in a 0603 package placed close to the VDDA pins on the CK-408.

One 10-µF bulk decoupling cap in a 1206 package placed close to the VDDA generation circuitry

11.8. Intel 855PM MCH Power Consumption Numbers

The following table shows the Intel 855PM MCH power consumption estimates.

Table 84. Intel 855PM MCH Power Consumption Estimates

Power Plane	Maximum Power Consumption				
	S0	S1M	S3	S4/S5	G3
V_{CCP} (1.05 V)	2.4 A	36 mA	N/A	N/A	N/A
V_{CC-MCH} (1.2 V Core)	1.65 A	66 mA	N/A	N/A	N/A
VCC1_5 (AGP)	370 mA	4 mA	N/A	N/A	N/A
VCC1_8 (HI 1.0)	200 mA	43 mA	N/A	N/A	N/A
VCCA (PLL 1.8 V)	N/A	N/A	N/A	N/A	N/A
VCCSM (DDR 2.5 V)	1.9 A	< 1 mA	< 1 mA	N/A	N/A
SMVREF	50 A	N/A	0 mA	N/A	N/A
SMRCOMP	80 mA	N/A	0 mA	N/A	N/A

11.9. Intel 82801DBM ICH4-M Power Consumption Numbers

The following table shows the Intel 82801DBM ICH4-M power consumption estimates.

Table 85. Intel 82801DBM ICH4-M Power Consumption Estimates

Power Plane	Maximum Power Consumption				
	S0	S1M	S3	S4/S5	G3
Vcc1_5 Core	550 mA	94 mA	N/A	N/A	N/A
Vcc3_3 I/O	528 mA	1 mA	N/A	N/A	N/A
VccLAN1_5 (S0/D0[2])	15.5 mA	N/A	N/A	N/A	N/A
VccLAN1_5 (D3[2])	13 mA	13 mA	4 mA	4 mA	N/A
VccLAN3_3 (S0/D0[2])	9.2 mA	N/A	N/A	N/A	N/A
VccLAN3_3 (D3[2])	2.1 mA	2.1 mA	2.1 mA	2.1 mA	N/A
VccSUS1_5[1]	67.5 mA	35.7 mA	8.4 mA	8.4 mA	N/A
VccSUS3_3[1]	165 mA	0.3 mA	0.09 mA	0.08 mA	N/A
V_{CCRTC}	N/A	N/A	N/A	N/A	5 A
$V_{\_CPU\_IO}$	2.5 mA	2.5 mA	N/A	N/A	N/A
VccHI (HI 1.0 – 1.8 V)	132 mA	132 mA	N/A	0 mA	N/A
V5REF	10 µA	10 µA	N/A	N/A	N/A
V5REF_SUS	10 µA	10 µA	10 µA	10 µA	N/A

NOTES:
1. This number assumes six High-speed USB ports transmitting and receiving.
2. D0 LAN state collected under 100 Mbps stress testing. D3 LAN state assumes connection to a 100-Mbit network.

11.10. Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus. The thermal design power number for the Intel 855PM MCH and Intel 82801DBM ICH4-M are listed below.

Table 86. Intel 855PM MCH Component Thermal Design Power

Intel 855PM MCH - Thermal Design Power Consumption Dissipation (estimated)	
Intel 855PM MCH	1.8 W (maximum)

Table 87. Intel 82801DBM ICH4-M Component Thermal Design Power

Intel 82801DBM ICH4-M - Thermal Design Power Consumption Dissipation (estimated)	
Intel 82801DBM ICH4-M	2.0 W (maximum)

12. Intel® PRO/Wireless 2100 and Bluetooth Design Requirements

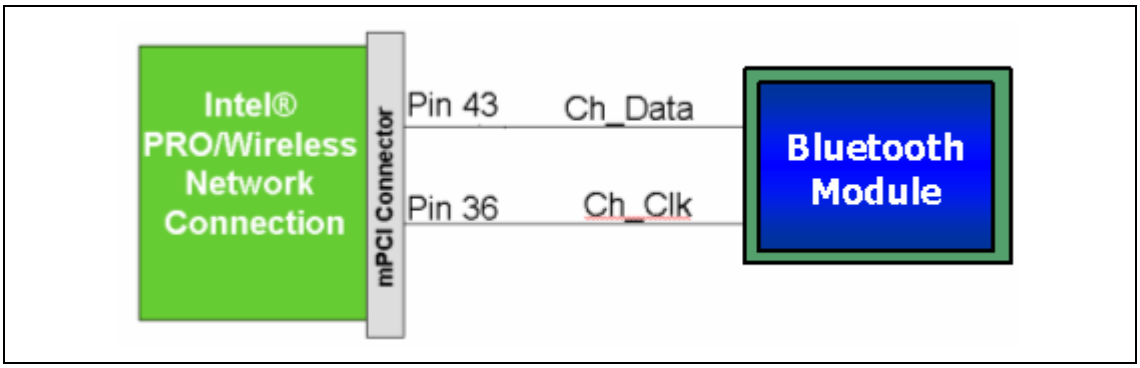
This section describes the design requirements needed to interface an Intel 802.11 wireless LAN device (Intel® PRO/Wireless 2100 family) to a Bluetooth module of choice that supports Intel's Wireless Coexistence System (WCS) specification. Other requirements for supporting Intel PRO/Wireless and Bluetooth features are also addressed. The following topics are covered in this section:

1. PCB interface requirements
2. DC power requirements for Bluetooth
3. Selective Suspend support requirements
4. Wake on Bluetooth support requirements
5. RF Disable support requirements for Intel PRO/Wireless and Bluetooth Devices

12.1. PCB Interface Requirements

Two PCB traces shall be used to carry channel number and clock signals between Bluetooth and Intel PRO/Wireless 2100. Although these traces do not need to match any length, width or impedance constraints a typical width of 5 mils and spacing of 5 mils is recommended. Pin # 43 of the mPCI connector needs to be routed to the Channel_Data signal of the Bluetooth module. Pin # 36 of the mPCI connector needs to be routed to the Channel_Clock signal of the Bluetooth module. The Channel_Data and Channel_Clock pins on the Bluetooth module are vendor specific. Please refer to the corresponding Bluetooth module vendor for this information. The traces between Intel PRO/Wireless 2100 and Bluetooth are a point-to-point connection and do not require any intervening components.

Figure 147. Recommended Topology for Coexistence Traces



12.2. DC Power Requirements for Bluetooth

Voltage levels to power Bluetooth modules are vendor specific. Typical voltage requirement to power Bluetooth module is 3.3Vwith 2% tolerance. This source may be derived from any power rail available on the platform capable of providing the Bluetooth module power requirements. Please note

that if implementing Wake on Bluetooth or Selective Suspend an appropriate power rail should be selected. See Section 12.3 and section 12.4 for details. The Fishhook reference board provides multiple power delivery solutions for the Bluetooth module including a 3.3-V source from the CRB and a 3.3-V source derived from the 5-V USB power rail.

12.3. Selective Suspend Support

USB based Bluetooth modules that plan to support the Microsoft Selective Suspend feature must be self-powered. Selective Suspend allows the processor to enter the C3/C4 state with the presence of a USB based Bluetooth module. The USB power rail is not a sufficient source for a self-powered module. The power rail must be always on in system states S0, S1 and S2 for a self-powered device. Generally it is recommended for all internal USB devices (in this case the Bluetooth module) to self-powered for best power efficiency and to be capable of waking up the system. For more information refer to:

"Power saving of using USB selective Suspend Support" published in
http://www.intel.com/design/mobile/platform/downloads/Power_Saving_USB_Selective_Suspend.pdf

12.4. Wake on Bluetooth Requirements

WoBT (Wake on Bluetooth) provides a method for the Bluetooth module to wake the system upon Bluetooth device activity. This functionality is similar to Wake on LAN. Support for WoBT requires the device to be self-powered and the power rail to be always on in system states S0-S4. The same signal used for WOL (Wake on LAN) is planned for use by the WoBT signal. This is a point to point interface and does not require any interface logic. There are no trace length or spacing requirements for this low speed signal.

12.5. RF Disable Support Requirements for Intel PRO/Wireless 2100 and Bluetooth Devices

The RF Disable interface to the Intel PRO/Wireless 2100 module occurs via pin 13 of the mini-PCI connector. This interface provides support to disable the Intel PRO/Wireless 2100 radio through methods including, but not limited to, an external mechanical switch or button on the notebook or through an embedded controller. This is an active low signal which provides the ability to disable the RF portions of Intel PRO/Wireless 2100. The Intel PRO/Wireless 2100 radio remains disabled until RF_KILL# is unasserted.

13. Reserved, NC, and Test Signals

The Intel Pentium M processor, Intel Celeron M and Intel 855PM MCH may have signals listed as "RSVD", "NC", or other name whose functionality is Intel reserved. The following section contains recommendations on how these Intel reserved signals on the processor or MCH should be handled.

13.1. Intel Pentium M Processor and Intel Celeron M RSVD Signals

The Intel Pentium M processor / Intel Celeron M processor has a total of three TEST and seven RSVD signals that are Intel reserved in the pin-map. All other RSVD signals are to be left unconnected but should have access to open routing channels for possible future use.

The location of the Intel reserved signals in the Intel Pentium M processor / Intel Celeron M processor pin-map is listed in Table 88.

Table 88. Processor RSVD and TEST Signal Pin-Map Locations

Signal Name	Ball Name
RSVD	AF7
RSVD	B2
RSVD	C3
RSVD	C14
RSVD	E26
RSVD	G1
RSVD	AC1
TEST1	C5
TEST2	F23
TEST3	C16

13.2. Intel 855PM MCH RSVD Signals

The Intel 855PM MCH has a total of nine RSVD and two NC signals that are Intel reserved in the pin-map. The recommendation is to provide test points for all RSVD signals for possible future use. All NC signals should be left as no connects. The 1-k resistor should not be populated by default. The location of the Intel reserved signals in the MCH pin-map is listed in Table 89.

The MCH's TESTIN# signal is used manufacturing and board level test purposes only. TESTIN# is an input signal and has an integrated pull-up. For normal operation, it can be left unconnected.

Table 89. MCH RSVD and NC Signal Pin-Map Locations

Signal Name	Ball Name
NC	AD26
NC	AD27
RSVD	G2
RSVD	G3
RSVD	G9
RSVD	G10
RSVD	G16
RSVD	G22
RSVD	H3
RSVD	H7
RSVD	H27
TESTIN#	H26

14. Platform Design Checklist

The following checklist provides design recommendations and guidance for the Intel Pentium M processor / Intel Celeron M processor systems with the Intel 855PM chipset platform. It should be used to ensure that design recommendations in this design guide have been followed **prior** to schematic reviews. However, this is not a complete list and does not contain detailed layout information.

Note: Unless otherwise specified the default tolerance on resistors is ± 5%**.** Also note that the (S) reference after power rails such as VCC3_3 (S) indicates a switched rail þu one that is powered off during S3-S5.

14.1. General Information

The following section should be filled out by the OEM or Intel Field Representative.

Processor (Intel Pentium M Processor)	
Processor Min Frequency targeted for this platform	
Processor/Max Frequency targeted for this platform	
Voltage Regulator Solution	Part#/Vendor: Target ICC(max):
Internal Graphics Used?	
External Graphics AGP Graphics	Part#/Vendor:
Target Thermal Envelope (Watts)	
LOM or mini-PCI LAN?	
Target FCS (First Customer Ship) Date	

14.2. Customer Implementation

Fill in Schematic Name of Voltage Rails on Mark Boxes of when Rails are powered on.

Name of Rail	On S0-S1	On S3	On S4	On S5

14.3. Design Checklist Implementation

The voltage rail designations in this design checklist were intended to be as general as possible. The following table describes the equivalent voltage rails in the Intel CRB schematics attached in this design guide.

Checklist Rail	Intel CRB Rail	On S0-S1	On S3	On S4	On S5
Vcc1_2[Vcc_mch]	V1.2S_MCH	X			
Vcc1_25[DDR_Vtt][4]	V1.25S	X			
Vcc1_5	V1.5S, 1.5S_AGP	X			
VccSus1_5	V1.5, V1.5ALWAYS	X	X	1,3	1,3
V1_5ALWAYS	See VccSus1_5	X	X	X	X
Vcc1_8	V1-8S	X			
VccSus2_5	V2.5_MCH, V2.5DDR	X	X		
Vcc3_3	V3S, V3.3S_ICH	X			
VccSus3_3	V3, V3ALWAYS	X	X	1, 3	1, 3
VccSus3_3LAN	V3.3_LAN	X	2	2	2
V3ALWAYS	See VccSus3_3	X	X	X	X
Vcc5	V5S	X			
VccSus5	V5	X	X	1	1
Vcc12	V12S	X			
VccRTC	VccRTC	X	X	X	X
VCCP[5]	VCCP	X			
VCC[Vcc_Core]	Vcc_core	X			

NOTES:

1. A rail powered in Sx is dependent on implementation.
2. A VccLANx rail powered on in Sx is dependent on implementation.
3. A VxALWAYS rail can be the SUS rail depending on implementation.
4. Vcc1_25 is the 1.25V VTT termination voltage for DDR. This power rail can be OFF during S3.
5. VCCP is the 1.05V FSB signaling level of the CPU, MCH, and ICH4-M (legacy signal). Also used for the ITP700 FLEX debug port, if used.

14.4. Intel Pentium M Processor and Intel Celeron M Processor

14.4.1. Resistor Recommendations

Intel Pentium M/Intel Celeron M Processor – Resistor Recommendations[1]					
Pin Name	**System Pull up/Pull down**		**Series Termination Resistor (**	**Notes**	✓
A20M#, IGNNE#, LINT0/INTR, LINT1/NMI, SLP#, SMI#, STPCLK#				Point-to-point connection to ICH4-M.	
BPM[3:0]#				**If ITP700FLEX Is Used:** See Section 14.4.2.1. **If ITP Interposer Is Used:** Leave the signals as NC (No Connect). **If ITP Not Supported:** Leave the signals as NC (No Connect).	
COMP[0], COMP[2]	Pull down to GND	27.4 ± 1%		Resistor placed within 0.5" of CPU pin via a Zo = 27.4 trace. Trace should be at least 25 mils (>50 mils preferred) away from any other toggling signal. See section 4.1.8 placement and routing guidelines.	
COMP[1], COMP[3]	Pull down to GND	54.9 ± 1%		Resistor placed within 0.5" of CPU pin via a Zo = 55 trace. Trace should be at least 25 mils (>50 mils preferred) away from any other toggling signal. See section 4.1.8 placement and routing guidelines.	
DBR#				**If ITP700FLEX Is Used**: Leave this signal as NC (No Connect). **If ITP Interposer is Used:** See Section 14.4.2.2 **If ITP Not Supported:** Leave this signal as NC (No Connect).	
DPSLP#				Daisy chain topology from ICH4-M to CPU to MCH. DPSLP# should fork at the pin of the CPU. T-split routing should not be used. See section 4.1.4.1.5 for more details.	
FERR#	Pull up to VCCP	56	56	FERR# is a 1.05V tolerant signal and voltage translation logic may be required. Parallel termination resistor should be placed near the ICH4-M or system receiver. Series resistor should	

Intel Pentium M/Intel Celeron M Processor – Resistor Recommendations[1]					
Pin Name	**System Pull up/Pull down**		**Series Termination Resistor (**	**Notes**	✓
				be placed between the receiver and termination resistor. Series resistor should have no stub when connecting to the FERR# trace from the CPU. See Section 4.1.4.1.2 for more details.	
GTLREF (pin AD26)		1 k ± 1% (top) 2 k ± 1% (bottom)		Voltage divider placed within 0.5" of CPU pin via a Zo = 55 trace. No decoupling should be placed on the pin. See Figure 148 and section 4.1.7 for more details.	
IERR#	Pull up to VCCP	56	56	IERR# is a 1.05 V tolerant signal and voltage translation logic may be required. **If IERR# Is NOT Used**: 56 pull-up to VCCP is required. **If IERR# Is Used**: Parallel termination resistor should be placed near the system receiver. Series resistor should be placed between the receiver and termination resistor. Series resistor should have no stub when connecting to IERR# trace from the CPU. See Section 4.1.4.1.1 for more details.	
INIT#	See Notes		R1 = 1.3 k R2 = 330 Rs = 330	INIT# is T-split from the ICH4-M to the CPU and FWH. A voltage translation circuit is required for the use with the Intel 82802AB/AC FWH (see Figure 149). The voltage translation circuit shown assumes the receiver uses a 3.3 V I/O supply voltage. For all other firmware devices, proper voltage translation should be ensured. See section 4.1.4.1.7 for more details.	
PRDY#, PREQ#				**If ITP700FLEX Is Used:** See Section 14.4.2.1. **If ITP Interposer Is Used:** Leave the signals as NC (No Connect). **If ITP Not Supported:** Leave the signals as NC (No Connect).	
PROCHOT#	Pull up to VCCP	56		PROCHOT# is a 1.05 V tolerant signal and voltage translation logic may be required. The ICH4-M's THRM# signal should not be driven by PROCHOT#. **If Voltage Translation Is Not Required**:	

Intel Pentium M/Intel Celeron M Processor – Resistor Recommendations[1]					
Pin Name	**System Pull up/Pull down**		**Series Termination Resistor (**	**Notes**	✓
				Point-to-point connection to system receiver. **If Voltage Translation Is Required**: Driver isolation resistor should be placed at the beginning of the T-split to the system receiver. See Figure 151 and Section 4.1.4.1.3 for details.	
PWRGOOD	Pull up to VCCP	330		Point-to-point connection to ICH4-M. Parallel termination resistor routing should fork at the pin of the CPU and T-split routing should not be used.	
RESET#	Pull up to VCCP (ITP700FLEX only)	54.9 ± 1% (ITP700FLEX only)	22.6 ± 1% (ITP700FLEX only)	**If ITP700FLEX Is Not Used**: Point-to-point connection to MCH. **If ITP700FLEX Is Used**: RESET# forks out from the MCH to the CPU and ITP700FLEX. 1st branch connects the MCH point-to-point to the CPU. 2nd branch needs to be pulled up to VCCP through a 54.9 ± 1% resistor placed close to the ITP700FLEX. The pull up resistor should be placed within 12" of the MCH. 2nd branch should connect to the ITP700FLEX through a 22.6 ± 1% series dampening resistor placed next to the 54.9 ± 1% pull up. Series resistor should also be placed within 0.5" of the ITP700FLEX. See Section 4.1.5 for more details	
RSVD (pin AC1, E26, G1)				These 3 signals were previously named GTLREF[3:1]. These 3 signals are currently classified as RSVD signals. Leave the signals as NC (No Connect).	
RSVD (Pin AF7, B2, C3, C14)				Design Options: 1. Route to test point (recommended). OR 2. Leave unconnected with access to open routing channels for possible future use.	
TCK				**If ITP700FLEX Is Used:** See Section 14.4.2.1. **If ITP Interposer Is Used:** See Section 14.4.2.2.	

Intel Pentium M/Intel Celeron M Processor – Resistor Recommendations[1]					
Pin Name	**System Pull up/Pull down**		**Series Termination Resistor (**	**Notes**	✓
				If ITP Not Supported: See Section 14.4.2.3.	
TDI				**If ITP700FLEX Is Used:** See Section 14.4.2.1. **If ITP Interposer Is Used:** See Section 14.4.2.2. **If ITP Not Supported:** See Section 14.4.2.3.	
TDO				**If ITP700FLEX Is Used:** See Section 14.4.2.1. **If ITP Interposer Is Used:** See Section 14.4.2.2. **If ITP Not Supported:** See Section 14.4.2.3.	
TEST[3:1] (pin C16, F23, C5)	Pull down to GND	1 k (Default: No Stuff)		Stuffing option for 1K pull down to GND should be provided for testing purposes. For normal operation, resistor should be No Stuff.	
THERMTRIP#	Pull up to VCCP	56	5 6	THERMTRIP# is a 1.05 V tolerant signal and voltage translation logic may be required. Parallel termination resistor should be placed near the ICH4-M or system receiver. Series resistor should be placed between the receiver and termination resistor. Series resistor should have no stub when connecting to the THERMTRIP# trace from the CPU. See section 4.1.4.1.2 for more details.	
TMS				**If ITP700FLEX Is Used:** See Section 14.4.2.1. **If ITP Interposer Is Used:** See Section 14.4.2.2. **If ITP Not Supported:** See Section 14.4.2.3.	
TRST#				**If ITP700FLEX Is Used:** See Section 14.4.2.1. **If ITP Interposer Is Used:** See Section 14.4.2.2. **If ITP Not Supported:** See Section 14.4.2.3.	
Intel Pentium M/Intel Celeron M Processor – Power Signals					

Intel Pentium M/Intel Celeron M Processor – Resistor Recommendations[1]					
Pin Name	**System Pull up/Pull down**		**Series Termination Resistor (**	**Notes**	✓
VCC[71:0]	Tie to VCC[Vcc_Core]			72 VCC pins	
VCCA[3:0]	Tie to Vcc1_8			See layout example in Section 5.3. Also see Section 14.4.4 for decoupling.	
VCCP[26:0]	Tie to VCCP			27 VCCP pins	
VCCSENSE	Pull down to GND	54.9 ± 1% (Default: No Stuff)		Stuffing option for 54.9 ± 1% pull down to GND should be provided for testing purposes. For normal operation, resistor should be No Stuff. Also, a test point for a differential probe ground should be placed between the two termination resistors of VCCSENSE and VSSSENSE.	
Intel Pentium M/Intel Celeron M Processor – GND Signals					
VSS[191:0]	Tie to GND			192 VSS pins	
VSSSENSE	Pull down to GND	54.9 ± 1% (Default: No Stuff)		Stuffing option for 54.9 ± 1% pull down to GND should be provided for testing purposes. For normal operation, resistor should be No Stuff. Also, a test point for a differential probe ground should be placed between the two termination resistors of VCCSENSE and VSSSENSE.	

NOTE: Default tolerance for resistors is ± 5% unless otherwise specified.

Figure 148. Processor GTLREF Voltage Divider Network

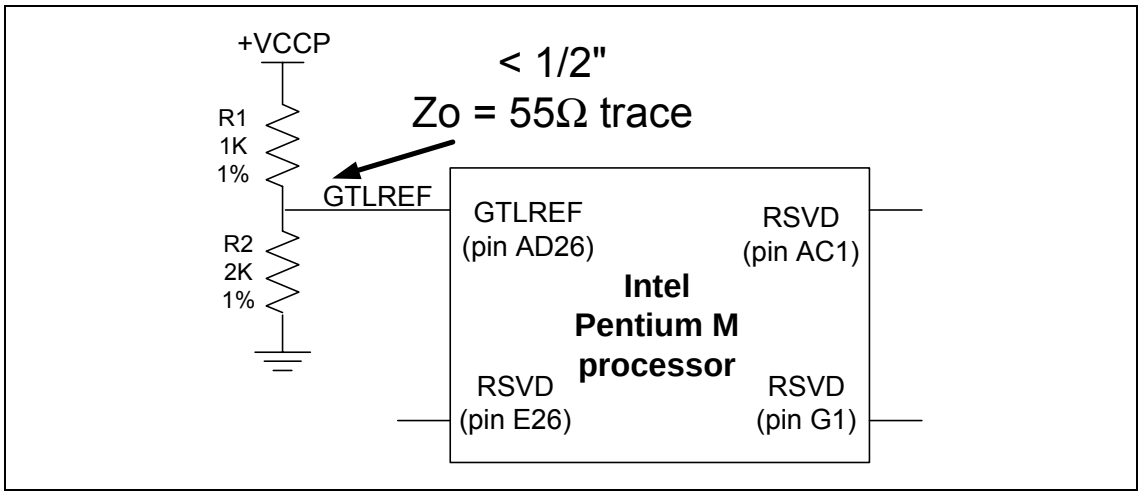


Figure 149. Routing Illustration for INIT#

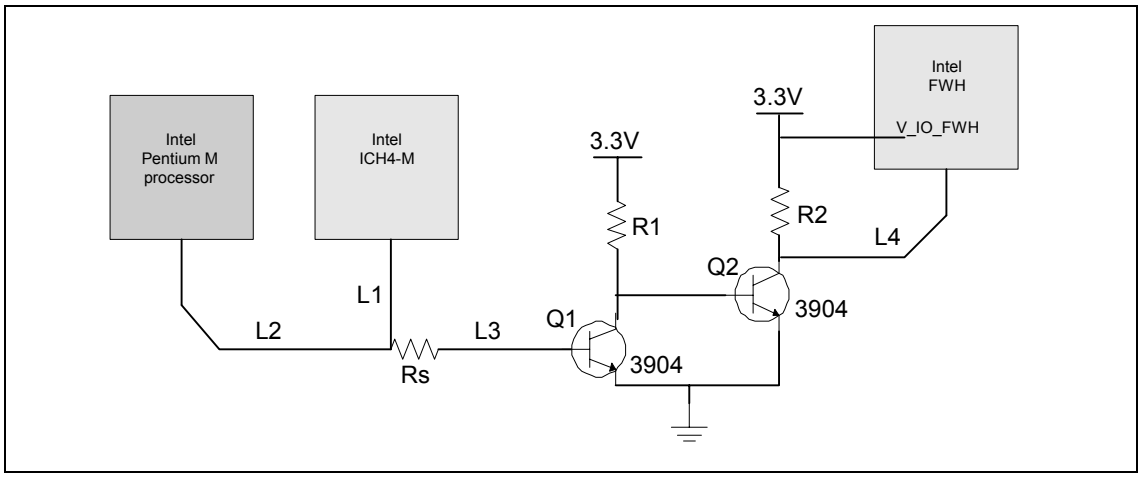


Figure 150. Voltage Translation Circuit

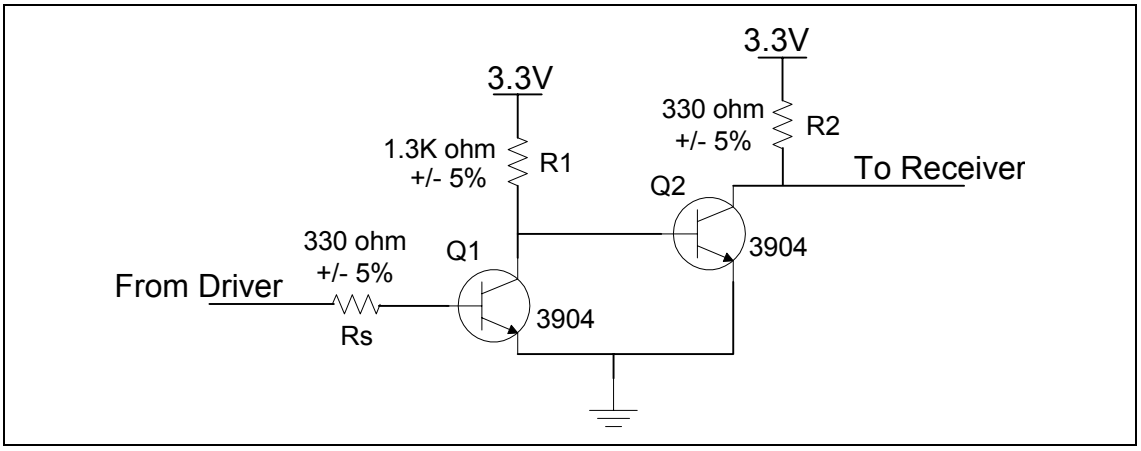
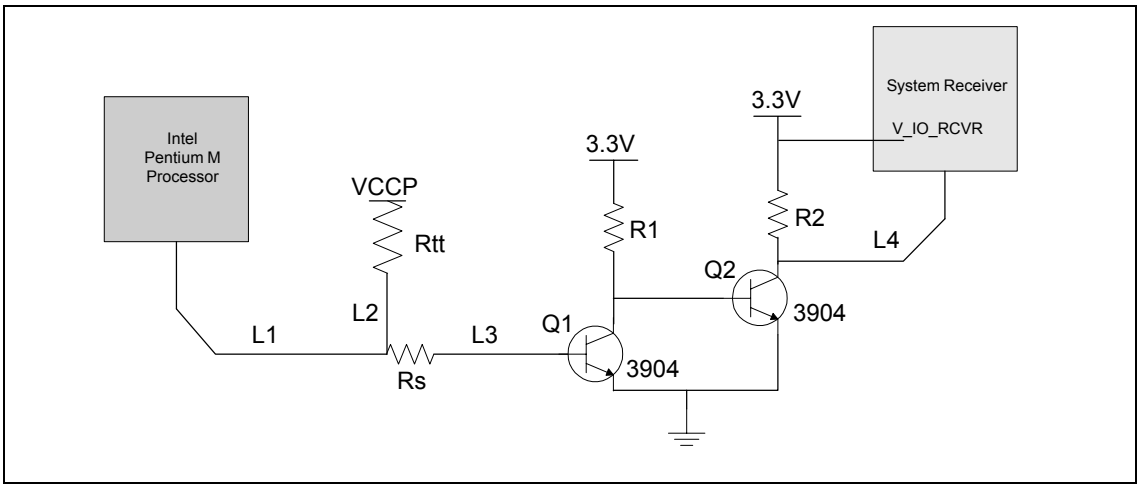


Figure 151. Routing Illustration for PROCHOT#



14.4.2. In Target Probe (ITP)

14.4.2.1. ITP700FLEX Connector [1, 2]

ITP700FLEX Debug Port Connector – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Termination Resistor (**	**Notes**	✓
BPM[5:0]#				**ITP700FLEX supported Validation Systems**: Point-to-point connection to CPU via a Zo = 55 trace. ITP700FLEX to CPU BPM[3:0]# BPM[3:0]# BPM[4]# PRDY# BPM[5]# PREQ# **ITP700FLEX supported Production Systems**: Leave the signals as NC (No Connect).	
DBA#	Pull up to target VCC	150 - 240		DBA# is an optional signal that may be implemented when the ITP700FLEX is used. **ITP700FLEX supported Validation Systems**: Pull up resistor should be placed within 1 ns of the ITP700FLEX. **ITP700FLEX supported Production Systems**: Leave this signal as NC (No Connect). See Section 4.3.1.1 and 4.3.1.4 for details.	
DBR#	Pull up to target VCC or See Notes	150 - 240		**ITP700FLEX supported Validation Systems**: The signal needs to be routed to system reset logic (e.g. connect to SYS_RESET# of ICH4-M with pull up to VccSUS3_3). Pull up resistor must be placed within 1 ns of the ITP700FLEX. **ITP700FLEX supported Production Systems**: Pull up may be required depending on impact to system reset logic that it is connected to. See Section 4.3.1.1 and 4.3.1.4 for details.	
RESET#				See RESET# in Section 14.4.1	
TCK	Pull down to GND	27.4 ± 1% (IF ITP700FLEX IS USED) 27 (IF ITP700FLEX IS NOT USED)		**ITP700FLEX supported Validation Systems**: Parallel termination resistor placed within ±200 ps of ITP700FLEX. **ITP700FLEX supported Production Systems**:	

ITP700FLEX Debug Port Connector – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Termination Resistor (**	**Notes**	✓
				Parallel termination resistor placed within 2.0” of CPU socket. See Section 4.3.1.1 and 4.3.1.4 for details..	
FBO	See Notes			**ITP700FLEX supported Validation Systems**: Point-to-point connection to CPU TCK pin. TCK should fork out at the CPU to both TCK and FBO. **ITP700FLEX supported Production Systems**: Leave the signal as NC (No Connect). See Section 4.3.1.1 and 4.3.1.4 for details.	
TDI	Pull up to VCCP	150 (IF ITP700FLEX IS USED) 150 (IF ITP700FLEX IS NOT USED)		**ITP700FLEX supported Validation Systems**: Parallel termination resistor placed within ±300 ps of CPU TDI pin. **ITP700FLEX supported Production Systems**: Parallel termination resistor placed within 2.0” of CPU pin. See Section 4.3.1.1 and 4.3.1.4 for details.	
TDO	Pull up to VCCP	54.9 ± 1% (IF ITP700FLEX IS USED)	22.6 ± 1% (IF ITP700FLEX IS USED)	**ITP700FLEX supported Validation Systems**: Signal needs to be pulled up to VCCP. Series dampening resistor placed within 1.0” of ITP700FLEX TDO pin. **ITP700FLEX supported Production Systems**: Leave the signal as NC (No Connect). See Section 4.3.1.1 and 4.3.1.4 for details.	
TMS	Pull up to VCCP	39.2 ± 1% (IF ITP700FLEX IS USED) 39 (IF ITP700FLEX IS NOT USED)		**ITP700FLEX supported Validation Systems**: Parallel termination resistor placed within ±200 ps of the ITP700FLEX TMS pin. **ITP700FLEX supported Production Systems**: Parallel termination resistor placed within 2.0” of CPU pin. See Section 4.3.1.1 and 4.3.1.4 for details.	
TRST#	Pull down to GND	510 - 680 (IF ITP700FLEX IS USED)		**ITP700FLEX supported Validation Systems**: Parallel termination resistor can be	

ITP700FLEX Debug Port Connector – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Termination Resistor (**	**Notes**	✓
		680 (IF ITP700FLEX IS NOT USED)		placed anywhere between CPU and ITP700FLEX. Avoid any trace stub from signal line to parallel termination resistor. **ITP700FLEX supported Production Systems**: Parallel termination resistor placed within 2.0” of CPU pin. See Section 4.3.1.1 and 4.3.1.4 for details.	
VTAP, VTT[1:0]	Tie to VCCP			The signals are tied together to VCCP. One 0.1 µF decoupling cap is required See section 4.3.1.1 for more details.	

NOTES:
1. See Section 14.4.2.2 if ITP Interposer is implemented.
2. See Section 14.4.2.3 if NO processor ITP debug port solution is implemented.
3. Default tolerance for resistors is +/-5% unless otherwise specified.

14.4.2.2. ITP Interposer [1, 2]

ITP Interposer					
Pin Name	**System Pull up/Pull down**		**Series Termination Resistor (**	**Notes**	✓
BPM[5:0]#				Leave the signals as NC (No Connect).	
DBA#	Pull up to target VCC	150 - 240		DBA# is an optional signal that may be implemented when an ITP Interposer is used. **ITP Interposer supported Validation Systems**: Pull up resistor should be placed within 1 ns of CPU socket. **ITP Interposer supported Production Systems:** Leave this signal as NC (No Connect). See section 4.3.2 and 4.3.2.2 for more details.	
DBR#	Pull up to V3ALWAYS	150 - 240		**ITP Interposer supported Validation Systems** This signal needs to be routed to system reset logic (e.g. SYS_RESET# of ICH4-M). Pull up resistor must be placed within 1ns of CPU socket. **ITP Interposer supported Production Systems:** Pull up may be required depending on impact to system reset logic that it is connected to. See section 4.3.2 and 4.3.2.2 for more details.	
RESET#				See RESET# in Section 14.4.1.	
TCK	Pull down to GND	27		Pull down needs to be placed within 2.0” of CPU socket.	
TDI	Pull up to VCCP	150		Pull up needs to be placed within 2.0” of CPU socket.	
TDO				Leave this signal as NC (No Connect)	
TMS	Pull up to VCCP	39		Pull up needs to be placed within 2.0” of CPU socket.	
TRST#	Pull down to GND	680		Pull down needs to be placed within 2.0” of CPU socket.	

NOTES:
1. See Section 14.4.2.1 if ITP700FLEX connector is implemented.
2. See Section 14.4.2.3 if NO processor ITP debug port solution is implemented.
3. Default tolerance for resistors is +/-5% unless otherwise specified.

14.4.2.3. Required Strapping when ITP Debug Port Disable [1, 2]

ITP Interposer					
Pin Name	**System Pull up/Pull down**		**Series Termination Resistor (**	**Notes**	✓
TCK	Pull down to GND	27		Pull down needs to be placed within 2.0" of CPU socket.	
TDI	Pull up to VCCP	150		Pull up needs to be placed within 2.0" of CPU socket.	
TDO				Leave the signal as NC (No Connect).	
TMS	Pull up to VCCP	39		Pull up needs to be placed within 2.0" of CPU socket.	
TRST#	Pull down to GND	680		Pull down needs to be placed within 2.0" of CPU socket.	

NOTES:
1. See Section 14.4.2.1 if ITP700FLEX connector is implemented.
2. See Section 14.4.2.3 if NO processor ITP debug port solution is implemented.
3. Default tolerance for resistors is +/-5% unless otherwise specified.

14.4.3. Thermal Sensor

Platform recommendations and design guidelines provided by your diode thermal sensor vendor should be adhered to ensure proper operation of your thermal sensor.

14.4.4. Decoupling Recommendations

Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	✓
VCCA[3:0]		10 µF 10 nF	4 4	VCCA[3:0] should be tied to Vcc1_8. One 1206 form factor 10 µF and one 0603 form factor 10 nF capacitor pair should be used for each VCCA pin. See Section 5.3.1 for details on guidelines for placement and routing of the VCCA decoupling capacitors	
VCC[Vcc_core]		220 µF 10 µF	4 35	**Polymer Covered Aluminium** (SP, AO Cap) **0805 MLCC, >=X6R** See Section 5.9.3 for details on guidelines for placement and routing of the VCC[Vcc_core] decoupling capacitors.	
VCCP		150 µF 0.1 µF	1 10	Polymer Covered Tantalum (POSCAP, Neocap, KO Cap) 0603 MLCC, >= X7R. Place all capacitors next to CPU. Also see Section 14.6.4 for VCCP decoupling requirement at the MCH. See Section 5.9.4 for details on Intel processor and MCH VCCP voltage plane	

Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	✓
				and decoupling.	

14.5. CK-408 Clock Checklist

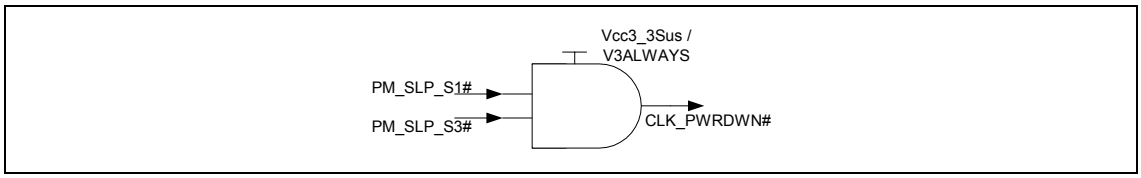
14.5.1. Resistor Recommendations

CK-408 Clock – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Resistor (**	**Notes**	✓
3V66[5:0]			33	Use three clock signals for MCH, ICH4-M, and AGP controller. See Section 10.2.2 for MCH and ICH4-M CLK66 routing requirements.	
CPU[0], CPU[0]# CPU[1], CPU[1]# CPU[2], CPU[2]#	Pull down to GND	49.9 ± 1%	33	It is required to connect one CPU clock pair to processor and another pair to MCH. See Section 12.2.1 for further discussion. **If ITP700FLEX Is Used**: Route 3rd CPU clock pair to ITP700FLEX (Routing to CPU socket NOT necessary). See Section 4.3.1.3 for routing requirements. **If ITP Interposer Is Used**: Route 3rd CPU clock pair to the ITP_CLK signals of the CPU socket (Routing to ITP700FLEX NOT necessary).	
CPU_STOP#				Point to point connection to the ICH4-M's STP_CPU# signal.	
DOT			33	If the signal is used, one 33 series resistor is required for each receiver. If NOT used, this signal can be left as NC (No Connect).	
IREF	Pull down to GND	475 ± 1%			
MULT[0]	Pull up to Vcc3_3	10 k			
PCI[6:0]			33	If the signal is used, one 33 series resistor is required for each receiver. If NOT used, this signal can be left as NC (No Connect). See Section 10.2.5 for routing requirements.	
PCI_STOP#				Point to point connection to the ICH4-M's STP_PCI# signal.	
PCIF[2:0]			33	Use one free running PCI clock signal for the ICH4-M. If NOT used, this signal can be left as NC (No Connect). See 10.2.4 for routing requirements.	
PWRDWN#				**If S1M Is Supported**: This signal should be driven by the logical AND of the ICH4-M's SLP_S1# and SLP_S3# signals. See Figure 152. **If S1M Is NOT Supported but S3 is supported**:	

CK-408 Clock – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Resistor (**	**Notes**	✓
				This signal should be driven by the ICH4-M's SLP_S3# signal.	
REF			33	If the signal is used, one 33 series resistor is required for each receiver. If NOT used, this signal can be left as NC (No Connect). See Section 10.2.7 for routing requirements.	
SEL[2:1]	Pull down to GND	1K			
SEL[0]	Pull up to Vcc3_3	1K			
USB			33	If the signal is used, one 33 series resistor is required for each receiver. If NOT used, this signal can be left as NC (No Connect).	
XTAL_IN	None See Notes			Connect to XTAL_OUT through a 14.318 MHz clock. Place crystal within 500 mils of CK-408.	
XTAL_OUT	None See Notes			Connect to XTAL_IN through a 14.318 MHz clock. Place crystal within 500 mils of CK-408.	
CK-408 Clock – Power Signals					
VDD[7:0], VDDA	Tie to Vcc3_3 See Notes			Also see Section 14.5.2 for decoupling requirement.	
CK-408 Clock – GND Signals					
VSS[5:0]	Tie to GND				
VSSA	Tie to GND				
VSSIREF	Tie to GND				

NOTE: Default tolerance for resistors is +/-5% unless otherwise specified.

Figure 152. Clock Power Down Implementation



14.5.2. CK-408 Decoupling Recommendation

Platform recommendations and decoupling guidelines provided by your CK-408 vendor should be adhered to ensure proper operation of your clock chip.

14.6. Intel 855PM MCH Checklist

14.6.1. System Memory

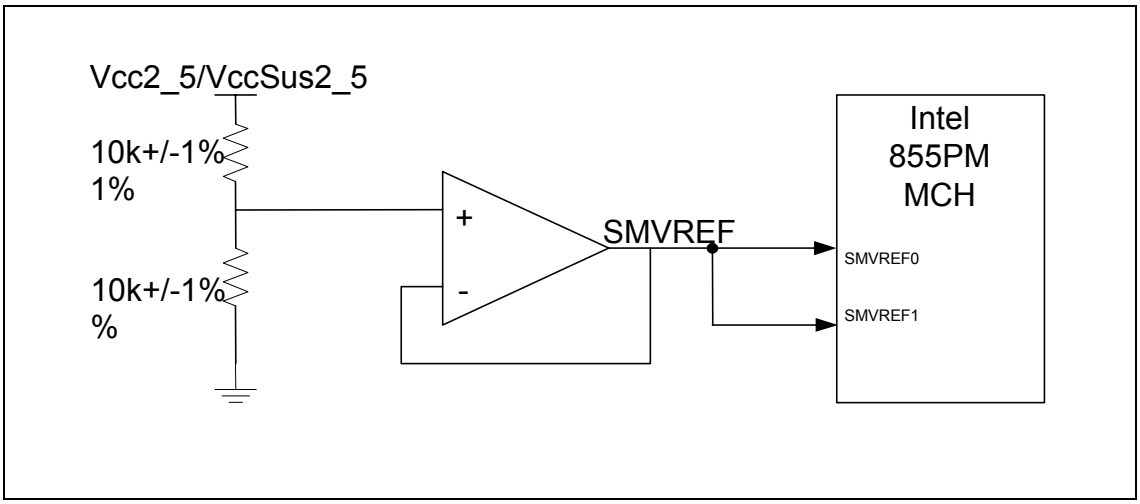
14.6.1.1. MCH System Memory Interface

Intel 855PM MCH – System Memory Interface					
Pin Name	**System Pull up/Pull down**		**Series Resistor (**	**Notes**	✓
RCVENIN#				Point to point connection to RCVENOUT#. See Section 6.1.5 for routing requirements.	
RCVENOUT#				Point to point connection to RCVENIN#. See Section 6.1.5 for routing requirements.	
SBS[1:0]	Pull up to Vcc1_25[DDR_Vtt]	56	10	Two routing topologies available for these signals. See Section 6.1.3 for routing requirements.	
SCAS#	Pull up to Vcc1_25[DDR_Vtt]	56	10	Two topologies available for routing this signal. See Section 6.1.3 for routing requirements.	
SCKE[3:0]	Pull up to Vcc1_25[DDR_Vtt]	56		See Section 6.1.2 for routing requirements.	
SCS#[3:0]	Pull up to Vcc1_25[DDR_Vtt]	56		See Section 6.1.2 for routing requirements.	
SDQ[63:0]	Pull up to Vcc1_25[DDR_Vtt]	56	10	See Section 6.1.1 for routing requirements.	
SDQ[71:64]	Pull up to Vcc1_25[DDR_Vtt] See Notes	56 See Notes	10 See Notes	See Section 6.1.1 for routing requirements. **If ECC is NOT Supported**: These signals can be left as NC (No Connect).	
SDQS[7:0]	Pull up to Vcc1_25[DDR_Vtt]	56	10	See Section 6.1.1 for routing requirements. Note that MCH package lengths must be accounted for when length matching DDR strobes and clocks. See package length information in Section 6.2.	
SDQS[8]	Pull up to Vcc1_25[DDR_Vtt] See Notes	56 See Notes	10 See Notes	Note that MCH package lengths must be accounted for when length matching DDR strobes and clocks. See package length information in Section 6.2. **If ECC is NOT Supported:** This signal can be left as NC (No Connect).	
SMA[12:0]	Pull up to Vcc1_25[DDR_Vtt]	56	10	Two routing topologies available for these signals. See Section 6.1.3 for routing requirements.	
SMVREF[1:0]	Voltage Divider	10 k 1% (top) 10 k 1% (bottom)		In S3, SMVREF [1:0] can be turned OFF. SMVREF[1:0] should be tied together. Reference voltage = (Vcc2_5 ± 5%) / 2 ± 2%. Note that a buffer is used to provide the necessary current and reference voltage to SMVREF[1:0]. A simple voltage divider may not be able to provide the necessary tolerance for these pins.	

Intel 855PM MCH – System Memory Interface					
Pin Name	**System Pull up/Pull down**		**Series Resistor (**	**Notes**	✓
				See Figure 153 and Section 11.5.3.1 for details.	
SRAS#	Pull up to Vcc1_25[DDR_Vtt]	56	10	Two routing topologies available for these signals. See Section 6.1.3 for routing requirements.	
SWE#	Pull up to Vcc1_25[DDR_Vtt]	56	10	Two routing topologies available for these signals. See Section 6.1.3 for routing requirements.	
Intel 855PM MCH – System Memory Clock Signals					
SCK[5:0], SCK[5:0]#				These differential clock signals can be routed to any SO-DIMM provided that the BIOS understands the routing implementation. Trace width option #2 (inner layer trace width=7 mils) is the recommended implementation for improved DDR timing margin. See Section 6.1.4 for routing requirements. Note that MCH package lengths must be accounted for when length matching DDR strobes and clocks. See package length information in Section 6.2. **If ECC is NOT Supported**: The 3rd differential clock pair routed to each SO-DIMM for ECC should be left as NC (No Connect). Intel design guidelines assume non-ECC memory utilizes only 2 SCK clock pairs.	
Intel 855PM MCH – System Memory Power Signals					
VCCSM[37:0]	Tie to VccSus2_5			See Section 14.6.4 for VccSus2_5 decoupling requirement.	

NOTE: Default tolerance for resistors is +/-5% unless otherwise specified.

Figure 153. Reference Voltage Level for SMVREF[1:0]



14.6.1.2. DDR SO-DIMM Interface

DDR SO-DIMM Interface					
Pin Name	**System Pull up/Pull down**		**Series Resistor**	**Notes**	✓
DDR SO-DIMM – ECC Related Signals					
CB[7:0]	See Notes			These signals are ECC related. **If ECC Is Supported**: These signals need to be routed to MCH. See SDQ[71:64] in Section 14.6.1.1. **If ECC Is NOT Supported:** These signals can be left as NC (No Connect).	
CKx, CKx# CKy, CKy#	See Notes			These signals are ECC related. CKx/CKx# and CKy/CKy# are the 3rd differential clock signal used to support ECC memory devices on a SO-DIMM module. **If ECC Is Supported:**: These signals need to be routed to MCH. See SCK[5:0], SCK[5:0]# in Section 14.6.1.1. **If ECC Is NOT Supported:** These signals should be left as NC (No Connect).	
DQS[8]	See Notes			This signal is ECC related. **If ECC Is Supported:** This signal needs to be routed to MCH. See DQS[8] in Section 14.6.1.1. **If ECC Is NOT Supported:** These signals can be left as NC (No Connect).	
DDR SO-DIMM – Reference Voltage Signals					
VREF[2:1]	See Notes			In S3, VREF[2:1] are powered ON in Intel CRB. Reference voltage = (VccSus2_5 ± 8%) / 2 ± 4%. Note that a buffer is used to provide the necessary current and reference voltage to VREF. A simple voltage divider may not be able to provide the necessary tolerance for these pins. See Section 11.5.6 for details.	
DDR SO-DIMM Interface-- Power Signals					
VDD[33:1]	Tie to VccSus2_5			Power must be supplied during S3.	
VDDSPD	Tie to Vcc3_3				
DDR SO-DIMM Interface—GND Signals					
DM[8:0]	Tie to GND				
VSS[31:1]	Tie to GND				
DDR SO-DIMM Interface—No Connect Signals					

DU[4:1]	See Notes			This signal can be left as NC (No Connect).	
GND[1:0]	See Notes			This signal can be left as NC (No Connect).	
RESET(DU)	See Notes			This signal can be left as NC (No Connect).	
VDDID	See Notes			This signal can be left as NC (No Connect).	
DDR SO-DIMM Interface—Misc Signal					
SA[2:0]	Tie to GND / Connect to VCC3_3 See Notes			SPD EEPROM Address Detection: **For 1st SO-DIMM address 'A0':** SA[2:0] should be tied to GND **For 2nd SO-DIMM address 'A2':** SA[0] – Tie to VCC3_3 SA[2:1] – Tie to GND	

14.6.2. Miscellaneous Signals

MCH – Miscellaneous Signals					
Pin Name	**System Pull up/Pull down**		**F**	**Notes**	✓
External Thermal Sensor Based Throttling Signal					
ETS#	See Notes	See Notes		If ETS# Is NOT Used: (Default is Disabled) No external pull up is required. If ETS# Is Used: This signal needs to be pulled up to a 2.5 V source through a 8.2 k to 10 k See Section 6.8 for details.	
Hub Interface Signals					
HSWNG[1:0]		301 ± 1% (top) 150 ± 1% (bottom)		Signal voltage level = 1/3 * VCCP. R1a = R1b = 301 ± 1% R2a = R2b = 150 ± 1% C1a = C1b = 0.1 uF See See Figure 154 and Section 4.1.8.2 for details.	
VCCHL[4:0]	Tie to Vcc1_8			Also see Section 14.6.4 for Vcc1_8 decoupling requirement.	
Other Signals					
TESTIN				This signal can be left as NC (No Connect).	
Power Signals					
VCC[9:0]	Tie to Vcc1_2[Vcc_mch]			See Section 14.6.4 for VCC_MCH decoupling requirements.	
VTT[19:0]	Tie to VCCP				
Ground Signals					
VSS[141:0]	Tie to GND				

Figure 154. Intel 855PM MCH HSWNG[1:0] Reference Voltage Generation Circuit

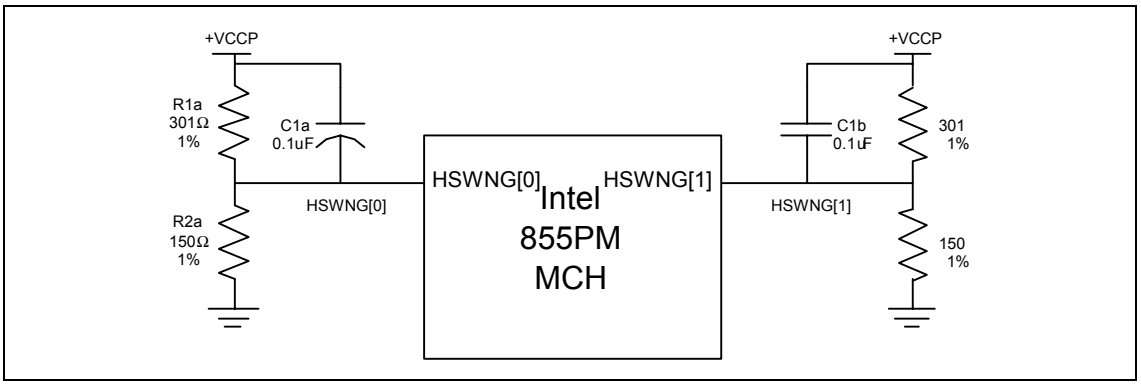
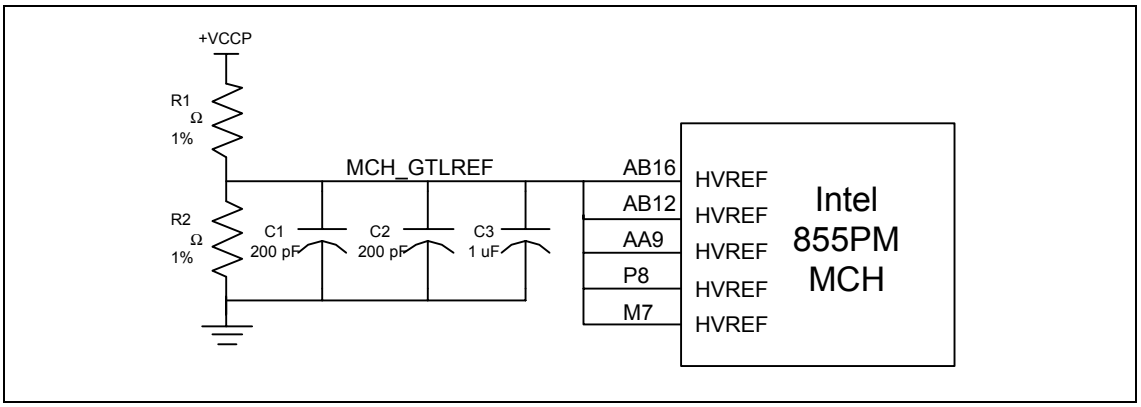


Figure 155. Intel 855PM MCH HVREF[4:0] Generation Circuit



14.6.3. Resistive Compensation

MCH – Resistive Compensation				
Pin Name	**System Pull up/Pull down**		**Notes**	✓
GRCOMP	Pull down to GND	36.5 ± 1%	GRCOMP resistor value = 2/3 * AGP routing channel impedance. Intel CRB uses 40.2 ± 1% pull down resistor for GRCOMP.	
HLRCOMP	Pull up to Vcc1_8	36.5 ± 1%	HLRCOMP resistor value = 2/3 * board impedance.	
HRCOMP[1:0]	Pull down to GND	27.4 ± 1%	Each signal should be pulled down to ground through a 27.4 ± 1% resistor with a Zo = 27.4 trace. Max trace length from pin to resistor should be < 0.5" and ~18 mils wide. Recommend routing 25 mils away from any switching signal. See Section 4.1.8.2 for details.	
SMRCOMP	Pull up to Vcc1_25[DDR_Vtt]	30.1 ± 1%	In S3, Vcc1_25[DDR_Vtt] (DDR channel termination voltage) can be turned OFF. One 0.1 µF decoupling cap is required for this signal.	

14.6.4. Decoupling Recommendations (MCH)

MCH– Decoupling Recommendations[1]					
Pin Name	**Configuration**	**F**	**Qty**	**Notes**	✓
SMRCOMP	Tie to Vcc1_25[DDR_Vtt]	0.1 µF	1	Decoupling capacitor must be connected to the power-side of the RCOMP resistor.	
Vcc1_8	Tie to Vcc1_8	0.1 µF	2	Two 0.1 µF capacitors are recommended for Vcc1_8 decoupling. All values are preliminary. See Section 8.5 for details	
VccSus2_5	Tie to VccSus2_5	0.1 µF	15	Place within 150 mils of MCH package. See Section 11.5.1.1	
VCC-MCH	Tie to VCC_MCH	150 µF 2.2 µF 220 nF 47 nF 22 nF 15 nF 10 nF	2 1 1 1 1 1 1	See Section 5.9.5for details.	
VCCGA, VCCHA	Tie to Vcc1_8	10 µF 10 nF	1 1	VCCGA and VCCHA can both share a 10 µF and 10nF decoupling capacitor.	
VCCP	Tie to VCCP	10 µF 0.1 µF	1 8	Polymer covered tantalum. Place next to the MCH. 0603 MLCC, >= X7R. Place next to the MCH.	

14.6.5. Memory Decoupling Recommendation

Memory Decoupling Recommendations[1]					
Pin Name	**Configuration**	**F**	**Qty**	**Notes**	✓
Vcc1_25[DDR_Vtt]	See Notes	0.1 µF	See Notes	In S3, Vcc1_25[DDR_Vtt] (DDR channel termination voltage) can be turned OFF. Place one 0.1 µF close to every 2 pull up resistors terminated to Vcc1_25[DDR_Vtt]. See Section 11.7.4 for details.	
VccSus2_5		0.1 µF	9	Place capacitors between the SO-DIMMs . See Section 11.5.1.2 for details.	

14.6.6. MCH Reference Voltage

MCH – Reference Voltage				
Pin Name	**System Pull up/Pull down**		**Notes**	✓
AGPREF	Voltage divider	1 k ± 1% (top & bottom)		
HI_REF	Voltage divider	100 - 150 ± 1% (top & bottom) See Notes	HIVREF(ICH4-M signal), HI_VSWING (ICH4-M signal), and HI_REF(MCH signal) may share a common hub interface reference voltage divider if the divider is located within 3” from both the MCH and ICH4-M. See Figure 157 and Section 8.4 for more details. For each of the 3 signals, a locally generated hub interface reference voltage divider must be used if the common reference voltage divider is located more than 3” away from the component. See Figure 158 and Section 8.4 for more details.	
HVREF[4:0]		49.9 ± 1% (top) 100 ± 1% (bottom)	Place R1 close to HVREF4 (ballout AB16) and R2 close to HVREF1 (ballout P8). See Figure 155. R1a = 49.9 ± 1% R2a = 100 ± 1% C1 = 200 pF C2 = 200 pF C3 = 1 µF See Section 4.1.7 for routing requirements.	

14.7. AGP Interface

14.7.1. Resistor Recommendations

Intel 855PM MCH AGP Interface – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
AD_STB[1:0]	See Notes			Point to point connection to AGP controller. MCH has an internal pull up. External pull up is **NOT** required.	
AD_STB[1:0]#	See Notes			Point to point connection to AGP controller. MCH has an internal pull down. External pull down is **NOT** required.	
DEVSEL# FRAME# GNT# IRDY# REQ# STOP# TRDY# PIPE# RBF# WBF#	See Notes			Point to point connection to AGP controller. MCH has an internal pull up. External pull up is **NOT** required.	
SB_STB	See Notes			Point to point connection to AGP controller. MCH has an internal pull up. External pullup is **NOT** required.	
SB_STB#	See Notes			Connect directly to AGP controller. MCH has an internal pull down. External pull down is **NOT** required.	
Intel(R) Intel 855PM MCH AGP Interface – Power Signals					
VCCAGP[15:0]	Tie to Vcc1_5			Also see Section 11.7.5 for decoupling requirement.	

NOTE: Default tolerance for resistors is +/-5% unless otherwise specified.

14.7.1.1. AGP Connector

AGP Connector Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
SERR#, PERR#	Pull up to Vcc1_5	8.2 k		PERR# and SERR# are not supported in the MCH. An external pull up to a 1.5 V source is required for AGP controllers that implement these signals.	
INTA#, INTB#				Route to the ICH4-M PIRQ signals.	

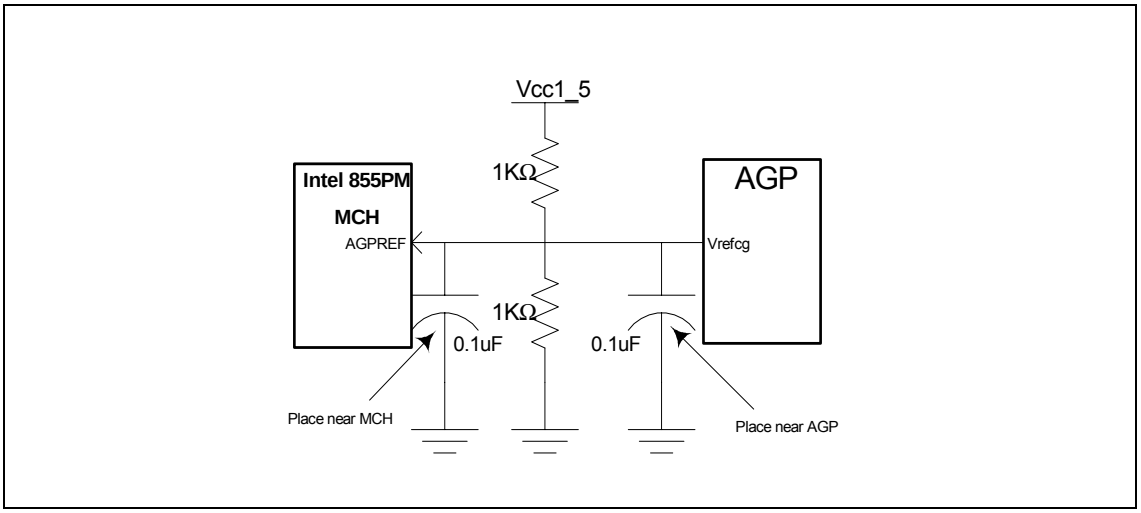
14.7.1.2. AGP Decoupling Recommendations

Intel 855PM MCH Interface – High Frequency Decoupling Recommendations[1]					
Pin Name	**Configuration**	**F**	**Qty**	**Notes**	✓
Vcc1_5	Pull down to GND	0.01 µF	6	Place a minimum of six 0.01 µF within 70 mils of the outer row of balls on the MCH. Place one extra 0.01 µF cap for every 10 vias that transition the AGP signal from one reference signal plane to another. Intel CRB uses 7x 0.1 µF, 1x 22 µF, and 1x 100 µF.	

14.7.1.3. AGP VREF Reference Voltage Dividers

MCH AGP Interface – Reference Voltage Dividers				
Pin Name	**System Pull up/Pull down**		**Notes**	✓
AGPREF	Voltage divider	1 k top) 1 k bottom)	Source generated VREFs are recommended. See Section 7.3.8 for more details. See Figure 156 for impelementation on Intel CRB.	

Figure 156. AGPREF Implementation (On Intel CRB)



14.8. ICH4-M Checklist

Note: All inputs to the ICH4-M must not be left floating. Many GPIO signals are fixed inputs that must be pulled up to different sources.

14.8.1. ICH4-M Resistor Recommendations

ICH4-M – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
PCI Resistor Recommendations					
DEVSEL#	Pull up to Vcc3_3	8.2 k			
FRAME#	Pull up to Vcc3_3	8.2 k			
GPIO0/REQA# GPIO1/REQB#/ REQ5#	Pull up to Vcc3_3	8.2 k		Each signal requires a pull up.	
GPIO16 / GNTA#	See Notes			GNT[A] has an added strap function of “top block swap”. This signal is sampled on the rising edge of PWROK. By default, this signal is HIGH or strap function is DISABLE. Strap function can be enabled by pulling down this signal to GND through a 1 k resistor.	
IRDY#	Pull up to Vcc3_3	8.2 k			
LOCK#	Pull up to Vcc3_3	8.2 k			
PERR#	Pull up to Vcc3_3	8.2 k			
SERR#	Pull up to Vcc3_3	8.2 k			
STOP#	Pull up to Vcc3_3	8.2 k			
TRDY#	Pull up to Vcc3_3	8.2 k			
REQ[4:0]#	Pull up to Vcc3_3	8.2 k		Each signal requires a pull up.	
Interrupt Interface Resistor Recommendations					
APICCLK	Pull down to GND (If NOT Used)			Recommended to disable APICCLK and APICD[1:0].	
APICD[1:0]	Pull down to GND (If NOT Used)	10 k		Recommended to disable APICCLK and APICD[1:0]: If XOR Chain Testing Is **NOT** Used: Pull down the signals through a shared 10-k resistor. If XOR Chain Testing Is Used: Each signal requires a separate 10-k pull down resistor.	
IRQ[15:14]	Pull up to Vcc3_3	8.2 k - 10 k			

ICH4-M – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
PIRQ#[A:D] PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5	Pull up to Vcc3_3 See Notes	8.2 k		External pull up is required for INT_PIRQ#[A:D]. External pull-up is required when muxed signal (INT_PIRQ[E:H]#/ GPIO[2:5]) is implemented as PIRQ.	
SERIRQ	Pull up to Vcc3_3	8.2 k			

NOTE: Default tolerance for resistors is +/-5% unless otherwise specified.

14.8.2. GPIO

Checklist Items	Recommendations	Reason/Impact
GPIO Balls	**GPIO[7] & [5:0]:** These balls are in the Main Power Well. Pull-ups must use the V_{CC}3_3 plane. Unused core well inputs must be pulled up to V_{CC}3_3. GPIO[1:0] can be used as REQ[B:A]#. GPIO[1] can be used as PCI REQ[5]#. GPIO[5:2] can be used as PIRQ[H:E]#. These signals are 5-V tolerant These pins are inputs	*Ensure ALL unconnected signals are OUTPUTS ONLY!*
	GPIO[8] & [13:11]: These balls are in the Resume Power Well. Pull-ups go to V_{CC}Sus3_3 plane. Unused resume well inputs must be pulled up to V_{CC}Sus3_3. These are the only GPIs that can be used as ACPI compliant wake events. These signals are not 5-V tolerant. GPIO[8] can be used as SMC_EXTSMI# GPIO[11] can be used as SMBALERT#. GPIO[13] can be used as SMC_WAKE_SCI# These pins are inputs	Main power well GPIOs are 5-V tolerant, except for GPIO[43:32]. Resume power well GPIOs are not 5-V tolerant
	GPIO[23:16]: Fixed as output only. Can be left NC. In Main Power Well (V_{CC}3_3). GPIO[17:16] can be used as GNT[B:A]#. GPIO[17] can be used as PCI GNT[5]#. STP_PCI#/GPIO[18] – used in mobile as STP_PCI# only. SLP_S1#/GPIO[19] – used in mobile as SLP_S1# only. STP_CPU#/GPIO[20] – used in mobile as STP_CPU# only. C3_STAT#/GPIO[21] – used in mobile as C3_STAT# only. CPUPERF#/GPIO[22] – open drain signal. Used in mobile as CPUPERF# only. SSMUXSEL/GPIO[23] – used in mobile as SSMUXSEL only.	
	GPIO[28,27,25,24]: I/O balls. Default as outputs. Can be left NC. These pins are in the Resume Power Well CLKRUN#/GPIO[24] (Note: use pull up to V_{CC}3_3 if signal is required to be pulled up) GPIO[28, 27, 25] From resume power well (V_{CC}Sus3_3). (Note: use pull up to V_{CC}3_3 if this signal is pulled up) These signals are NOT 5-V tolerant. GPIO[25] can be used as AUDIO_PWRDN	

	GPIO[43:32]: I/O balls. From main power well ($V_{CC}3\_3$). Default as outputs when enabled as GPIOs These signals are NOT 5-V tolerant GPIO[32] can be used as AGP_SUSPEND# GPIO[33] can be used as KSC_VPPEN# GPIO[34] can be used as SER_EN GPIO[35] can be used as FWH_WP# GPIO[36] can be used as FWH_TBL# GPIO[40] can be used as IDE_PATADET GPIO[41] can be used as IDE_SATADET	

14.8.3. AGP Busy/Stop Design Requirements

AGP Busy/Stop design requirements				
Signal	**System Pull up/Pull down**		**Notes**	✓
AGPBUSY#	Pull up to Vcc3_3	10 k	This ICH4-M signal requires a pull up to the switched 3.3-V rail (the 3.3V power rail which will be powered OFF during S3). This ICH4-M signal must be connected to the AGP_BUSY# output of the external AGP Graphics Controller.	
C3_STAT#	No pull up/pull down required. See notes		When an external AGP device is enabled, this signal must be connected from ICH4-M to the external AGP Graphics Controller for STP_AGP# signal implementation.	
SUS_STAT#	No pull up/pull down required. See notes		When an external AGP device is enabled, this signal must be connected from ICH4-M to the external AGP Graphics Controller if the AGP device is designed to use this signal. Assertion of this ICH4-M signal indicates that the system will be entering one of the S1-S5 low-power states, and that the platform clocks (including the AGP clock) will soon stop toggling. This signal can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used as an indication that the peripherals should isolate their outputs that may be going to powered-off planes.	

NOTE: Please also consult Intel for the latest AGP Busy and Stop signal implementation.

14.8.4. System Management Bus (SMBus) Interface

ICH4-M System Management Interface – Resistor Recommendations				
Pin Name	**System Pull up/Pull down**		**Notes**	✓
INTRUDER#	Pull up to VccRTC	10 k	RTC well input requires pull up to reduce leakage from coin cell battery in G3.	
SMBALERT#/ GPIO[11]	Pull up to V3ALWAYS	10 k		
SMBCLK SMBDATA	Pull up to V3ALWAYS	See Notes	Requires external pull up resistors. Pull up value is determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. Resistor change for faster rise time and to ensure timings are within specification. Value of pull up resistor is also determined by line load. Intel CRB uses 10K pull up resistor. Please see Intel CRB schematics page 18. The SMBus and SMLink signals must be tied together externally in S0 for SMBus 2.0 compliance: SMBCLK connects to SMLink[0] SMBDATA connects to SMLink[1]	
SMLINK[1:0]	Pull up to V3ALWAYS	See Notes	Requires external pull up resistors. Pull up value is determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. Resistor change for faster rise time and to ensure timings are within specification. Value of pull up resistor is also determined by line load. Intel CRB uses 4.7 k pull up resistor. Please see Intel schematics page 18. The SMLink and SMBus signals must be tied together externally in S0 for SMBus 2.0 compliance: SMLink[0] connects to SMBCLK SMLink[1] connects to SMBDATA	

14.8.5. AC ’97 Interface

ICH4-M AC ’97 Interface – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Termination Resistor**	**Notes**	✓
AC_BIT_CLK			33 - 47	The internal pull down resistor is controlled by the AC’97 Global Control Register, ACLINK Shut Off bit: 1 = enabled 0 = disabled When no AC'97 devices are connected to the link, BIOS must set the ACLINK Shut Off bit for the internal keeper resistors to be ENABLED. At that point, pull ups/pull downs are NOT needed on ANY of the link signals. See Section 9.3 for routing requirements	
AC_SDIN[2:0]			33 - 47	A series termination resistor (R1) is required for the PRIMARY CODEC. A series termination resistor is required for the SECONDARY (R2=R1) and TERTIARY (R3=R1) CODEC if the resistor is not found on CODEC. See Section 9.3 for routing requirements.	
AC_SDOUT			33 - 47	A series termination resistor is required for the PRIMARY CODEC. One series termination resistor (R2=R1) is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card. See Section 9.3 for routing requirements.	
AC_SYNC			33 - 47	A series termination resistor is required for the PRIMARY CODEC. One series termination resistor (R2=R1) is required for the SECONDARY/ TERTIARY CODEC connector card if the resistor is not found on the connector card. See Section 9.3 for routing requirements.	

14.8.6. ICH4-M Power Management Interface

ICH4-M Power Management Interface – Resistor Recommendations					
Pin Name	**System Pull up/ Pull down**		**Series Damping**	**Notes**	✓
DPRSLPVR				External pull down not required. Signal has integrated pull down in ICH4-M.	
SLP_S1# SLP_S3# SLP_S4# SLP_S5#				External pull up not required. Signals driven by ICH4-M.	
BATLOW#	See Notes	10 k		Pull up is not required if it is used. However, signal must not float if it is NOT being used (Signal should be pull up to V3ALWAYS through a 10 k pull up resistor).	
CLKRUN#	Pull up to Vcc3_3	10 k			
PWRBTN#				When asserted, this ICH4-M input signal will indicate a system request to go into a sleep event or cause a wake event (if the system is already in a Sleep state). This signal is recommended to connect to a power button or any other equivalent driver. This signal has integrated pull up External pull up/down not required.	
PWROK	Pull down to GND See Notes	100 k		RTC well input requires pull down to reduce leakage from coin cell battery in G3. Input must not float in G3. This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both Vcc3_3 and Vcc1_8 have reached their nominal voltages. Intel CRB uses a 100 k pull down to reduce leakage from coin cell battery in G3.	
RI#	Pull up to V3ALWAYS	10 k		If this signal is enabled as a wake event, it is important to keep this signal powered during a power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.	
RSMRST#	Pull down to GND	100 k		RSMRST# is a RTC well input and requires pull down to reduce leakage from coin cell battery in G3. Input must not float in G3. This signal should be connected to power monitoring logic and should go high no sooner than 5 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Intel CRB uses a 100 k pull-down to reduce leakage from coin cell battery in G3.	
THRM#	Pull up to Vcc3_3 (If NOT USED)	8.2 k (If NOT Used)		**If THRM# Is Used**: THRM# is a 3.3 V tolerant signal. Voltage translation may be required if other thermal	

ICH4-M Power Management Interface – Resistor Recommendations					
Pin Name	**System Pull up/ Pull down**		**Series Damping**	**Notes**	✓
				sensors are used. **If THRM# Is NOT Used**: If this signal is not connected to a driver, then it is required to be terminated with a 8.2 k pull up to Vcc3_3.	
SYS_RESET#	Pull up to VccSus3_3	100 k (if signal is not used)		Implementation of this signal is optional. When this signal is asserted, system will be put into reset. **If SYS_RESET# Is Used:** A weak pull up is required to prevent the signal from floating. **If SYS_RESET# Is NOT Used:** Pull up to VccSus3_3 through a 100 k	

14.8.7. FWH/LPC Interface

ICH4-M FWH/LPC Interface – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
FWH[3:0]/LAD[3:0]	See Notes			Extra pull ups not required. Connect directly to FWH/LPC.	

14.8.8. USB Interface

ICH4-M USB Interface – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
OC[5:0]#	Pul lup to V3ALWAYS	10 k		These signals are inputs into the ICH4-M and must not be left floating. Pull up is required. If an OC pin is not connected to a current monitor or equivalent device for a given USB port, an alternative mechanism should be provided to handle a potential over current condition.	
USBRBIAS USBRBIAS#	Pull down to GND	22.6 ± 1%		Tie signals together and pull down through a common 22.6 ± 1% resistor. The RBIAS resistor should be placed within 500 mils of the ICH4-M and avoid routing next to clock pins.	

14.8.9. Hub Interface

14.8.9.1. Hub Interface Resistor Recommendations

ICH4-M Hub Interface – Resistor Recommendations				
Pin Name	**System Pull up/Pull down**		**Notes**	✓
HICOMP	Pull down to GND See Notes	36.5 ± 1%	HICOMP resistor value = 2/3 * board impedance. Place resistor within 0.5” of ICH4-M pad using a thick trace. Intel CRB uses 36.5 ± 1% resistor.	

NOTE: Default tolerance for resistors is +/-5% unless otherwise specified.

14.8.9.2. Reference Voltage Dividers

ICH4-M Hub Interface – Reference Voltage Dividers[1]				
Pin Name	**System Pull up/Pull down**		**Notes**	✓
HIVREF	See Notes		HIVREF, HI_VSWING and HI_REF(MCH signal) can share a common hub interface reference divider. Also see Figure 157. For each of the 3 signals, a locally generated hub interface reference divider must be used if the common reference divider is located at more than 3” away. Please see Figure 158. See page 8 and 15 in the Intel CRB schematics.	
HI_VSWING	See Notes		HIVREF, HI_VSWING and HI_REF(MCH signal) can share a common hub interface reference divider. Also see Figure 157. For each of the 3 signals, a locally generated hub interface reference divider must be used if the common reference divider is located at more than 3” away. Please see Figure 158. See page 8 and 15 in the Intel CRB schematics.	

Figure 157. Hub Interface with Signal Reference Voltage Divider Circuit

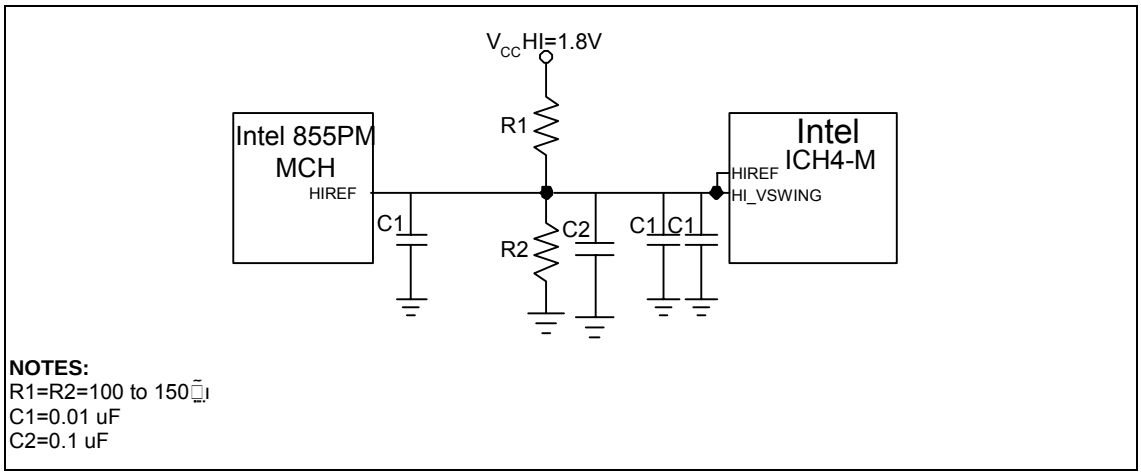
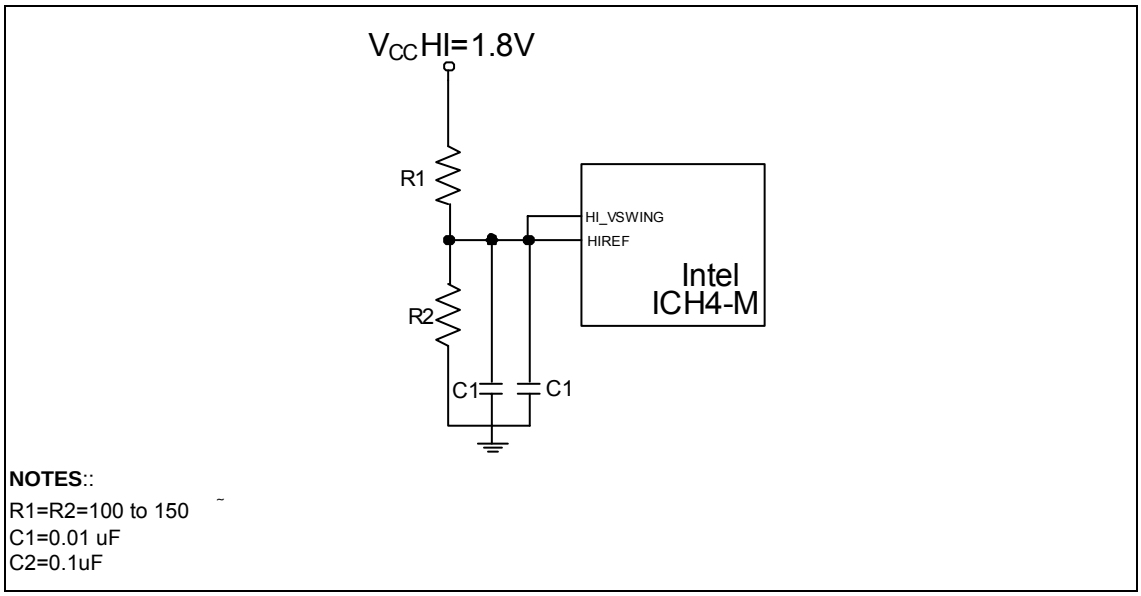


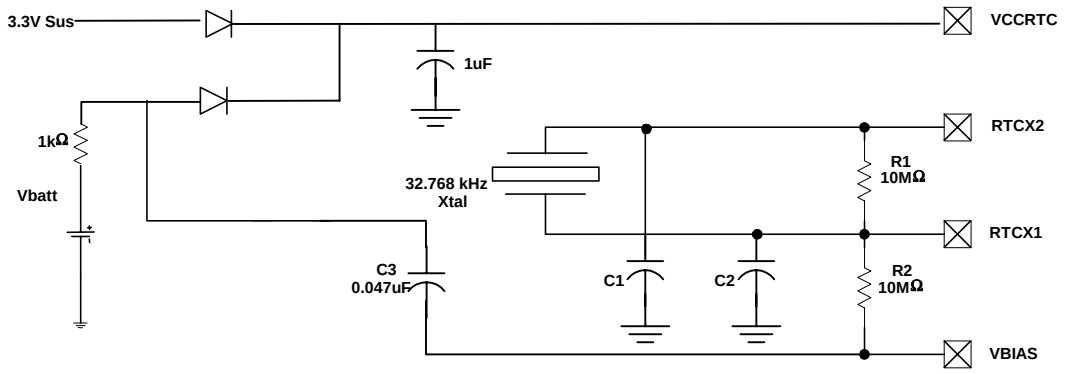
Figure 158. Hub Interface with Locally Generated Reference Voltage Divider Circuit



14.8.10. RTC Circuitry

ICH4-M RTC Circuitry Topology Recommendations				
Pin Name	**System Pull up/Pull down**		**Notes**	✓
RTCRST#	Vcc_RTC	180 k	Pull up to VccRTC through a 180 k resistor. Also see Section 8.16 for decoupling requirements. RTC_RST# should have a 18 – 25 ms delay. Any RC circuit which will result in the 18-25 ms delay is acceptable.	
CLK_RTCX1, CLK_RTCX2	See notes		Connect a 32.768 kHZ crystal oscillator across these pins with a 10 m resistor and use a decoupling cap at each signal. Please consult Section 9.8.2 for calculating a specific capacitance value for C1 and C2. See Figure 159 Please note that peak-to-peak swing on RTCX1 cannot exceed 1.0 V	
CLK_VBIAS	See notes		Connect to CLK_RTCX1 through a 10-m resistor. Connect to Vbatt through a 1k ohms in series with a 0.047-µF capacitor.	

Figure 159 External Circuitry for the RTC



Notes
Reference Designators Arbitrarily Assigned
3.3V Sus is Active Whenever System Plugged In
Vbatt is Voltage Provided By Battery

VBIAS, VCCRTC, RTCX1, and RTCX2 are ICH4-M pins
VBIAS is used to bias the ICH4 Internal Oscillator
VCCRTC powers the RTC well of the ICH4-M
RTCX1 is the Input to the Internal Oscillator
RTCX2 is the feedback for the external crystal

14.8.11. LAN Interface

ICH4-M LAN Interface Recommendations				
Pin Name	**System Pull up/Pull down**		**Notes**	✓
LAN_CLK	See Notes		Connect to LAN_CLK on the platform LAN Connect Device. See Section 9.9.2 for routing requirements. If LAN interface is not used, leave the signal unconnected (NC)	
LAN_RST#	See Notes		Timing Requirement: Signal should be connected to power monitoring logic, and should go high no sooner than 5 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages. NOTE: If ICH4-M LAN controller is NOT used, pull LAN_RST# down through a 10K resistor.	
LAN_RXD[2:0]	See Notes		Connect to LAN_RXD on the platform LAN Connect Device. See Section 9.9.2 for routing requirements. If LAN interface is not used, leave the signal unconnected (NC)	
LAN_TXD[2:0]	See Notes		Connect to LAN_TXD on Platform LAN Connect Device. See Section 9.9.2for routing requirements. If LAN interface is not used, leave the signal unconnected (NC)	
LAN_RSTYSNC	See Notes		Connect to LAN_RSTSYNC on Platform LAN Connect Devce. See Section 9.9.2 for routing requirements. If LAN interface is not used, leave the signal unconnected (NC).	
VCCLAN1.5[1:0] VCCLAN3.3[1:0]	See Notes		If ICH4-M LAN connect interface is used: Connect VCCLAN1.5[1:0] to the customer designated 1.5VLAN power rail Connect VCCLAN3.3[1:0] to the customer designated 3.3VLAN power rail If ICH4-M LAN connect interface is not used: Connect VCCLAN1.5[1:0] to Vcc1_5 Connect VCCLAN3.3[1:0] to Vcc3_3	

14.8.12. Primary IDE Interface

ICH4-M IDE Interface – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
PDD[15:0]	None			No extra series termination resistors or other pull ups/pull downs are required. These signals have integrated series resistors. PDD7/SDD7 does not require a 10 KΩ pull down resistor. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω. Refer to ATA ATAPI-4 specification.	
PDA[2:0], PDCS1#, PDCS3#, PDDACK#, PDIOW#, PDIOR#	None			No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns. These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 but can range from 31 to 43 .	
PDDREQ	None			No extra series termination resistors. No pull-down resistors needed. These signals have integrated series resistors in the ICH4-M. These signals have integrated pull down resistors in the ICH4-M.	
PIORDY	Pull up to Vcc3_3	4.7 k		This signal has integrated series resistor in the ICH4-M	
PCI_RST#			22 - 47	The signal must be buffered to form IDE_RST# for improved signal integrity.	
Mobile IDE Swap Bay Support				See Section 9.1.4 for implementating the ICH4-M's IDE interface tri-state feature. This feature can be used for systems designed to support an IDE "hot" swap drive bay.	

14.8.13. IDE Interface (Secondary IDE Connector)

ICH4-M IDE Interface – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
SDD[15:0]	None			No extra series termination resistors or other pull ups/pull downs are required. These signals have integrated series resistors. PDD7/SDD7 does not require a 10 KΩ pull down resistor. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω. Refer to ATA ATAPI-4 specification.	
SDA[2:0], SDCS1#, SDCS3#, SDDACK#, SDIOW#, SDIOR#	None			No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns. These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 but can range from 31 to 43 .	
SDDREQ	None			No extra series termination resistors. No pull down resistors needed. This signal has integrated series resistors in the ICH4-M. This signal has integrated pull down resistors in the ICH4-M.	
SIORDY	Pull up to Vcc3_3	4.7 k		This signal has integrated series resistor in the ICH4-M	
PCI_RST#			22 - 47	The signal must be buffered to form IDE_RST# for improved signal integrity.	
Mobile IDE Swap Bay Support				See Section 9.1.4 contains recommendations for implementating the ICH4-M's IDE interface tri-state feature. This feature can be used for systems designed to support an IDE "hot" swap drive bay.	

14.8.14. Miscellaneous Signals

ICH4-M Miscellaneous Signals					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
SPKR	See notes			SPKR is a strapping option for the TCO Timer Reboot function and is sampled on the rising edge of PWROK. An integrated weak pull down is enabled only at boot/reset. Status of strap is readable via the NO_REBOOT bit (D31:F0, Offset D4h, bit 1) 1 = disabled 0 = enabled (normal operation) To disable, a jumper can be populated to pull SPKR high. Value of pull up must be such that the voltage divider output caused by the pull up, effective impedance of speaker and codec circuit, and internal pull down will be read as logic high (0.5 * Vcc3_3 to Vcc3_3 + 0.5)	

14.8.15. ICH4-M Power Signals & Decoupling Recommendations

ICH4-M – Power Signals & Decoupling Recommendations[1,2]				
Pin Name	**System Pull up/Pull down**		**Notes**	✓
VCC1.5[15:0]	Tie to Vcc1_5		Two 0.1 µF capacitors (place near balls: K23 and C23) are required for decoupling.	
VCC3.3[15:0]	Tie to Vcc3_3		Six 0.1 µF capacitors (place near ball : A1, A4, H1, T1, AC10, and AC18) are required for decoupling.	
VCCSUS1.5[7:0]	Tie to V1_5ALWAYS		Two 0.1 µF capacitors (place near balls: A16 and AC1) are required for decoupling.	
VCCSUS3.3[9:0]	Tie to V3ALWAYS		Two 0.1 µF capacitors (place near ball: A22 and AC5) are required for decoupling.	
VCCLAN1.5[1:0]	Tie to VccSus1_5		Two 0.1 µF capacitors (place near ball: F6 and F7) are required for decoupling.	
VCCLAN3.3[1:0]	Tie to VccSus3_3		Two 0.1 µF capacitors (place near ball: E9 and F9) are required for decoupling.	
VCC5REF[2:1]	Tie to Vcc5	1 k	One 0.1 µF capacitor (place near ball: E7) is required for decoupling.	
VCC5REFSUS1	See Notes		One 0.1 µF capacitor (place near ball: A16) is required for decoupling. **If Wake on USB from S3 and self-powered USB devices are supported:** Tie to V5ALWAYS **If Wake on USB from S3 and self-powered USB devices are NOT supported:** Tie to a combination of V3ALWAYS and Vcc5 or VccSus5. See Section 11.4.1.3 for more details.	
VCC_CPU_IO[2:0]	Tie to VCCP		One 0.1 µF capacitor (place near ball: AA23) is required for decoupling.	
VCCPLL	Tie to Vcc1_5		One 0.1 µF and one 0.01 uF capacitors (place near ball C22) are required for decoupling.	
VCCRTC	Tie to Vcc_RTC		One 0.1 µF capacitor (place near ball: AB5) is required for decoupling.	
VCCHI[3:0]	Tie to Vcc1_8		Two 0.1 µF capacitors (place near balls: T23 and N23) are required for decoupling.	

NOTES:

1. All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, and PCB board design into consideration when deciding on their overall decoupling solution
2. Capacitors should be place less than 100 mils from the package

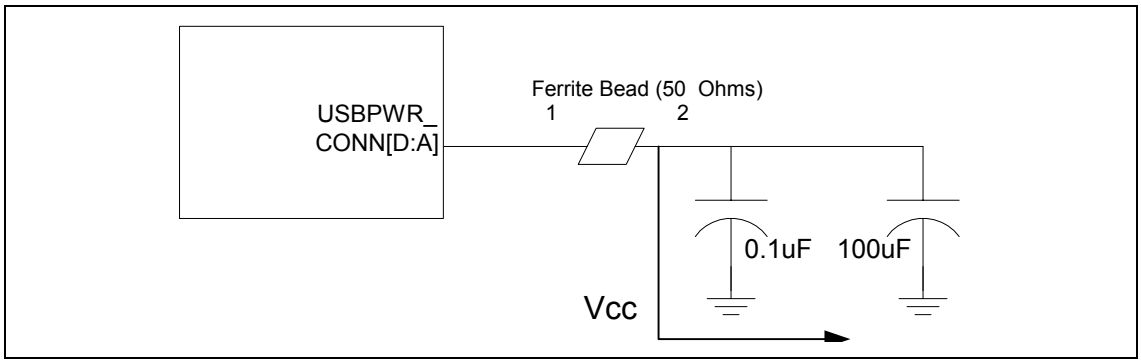
14.9. USB Checklist

14.9.1. Resistor Recommendations

USB – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
USBPWR_CONN[E:A]				Each signal requires a LC Pi filter that consists of one 0.1 µF, one 100 µF and one ferrite bead in Intel CRB. See Figure 160 Both caps on Pin 2 of ferrite bead. Optimal decoupling achieve with 100 µF cap on connector side of ferrite bead.	

NOTE: Default tolerance for resistors is +/-5% unless otherwise specified.

Figure 160. USBPWR_CONN[E:A] Design Recommendation



14.9.2. Decoupling Recommendations

USB – Decoupling Recommendations[1]					
Signal	**Configuration**	**F**	**Qty**	**Notes**	✓
V5_USB[3:1] (signal)	Pull down to GND	0.1 µF	1	In Intel CRB, each signal requires a decoupling cap.	

NOTE: All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, and PCB board design into consideration when deciding on their overall decoupling solution.

14.10. FWH Checklist

14.10.1. Resistor Recommendations

FWH – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
FGPI[4:0]	See Notes			Can be connected directly to GND In Intel CRB, each signal requires a 100 ohms pull down resistor.	
IC	See Notes			In Intel CRB, the signal requires a 10 kohms pull down resistor.	
RST#			100	In Intel CRB, the signal requires a 100 ohms series damping resistor.	
FWH – Power SIgnals					
VCC[2:1] VCCA VPP	Tie to Vcc3_3 See Notes			Also see Section 10.2 for decoupling requirement.	
FWH – GND SIgnals					
GND[2:1], GNDA	Tie to GND				
FWH – Test Point Signals					
ID[3:0]	See Notes			Signals are recommended to be connected to test points.	
RSVD[5:1]	See Notes			Signals are recommended to be connected to test points.	
FWH – Not Connected Signals					
NC[8:1]	None			The signals should be left as NC (“Not Connected”)	

NOTE: Default tolerance for resistors is +/-5% unless otherwise specified.

14.10.2. Decoupling Recommendations

FWH – Decoupling Recommendations[1]					
Pin Name	**Configuration**	**F**	**Qty**	**Notes**	✓

FWH – Decoupling Recommendations[1]					
Pin Name	**Configuration**	**F**	**Qty**	**Notes**	✓
VCC[2:1] VCCA VPP	Pull down to GND	0.1 µF 4.7 µF	2 1	In Intel CRB, two 0.1 µF s and one 4.7 µF capacitors are used for decoupling. The decoupling recommendation is shared among all 5 signals. Please see Intel CRB schematics.	

NOTE: All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, and PCB board design into consideration when deciding on their overall decoupling solution.

14.11. LAN / HomePNA Checklist

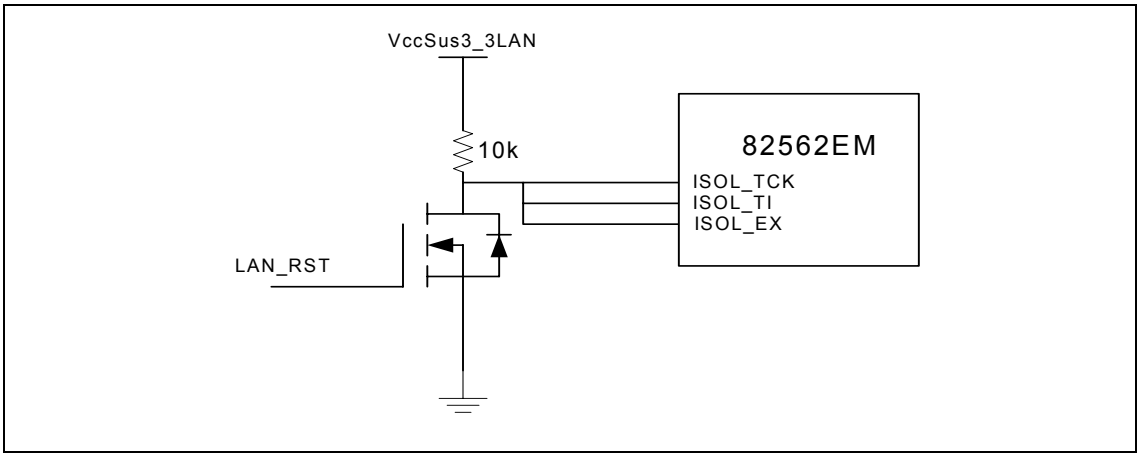
14.11.1. LAN Interface (82562ET / 82562EM)

14.11.1.1. Resistor Recommendations

LAN – Resistor Recommendations					
Pin Name	**System Pull up/Pull down**		**Series Damping**	**Notes**	✓
ISOL_EX, ISOL_TCK, ISOL_TI	Pull up to VccSus3_3LAN	10 k		All three signals are pulled up to VccSus3_3LAN through a common 10 kohms pull up resistor. See Figure 161	
RBIAS10	Pull down to GND	549 ± 1%			
RBIAS100	Pull down to GND	619 ±1%			
RDP, RDN	See Notes	121 ± 1%		Connect RDP to RDN through a 121ohms resistor	
TDP, TDN	See Notes	100 ± 1%		Connect TDP to TDN through a 100 +/ 1% resistor.	
TESTEN	Pull down to GND	100		This signal is pulled down to ground through a 100 in Intel CRB.	
X1 X2	See Notes			Connect a 25 MHz crystal across these two pins.	
LAN – Power Signals					
VCC[2:1], VCCP[2:1], VCCA[2:1], VCCT[4:1], VCCR[2:1]	Tie to VccSus3_3			Also see Section 11.1.2 for decoupling requirement.	
LAN – GND Signals					
VSS[5:1], VSSP[2:1], VSSA[2:1], VSSR[2:1]	Tie to GND				

NOTE: Default tolerance for resistors is +/-5% unless otherwise specified.

Figure 161. LAN_RST# Design Recommendation (On Intel CRB)



14.11.1.2. Decoupling Recommendations

LAN – Decoupling Recommendations[1]					
Signal Name	**Configuration**	**F**	**Qty**	**Notes**	**✓**
VccLan3_3	Pull down to GND	0.1 µF 4.7 µF	4 2		
VccLan_L3_3	Pull down to GND	0.1 µF 4.7 µF	1 1		
LAN_X1, LAN_X2	Pull down to GND	22 pF	1	Each pin requires a decoupling cap	

NOTE: All decoupling guidelines are recommendations based on our reference board design. Customers will need to take their layout, and PCB board design into consideration when deciding on their overall decoupling solution.

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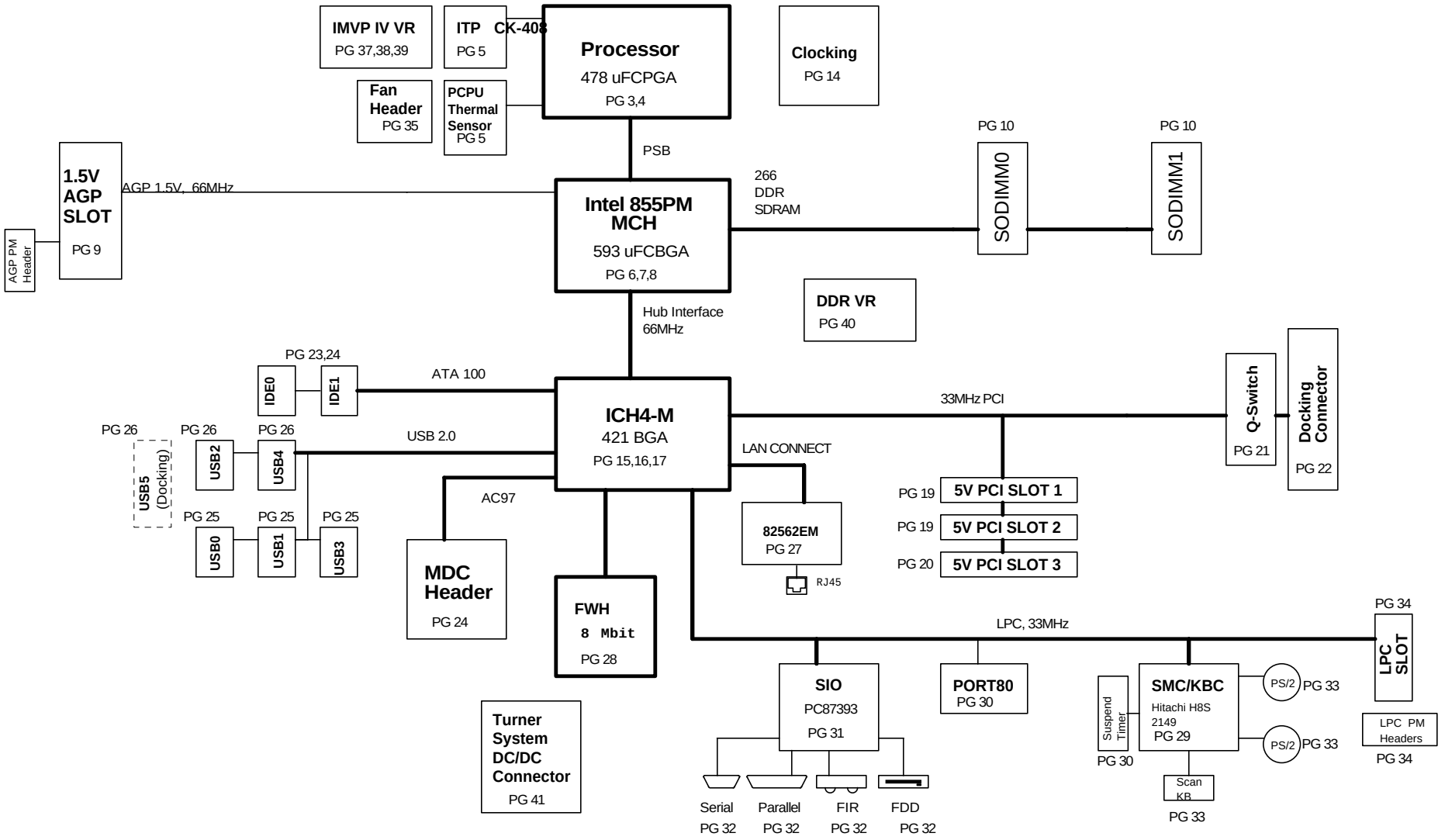
15. Intel Customer Reference Board Schematics

See the following page for customer reference board schematics.



Title: BLOCK DIAGRAM			
Size: A	Project: 855PM Platform	Document Number	Rev
Date: Monday, February 24, 2003		Sheet 1 of 4 7	

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

+VDC	Primary DC system power supply (10 to 21V)
+VCC_CORE	Core voltage for Processor
+VCCP	1.05V rail for Processor I/O
+V1.2S_MCH	1.2V For 855PM Core(off in S3-S5)
+V1.25	DDR Termination voltage(off in S4-S5)
+V1.5S	1.5V switched power rail (off in S3-S5)
+V1.5ALWAYS	1.5V always on power rail
+V1.5	1.5V power rail (off in S4-S5)
+V1.8S	1.8V switched power rail (off in S3-S5)
+V2.5	2.5V power rail for DDR
+V3.3ALWAYS	3.3V always on power rail
+V3.3	3.3V power rail (off in S4-S5)
+V3.3S	3.3V switched power rail (off in S3-S5)
+V5ALWAYS	5.0V always on power rail
+V5	5.0V power rail (off in S4-S5)
+V5S	5.0V switched power rail (off in S3-S5)
+V12S	12.0V switched power rail (off in S3-S5)
-V12S	-12.0V switched power rail for PCI (off in S3-S5)

PCI Devices

Device	IDSEL #	REQ/GNT #		Interrupts	PC/PCI
Slot 1	AD25	1	1	A, B, C, D	A
Slot 2	AD26	2	2	B, C, D, A	A
Slot 3	AD27	3	3	C, D, A, B	A
Docking	AD28	4	4	B, C, D, A	B
AGP	(AD17 internal)			A, B	
LAN	(AD24 internal)				

DDR Termination:

Command/Address/CS	BS#, RAS#, CAS#, WE#	1 Series and 1 Parallel
DATA	DQS, DATA, CB	1 Series and 1 Parallel
Control/Enable	CKE, CS#	1 Parallel

POWER STATES

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*	+V*S	Clocks
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend To Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

I²C / SMB Addresses

Device	Address	Hex	Bus
Clock Generator	1101 001x	D2	SMB_ICH
SO-DIMM0	1010 000x	A0	SMB_ICH
SO-DIMM1	1010 001x	A2	SMB_ICH
Thermal Diode	1001 110x	9C	SMB_THRM
Smart Battery	0001 011x	16	SMB_SB
Smart Battery Charger	0001 001x	12	SMB_SB
Smart Selector	0001 010x	14	SMB_SB

Net Name Suffix

\# = Active Low signal

LED	Page	Ref
SMC/KBC SCROLL LOCK	29	DS3
SMC/KBC NUMLOCK	29	DS1
SMC/KBC CAPS LOCK	29	DS4
Secondary IDE	24	DS7
Primary IDE	24	DS8
PWR/SUS LED	24	DS6
ON_BOARD_VR_PWRGD	38	DS2

SW	Page	Ref
VIRTUAL BATTERY	29	SW1
LID	29	SW2
POWER	40	SW3
RESET	40	SW4

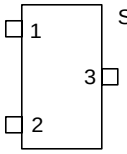
Default Jumper Settings			Page
J1	1-X	KBC 60/64 DECODE DISABLE	29
J6	1-X	INIT CLK DISABLE	30
J12	1-2	SMC/KBC DISABLE	29
J21	1-X	SMC/KBC Programming	29
J52	1-2	SIO Disable	31
J94	1-X	CMOS CLEAR	16

Wake Events

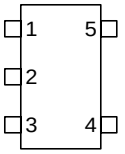
RI# (Ring Indicate) from serial port
PME# (Power Management Event) from
PCI/mini-PCI slots, AGP slot, LPC slot
LCI I/O from 82562EM
LID switch attached to SMC
USB
AC97 wake on ring
SmLink for AOL II
Hot Key from the scan matrix keyboard

PCB Footprints

As seen from top

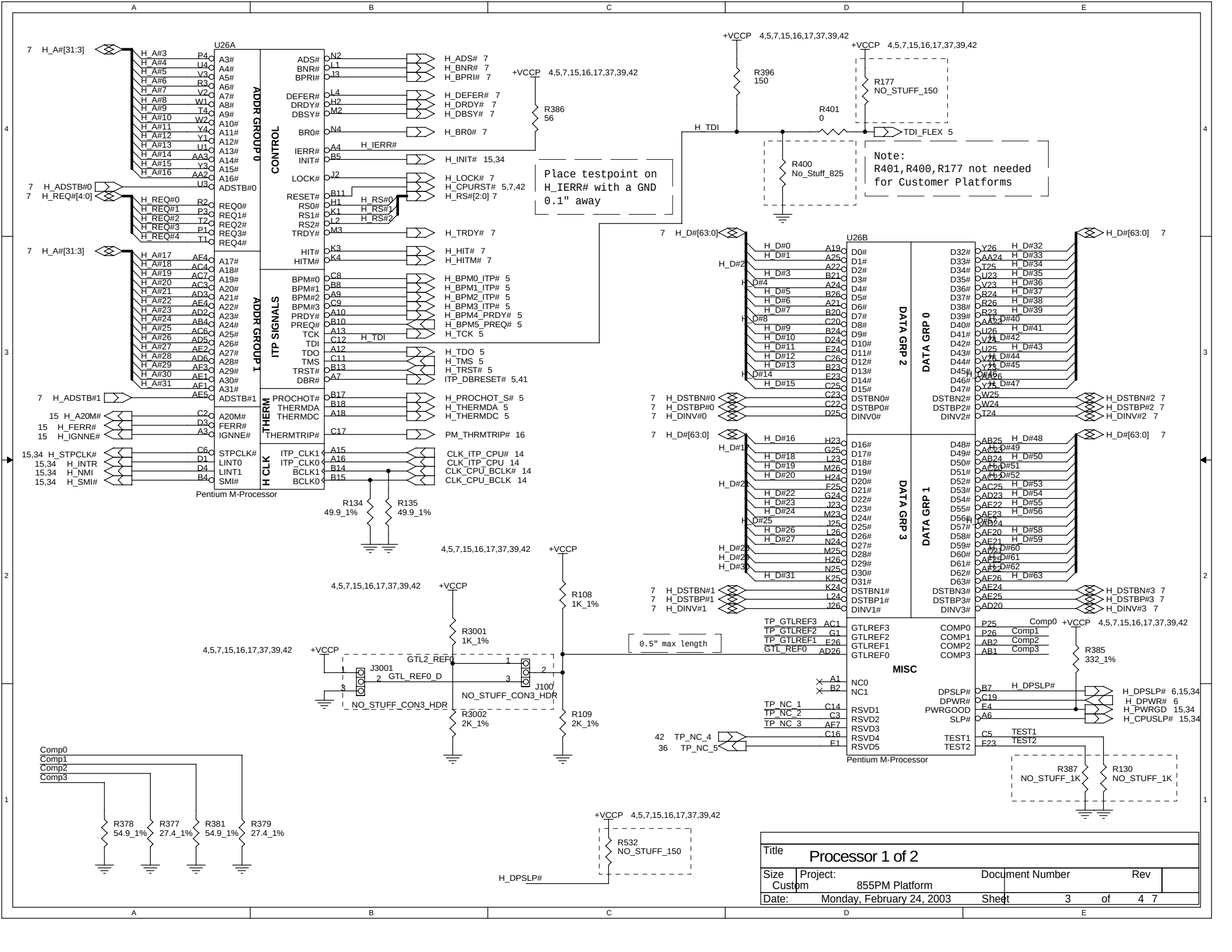


SOT-23



SOT23-5

Title: Notes and Annotations				
Size: A	Project: 855PM Platform	Document Number		Rev
Date: Monday, February 24, 2003	Sheet 2 of 47			


U26A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
ITP SIGNALS
THERM
H CLK
Pentium M-Processor
U26B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Pentium M-Processor
Place testpoint on H_IERR# with a GND 0.1" away
Note:
R401,R400,R177 not needed for Customer Platforms
0.5" max length
NO_STUFF_CON3_HDR
Comp0
Comp1
Comp2
Comp3
R378 54.9_1%
R377 27.4_1%
R381 54.9_1%
R379 27.4_1%
R532 NO_STUFF_150
R387 NO_STUFF_1K
R130 NO_STUFF_1K
Title
Processor 1 of 2
Size Custom
Project: 855PM Platform
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Rev
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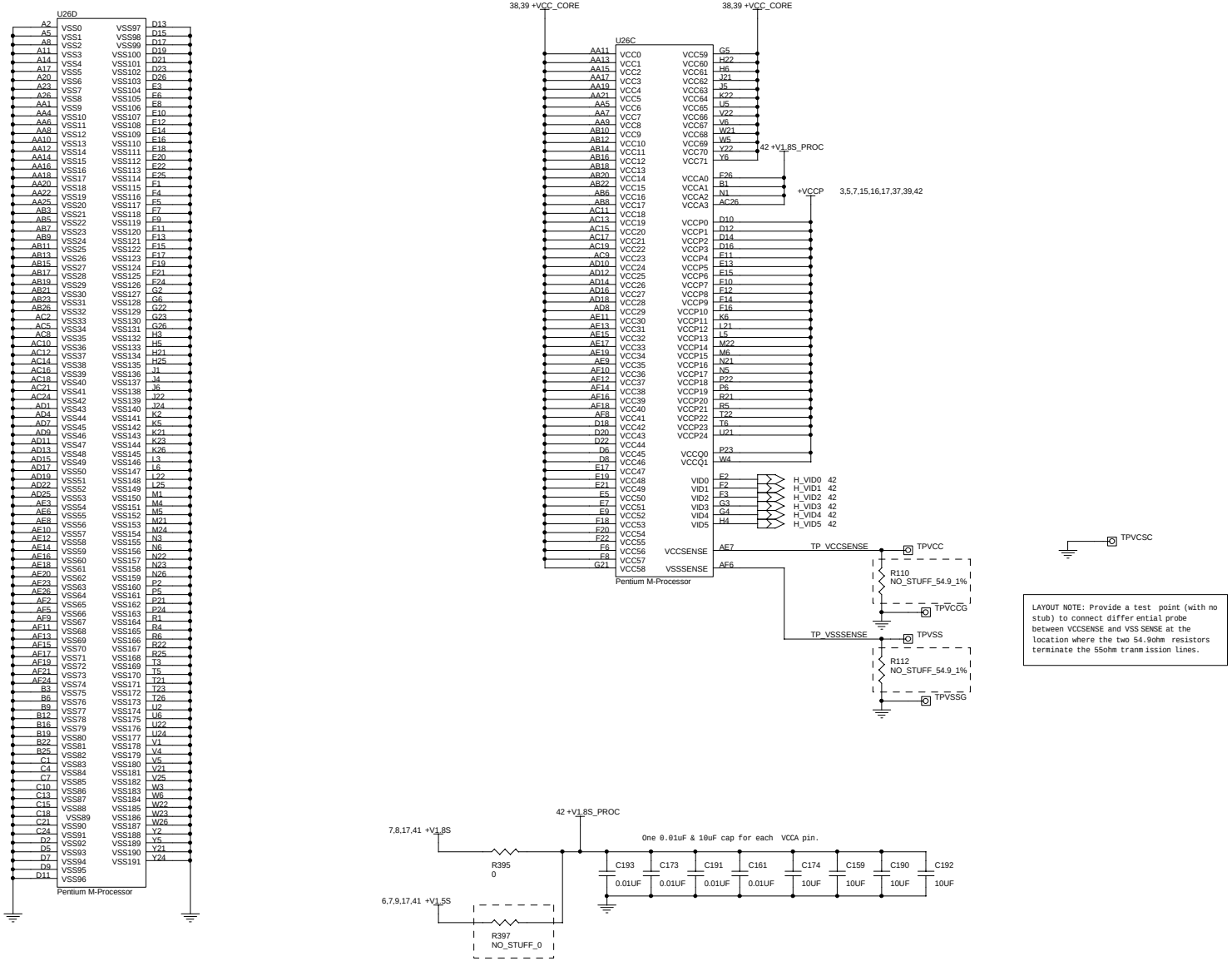
Sheet 3 of 4 7



Title	Processor 2 of 2		
Size A	Project: 855PM Platform	Document Number	Rev
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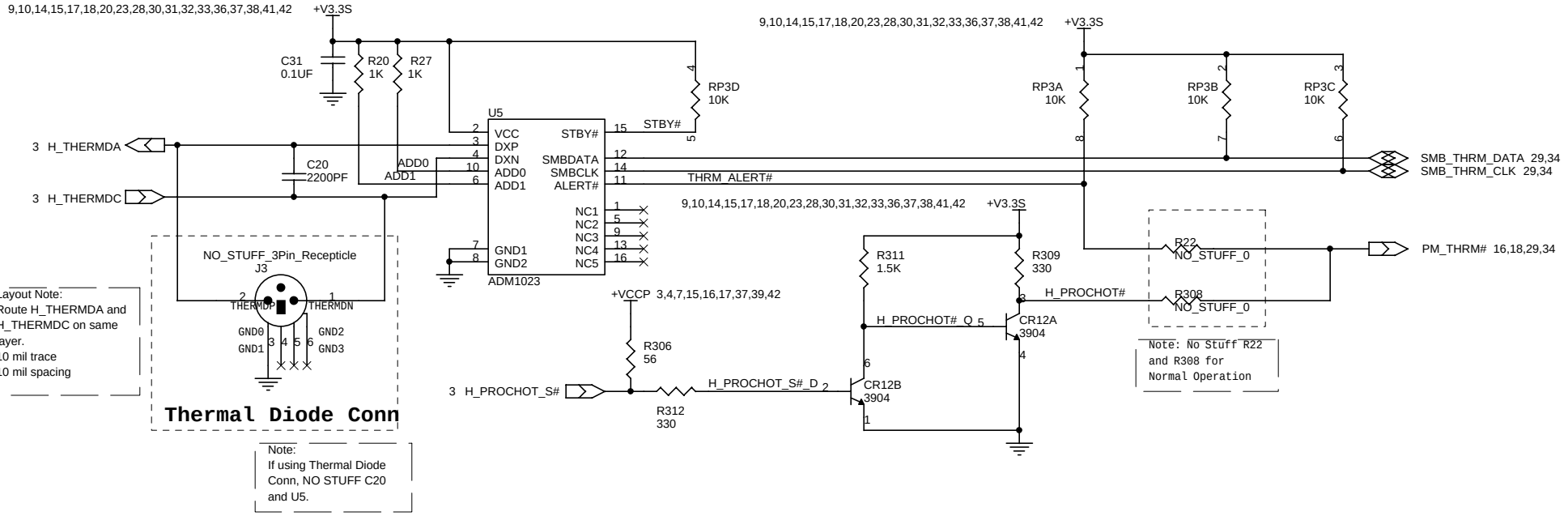
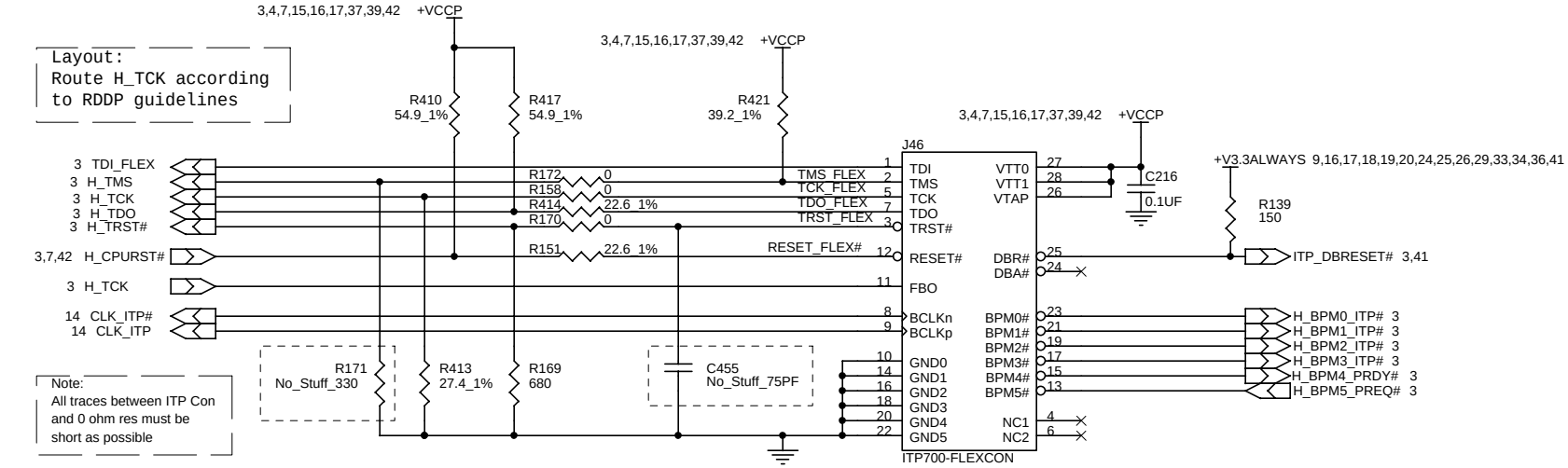
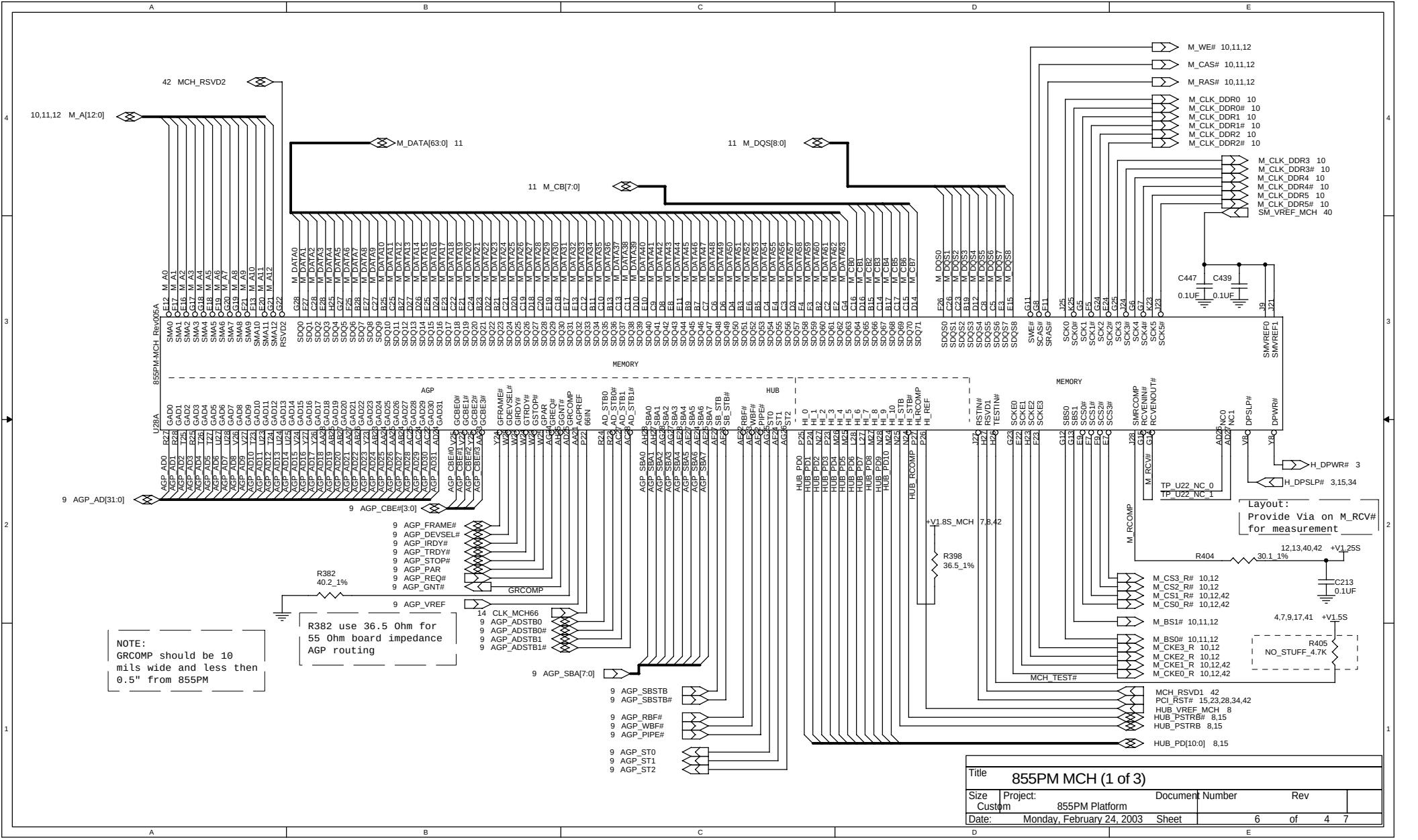
CPU Thermal Sensor





Title	Processor Thermal Sensor & ITP		
Size A	Project: 855PM Platform	Document Number	Rev
Date: Monday, February 24, 2003	Sheet 5 of 47		


42 MCH_RSVD2
10,11,12 M_A[12:0]
M_DATA[63:0] 11
11 M_DQS[8:0]
11 M_CB[7:0]
M_WE# 10,11,12
M_CAS# 10,11,12
M_RAS# 10,11,12
M_CLK_DDR0 10
M_CLK_DDR0# 10
M_CLK_DDR1 10
M_CLK_DDR1# 10
M_CLK_DDR2 10
M_CLK_DDR2# 10
M_CLK_DDR3 10
M_CLK_DDR3# 10
M_CLK_DDR4 10
M_CLK_DDR4# 10
M_CLK_DDR5 10
M_CLK_DDR5# 10
SM_VREF_MCH 40
C447 0.1UF
C439 0.1UF
855PM-MCH Rev005A
U28A
MEMORY
AGP
HUB
MEMORY
SM_VREF0
SM_VREF1
9 AGP_AD[31:0]
9 AGP_CBE#[3:0]
9 AGP_FRAME#
9 AGP_DEVSEL#
9 AGP_IRDY#
9 AGP_TRDY#
9 AGP_STOP#
9 AGP_PAR
9 AGP_REQ#
9 AGP_GNT#
9 AGP_VREF
R382 40.2_1%
GRCOMP
14 CLK_MCH66
9 AGP_ADSTB0
9 AGP_ADSTB0#
9 AGP_ADSTB1
9 AGP_ADSTB1#
9 AGP_SBA[7:0]
9 AGP_SBSTB
9 AGP_SBSTB#
9 AGP_RBF#
9 AGP_WBF#
9 AGP_PIPE#
9 AGP_ST0
9 AGP_ST1
9 AGP_ST2
HUB_PD[10:0]
HUB_RCOMP
HI_REF
+V1.8S_MCH 7,8,42
R398 36.5_1%
H_DPWR# 3
H_DPSLP# 3,15,34
TP_U22_NC_0
TP_U22_NC_1
M_RCOMP
M_RCV#
Layout:
Provide Via on M_RCV#
for measurement
12,13,40,42 +V1.25S
R404 30.1_1%
C213 0.1UF
4,7,9,17,41 +V1.5S
R405 NO_STUFF_4.7K
M_CS3_R# 10,12
M_CS2_R# 10,12
M_CS1_R# 10,12,42
M_CS0_R# 10,12,42
M_BS1# 10,11,12
M_BS0# 10,11,12
M_CKE3_R 10,12
M_CKE2_R 10,12
M_CKE1_R 10,12,42
M_CKE0_R 10,12,42
MCH_TEST#
MCH_RSVD1 42
PCI_RST# 15,23,28,34,42
HUB_VREF_MCH 8
HUB_PSTRB# 8,15
HUB_PSTRB 8,15
HUB_PD[10:0] 8,15
NOTE:
GRCOMP should be 10
mils wide and less then
0.5" from 855PM
R382 use 36.5 Ohm for
55 Ohm board impedance
AGP routing
Title
855PM MCH (1 of 3)
Size
Custom
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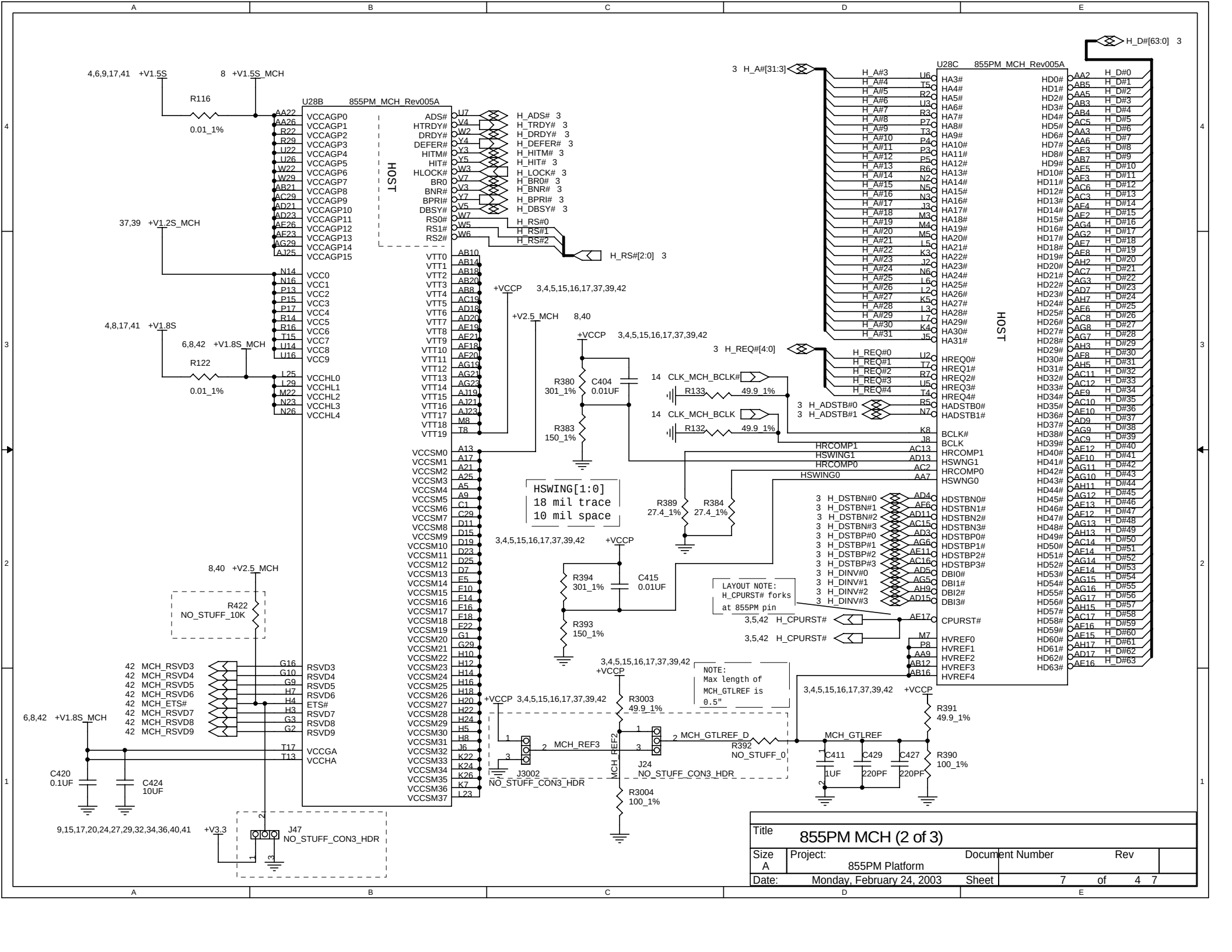
U28B 855PM_MCH_Rev005A
HOST
U28C 855PM_MCH_Rev005A
HOST
R116
0.01_1%
R122
0.01_1%
R380 301_1% C404 0.01UF
R383 150_1%
R394 301_1% C415 0.01UF
R393 150_1%
R389 27.4_1%
R384 27.4_1%
R133 49.9_1%
R132 49.9_1%
R422 NO_STUFF_10K
R3003 49.9_1%
R3004 100_1%
R391 49.9_1%
R392 NO_STUFF_0
R390 100_1%
C420 0.1UF
C424 10UF
C411 1UF
C429 220PF
C427 220PF
J3002 NO_STUFF_CON3_HDR
J24 NO_STUFF_CON3_HDR
J47 NO_STUFF_CON3_HDR
HSWING[1:0]
18 mil trace
10 mil space
LAYOUT NOTE:
H_CPURST# forks
at 855PM pin
NOTE:
Max length of
MCH_GTLREF is
0.5"
Title
855PM MCH (2 of 3)
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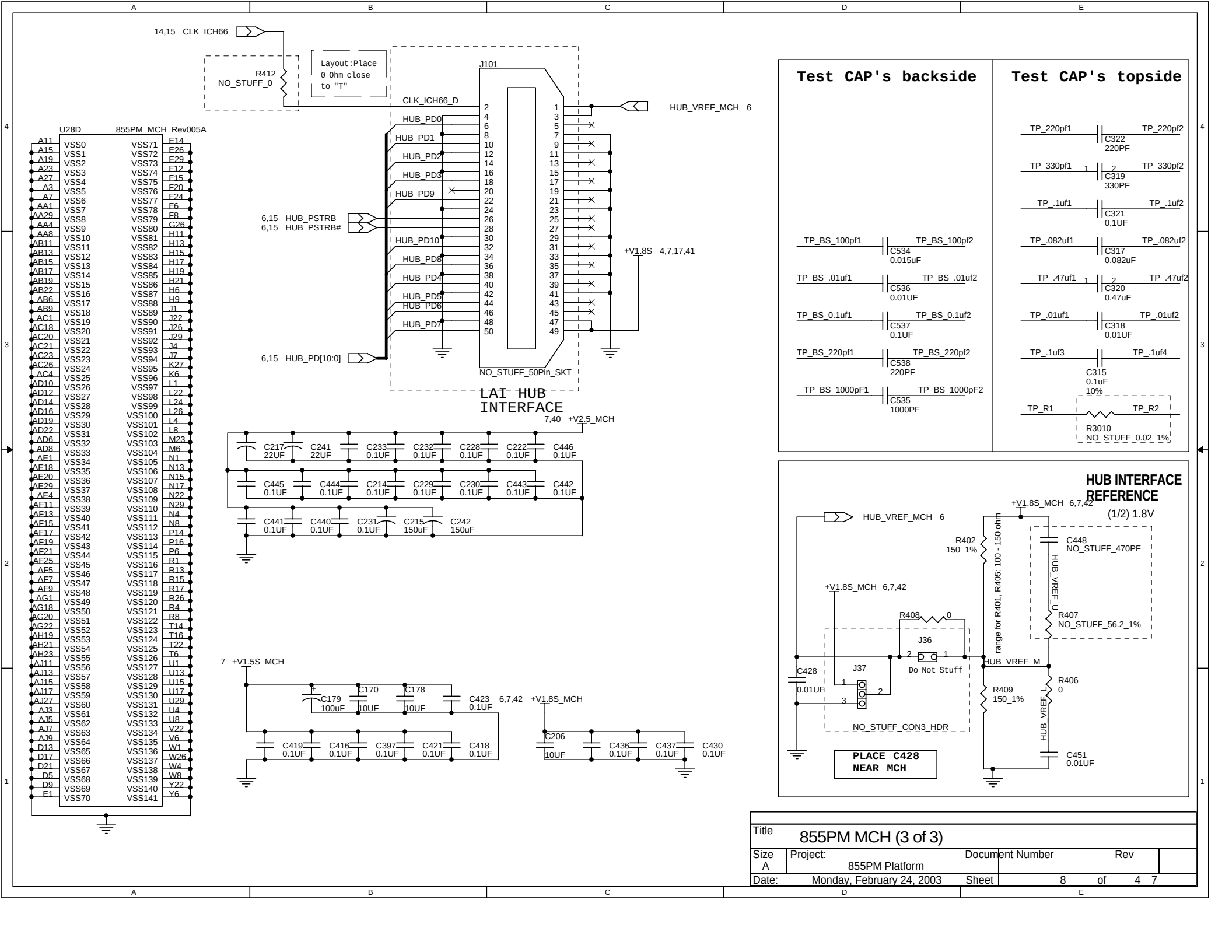

Title	855PM MCH (3 of 3)		
Size A	Project: 855PM Platform	Document Number	Rev
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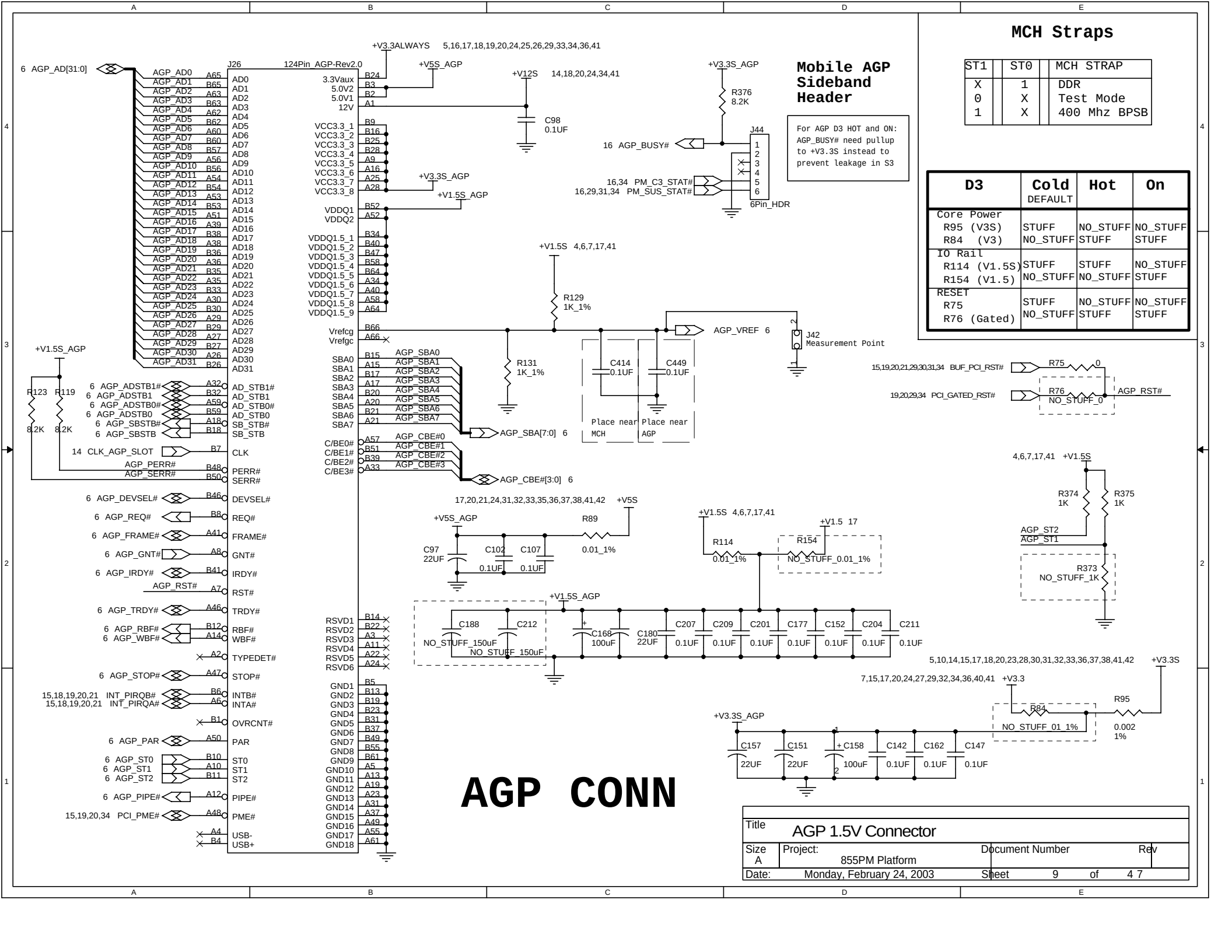
MCH Straps
ST1 | ST0 | MCH STRAP
X | 1 | DDR
0 | X | Test Mode
1 | X | 400 Mhz BPSB
Mobile AGP Sideband Header
For AGP D3 HOT and ON: AGP_BUSY# need pullup to +V3.3S instead to prevent leakage in S3
D3 | Cold DEFAULT | Hot | On
Core Power
R95 (V3S) | STUFF | NO_STUFF | NO_STUFF
R84 (V3) | NO_STUFF | STUFF | STUFF
IO Rail
R114 (V1.5S) | STUFF | STUFF | NO_STUFF
R154 (V1.5) | NO_STUFF | NO_STUFF | STUFF
RESET
R75 | STUFF | NO_STUFF | NO_STUFF
R76 (Gated) | NO_STUFF | STUFF | STUFF
J26
124Pin_AGP-Rev2.0
J44
6Pin_HDR
J42
Measurement Point
AGP_AD[31:0]
AGP_SBA[7:0]
AGP_CBE#[3:0]
AGP_VREF
AGP_RST#
Place near MCH
Place near AGP
AGP CONN
Title
AGP 1.5V Connector
Size A
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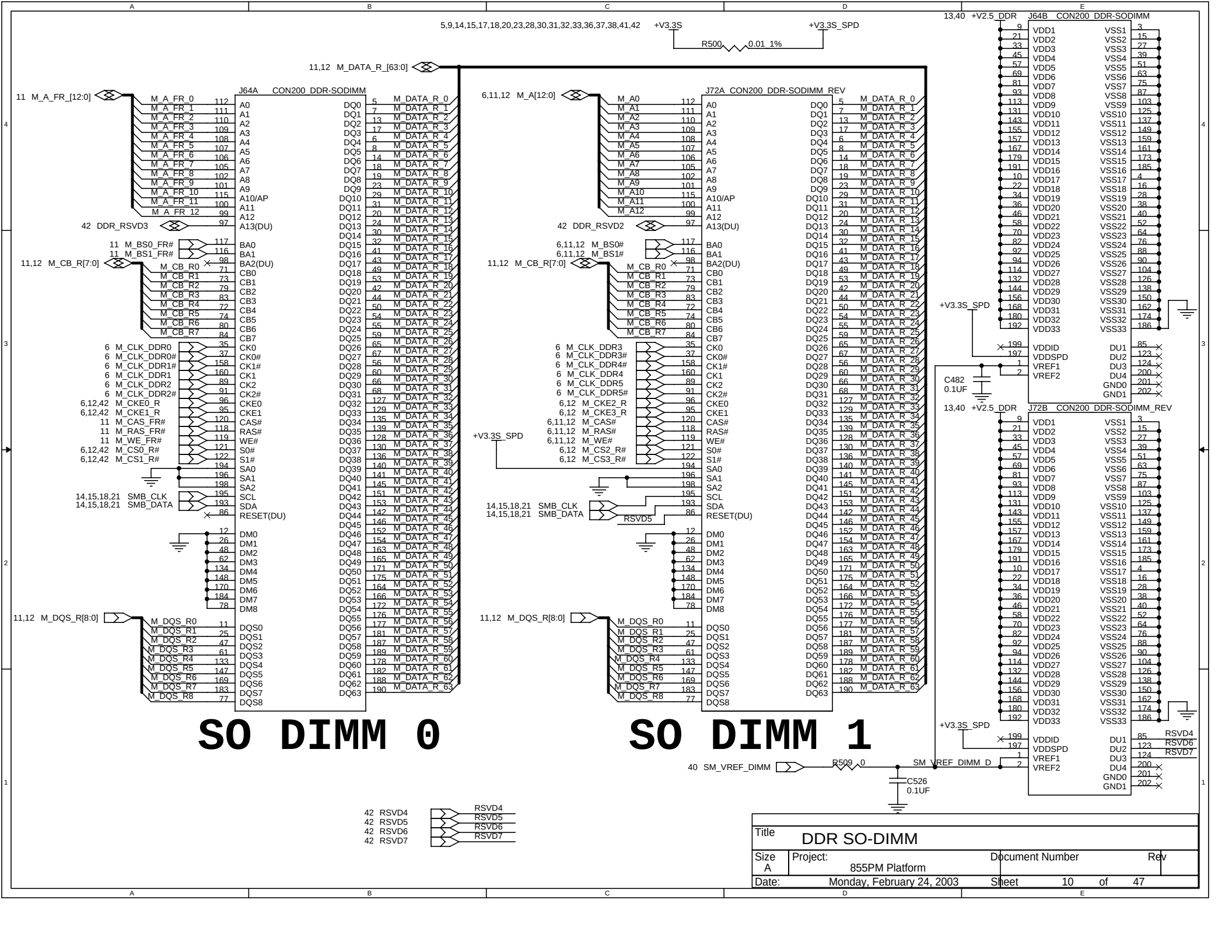
5,9,14,15,17,18,20,23,28,30,31,32,33,36,37,38,41,42
+V3.3S
+V3.3S_SPD
R500
0.01 1%
11,12 M_DATA_R_[63:0]
J64A CON200_DDR-SODIMM
11 M_A_FR_[12:0]
M_A_FR_0
M_A_FR_1
M_A_FR_2
M_A_FR_3
M_A_FR_4
M_A_FR_5
M_A_FR_6
M_A_FR_7
M_A_FR_8
M_A_FR_9
M_A_FR_10
M_A_FR_11
M_A_FR_12
42 DDR_RSVD3
11 M_BS0_FR#
11 M_BS1_FR#
11,12 M_CB_R[7:0]
M_CB_R0
M_CB_R1
M_CB_R2
M_CB_R3
M_CB_R4
M_CB_R5
M_CB_R6
M_CB_R7
6 M_CLK_DDR0
6 M_CLK_DDR0#
6 M_CLK_DDR1#
6 M_CLK_DDR1
6 M_CLK_DDR2
6 M_CLK_DDR2#
6,12,42 M_CKE0_R
6,12,42 M_CKE1_R
11 M_CAS_FR#
11 M_RAS_FR#
11 M_WE_FR#
6,12,42 M_CS0_R#
6,12,42 M_CS1_R#
14,15,18,21 SMB_CLK
14,15,18,21 SMB_DATA
11,12 M_DQS_R[8:0]
M_DQS_R0
M_DQS_R1
M_DQS_R2
M_DQS_R3
M_DQS_R4
M_DQS_R5
M_DQS_R6
M_DQS_R7
M_DQS_R8
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12
A13(DU)
BA0
BA1
BA2(DU)
CB0
CB1
CB2
CB3
CB4
CB5
CB6
CB7
CK0
CK0#
CK1#
CK1
CK2
CK2#
CKE0
CKE1
CAS#
RAS#
WE#
S0#
S1#
SA0
SA1
SA2
SCL
SDA
RESET(DU)
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
DM8
DQS0
DQS1
DQS2
DQS3
DQS4
DQS5
DQS6
DQS7
DQS8
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
DQ36
DQ37
DQ38
DQ39
DQ40
DQ41
DQ42
DQ43
DQ44
DQ45
DQ46
DQ47
DQ48
DQ49
DQ50
DQ51
DQ52
DQ53
DQ54
DQ55
DQ56
DQ57
DQ58
DQ59
DQ60
DQ61
DQ62
DQ63
M_DATA_R_0
M_DATA_R_1
M_DATA_R_2
M_DATA_R_3
M_DATA_R_4
M_DATA_R_5
M_DATA_R_6
M_DATA_R_7
M_DATA_R_8
M_DATA_R_9
M_DATA_R_10
M_DATA_R_11
M_DATA_R_12
M_DATA_R_13
M_DATA_R_14
M_DATA_R_15
M_DATA_R_16
M_DATA_R_17
M_DATA_R_18
M_DATA_R_19
M_DATA_R_20
M_DATA_R_21
M_DATA_R_22
M_DATA_R_23
M_DATA_R_24
M_DATA_R_25
M_DATA_R_26
M_DATA_R_27
M_DATA_R_28
M_DATA_R_29
M_DATA_R_30
M_DATA_R_31
M_DATA_R_32
M_DATA_R_33
M_DATA_R_34
M_DATA_R_35
M_DATA_R_36
M_DATA_R_37
M_DATA_R_38
M_DATA_R_39
M_DATA_R_40
M_DATA_R_41
M_DATA_R_42
M_DATA_R_43
M_DATA_R_44
M_DATA_R_45
M_DATA_R_46
M_DATA_R_47
M_DATA_R_48
M_DATA_R_49
M_DATA_R_50
M_DATA_R_51
M_DATA_R_52
M_DATA_R_53
M_DATA_R_54
M_DATA_R_55
M_DATA_R_56
M_DATA_R_57
M_DATA_R_58
M_DATA_R_59
M_DATA_R_60
M_DATA_R_61
M_DATA_R_62
M_DATA_R_63
SO DIMM 0
6,11,12 M_A[12:0]
J72A CON200_DDR-SODIMM_REV
42 DDR_RSVD2
6,11,12 M_BS0#
6,11,12 M_BS1#
11,12 M_CB_R[7:0]
6 M_CLK_DDR3
6 M_CLK_DDR3#
6 M_CLK_DDR4#
6 M_CLK_DDR4
6 M_CLK_DDR5
6 M_CLK_DDR5#
6,12 M_CKE2_R
6,12 M_CKE3_R
6,11,12 M_CAS#
6,11,12 M_RAS#
6,11,12 M_WE#
6,12 M_CS2_R#
6,12 M_CS3_R#
+V3.3S_SPD
14,15,18,21 SMB_CLK
14,15,18,21 SMB_DATA
RSVD5
11,12 M_DQS_R[8:0]
SO DIMM 1
13,40 +V2.5_DDR
J64B CON200_DDR-SODIMM
+V3.3S_SPD
C482
0.1UF
13,40 +V2.5_DDR
J72B CON200_DDR-SODIMM_REV
+V3.3S_SPD
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDD10
VDD11
VDD12
VDD13
VDD14
VDD15
VDD16
VDD17
VDD18
VDD19
VDD20
VDD21
VDD22
VDD23
VDD24
VDD25
VDD26
VDD27
VDD28
VDD29
VDD30
VDD31
VDD32
VDD33
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
VSS19
VSS20
VSS21
VSS22
VSS23
VSS24
VSS25
VSS26
VSS27
VSS28
VSS29
VSS30
VSS31
VSS32
VSS33
VDDID
VDDSPD
VREF1
VREF2
DU1
DU2
DU3
DU4
GND0
GND1
40 SM_VREF_DIMM
R509 0
SM_VREF_DIMM_D
C526
0.1UF
42 RSVD4
42 RSVD5
42 RSVD6
42 RSVD7
RSVD4
RSVD5
RSVD6
RSVD7
Title
DDR SO-DIMM
Size
A
Project:
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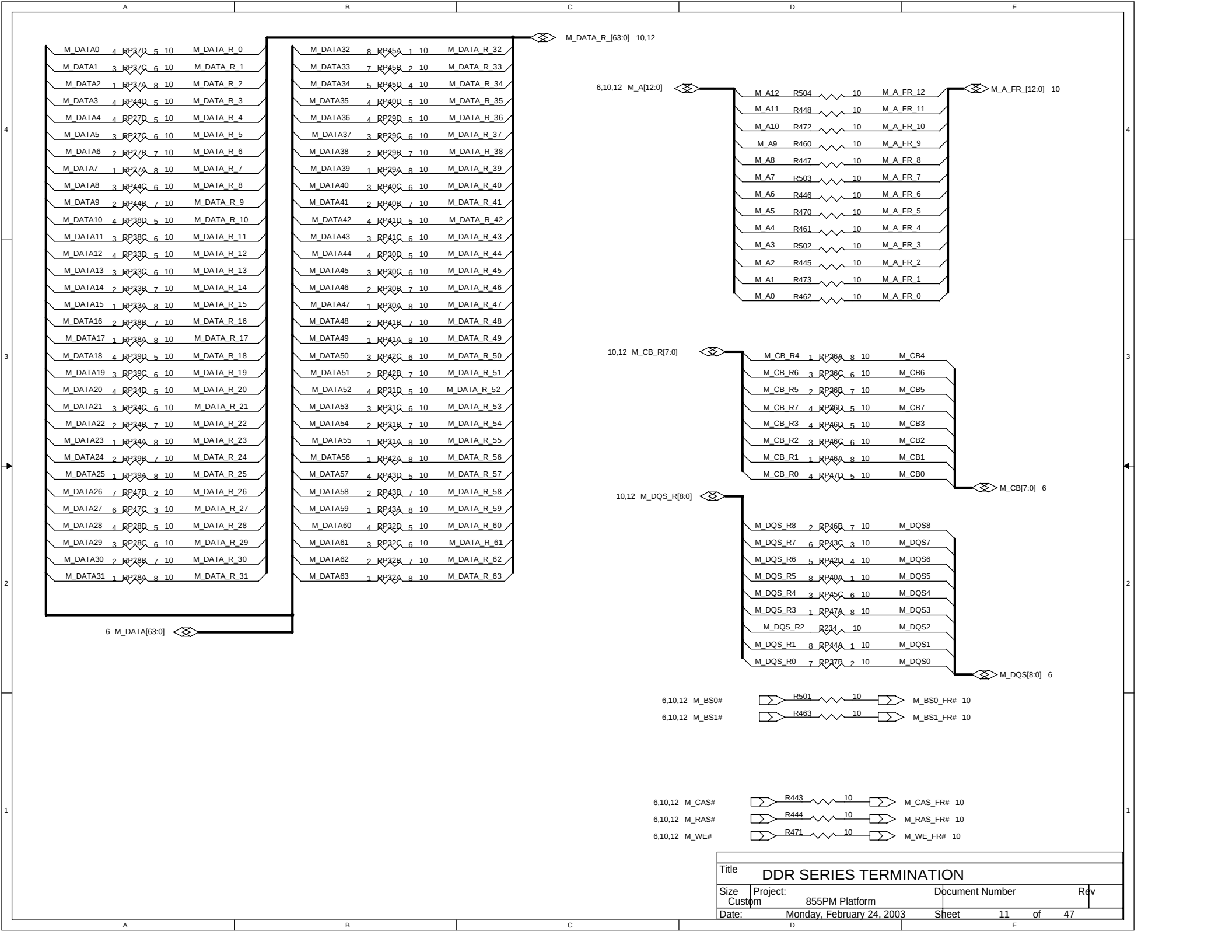
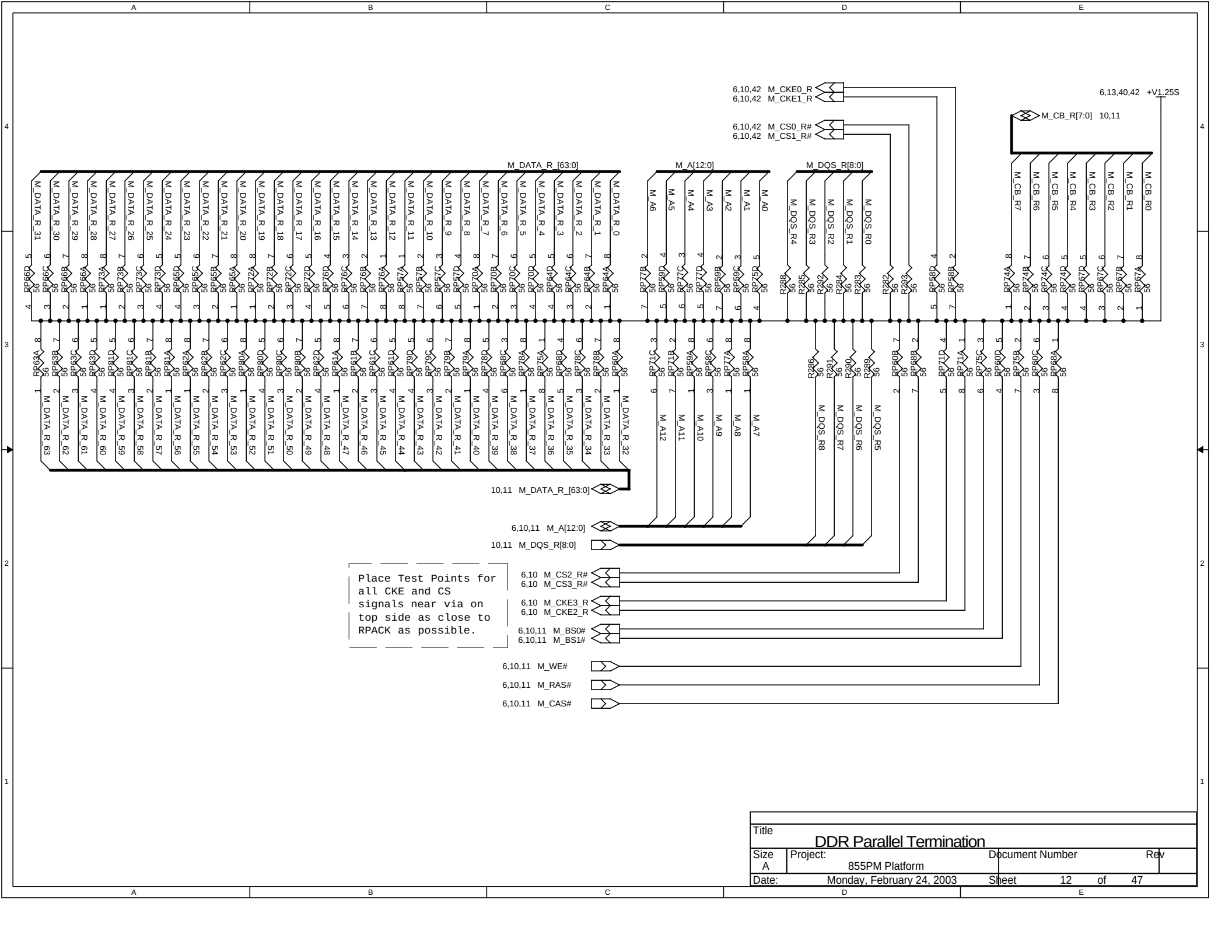

M_DATA0 4 RP37D 5 10 M_DATA_R_0
M_DATA1 3 RP37C 6 10 M_DATA_R_1
M_DATA2 1 RP37A 8 10 M_DATA_R_2
M_DATA3 4 RP44D 5 10 M_DATA_R_3
M_DATA4 4 RP27D 5 10 M_DATA_R_4
M_DATA5 3 RP27C 6 10 M_DATA_R_5
M_DATA6 2 RP27B 7 10 M_DATA_R_6
M_DATA7 1 RP27A 8 10 M_DATA_R_7
M_DATA8 3 RP44C 6 10 M_DATA_R_8
M_DATA9 2 RP44B 7 10 M_DATA_R_9
M_DATA10 4 RP38D 5 10 M_DATA_R_10
M_DATA11 3 RP38C 6 10 M_DATA_R_11
M_DATA12 4 RP33D 5 10 M_DATA_R_12
M_DATA13 3 RP33C 6 10 M_DATA_R_13
M_DATA14 2 RP33B 7 10 M_DATA_R_14
M_DATA15 1 RP33A 8 10 M_DATA_R_15
M_DATA16 2 RP38B 7 10 M_DATA_R_16
M_DATA17 1 RP38A 8 10 M_DATA_R_17
M_DATA18 4 RP39D 5 10 M_DATA_R_18
M_DATA19 3 RP39C 6 10 M_DATA_R_19
M_DATA20 4 RP34D 5 10 M_DATA_R_20
M_DATA21 3 RP34C 6 10 M_DATA_R_21
M_DATA22 2 RP34B 7 10 M_DATA_R_22
M_DATA23 1 RP34A 8 10 M_DATA_R_23
M_DATA24 2 RP29B 7 10 M_DATA_R_24
M_DATA25 1 RP29A 8 10 M_DATA_R_25
M_DATA26 7 RP47B 2 10 M_DATA_R_26
M_DATA27 6 RP47C 3 10 M_DATA_R_27
M_DATA28 4 RP28D 5 10 M_DATA_R_28
M_DATA29 3 RP28C 6 10 M_DATA_R_29
M_DATA30 2 RP28B 7 10 M_DATA_R_30
M_DATA31 1 RP28A 8 10 M_DATA_R_31
M_DATA32 8 RP45A 1 10 M_DATA_R_32
M_DATA33 7 RP45B 2 10 M_DATA_R_33
M_DATA34 5 RP45D 4 10 M_DATA_R_34
M_DATA35 4 RP40D 5 10 M_DATA_R_35
M_DATA36 4 RP29D 5 10 M_DATA_R_36
M_DATA37 3 RP29C 6 10 M_DATA_R_37
M_DATA38 2 RP29B 7 10 M_DATA_R_38
M_DATA39 1 RP29A 8 10 M_DATA_R_39
M_DATA40 3 RP40C 6 10 M_DATA_R_40
M_DATA41 2 RP40B 7 10 M_DATA_R_41
M_DATA42 4 RP41D 5 10 M_DATA_R_42
M_DATA43 3 RP41C 6 10 M_DATA_R_43
M_DATA44 4 RP30D 5 10 M_DATA_R_44
M_DATA45 3 RP30C 6 10 M_DATA_R_45
M_DATA46 2 RP30B 7 10 M_DATA_R_46
M_DATA47 1 RP30A 8 10 M_DATA_R_47
M_DATA48 2 RP41B 7 10 M_DATA_R_48
M_DATA49 1 RP41A 8 10 M_DATA_R_49
M_DATA50 3 RP42C 6 10 M_DATA_R_50
M_DATA51 2 RP42B 7 10 M_DATA_R_51
M_DATA52 4 RP31D 5 10 M_DATA_R_52
M_DATA53 3 RP31C 6 10 M_DATA_R_53
M_DATA54 2 RP31B 7 10 M_DATA_R_54
M_DATA55 1 RP31A 8 10 M_DATA_R_55
M_DATA56 1 RP42A 8 10 M_DATA_R_56
M_DATA57 4 RP43D 5 10 M_DATA_R_57
M_DATA58 2 RP43B 7 10 M_DATA_R_58
M_DATA59 1 RP43A 8 10 M_DATA_R_59
M_DATA60 4 RP32D 5 10 M_DATA_R_60
M_DATA61 3 RP32C 6 10 M_DATA_R_61
M_DATA62 2 RP32B 7 10 M_DATA_R_62
M_DATA63 1 RP32A 8 10 M_DATA_R_63
M_DATA_R_[63:0] 10,12
6 M_DATA[63:0]
6,10,12 M_A[12:0]
M_A12 R504 10 M_A_FR_12
M_A11 R448 10 M_A_FR_11
M_A10 R472 10 M_A_FR_10
M_A9 R460 10 M_A_FR_9
M_A8 R447 10 M_A_FR_8
M_A7 R503 10 M_A_FR_7
M_A6 R446 10 M_A_FR_6
M_A5 R470 10 M_A_FR_5
M_A4 R461 10 M_A_FR_4
M_A3 R502 10 M_A_FR_3
M_A2 R445 10 M_A_FR_2
M_A1 R473 10 M_A_FR_1
M_A0 R462 10 M_A_FR_0
M_A_FR_[12:0] 10
10,12 M_CB_R[7:0]
M_CB_R4 1 RP36A 8 10 M_CB4
M_CB_R6 3 RP36C 6 10 M_CB6
M_CB_R5 2 RP36B 7 10 M_CB5
M_CB_R7 4 RP36D 5 10 M_CB7
M_CB_R3 4 RP46D 5 10 M_CB3
M_CB_R2 3 RP46C 6 10 M_CB2
M_CB_R1 1 RP46A 8 10 M_CB1
M_CB_R0 4 RP47D 5 10 M_CB0
M_CB[7:0] 6
10,12 M_DQS_R[8:0]
M_DQS_R8 2 RP46B 7 10 M_DQS8
M_DQS_R7 6 RP43C 3 10 M_DQS7
M_DQS_R6 5 RP42D 4 10 M_DQS6
M_DQS_R5 8 RP40A 1 10 M_DQS5
M_DQS_R4 3 RP45C 6 10 M_DQS4
M_DQS_R3 1 RP47A 8 10 M_DQS3
M_DQS_R2 R234 10 M_DQS2
M_DQS_R1 8 RP44A 1 10 M_DQS1
M_DQS_R0 7 RP27B 2 10 M_DQS0
M_DQS[8:0] 6
6,10,12 M_BS0#
R501 10 M_BS0_FR# 10
6,10,12 M_BS1#
R463 10 M_BS1_FR# 10
6,10,12 M_CAS#
R443 10 M_CAS_FR# 10
6,10,12 M_RAS#
R444 10 M_RAS_FR# 10
6,10,12 M_WE#
R471 10 M_WE_FR# 10
Title
DDR SERIES TERMINATION
Size
Custom
Project:
855PM Platform
Document Number
Rev
Date:
Monday, February 24, 2003
Sheet 11 of 47


6,10,42 M_CKE0_R
6,10,42 M_CKE1_R
6,10,42 M_CS0_R#
6,10,42 M_CS1_R#
6,13,40,42 +V1.25S
M_CB_R[7:0] 10,11
M_DATA_R_[63:0]
M_A[12:0]
M_DQS_R[8:0]
10,11 M_DATA_R_[63:0]
6,10,11 M_A[12:0]
10,11 M_DQS_R[8:0]
6,10 M_CS2_R#
6,10 M_CS3_R#
6,10 M_CKE3_R
6,10 M_CKE2_R
6,10,11 M_BS0#
6,10,11 M_BS1#
6,10,11 M_WE#
6,10,11 M_RAS#
6,10,11 M_CAS#
Place Test Points for all CKE and CS signals near via on top side as close to RPACK as possible.
Title
DDR Parallel Termination
Size A
Project: 855PM Platform
Document Number
Rev
Date: Monday, February 24, 2003
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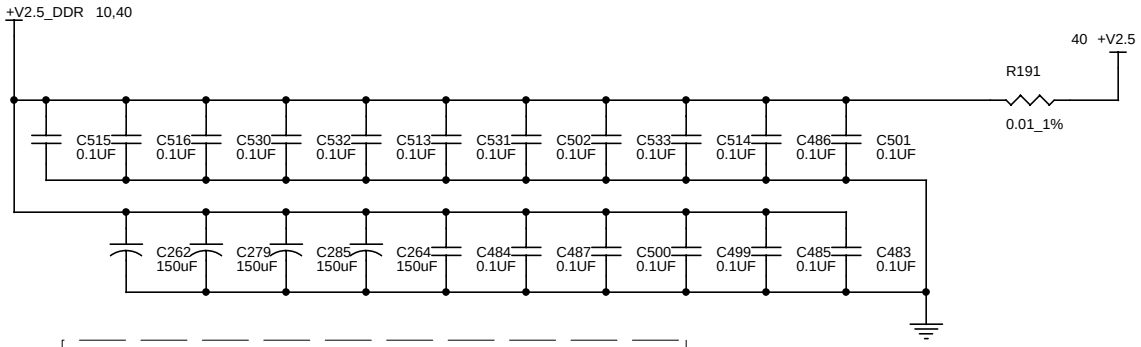
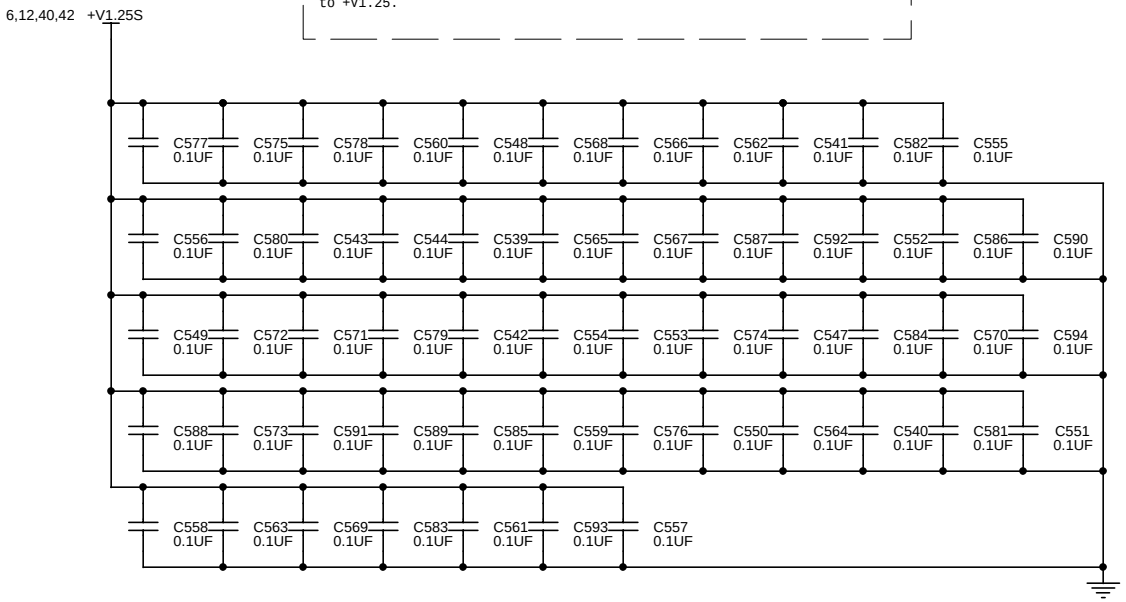
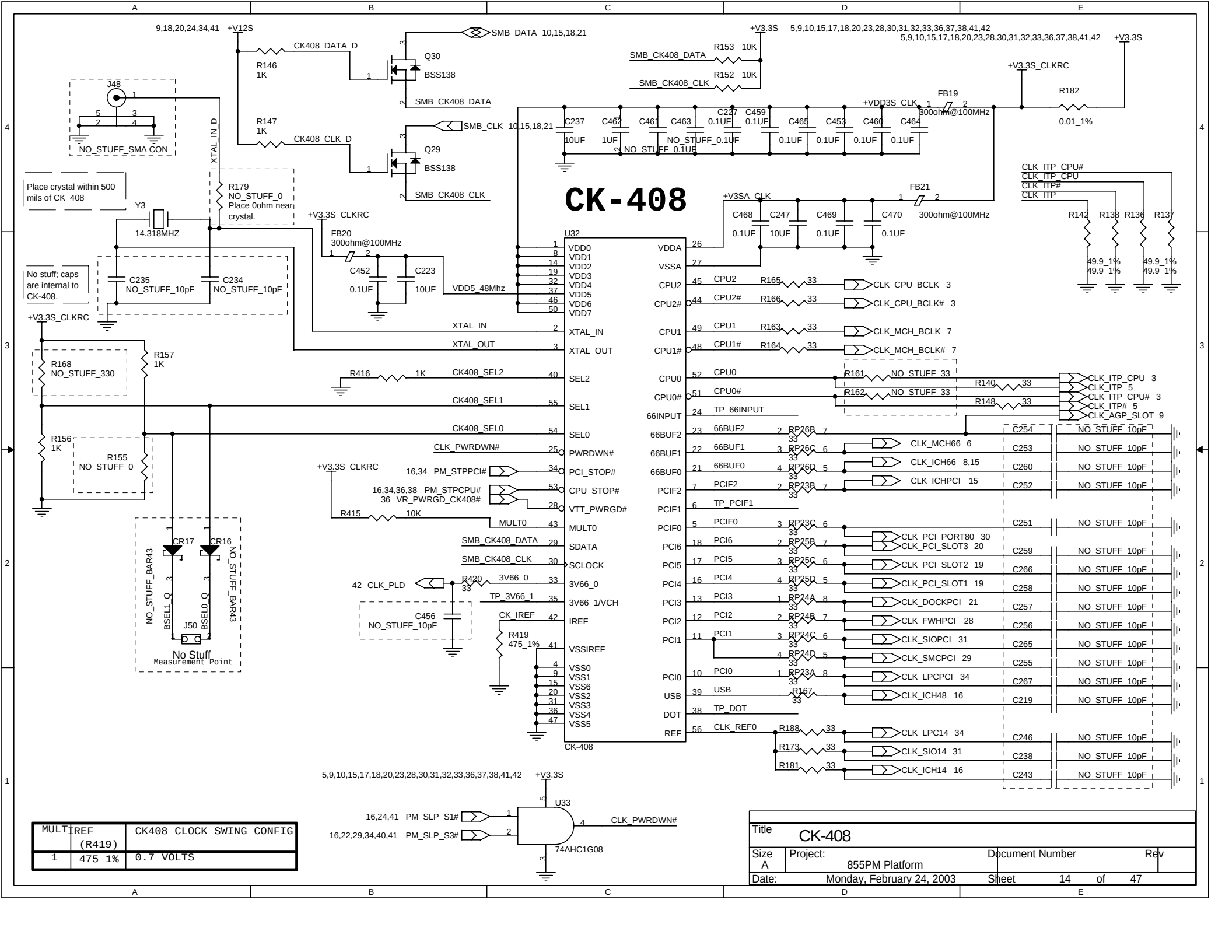


Layout note: Place capacitors between and near DDR connector if possible.

Layout note: Place one cap close to every 2 pullup resistors terminated to +V1.25.



Title	DDR Decoupling		
Size A	Project: 855PM Platform	Document Number	Rev
Date: Monday, February 24, 2003		Sheet 13 of 47	


CK-408
U32
CK-408
U33
74AHC1G08
Place crystal within 500 mils of CK_408
No stuff; caps are internal to CK-408.
Place 0ohm near crystal.
No Stuff
Measurement Point
NO_STUFF_SMA CON
NO_STUFF_BAR43
MULTI
IREF (R419)
CK408 CLOCK SWING CONFIG
1
475 1%
0.7 VOLTS
Title
CK-408
Size A
Project: 855PM Platform
Document Number
Rev
Date: Monday, February 24, 2003
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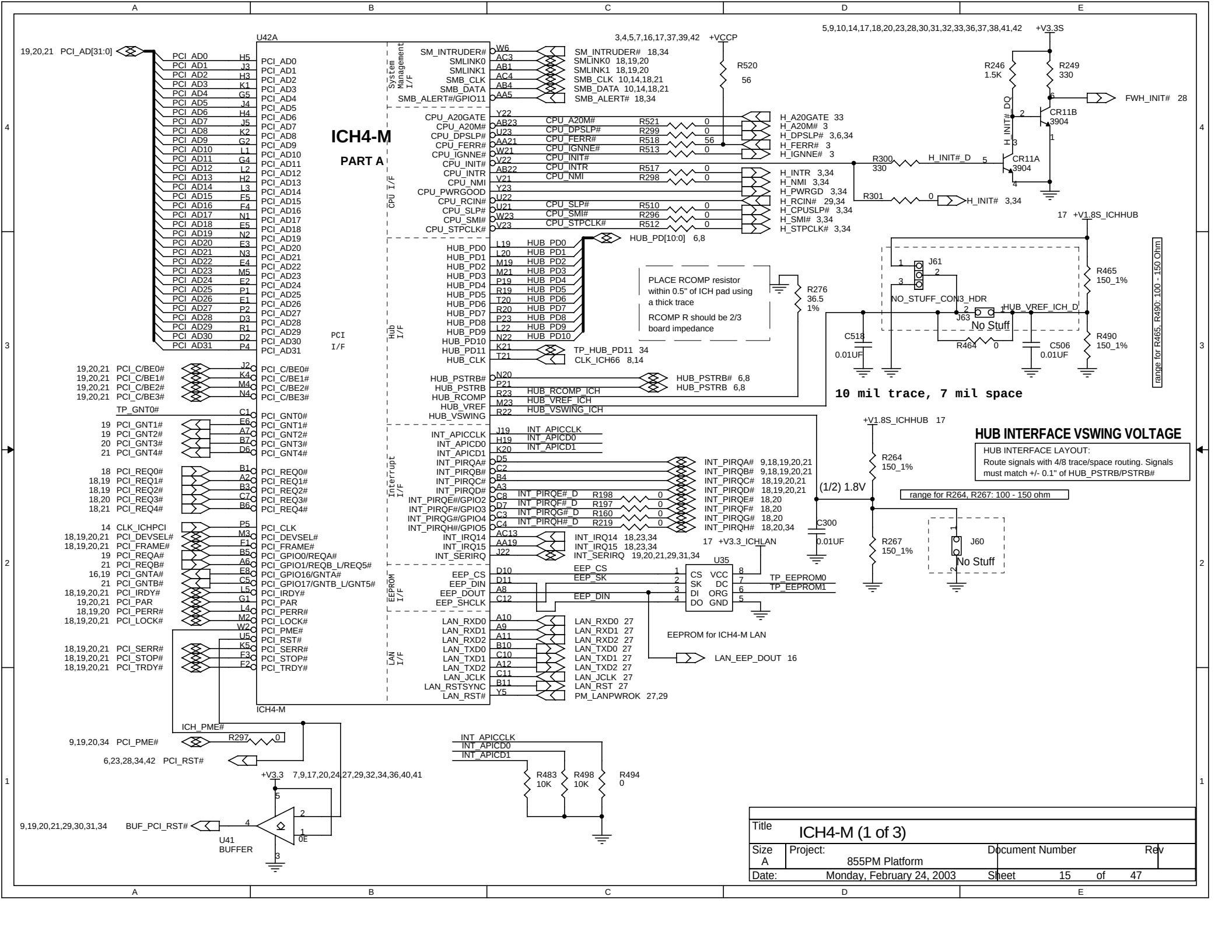
ICH4-M
PART A
U42A
PCI I/F
System Management I/F
CPU I/F
Hub I/F
Interrupt I/F
EEPROM I/F
LAN I/F
HUB INTERFACE VSWING VOLTAGE
HUB INTERFACE LAYOUT:
Route signals with 4/8 trace/space routing. Signals must match +/- 0.1" of HUB_PSTRB/PSTRB#
PLACE RCOMP resistor within 0.5" of ICH pad using a thick trace
RCOMP R should be 2/3 board impedance
10 mil trace, 7 mil space
range for R465, R490: 100 - 150 Ohm
range for R264, R267: 100 - 150 ohm
No Stuff
EEPROM for ICH4-M LAN
U35
U41
BUFFER
Title
ICH4-M (1 of 3)
Size A
Project:
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Rev
Date:
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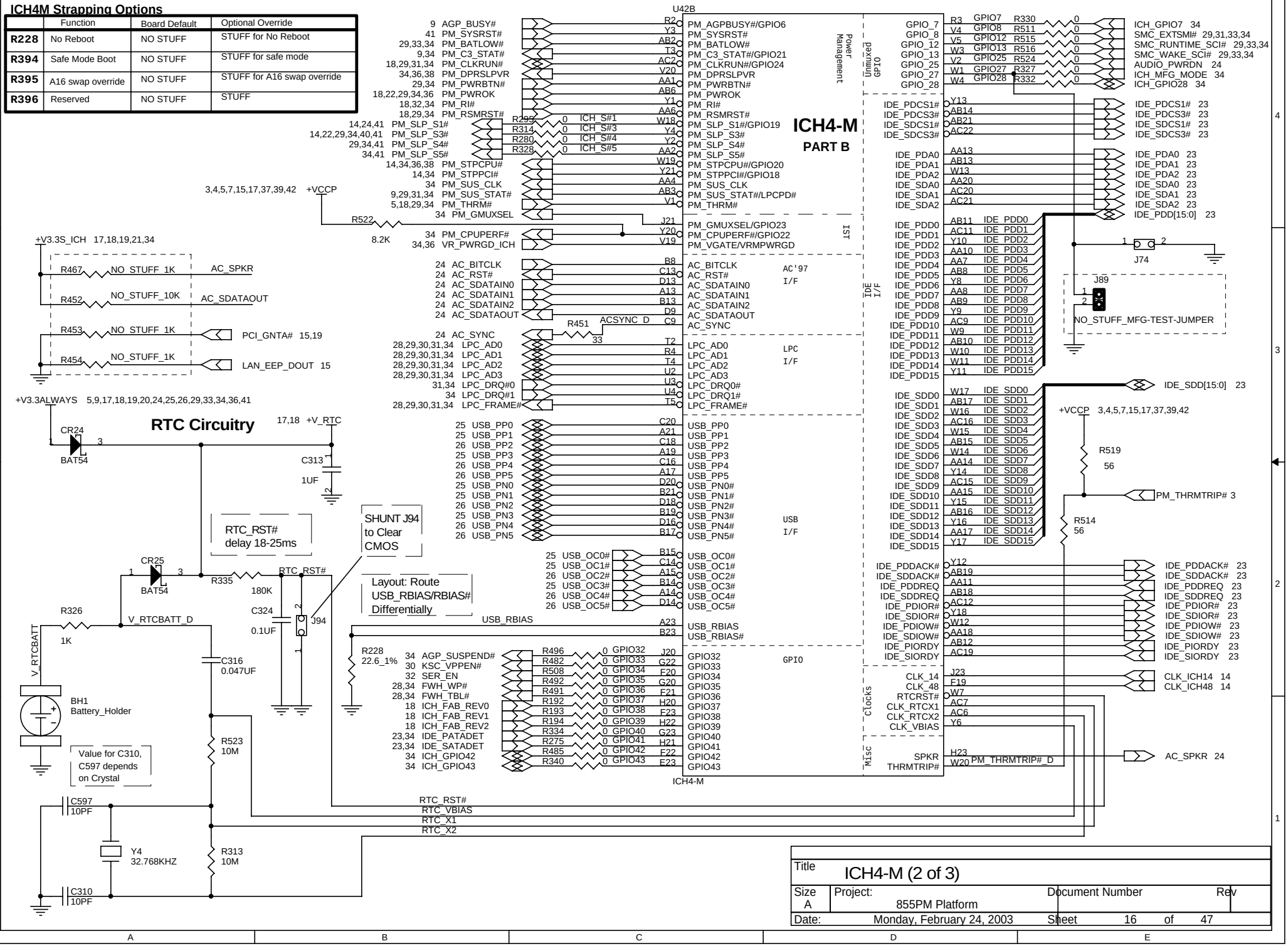
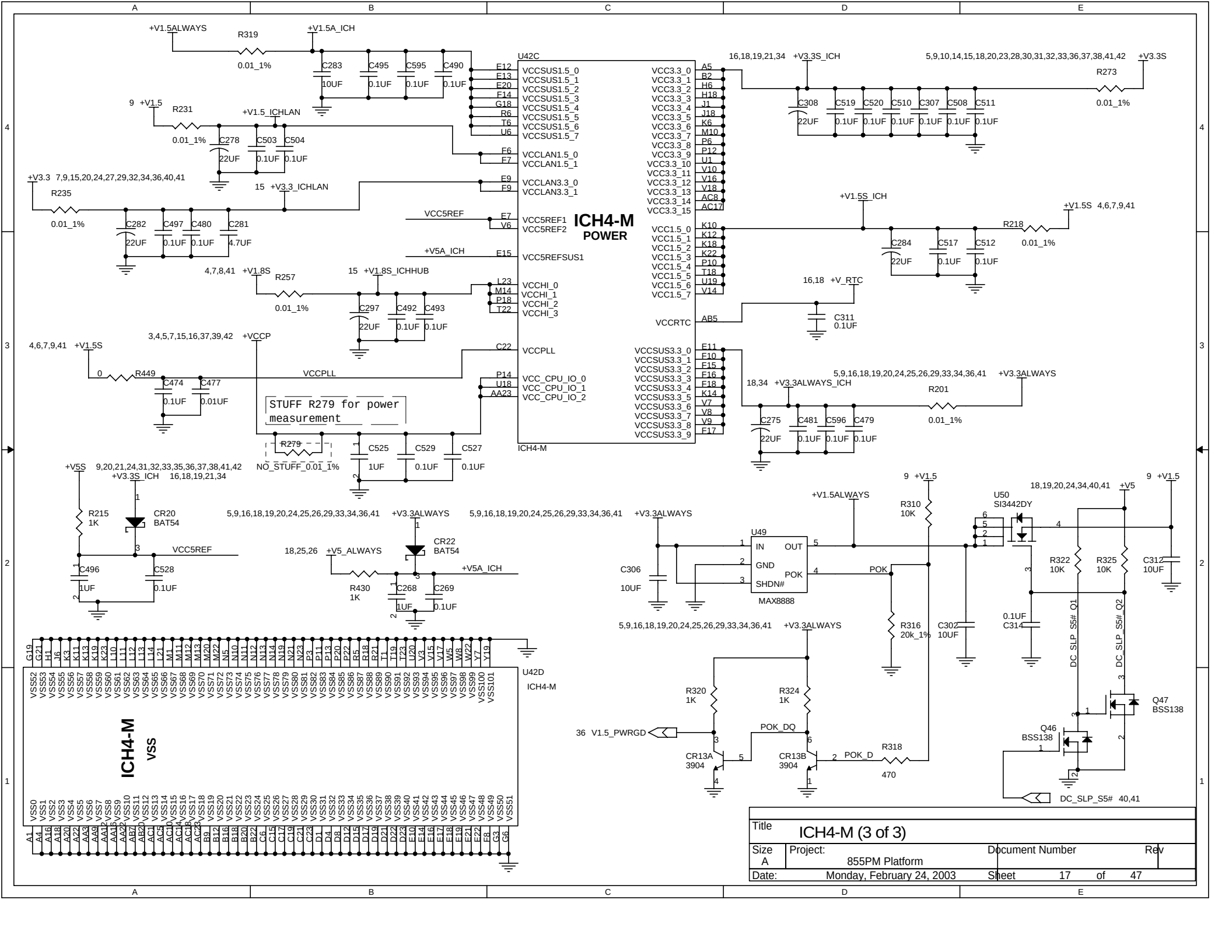
ICH4M Strapping Options

	Function	Board Default	Optional Override
R228	No Reboot	NO STUFF	STUFF for No Reboot
R394	Safe Mode Boot	NO STUFF	STUFF for safe mode
R395	A16 swap override	NO STUFF	STUFF for A16 swap override
R396	Reserved	NO STUFF	STUFF




+V1.5ALWAYS
R319
+V1.5A_ICH
0.01_1%
C283 10UF
C495 0.1UF
C595 0.1UF
C490 0.1UF
U42C
VCCSUS1.5_0
VCCSUS1.5_1
VCCSUS1.5_2
VCCSUS1.5_3
VCCSUS1.5_4
VCCSUS1.5_5
VCCSUS1.5_6
VCCSUS1.5_7
VCCLAN1.5_0
VCCLAN1.5_1
VCCLAN3.3_0
VCCLAN3.3_1
VCC5REF1
VCC5REF2
VCC5REFSUS1
VCCHI_0
VCCHI_1
VCCHI_2
VCCHI_3
VCCPLL
VCC_CPU_IO_0
VCC_CPU_IO_1
VCC_CPU_IO_2
ICH4-M
POWER
VCC3.3_0
VCC3.3_1
VCC3.3_2
VCC3.3_3
VCC3.3_4
VCC3.3_5
VCC3.3_6
VCC3.3_7
VCC3.3_8
VCC3.3_9
VCC3.3_10
VCC3.3_11
VCC3.3_12
VCC3.3_13
VCC3.3_14
VCC3.3_15
VCC1.5_0
VCC1.5_1
VCC1.5_2
VCC1.5_3
VCC1.5_4
VCC1.5_5
VCC1.5_6
VCC1.5_7
VCCRTC
VCCSUS3.3_0
VCCSUS3.3_1
VCCSUS3.3_2
VCCSUS3.3_3
VCCSUS3.3_4
VCCSUS3.3_5
VCCSUS3.3_6
VCCSUS3.3_7
VCCSUS3.3_8
VCCSUS3.3_9
16,18,19,21,34 +V3.3S_ICH
5,9,10,14,15,18,20,23,28,30,31,32,33,36,37,38,41,42 +V3.3S
R273
0.01_1%
C308 22UF
C519 0.1UF
C520 0.1UF
C510 0.1UF
C307 0.1UF
C508 0.1UF
C511 0.1UF
9 +V1.5
R231
+V1.5_ICHLAN
0.01_1%
C278 22UF
C503 0.1UF
C504 0.1UF
+V3.3 7,9,15,20,24,27,29,32,34,36,40,41
R235
15 +V3.3_ICHLAN
0.01_1%
C282 22UF
C497 0.1UF
C480 0.1UF
C281 4.7UF
+V1.5S_ICH
+V1.5S 4,6,7,9,41
R218
0.01_1%
C284 22UF
C517 0.1UF
C512 0.1UF
16,18 +V_RTC
C311 0.1UF
4,7,8,41 +V1.8S
R257
15 +V1.8S_ICHHUB
0.01_1%
C297 22UF
C492 0.1UF
C493 0.1UF
3,4,5,7,15,16,37,39,42 +VCCP
4,6,7,9,41 +V1.5S
0
R449
VCCPLL
C474 0.1UF
C477 0.01UF
STUFF R279 for power measurement
R279
NO_STUFF_0.01_1%
C525 1UF
C529 0.1UF
C527 0.1UF
5,9,16,18,19,20,24,25,26,29,33,34,36,41 +V3.3ALWAYS_ICH
18,34 +V3.3ALWAYS_ICH
R201
0.01_1%
C275 22UF
C481 0.1UF
C596 0.1UF
C479 0.1UF
+V5S
9,20,21,24,31,32,33,35,36,37,38,41,42
+V3.3S_ICH 16,18,19,21,34
R215 1K
CR20 BAT54
VCC5REF
C496 1UF
C528 0.1UF
5,9,16,18,19,20,24,25,26,29,33,34,36,41 +V3.3ALWAYS
18,25,26 +V5_ALWAYS
CR22 BAT54
+V5A_ICH
R430 1K
C268 1UF
C269 0.1UF
5,9,16,18,19,20,24,25,26,29,33,34,36,41 +V3.3ALWAYS
U49
IN
GND
SHDN#
OUT
POK
MAX8888
C306 10UF
+V1.5ALWAYS
9 +V1.5
R310 10K
18,19,20,24,34,40,41 +V5
9 +V1.5
U50
SI3442DY
R322 10K
R325 10K
C312 10UF
C302 10UF
R316 20k_1%
0.1UF C314
DC_SLP_S5#_Q1
DC_SLP_S5#_Q2
5,9,16,18,19,20,24,25,26,29,33,34,36,41 +V3.3ALWAYS
R320 1K
R324 1K
36 V1.5_PWRGD
POK_DQ
CR13A 3904
CR13B 3904
POK_D
R318 470
Q47 BSS138
Q46 BSS138
DC_SLP_S5# 40,41
U42D
ICH4-M
VSS
G19 G21 H1 J6 K3 K11 K13 K19 K23 L10 L11 L12 L13 L14 L21 M1 M11 M12 M13 M20 M22 N5 N10 N11 N12 N13 N14 N19 N21 N23 P3 P11 P13 P20 P22 R5 R18 R21 T1 T19 T23 U20 V3 V15 V17 W5 W8 W22 Y7 Y19
VSS52 VSS53 VSS54 VSS55 VSS56 VSS57 VSS58 VSS59 VSS60 VSS61 VSS62 VSS63 VSS64 VSS65 VSS66 VSS67 VSS68 VSS69 VSS70 VSS71 VSS72 VSS73 VSS74 VSS75 VSS76 VSS77 VSS78 VSS79 VSS80 VSS81 VSS82 VSS83 VSS84 VSS85 VSS86 VSS87 VSS88 VSS89 VSS90 VSS91 VSS92 VSS93 VSS94 VSS95 VSS96 VSS97 VSS98 VSS99 VSS100 VSS101
VSS0 VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51
A1 A4 A16 A18 A20 A22 A3 A9 A11 A13 AB7 AB2 AC1 AC5 AC10 AC14 AC18 AC23 B9 B12 B16 B18 B20 B22 C6 C15 C17 C19 C21 C23 D1 D4 D8 D12 D15 D17 D19 D21 D22 D23 E10 E14 E16 E17 E18 E19 E21 E22 F8 G3 G6
Title ICH4-M (3 of 3)
Size A
Project: 855PM Platform
Document Number
Rev
Date: Monday, February 24, 2003
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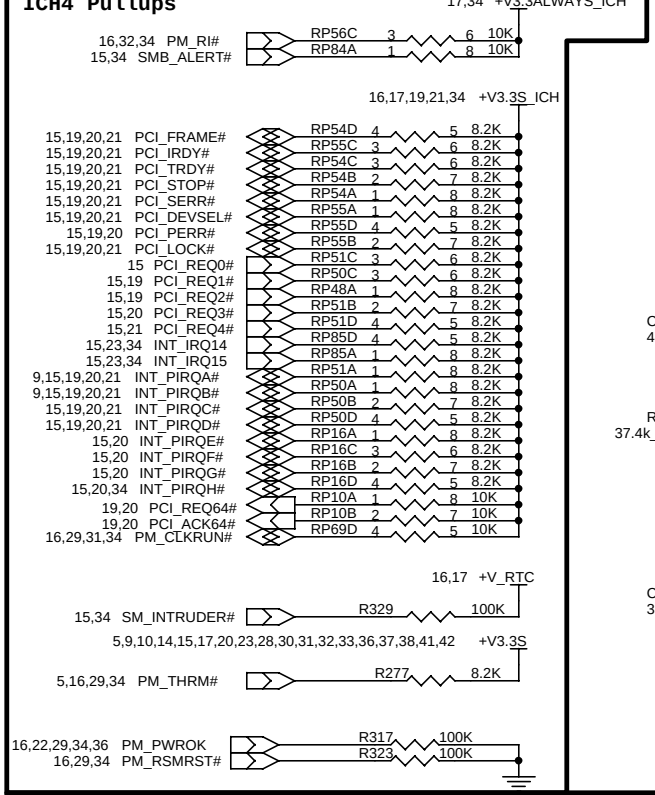
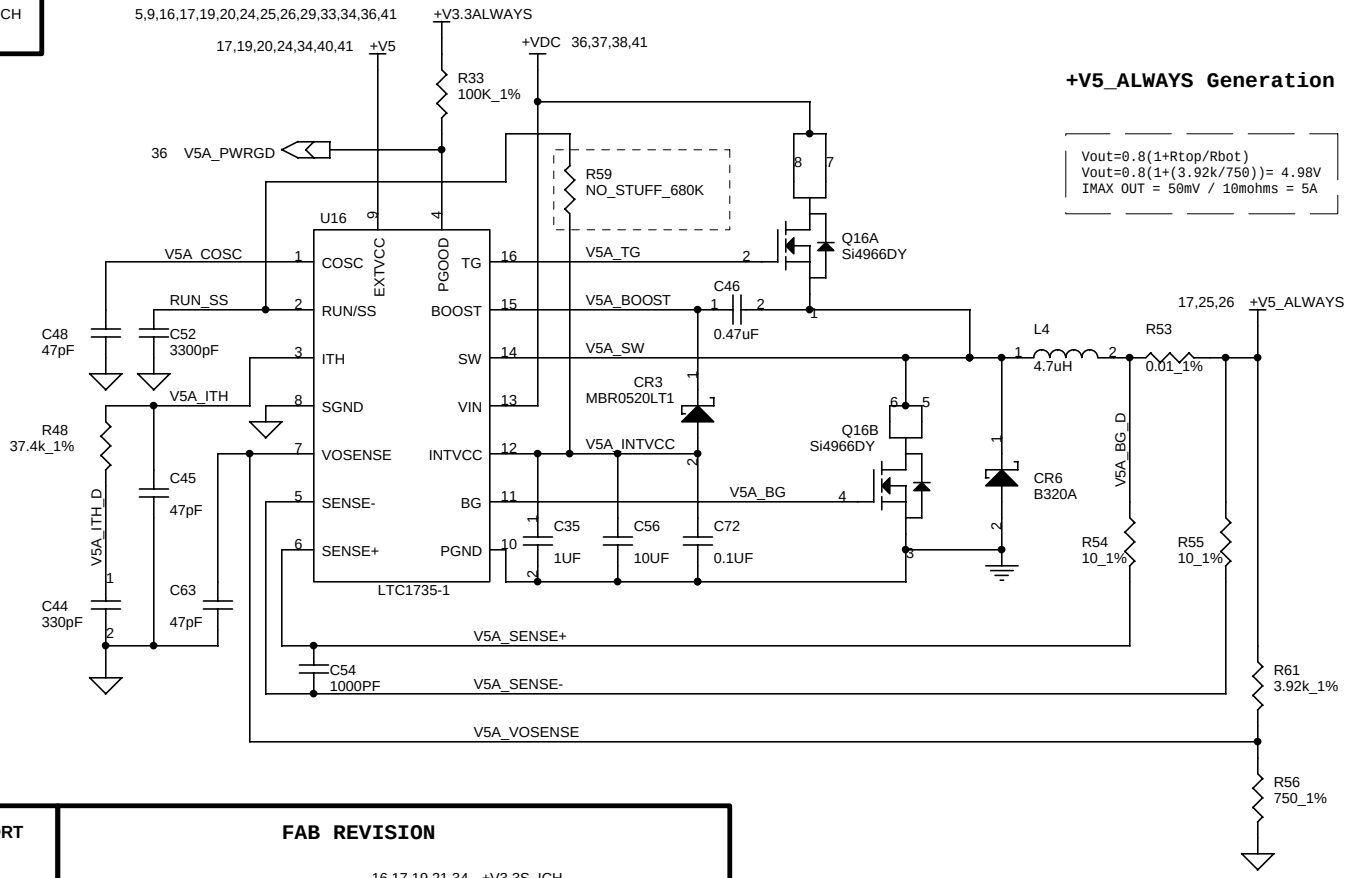
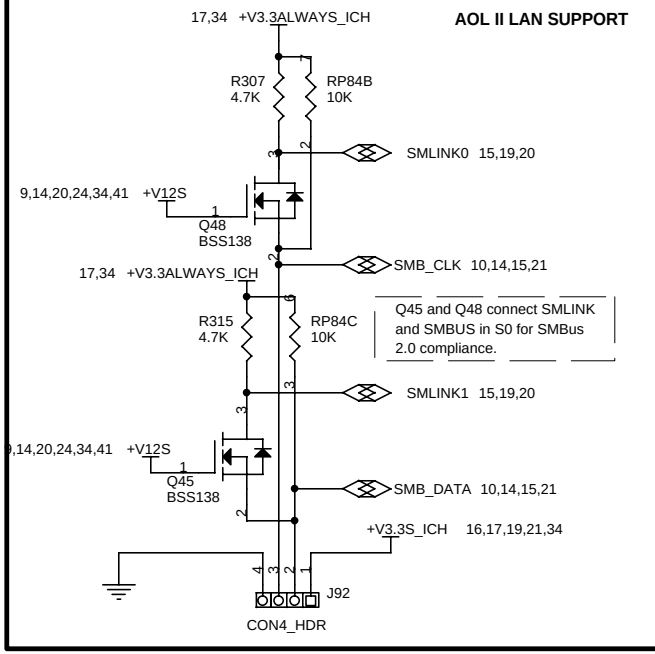
ICH4 Pullups



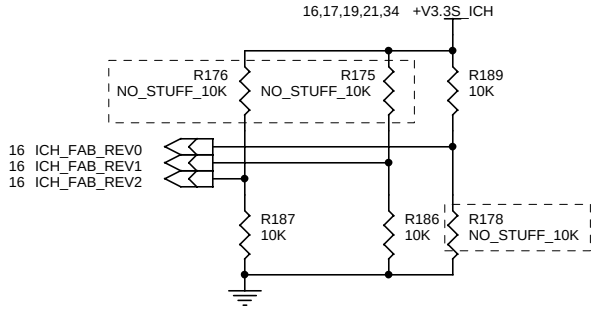
+V5_ALWAYS Generation



AOL II LAN SUPPORT

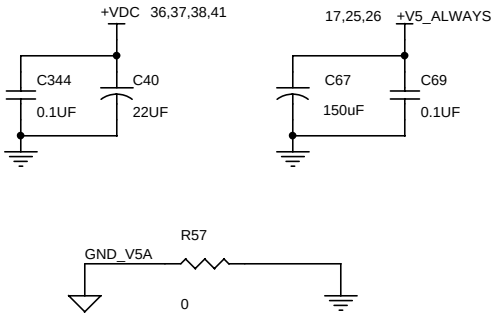


FAB REVISION



FAB ID Strapping Table

ICH_FAB_REV 2	1	0	BOARD FAB
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8



Title	+V5_ALWAYS VR, ICH4-M Pullups and Testpoints		
Size A	Project: 855PM Platform	Document Number	Rev
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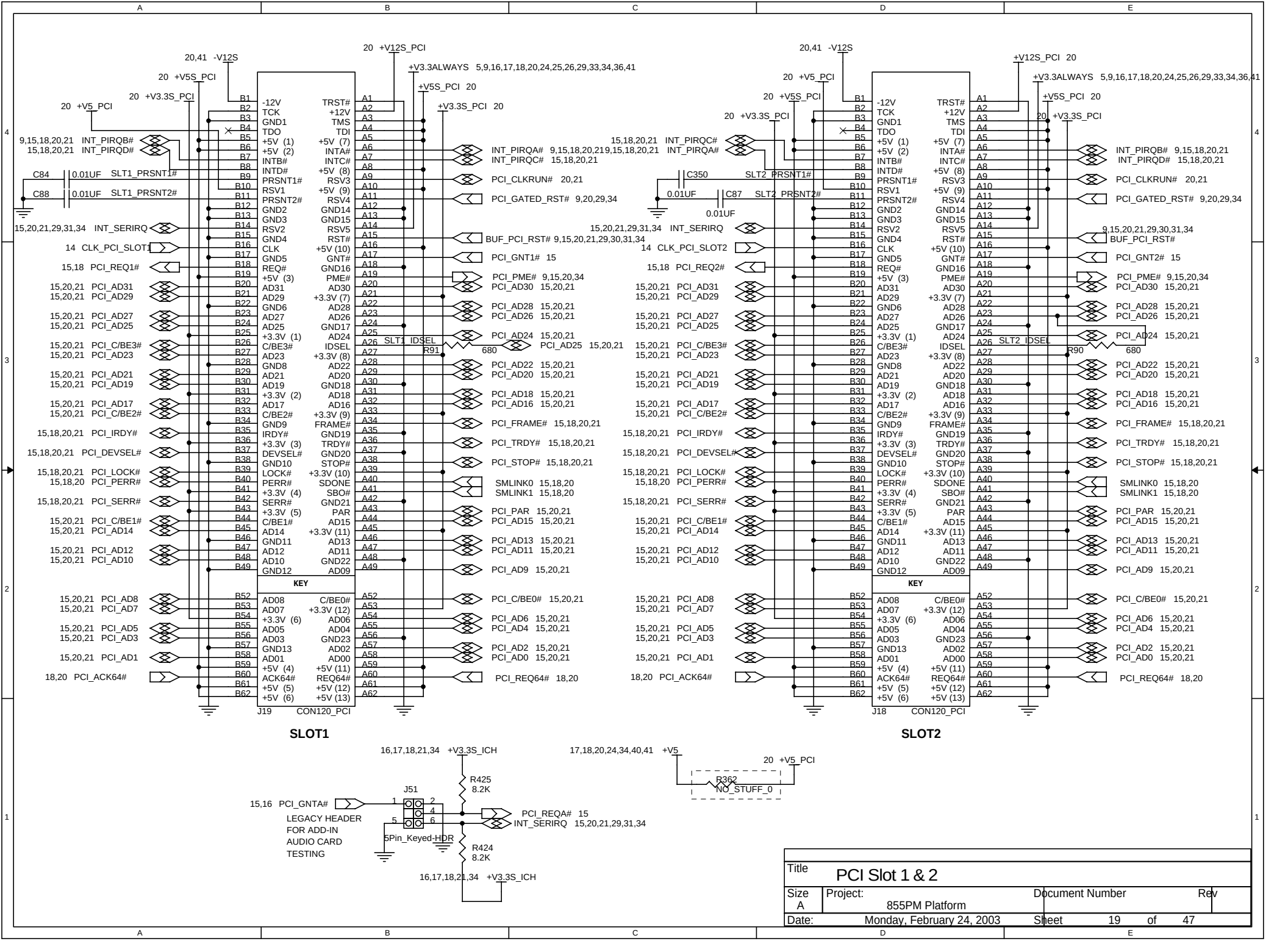
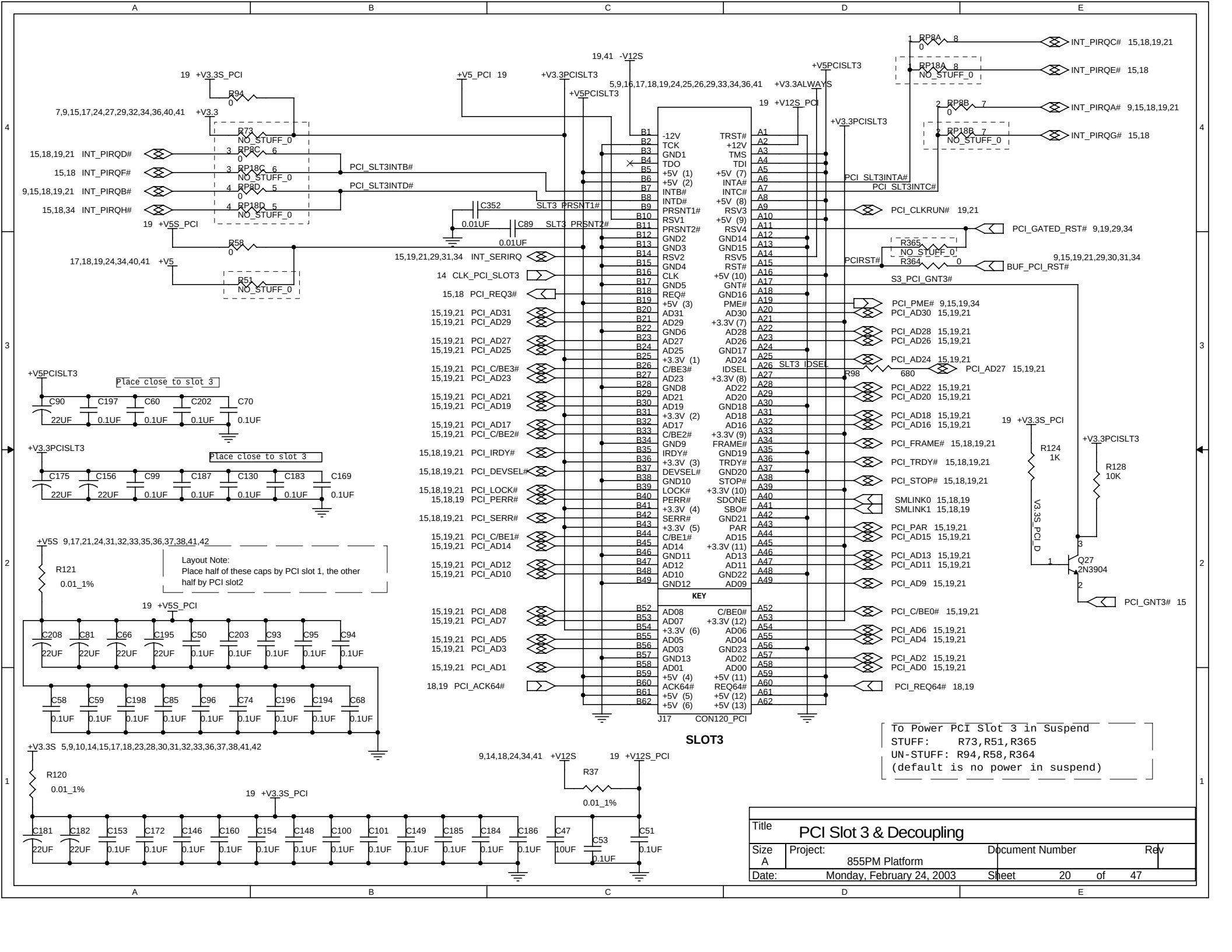


Title	PCI Slot 1 & 2		
Size A	Project: 855PM Platform	Document Number	Rev
Date: Monday, February 24, 2003		Sheet 19 of 47	


SLOT3
J17 CON120_PCI
KEY
Layout Note:
Place half of these caps by PCI slot 1, the other half by PCI slot2
Place close to slot 3
To Power PCI Slot 3 in Suspend
STUFF: R73,R51,R365
UN-STUFF: R94,R58,R364
(default is no power in suspend)
Title PCI Slot 3 & Decoupling
Size A
Project: 855PM Platform
Document Number
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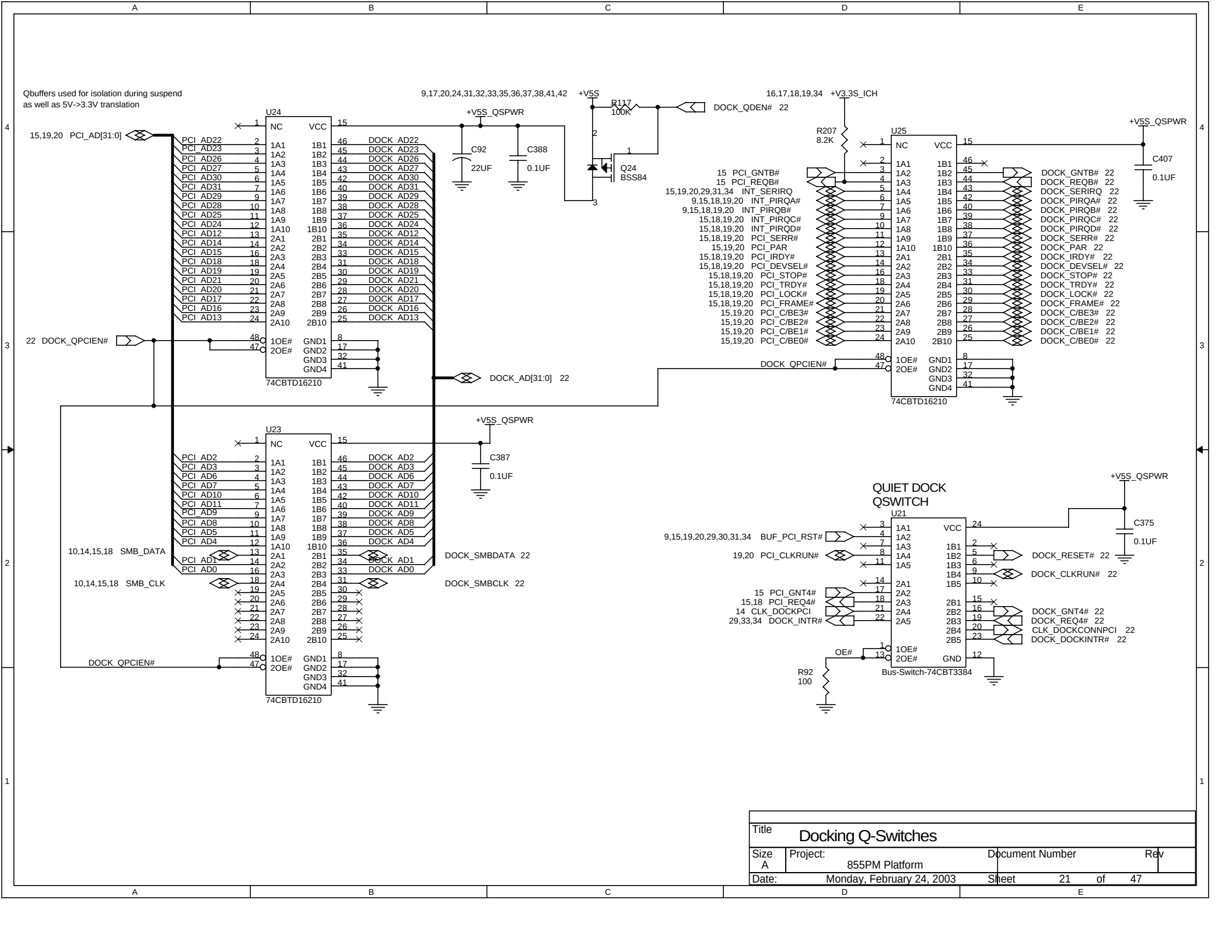
Qbuffers used for isolation during suspend
as well as 5V->3.3V translation
U24
U25
U23
74CBTD16210
9,17,20,24,31,32,33,35,36,37,38,41,42 +V5S
16,17,18,19,34 +V3.3S_ICH
+V5S_QSPWR
R117
100K
DOCK_QDEN# 22
R207
8.2K
C92
22UF
C388
0.1UF
C407
C387
Q24
BSS84
15,19,20 PCI_AD[31:0]
22 DOCK_QPCIEN#
DOCK_AD[31:0] 22
DOCK_QPCIEN#
10,14,15,18 SMB_DATA
10,14,15,18 SMB_CLK
DOCK_SMBDATA 22
DOCK_SMBCLK 22
QUIET DOCK
QSWITCH
U21
9,15,19,20,29,30,31,34 BUF_PCI_RST#
19,20 PCI_CLKRUN#
15 PCI_GNT4#
15,18 PCI_REQ4#
14 CLK_DOCKPCI
29,33,34 DOCK_INTR#
OE#
R92
100
Bus-Switch-74CBT3384
C375
0.1UF
Title
Docking Q-Switches
Size
A
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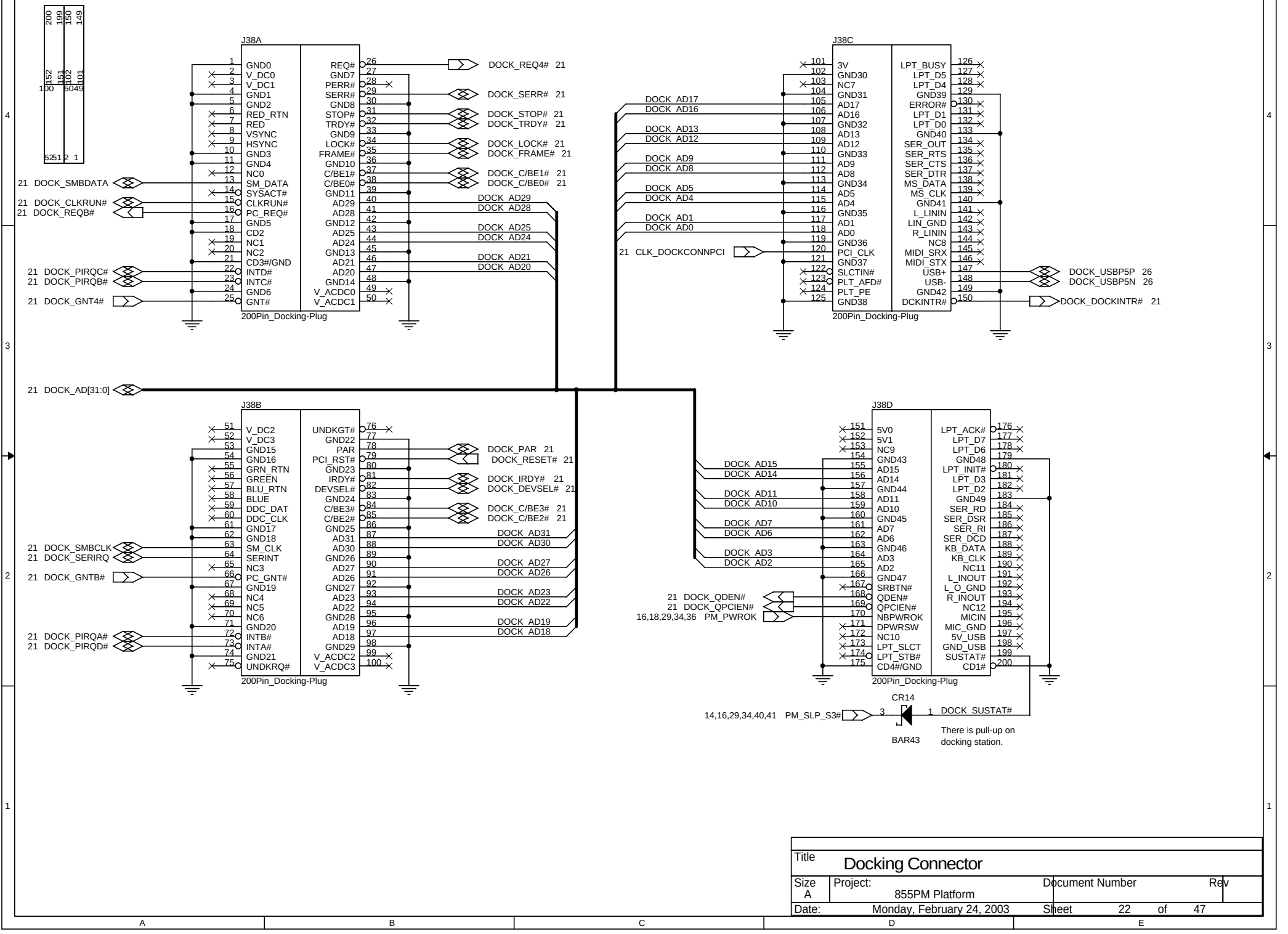

Title	Docking Connector		
Size A	Project: 855PM Platform	Document Number	Rev
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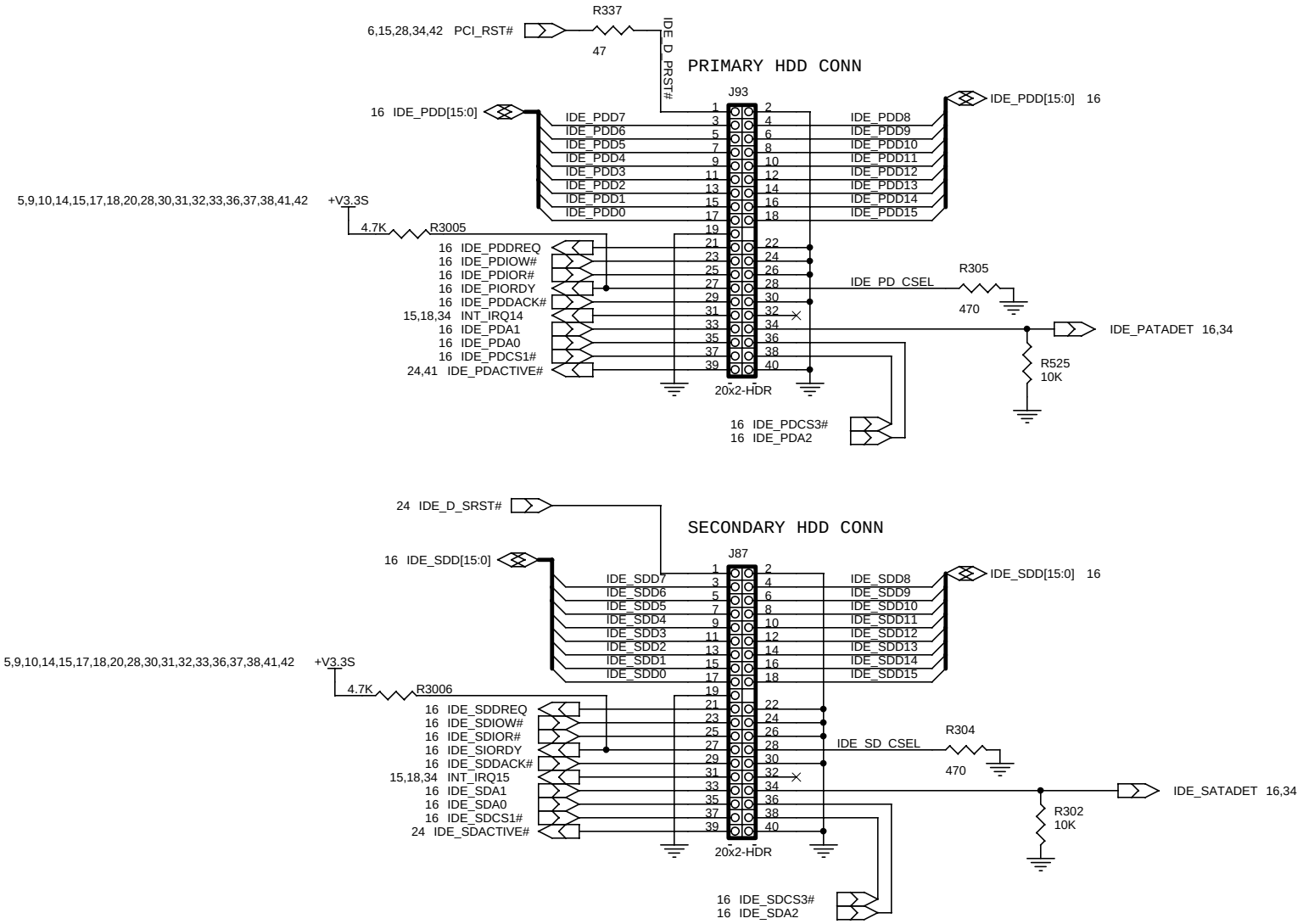

Title	IDE 1 of 2		
Size A	Project: 855PM Platform	Document Number	Rev
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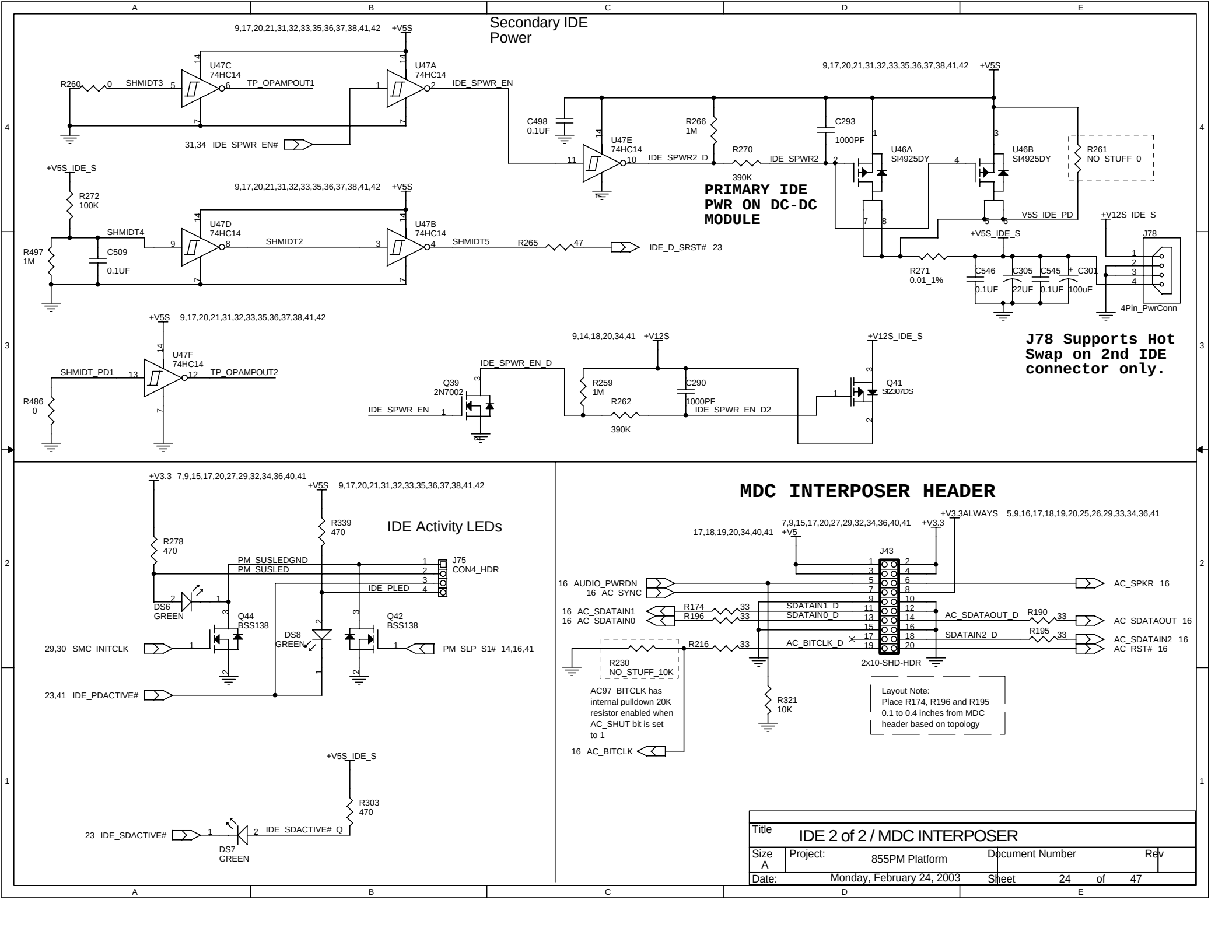
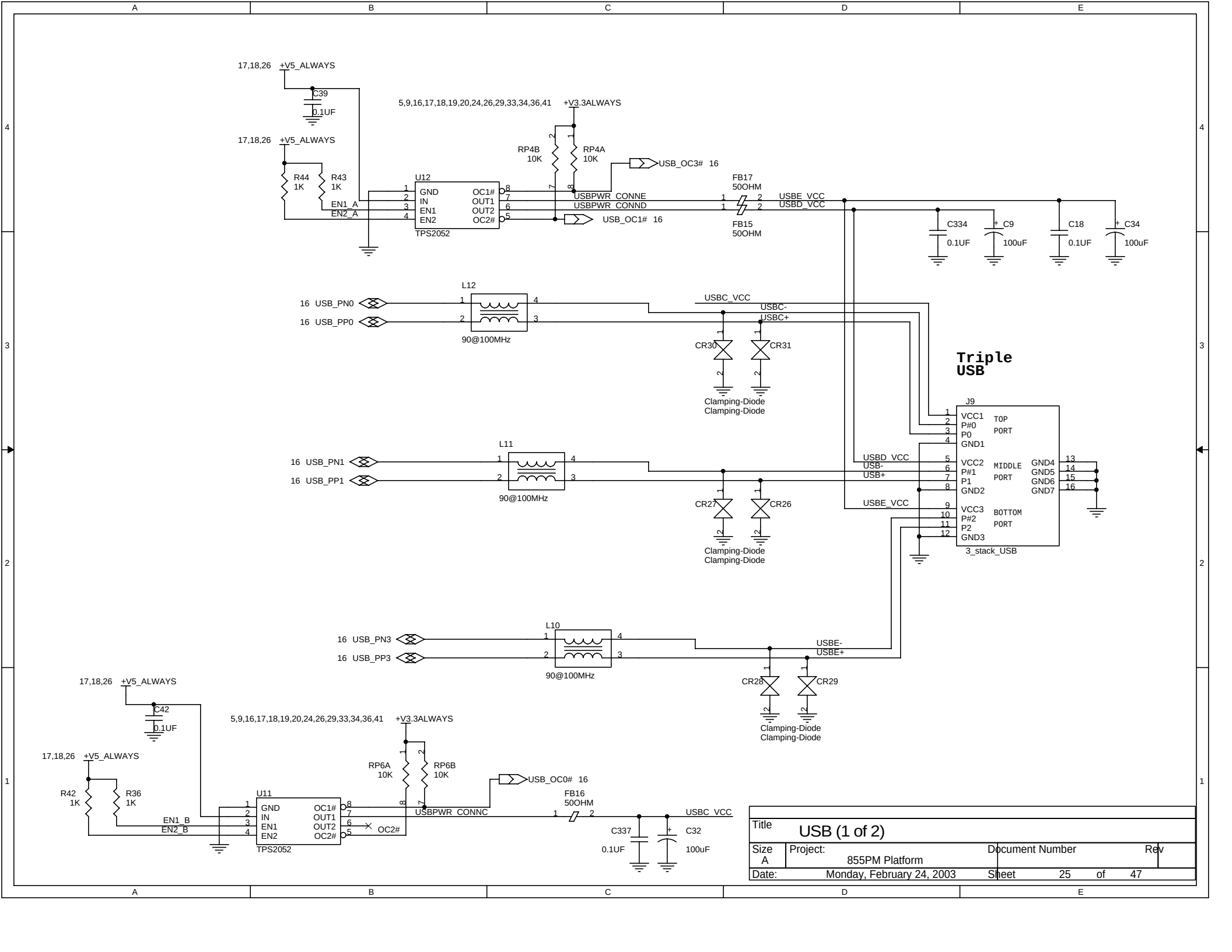

Secondary IDE Power
9,17,20,21,31,32,33,35,36,37,38,41,42 +V5S
U47C 74HC14
U47A 74HC14
R260 0 SHMIDT3 TP_OPAMPOUT1
IDE_SPWR_EN
31,34 IDE_SPWR_EN#
C498 0.1UF
U47E 74HC14
R266 1M
C293 1000PF
R270 390K
IDE_SPWR2_D
IDE_SPWR2
U46A SI4925DY
U46B SI4925DY
R261 NO_STUFF_0
PRIMARY IDE PWR ON DC-DC MODULE
+V5S_IDE_S
R272 100K
U47D 74HC14
U47B 74HC14
SHMIDT4
SHMIDT2
SHMIDT5
R265 47
IDE_D_SRST# 23
R497 1M
C509 0.1UF
V5S_IDE_PD
+V12S_IDE_S
J78
R271 0.01_1%
C546 0.1UF
C305 22UF
C545 0.1UF
C301 100uF
4Pin_PwrConn
J78 Supports Hot Swap on 2nd IDE connector only.
U47F 74HC14
SHMIDT_PD1
TP_OPAMPOUT2
R486 0
9,14,18,20,34,41 +V12S
IDE_SPWR_EN_D
Q39 2N7002
IDE_SPWR_EN
R259 1M
R262 390K
C290 1000PF
IDE_SPWR_EN_D2
Q41 SI2307DS
IDE Activity LEDs
+V3.3 7,9,15,17,20,27,29,32,34,36,40,41
R339 470
R278 470
PM_SUSLEDGND
PM_SUSLED
IDE_PLED
J75 CON4_HDR
DS6 GREEN
Q44 BSS138
DS8 GREEN
Q42 BSS138
29,30 SMC_INITCLK
PM_SLP_S1# 14,16,41
23,41 IDE_PDACTIVE#
R303 470
23 IDE_SDACTIVE#
IDE_SDACTIVE#_Q
DS7 GREEN
MDC INTERPOSER HEADER
+V3.3ALWAYS 5,9,16,17,18,19,20,25,26,29,33,34,36,41
7,9,15,17,20,27,29,32,34,36,40,41 +V3.3
17,18,19,20,34,40,41 +V5
J43
16 AUDIO_PWRDN
16 AC_SYNC
AC_SPKR 16
16 AC_SDATAIN1
16 AC_SDATAIN0
R174 33
R196 33
SDATAIN1_D
SDATAIN0_D
AC_SDATAOUT_D
R190 33
AC_SDATAOUT 16
SDATAIN2_D
R195 33
AC_SDATAIN2 16
AC_RST# 16
AC_BITCLK_D
R216 33
R230 NO_STUFF_10K
2x10-SHD-HDR
AC97_BITCLK has internal pulldown 20K resistor enabled when AC_SHUT bit is set to 1
R321 10K
16 AC_BITCLK
Layout Note: Place R174, R196 and R195 0.1 to 0.4 inches from MDC header based on topology
Title IDE 2 of 2 / MDC INTERPOSER
Size A
Project: 855PM Platform
Document Number
Rev
Date: Monday, February 24, 2003
Sheet 24 of 47


17,18,26 +V5_ALWAYS
C39
0.1UF
5,9,16,17,18,19,20,24,26,29,33,34,36,41 +V3.3ALWAYS
RP4B 10K
RP4A 10K
USB_OC3# 16
R44 1K
R43 1K
U12
GND
IN
EN1
EN2
OC1#
OUT1
OUT2
OC2#
EN1_A
EN2_A
TPS2052
USBPWR_CONNE
USBPWR_CONND
USB_OC1# 16
FB17 50OHM
FB15 50OHM
USBE_VCC
USBD_VCC
C334 0.1UF
C9 100uF
C18 0.1UF
C34 100uF
L12
16 USB_PN0
16 USB_PP0
90@100MHz
USBC_VCC
USBC-
USBC+
CR30
CR31
Clamping-Diode
Clamping-Diode
Triple USB
J9
VCC1
P#0
P0
GND1
TOP PORT
VCC2
P#1
P1
GND2
MIDDLE PORT
VCC3
P#2
P2
GND3
BOTTOM PORT
GND4
GND5
GND6
GND7
3_stack_USB
L11
16 USB_PN1
16 USB_PP1
90@100MHz
USBD_VCC
USB-
USB+
CR27
CR26
Clamping-Diode
Clamping-Diode
USBE_VCC
L10
16 USB_PN3
16 USB_PP3
90@100MHz
USBE-
USBE+
CR28
CR29
Clamping-Diode
Clamping-Diode
17,18,26 +V5_ALWAYS
C42
0.1UF
5,9,16,17,18,19,20,24,26,29,33,34,36,41 +V3.3ALWAYS
17,18,26 +V5_ALWAYS
R42 1K
R36 1K
RP6A 10K
RP6B 10K
USB_OC0# 16
U11
GND
IN
EN1
EN2
OC1#
OUT1
OUT2
OC2#
EN1_B
EN2_B
TPS2052
USBPWR_CONNC
OC2#
FB16 50OHM
USBC_VCC
C337 0.1UF
C32 100uF
Title
USB (1 of 2)
Size A
Project:
855PM Platform
Document Number
Rev
Date:
Monday, February 24, 2003
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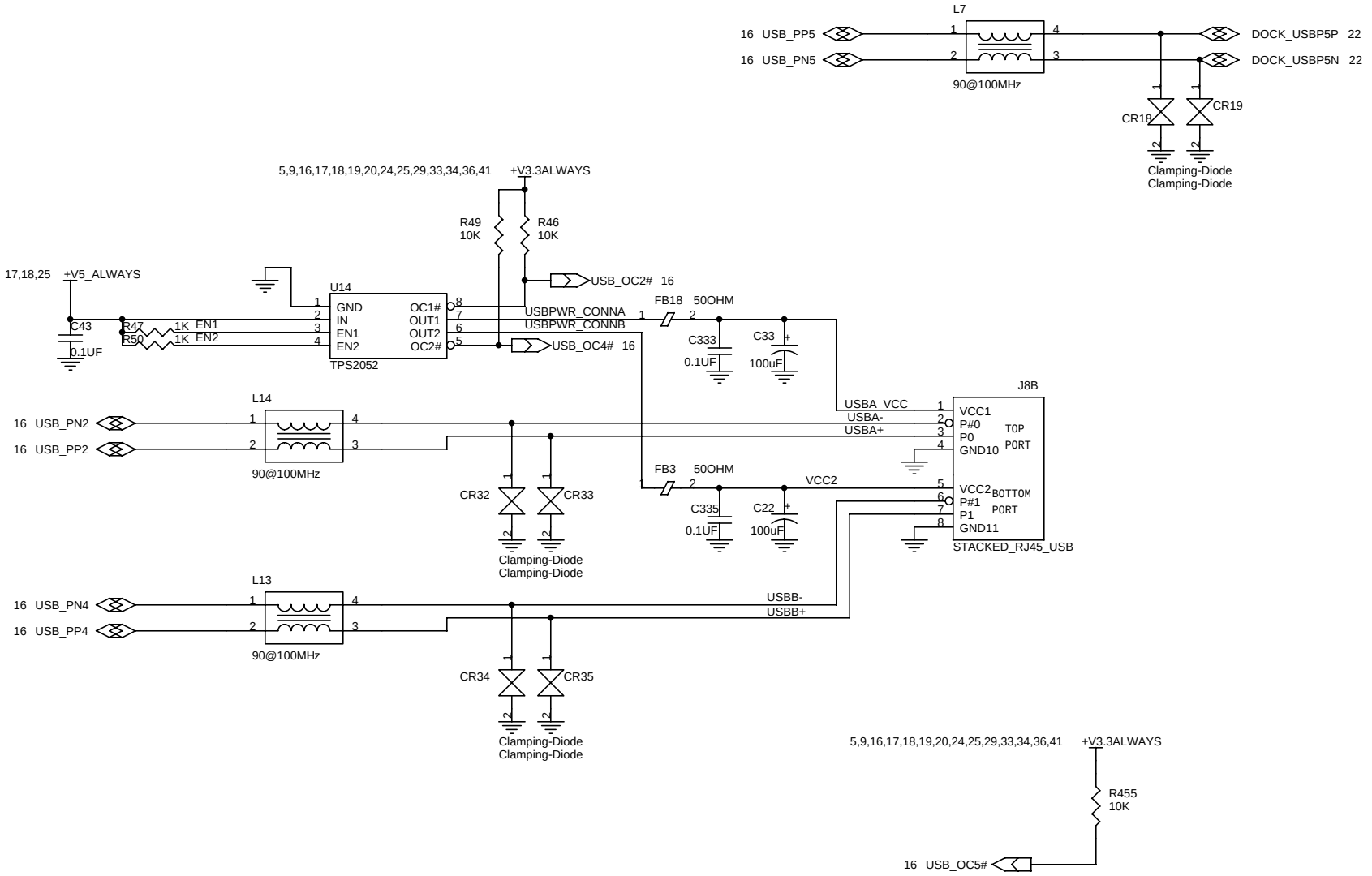
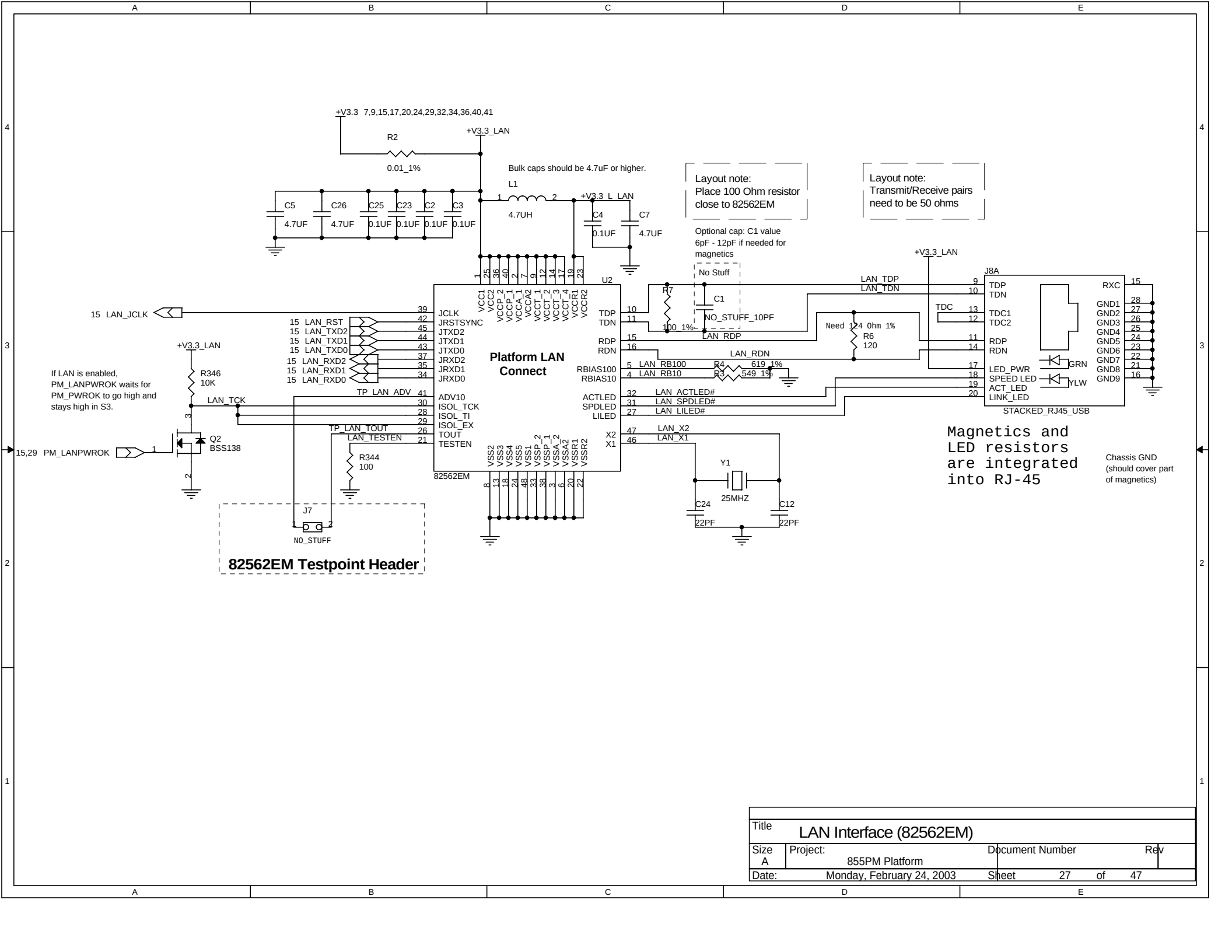
DOCKING
UNIVERSAL SERIAL BUS



Title	USB (2 of 2)		
Size A	Project: 855PM Platform	Document Number	Rev
Date: Monday, February 24, 2003	Sheet 26 of 47		


+V3.3 7,9,15,17,20,24,29,32,34,36,40,41
+V3.3_LAN
R2
0.01_1%
Bulk caps should be 4.7uF or higher.
L1
4.7UH
+V3.3_L_LAN
C5 4.7UF
C26 4.7UF
C25 0.1UF
C23 0.1UF
C2 0.1UF
C3 0.1UF
C4 0.1UF
C7 4.7UF
Layout note:
Place 100 Ohm resistor close to 82562EM
Optional cap: C1 value 6pF - 12pF if needed for magnetics
No Stuff
C1
NO_STUFF_10PF
R7
100_1%
LAN_TDP
LAN_TDN
LAN_RDP
LAN_RDN
Need 124 Ohm 1%
R6
120
Layout note:
Transmit/Receive pairs need to be 50 ohms
+V3.3_LAN
J8A
TDP
TDN
TDC
TDC1
TDC2
RDP
RDN
LED_PWR
SPEED LED
ACT_LED
LINK_LED
RXC
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GRN
YLW
STACKED_RJ45_USB
Magnetics and LED resistors are integrated into RJ-45
Chassis GND (should cover part of magnetics)
15 LAN_JCLK
15 LAN_RST
15 LAN_TXD2
15 LAN_TXD1
15 LAN_TXD0
15 LAN_RXD2
15 LAN_RXD1
15 LAN_RXD0
TP_LAN_ADV
LAN_TCK
TP_LAN_TOUT
LAN_TESTEN
U2
JCLK
JRSTSYNC
JTXD2
JTXD1
JTXD0
JRXD2
JRXD1
JRXD0
ADV10
ISOL_TCK
ISOL_TI
ISOL_EX
TOUT
TESTEN
Platform LAN Connect
RDP
RDN
RBIAS100
RBIAS10
ACTLED
SPDLED
LILED
X2
X1
LAN_RB100
LAN_RB10
R4 619 1%
R3 549 1%
LAN_ACTLED#
LAN_SPDLED#
LAN_LILED#
LAN_X2
LAN_X1
82562EM
Y1
25MHZ
C24 22PF
C12 22PF
If LAN is enabled, PM_LANPWROK waits for PM_PWROK to go high and stays high in S3.
+V3.3_LAN
R346 10K
Q2 BSS138
15,29 PM_LANPWROK
R344 100
J7
NO_STUFF
82562EM Testpoint Header
Title
LAN Interface (82562EM)
Size A
Project: 855PM Platform
Document Number
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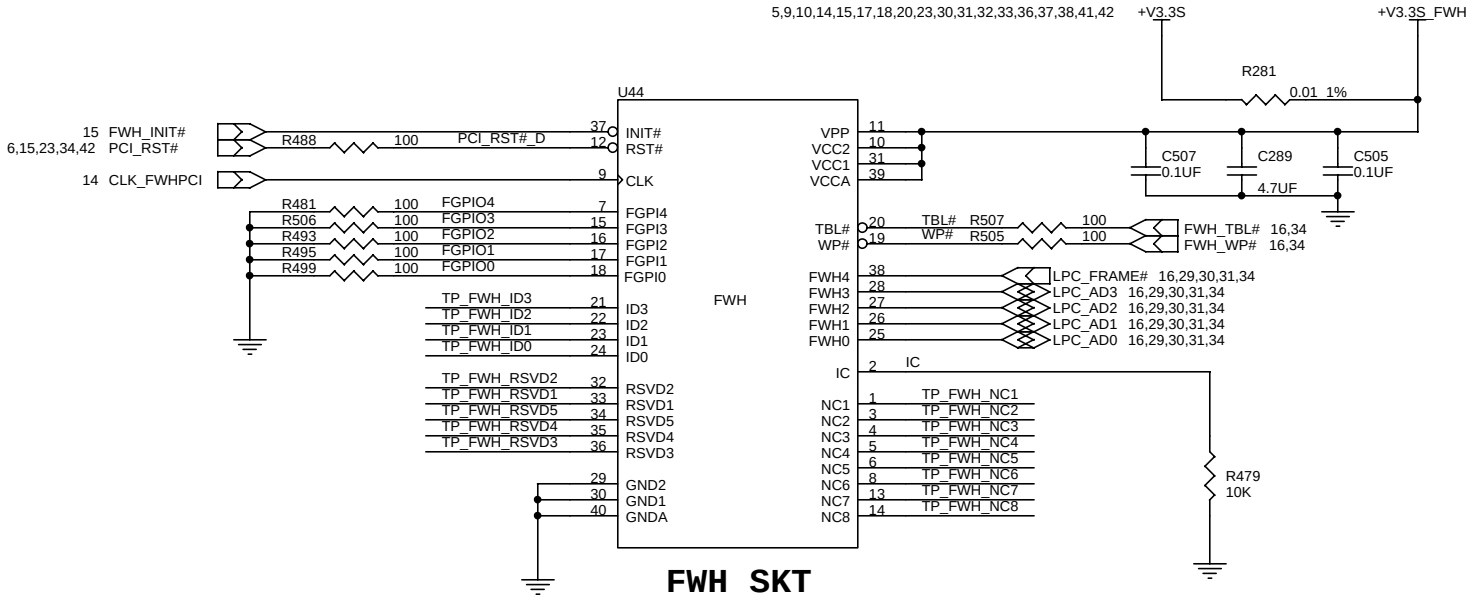
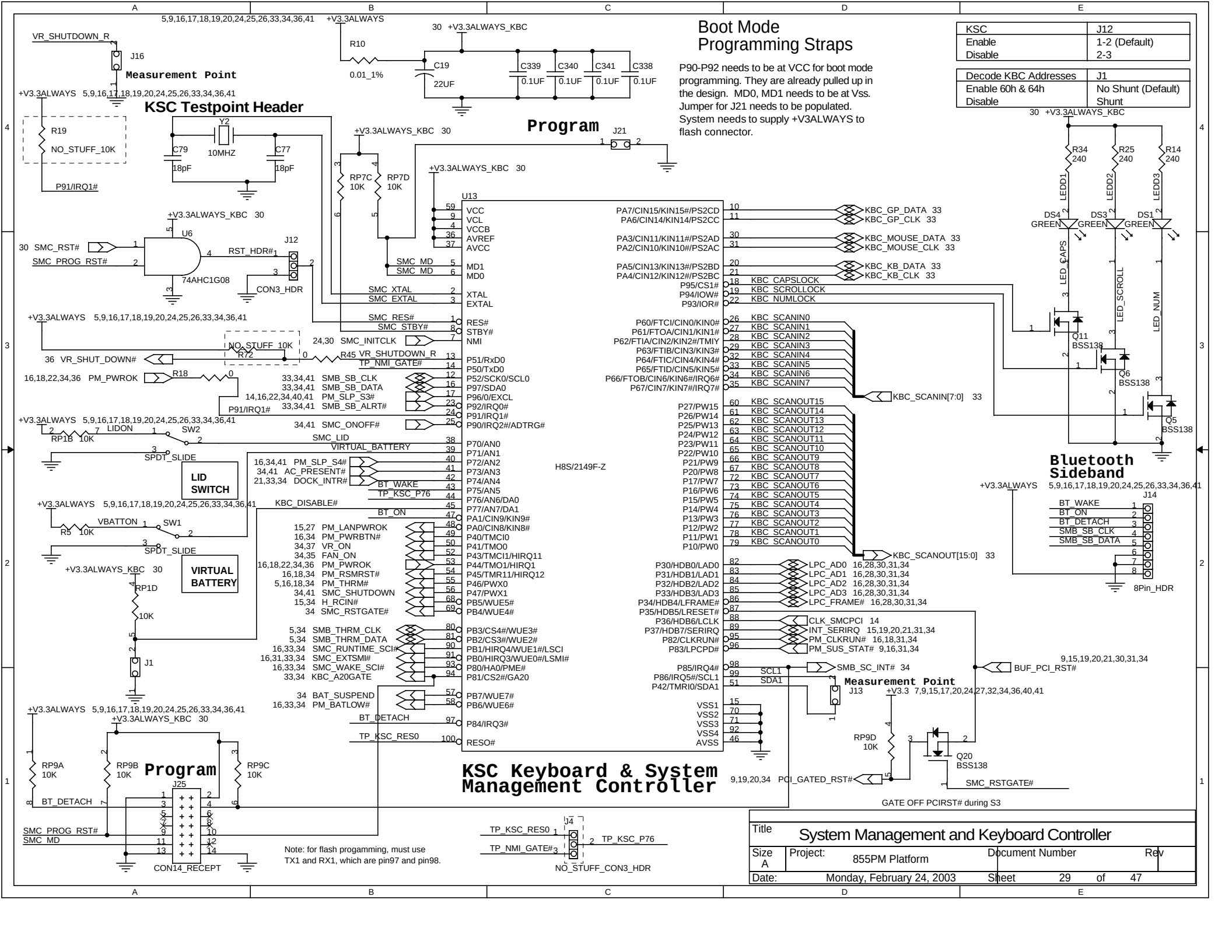


FWH SKT

FWH sits in the
FWH_TSOP_Socket,
Not on the board

Title	FWH		
Size A	Project: 855PM Platform	Document Number	Rev
Date: Monday, February 24, 2003	Sheet 28 of 47		


Boot Mode Programming Straps
P90-P92 needs to be at VCC for boot mode programming. They are already pulled up in the design. MD0, MD1 needs to be at Vss. Jumper for J21 needs to be populated. System needs to supply +V3ALWAYS to flash connector.
KSC | J12
Enable | 1-2 (Default)
Disable | 2-3
Decode KBC Addresses | J1
Enable 60h & 64h | No Shunt (Default)
Disable | Shunt
KSC Testpoint Header
Program
Measurement Point
LID SWITCH
VIRTUAL BATTERY
Bluetooth Sideband
H8S/2149F-Z
KSC Keyboard & System Management Controller
Note: for flash progamming, must use TX1 and RX1, which are pin97 and pin98.
GATE OFF PCIRST# during S3
Title: System Management and Keyboard Controller
Size: A
Project: 855PM Platform
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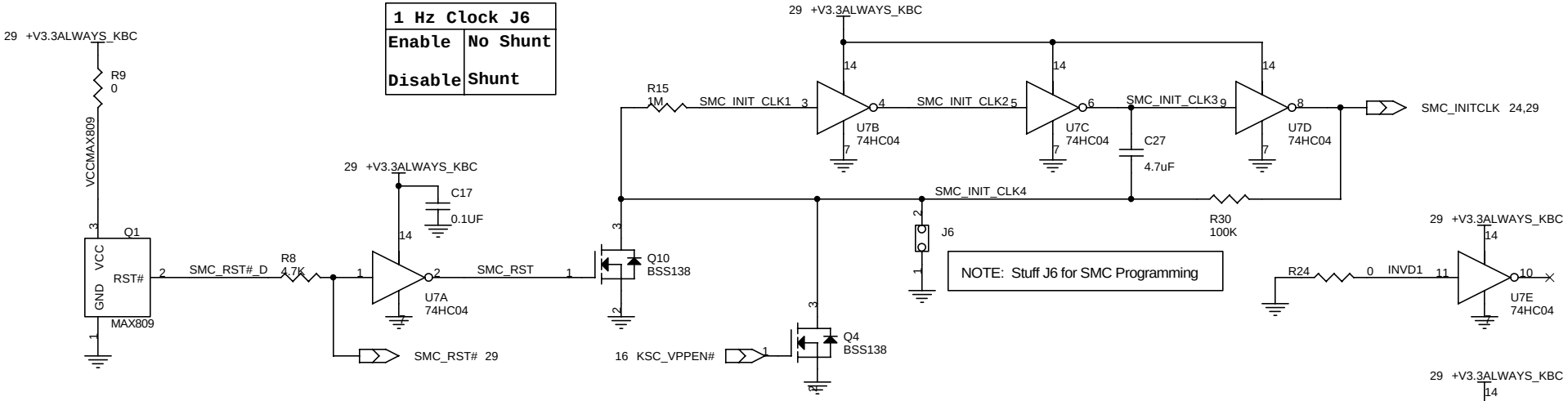
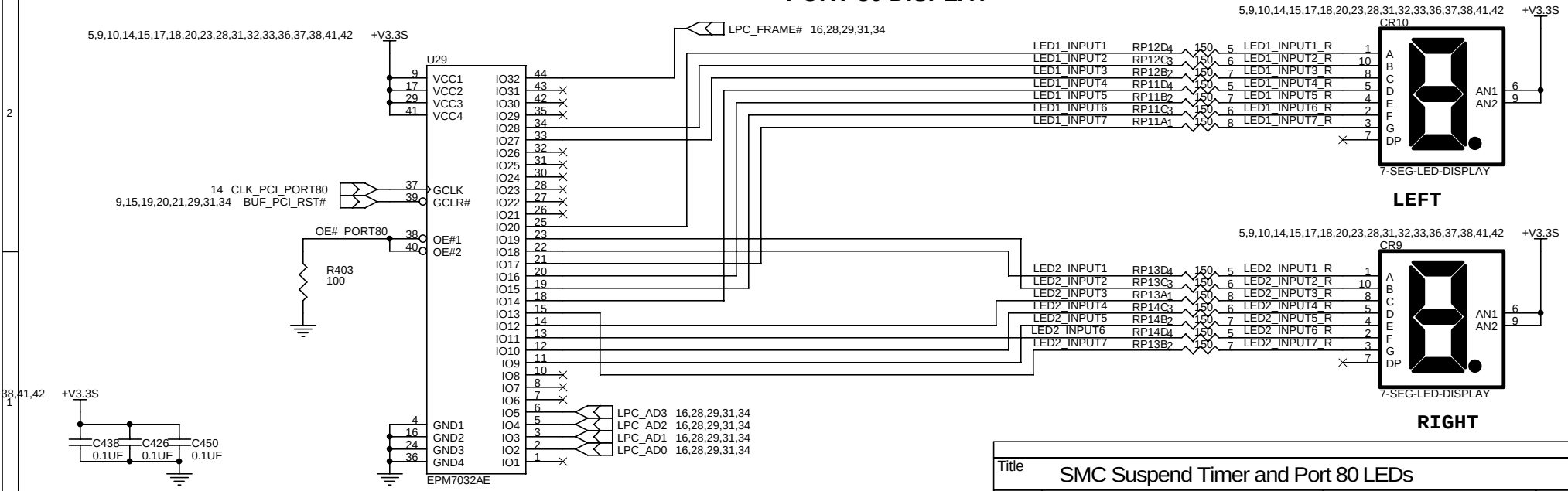
Circuitry provides an interrupt to the SMC every 1s while in suspend (this allows the SMC to complete housekeeping functions while suspended)

1 Hz Clock J6	
Enable	No Shunt
Disable	Shunt

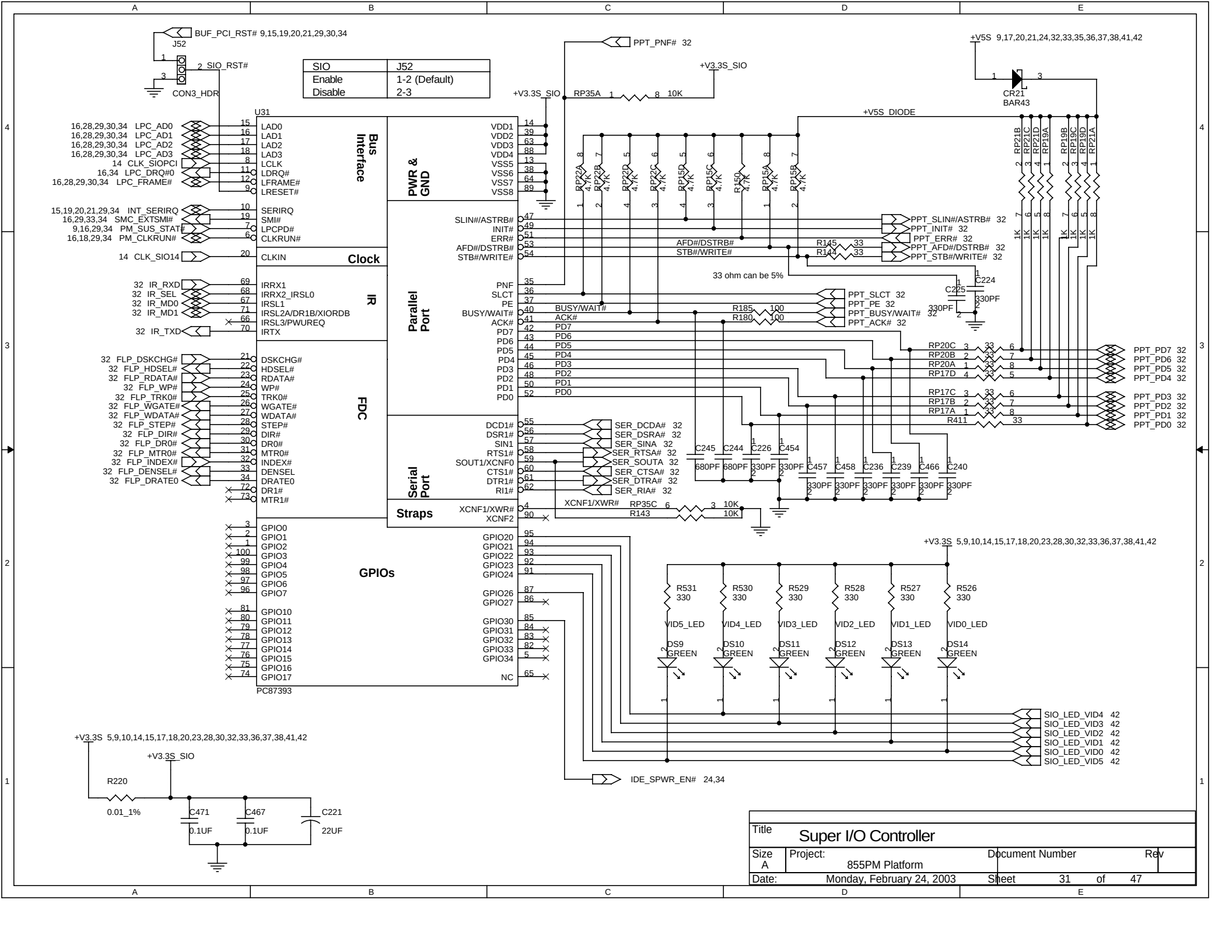


SMC SUSPEND TIMER

PORT 80 DISPLAY



Title	SMC Suspend Timer and Port 80 LEDs		
Size A	Project: 855PM Platform	Document Number	Rev
Date: Monday, February 24, 2003		Sheet 30 of 47	


BUF_PCI_RST# 9,15,19,20,21,29,30,34
J52
2 SIO_RST#
CON3_HDR
SIO | J52
Enable | 1-2 (Default)
Disable | 2-3
PPT_PNF# 32
+V3.3S_SIO
RP35A 10K
+V5S 9,17,20,21,24,32,33,35,36,37,38,41,42
CR21
BAR43
+V5S_DIODE
U31
Bus Interface
LAD0
LAD1
LAD2
LAD3
LCLK
LDRQ#
LFRAME#
LRESET#
SERIRQ
SMI#
LPCPD#
CLKRUN#
Clock
CLKIN
IR
IRRX1
IRRX2_IRSL0
IRSL1
IRSL2A/DR1B/XIORDB
IRSL3/PWUREQ
IRTX
FDC
DSKCHG#
HDSEL#
RDATA#
WP#
TRK0#
WGATE#
WDATA#
STEP#
DIR#
DR0#
MTR0#
INDEX#
DENSEL
DRATE0
DR1#
MTR1#
GPIOs
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
PC87393
PWR & GND
VDD1
VDD2
VDD3
VDD4
VSS5
VSS6
VSS7
VSS8
Parallel Port
SLIN#/ASTRB#
INIT#
ERR#
AFD#/DSTRB#
STB#/WRITE#
PNF
SLCT
PE
BUSY/WAIT#
ACK#
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
Serial Port
DCD1#
DSR1#
SIN1
RTS1#
SOUT1/XCNF0
CTS1#
DTR1#
RI1#
Straps
XCNF1/XWR#
XCNF2
RP22A 4.7K
RP22B 4.7K
RP22D 4.7K
RP22C 4.7K
RP15D 4.7K
RP15C 4.7K
R150 4.7K
RP15A 4.7K
RP15B 4.7K
RP21B 1K
RP21C 1K
RP21D 1K
RP19A 1K
RP19B 1K
RP19C 1K
RP19D 1K
RP21A 1K
PPT_SLIN#/ASTRB# 32
PPT_INIT# 32
PPT_ERR# 32
PPT_AFD#/DSTRB# 32
PPT_STB#/WRITE# 32
R145 33
R144 33
33 ohm can be 5%
C224 330PF
C225 330PF
PPT_SLCT 32
PPT_PE 32
PPT_BUSY/WAIT# 32
PPT_ACK# 32
R185 100
R180 100
RP20C 33
RP20B 33
RP20A 33
RP17D 33
RP17C 33
RP17B 33
RP17A 33
R411 33
PPT_PD7 32
PPT_PD6 32
PPT_PD5 32
PPT_PD4 32
PPT_PD3 32
PPT_PD2 32
PPT_PD1 32
PPT_PD0 32
SER_DCDA# 32
SER_DSRA# 32
SER_SINA 32
SER_RTSA# 32
SER_SOUTA 32
SER_CTSA# 32
SER_DTRA# 32
SER_RIA# 32
C245 680PF
C244 680PF
C226 330PF
C454 330PF
C457 330PF
C458 330PF
C236 330PF
C239 330PF
C466 330PF
C240 330PF
XCNF1/XWR# RP35C 10K
R143 10K
+V3.3S 5,9,10,14,15,17,18,20,23,28,30,32,33,36,37,38,41,42
R531 330
R530 330
R529 330
R528 330
R527 330
R526 330
VID5_LED
VID4_LED
VID3_LED
VID2_LED
VID1_LED
VID0_LED
DS9 GREEN
DS10 GREEN
DS11 GREEN
DS12 GREEN
DS13 GREEN
DS14 GREEN
SIO_LED_VID4 42
SIO_LED_VID3 42
SIO_LED_VID2 42
SIO_LED_VID1 42
SIO_LED_VID0 42
SIO_LED_VID5 42
IDE_SPWR_EN# 24,34
+V3.3S 5,9,10,14,15,17,18,20,23,28,30,32,33,36,37,38,41,42
+V3.3S_SIO
R220 0.01_1%
C471 0.1UF
C467 0.1UF
C221 22UF
Title
Super I/O Controller
Size A
Project: 855PM Platform
Document Number
Rev
Date: Monday, February 24, 2003
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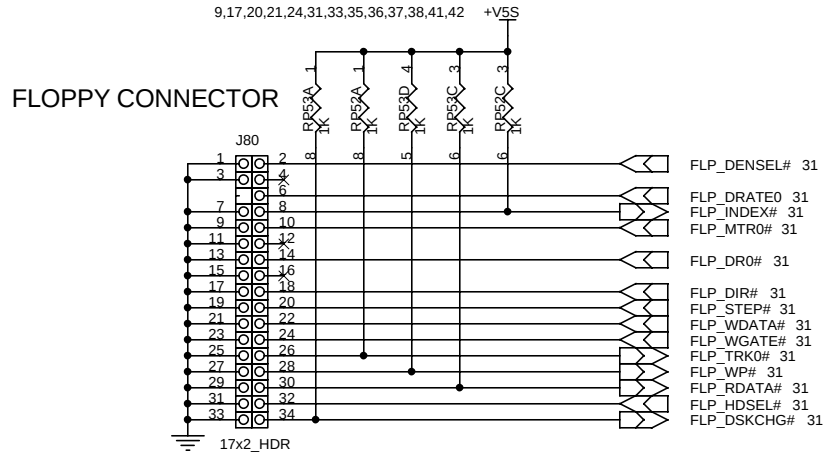
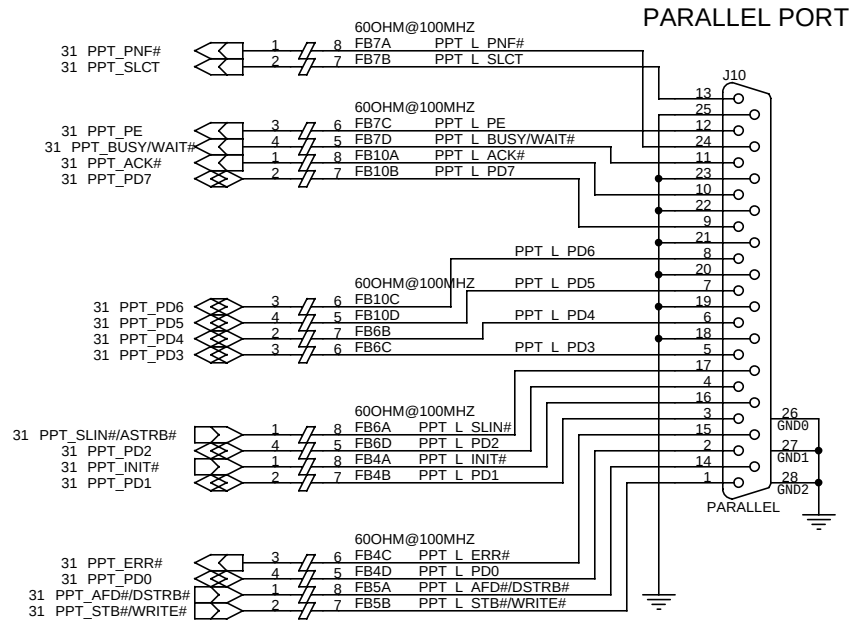
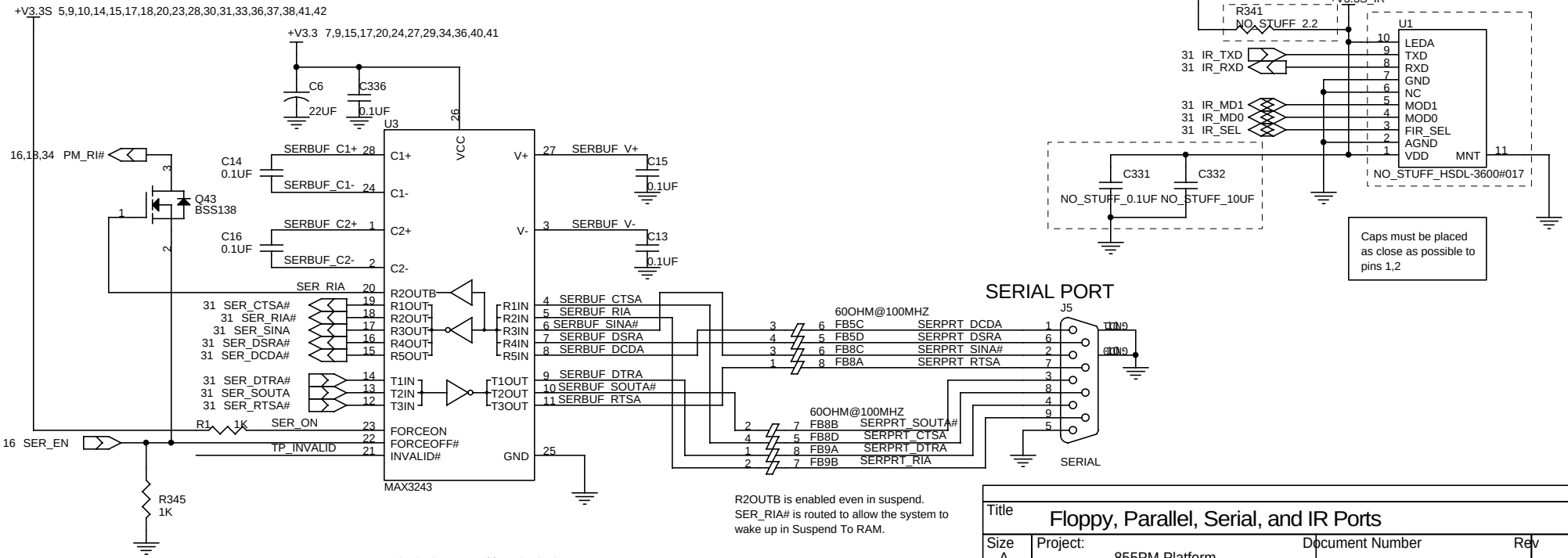
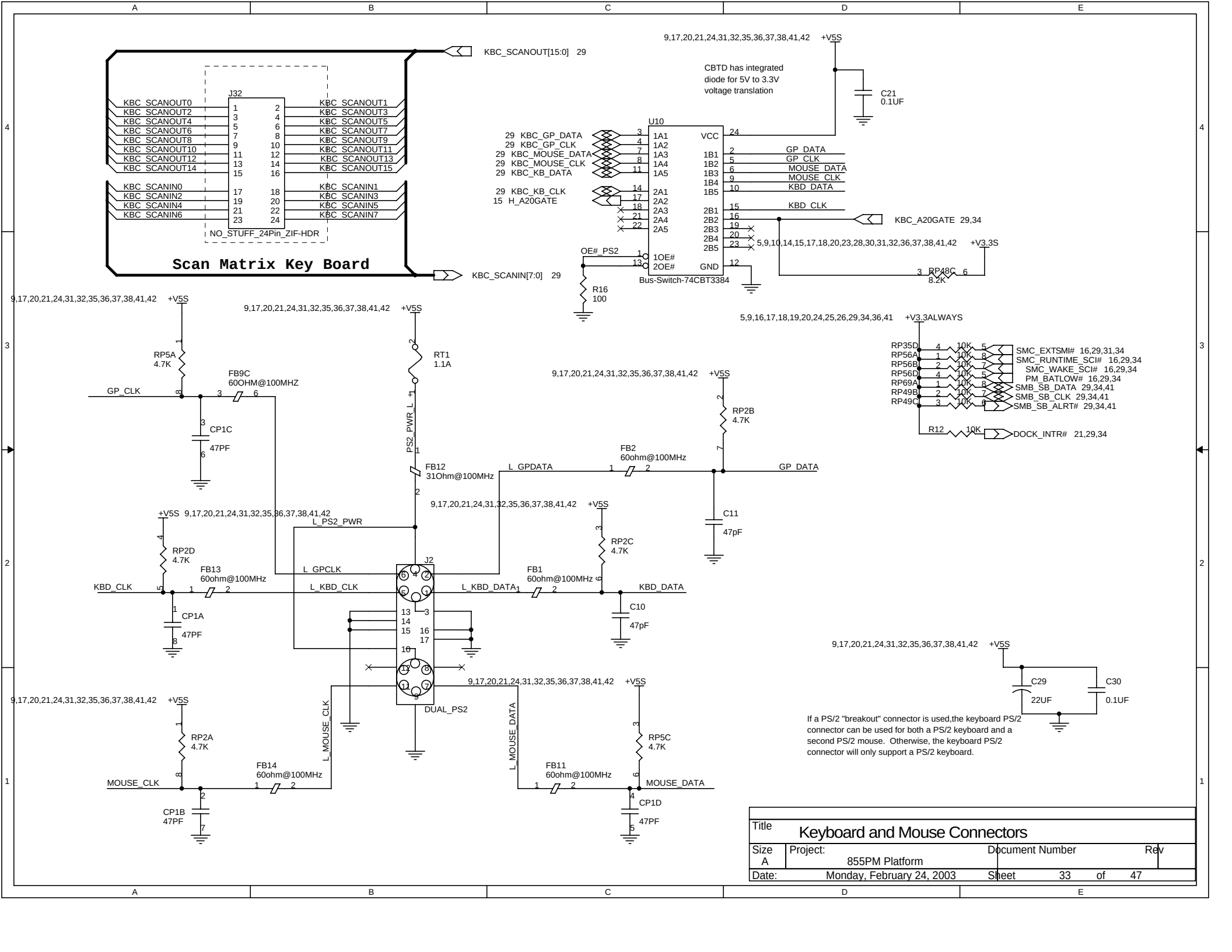






Title	Floppy, Parallel, Serial, and IR Ports		
Size A	Project: 855PM Platform	Document Number	Rev
Date: Monday, February 24, 2003		Sheet 32 of 47	



Title	Keyboard and Mouse Connectors		
Size A	Project: 855PM Platform	Document Number	Rev
Date: Monday, February 24, 2003	Sheet 33 of 47		

LPC POWERED ON SUSPEND RAIL FOR ADD-IN H8 CARD

LPC Debug Slot

J41 — 60Pin_CardCon

	B1	12V1	12V2	A1	
16 PM_SUS_CLK	B2	SUSCLK	NEG_12V	A2	
	B3	GND1	GND2	A3	
	B4	LREQ	BP_CLK	A4	
	B5	VCC3_1	VCC3_2	A5	
	B6	LCNTL0	LCNTL1	A6	
	B7	GND3	GND5	A7	
	B8	LDC	LD6	A8	
	B9	LD5	LD4	A9	
	B10	GND4	GND7	A10	
	B11	LD3	LD2	A11	
	B12	LD1	LD0	A12	
	B13	GND6	VCC5_2	A13	
	B14	3V_STBY	SCLK	A14	
	B15	LPS	GND10	A15	
15,29 H_RCIN#	B16	KBRESTE#	SERIRQ	A16	INT_SERIRQ 15,19,20,21,29,31
29,33 KBC_A20GATE	B17	A20GATE#	CLKRUN#	A17	PM_CLKRUN# 16,18,29,31
	B18	GND8	GND12	A18	
16,29,31,33 SMC_EXTSMI#	B19	LSMI#	LINK_ON	A19	
		KEY			
	B20	VCC5_1	VCC5_3	A20	
16 LPC_DRQ#1	B21	LDRQ1#	LDRQ0#	A21	LPC_DRQ#0 16,31
16,28,29,30,31 LPC_FRAME#	B22	LFRAME1#	GND14	A22	
	B23	GND9	LAD3	A23	LPC_AD3 16,28,29,30,31
16,28,29,30,31 LPC_AD2	B24	LAD2	LAD1	A24	LPC_AD1 16,28,29,30,31
16,28,29,30,31 LPC_AD0	B25	LAD0	GND15	A25	
	B26	GND11	PCICLK	A26	CLK_LPCPCI 14
	B27	PCIRST#	LPCPD#	A27	PM_SUS_STAT# 9,16,29,31
	B28	GND13	GND16	A28	
14 CLK_LPC14	B29	OSC	PME#	A29	PCI_PME# 9,15,19,20
	B30	VCC3_3	VCC3_4	A30	

9,14,18,20,24,41 +V12S

+V3.3_LPCSLOT

+V5_LPCSLOT

9,16,17,18,19,20,24,25,26,29,33,36,41 +V3.3ALWAYS

LPC_RST#

9,19,20,29 PCI_GATED_RST# — R222 NO_STUFF_0 — R225 0 — BUF_PCI_RST# 9,15,19,20,21,29,30,31

Layout Note:
Line up LPC slot
with PCI Slot 3

NOTE:

Route Processor Test signals stubless to headers

SMBus Debug Header

16,17,18,19,21 +V3.3S_ICH

RP87A 10K — RP87C 10K — RP87B 10K

16 ICH_GPIO7 — J97 CON4_HDR — 16 ICH_GPIO42 — 16 ICH_GPIO43

ICH4-M Testpoint Header

17,18 +V3.3ALWAYS_ICH

R331 4.7K

J98 — 2X5-Header

15 TP_HUB_PD11	1 2	ICH_GPIO28 16
	3 4	IDE_PATADET 16,23
15,18,20 INT_PIRQH#	5 6	IDE_SATADET 16,23
16 ICH_MFG_MODE	7 8	
9,15,19,20 PCI_PME#	9 10	

J69 — 2X8_HDR

3,15 H_PWRGD	1 2	H_INIT# 3,15
15,18 SM_INTRUDER#	3 4	H_INTR 3,15
16,18,32 PM_RI#	5 6	PCI_RST# 6,15,23,28,42
	7 8	
	9 10	
15,18 SMB_ALERT#	11 12	H_STPCLK# 3,15
3,15 H_NMI	13 14	
3,15 H_SMI#	15 16	H_CPUSLP# 3,15

J70 — 6Pin_HDR

14,16 PM_STPPCI#	1	
16,41 PM_SLP_S5#	2 3	
3,6,15 H_DPSLP#	4 5	
16,36,38 PM_DPRSLPVR	6	

J85 — 2X8_HDR

14,16,36,38 PM_STPCPU#	1 2	INT_IRQ14 15,18,23
	3 4	INT_IRQ15 15,18,23
9,16 PM_C3_STAT#	5 6	
	7 8	
16,36 VR_PWRGD_ICH	9 10	
	11 12	
	13 14	PM_CLKRUN# 16,18,29,31
	15 16	PM_SLP_S4# 16,29,41

J68 — 8Pin HDR — SIO Sidebands

41 IDE_PPWR_EN	1 2	FWH_WP# 16,28
24,31 IDE_SPWR_EN#	3 4	FWH_TBL# 16,28
	5 6	
	7 8	

TEST HEADER

J84 — 8Pin HDR

16,29,31,33 SMC_EXTSMI#	1 2	PM_CPUPERF# 16
36 IMVP_PWRGD	3 4	PM_SUS_CLK 16
16 PM_GMUXSEL	5 6	AGP_SUSPEND# 16
	7 8	

J33 — 15x2_HDR

5,16,18,29 PM_THRM#	1 2	SMC_RUNTIME_SCI# 16,29,33
16,29 PM_PWRBTN#	3 4	SMC_WAKE_SCI# 16,29,33
29,41 SMC_ONOFF#	5 6	FAN_ON 29,35
29,37 VR_ON	7 8	SMB_THRM_CLK 5,29
16,18,22,29,36 PM_PWROK	9 10	SMB_THRM_DATA 5,29
	11 12	
16,18,29 PM_RSMRST#	13 14	SMB_SB_CLK 29,33,41
29,41 AC_PRESENT#	15 16	SMB_SB_DATA 29,33,41
	17 18	SMB_SB_ALRT# 29,33,41
14,16,22,29,40,41 PM_SLP_S3#	19 20	PM_BATLOW# 16,29,33
	21 22	
29,41 SMC_SHUTDOWN	23 24	
29 BAT_SUSPEND	25 26	
29 SMC_RSTGATE#	27 28	SMB_SC_INT# 29
21,29,33 DOCK_INTR#	29 30	

SMC Sidebands for LPC Power Management

NO STUFF

GROUND HEADERS

J96 J40 J49 J82 J15 J95 J11 J34 J39

17,18,19,20,24,40,41 +V5 — R210 0.01 1% — +V5_LPCSLOT — C270 22UF — C261 0.1UF

+V3.3 7,9,15,17,20,24,27,29,32,36,40,41 — R233 0.01 1% — +V3.3_LPCSLOT — C287 22UF — C218 0.1UF — C220 0.1UF — C276 0.1UF

Title	LPC Slot & Debug Headers		
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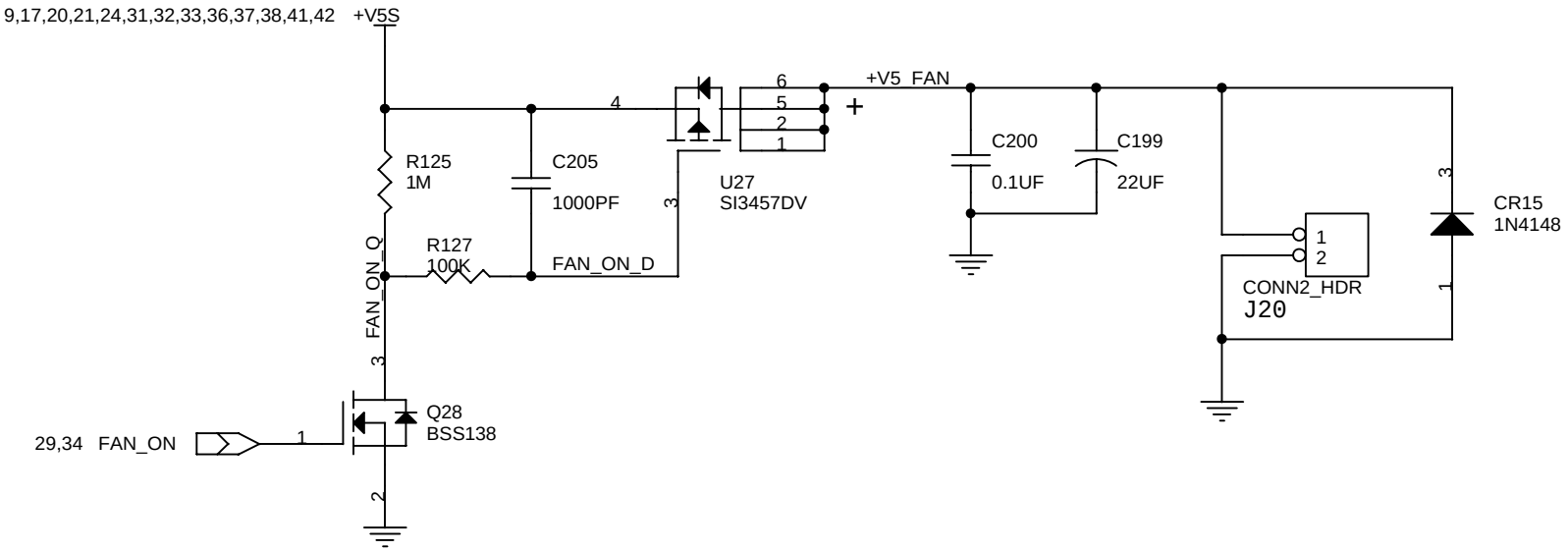
Fan Power Control



Title: Fan Circuit			
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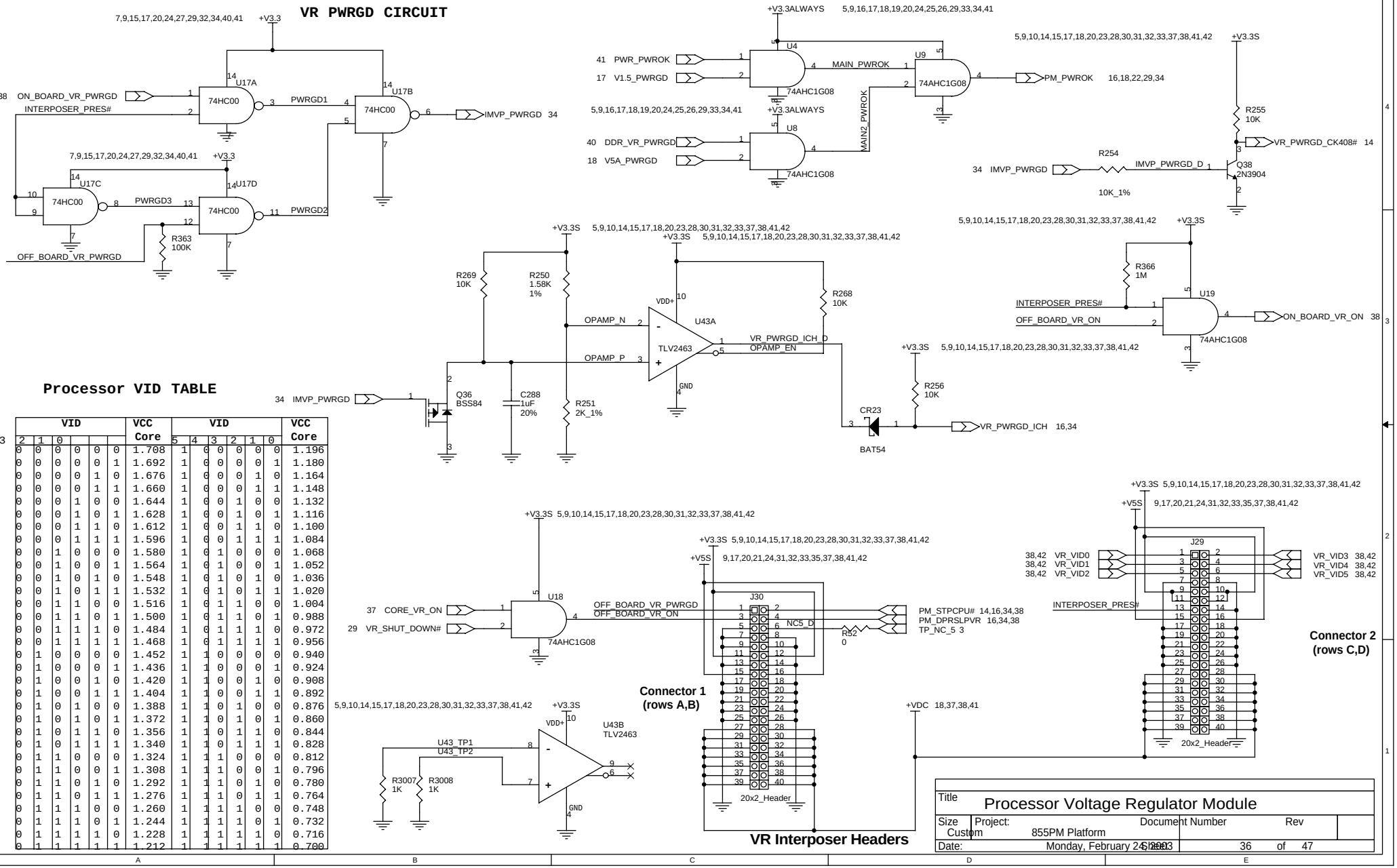
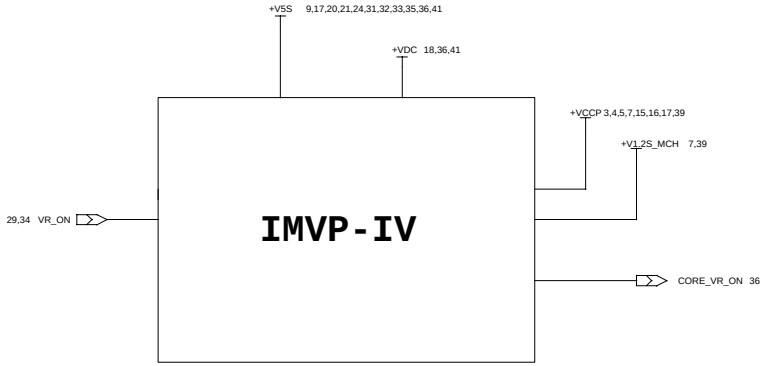


VID						VCC Core	VID						VCC Core
2	1	0					5	4	3	2	1	0	
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

855PM Core and Processor IO VR's (+VCCP)



Title: 855PM VR AND VCCP			
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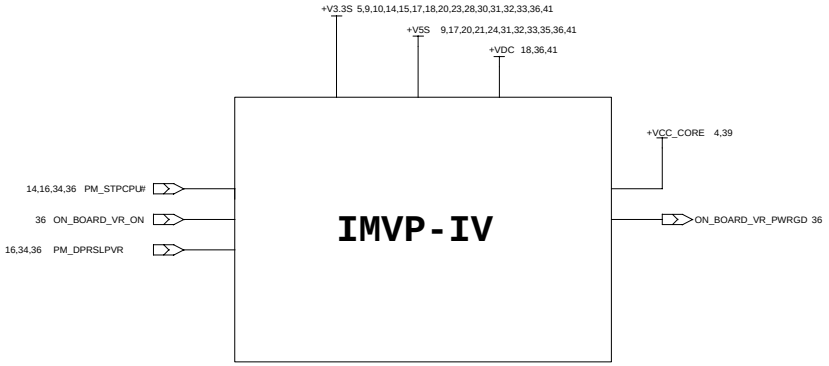
IMVP-IV Core VR



Title: IMVP-IV VR Controller			
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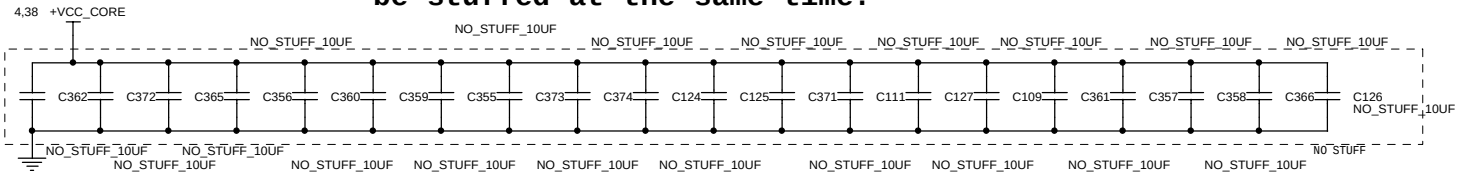
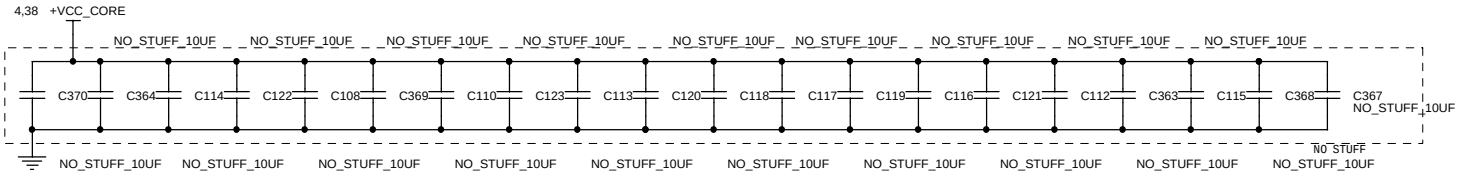
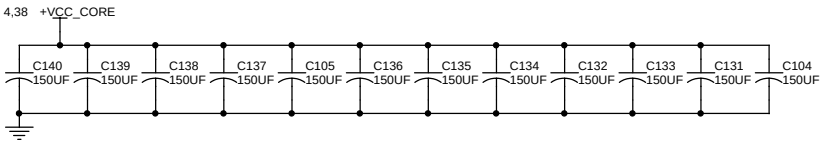
VCore HF and Bulk Decoupling

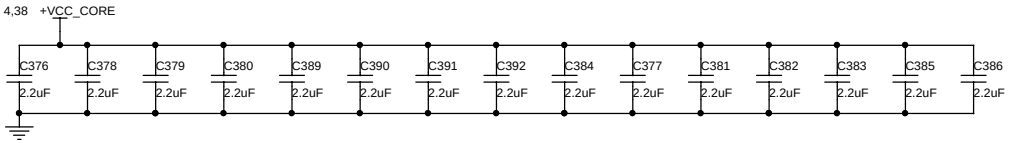
This solution will allow any of the decoupling options. All caps should NOT be stuffed at the same time.



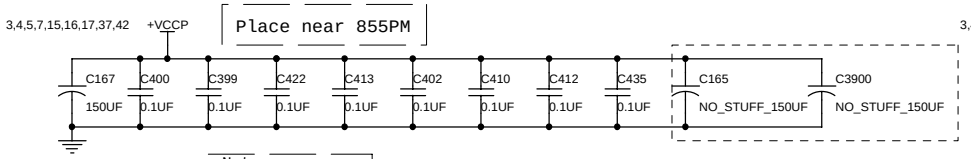


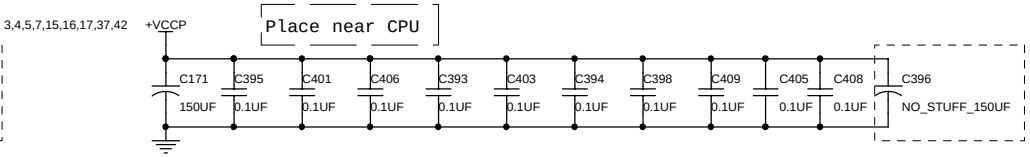


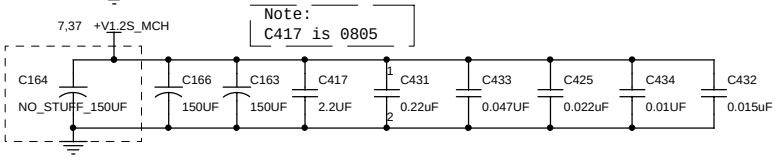
Bulk decoupling values are tuned to Intels IMVP-IV 2Phase VR design. Circuits using other converter topologies may have different requirements.



Note:
2.2uF Caps are 0612 geometry







Title: Decoupling			
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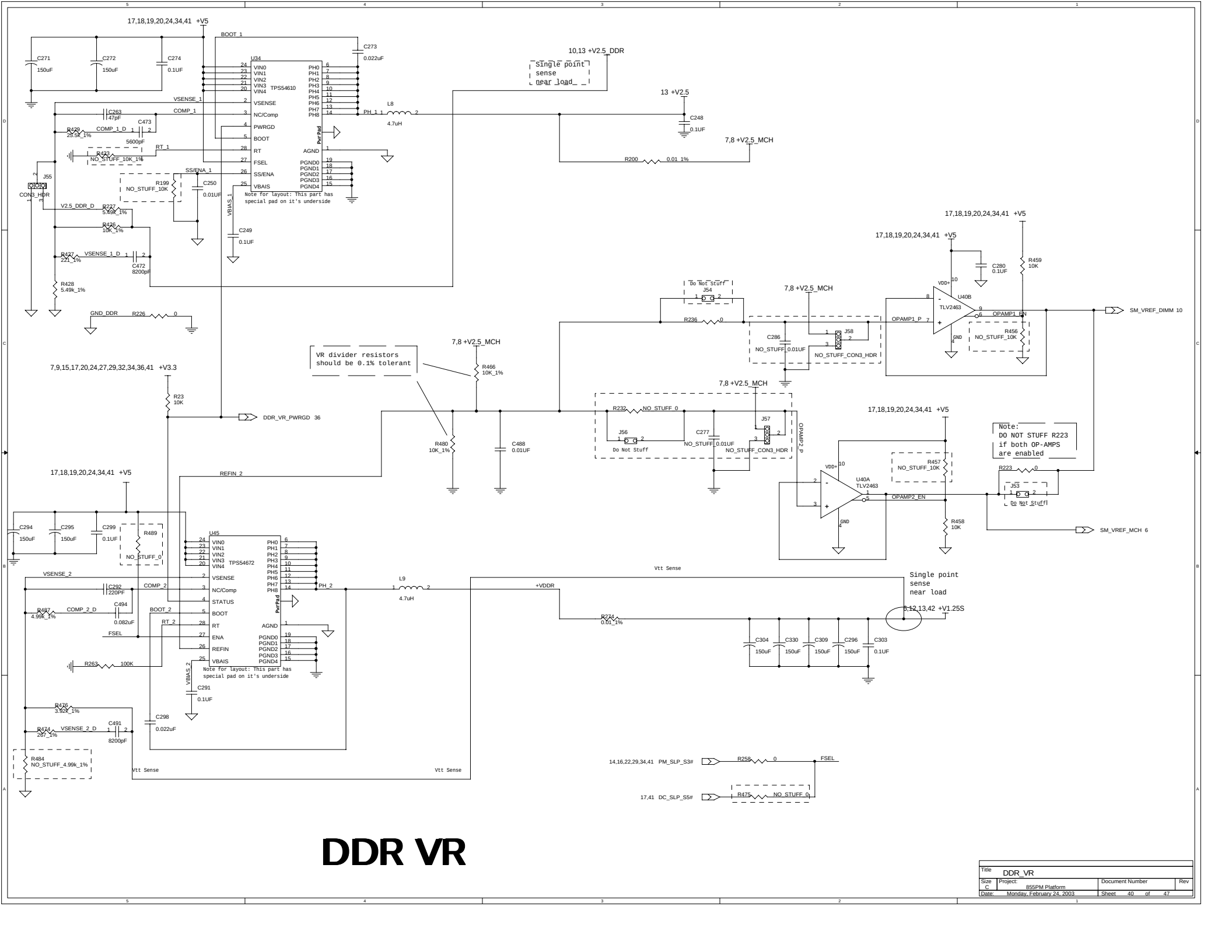

DDR VR

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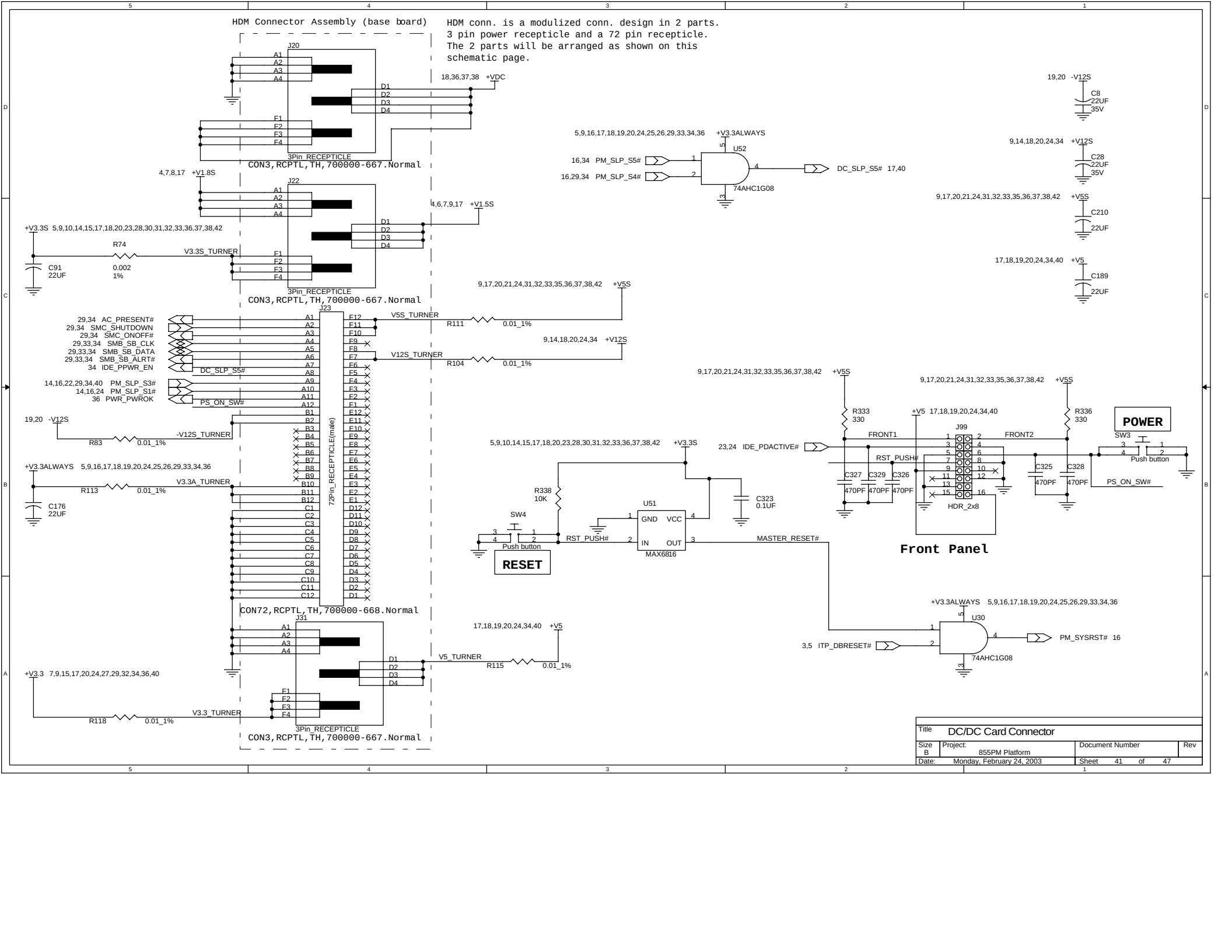
HDM Connector Assembly (base board)

HDM conn. is a modulized conn. design in 2 parts.
3 pin power recepticle and a 72 pin recepticle.
The 2 parts will be arranged as shown on this
schematic page.



Title	DC/DC Card Connector		
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Title	DEBUG LOGIC		
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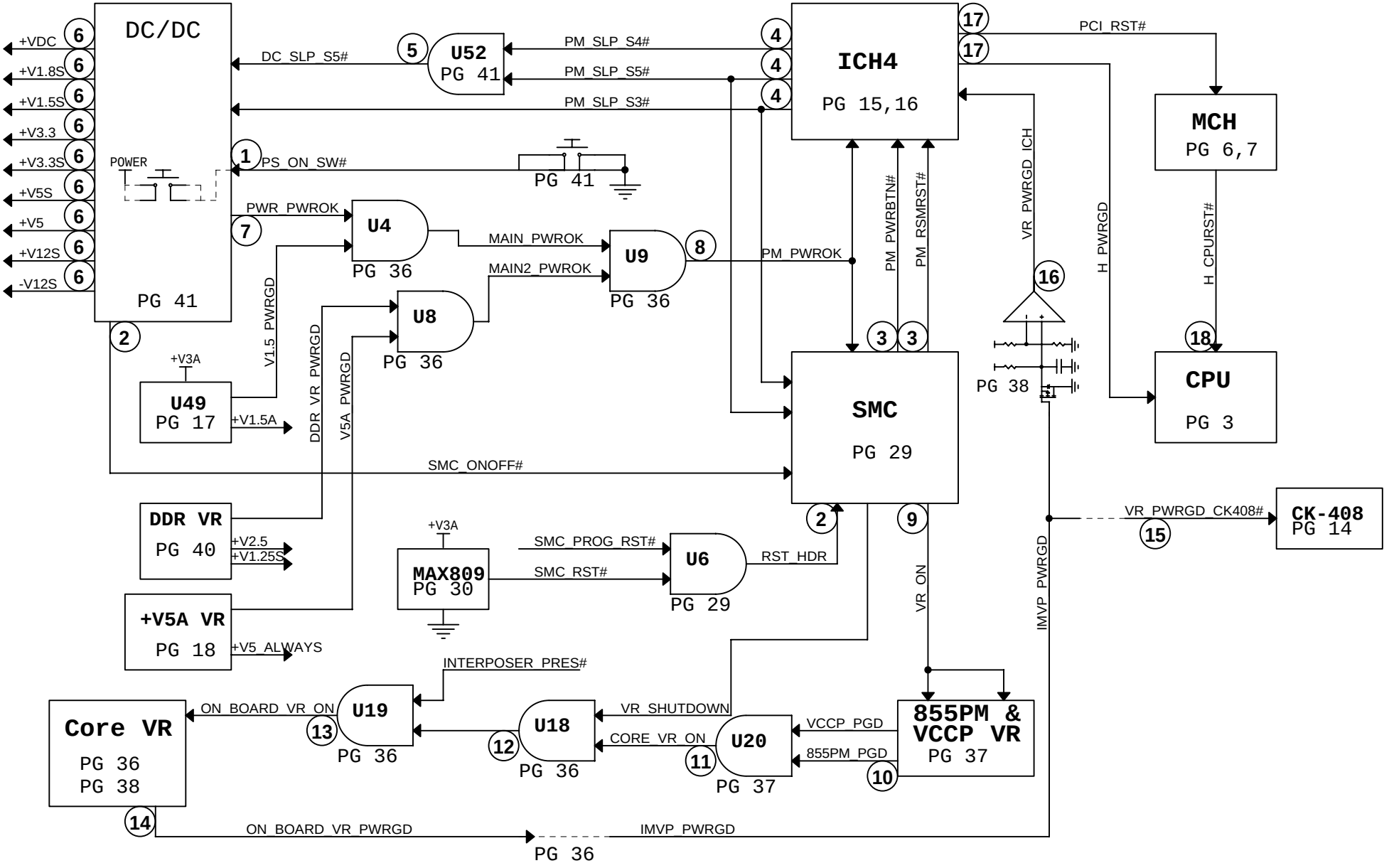
Power On Sequence



Title: Power On Checklist			
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