Z8060/Z8560
FIFO Buffer Unit

October 1988

FEATURES

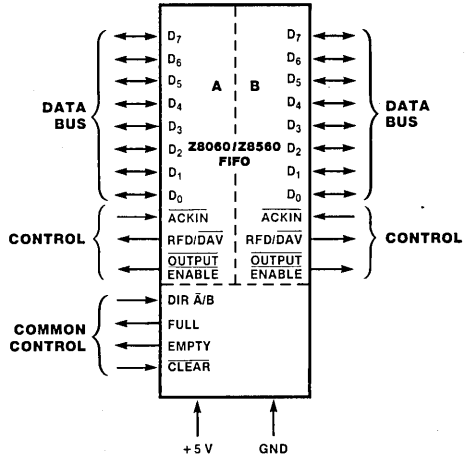
- Bidirectional, asynchronous data transfer capability.
- Large 128-bit-by-8-bit buffer memory.
- Two-wire, interlocked handshake protocol.
- Wire-ORing of empty and full outputs for sensing of multiple-unit buffers.
- 3-state data outputs.
- Connects any number of FIFOs in series to form buffer of any desired length.
- Connects any number of FIFOs in parallel to form buffer of any desired width.

GENERAL DESCRIPTION

The Z8060/Z8560 First-In First-Out (FIFO) Buffer Units consist of a 128-bit-by-8-bit memory, bidirectional data transfer and handshake logic. The structure of the FIFO unit is similar to that of other available buffer units. FIFO is a general-purpose unit; its handshake logic is compatible with that of other members of Zilog's Z8® and Z8000® Families.

FIFOs can be cascaded end-to-end without limit to form a parallel 8-bit buffer of any desired length (in 128-byte increments). Any number of single- or multiple-unit FIFO serial buffers can be connected in parallel to form buffers of any desired width (in 8-bit increments).

The FIFO buffer units are available as 28-pin packages. Figures 1 and 2 show the pin functions and pin assignments, respectively, of the FIFO device. A block diagram is shown in Figure 3.



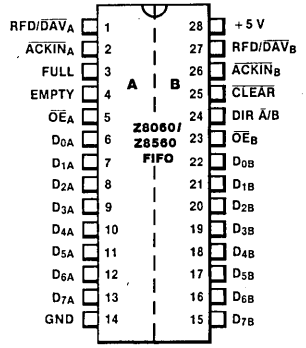


Figure 2. FIFO Pin Assignments

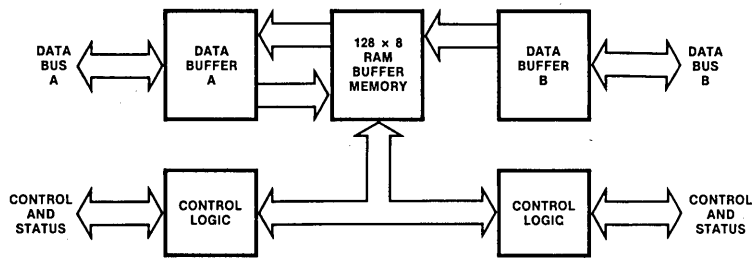


Figure 3. Functional Block Diagram

PIN DESCRIPTIONS

$\overline{\text{ACKIN}}$. *Acknowledge Input* (input, active Low). This line signals the FIFO that output data has been received by peripherals or that input data is valid.

$\overline{\text{CLEAR}}$. *Clear Buffer* (input, active Low). When set to Low, this line causes all data to be cleared from the FIFO buffer.

D_0-D_7. *Data Bus* (inputs/outputs, bidirectional). These bidirectional lines are used by the FIFO to receive and to transmit data.

DIR $\overline{\text{A}}$/B. *Direction Input A/B* (input, two control states). A High on this line signals that input data is to be received at Port B. A Low on this line signals that input data is to be received at Port A.

EMPTY. *Buffer Status* (output, active High, open-drain). A High on this line indicates that the FIFO buffer is empty.

FULL. *Buffer Status* (output, active High, open-drain). A High on this line indicates that the FIFO buffer is full.

$\overline{\text{OEA}}$, $\overline{\text{OEB}}$. *Output Enable A, Output Enable B* (inputs, active Low). When Low, $\overline{\text{OEA}}$ enables the bus drivers for Port A; when High, $\overline{\text{OEA}}$ causes the bus drivers to float to a high-impedance level. Input $\overline{\text{OEB}}$ controls the bus drivers for Port B in the same manner as $\overline{\text{OEA}}$ controls those for Port A.

RFD/$\overline{\text{DAV}}$. *Ready-for-Data/Data Available* (outputs RFD, active High; $\overline{\text{DAV}}$ active Low). RFD, when High, signals to the peripherals involved that the FIFO is ready to receive data. $\overline{\text{DAV}}$, when Low, signals to the peripherals involved that FIFO has data available to send.

FUNCTIONAL DESCRIPTION

Interlocked 2-Wire Handshake. In interlocked 2-wire handshake operation, the action of FIFO must be acknowledged by the other half of the handshake before the next action can occur. In an Output Handshake mode, the FIFO indicates that new data is available only after the external device has indicated that it is ready for the data. In an Input Handshake mode, the FIFO does not indicate that it is ready for new data until the data source indicates that the previous byte of the data is no longer available, thereby acknowledging the acceptance of the last byte. This control feature allows the FIFO, with no external logic, to directly interface with the port of any CPU in the Z8 Family—a CIO, a UPC, an Z-FIO, or another FIFO. The timing for the input and output handshake operations is shown in Figures 4 and 5, respectively.

Resetting or Clearing the FIFO. The $\overline{\text{CLEAR}}$ input is used to initialize and clear the FIFO. A Low level on this input clears all data from the FIFO, allows the EMPTY output to go High and forces both outputs RFD/$\overline{\text{DAV}}_A$ and RFD/$\overline{\text{DAV}}_B$ High. A High level on $\overline{\text{CLEAR}}$ allows the data to transfer through the FIFO.

Bidirectional Transfer Control. The FIFO has bidirectional data transfer capability under control of the DIR $\overline{\text{A}}$/B input. When DIR $\overline{\text{A}}$/B is set Low, Port A becomes input handshake and Port B becomes output handshake; data transfers are then made from Port A to Port B. Setting DIR $\overline{\text{A}}$/B High reverses the handshake assignments and the direction of transfer. This bidirectional control is illustrated in Table 1.

Table 1. Bidirectional Control Function Table

DIR $\overline{\text{A}}$/B	Port A Handshake	Port B Handshake	Transfer
0	Input	Output	A to B
1	Output	Input	B to A

The FIFO buffer must be empty before the direction of transfer is changed; otherwise, the results of the change will be unpredictable. If FIFO status is unknown when a transfer direction change is to be made, the recommended procedure is:

(1) Force and hold $\overline{\text{CLEAR}}$ Low.

(2) Set DIR $\overline{\text{A}}$/B to the level required for the desired direction.

(3) Force $\overline{\text{CLEAR}}$ High.

Empty and Full Operation. The EMPTY and FULL output lines can be wire-ORed with the EMPTY and FULL lines of other FIFOs and Z-FIOs. This capability enables the user to determine the empty/full status of a buffer consisting of multiple FIFOs, Z-FIOs, or a combination of both. Table 2 shows the various states of EMPTY and FULL.

Table 2. Signals EMPTY and FULL Operation Table

Number of Bytes in FIFO	EMPTY	FULL
0	High	Low
1-127	Low	Low
128	Low	High

Interconnection Example. Figure 6 illustrates a simplified block diagram showing the manner in which FIFOs can be interconnected to extend a Z-FIO buffer.

Output Enable Operation. The FIFO provides a separate Output Enable ($\overline{\text{OE}}$) signal for each port of the buffer. An $\overline{\text{OE}}$ output is valid only when its port is in the Output Handshake mode. The control of this output function is shown in Table 3. Signal $\overline{\text{OE}}$ operates with lines DIR $\overline{\text{A}}$/B. A High on a valid $\overline{\text{OE}}$ line 3-states its port's data bus but does not affect the handshake operation. A Low level on a valid $\overline{\text{OE}}$ enables the data bus outputs if its port is in the Output Handshake mode. Note that the handshake operation is unaffected by the Output Enable pin.

Table 3. Output Control Function Table

DIR $\overline{\text{A}}$/B	$\overline{\text{OE}}_A$	$\overline{\text{OE}}_B$	Function
0	X	0	Disable Port A Output Enable Port B Output
0	X	1	Disable Port A Output Disable Port B Output
1	0	X	Enable Port A Output Disable Port B Output
1	1	X	Disable Port A Output Disable Port B Output

NOTE: X = Don't care.

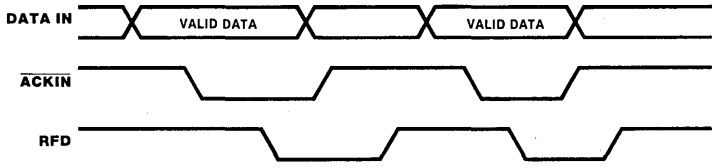


Figure 4. Two-Wire Interlocked Handshake Timing (input)

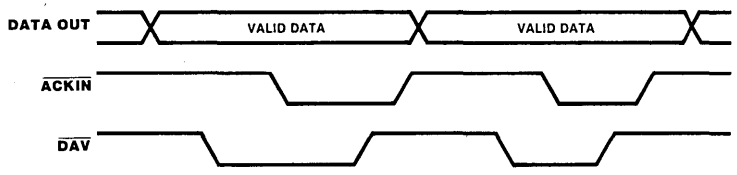


Figure 5. Two-Wire Interlocked Handshake Timing (output)

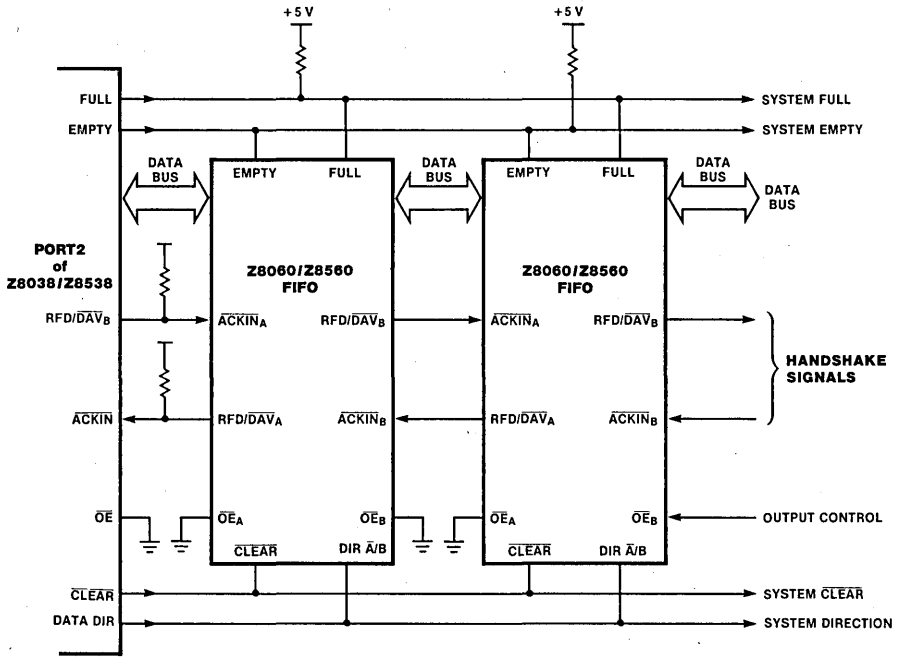


Figure 6. Typical Interconnection (Simplified Diagram)

ABSOLUTE MAXIMUM RATINGS

Voltages on all pins with respect to GND . . . . . −0.3V to +7V
Operating Ambient Temperature. . . . . .See Ordering Information
Storage Temperature . . . . . −65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The AC characteristics and capacitance sections listed below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Standard conditions are as follows:

- $+4.75V \leq V_{CC} \leq +5.25V$
- GND = 0V
- T_A as specified in Ordering Information. All AC parameters assume a load capacitance of 50 pf max.

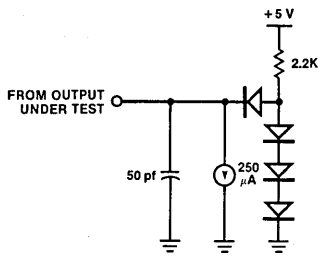


Figure 7. Standard Test Load

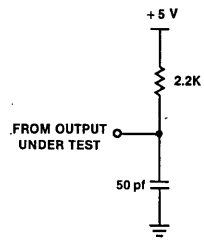


Figure 8. Open-Drain Test Load

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0	$V_{CC}+0.3$	V	
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -250\,\mu A$
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.0$ mA
			0.5	V	$I_{OL} = 3.2$ mA
I_{IL}	Input Leakage		±10	μA	$0.4 \leq V_{IN} \leq 2.4V$
I_{OL}	Output Leakage		±10	μA	$0.4 \leq V_{OUT} \leq 2.4V$
I_{CC}	V_{CC} Supply Current		200	mA	

NOTE: $V_{CC} = +5V \pm 5\%$ unless otherwise specified over specified temperature range.

CAPACITANCE

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance		10	pf
C_{OUT}	Output Capacitance		15	pf
$C_{I/O}$	Bidirectional Capacitance		20	pf
Input				
tr	Any input rise time		100	ns
tf	Any input fall time		100	ns

Over specified temperature range; f = 1 MHz.
Unmeasured pins returned to ground.

2-WIRE INTERLOCKED HANDSHAKE TIMING

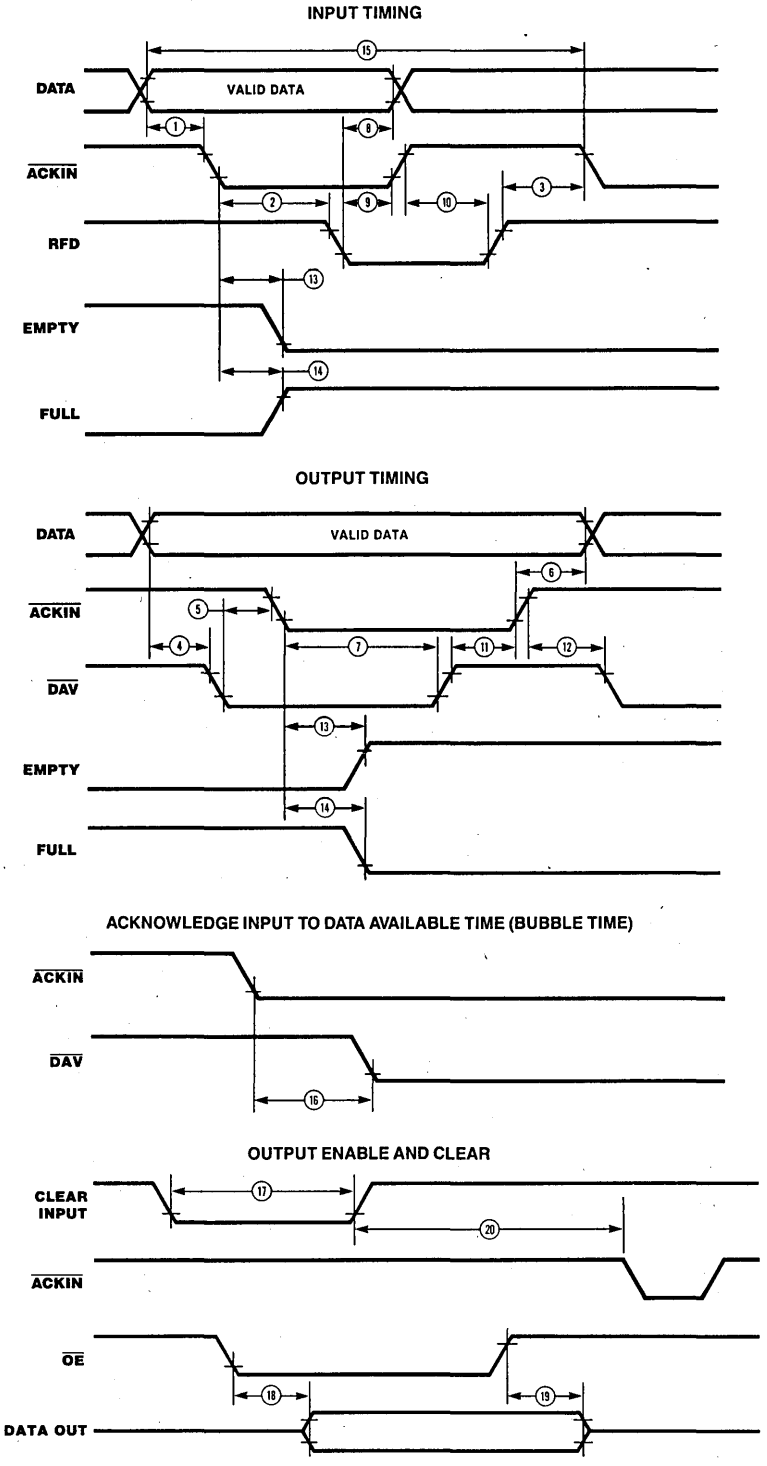


Figure 9. Timing Diagrams

FIFO 2-Wire Handshake Timing. Timing for 2-wire interlocked handshake operation is shown in Figure 9. The symbol, description and values for the numbered parameters (Figure 9) are given in AC Characteristics.

AC CHARACTERISTICS

Number	Symbol	Parameter	Min	Max	Units*
1	TsDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ to Setup ime	50		ns
2	TdACKf(RFD)	$\overline{ACKIN}$ ↓ to RFD ↓ Delay		500	ns
3	TdRFDr(ACK)	RFD ↑ to $\overline{ACKIN}$ ↓ Delay	0		ns
4	TsDO(DAV)	Data Out to $\overline{DAV}$ ↓ Setup Time	50		ns
5	TdDAVf(ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ Delay	0		ns
6	ThDO(ACK)	Data Out to $\overline{ACKIN}$ ↑ Hold Time	50		ns
7	TdACK(DAV)	$\overline{ACKIN}$ ↓ to DAV ↑ Delay		500	ns
8	ThDI(RFD)	Data Input to RFD ↓ Hold Time	0		ns
9	TdRFDf(ACK)	RFD ↓ to $\overline{ACKIN}$ ↑ Delay	0		ns
10	TdACKr(RFD)	$\overline{ACKIN}$ ↑ to RFD ↑ Delay		400	ns
11	TdDAVr(ACK)	$\overline{DAV}$ ↑ to $\overline{ACKIN}$ ↑	0		ns
12	TdACKr(DAV)	$\overline{ACKIN}$ ↑ to $\overline{DAV}$ ↓		800	ns
13	TdACKINf(EMPTY)	(Input) $\overline{ACKIN}$ ↓ to EMPTY ↓ Delay (Output) $\overline{ACKIN}$ ↓ to EMPTY ↑ Delay		600	ns
14	TdACKINf(FULL)	(Input) $\overline{ACKIN}$ ↓ to FULL ↑ Delay (Output) $\overline{ACKIN}$ ↓ to FULL ↓ Delay		600	ns
15	ACKIN Clock Rate	(Input or Output)		1.0	MHz
16	TdACKINf(DAVf)	(Bubble Time)		1000	ns
17	TwCLR	Width of Clear to Reset FIFO	700		ns
18	TdOE(DO)	$\overline{OE}$ ↓ to Data Bus Driven		210	ns
19	TdOE(DRZ)	$\overline{OE}$ ↑ to Data Bus Float		150	ns
20	TdCLR(ACK)	$\overline{CLEAR}$ ↑ to $\overline{ACKIN}$ ↓		800	ns

*All timing references assume 2.0V for a logic 1 and 0.8V for a logic 0. Timings are preliminary and subject to change.