

W89C840F



FAST ETHERNET CONTROLLER WITH PCI AND MII INTERFACE

GENERAL DESCRIPTION

The W89C840F is a highly integrated Ethernet LAN controller for both 100BASE and 10BASE Ethernet. It provides host bus interface complying with the PCI Local Bus Specification revision 2.1, and the MII interface complying with the IEEE 802.3u standard for easily implementing an Ethernet LAN adapter. The built in 2K bytes transmit FIFO and 4K bytes receive FIFO, controlled by the on-chip bus master, are designed for improving network performance and the host bus utilization.

The on-chip DMA controller handles the data transfer between the system memory and the FIFOs. The data received from network are queued into the received FIFO and, then, moved into the system memory through the PCI bus directly. On the other hand, the transmit data are fetched from the system memory and queued into the transmit FIFO directly. No extra memory devices are needed for data buffering during the transmit and receive operation.

Up to 31 internal registers, including host bus control registers, direct memory access(DMA) control registers, media access(MAC) control registers and signature identification registers, are implemented for system configuring. All of these long word accessible registers perform the status report and the precisely control on the transmit and receive operation. It also provides an extra channel for the on-line application program to update the on board expansion ROM device in some specific application environment.

FEATURES

- Complies with IEEE802,3, IEEE802.3 u, ANSI 8802-3, and Ethernet standards
- Complies with the PCI Ver. 2.1 standard
- Prefetch function on both path of transmit and receive
- Both half duplex and full duplex mode available
- Independent deep receive and transmit FIFO available
- Early interrupt function available for transmitting and receiving
- Flexible data structure for host compatibility and speeding system performance
- Supports 25 to 33 MHz PCI clock speed
- Implemented PCI bus master for direct memory access, no on-board memory is required
- Supports MII management function
- Supports EEPROM and Flash on line read/ write function
- Supports boot ROM on-line read function
- Supports both big and little endian byte ordering for descriptor and buffer

- Flexible address filtering modes
 - 64-bit hash-table and one perfect address
 - all multicast
 - promiscuous
- Provides an boot ROM interface of up to 256K bytes
- Supports configuration registers autoloading function
- Internal/external loopback mode for diagnostic
- Two LED support for status indication
- single +5V power supply and 100 pins PQFP package

 **Back to Index**