

**W83667HG-A**  
**Nuvoton LPC I/O**

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## **1. GENERAL DESCRIPTION**

The W83667HG-A is a member of Nuvoton's LPC Super I/O product line for desktop PCs. This family features an Intel® PECEI (Platform Environment Control Interface) port for direct connection to the CPU for digital temperature information. For CPUs without PECEI functionality, the W83667HG-A connects to the standard CPU thermal diode using the advanced dual current source method to increase accuracy and ease layout requirements.

The W83667HG-A also includes a PC health monitoring function to measure system voltages and temperatures and report these to the operating system. The W83667HG-A also supports the Smart Fan control system, including "SMART FAN™ I", "SMART FAN™ III" and "SMART FAN™ IV", to control cooling fans based on the measured temperatures. This Nuvoton innovation provides an easy to implement cooling solution with maximum safety and flexibility.

The W83667HG-A implements a complete range of legacy interface components as described below.

The W83667HG-A supports four – 360K, 720K, 1.2M, 1.44M, or 2.88M – floppy disk drivers with data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2Mb/s. The disk drive adapter supports the functions of floppy disk driver controller (compatible with the industry standard 82077/NEC765), data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic.

The W83667HG-A provides two high-speed serial communication ports (UARTs), one of which implements IR functions - IrDA 1.0 with SIR at 1.152K bps. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. Both UARTs support legacy speeds up to 115.2K bps as well as higher baud rate of 230K, 460K, or 921K bps to support high speed modems.

The W83667HG-A supports the PC-compatible parallel printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP).

The W83667HG-A provides a serial flash ROM interface that supports up to 64M bits serial flash ROM eliminating the need for older, more expensive parallel flash for BIOS storage.

The W83667HG-A provides flexible I/O control functions through a set of 66 general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The W83667HG-A fully complies with the Microsoft© PC98 and PC99 Hardware Design Guides and meets the requirements of ACPI.

The configuration registers inside the W83667HG-A support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows 95/98/2000/XP™, making the allocation of the system resources more efficient than ever.

One special characteristic of the Super I/O product line is the separation of the power supply in normal operation from that in standby operation. Please pay attention to the layout of these two power supplies to avoid short circuits. Otherwise, the feature will not function.

## 2. FEATURES

### General

- Comply with LPC specification 1.1 version
- Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
- Integrated hardware monitor functions
- Compliant with Microsoft PC2000/PC2001 Hardware Design Guide
- Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
- Programmable configuration settings
- Single 24- or 48-MHz clock input
- Support selective pins of 5 V tolerance

### FDC

- Variable write pre-compensation with track-selection capability
- Support vertical recording format
- DMA-enable logic
- 16-byte data FIFOs
- Support floppy disk drivers and tape drives
- Detect all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD-write enable signal (write data signal forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Compatible with industry standard 82077
- 360K / 270K / 1.2M / 1.44M / 2.88M formats
- 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD and its Windows driver

### UART

- Two high-speed, 16550-compatible UARTs with 16-byte send / receive FIFOs
- Fully programmable serial-interface characteristics:
  - 5, 6, 7 or 8-bit characters
  - Even, odd or no parity bit generation/detection
  - 1, 1.5 or 2 stop-bit generation
- Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Programmable baud rate generator allows division of clock source by any value from 1 to ( $2^{16}-1$ )
- Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24MHz is 1.5M bps.

### Parallel Port

- Compatible with IBM parallel port
- Support PS/2-compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

### Keyboard Controller

- 8042-based keyboard controller
- Asynchronous Access to two data registers and one status register
- Software-compatible with 8042
- Support PS/2 mouse
- Support Port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 12MHz operating frequency

### Hardware Monitor Functions

- Smart Fan control system, supporting the functions of SMART FAN™ I – “Thermal Cruise™” and “Speed Cruise™” modes, “SMART FAN™ III”, and “SMART FAN™ IV”
- Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in SMART FAN™ I, SMART FAN™ III and SMART FAN™ IV
- Three thermal inputs from the different combinations of remote thermistors, and the thermal diode output
- Support Current Mode (dual current source) temperature sensing method
- Eight voltage inputs (CPUVCORE, VIN[0..2] and 3VCC, AVCC, 3VSB, VBAT)
- Five fan-speed monitoring inputs
- Three fan-speed controls
- Dual mode for fan control (PWM and DC)
- Built-in caseopen detection circuit
- Built-in SKTOCC detection circuit
- Programmable hysteresis and setting points for all monitored items
- Over-temperature indicator output
- Issue SMI#, OVT# to activate system protection
- Nuvoton Hardware Doctor™ support
- Eight VID inputs / outputs control
- BUSSEL inputs / outputs control
- Provide I<sup>2</sup>C interface to read / write Hardware monitor registers
- CPU Vcore protected when CPUVCORE voltage over CPUVCORE reference
- Asus glue logic.

### Serial Peripheral Interface

- Support up to 64Mbits SPI Flash Memory with clock up to 33 MHz

**Infrared**

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,6000 bps

**General Purpose I/O Ports**

- 72 programmable general purpose I/O ports
- GPIO port 4 supports the optional functions of Watchdog Timer Out and Suspend LED output
- GP37, GP50 and GP53 can distinguish whether the input pins undergo any transitions by reading the registers. All of the 3 GPIOs can assert PSOUT# or PME# to wake up the system if each of them undergoes any transition.

**OnNow Functions**

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

**PECI Interface**

- Support PECI 1.0 and 1.1a Specification
- Support 4 CPU addresses and 2 domains per CPU address

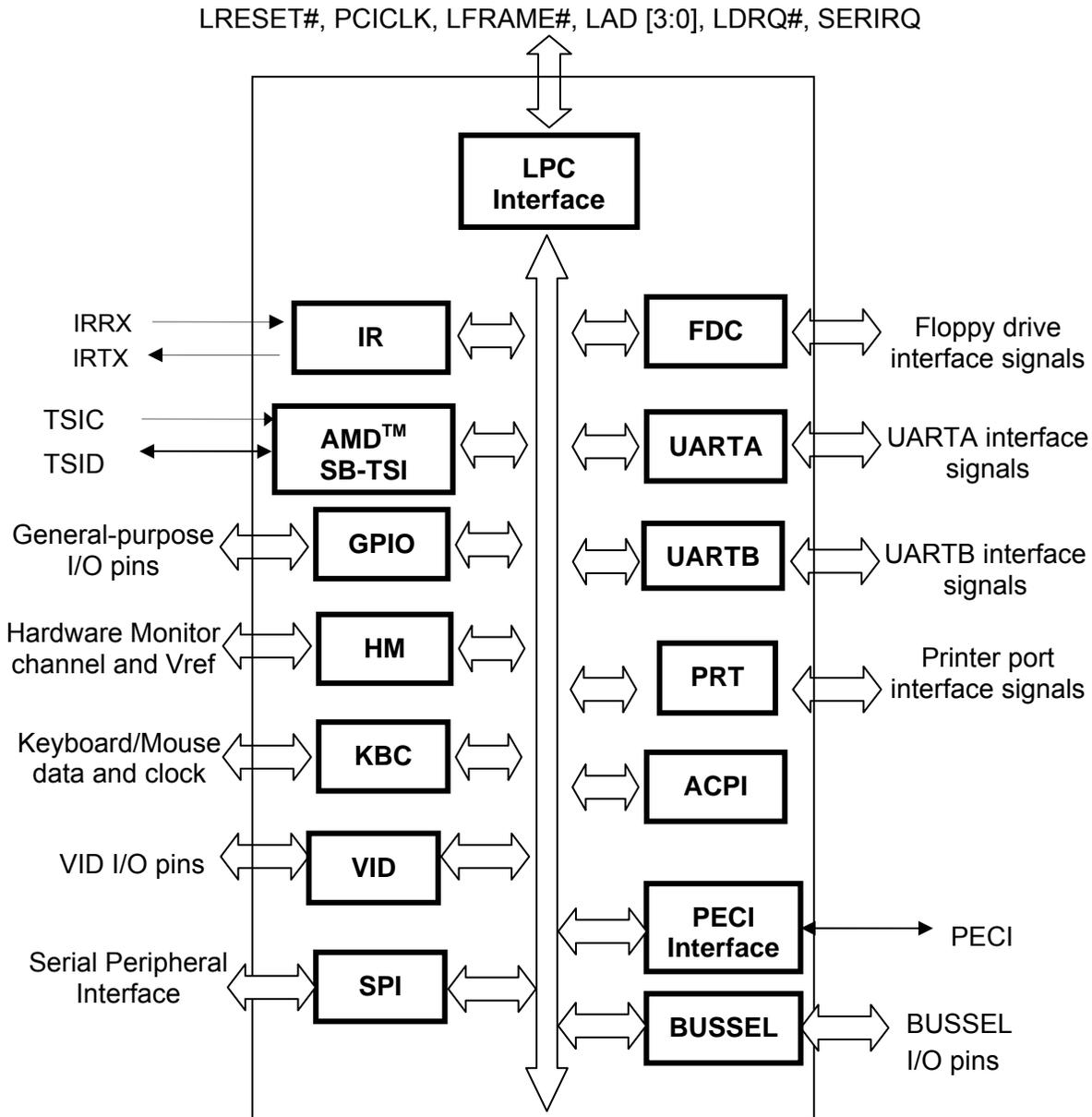
**AMDTM SB-TSI Interface**

- Support AMD™ SB-TSI Specification

**Package**

- 128-pin QFP
- Pb-free / Green-compliant

3. BLOCK DIAGRAM



W83667HG-A

Figure 3-1 W83667HG-A Block Diagram

4. PIN LAYOUT

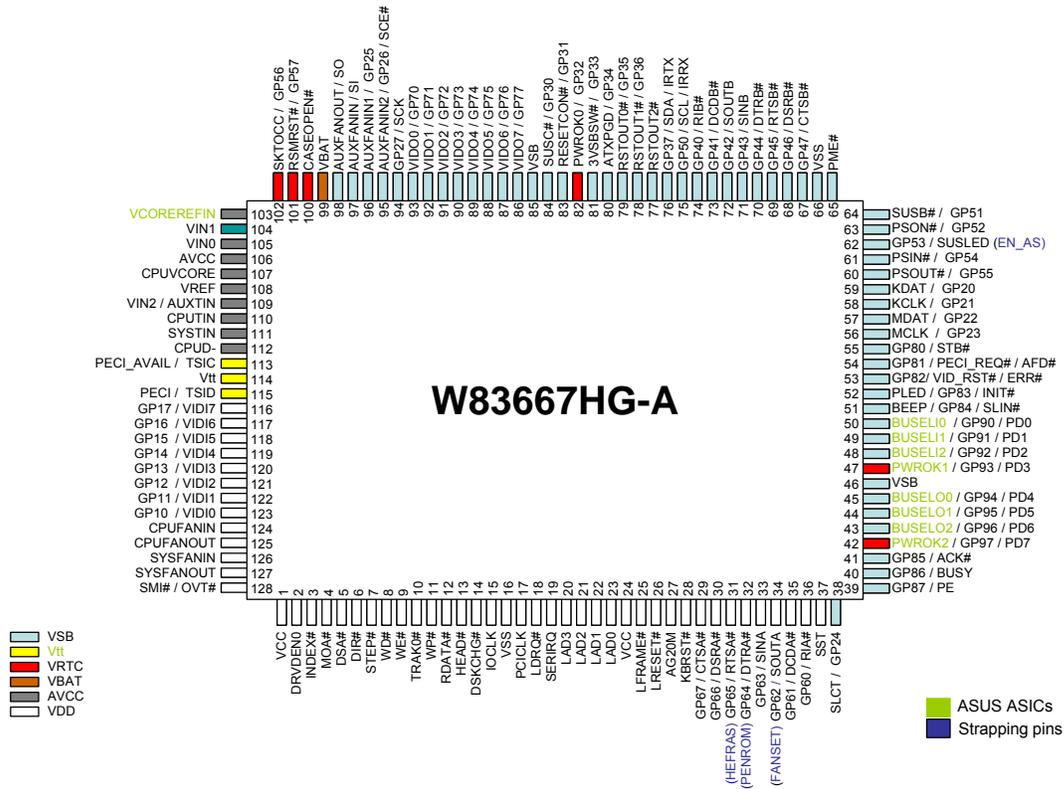


Figure 4-1 W83667HG-A Pin Layout

## 5. PIN DESCRIPTION

**Note:** Please refer to [22.2 DC CHARACTERISTICS](#) for details.

AOUT	- Analog output pin
AIN	- Analog input pin
IN <sub>cd</sub>	- CMOS-level input pin with internal pull-down resistor
IN <sub>cu</sub>	- CMOS-level input pin with internal pull-up resistor
IN <sub>cs</sub>	- CMOS-level, Schmitt-trigger input pin
IN <sub>csu</sub>	- CMOS-level, Schmitt-trigger input pin with internal pull-up resistor
IN <sub>t</sub>	- TTL-level input pin
IN <sub>g</sub>	- GTL-level input pin
IN <sub>td</sub>	- TTL-level input pin with internal pull-down resistor
IN <sub>ts</sub>	- TTL-level, Schmitt-trigger input pin
IN <sub>tp3</sub>	- 3.3V TTL-level input pin
IN <sub>tsp3</sub>	- 3.3V TTL level Schmitt-trigger input pin
IN <sub>tu</sub>	- TTL-level input pin with internal pull-up resistor
I/O <sub>8</sub>	- bi-directional pin with 8-mA source-sink capability
I/O <sub>8t</sub>	- TTL-level, bi-directional pin with 8-mA source-sink capability
I/O <sub>12</sub>	- bi-directional pin with 12-mA source-sink capability
I/O <sub>12t</sub>	- TTL-level, bi-directional pin with 12-mA source-sink capability
I/O <sub>12ts</sub>	- Schmitt-trigger, bi-directional pin with 12-mA source-sink capability
I/O <sub>12tp3</sub>	- 3.3V, TTL-level, bi-directional pin with 12-mA source-sink capability
I/OD <sub>8t</sub>	- TTL-level, bi-directional pin. Open-drain output with 8-mA sink capability
I/OD <sub>12</sub>	- Bi-directional pin. Open-drain output with 12-mA sink capability
I/OD <sub>12t</sub>	- TTL-level bi-directional pin. Open-drain output with 12-mA sink capability
I/OD <sub>12cs</sub>	- CMOS-level, bi-directional, Schmitt-trigger pin. Open-drain output with 12-mA sink capability
I/OD <sub>12ts</sub>	- TTL-level, bi-directional, Schmitt-trigger pin. Open-drain output with 12-mA sink capability
I/OD <sub>12tp3</sub>	- 3.3V, TTL-level, bi-directional pin. Open-drain output with 12-mA sink capability
I/OD <sub>16t</sub>	- TTL-level, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD <sub>16ts</sub>	- Schmitt-trigger, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD <sub>16cs</sub>	- CMOS-level, Schmitt-trigger, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD <sub>24t</sub>	- TTL-level, bi-directional pin. Open-drain output with 24-mA sink capability
O <sub>12p3</sub>	- 3.3V output pin with 12-mA source-sink capability
O <sub>12pt3</sub>	- 3.3V, TTL-level output pin with 12-mA source-sink capability <sub>12p3</sub>
O <sub>8</sub>	- TTL-level output pin with 8-mA source-sink capability
O <sub>12</sub>	- TTL-level output pin with 12-mA source-sink capability
O <sub>24</sub>	- TTL-level output pin with 24-mA source-sink capability
OD <sub>8</sub>	- Open-drain output pin with 8-mA sink capability
OD <sub>12</sub>	- Open-drain output pin with 12-mA sink capability
OD <sub>24</sub>	- Open-drain output pin with 24-mA sink capability
I <sub>v3</sub>	- Input pin with source capability of 6 mA and sink capability of 1 mA
I/O <sub>v3</sub>	- Bi-direction pin with source capability of 6 mA and sink capability of 1 mA

## 5.1 LPC Interface

SYMBOL	PIN	I/O	DESCRIPTION
IOCLK	15	IN <sub>tp3</sub>	System clock input, either 24MHz or 48MHz. The actual frequency must be specified in the register. The default value is 48MHz.
PCICLK	17	IN <sub>tsp3</sub>	PCI-clock 33-MHz input.
LDRQ#	18	O <sub>12p3</sub>	Encoded DMA Request signal.
SERIRQ	19	I/OD <sub>12tp3</sub>	Serialized IRQ input / output.
LAD[3:0]	20 - 23	I/O <sub>12tp3</sub>	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	25	IN <sub>tsp3</sub>	Indicates the start of a new LPC cycle or the termination of a broken cycle.
LRESET#	26	IN <sub>tsp3</sub>	Reset LPC signal. It can be connected to the PCIRST# signal on the host.
PME#	65	OD <sub>12p3</sub>	Generated PME event.

## 5.2 FDC Interface

SYMBOL	PIN	I/O	DESCRIPTION
DRVDENO	2	OD <sub>24</sub>	Drive Density Select bit 0.
INDEX#	3	IN <sub>cs</sub>	Schmitt-trigger input from the disk drive. This signal is active-low when the head is positioned over the index hole. This input pin should be pulled-up with a 1-K $\Omega$ resistor to 5V for Floppy Drive compatibility.
MOA#	4	OD <sub>24</sub>	Motor A On. When set to 0, this pin activates disk drive A. This is an open-drain output.
DSA#	5	OD <sub>24</sub>	Drive Select A. When set to 0, this pin activates disk drive A. This is an open-drain output.
DIR#	6	OD <sub>24</sub>	Direction of the head step motor. An open-drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	7	OD <sub>24</sub>	Step output pulses. This active-low open-drain output produces a pulse to move the head to another track.
WD#	8	OD <sub>24</sub>	Write data. This logic-low open-drain writes pre-compensation serial data to the selected FDD. An open-drain output.
WE#	9	OD <sub>24</sub>	Write enable. An open-drain output.
TRAK0#	10	IN <sub>cs</sub>	Track 0. This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the outermost track. This input pin should be pulled-up with a 1-K $\Omega$ resistor to 5V for Floppy Drive compatibility.

SYMBOL	PIN	I/O	DESCRIPTION
WP#	11	IN <sub>CS</sub>	Write protected. This active-low signal from the disk drive indicates that the diskette is write-protected. This input pin should be pulled-up with a 1-K $\Omega$ resistor to 5V for Floppy Drive compatibility.
RDATA#	12	IN <sub>CS</sub>	The read-data input signal from the FDD. This input pin should be pulled-up with a 1-K $\Omega$ resistor to 5V for Floppy Drive compatibility.
HEAD#	13	OD <sub>24</sub>	Head selection. This open-rain output selects which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	14	IN <sub>CS</sub>	Diskette change. This signal is active-low at power-on and whenever the diskette is removed. This input pin should be pulled-up with a 1-K $\Omega$ resistor to 5V for Floppy Drive compatibility.

### 5.3 Multi-mode Parallel Port

SYMBOL	PIN	I/O	DESCRIPTION
SLCT	38	IN <sub>ts</sub>	PRINTER MODE: SLCT An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
GP24		I/OD <sub>12ts</sub>	General-purpose I/O port 2 bit 4. (Default)
PE	39	IN <sub>ts</sub>	PRINTER MODE: PE An active-high input on this pin indicates that the printer has detected the end of the paper.
GP87		I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 7. (Default)
BUSY	40	IN <sub>ts</sub>	PRINTER MODE: BUSY An active-high input indicates that the printer is not ready to receive data.
GP86		I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 6. (Default)
ACK#	41	IN <sub>ts</sub>	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data.
GP85		I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 5. (Default)
PD7	42	I/O <sub>12ts</sub>	PRINTER MODE: PD7 Parallel port data bus bit 7.
GP97		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 7.
PWROK2		OD <sub>12</sub>	This pin generates the PWRGD signal while VCC is present. (Default)
PD6	43	I/O <sub>12ts</sub>	PRINTER MODE: PD6 Parallel port data bus bit 6. .

SYMBOL	PIN	I/O	DESCRIPTION
GP96		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 6. (Default)
PD5	44	I/O <sub>12ts</sub>	PRINTER MODE: PD5 Parallel port data bus bit 5.
GP95		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 5. (Default)
PD4	45	I/O <sub>12ts</sub>	PRINTER MODE: PD4 Parallel port data bus bit 4.
GP94		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 4. (Default)
PD3	47	I/O <sub>12ts</sub>	PRINTER MODE: PD3 Parallel port data bus bit 3.
GP93		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 3.
PWROK1		OD <sub>12</sub>	This pin generates the PWRGD signal while VCC is present. (Default)
PD2	48	I/O <sub>12ts</sub>	PRINTER MODE: PD2 Parallel port data bus bit 2.
GP92		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 2. (Default)
PD1	49	I/O <sub>12ts</sub>	PRINTER MODE: PD1 Parallel port data bus bit 1.
GP91		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 1. (Default)
PD0	50	I/O <sub>12ts</sub>	PRINTER MODE: PD0 Parallel port data bus bit 0.
GP90		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 0. (Default)
SLIN#	51	OD <sub>12</sub>	PRINTER MODE: SLIN# Output line for detection of printer selection.
GP84		I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 4.
BEEP		OD <sub>12</sub>	Beep function for hardware monitor. This pin is low after system reset. (Default)
INIT#	52	OD <sub>12</sub>	PRINTER MODE: INIT# Output line for the printer initialization.
GP83		I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 3.
PLED		OD <sub>12</sub>	Power LED output. (Default)
ERR#	53	IN <sub>ts</sub>	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error condition.
VID_RST#		IN <sub>g</sub>	VID controller reset signal.
GP82		I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 2. (Default)
AFD#	54	OD <sub>12</sub>	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed.

SYMBOL	PIN	I/O	DESCRIPTION
PECI_REQ#		OD <sub>12</sub>	INTEL <sup>®</sup> CPU Peci interface. Connect to BM_BUSY#.
GP81		I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 1. (Default)
STB#	55	OD <sub>12</sub>	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer.
GP80		I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 0. (Default)

#### 5.4 Serial Port (UART A and UART B)

SYMBOL	PIN	I/O	DESCRIPTION
CTSA#	29	IN <sub>t</sub>	UART A Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register. (Default)
GP67		I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 7.
DSRA#	30	IN <sub>t</sub>	UART A Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. (Default)
GP66		I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 6.
RTSA#	31	O <sub>8</sub>	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data. (Default)
HEFRAS		IN <sub>cd</sub>	Strap - During power on reset, this pin is pulled down internally and if a 1-k $\Omega$ pull up resistor is detected the base address is set to 4Eh. If a 1-k $\Omega$ pull down resistor is detected the base address is set to 2Eh. The detected value is stored in CR[26h] bit 6 (HEFRAS).
GP65		I/O <sub>12t</sub>	General-purpose I/O port 6 bit 5.
DTRA#	32	O <sub>8</sub>	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate. (Default)
PENROM		IN <sub>cd</sub>	Strap - During power on reset, this pin is pulled down internally and if a 1-k $\Omega$ pull up resistor is detected the SPI interface is enabled. If a 1-k $\Omega$ pull down resistor is detected the SPI interface is disabled. The detected value is stored in CR[24h] bit 1 (ENROM).
GP64		I/O <sub>12t</sub>	General-purpose I/O port 6 bit 4.
SINA	33	IN <sub>t</sub>	UART A Serial Input. This pin is used to receive serial data through the communication link. (Default)
GP63		I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 3.
SOUTA	34	O <sub>8</sub>	UART A Serial Output. This pin is used to transmit serial data out to the communication link. (Default)
FANSET		IN <sub>cd</sub>	Determines the FAN initial speed. Power on configuration for fan speed rotation rate levels at 100% and 50%. During power-

SYMBOL	PIN	I/O	DESCRIPTION
			ok reset, this pin needs a pulled-up or a pull-down resistor to decide the fan rotation rate is 100% or 50%. Only CPUFANOUT support.
GP62		I/O <sub>8</sub>	General-purpose I/O port 6 bit 2.
DCDA#	35	IN <sub>t</sub>	UART A Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier. (Default)
GP61		I/OD <sub>8t</sub> I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 1.
RIA#	36	IN <sub>t</sub>	UART A Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set. (Default)
GP60		I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 0.
CTSB#	67	IN <sub>t</sub>	UART B Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP47		I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 7. (Default)
DSRB#	68	IN <sub>t</sub>	UART B Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP46		I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 6. (Default)
RTSB#	69	O <sub>12</sub>	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
GP45		I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 5. (Default)
DTRB#	70	O <sub>12</sub>	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
GP44		I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 4. (Default)
SINB	71	IN <sub>t</sub>	UART B Serial Input. This pin is used to receive serial data through the communication link.
GP43		I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 3. (Default)
SOUTB	72	O <sub>12</sub>	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
GP42		I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 2. (Default)
DCDB#	73	IN <sub>t</sub>	UART B Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
GP41		I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 1. (Default)
RIB#	74	IN <sub>t</sub>	UART B Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
GP40		I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 0. (Default)

### 5.5 KBC Interface

SYMBOL	PIN	I/O	DESCRIPTION
GA20M	27	O <sub>12</sub>	Gate A20 output. This pin is high after system reset. (KBC P21)
KBRST#	28	O <sub>12</sub>	Keyboard reset. This pin is high after system reset. (KBC P20)
MCLK	56	I/OD <sub>12ts</sub>	PS2 Mouse Clock. (Default)
GP23		I/OD <sub>12ts</sub>	General-purpose I/O port 2 bit 3.
MDAT	57	I/OD <sub>12ts</sub>	PS2 Mouse Data. (Default)
GP22		I/OD <sub>12ts</sub>	General-purpose I/O port 2 bit 2.
KCLK	58	I/OD <sub>12ts</sub>	Keyboard Clock. (Default)
GP21		I/OD <sub>12ts</sub>	General-purpose I/O port 2 bit 1.
KDAT	59	I/OD <sub>12ts</sub>	Keyboard Data. (Default)
GP20		I/OD <sub>12ts</sub>	General-purpose I/O port 2 bit 0.

### 5.6 Serial Peripheral Interface

SYMBOL	PIN	I/O	DESCRIPTION
SCK	94	O <sub>12</sub>	Clock output for serial flash (33MHz). (Default strapped by pin 32)
GP27		I/OD <sub>12t</sub>	General-purpose I/O port 2 bit 7.
SCE#	95	O <sub>12</sub>	Serial Flash ROM interface chip select. (Default strapped by pin 32)
AUXFANIN2		I/O <sub>12t</sub>	0 to +3 V amplitude fan tachometer input. (Default if disable SPI ROM)
GP26		I/OD <sub>12t</sub>	General-purpose I/O port 2 bit 6.
SI	97	IN <sub>t</sub>	Receive data from Serial Flash. This pin is connected to Serial Flash SO. (Default strapped by pin 32)
AUXFANIN		IN <sub>t</sub>	0 to +3 V amplitude fan tachometer input. (Default if disable SPI ROM strapping.)
SO	98	O <sub>12</sub>	Transfer commands, address or data to Serial Flash. This pin is connected to Serial Flash SI. (Default strapped by pin 32)
AUXFANOUT		AOUT O <sub>12</sub> OD <sub>12</sub>	DC/PWM fan output control. (Default if disable SPI ROM strapping.)

## 5.7 Hardware Monitor Interface

SYMBOL	PIN	I/O	DESCRIPTION
SCE#	95	O <sub>12</sub>	Serial Flash ROM interface chip select. (Default strapped by pin 32)
AUXFANIN2		I/O <sub>12T</sub>	0 to +3 V amplitude fan tachometer input. (Default if disable SPI ROM)
GP26		I/OD <sub>12T</sub>	GENERAL-PURPOSE I/O PORT 2 BIT 6.
AUXFANIN1	96	I/O <sub>12t</sub>	0 to +3 V amplitude fan tachometer input. (Default)
GP25		I/OD <sub>12t</sub>	General-purpose I/O port 2 bit 5.
SI	97	IN <sub>t</sub>	Receive data from Serial Flash. This pin is connected to Serial Flash SO. (Default strapped by pin 32)
AUXFANIN		IN <sub>t</sub>	0 to +3 V amplitude fan tachometer input. (Default if disable SPI ROM)
SO	98	O <sub>12</sub>	Transfer commands, address or data to Serial Flash. This pin is connected to Serial Flash SI. (Default strapped by pin 32)
AUXFANOUT		AOUT O <sub>12</sub> OD <sub>12</sub>	DC / PWM fan output control. (Default if disable SPI ROM)
CASEOPEN#	100	IN <sub>t</sub>	CASE OPEN. An active-low input from an external switch to detect an open case lid. This signal is detected and latched when pin VBAT is connected to the battery, even if the W83667HG-A is otherwise powered down. Pulling up with a 2-MΩ resistor to VBAT is recommended if not used.
SKTOCC	102	IN <sub>t</sub>	To detect CPU presence. This pin is high-active. (Default)
GP56		I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 6.
VCROE_REFIN	103	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
VIN1	104	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
VIN0	105	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
CPUVCORE	107	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
VREF	108	AOUT	Reference Voltage (Approx 2.048 V).
VIN2	109	AIN	Analog Inputs for voltage measurement (Range: 0 to 2.048 V)
AUXTIN		AIN	The input of temperature sensor 3.
CPUTIN	110	AIN	The input of temperature sensor 2.
SYSTIN	111	AIN	The input of temperature sensor 1.
CPUFANIN	124	I/O <sub>12ts</sub>	0 to +3 V amplitude fan tachometer input.
CPUFANOUT	125	AOUT O <sub>12</sub> OD <sub>12</sub>	DC / PWM fan output control.
SYSFANIN	126	I/O <sub>12ts</sub>	0 to +3 V amplitude fan tachometer input.

SYMBOL	PIN	I/O	DESCRIPTION
SCE#	95	O <sub>12</sub>	Serial Flash ROM interface chip select. (Default strapped by pin 32)
AUXFANIN2		I/O <sub>12T</sub>	0 to +3 V amplitude fan tachometer input. (Default if disable SPI ROM)
GP26		I/OD <sub>12T</sub>	GENERAL-PURPOSE I/O PORT 2 BIT 6.
SYSFANOUT	127	AOUT O <sub>12</sub> OD <sub>12</sub>	DC / PWM fan output control.
SMI#	128	OD <sub>12</sub>	System Management Interrupt channel output.
OVT#		OD <sub>12</sub>	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after PCIRST)

### 5.8 INTEL® PECCI and AMD™ SB-TSI Interface

SYMBOL	PIN	I/O	DESCRIPTION
PECCI_REQ#	54	OD <sub>12</sub>	INTEL® CPU PECCI interface. Connect to BM_BUSY#.
AFD#		OD <sub>12</sub>	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed.
GP81		I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 1. (Default)
PECCI_AVAIL	113	I <sub>V3</sub>	INTEL® CPU PECCI interface. Connect to DPSLP#.
TSIC		IN <sub>ts</sub>	AMD™ SB-TSI clock output.
PECCI	115	I/O <sub>V3</sub>	INTEL® CPU PECCI interface. Connect to CPU.
TSID		I/OD <sub>12ts</sub>	AMD™ SB-TSI data input. (Default)

### 5.9 Advanced Configuration and Power Interface

SYMBOL	PIN	I/O	DESCRIPTION
PSOUT#	60	OD <sub>12</sub>	Panel Switch Output. This signal is used to wake-up the system from S5 state. This pin is pulse-output, active-low. (Default)
GP55		I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 7.
PSIN#	61	IN <sub>t</sub>	Panel Switch Input. This pin is active-low with an internal pulled-up resistor. (Default)
GP54		I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 4.
SUSLED	62	O <sub>12</sub>	Suspended LED output.
GP53		O <sub>12</sub>	General-purpose I/O port 5 bit 3. (Default)
PSON#	63	OD <sub>12</sub>	Power supply on-off output. (Default)
GP52		I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 2.

SYMBOL	PIN	I/O	DESCRIPTION
SUSB#	64	IN <sub>t</sub>	System S3 states input. (Default)
GP51		I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 1.
ATXPGD	80	IN <sub>t</sub>	ATX valid power input signal. (Default)
GP34		I/OD <sub>12t</sub>	General-purpose I/O port 3 bit 4.
3VSBSW#	81	O <sub>12</sub>	Switch 3VSB power to memory when in S3 state. (Default)
GP33		I/OD <sub>12t</sub>	General-purpose I/O port 3 bit 3.
PWROK0	82	OD <sub>12</sub>	This pin generates the PWRGD signal while VCC is present. (Default)
GP32		I/OD <sub>12t</sub>	General-purpose I/O port 3 bit 2.
RESETCON#	83	IN <sub>t</sub>	Connect to Front panel reset button. (Default)
GP31		I/OD <sub>8t</sub>	General-purpose I/O port 3 bit 1.
SUSC#	84	IN <sub>t</sub>	System S5 states input. (Default)
GP30		I/OD <sub>12t</sub>	General-purpose I/O port 3 bit 0.
RSMRST#	101	OD <sub>12</sub>	Resume reset signal output. (Default)
GP57		I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 7.
RSTOUT2#	77	O <sub>24</sub>	PCI Reset Buffer 2. (Default)
RSTOUT1#	78	O <sub>24</sub>	PCI Reset Buffer 1. (Default)
GP36		I/OD <sub>24t</sub>	General-purpose I/O port 3 bit 6.
RSTOUT0#	79	OD <sub>24</sub>	PCI Reset Buffer 0. (Default)
GP35		I/OD <sub>24t</sub>	General-purpose I/O port 3 bit 4.
PD7	42	I/O <sub>12ts</sub>	PRINTER MODE: PD7 Parallel port data bus bit 7.
GP97		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 7.
PWROK2		OD <sub>12</sub>	200mS after PWROK0 active.(Default)
PD3	47	I/O <sub>12ts</sub>	PRINTER MODE: PD3 Parallel port data bus bit 3.
GP93		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 3.
PWROK1		OD <sub>12</sub>	This pin generates the PWRGD signal while VCC is present. (Default)

## 5.10 General Purpose I/O Port

### 5.10.1GPIO Power Source

SYMBOL	POWER SOURCE
GPIO port 1	3VCC
GPIO port 2	3VSB
GPIO port 3	3VSB
GPIO port 4	3VSB
GPIO port 5	3VSB
GPIO port 6	3VCC
GPIO port 7	3VSB
GPIO port 8	3VSB
GPIO port 9	3VSB

### 5.10.2GPIO-1 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP17	116	I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 7.
VIDI7		IN <sub>g</sub>	VID input detection. (Default)
GP16	117	I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 6.
VIDI6		IN <sub>g</sub>	VID input detection. (Default)
GP15	118	I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 5.
VIDI5		IN <sub>g</sub>	VID input detection. (Default)
GP14	119	I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 4.
VIDI4		IN <sub>g</sub>	VID input detection. (Default)
GP13	120	I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 3.
VIDI3		IN <sub>g</sub>	VID input detection. (Default)
GP12	121	I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 2.
VIDI2		IN <sub>g</sub>	VID input detects. (Default)
GP11	122	I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 1.
VIDI1		IN <sub>g</sub>	VID input detects. (Default)
GP10	123	I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 0.
VIDI0		IN <sub>g</sub>	VID input detects. (Default)

### 5.10.3GPIO-2 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP24	38	I/OD <sub>12ts</sub>	General-purpose I/O port 2 bit 4. (Default)

SYMBOL	PIN	I/O	DESCRIPTION
SLCT		$IN_{ts}$	PRINTER MODE: SLCT An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
GP23	56	$I/OD_{12ts}$	General-purpose I/O port 2 bit 3.
MCLK		$I/OD_{16ts}$	PS2 Mouse Clock. (Default)
GP22	57	$I/OD_{12ts}$	General-purpose I/O port 2 bit 2.
MDAT		$I/OD_{16ts}$	PS2 Mouse Data. (Default)
GP21	58	$I/OD_{12ts}$	General-purpose I/O port 2 bit 1.
KCLK		$I/OD_{16ts}$	Keyboard Clock. (Default)
GP20	59	$I/OD_{12ts}$	General-purpose I/O port 2 bit 0.
KDAT		$I/OD_{16ts}$	Keyboard Data. (Default)
GP27	94	$I/OD_{12t}$	General-purpose I/O port 2 bit 7.
SCK		$O_{12}$	Clock output for serial flash. (33MHz). (Default strapped by pin 32)
GP26	95	$I/OD_{12t}$	General-purpose I/O port 2 bit 6.
AUXFANIN2		$I/O_{12t}$	0 to +3 V amplitude fan tachometer input. (Default if disable SPI ROM)
SCE#		$O_{12}$	Serial flash ROM interface chip selection. (Default strapped by pin 32)
GP25	96	$I/OD_{12t}$	General-purpose I/O port 2 bit 5.
AUXFANIN1		$I/O_{12t}$	0 to +3 V amplitude fan tachometer input. (Default)

#### 5.10.4GPIO-3 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP37	76	$I/OD_{12t}$	General-purpose I/O port 3 bit 7. (Default)
SDA		$I/OD_{12ts}$	SMBus data.
IRTX		$O_{12}$	IR Transmitter output.
GP36	78	$I/OD_{24t}$	General-purpose I/O port 3 bit 6.
RSTOUT1#		$O_{24}$	PCI Reset Buffer 1. (Default)
GP35	79	$I/OD_{24t}$	General-purpose I/O port 3 bit 4.
RSTOUT0#		$OD_{24}$	PCI Reset Buffer 0. (Default)
GP34	80	$I/OD_{12t}$	General-purpose I/O port 3 bit 4.
ATXPGD		$IN_t$	ATX power good input signal. (Default)
GP33	81	$I/OD_{12t}$	General-purpose I/O port 3 bit 3.
3VSBSW#		$O_{12}$	Switch 3VSB power to memory when in S3 state. (Default)
GP32	82	$I/OD_{12t}$	General-purpose I/O port 3 bit 2.

SYMBOL	PIN	I/O	DESCRIPTION
PWROK0		OD <sub>12</sub>	This pin generates the PWRGD signal while VCC is present.
GP31	83	I/OD <sub>8t</sub>	General-purpose I/O port 3 bit 1.
RESETCON#		IN <sub>t</sub>	Connect to Front panel reset button. (Default)
GP30	84	I/OD <sub>12t</sub>	General-purpose I/O port 3 bit 0.
SUSC#		IN <sub>t</sub>	System S5 states input. (Default)

#### 5.10.5GPIO-4 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP47	67	I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 7. (Default)
CTSB#		IN <sub>t</sub>	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP46	68	I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 6. (Default)
DSRB#		IN <sub>t</sub>	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP45	69	I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 5. (Default)
RTSB#		O <sub>8</sub>	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
GP44	70	I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 4. (Default)
DTRB#		O <sub>8</sub>	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
GP43	71	I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 3. (Default)
SINB		IN <sub>t</sub>	Serial Input. This pin is used to receive serial data through the communication link.
GP42	72	I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 2. (Default)
SOUTB		O <sub>8</sub>	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
GP41	73	I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 1. (Default)
DCDB#		IN <sub>t</sub>	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
GP40	74	I/OD <sub>12t</sub>	General-purpose I/O port 4 bit 0. (Default)
RIB#		IN <sub>t</sub>	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.

**5.10.6GPIO-5 Interface**

SYMBOL	PIN	I/O	DESCRIPTION
GP55	60	I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 5.
PSOUT#		OD <sub>12</sub>	Panel Switch Output. This signal is used to wake-up the system from S5 state. This pin is pulse-output, active-low. (Default)
GP54	61	I/OD <sub>8t</sub>	General-purpose I/O port 5 bit 4.
PSIN#		IN <sub>t</sub>	Panel Switch Input. This pin is active-low. (Default)
GP53	62	O <sub>8</sub>	General-purpose I/O port 5 bit 0. (Default)
SUSLED		O <sub>8</sub>	Suspended LED output.
GP52	63	I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 3.
PSON#		OD <sub>12</sub>	Power supply on-off output. (Default)
GP51	64	I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 2.
SUSB#		IN <sub>t</sub>	System S3 states input. (Default)
GP50	75	I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 0. (Default)
SCL		IN <sub>ts</sub>	Serial Bus clock.
IRRX		IN <sub>ts</sub>	IR Receiver input.
GP57	101	I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 7.
RSMRST#		OD <sub>12</sub>	Resume reset signal output. (Default)
GP56	102	I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 6.
SKTOCC		IN <sub>t</sub>	To detect CPU presence. This pin is high-active. (Default)

**5.10.7GPIO-6 Interface**

SYMBOL	PIN	I/O	DESCRIPTION
GP67	29	I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 7.
CTSA#		IN <sub>t</sub>	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register. (Default)
GP66	30	I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 6.
DSRA#		IN <sub>t</sub>	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. (Default)
GP65	31	I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 5.
HEFRAS		IN <sub>cd</sub>	During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to prevent selecting I/O port's configuration address to 2EH unsuccessfully, and a 1-kΩ resistor is recommended to pull it up if select 4EH as I/O port's configuration address.

SYMBOL	PIN	I/O	DESCRIPTION
RTSA#		O <sub>8</sub>	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. (Default)
GP64	32	I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 4.
PENROM		IN <sub>cd</sub>	During power-on reset, this pin is pulled down internally and is defined as PENROM disable, which provides the power-on value for CR24 bit 1 (ENROM). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to prevent disabling SPI interface unsuccessfully, and a 1-kΩ resistor is recommended to pull it up to if enable ROM
DTRA#		O <sub>8</sub>	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate. (Default)
GP63	33	I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 3.
SINA		IN <sub>t</sub>	Serial Input. This pin is used to receive serial data through the communication link. (Default)
GP62	34	I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 2.
SOUTA		O <sub>8</sub>	UART A Serial Output. This pin is used to transmit serial data out to the communication link. (Default)
FANSET		IN <sub>cd</sub>	Determines the FAN initial speed. Power on configuration for fan speed rotation rate levels at 100% and 50%. During power-ok reset, this pin needs a pulled-up or a pull-down resistor to decide the fan rotation rate is 100% or 50%. Only CPUFANOUT support.
GP61	35	I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 1.
DCDA#		IN <sub>t</sub>	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier. (Default)
GP60	36	I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 0.
RIA#		IN <sub>t</sub>	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set. (Default)

#### 5.10.8GPIO-7 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP77	86	I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 7.
VIDO7		OD <sub>12</sub>	VID output control. (Default)
GP76	87	I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 6.
VIDO6		OD <sub>12</sub>	VID output control. (Default)
GP75	88	I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 5.
VIDO5		OD <sub>12</sub>	VID output control. (Default)
GP74	89	I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 4.

SYMBOL	PIN	I/O	DESCRIPTION
VIDO4		OD <sub>12</sub>	VID output control. (Default)
GP73	90	I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 3.
VIDO3		OD <sub>12</sub>	VID output control. (Default)
GP72	91	I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 2.
VIDO2		OD <sub>12</sub>	VID output control. (Default)
GP71	92	I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 1.
VIDO1		OD <sub>12</sub>	VID output control. (Default)
GP70	93	I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 0.
VIDO0		OD <sub>12</sub>	VID output control. (Default)

#### 5.10.9GPIO-8 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP87	39	I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 7. (Default)
PE		IN <sub>ts</sub>	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper.
GP86	40	I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 6. (Default)
BUSY		IN <sub>ts</sub>	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data.
GP85	41	I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 5. (Default)
ACK#		IN <sub>ts</sub>	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data.
GP84	51	I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 4.
BEEP		OD <sub>12</sub>	Beep function for hardware monitor. This pin is low after system reset. (Default)
SLIN#		OD <sub>12</sub>	PRINTER MODE: SLIN# Output line for detection of printer selection.
GP83	52	I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 3.
PLED		OD <sub>12</sub>	Power LED output. (Default)
INIT#		OD <sub>12</sub>	PRINTER MODE: INIT# Output line for the printer initialization.
GP82	53	I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 2. (Default)
VID_RST#		IN <sub>g</sub>	VID controller reset signal.
ERR#		IN <sub>ts</sub>	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has

SYMBOL	PIN	I/O	DESCRIPTION
			encountered an error condition.
GP81	54	I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 1. (Default)
PECI_REQ#		OD <sub>12</sub>	INTEL® CPU Peci interface.
AFD#		OD <sub>12</sub>	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed.
GP80	55	I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 0. (Default)
STB#		OD <sub>12</sub>	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer.

#### 5.10.10 GPIO-9 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP97	42	I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 7.
PD7		I/O <sub>12ts</sub>	PRINTER MODE: PD7 Parallel port data bus bit 7.
PWROK2		OD <sub>12</sub>	200mS after PWROK0 active.(Default)
GP96	43	I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 6.
PD6		I/O <sub>12ts</sub>	PRINTER MODE: PD6 Parallel port data bus bit 6.
GP95	44	I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 5.
PD5		I/O <sub>12ts</sub>	PRINTER MODE: PD5 Parallel port data bus bit 5.
GP94	45	I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 4.
PD4		I/O <sub>12ts</sub>	PRINTER MODE: PD4 Parallel port data bus bit 4.
GP93	47	I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 3.
PD3		I/O <sub>12ts</sub>	PRINTER MODE: PD3 Parallel port data bus bit 3.
PWROK1		OD <sub>12</sub>	This pin generates the PWRGD signal while VCC is present. (Default)
GP92	48	I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 2.
PD2		I/O <sub>12ts</sub>	PRINTER MODE: PD2 Parallel port data bus bit 2.
GP91	49	I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 1.
PD1		I/O <sub>12ts</sub>	PRINTER MODE: PD1 Parallel port data bus bit 1.
GP90	50	I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 0.

SYMBOL	PIN	I/O	DESCRIPTION
PD0		I/O <sub>12ts</sub>	PRINTER MODE: PD0 Parallel port data bus bit 0.

### 5.11 VID Input / Output

SYMBOL	PIN	I/O	DESCRIPTION
VIDO7	86	OD <sub>12</sub>	VID output control. (Default)
GP77		I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 7.
VIDO6	87	OD <sub>12</sub>	VID output control. (Default)
GP76		I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 6.
VIDO5	88	OD <sub>12</sub>	VID output control. (Default)
GP75		I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 5.
VIDO4	89	OD <sub>12</sub>	VID output control. (Default)
GP74		I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 4.
VIDO3	90	OD <sub>12</sub>	VID output control. (Default)
GP73		I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 3.
VIDO2	91	OD <sub>12</sub>	VID output control. (Default)
GP72		I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 2.
VIDO1	92	OD <sub>12</sub>	VID output control. (Default)
GP71		I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 1.
VIDO0	93	OD <sub>12</sub>	VID output control. (Default)
GP70		I/OD <sub>12t</sub>	General-purpose I/O port 7 bit 0.
VIDI7	116	IN <sub>g</sub>	VID input detection. (Default)
GP17		I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 7.
VIDI6	117	IN <sub>g</sub>	VID input detection. (Default)
GP16		I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 6.
VIDI5	118	IN <sub>g</sub>	VID input detection. (Default)
GP15		I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 5.
VIDI4	119	IN <sub>g</sub>	VID input detection. (Default)
GP14		I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 4.
VIDI3	120	IN <sub>g</sub>	VID input detection. (Default)
GP13		I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 3.
VIDI2	121	IN <sub>g</sub>	VID input detection. (Default)
GP12		I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 2.
VIDI1	122	IN <sub>g</sub>	VID input detection. (Default)
GP11		I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 1.

SYMBOL	PIN	I/O	DESCRIPTION
VIDI0	123	IN <sub>g</sub>	VID input detection. (Default)
GP10		I/OD <sub>12t</sub>	General-purpose I/O port 1 bit 0.
GP82	53	I/OD <sub>12t</sub>	General-purpose I/O port 8 bit 2. (Default)
VID_RST#		IN <sub>g</sub>	VID controller reset signal.
ERR#		IN <sub>ts</sub>	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error condition.

### 5.12 IR

SYMBOL	PIN	I/O	DESCRIPTION
IRTX	76	O <sub>12</sub>	IR Transmitter output.
GP37		I/OD <sub>12t</sub>	General-purpose I/O port 3 bit 7. (Default)
SDA		I/OD <sub>12t</sub>	Serial Bus data.
IRRX	75	IN <sub>t</sub>	IR Receiver input.
GP50		I/OD <sub>12t</sub>	General-purpose I/O port 5 bit 0. (Default)
SCL		IN <sub>ts</sub>	Serial Bus clock.

### 5.13 Power Pins

SYMBOL	PIN	DESCRIPTION
CPUD-	112	Analog ground. The ground reference for all analog input. Internally connected to all analog circuits.
VCC	1, 24	+3.3 V power supply for driving 3 V on host interface.
VSB	46, 85	+3.3 V stand-by power supply for the digital circuits.
VSS	16, 66	Ground.
VBAT	99	+3 V on-board battery for the digital circuits.
AVCC	106	Analog +3.3 V power input. Internally supply power to all analog circuits.
V <sub>tt</sub>	114	INTEL® CPU V <sub>tt</sub> power.

### 5.14 Strapping Pins

SYMBOL	PIN	I/O	DESCRIPTION
HEFRAS	31	IN <sub>cd</sub>	During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to prevent selecting I/O

SYMBOL	PIN	I/O	DESCRIPTION
			port's configuration address to 2EH unsuccessfully, and a 1-k $\Omega$ resistor is recommended to pull it up if select 4EH as I/O port's configuration address.(Strapping LRESET#; 0:2Eh , 1:4Eh)
RTSA#		O <sub>8</sub>	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data. (Default)
GP65		I/OD <sub>12t</sub>	General-purpose I/O port 6 bit 5.
PENROM	32	IN <sub>cd</sub>	During power-on reset, this pin is pulled down internally and is defined as PENROM disable, which provides the power-on value for CR24 bit 1 (ENROM). The PCB layout should reserve space for a 1-k $\Omega$ resistor to pull down this pin to prevent disabling SPI interface unsuccessfully, and a 1-k $\Omega$ resistor is recommended to pull it up to if enable ROM. (Strapping LRESET#; 0:Disable SPI function , 1: Enable SPI function)
DTRA#		O <sub>8</sub>	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate. (Default)
GP64		I/O <sub>12t</sub>	General-purpose I/O port 6 bit 4.
FANSET	34	IN <sub>cd</sub>	Determines the FAN initial speed. Power on configuration for fan speed rotation rate levels at 100% and 50%. During power-ok reset, this pin needs a pulled-up or a pull-down resistor to decide the fan rotation rate is 100% or 50%. Only CPUFANOUT support. (Strapping Pin82 PWROK ; 0:50% , 1:100%h)
SOUTA		O <sub>8</sub>	UART A Serial Output. This pin is used to transmit serial data out to the communication link. (Default)
GP62		I/O <sub>12t</sub>	General-purpose I/O port 6 bit 2.
EN_AS	62	IN <sub>cd</sub>	Enable ASUS specific function. (See 5.16 for more detail.)
GP53		I/O <sub>12t</sub>	General-purpose I/O port 5 bit 0. (Default)
SUSLED		O <sub>12</sub>	Suspended LED output.

### 5.15 Reserved Pins

SYMBOL	PIN	DESCRIPTION
RSVD	37	This pin is reserved for future application.

### 5.16 ASUS ASICs

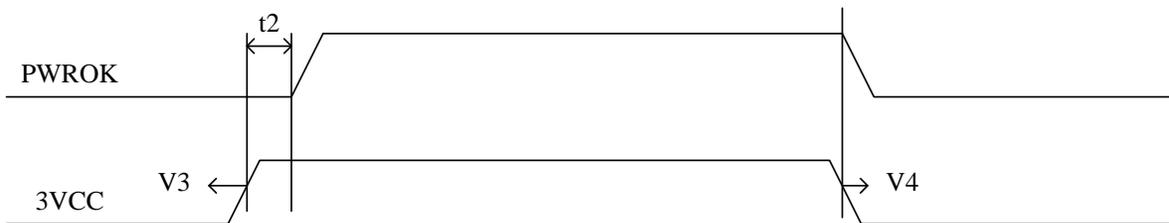
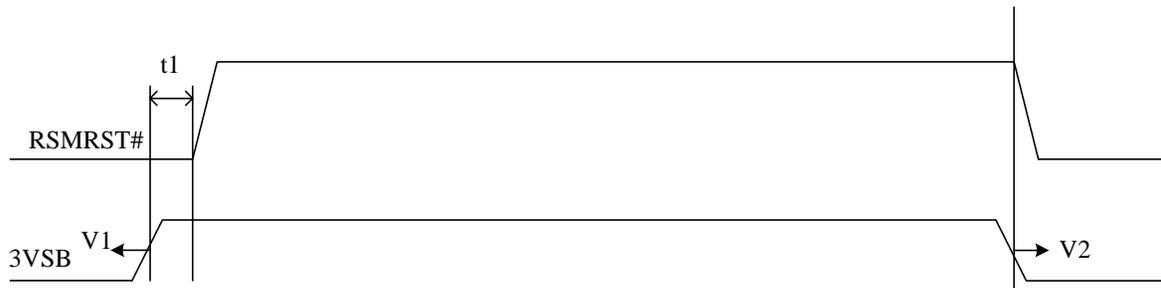
SYMBOL	PIN	I/O	DESCRIPTION
EN_AS	62	IN <sub>cd</sub>	During VSB power reset (RSMRST), this pin is pulled down internally and is defined as EN_AS (enabling ASUS ASIC functions), which provides the value for CR2Fh bit 6

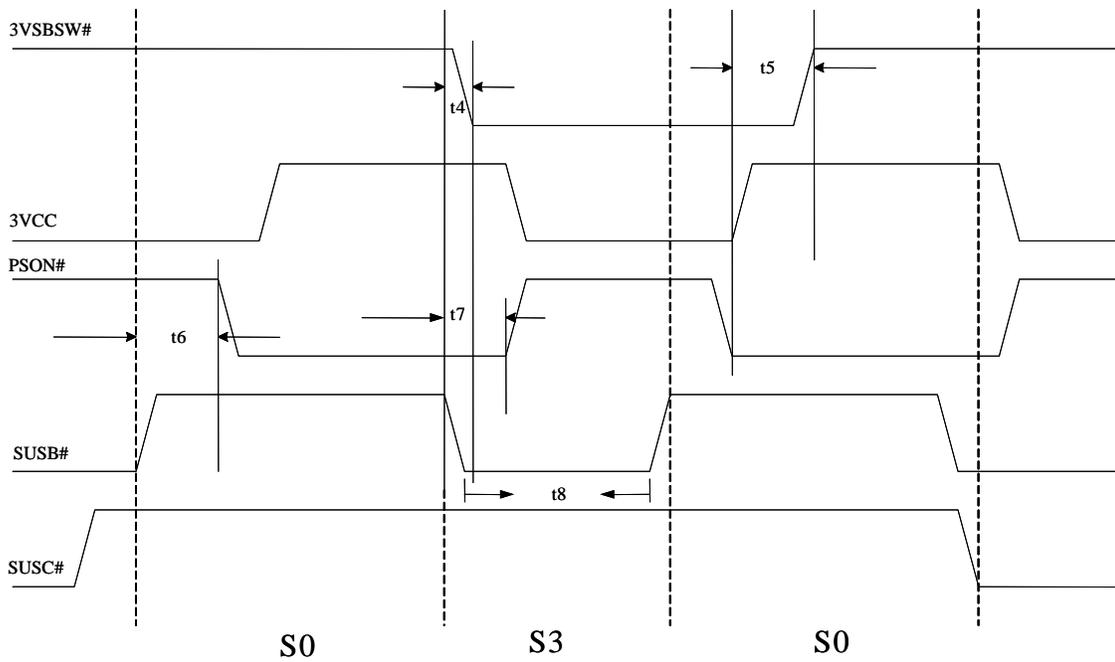
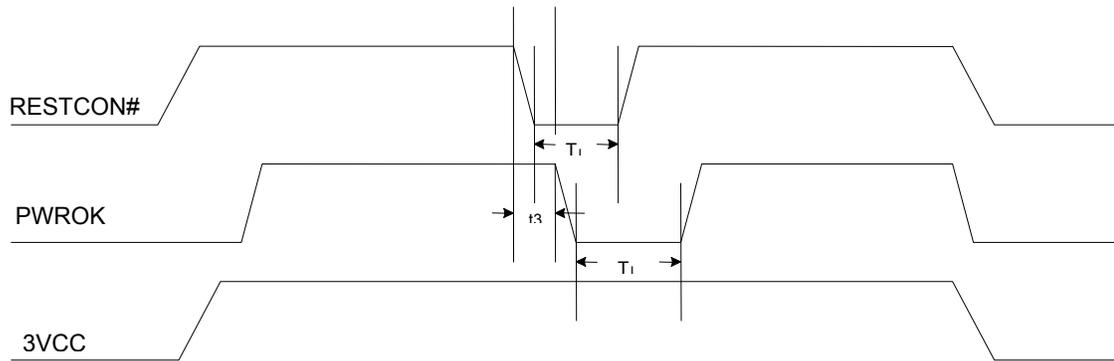
SYMBOL	PIN	I/O	DESCRIPTION
			(EN_AS). The PCB layout should reserve space for a 1-k $\Omega$ resistor to pull down this pin to prevent disabling ASUS function unsuccessfully, and a 1-k $\Omega$ resistor is recommended to pull it up if enable ASUS function. (Strapping RSMRST#, 0:Disable ASUS ASIC , 1:Enable ASUS ASIC)
GP53		I/O <sub>12t</sub>	General-purpose I/O port 5 bit 0. (Default)
SUSLED		O <sub>12</sub>	Suspended LED output.
BUSELO2	43	OD <sub>12</sub>	CPU FSB output control 2. (Default strapped by pin 62)
GP96		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 6.
PD6		I/O <sub>12ts</sub>	PRINTER MODE: PD6 Parallel port data bus bit 6.
BUSELO1	44	OD <sub>12</sub>	CPU FSB output control 1. (Default strapped by pin 62)
GP95		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 5.
PD5		I/O <sub>12ts</sub>	PRINTER MODE: PD5 Parallel port data bus bit 5.
BUSELO0	45	OD <sub>12</sub>	CPU FSB output control 0. (Default strapped by pin 62)
GP94		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 4.
PD4		I/O <sub>12ts</sub>	PRINTER MODE: PD4 Parallel port data bus bit 4.
BUSELI2	48	IN <sub>g</sub>	CPU FSB input control 2. (Default strapped by pin 62)
GP92		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 2.
PD2		I/O <sub>12ts</sub>	PRINTER MODE: PD2 Parallel port data bus bit 2.
BUSELI1	49	IN <sub>g</sub>	CPU FSB input control 1. (Default strapped by pin 62)
GP91		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 1.
PD1		I/O <sub>12ts</sub>	PRINTER MODE: PD1 Parallel port data bus bit 1.
BUSELI0	50	IN <sub>g</sub>	CPU FSB input control 0. (Default strapped by pin 62)
GP90		I/OD <sub>12t</sub>	General-purpose I/O port 9 bit 0.
PD0		I/O <sub>12ts</sub>	PRINTER MODE: PD0 Parallel port data bus bit 0.
VCORE_REFIN	103	AIN	CPU VCORE reference input. (Default strapped by pin 62) Note. When ASUS function is enable, Pin107 CPUVCORE voltage must under Pin103 VCORE_REFIN ,otherwise Pin63 PSON# will be blocked.

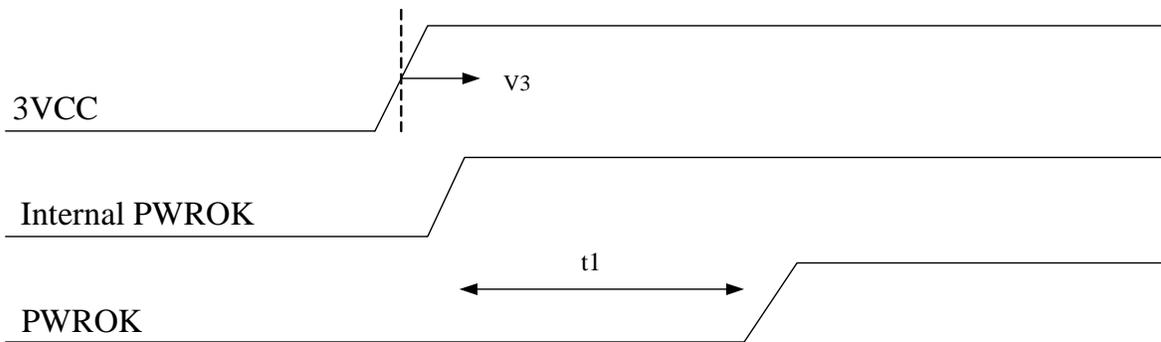
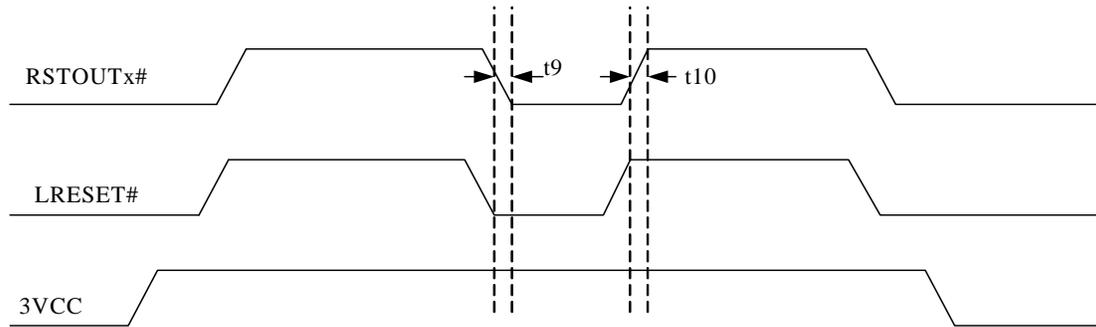
6. ACPI GLUE LOGIC

Table 6-1 Pin Description

SYMBOL	PIN	DESCRIPTION
SUSC#	84	SLP_S5# input.
RESETCON#	83	Connect to the reset button. This pin has internal de-bounce circuit whose de-bounce time is at least 32 mS.
3VBSW#	81	Switch 3VSB power to memory when in S3 state.
PWROK0	82	This pin generates the PWRGD signals while 3VCC is present.
ATXPGD	80	ATX power good input signal. It is connected to the PWROK signal from the power supply for PWROK/PWRGD generation. The default is enabled.
PWROK1	47	This pin generates the PWRGD signals while 3VCC is present. (Same as PWROK0)
PWROK2	42	200mS after PWROK0 active.







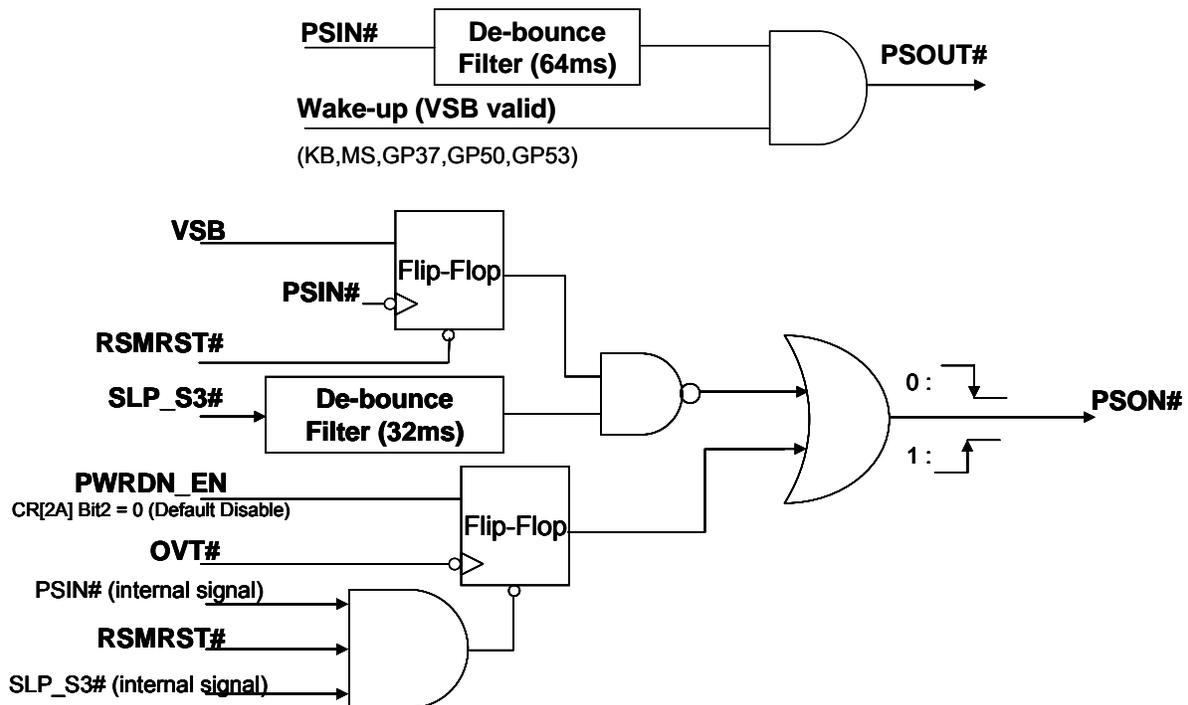
TIMING	PARAMETER	MIN	MAX	UNIT
t1	Valid 3VSB to RSMRST# inactive	100	200	mS
t2	Valid 3VCC to PWROK/PWRGD active	300	500	mS
t3	RESETCON# active to PWROK/PWRGD active	15	45	mS
t4	SUSB# active to 3VSBSW# active	0	80	nS
t5	PSON# active to 3VSBSW# inactive	90	142	mS
t6	SUSB# inactive to PSON# active	0	80	nS
t7	SUSB# active to PSON# inactive	15	45	mS
t8	SUSB# minimal Low Time	40	-	mS
t9	LRESET# active to RSTOUTx# active	0	80	nS
t10	LRESET# inactive to RSTOUTx# inactive	0	80	nS

DC	PARAMETER	MIN	MAX	UNIT
V1	3VSB Valid Voltage	-	3.0	Volt
V2	3VSB Ineffective Voltage	2.4	-	Volt
V3	3VCC Valid Voltage	-	3.0	Volt
V4	3VCC Ineffective Voltage	2.4	-	Volt

Note : 1. The values above are the worst-case results of R&D simulation.  
 2. The length of T<sub>L</sub> level is based on the length of the low level of RESETCON#

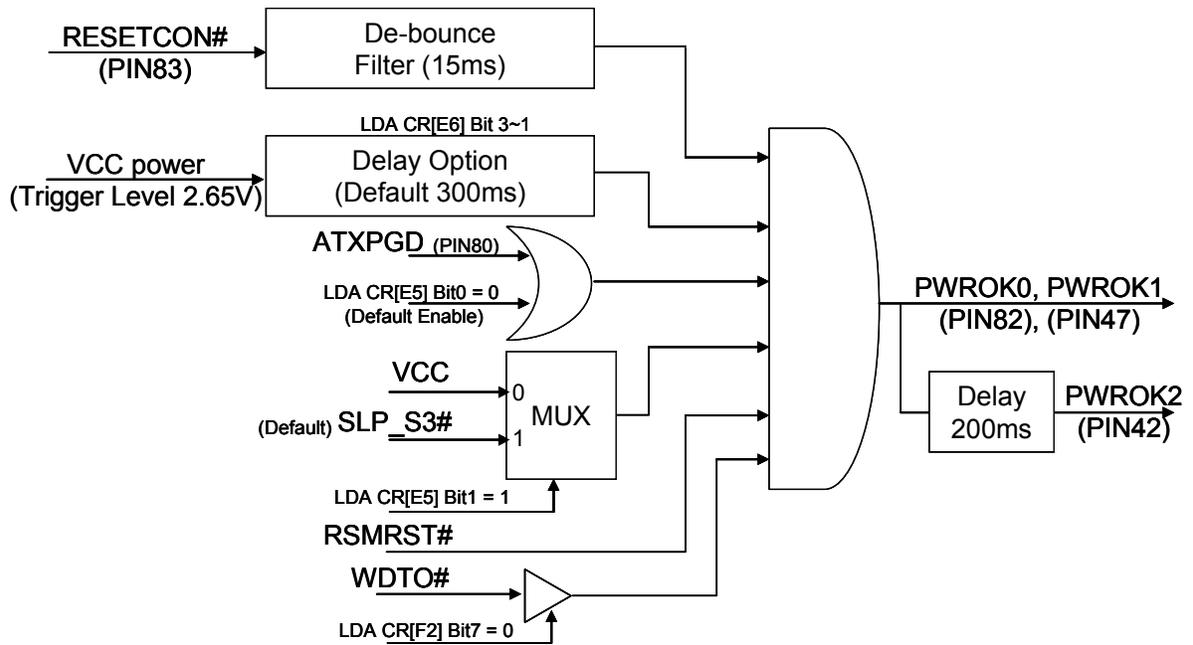
### 6.1 PSON# Block Diagram

The PSON# signal used to control ATX-power on and off. The ATX-power will output Vcc power while PSON# is low.



## 6.2 PWROK Block Diagram

The block diagram is shown the PWROK active condition.



## 7. CONFIGURATION REGISTER ACCESS PROTOCOL

The W83667HG-A uses a special protocol to access configuration registers to set up different types of configurations. The W83667HG-A has a total of fourteen Logical Devices (from Logical Device 0 to Logical Device F with the exception of Logical Device 4 and Logical Device E for backward compatibility) corresponding to fourteen individual functions: FDC (Logical Device 0), Parallel Port (Logical Device 1), UART A (Logical Device 2), UART B (Logical Device 3), Keyboard Controller (Logical Device 5), Serial Peripheral Interface (Logical Device 6) and GPIO6, 7, 8, 9 (Logical Device 7), WDTO# & PLED & GPIO1 (Logical Device 8), GPIO2, 3, 4, 5 (Logical Device 9), ACPI (Logical Device A), Hardware Monitor and SB-TSI (Logical Device B), PECl (Logical Device C), VID (Logical Device D), and GPIO Push-Pull/OD Select (Logical Device F).

It would require a large address space to access all of the logical device configuration registers if they were mapped into the normal PC address space. The W83667HG-A, then, maps all the configuration registers through two I/O addresses (2Eh/2Fh or 4Eh/4Fh) set at power on by the strap pin HEFRAS. The two I/O addresses act as an index/data pair to read or write data to the Super I/O. One must write an index to the first I/O address which points to the register and read or write to the second address which acts as a data register.

An extra level of security is added by only allowing data updates when the Super I/O is in a special mode, called the Extended Function Mode. This mode is entered by two successive writes of 87h data to the first I/O address. This special mode ensures no false data can corrupt the Super I/O configuration during a program runaway.

There are a set of global registers located at index 0h – 2Fh, containing information and configuration for the entire chip.

The method to access the control registers of the individual logical devices is straightforward. Simply write the desired logical device number into the global register 07h. Subsequent accesses with indexes of 30h or higher are directly to the logical device registers.

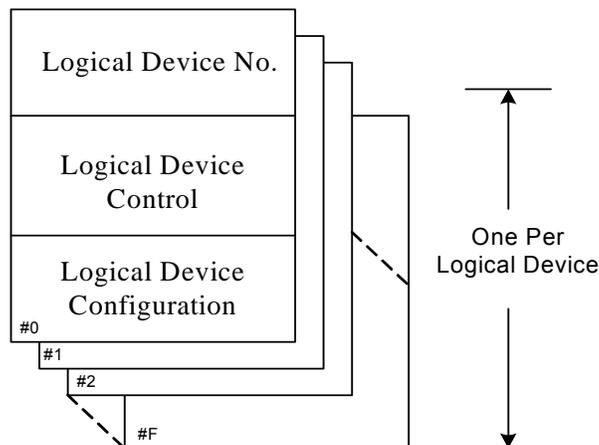


Figure 7-1 Structure of the Configuration Register

Table 7-1 Devices of I/O Base Address

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
0	FDC	100h ~ FF8h
1	Parallel Port	100h ~ FF8h
2	UART A	100h ~ FF8h
3	UART B	100h ~ FF8h
4	Reserved	
5	Keyboard Controller	100h ~ FFFh
6	Serial Peripheral Interface	100h ~ FF8h
7	GPIO 6 ~ GPIO 9	Reserved
8	WDTO# & GPIO 1	Reserved
9	GPIO 2, 3, 4, 5	Reserved
A	ACPI	Reserved
B	Hardware Monitor & SB-TSI	100h ~ FFEh
C	PECI	Reserved
D	VID	Reserved
E	Reserved	
F	GPIO Push-Pull/OD Select	Reserved

7.1 Configuration Sequence

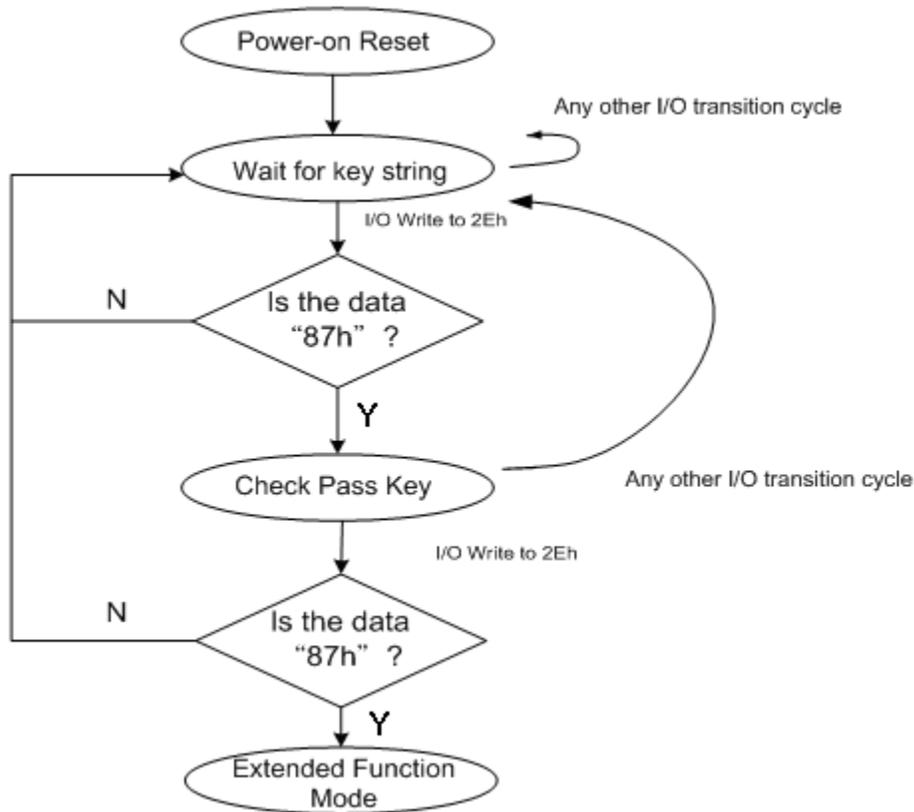


Figure 7-2 Configuration Register

To program the W83667HG-A configuration registers, the following configuration procedures must be followed in sequence:

- (1). Enter the Extended Function Mode.
- (2). Configure the configuration registers.
- (3). Exit the Extended Function Mode.

7.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

### 7.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

### 7.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

### 7.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR[26h] bit 6 showing the value of the strap pin at power on) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

This example programs the configuration register F0h (clock source) of logical device 1 (UART A) to the value of 3Ch (24MHz). First, one must enter the Extended Function Mode, then setting the Logical Device Number (Index 07h) to 01h. Then program index F0h to 3Ch. Finally, exit the Extended Function Mode.

```

;-----
; Enter the Extended Function Mode
;-----
MOV  DX, 2EH
MOV  AL, 87H
OUT  DX, AL
OUT  DX, AL

;-----
; Configure Logical Device 1, Configuration Register CRF0
;-----
MOV  DX, 2EH
MOV  AL, 07H
OUT  DX, AL      ; point to Logical Device Number Reg.
MOV  DX, 2FH
MOV  AL, 01H
OUT  DX, AL      ; select Logical Device 1
;
MOV  DX, 2EH
MOV  AL, F0H
OUT  DX, AL      ; select CRF0
MOV  DX, 2FH

```

```

MOV  AL, 3CH
OUT  DX, AL      ; update CRF0 with value 3CH
;-----
; Exit the Extended Function Mode
;-----
MOV  DX, 2EH
MOV  AL, AAH
OUT  DX, AL

```

Table 7-2 Chip (Global) Control Registers

INDEX	R/W	DEFAULT VALUE	DESCRIPTION
02h	Write Only		Software Reset
07h	R/W	00h	Logical Device
20h	Read Only	B3h	Chip ID, MSB
21h	Read Only	5xh	Chip ID, LSB
22h	R/W	FFh	Device Power Down
23h	R/W	00h	Immediate Power Down
24h	R/W	0100_0ss0b	Global Option
25h	R/W	00h	Interface Tri-state Enable
26h	R/W	0s000000b	Global Option
27h	R/W	FFh	Global Option
28h	R/W	50h	Global Option
29h	R/W	00h	Multi-function Pin Selection
2Ah	R/W	00h	SPI Configuration
2Bh	R/W	7Fh	GP3X Multifunction Selection
2Ch	R/W	0Ah	Multi-function Pin Selection
2Dh	R/W	08h	Multi-function Pin Selection
2Eh	R/W	00h	Reserved
2Fh	R/W	-	Strapping Function Result

S: Strapping; x: chip version.

## 8. HARDWARE MONITOR

### 8.1 General Description

The W83667HG-A monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures, all of which are very important for a high-end computer system to work stably and properly. In addition, proprietary hardware reduces the amount of programming and processor intervention to control cooling fan speeds, minimizing ambient noise and maximizing system temperature and reliability.

The W83667HG-A can simultaneously monitor all of the following inputs:

- Nine analog voltage inputs (five internal voltages CPUVCORE, VBAT, 3VSB, 3VCC and AVCC; four external voltage inputs)
- Five fan tachometer inputs
- Three remote temperatures, using either a thermistor or from the CPU thermal diode (voltage or Current Mode measurement method)
- One case-open detection signal.

These inputs are converted to digital values using the integrated, eight-bit analog-to-digital converter (ADC).

In response to these inputs, the W83667HG-A can generate the following outputs:

- Three PWM (pulse width modulation) or DC fan outputs for the fan speed control
- Beep tone output for warnings
- SMI#
- OVT# signals for system protection events

The W83667HG-A provides hardware access to all monitored parameters through the LPC or I<sup>2</sup>C interface<sup>Note1</sup>, and software access through application software, such as Nuvoton's Hardware Doctor<sup>TM</sup>, or BIOS. In addition, the W83667HG-A can generate pop-up warnings or beep tones when a parameter goes outside of a user-specified range.

Note1. LPC and SMBus could not access hardware monitor register at the same time. Under this situation read or write data may incorrectly.

The rest of this section introduces the various features of the W83667HG-A hardware-monitor capability. These features are divided into the following sections:

- Access Interfaces
- Analog Inputs
- Fan Speed Measurement and Control
- Smart Fan Control
- SMI# interrupt mode
- OVT# interrupt mode
- Registers and Value RAM

## 8.2 Access Interfaces

The W83667HG-A provides two interfaces, LPC and I<sup>2</sup>C, for the microprocessor to read or write the internal registers of the hardware monitor.

### 8.2.1 LPC Interface

The internal registers of the hardware monitor block are accessible through two separate methods on the LPC bus. The first set of registers, which primarily enable the block and set its address in the CPU I/O address space are accessed by the Super I/O protocol described in Chapter 7 at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed from an index/data pair of CPU I/O addresses. The standard locations are usually 295h/296h and are set by CR[60h]&CR[61h] accessed using the Super I/O protocol as described in Chapter 7.

Due to the number of internal register, it is necessary to separate the register sets into “banks” specified by register 4Eh. The structure of the internal registers is shown in the following figure.

### 8.2.2 I<sup>2</sup>C interface

The I<sup>2</sup>C interface is a second, serial port into the internal registers of the hardware monitor function block. The interface is totally compatible with the industry-standard I<sup>2</sup>C specification, allowing external components that are also compatible to read the internal registers of the W83667HG-A hardware monitor and control fan speeds. The address of the I<sup>2</sup>C peripheral is set by the register located at index 48h (which is accessed by the index/data pair at I/O address typically at 295h/296h)

The two timing diagrams below illustrate how to use the I<sup>2</sup>C interface to write to an internal register and how to read the value in an internal register, respectively.

(a) Serial bus write to internal address register followed by the data byte

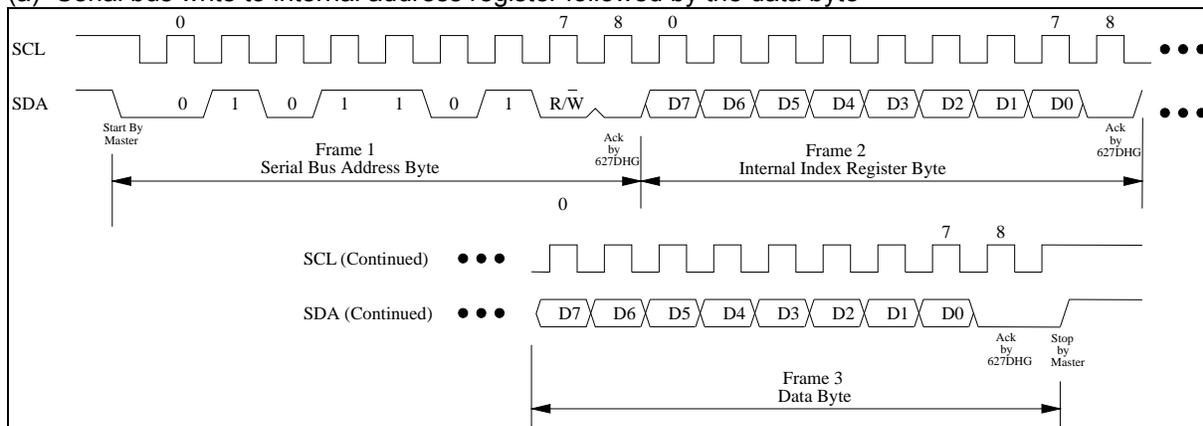


Figure 8-1 Serial Bus Write to Internal Address Register Followed by the Data Byte

(b) Serial bus read from a register

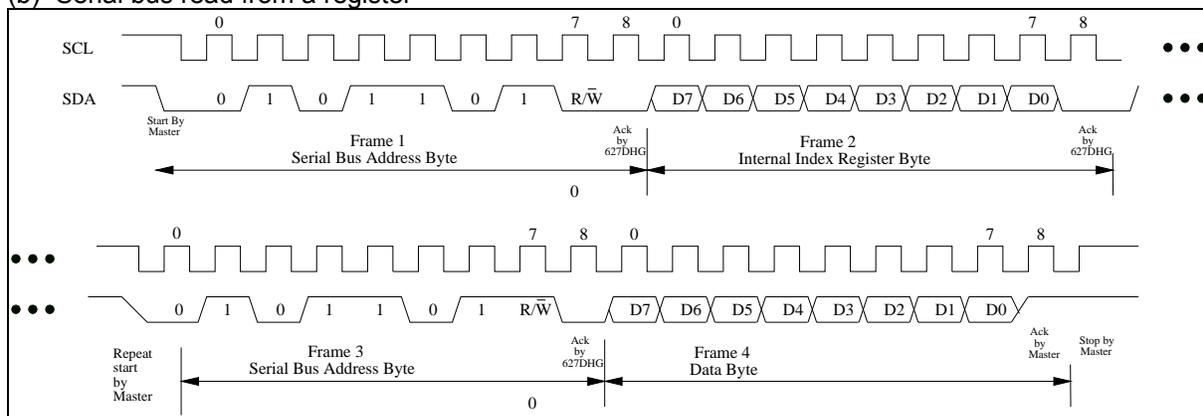


Figure 8-2 Serial Bus Read from Internal Address Register

### 8.3 Analog Inputs

The nine analog inputs of the hardware monitor block connect to an 8-bit Analog to Digital Converter (ADC) and consist of 4 general-purpose inputs connected to external device pins (VIN0 –VIN2) and five internal signals connected to the power supplies (CPUVCORE, AVCC, VBAT, 3VSB and 3VCC). All inputs are limited to a maximum voltage of 2.048V due to an internal setting of 8mV LSB (256 steps x 8mV = 2.048V). All inputs to the ADC must limit the maximum voltage by using a voltage divider. The power supplies have internal resistors, while the external pins require outside limiting resistors as described below.

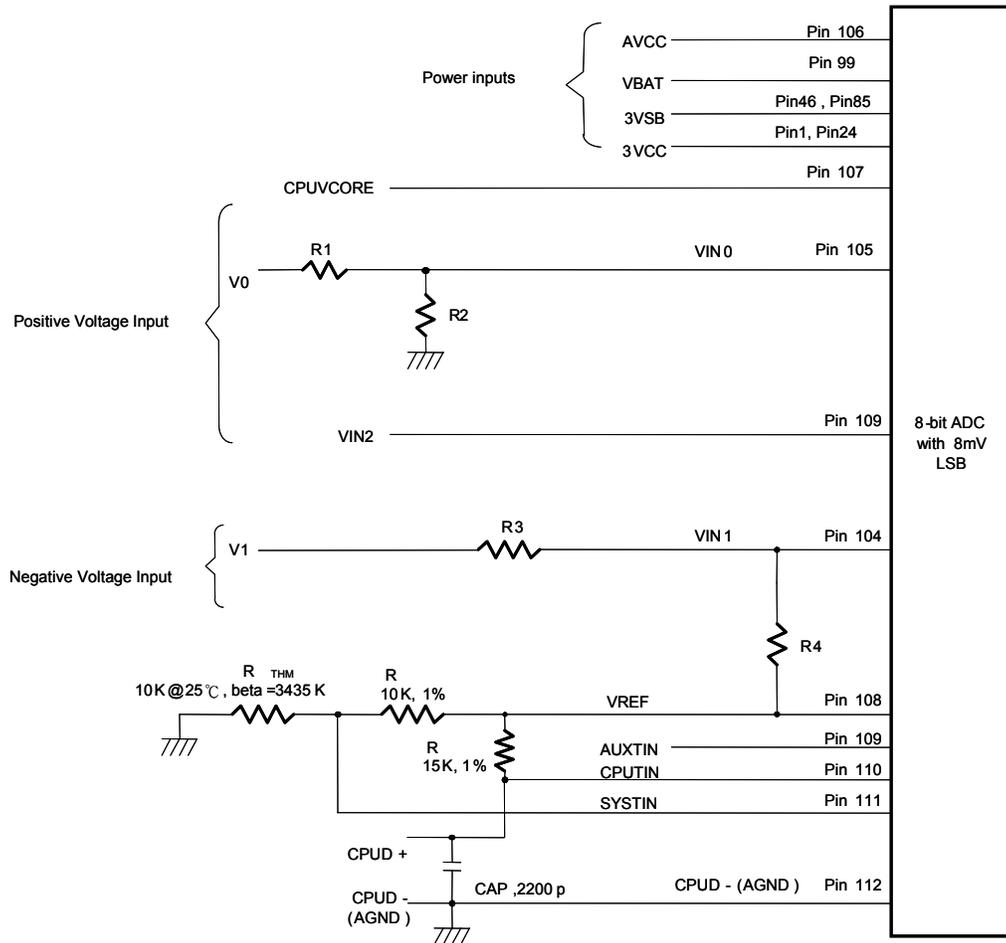


Figure 8-3 Analog Inputs and Application Circuit of the W83667HG-A

As illustrated in the figure above, other connections may require some external circuits. The rest of this section provides more information about voltages outside the range of the 8-bit ADC, CPU Vcore voltage detection, and temperature sensing

### 8.3.1 Voltages Over 2.048 V or Less Than 0 V

Input voltages greater than Pin108 VREF (Approx 2.048V) should be reduced by an external resistor divider to keep the input voltages in the proper range. For example, input voltage  $V_0$  (+12 V) should be reduced before it is connected to VIN0 according to the following equation:

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

R1 and R2 can be set to 56 K $\Omega$  and 10 K $\Omega$ , respectively, to reduce  $V_0$  from +12 V to less than 2.048 V.

All the internal inputs of the ADC, AVCC, VBAT, 3VSB and 3VCC utilize an integrated voltage divider with both resistors equal to 34K $\Omega$ , yielding a voltage one half of the power supply. Since one would expect a worst-case 10% variation or a 3.63V maximum voltage, the input to the ADC will be 1.815V, well within the maximum range.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V, \text{ where } VCC \text{ is set to } 3.3V$$

The CPUVCORE pin feeds directly into the ADC with no voltage divider since the nominal voltage on this pin is only 1.2V.

Negative voltages are handled similarly, though the equation looks a little more complicated. For example, negative voltage  $V_1$  (-12V) can be reduced according to the following equation:

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, \text{ where } V_1 = -12$$

R3 and R4 can be set to 232 K $\Omega$  and 10 K $\Omega$ , respectively, to reduce negative input voltage  $V_1$  from -12 V to less than 2.048 V. Note that R4 is referenced to VREF, or 2.048V instead of 0V to allow for more dynamic range. This is simply good analog practice to yield the most precise measurements.

Both of these solutions are illustrated in the figure above.

### 8.3.2 Voltage Data Format

The data format for voltage detection is an eight-bit value, and each unit represents an interval of 8 mV.

$$\text{Detected Voltage} = \text{Reading} * 0.008 \text{ V}$$

If the source voltage was reduced by a voltage divider, the detected voltage value must be scaled accordingly.

### 8.3.3 Temperature Data Format

The data format for sensors SYSTIN, CPUTIN and AUXIN is 9-bit, two's-complement. This is illustrated in the table below.

Table 8-1 Temperature Data Format

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

For nine-bit temperature data, the 8 MSB are read from Bank0 Index[27h], Bank1 / Bank2 Index[50h], and the LSB is read from Bank0 Index[7Ch] bit7, Bank1 / Bank2 Index[51h] bit 7. There are two sources of temperature data: external thermistors or thermal diodes.

**8.3.3.1. Monitor Temperature from Thermistor**

External thermistor should have a  $\beta$  value of 3435K and a resistance of 10 K $\Omega$  at 25°C. As illustrated in the schematic above, the thermistor is connected in series with a 10-K $\Omega$  resistor and then connects to VREF (pin 108). The configuration registers to select a thermistor temperature sensor and the measurement method are found at Bank 0, index 5Dh and 5Eh.

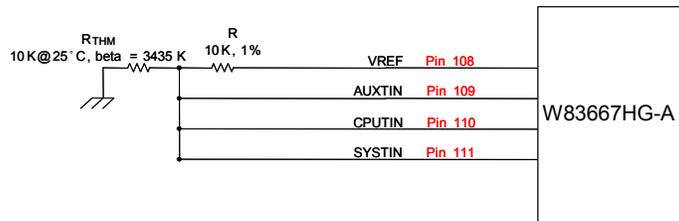
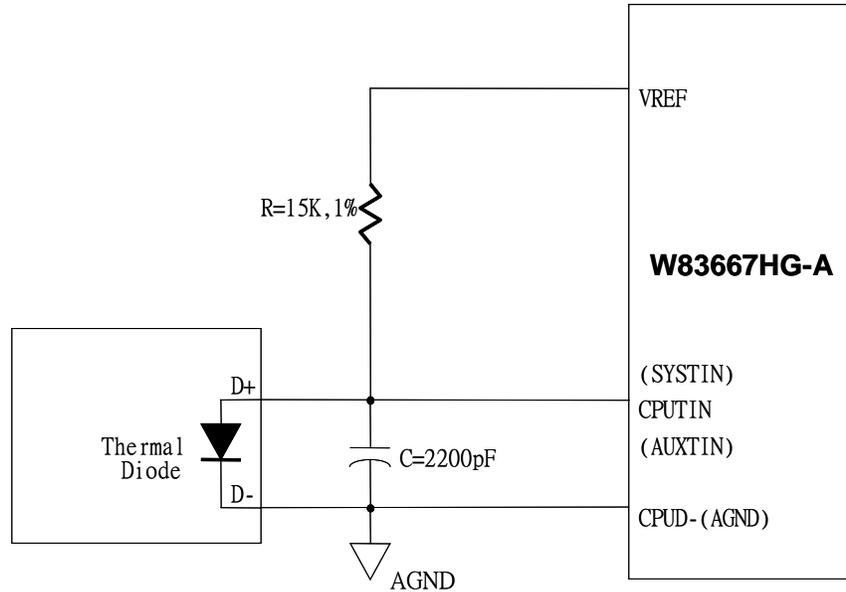


Figure 8-4 Monitoring Temperature from Thermistor

**8.3.3.2. Monitor Temperature from Thermal Diode (Voltage Mode)**

The thermal diode D- pin is connected to AGND (pin 112), and the D+ pin is connected to the temperature sensor pin in the W83667HG-A. A 15-K $\Omega$  resistor is connected to VREF to supply the bias current for the diode, and the 2200-pF, bypass capacitor is added to filter high-frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh and 5Eh.

Figure 8-5 Monitoring Temperature from Thermal Diode (Voltage Mode)



**8.3.3.3. Monitor Temperature from Thermal Diode (Current Mode)**

The W83667HG-A can also sense the diode temperature through Current Mode and the circuit is shown in the following figure.

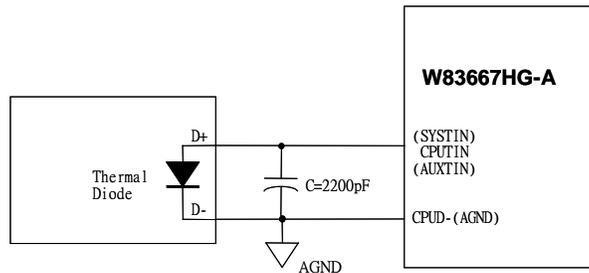


Figure 8-6 Monitoring Temperature from Thermal Diode (Current Mode)

The pin of processor D- is connected to CPUD- (pin 112) and the pin D+ is connected to temperature sensor pin in the W83667HG-A. A bypass capacitor C=2200pF should be added to filter the high frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh and 5Eh.

8.3.3.4. Relative Register of Temperature Sensing

Table 8-2 Sensor type setting:

	SYSTIN	CPUTIN	AUXTIN
<b>Thermistor</b>	<b>(Default of SYSTIN)</b> Bank0, index5D[1]=0 Bank0, index5E[1]=0	Bank0, index5D[2]=0 Bank0, index5E[2]=0	<b>(Default of AUXTIN)</b> Bank0, index5D[3]=0 Bank0, index5E[3]=0
<b>Current mode (Thermal diode)</b>	Bank0, index5D[1]=1 Bank0, index5E[1]=1	<b>(Default of CPUTIN)</b> Bank0, index5D[2]=1 Bank0, index5E[2]=1	Bank0, index5D[3]=1 Bank0, index5E[3]=1
<b>Voltage mode (Thermal diode)</b>	Bank0, index5D[1]=1 Bank0, index5E[1]=0	Bank0, index5D[2]=1 Bank0, index5E[2]=0	Bank0, index5D[3]=1 Bank0, index5E[3]=0

Table 8-3 Temperature reading selection and data register

Temperature Source Select : Bank0,Index7D bit2~0				Report Temperature Register
bit2~0=000	SYSTIN	bit2~0=100	PECI agent 1	<b>Bank0 Index7E (Read Only)</b>
bit2~0=001	CPUTIN	bit2~0=101	PECI agent 2	
bit2~0=010	AUXTIN	bit2~0=110	PECI agent 3	
bit2~0=011	AMDTSI	bit2~0=111	PECI agent 4	

Besides, SMART FAN Control referred temperature source select register (Bank0 Index49 and 4A) also can report temperature data (Bank0\_Index27, Bank1\_Index50 and Bank2\_Index50) for monitor purpose.

Table 8-4 SMART FAN control referred temp source

		SYSFANOUT	CPUFANOUT	AUXFANOUT
<b>SMART FAN Control Referred Temp Source</b>	<b>Referred Temp Source Data (Read Only)</b>	Bank0, Index27 (Integer) Index7C,bit7 (0.5°C)	Bank1, Index50 (Integer) Index51,bit7 (0.5°C)	Bank2, Index50 (Integer) Index51,bit7 (0.5°C)
	<b>Temp Source Select</b>	Bank0,Index4A, bit7~5 000: SYSTIN (Default) 001: CPUTIN 010: AUXTIN 011: AMDTSI 100: Peci agent 1 101: Peci agent 2 110: Peci agent 3 111: Peci agent 4	Bank0,Index49, bit2~0 000: SYSTIN 001: CPUTIN (Default) 010: AUXTIN 011: AMDTSI 100: Peci agent 1 101: Peci agent 2 110: Peci agent 3 111: Peci agent 4	Bank0,Index49, bit6~4 000: SYSTIN 001: CPUTIN 010: AUXTIN (Default) 011: AMDTSI 100: Peci agent 1 101: Peci agent 2 110: Peci agent 3 111: Peci agent 4

## 8.4 PECCI and SB Temperature Sensor Interface (SB-TSI)

### 8.4.1 PECCI

PECCI (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECCI uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECCI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECCI is one of the temperature sensing methods that the W83667HG-A supports. The W83667HG-A contains a PECCI master and reads the CPU PECCI temperature. The CPU is a PECCI client.

The PECCI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECCI temperatures. For further information, refer to the PECCI specification. All references to "temperature" in this section are in "counts" instead of "°C".

**Figure 8-7 PECCI Temperature** shows a typical fan speed (PWM duty cycle) and PECCI temperature relationship.

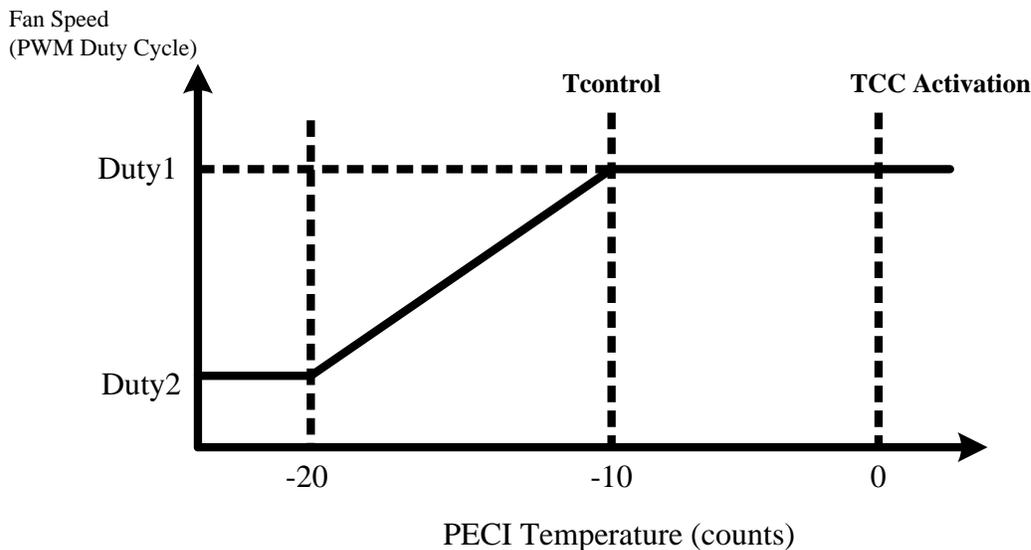


Figure 8-7 PECCI Temperature

In this illustration, when PECCI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECCI temperature is -10, the PWM duty cycle is at Duty1.

At TControl PECCI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of TControl can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The TControl MSR address is

usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, TControl is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

W83667HG-A's fan control circuit can only accept positive real-time temperature inputs and limits setting (in Smart Fan™ mode). The device provides offset registers to 'shift' the negative PECI readings to positive values otherwise the fan control circuit will not function properly. The offset registers are the TBase registers located at Logical Device C, CR[E1h]~CR[E4h]. These registers should be programmed with (positive) values so that the resultant value (Tbase + PECI) is always positive. The unit of the TBase register contents is "count" to match that of PECI values. The resultant value (TBase + PECI) should not be interpreted as the "temperature" (whether in count or °C) of the PECI client (CPU).

**Figure 8-8 Temperature and Fan Speed Relation after Tbase Offsets** shows the temperature/fan speed relationship after Tbase offsets are applied (based on **Figure 8-7 PECI Temperature**). This view is from the perspective of the W83667HG-A fan control circuit.

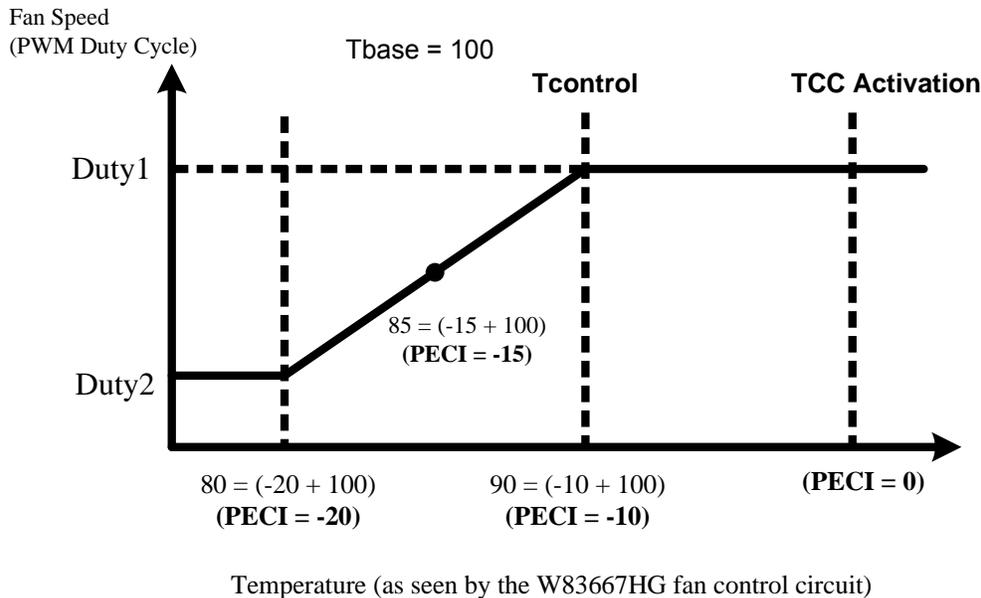


Figure 8-8 Temperature and Fan Speed Relation after Tbase Offsets

Assuming TBase is set to 100 and the PECI temperature is -15, the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using Smart Fan control function of W83667HG-A, BIOS/software must include Tbase in determining the thresholds (limits). In this example, assuming TControl is -10 and Tbase is set to 100<sup>(1)</sup>, the threshold temperature value corresponding to the "100% fan duty cycle" event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

(1) TControl is typically -10 to -20 for PECI-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is

applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of TControl to match the specific application.

### 8.4.2 SB Temperature Sensor Interface (SB-TSI)

The W83667HG-A is equipped with a built-in temperature sensor which uses the SBI Temperature Sensor Interface (SB-TSI) interface. The SB-TSI largely follows SMBus v2.0 specification except:

- The statement “An SMBus device must always acknowledge (ACK) its own address “does not apply since a processor may NACK on repeated start conditions even if the address matches its own SMBus address.
- Only 7-bits SMBus addresses are supported.
- SB-TSI implements the Send/Receive Byte and Read/Write Byte protocols.
- SB-TSI registers can only be written using a write byte command.
- Address Resolution Protocol (ARP) is not implemented.
- Packet Error Checking (PEC) is not supported.

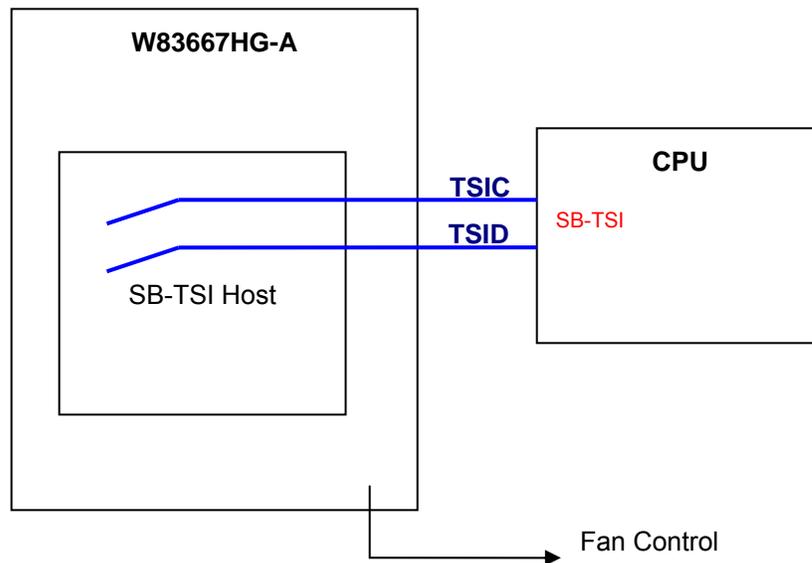


Figure 8-9 AMD-TSI Illustration

SB-TSI temperature readings and limit registers encode the temperature in increments of one eighth of a degree from 0 to 255.875. The high byte represents the integer portion of the temperature from 0 to 255. One increment in the high byte is equivalent to a step of 1°C. The upper three bits of the low byte represent the decimal portion of the temperature. One increment of these bits is equivalent to a step of 0.125°C.

Table 8-5 SB-TSI Temperature Encoding Examples

TEMPERATURE	TEMPERATURE HIGH BYTE	TEMPERATURE LOW BYTE
0.000°C	0000_0000b	0000_0000b
1.000°C	0000_0001b	0000_0000b
25.125°C	0001_1001b	0010_0000b
50.500°C	0011_0010b	1000_0000b
127.875°C	0111_1111b	1110_0000b
128.000°C	1000_0000b	0000_0000b
255.875°C	1111_1111b	1110_0000b

## 8.5 Fan Speed Measurement and Control

This section is divided into two parts, one to measure the speed and one to control the speed.

### 8.5.1 Fan Speed Measurement

The W83667HG-A can measure fan speed for fans equipped with tachometer outputs. The tachometer signals should be set to TTL-level, and the maximum input voltage cannot exceed +3.3 V. If the tachometer signal exceeds +3.3 V, an external trimming circuit should be added to reduce the voltage accordingly.

The fan speed counter is read from Bank0 Index 28h, 29h, 2Ah, and 3Fh and Bank5 index 53h. The fan speed can then be evaluated by the following equation:

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 8 and is specified at Bank0 Index 47h, bits 7 ~ 4; Index 4Bh, bits 7 ~ 6; Index 4Ch, bit 7; Index 59h, bit 7 and bits 3 ~ 2; and Index 5Dh, bits 5 ~ 7. There are three bits for each divisor, and the corresponding divisor is listed in the table below.

Table 8-6 Fan Divisor Definition

BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
0	0	0	<b>1</b>	1	0	0	<b>16</b>
0	0	1	<b>2</b>	1	0	1	<b>32</b>
0	1	0	<b>4</b>	1	1	0	<b>64</b>
0	1	1	<b>8</b>	1	1	1	<b>128</b>

FAN IN	Divisor Bit2	Divisor Bit1	Divisor Bit0	Fan Counts Reading
CPUFANIN,PIN124	B0,CR5D,bit6	B0,CR47,bit7	B0,CR47,bit6	Bank0,CR29
SYSFANIN,PIN126	B0,CR5D,bit5	B0,CR47,bit5	B0,CR47,bit4	Bank0,CR28
AUXFANIN,PIN97	B0,CR5D,bit7	B0,CR4B,bit7	B0,CR4B,bit6	Bank0,CR2A
AUXFANIN2,PIN95	B0,CR59,bit7	B0,CR59,bit3	B0,CR59,bit2	Bank5,CR53
AUXFANIN1,PIN96	B0,CR4C,bit7	B0,CR59,bit1	B0,CR59,bit0	Bank0,CR3F

The following table provides some examples of the relationship between divisor, RPM, and count.

Table 8-7 Divisor, RPM, and Count Relation

DIVISOR	NOMINAL RPM	TIME PER REVOLUTION	COUNTS	70% RPM	TIME FOR 70%
1	8800	6.82 ms	153	6160	9.84 ms
2	4400	13.64 ms	153	3080	19.48 ms
4	2200	27.27 ms	153	1540	38.96 ms
<b>8(default)</b>	1100	54.54 ms	153	770	77.92 ms
16	550	109.08 ms	153	385	155.84 ms
32	275	218.16 ms	153	192	311.68 ms
64	137	436.32 ms	153	96	623.36 ms
128	68	872.64 ms	153	48	1246.72 ms

### 8.5.2 Fan Speed Control

The W83667HG-A has three output pins for fan control, each of which offers PWM duty cycle and DC voltage to control the fan speed. The output type (PWM or DC) of each pin is configured by Bank0 Index 04h, bits 1 ~ 0 and Index 12h, bit 0.

Table 8-8 Fan Speed Control related registers

		SYSFANOUT	CPUFANOUT	AUXFANOUT
<b>Output Type Select</b>		Bank0, Index04 bit0  0: PWM output 1: DC output (default)	Bank0, Index04 bit1  0: PWM output (default) 1: DC output	Bank0, Index12 bit0  0: PWM output (default) 1: DC output
<b>Output Type Select (in PWM output)</b>		CR24 bit4  0: open-drain (default) 1: push-pull	CR24 bit3  0: open-drain (default) 1: push-pull	CR24 bit5  0: push-pull (default) 1: open-drain
<b>PWM Output Frequency</b>		Bank0, Index00	Bank0, Index02	Bank0, Index10
<b>Fan Control Mode Select</b>	<b>SMART FAN I and III</b> <sup>NOTE</sup>	Bank0, Index04, bit3~2  00: Manual mode (def.) 01: Thermal Cruise 10: Speed Cruise	Bank0, Index04, bit5~4  00: Manual mode 01: Thermal Cruise(def.) 10: Speed Cruise	Bank0, Index12, bit2~1  00: Manual mode (def.) 01: Thermal Cruise 10: Speed Cruise

**SMART FAN I and III**<sup>NOTE</sup>

		11: SMART FAN III	11: SMART FAN III	11: SMART FAN III
	<b>SMART FAN IV</b>	Bank9, Index50 bit0  0: SMART FAN I,III (def.) 1: SMART FAN IV	Bank A, Index50 bit0  0: SMART FAN I,III (def.) 1: SMART FAN IV	Bank B, Index50 bit0  0: SMART FAN I,III (def.) 1: SMART FAN IV
<b>Output Value</b> (Read/write for Manual mode; Read only for SMART FAN Control)		Bank0, Index01  PWM: bit7~0 DC: bit7~2	Bank0, Index03  PWM: bit7~0 DC: bit7~2	Bank0, Index11  PWM: bit7~0 DC: bit7~2
<b>SMART FAN Control Referred Temp Source</b>	<b>Referred Temp Source</b>	Bank0, Index27 (Read Only)	Bank1, Index50 (Read Only)	Bank2, Index50 (Read Only)
	<b>Temp Source Select</b>	Bank0, Index4A, bit7~5	Bank0, Index49, bit2~0	Bank0, Index49, bit6~4

**NOTE:** To use SMART FAN I and III, correspondingly SMART FAN IV enable bit (Bank9, A or B Index50 bit0) must be set 0.

For PWM, the duty cycle is programmed by eight-bit registers at Bank0 Index 01h, Index 03h and Index 11h. The duty cycle can be calculated using the following equation:

$$\text{Dutycycle(\%)} = \frac{\text{Programmed 8-bit Register Value}}{255} \times 100\%$$

The default duty cycle is FFh, or 100%. The PWM clock frequency is programmed at Bank0 Index 00h, Index 02h and Index 10h.

For DC, the W83667HG-A has a six bit digital-to-analog converter (DAC) that produces 0 to Vref (Approx 2.048V) Volts DC. The analog output is programmed at Bank0 Index 01h, Index 03h and Index 11h. The analog output can be calculated using the following equation:

$$\text{Output Voltage} = V_{\text{ref}} \times \frac{\text{Programmed 6-bit Register Value}}{64} \times 100\%$$

The default value is 111111YY, or nearly Vref (Pin 108), and Y is a reserved bit.

8.5.3 SMART FAN™ Control

The W83667HG-A supports various different fan control features:

- ♦ SMART FAN™ I (Thermal Cruise & Speed Cruise)
- ♦ SMART FAN™ III
- ♦ SMART FAN™ IV

Table 8-9 SMART FAN Mode selection

		SYSFANOUT	CPUFANOUT	AUXFANOUT
Fan Control Mode Select	SMART FAN I and SMART FAN III <sup>NOTE</sup>	Bank0, Index04, bit3~2  00: Manual mode (def.) 01: Thermal Cruise 10: Speed Cruise 11: SMART FAN III	Bank0, Index04, bit5~4  00: Manual mode 01: Thermal Cruise(def.) 10: Speed Cruise 11: SMART FAN III	Bank0, Index12, bit2~1  00: Manual mode (def.) 01: Thermal Cruise 10: Speed Cruise 11: SMART FAN III
	SMART FAN IV	Bank9, Index50 bit0  0: SMART FAN I,III (def.) 1: SMART FAN IV	Bank A, Index50 bit0  0: SMART FAN I,III (def.) 1: SMART FAN IV	Bank B, Index50 bit0  0: SMART FAN I,III (def.) 1: SMART FAN IV

NOTE: To use SMART FAN I and III, correspondingly SMART FAN IV enable bit (Bank9, A or B Index50 bit0) must be set 0

Each SMART FAN control output has to refer one temperature data to output corresponding duty. Referring Table 8-10 show the detail setting.

Table 8-10 Select temperature source for each fan control output

		SYSFANOUT	CPUFANOUT	AUXFANOUT
SMART FAN Control Referred Temp Source	Referred Temp Source	Bank0, Index27 (Read Only)	Bank1, Index50 (Read Only)	Bank2, Index50 (Read Only)
	Temp Source Select	Bank0, Index4A, bit7~5 000: SYSTIN (Default) 001: CPUTIN 010: AUCTIN 011: AMDTSI 100: PECI agent 1 101: PECI agent 2 110: PECI agent 3 111: PECI agent 4	Bank0, Index49, bit2~0 000: SYSTIN 001: CPUTIN (Default) 010: AUCTIN 011: AMDTSI 100: PECI agent 1 101: PECI agent 2 110: PECI agent 3 111: PECI agent 4	Bank0, Index49, bit6~4 000: SYSTIN 001: CPUTIN 010: AUCTIN (Default) 011: AMDTSI 100: PECI agent 1 101: PECI agent 2 110: PECI agent 3 111: PECI agent 4

Each fan output and corresponding temperature sensor is illustrated in the figure below.

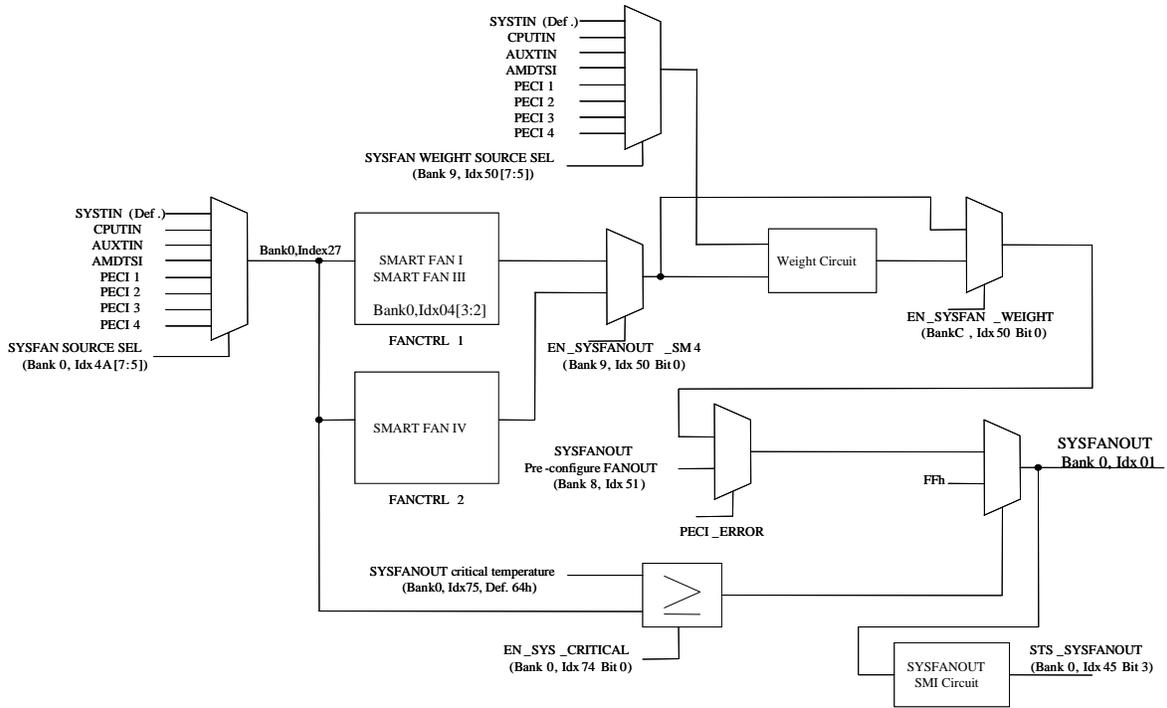


Figure 8-10 SYSFANOUT and Corresponding Temperature Sensors in SMART FAN™ I, III and IV

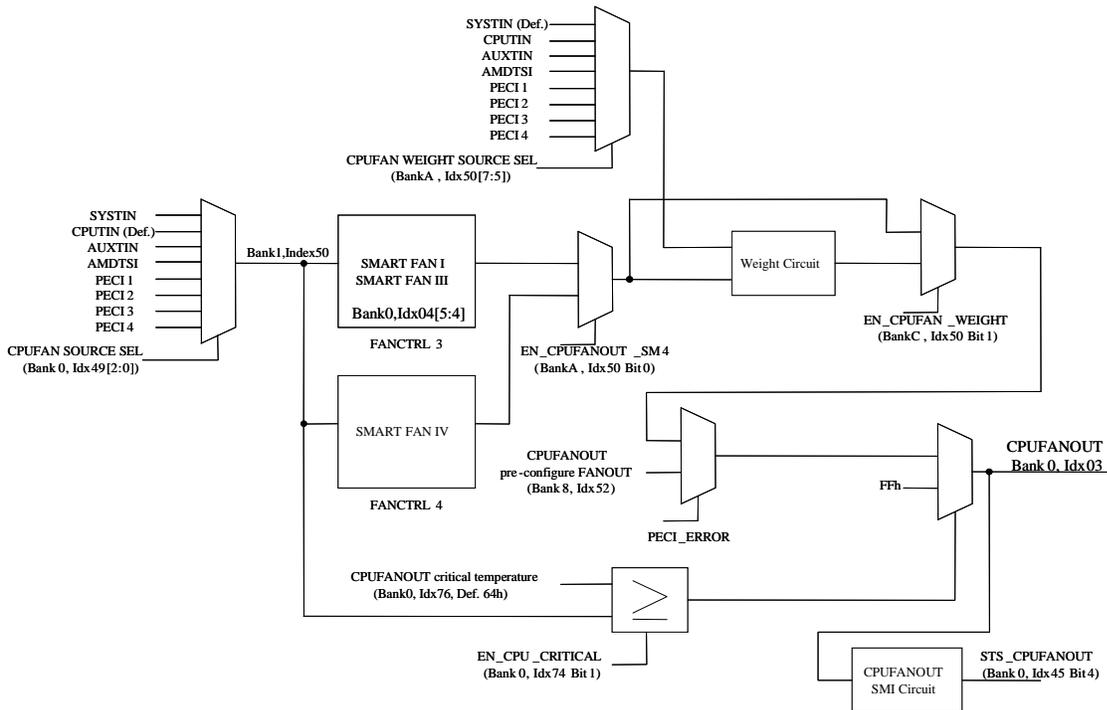


Figure 8-11 CPUFANOUT and Corresponding Temperature Sensors in SMART FAN™ I, III and IV

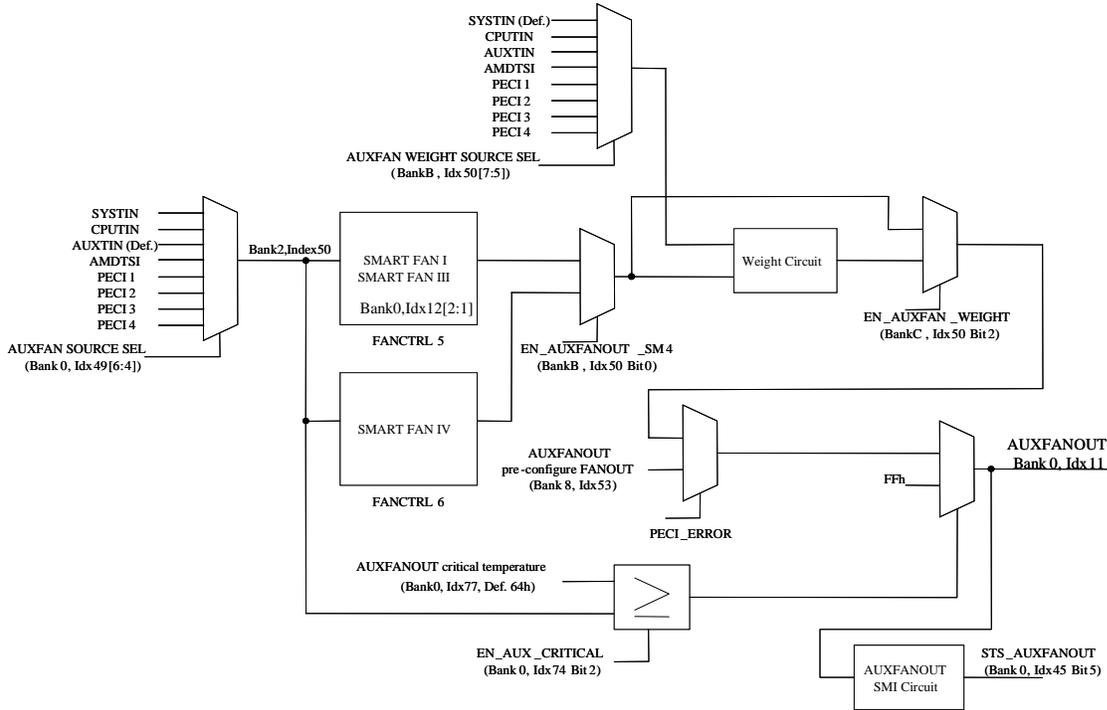


Figure 8-12 AUXFANOUT and Corresponding Temperature Sensors in SMART FAN™ I, III and IV

### 8.5.3.1. Thermal Cruise Mode

There are three pairs of temperature sensors and fan outputs in Thermal Cruise mode:

- SYSFANOUT and the temperature sensor selected by Bank0 Index 4Ah, bits 7 ~ 5. (Bit 0 of Index 50h, Bank 9 must be 0.)
- CPUFANOUT and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0. (Bit 0 of Index 50h, Bank A must be 0.)
- AUXFANOUT and the temperature sensor selected by Bank0 Index 49h, bits 6 ~ 4. (Bit 0 of Index 50h, Bank B must be 0.)

Thermal Cruise mode controls the fan speed to keep the temperature in a specified range. First, this range is defined in BIOS by a temperature and the interval (e.g., 55 °C ± 3 °C). As long as the current temperature remains below the low end of this range (i.e., 52 °C), the fan is off. Once the temperature exceeds the low end, the fan turns on at a speed defined in BIOS (e.g., 20% output). Thermal Cruise mode then controls the fan output according to the current temperature. Three conditions may occur:

- (1) If the temperature still exceeds the high end, fan output increases slowly. If the fan is operating at full speed but the temperature still exceeds the high end, a warning message is issued to protect the system.
- (2) If the temperature falls below the high end (e.g., 58°C) but remains above the low end (e.g., 52 °C), fan output remains the same.
- (3) If the temperature falls below the low end (e.g., 52 °C), fan output decreases slowly to zero or to a specified “stop value”. This stop value is enabled by Bank0 Index12h, bits 3 ~ 5, and the value itself is specified in Bank0 Index08h, Index09h and Index15h. The fan remains at the stop value for the period of time defined in Bank0 Index0Ch, Index0Dh and Index17h.

In general, Thermal Cruise mode means

- if the current temperature is higher than the high end, increase the fan speed;
- if the current temperature is lower than the low end, decrease the fan speed;
- otherwise, keep the fan speed the same.

The following figures illustrate two examples of Thermal Cruise mode.

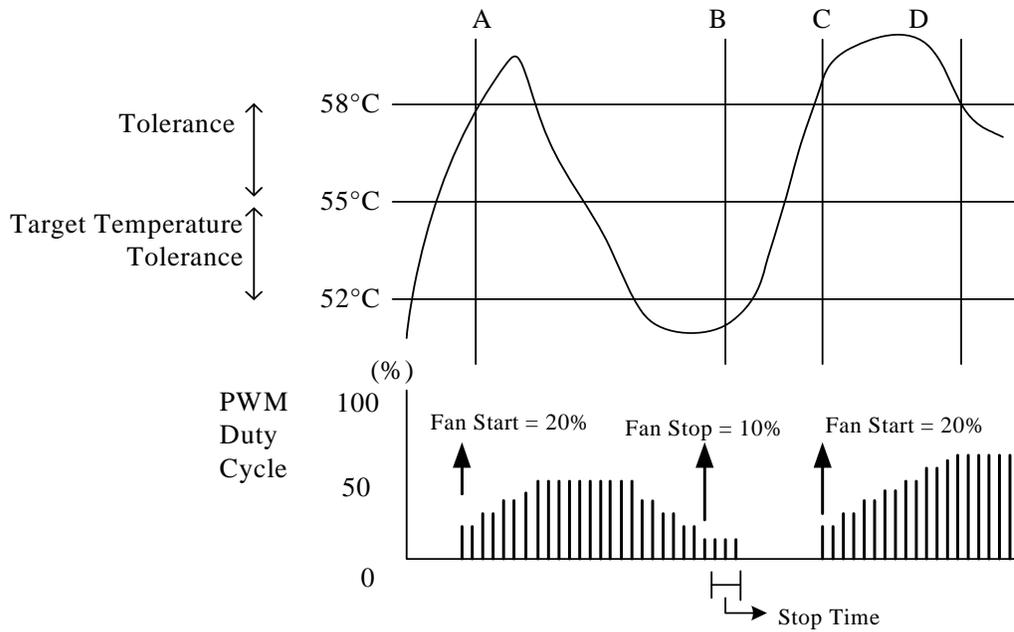


Figure 8-13 Mechanism of Thermal Cruise™ Mode (PWM Duty Cycle)

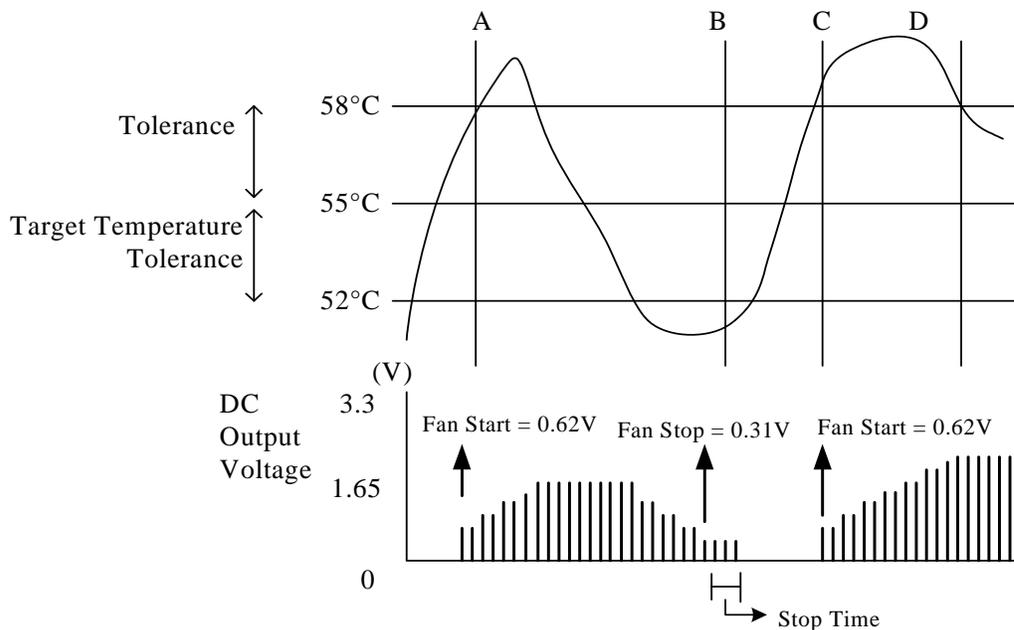


Figure 8-14 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)

The following tables show the relative control registers in Thermal Cruise.

Table 8-11 Relative Registers - at Thermal Cruise™ Mode

THERMAL-CRUISE MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP-DOWN TIME	STEP-UP TIME
SYSFANOUT	Bank 0, Index 05h	Bank 0, Index 07h, Bit0-3	Bank 0, Index 0Ah	Bank 0, Index 08h	Bank 0, Index 12h, Bit5	Bank 0, Index 0Ch	Bank 0, Index 0Eh	Bank 0, Index 0Fh
CPUFANOUT	Bank 0, Index 06h	Bank 0, Index 07h, Bit4-7	Bank 0, Index 0Bh	Bank 0, Index 09h	Bank 0, Index 12h, Bit4	Bank 0, Index 0Dh	Bank 0, Index 70h	Bank 0, Index 71h
AUXFANOUT	Bank 0, Index 13h	Bank 0, Index 14h, Bit0-3	Bank 0, Index 16h	Bank 0, Index 15h	Bank 0, Index 12h, Bit3	Bank 0, Index 17h	Bank 0, Index 72h	Bank 0, Index 73h
<b>THERMAL-CRUISE MODE</b>	<b>ENABLE THERMAL CRUISE MODE</b>							
SYSFANOUT	Bank0,Index 04h,bit3~2=01							
CPUFANOUT	Bank0,Index 04h,bit5~4=01							
AUXFANOUT	Bank0,Index 12h,bit2~1=01							

### 8.5.3.2. Speed Cruise Mode

There are three pairs of fan input sensors and fan outputs in Fan Speed Cruise mode.

- SYSFANOUT and the temperature sensor selected by Bank0 Index 4Ah, bits 7 ~ 5. (Bit 0 of Index 50h, Bank 9 must be 0.)
- CPUFANOUT and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0. (Bit 0 of Index 50h, Bank A must be 0.)
- AUXFANOUT and the temperature sensor selected by Bank0 Index 49h, bits 6 ~ 4. (Bit 0 of Index 50h, Bank B must be 0.)

Fan Speed Cruise mode keeps the fan speed in a specified range. First, this range is defined in BIOS by a fan speed count (the amount of time between clock input signals, not the number of clock input signals in a period of time) and an interval (e.g.,  $160 \pm 10$ ). As long as the fan speed count is in the specified range, fan output remains the same. If the fan speed count is higher than the high end (e.g., 170), fan output increases to make the count lower. If the fan speed count is lower than the low end (e.g., 150), fan output decreases to make the count higher. One example is illustrated in this figure.

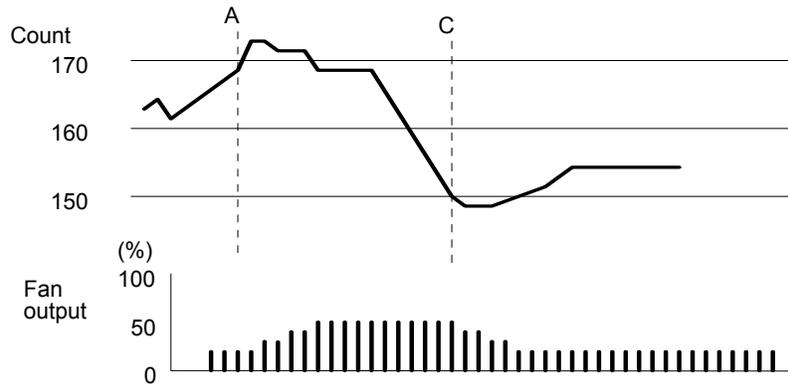


Figure 8-15 Mechanism of Fan Speed Cruise™ Mode

The following tables show current temperatures, fan output values and the relative control registers at Thermal Cruise and Fan Speed mode.

Table 8-12 Relative Registers - at Speed Cruise™ Mode

SPEED CRUISE MODE	TARGET-SPEED COUNT	TOLERANCE	KEEP MIN. FAN OUTPUT VALUE	STEP-DOWN TIME	STEP-UP TIME	ENABLE SPEED CRUISE MODE
SYSFANOUT	Bank 0, Index 05h	Bank 0, Index 07h, Bit0-3	Bank 0, Index 12h, Bit5	Bank 0, Index 0Eh	Bank 0, Index 0Fh	Bank0,Index 04,bit3~2=10
CPUFANOUT	Bank 0, Index 06h	Bank 0, Index 07h, Bit4-7	Bank 0, Index 12h, Bit4	Bank 0, Index 70h	Bank 0, Index 71h	Bank0,Index 04,bit5~4=10
AUXFANOUT	Bank 0, Index 13h	Bank 0, Index 14h, Bit0-3	Bank 0, Index 12h, Bit3	Bank 0, Index 72h	Bank 0, Index 73h	Bank0,Index 12,bit2~1=10

Besides, critical temperature can be set by optional. Once current temperature higher than critical temperature, then fan output duty will be maximum, FFh.

Table 8-13 Critical Temperature Relative Registers for SMART FAN I, III, IV (Option)

	ENABLE CRITICAL TEMPERATURE	CRITICAL TEMPERATURE	CRITICAL TEMPERATURE TOLERANCE
SYSFANOUT	Bank 0, Index 74h, bit 0	Bank0, Index75h	BankD,Index52h
CPUFANOUT	Bank 0, Index 74h, bit 1	Bank0, Index76h	BankD,Index53h
AUXFANOUT	Bank 0, Index 74h, bit 2	Bank0, Index77h	BankD,Index54h

**8.5.3.3 SMART FAN™ III**

SMART FAN™ III controls the fan speed so that the temperature meets the target temperature set in BIOS or application software. There are three pairs of fan outputs and temperature sensors in SMART FAN™ III mode.

- SYSFANOUT and the temperature sensor selected by Bank0 Index 4Ah, bits 7 ~ 5. (Bit 0 of Index 50h, Bank 9 must be 0)
- CPUFANOUT and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0. (Bit 0 of Index 50h, Bank 0 must be 0)
- AUXFANOUT and the temperature sensor selected by Bank0 Index 49h, bits 6 ~ 4. (Bit 0 of Index 50h, Bank B must be 0)

The algorithm is as follows:

- (1) The target temperature, temperature tolerance, maximum and minimum fan outputs and step are set.
- (2) The following figure shows the initial conditions. If the current temperature is within (Target Temperature ± Temperature Tolerance), the fan speed remains constant.

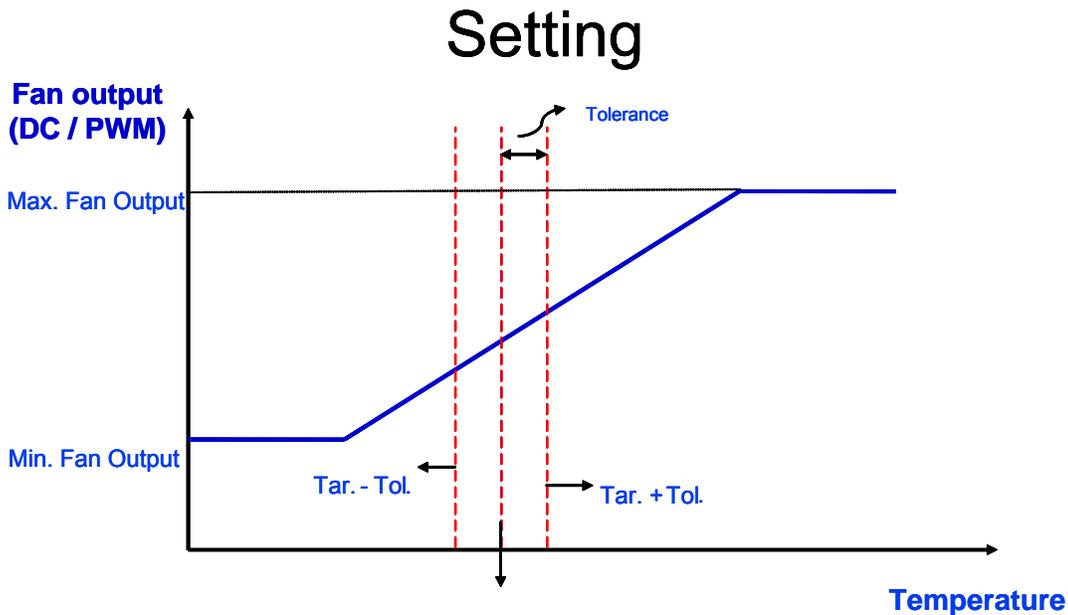


Figure 8-16 Setting of SMART FAN™ III

- (3) If the current temperature is higher than (Target Temperature + Temperature Tolerance), fan speed rises one step. The step is the value in the CPUFANOUT Output Value Select Register, Bank0 Index03h or Index61h. In addition, the target temperature shifts to (Target Temperature + Temperature Tolerance), creating a new target temperature, named Target Temperature 1 in this figure.

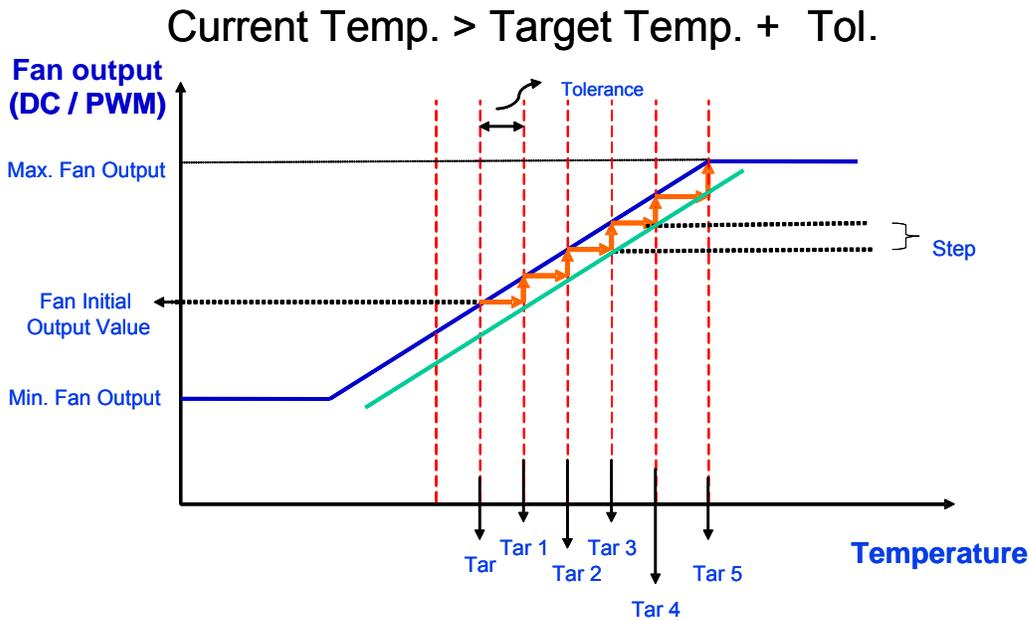


Figure 8-17 SMART FAN™ III Mechanism (Current Temp. > Target Temp. + Tol.)

If the current temperature rises higher than (Target Temperature 1 + Temperature Tolerance), the fan speed rises one step again, and the target temperature shifts to (Target Temperature 1 + Temperature Tolerance), or Target Temperature 2. This process repeats whenever the current temperature is higher than (Target Temperature X ± Temperature Tolerance) or until the fan speed reaches its maximum speed.

- (4) If the current temperature falls below (Target Temperature – Temperature Tolerance), the fan speed falls one step. The step is the value in the CPUFANOUT Output Value Select Register, Bank0 Index03h or Index61h. In addition, the target temperature shifts to (Target Temperature – Temperature Tolerance), creating a new target temperature named Target Temperature 1. This is illustrated in the figure below.

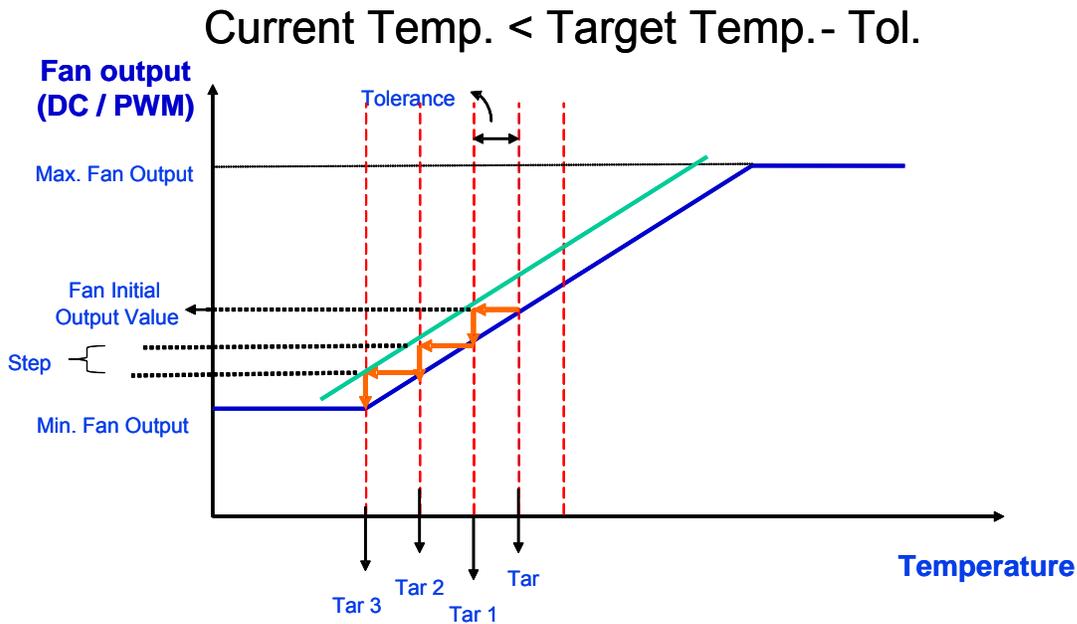


Figure 8-18 SMART FAN™ III Mechanism (Current Temp. < Target Temp. - Tol.)

If the current temperature falls lower than (Target Temperature 1 – Temperature Tolerance), the fan speed is reduced one step again, and the target temperature shifts to (Target Temperature 1 – Temperature Tolerance), or Target Temperature 2. This process repeats whenever the current temperature is lower than (Target Temperature X – Temperature Tolerance) or until the fan speed reaches its minimum speed.

- (5) If the current temperature is always lower than (Target Temperature X – Temperature Tolerance), the fan speed decreases slowly to zero or to a specified stop value. The stop value is enabled by register Bank0 12h, bit 4 and bit 6, and the stop value is specified in Bank0 Index09h and Index 64h. The fan remains at the stop value for the period of time defined in Bank0 Index0Dh and Index 66h.

The following tables show current temperatures, fan output values and the relative control registers at SMART FAN™ III mode.

Table 8-14 Relative Register-at **SMART FAN™ III** Control Mode

DESCRIPTION	TARGET TEMPERATURE	TOLERANCE	STOP VALUE (MIN. FAN OUTPUT) NOTE1	MAX. FAN OUTPUT	STOP TIME
SYSFANOUT	Bank 0, Index 05h	Bank 0, Index 07, bit 0-3	Bank 0, Index 08h	Bank 0, Index 67h	Bank 0, Index 0Ch
CPUFANOUT	Bank 0, Index 06h	Bank 0, Index 07h, bit 4-7	Bank 0, Index 09h	Bank 0, Index 69h	Bank 0, Index 0Dh
AUXFANOUT	Bank 0, Index 13h	Bank 0, Index 14h, bit 0-3	Bank 0, Index 15h	Bank 0, Index 6Bh	Bank 0, Index 17h
DESCRIPTION	OUTPUT STEP	STEP DOWN TIME	STEP UP TIME	KEEP MIN. FAN OUTPUT VALUE	INITIAL VALUE NOTE1
SYSFANOUT	Bank 0, Index 68h	Bank 0, Index 0Eh	Bank 0, Index 0Fh	Bank 0, Index 12h, bit 5	Bank 0, Index 01h
CPUFANOUT	Bank 0, Index 6Ah	Bank 0, Index 70h	Bank 0, Index 71h	Bank 0, Index 12h, bit 4	Bank 0, Index 03h
AUXFANOUT	Bank 0, Index 6Ch	Bank 0, Index 72h	Bank 0, Index 73h	Bank 0, Index 12h, bit 3	Bank 0, Index 11h
DESCRIPTION	ENABLE SMART FAN III NOTE2	Note: 1. Set INITIAL VALUE as the same parameter of STOP VALUE. 2. Enable SMART FAN III must be the last step after whole parameters are decided. Set to manual mode if any parameter needs to be changed then enable SMART FAN III.			
SYSFANOUT	Bank0,Index 04h, bit3~2=11				
CPUFANOUT	Bank0,Index 04h, bit5~4=11				
AUXFANOUT	Bank0,Index 12h, bit2~1=11				

Table 8-15 Critical Temperature Relative Registers for SMART FAN I, III, IV (Option)

	ENABLE CRITICAL TEMPERATURE	CRITICAL TEMPERATURE	CRITICAL TEMPERATURE TOLERANCE
SYSFANOUT	Bank 0, Index 74h, bit 0	Bank0, Index75h	BankD,Index52h
CPUFANOUT	Bank 0, Index 74h, bit 1	Bank0, Index76h	BankD,Index53h
AUXFANOUT	Bank 0, Index 74h, bit 2	Bank0, Index77h	BankD,Index54h

8.5.3.4 SMART FAN™ IV

SMART FAN™ IV offers 5 slopes to control the fan speed. There are three pairs of fan outputs and temperature sensors in SMART FAN™ IV mode.

- SYSFANOUT and the temperature sensor selected by Bank0 Index 4Ah, bits 7 ~ 5
- CPUFANOUT and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0
- AUXFANOUT and the temperature sensor selected by Bank0 Index 49h, bits 6 ~ 4

The 5 slopes can be obtained by setting PWM1~PWM6 and Temperature1~Temperature6 through the registers. When the temperature rises, FAN Output will calculate the DC/PWM output based on the current slope. For example, in the following figure, T1~T6 are the temperature set and DC/PWM1 ~ DC/PWM6 are the fan output set. Assume Tx is the current temperature and DC/PWMy is the fan output, then

The slope:

$$X3 = \frac{(DC/PWM4) - (DC/PWM3)}{(T4 - T3)}$$

Fan Output:

$$DC/PWMy = (DC/PWM3) + (Tx - T3) \cdot X3$$

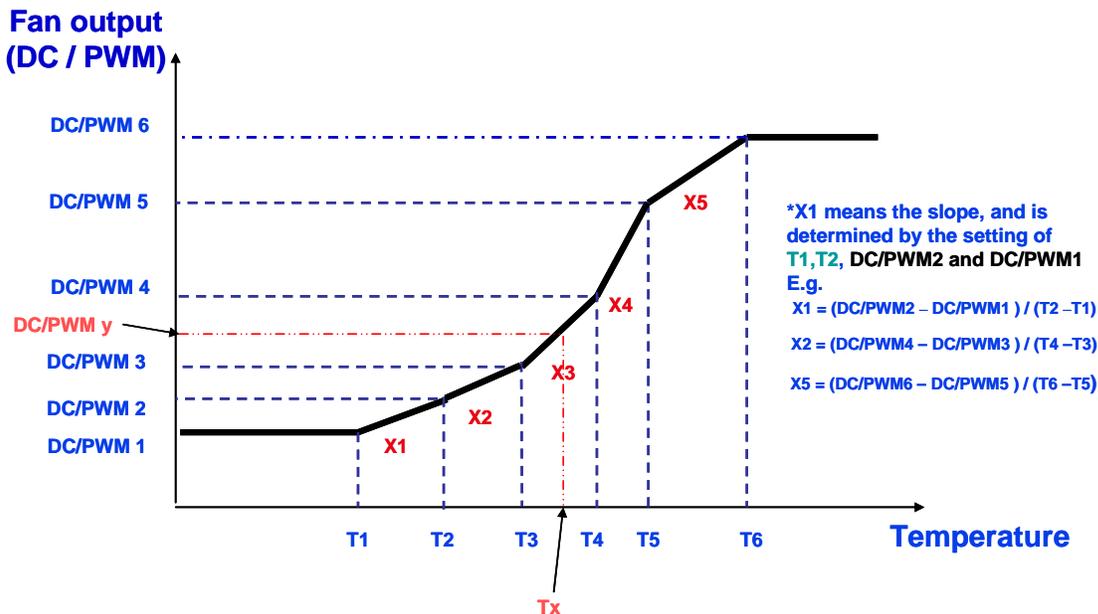


Figure 8-19 SMART FAN™ IV Mechanism

In addition, SMART FAN™ IV can also set “tolerances” for monitored-temperature and critical-temperature respectively. By setting tolerances for monitored-temperature and critical-temperature, the curve becomes saw-toothed; see on Figure 8-20. When set the tolerance for monitored-temperature, the fan output value will only update when “**current monitored-temperature > last monitored-temperature + tolerance**” or “**current monitored-temperature < last monitored-temperature - tolerance**”. Furthermore, if 「critical-temperature」 and 「critical-temperature tolerance」 is set, once the current temperature exceeds “critical-temperature”, the fan output value will output 100% (Full speed) value immediately. And the fan output value will return to original SMART FAN™ IV’s slope when current temperature is under “**critical temperature – critical temperature tolerance**”.

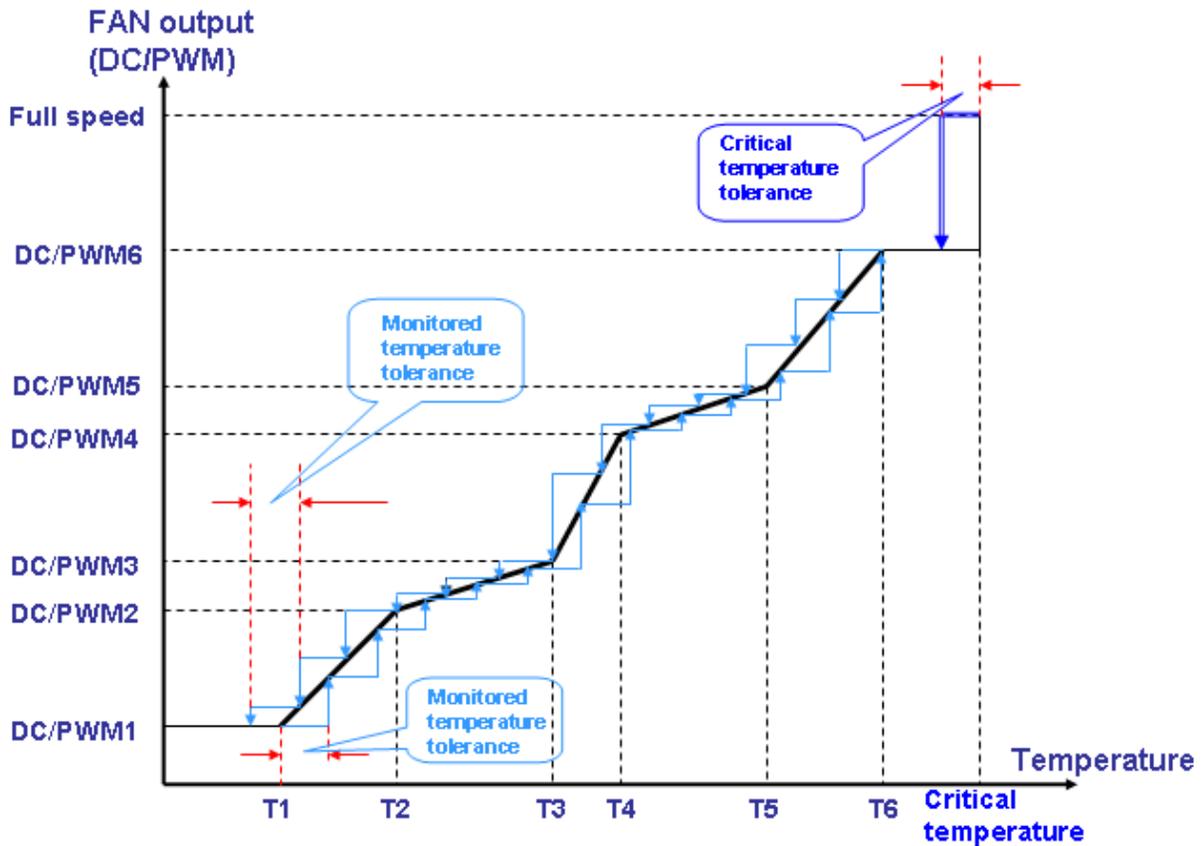


Figure 8-20 Setting of SMART FAN™ IV

Table 8-16 SMART FAN™ IV Control Mode Relative Register

DESCRIPTION	T1	T2	T3	T4	T5	T6
SYSFANOUT	Bank 9, Index 51h	Bank 9, Index 52h	Bank 9, Index 53h	Bank 9, Index 54h	Bank 9, Index 55h	Bank 9, Index 56h
CPUFANOUT	Bank A, Index 51h	Bank A, Index 52h	Bank A, Index 53h	Bank A, Index 54h	Bank A, Index 55h	Bank A, Index 56h
AUXFANOUT	Bank B, Index 51h	Bank B, Index 52h	Bank B, Index 53h	Bank B, Index 54h	Bank B, Index 55h	Bank B, Index 56h
DESCRIPTION	DC/PWM1	DC/PWM2	DC/PWM3	DC/PWM4	DC/PWM5	DC/PWM6
SYSFANOUT	Bank 9, Index 57h	Bank 9, Index 58h	Bank 9, Index 59h	Bank 9, Index 5Ah	Bank 9, Index 5Bh	Bank 9, Index 5Ch
CPUFANOUT	Bank A, Index 57h	Bank A, Index 58h	Bank A, Index 59h	Bank A, Index 5Ah	Bank A, Index 5Bh	Bank A, Index 5Ch
AUXFANOUT	Bank B, Index 57h	Bank B, Index 58h	Bank B, Index 59h	Bank B, Index 5Ah	Bank B, Index 5Bh	Bank B, Index 5Ch
DESCRIPTION	Tolerance <small>NOTE1.</small>	STEP DOWN TIME <small>NOTE1.</small>	STEP UP TIME <small>NOTE1.</small>	TARGET TEMPERATU RE <small>NOTE2.</small>	Enable SMART FAN IV <small>NOTE3.</small>	
SYSFANOUT	Bank 0, Index 07, bit 0-3	Bank 0, Index 0Eh	Bank 0, Index 0Fh	Bank 0, Index 05h	Bank 9, Index 50h, bit0=1	
CPUFANOUT	Bank 0, Index 07h, bit 4-7	Bank 0, Index 70h	Bank 0, Index 71h	Bank 0, Index 06h	Bank A, Index 50h, bit0=1	
AUXFANOUT	Bank 0, Index 14h, bit 0-3	Bank 0, Index 72h	Bank 0, Index 73h	Bank 0, Index 13h	Bank B, Index 50h, bit0=1	

**NOTE:**

- Step down and up time are only useful when Tolerance setting value is not 00h. Step down/up time means the delay time for current fan output value decrease/increase to next step would take.
- Set Target Temperature as the same value as T1.
- Enable SMART FAN IV after all setting is done.

Table 8-17 Critical Temperature Relative Registers for SMART FAN I, III, IV (Option)

	ENABLE CIRITICAL TEMPERATURE	CRITICAL TEMPERATURE	CRITICAL TEMPERATURE TOLERENCE
SYSFANOUT	Bank 0, Index 74h, bit 0	Bank0, Index75h	BankD, Index52h
CPUFANOUT	Bank 0, Index 74h, bit 1	Bank0, Index76h	BankD, Index53h
AUXFANOUT	Bank 0, Index 74h, bit 2	Bank0, Index77h	BankD, Index54h

### 8.5.4 Weight Value Control

The W83667HG-A supports weight value control for fan duty output. By register configuration, the results of weight value circuit can be added to the fan duty of SMART FAN™ I、III or IV and output to the fan. Take CPUFANOUT for example, if SMART FAN™ IV is selected, CPUTIN is the temperature source, and weight value control is enabled, SMART FAN™ IV will calculate the output duty, and weight value circuit will calculate the corresponding weight value based on SYSTIN. As the SYSTIN temperature rises, its corresponding weight value increases. Then, the two values will be summed up and output to CPU fan. In other words, the CPU fan duty is affected not only by the CPUTIN but also the SYSTIN temperature.

**Figure 8-21 SYS TEMP and Weight Value Relations** shows the relation between the SYSTIN temperature and the weight value. Tolerance setup is offered on each change point to avoid weight value fluctuation resulted from SYSTIN temperature change. The weight value will increase by one weight value step only when the SYSTIN temperature is higher than the point value plus tolerance. Likewise, the weight value decreases by one weight value step only when the SYSTIN temperature is lower than the point value minus tolerance.

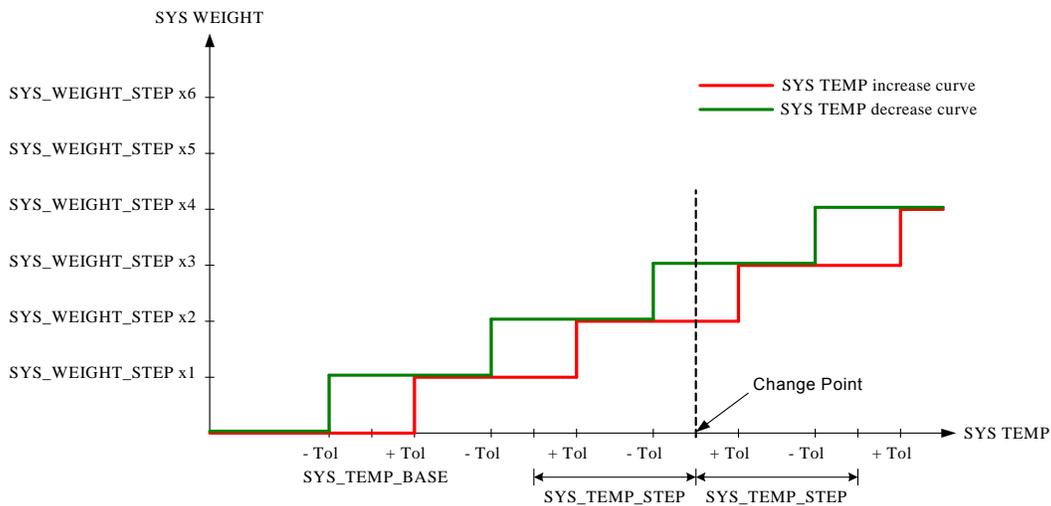


Figure 8-21 SYS TEMP and Weight Value Relations

**Figure 8-22 Fan out Duty Curves** illustrates the curves of Fanout Duty. With different register setup, the user can define n curves. As the SYSTIN temperature rises, the curve may jump from curve 1 to curve 2, curve 2 to curve 3, ... and curve n-1 to curve n. Likewise, as the temperature falls, the curve may change from curve n to curve n-1, ... , and curve 2 to curve 1.

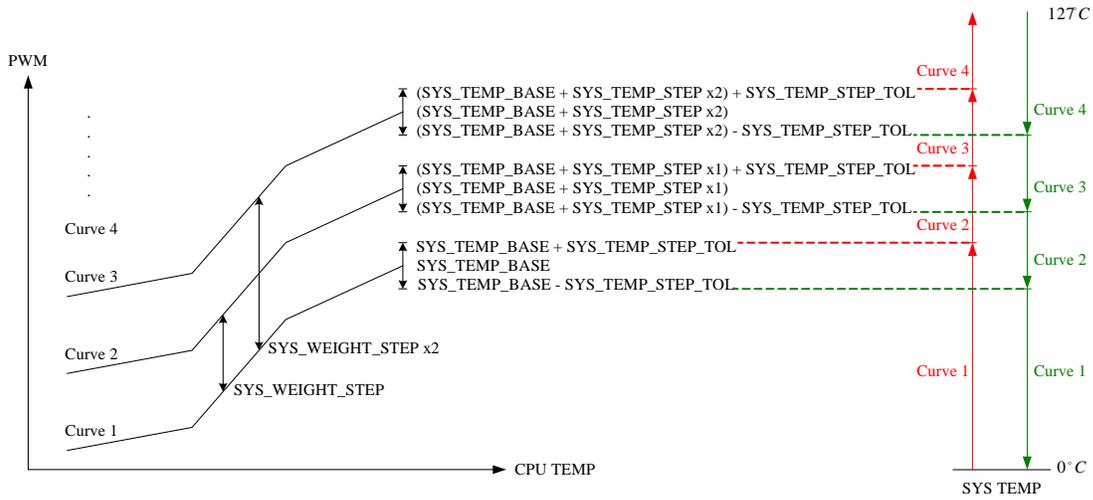


Figure 8-22 Fan out Duty Curves

Table 8-18 Relative Register-at Weight Value Control

DESCRIPTION	TEMP_BASE	TEMP_STEP	TEMP_STEP_TOL	WEIGHT_STEP	WEIGHT_SOURCE_SELECT	ENABLE_WEIGHT
SYSFANOUT	Bank C, Index 57h	Bank C, Index 51h	Bank C, Index 5Ah	Bank C, Index 54h	Bank9, Index 50, bit7~5	Bank C, Index50h, bit0
CPUFANOUT	Bank C, Index 58h	Bank C, Index 52h	Bank C, Index 5Bh	Bank C, Index 55h	BankA, Index 50, bit7~5	Bank C, Index50h, bit1
AUXFANOUT	Bank C, Index 59h	Bank C, Index 53h	Bank C, Index 5Ch	Bank C, Index 56h	BankB, Index 50, bit7~5	Bank C, Index50h, bit2

## 8.6 Interrupt Detection

### 8.6.1 SMI# Interrupt Mode

The SMI#/OVT# pin (pin 128) is a multi-function pin. It can be in HM\_SMI# mode or in OVT# mode by setting Configuration Register CR[29h], bit 6 to one or zero, respectively. In HM\_SMI# mode, it can monitor voltages, fan counts, or temperatures.

#### 8.6.1.1. Voltage SMI# Mode

The SMI# pin can create an interrupt if a voltage exceeds a specified high limit or falls below a specified low limit. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the following figure.

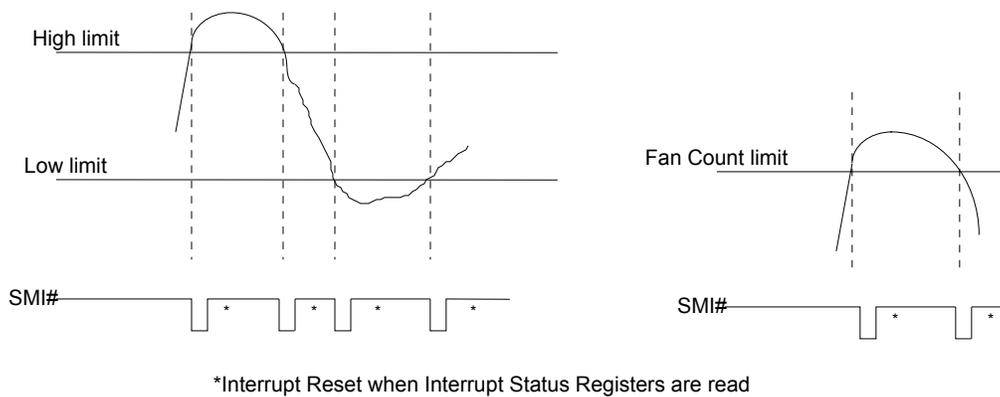


Figure 8-23 SMI Mode of Voltage and Fan Inputs

#### 8.6.1.2. Fan SMI# Mode

The SMI# pin can create an interrupt if a fan count crosses a specified fan limit (rises above it or falls below it). This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the figure above.

### 8.6.1.3. Temperature SMI# Mode

The SMI# pin can create interrupts that depend on the temperatures measured by SYSTIN, CPUTIN, and AUXTIN. These interrupts are divided into two parts, one for SYSTIN and the other for CPUTIN / AUXTIN.

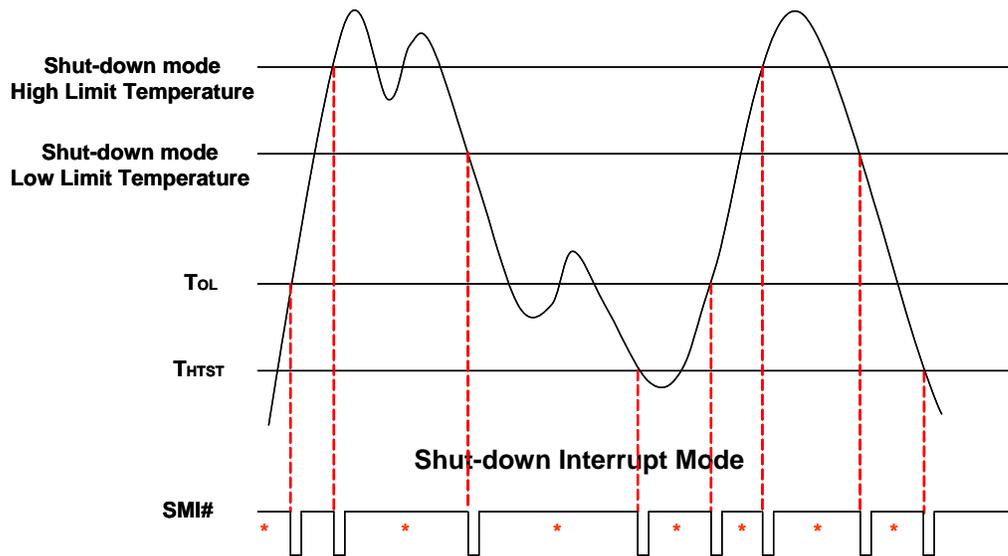
#### 8.7.1.3.1. Temperature Sensor 1(SYSTIN) SMI# Interrupt

The SMI# pin has three interrupt modes with SYSTIN.

##### (1) Shut-down Interrupt Mode

This mode is enabled by setting  $T_{HYST}$  (Temperature Hysteresis) lower than  $T_{OL}$  and setting Bank0 Index 40h, bit 4 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above  $T_{OL}$  or Shut-down mode high limit temperature, and when the current temperature falls below  $T_{HYST}$  or Shut-down mode low limit temperature. Once the temperature rises above  $T_{OL}$ , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above  $T_{OL}$ , until the temperature falls below  $T_{HYST}$ . This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.



\* Interrupt Reset when Interrupt Status Registers are read

##### (2) Comparator Interrupt Mode

This mode is enabled by setting  $T_{HYST}$  (Temperature Hysteresis) to 127°C.

In this mode, the SMI# pin can create an interrupt as long as the current temperature exceeds  $T_O$  (Over Temperature). This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. If the interrupt is reset, the SMI# pin continues to create interrupts until the temperature goes below  $T_O$ . This is illustrated in the figure below.

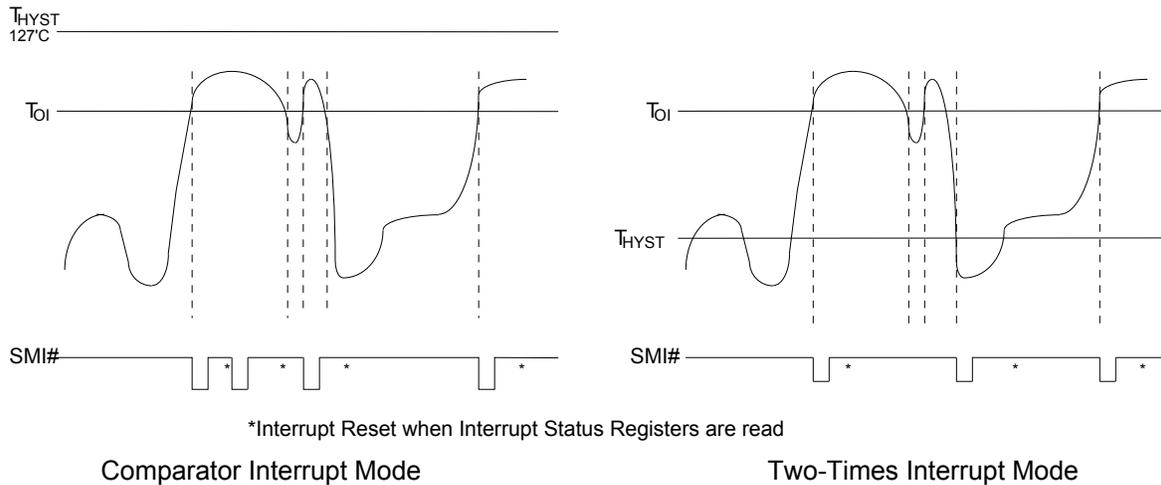


Figure 8-24 SMI Mode of SYSTIN I

### (3) Two-Times Interrupt Mode

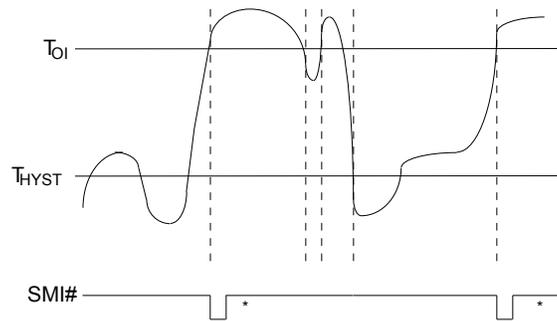
This mode is enabled by setting  $T_{HYST}$  (Temperature Hysteresis) lower than  $T_O$  and setting Bank0 Index 4Ch, bit 5 to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above  $T_O$  or when the current temperature falls below  $T_{HYST}$ . Once the temperature rises above  $T_O$ , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above  $T_O$ , until the temperature falls below  $T_{HYST}$ . This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

### (4) One-Time Interrupt Mode

This mode is enabled by setting  $T_{HYST}$  (Temperature Hysteresis) lower than  $T_O$  and setting Bank0 Index 4Ch, bit 5 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above  $T_O$ . Once the temperature rises above  $T_O$ , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above  $T_O$ , until the temperature falls below  $T_{HYST}$ . This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the following figure.



\*Interrupt Reset when Interrupt Status Registers are read

One-Time Interrupt Mode

Figure 8-25 SMI Mode of SYSTIN II

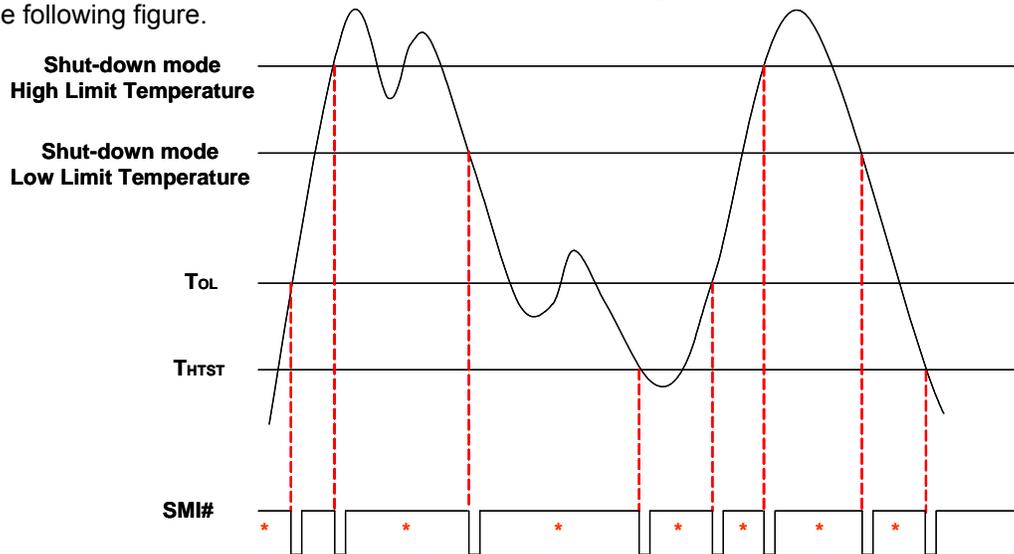
8.7.1.3.2. Temperature Sensor 2(CPUTIN) And Sensor 3(AUXTIN) SMI# Interrupt

The SMI# pin has two interrupt modes with CPUTIN / AUXTIN.

(1) Shut-down Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6 to zero and Bank0 Index 40h, bit 6-5 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above  $T_{OL}$  or Shut-down mode high limit temperature, and when the current temperature falls below  $T_{HYST}$  or Shut-down mode low limit temperature. Once the temperature rises above  $T_{OL}$ , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above  $T_{OL}$ , until the temperature falls below  $T_{HYST}$ . This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.



\* Interrupt Reset when Interrupt Status Registers are read  
Shut-down Interrupt Mode

## (2) Comparator Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to one.

In this mode, the SMI# pin can create an interrupt when the current temperature exceeds  $T_O$  (Over Temperature) and continues to create interrupts until the temperature falls below  $T_{HYST}$ . This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure below.

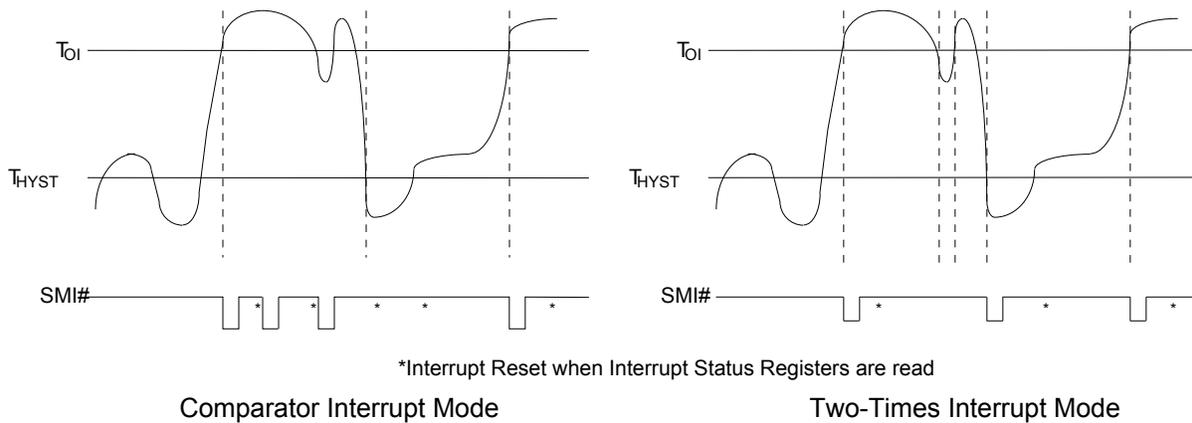


Figure 8-26 SMI Mode of CPUTIN

## (3) Two-Times Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above  $T_O$  or when the current temperature falls below  $T_{HYST}$ . Once the temperature rises above  $T_O$ , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above  $T_O$ , until the temperature falls below  $T_{HYST}$ . This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

### 8.6.2 OVT# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR[29h], bit 6 to one or zero, respectively. In OVT# mode, it can monitor temperatures, and it is enabled or disabled for SYSTIN, CPUTIN, and AUX TIN by Bank0 Index 18h, bit 6; Bank1 Index 52h, bit 1; and Bank2 Index 52h, bit1.

The OVT# pin has two interrupt modes, comparator and interrupt. The modes are illustrated in this figure.

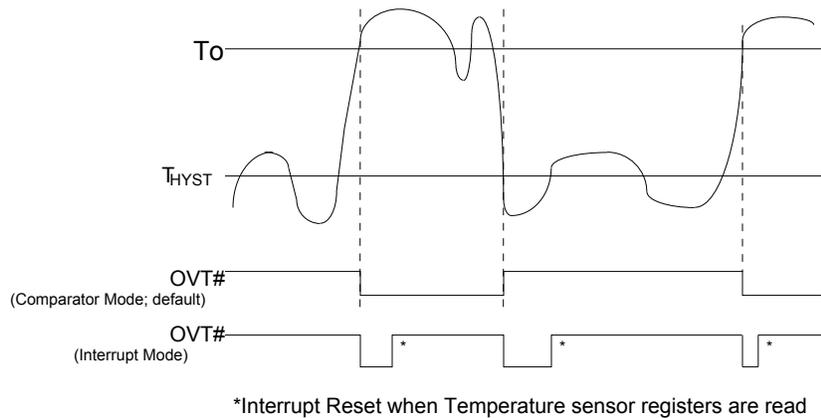


Figure 8-27 OVT# Modes of Temperature Inputs

If Bank0 Index 18h, bit 6, is set to zero, the OVT# pin is in comparator mode. In comparator mode, the OVT# pin can create an interrupt once the current temperature exceeds  $T_O$  and continues to create interrupts until the temperature falls below  $T_{HYST}$ . The OVT# pin is asserted once the temperature has exceeded  $T_O$  and has not yet fallen below  $T_{HYST}$ .

If Bank0 Index 18h, bit 6, is set to one, the OVT# pin is in interrupt mode. In interrupt mode, the OVT# pin can create an interrupt once the current temperature rises above  $T_O$  or when the temperature falls below  $T_{HYST}$ . Once the temperature rises above  $T_O$ , however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above  $T_O$ , until the temperature falls below  $T_{HYST}$ . This interrupt must be reset by reading all the interrupt status registers. The OVT# pin is asserted when an interrupt is generated and remains asserted until the interrupt is reset.

### 8.6.3 Caseopen Detection

The purpose of Caseopen function is used to detect whether the computer case has been opened and possible tampered with. This feature must function even when there is no 3VSB power. Consequently, the power source for the circuit is from either Pin 99 (VBAT) or Pin 85 (3VSB). 3VSB is the default power source. If there is no 3VSB power, the power source is VBAT. This is designed to save power consumption of the battery.

When the case is closed, CASEOPEN# (pin 100) must be pulled high by an externally pulled-up  $2M\Omega$  resistor that is connected to VBAT (pin 99). When the case is opened, CASEOPEN# will be switched from high to low. Meanwhile, the detection circuit inside the IC latches the signal. As a result, the interrupt status and the real-time status can be read at the registers next time when the computer is powered. The status will not be cleared unless CR[46h], bit 7, or CR[E6h] bit 5 at Logical Device A is set to "1" first and then to "0".

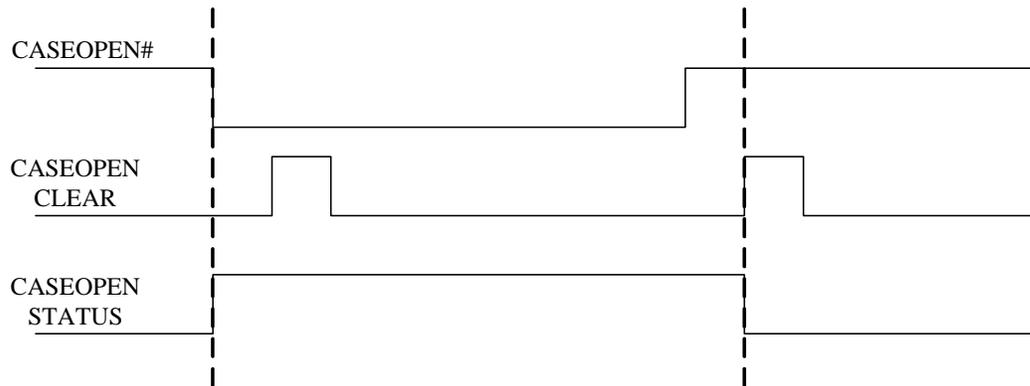


Figure 8-28 Caseopen Mechanism

#### 8.6.4 BEEP Alarm Function

The W83667HG-A provides an alarm output function at the BEEP/SO pin. The BEEP/SO pin is a multi-function pin and can be configured as BEEP output, if Configuration Register CR[24h], bit 1 is set to zero.

The BEEP outputs a warning tone when one of the monitored parameters in the following events is out of the preset range.

- Any voltage input of the nine pins (CPUVCORE, VIN[0..3], 3VCC, AVCC, 3VSB and VBAT) is out of the allowed range;
- Any temperature input of the three pins (SYSTIN, CPUTIN and AUXTIN) exceeds the limit;
- Any fan input of the five pins (SYSFANIN, CPUFANIN, AUXFANIN, AUXFANIN1 and AUXFANIN2) exceeds the limit;
- CASEOPEN# input pin is sampled low;
- User-defined bit (Bank 4, Index 53h, bit 5) is written to 1.

The BEEP alarm function is enabled or disabled by the control bit at Hardware Monitor Device, Bank 0, Index 57h, bit 7. Also, each event has their individual enable bit at Hardware Monitor Device, Bank 0, Index 56h bit[7:0], Index 57h bit[6:0] and Bank 4, Index 53h, bit[1:0].

BEEP/SO is an open-drain output pin and its default state is low. When the BEEP alarm function is activated, this pin repeatedly outputs 600 Hz square wave for 0.5 second and 1.2 KHz square wave for 0.5 second in turn until the enable bit or the abnormal event is cleared.

## 9. HARDWARE MONITOR REGISTER SET

The base address of the Address Port and Data Port is specified in registers CR[60h] and CR[61h] of Logical Device B, the hardware monitor device. CR[60h] is the high byte, and CR[61h] is the low byte. The Address Port and Data Port are located at the base address, plus 5h and 6h, respectively. For example, if CR[60h] is 02h and CR[61h] is 90h, the Address Port is at 0x295h, and the Data Port is at 0x296h.

Remember that this access is from the host CPU I/O address range. To conserve space in the crowded CPU I/O addresses, many of the hardware monitor registers are “banked” with the bank number located at index 04Eh. Indexes from 000h to 04Fh are “global” or accessible from all banks, while indexes 050h to 0FFh are specific to each bank.

### 9.1 Address Port (Port x5h)

Attribute: Bit 6:0 Read/Write , Bit 7: Reserved

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	RESERVED.
6-0	READ/WRITE.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved (Power On default 0)	Address Pointer (Power On default 00h)						
	A6	A5	A4	A3	A2	A1	A0

### 9.2 Data Port (Port x6h)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Data to be read from or to be written to Value RAM and Register.

### 9.3 SYSFANOUT PWM Output Frequency Configuration Register - Index 00h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL1	PWM_SCALE1						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when SYSFANOUT is programmed for PWM output (i.e., Bank0, Index 04h, bit 0 is 0).

BIT	DESCRIPTION
7	<b>PWM_CLK_SEL1. SYSFANOUT PWM Input Clock Source Select.</b> This bit selects the clock source for PWM output frequency. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	<b>PWM_SCALE1. SYSFANOUT PWM Pre-Scale divider.</b> The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. $\text{PWM output frequency} = \frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should not be set to 0.

### 9.4 SYSFANOUT Output Value Select Register - Index 01h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index 04h, bit 0 is 0)	<b>DESCRIPTION</b>	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index 04h, bit 0 is 1)	<b>DESCRIPTION</b>	SYSFANOUT voltage control. The output voltage is calculated according to this equation. $\text{OUTPUT Voltage} = V_{REF} * \frac{\text{FANOUT}}{64}$ Note. VREF is approx 2.048V.						Reserved	

**9.5 CPUFANOUT PWM Output Frequency Configuration Register - Index 02h (Bank 0)**

Attribute: Read/Write  
 Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL2	PWM_SCALE2						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when CPUFANOUT is programmed for PWM output.

BIT	DESCRIPTION
7	<b>PWM_CLK_SEL2. CPUFANOUT PWM Input Clock Source Select.</b> This bit selects the clock source for the PWM output. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	<b>PWM_SCALE2. CPUFANOUT PWM Pre-Scale divider.</b> The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. $\text{PWM output frequency} = \frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should not be set to 0.

**9.6 CPUFANOUT Output Value Select Register - Index 03h (Bank 0)**

Attribute: Read/Write  
 Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value							
DEFAULT	Strap by FAN_SET (Pin34)							

FUNCTION MODE		7	6	5	4	3	2	1	0	
PWM Output (Bank0, Index 04h, bit 1 is 0)	<b>DESCRIPTION</b>	CPUFANOUT PWM Duty. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and creates a duty cycle of 0%.								
DC Voltage Output (Bank0, Index 04h, bit 1 is 1)	<b>DESCRIPTION</b>	CPUFANOUT Voltage Control. The output voltage is calculated according to this equation: $\text{OUTPUT Voltage} = V_{REF} * \frac{\text{FANOUT}}{64}$ Note. VREF is approx 2.048V.						Reserved		

### 9.7 FAN Configuration Register I - Index 04h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		CPUFANOUT_Mode		SYSFANOUT_Mode		CPUFANOUT_SEL	SYSFANOUT_SEL
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-6	Reserved.
5-4	<b>CPUFANOUT_MODE. CPUFANOUT Mode Control.</b> 00: CPUFANOUT is in Manual Mode. 01: CPUFANOUT is in Thermal Cruise Mode. (Default) 10: CPUFANOUT is in Fan Speed Cruise Mode. 11: CPUFANOUT is in SMART FAN <sup>TM</sup> III Mode.
3-2	<b>SYSFANOUT_MODE. SYSFANOUT Mode Control.</b> 00: SYSFANOUT is in Manual Mode. (Default) 01: SYSFANOUT is in Thermal Cruise Mode. 10: SYSFANOUT is as Fan Speed Cruise Mode. 11: SYSFANOUT is in SMART FAN <sup>TM</sup> III Mode.
1	<b>CPUFANOUT_SEL. CPUFANOUT Output Mode Selection.</b> 0: CPUFANOUT pin produces a PWM output duty cycle. (Default) 1: CPUFANOUT pin produces DC output.
0	<b>SYSFANOUT_SEL. SYSFANOUT Output Mode Selection.</b> 0: SYSFANOUT pin produces a PWM duty cycle output. 1: SYSFANOUT pin produces DC output. (Default)

### 9.8 SYSTIN Target Temperature Register/ SYSFANIN Target Speed Register - Index 05h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	SYSTIN Target Temperature / SYSFANIN Target Speed						
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise <sup>TM</sup>	DESCRIPTION	Reserved	SYSTIN Target Temperature						
Fan Speed Cruise <sup>TM</sup>	DESCRIPTION	SYSFANIN Target Speed							

### 9.9 CPUTIN Target Temperature Register/ CPUFANIN Target Speed Register - Index 06h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN Target Temperature / CPUFANIN Target Speed							
DEFAULT	0	0	1	1	0	0	1	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™ or SMART FAN™ III	DESCRIPTION	Reserved	CPUTIN Target Temperature						
Fan Speed Cruise™	DESCRIPTION	CPUFANIN Target Speed							

### 9.10 Tolerance of Target Temperature or Target Speed Register - Index 07h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Tolerance of Target Temperature or Target Speed							
DEFAULT	0	0	1	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™ or SMART FAN™ III	DESCRIPTION	Tolerance of CPUTIN Target Temperature				Tolerance of SYSTIN Target Temperature			
Fan Speed Cruise™	DESCRIPTION	Tolerance of CPUFANIN Target Speed.				Tolerance of SYSFANIN Target Speed.			

### 9.11 SYSFANOUT Stop Value Register - Index 08h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the SYSFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

### 9.12 CPUFANOUT Stop Value Register - Index 09h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Value							
DEFAULT	1	0	0	0	0	0	0	0

In Thermal Cruise mode or SMART FAN™ III mode, the CPUFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

### 9.13 SYSFANOUT Start-up Value Register - Index 0Ah (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, SYSFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

### 9.14 CPUFANOUT Start-up Value Register - Index 0Bh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, CPUFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

### 9.15 SYSFANOUT Stop Time Register - Index 0Ch (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, if the stop value is enabled, this register determines the amount of time it takes the SYSFANOUT value to fall from the stop value to zero.

(1)For PWM output:

The units are intervals of 0.1 seconds. The default time is 6 seconds.

(2)For DC output:

The units are intervals of 0.4 seconds. The default time is 24 seconds.

### 9.16 CPUFANOUT Stop Time Register - Index 0Dh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode or SMART FAN™ III mode, this register determines the amount of time it takes the CPUFANOUT value to fall from the stop value to zero.

(1)For PWM output:

The units are intervals of 0.1 seconds. The default time is 6 seconds.

(2)For DC output:

The units are intervals of 0.4 seconds. The default time is 24 seconds.

### 9.17 SYSFANOUT Step Down Time Register - Index 0Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to decrease its value by one step.

(1)For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2)For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

### 9.18 SYSFANOUT Step Up Time Register - Index 0Fh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to increase its value by one step.

(1)For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2)For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

### 9.19 AUXFANOUT PWM Output Frequency Configuration Register - Index 10h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL3	PWM_SCALE3						
DEFAULT	0	0	0	0	0	1	0	0

This register is only meaningful when AUXFANOUT is programmed for PWM output (i.e. Bank0, Index 12h, bit 0 is 0)

BIT	DESCRIPTION
7	<b>PWM_CLK_SEL3. AUXFANOUT PWM Input Clock Source Select.</b> This bit selects the clock source of PWM output frequency. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	<b>PWM_CLK_SCALE3. AUXFANOUT PWM Pre-Scale divider.</b> The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency.  $\text{PWM output frequency} = \frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should not be set to 0.

### 9.20 AUXFANOUT Output Value Select Register - Index 11h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index 12h, bit 0 is 0)	<b>DESCRIPTION</b>	AUXFANOUT PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Output (Bank0, Index 12h, bit 0 is 1)	<b>DESCRIPTION</b>	AUXFANOUT voltage control. The output voltage is calculated according to this equation:  <b>OUTPUT Voltage = <math>V_{REF} * \frac{FANOUT}{64}</math></b>  Note. VREF is approx 2.048V.						Reserved	

### 9.21 FAN Configuration Register II - Index 12h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	RESERVED	SYSFANOUT _MIN_VALUE	CPUFANOUT _MIN_VALUE	AUXFANOUT _MIN_VALUE	AUXFANOUT _MODE	AUXFANOUT _MODE	AUXFANOUT_SEL	
<b>DEFAULT</b>	0	0	0	1	0	0	0	0

BIT	DESCRIPTION
7-6	<b>Reserved.</b>
5	<b>SYSFANOUT_MIN_Value.</b> 0: SYSFANOUT value decreases to zero when the temperature goes below the target range. 1: SYSFANOUT value decreases to the value specified in Index 08h when the temperature goes below the target range.
4	<b>CPUFANOUT_MIN_Value.</b> 0: CPUFANOUT value decreases to zero when the temperature goes below the target range. 1: CPUFANOUT value decreases to the value specified in Index 09h when the temperature goes below the target range.
3	<b>AUXFANOUT_MIN_Value.</b> 0: AUXFANOUT value decreases to zero when the temperature goes below the target range. 1: AUXFANOUT value decreases to the value specified in Index 17h when the temperature goes below the target range.
2-1	<b>AUXFANOUT_Mode. AUXFANOUT Mode Control.</b> 00: AUXFANOUT is in Manual Mode. (Default). 01: AUXFANOUT is in Thermal Cruise Mode. 10: AUXFANOUT is in Fan Speed Cruise Mode. 11: AUXFANOUT is in SMART FAN <sup>TM</sup> III Mode.
0	<b>AUXFANOUT_SEL.</b> 0: AUXFANOUT pin produces a PWM output duty cycle. (Default)

BIT	DESCRIPTION
	1: AUXFANOUT pin produces DC output.

### 9.22 AUXTIN Target Temperature Register/ AUXFANIN Target Speed Register - Index 13h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN Target Temperature / AUXFANIN Target Speed Value							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	Reserved		AUXTIN Target Temperature					
Fan Speed Cruise™	DESCRIPTION	AUXFANIN Target Speed							

### 9.23 Tolerance of Target Temperature or Target Speed Register - Index 14h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Tolerance of Target Temperature or Target Speed Value							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	Reserved				Tolerance of AUXTIN Target Temperature			
Fan Speed Cruise™	DESCRIPTION	Reserved				Tolerance of AUXFANIN Target Speed			

### 9.24 AUXFANOUT Stop Value Register - Index 15h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

### 9.25 AUXFANOUT Start-up Value Register - Index 16h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

### 9.26 AUXFANOUT Stop Time Register - Index 17h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, if the stop value is enabled, this register determines the amount of time it takes the AUXFANOUT value to fall from the stop value to zero.

(1) For PWM output,

The units are intervals of 0.1 second. The default time is 6 seconds.

(2) For DC output,

The units are intervals of 0.4 second. The default time is 24 seconds.

### 9.27 OVT# Configuration Register - Index 18h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	DIS_OVT1	RESERVED	OVT1_Mode	RESERVED			
DEFAULT	0	1	0	0	0	0	1	1

BIT	DESCRIPTION
7	Reserved.
6	<b>DIS_OVT1.</b> 0: Enables SYSTIN OVT# output. (Default) 1: Disable temperature sensor SYSTIN over-temperature (OVT#) output.

BIT	DESCRIPTION
5	Reserved.
4	<b>OVT1_Mode.</b> 0: Compare Mode. (Default) 1: Interrupt Mode.
3-0	Reserved.

### 9.28 Reserved Registers - Index 19h ~ 1Fh (Bank 0)

### 9.29 Value RAM 1 — Index 20h ~ 3Fh (Bank 0)

ADDRESS A6-A0	DESCRIPTION
20h	CPUVCORE reading
21h	VIN0 reading
22h	AVCC reading
23h	3VCC reading
24h	VIN1 reading
25h	VCORE_REFIN reading
26h	VIN2 reading
27h	SYSFAN temperature source reading (High Byte) Note. Low Byte is locate on Bank0, Index 7Ch
28h	SYSFANIN reading Note: This location stores the number of counts of the internal clock per revolution.
29h	CPUFANIN reading Note: This location stores the number of counts of the internal clock per revolution.
2Ah	AUXFANIN reading Note: This location stores the number of counts of the internal clock per revolution.
2Bh	CPUVCORE High Limit
2Ch	CPUVCORE Low Limit
2Dh	VIN0 High Limit
2Eh	VIN0 Low Limit
2Fh	AVCC High Limit
30h	AVCC Low Limit
31h	3VCC High Limit
32h	3VCC Low Limit
33h	VIN1 High Limit
34h	VIN1 Low Limit

ADDRESS A6-A0	DESCRIPTION
35h	VCROE_REFIN High Limit
36h	VCROE_REFIN Low Limit
37h	VIN2 High Limit
38h	VIN2 Low Limit
39h	SYSTIN temperature sensor High Limit
3Ah	SYSTIN temperature sensor Hysteresis Limit (Set this register value to 7Fh will enable SMI# Comparator Interrupt Mode of SYSTIN)
3Bh	SYSFANIN Fan Count Limit <b>Note:</b> It is the number of counts of the internal clock for the Limit of the fan speed.
3Ch	CPUFANIN Fan Count Limit <b>Note:</b> It is the number of counts of the internal clock for the Limit of the fan speed.
3Dh	AUXFANIN Fan Count Limit <b>Note:</b> It is the number of counts of the internal clock for the Limit of the fan speed.
3Eh	AUXFANIN1 Fan Count Limit <b>Note:</b> It is the number of counts of the internal clock for the Limit of the fan speed.
3Fh	AUXFANIN1 reading <b>Note:</b> This location stores the number of counts of the internal clock per revolution.

Note. Value RAM 2 is located in Bank5 Index50-5Fh.

### 9.30 Configuration Register - Index 40h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	INITIALIZATION	EN_WS2	EN_WS1	EN_WS	INT_CLEAR	RESERVED	SMI#ENABLE	START
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	<b>Initialization.</b> A one restores the power-on default values to some registers. This bit clears itself since the power-on default of this bit is zero.
6	<b>EN_WS2.</b> 1: SMI# output type of temperature AUX TIN is Shut-down Interrupt Mode. 0: SMI# output type of AUX TIN is depend on Bank0,CR4C,bit6. (Default)

BIT	DESCRIPTION
5	<b>EN_WS1.</b> 1: SMI# output type of temperature CPUTIN is Shut-down Interrupt Mode. 0: SMI# output type of CPUTIN is depend on Bank0,CR4C,bit6. (Default)
4	<b>EN_WS.</b> 1: SMI# output type of temperature SYSTIN is Shut-down Interrupt Mode. 0: SMI# output type of SYSTIN is depend on Bank0,CR4C,bit5. (Default)
3	<b>INT_Clear.</b> A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
2	<b>Reserved.</b>
1	<b>SMI# Enable.</b> 1: Enable SMI#. 0: Disable SMI#. (Default)
0	<b>Start.</b> A one enables startup of monitoring operations. A zero puts the part in standby mode. <b>Note:</b> Unlike the "INT_Clear" bit, the outputs of interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred.

### 9.31 Interrupt Status Register 1 - Index 41h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	CPUFANIN	SYSFANIN	CPUTIN	SYSTIN	3VCC	AVCC	VIN0	CPUVCORE
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	<b>CPUFANIN.</b> A one indicates the fan count limit of CPUFANIN has been exceeded.
6	<b>SYSFANIN.</b> A one indicates the fan count limit of SYSFANIN has been exceeded.
5	<b>CPUTIN.</b> A one indicates the high limit of CPUTIN temperature has been exceeded.
4	<b>SYSTIN.</b> A one indicates the high limit of SYSTIN temperature has been exceeded.
3	<b>3VCC.</b> A one indicates the high or low limit of 3VCC has been exceeded.
2	<b>AVCC (Pin 106).</b> A one indicates the high or low limit of AVCC has been exceeded.
1	<b>VIN0.</b> A one indicates the high or low limit of VIN0 has been exceeded.
0	<b>CPUVCORE.</b> A one indicates the high or low limit of CPUVCORE has been exceeded.

### 9.32 Interrupt Status Register 2 - Index 42h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	TAR2	TAR1	AUXTIN	CASEOPEN	AUXFANIN	VCROE_REFIN	VIN2	VIN1
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	<b>TAR2.</b> A one indicates that the CPUTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode.
6	<b>TAR1.</b> A one indicates that the SYSTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode.
5	<b>AUXTIN.</b> A one indicates the high limit of AUXTIN temperature has been exceeded.
4	<b>CASEOPEN.</b> A one indicates the case has been opened.
3	<b>AUXFANIN.</b> A one indicates the fan count limit of AUXFANIN has been exceeded.
2	<b>VCROE_REFIN.</b> A one indicates the high or low limit of VCROE_REFIN has been exceeded.
1	<b>VIN2.</b> A one indicates the high or low limit of VIN2 has been exceeded.
0	<b>VIN1.</b> A one indicates the high or low limit of VIN1 has been exceeded.

### 9.33 SMI# Mask Register 1 - Index 43h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	CPUFANIN	SYSFANIN	CPUTIN	SYSTIN	3VCC	AVCC	VIN0	CPUVCORE
<b>DEFAULT</b>	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7	<b>CPUFANIN.</b>
6	<b>SYSFANIN.</b>
5	<b>CPUTIN.</b>
4	<b>SYSTIN.</b>
3	<b>3VCC.</b>
2	<b>AVCC (Pin 106).</b>
1	<b>VIN0.</b>
0	<b>CPUVCORE.</b>
A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 1 – Index 41h (Bank0))	

### 9.34 SMI# Mask Register 2 - Index 44h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	TAR2	TAR1	AUXTIN	CASEOPEN	AUXFANIN	VCROE_REFIN	VIN2	VIN1
<b>DEFAULT</b>	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	TAR2.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 2 - Index 42h (Bank 0))
6	TAR1.	
5	AUXTIN.	
4	CASEOPEN.	
3	AUXFANIN. (Pin97)	
2	VCROE_REFIN.	
1	VIN2.	
0	VIN1.	

### 9.35 Interrupt Status Register 4 - Index 45h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VID	VID(Auto Clear)	AUXFANOUT	CPUFANOUT	SYSFANOUT	Shut_AUX	Shut_CPU	Shut_SYS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	<b>VID.</b> "1" indicates that the VIDI is on the flying.
6	<b>VID (Auto Clear).</b> "1" indicates that the VIDI is on the flying.
5	<b>AUXFANOUT.</b> "1" indicates that AUXFANOUT works for three minutes at the full fan speed.
4	<b>CPUFANOUT.</b> "1" indicates that CPUFANOUT works for three minutes at the full fan speed.
3	<b>SYSFANOUT.</b> "1" indicates that SYSFANOUT works for three minutes at the full fan speed.
2	<b>Shut_AUX.</b> "1" indicates the high limit of AUXTIN temperature of SMI# Shut-down mode has been exceeded.
1	<b>Shut_CPU.</b> "1" indicates the high limit of CPUTIN temperature of SMI# Shut-down mode has been exceeded.
0	<b>Shut_SYS.</b> "1" indicates the high limit of SYSTIN temperature of SMI# Shut-down mode has been exceeded.

### 9.36 SMI# Mask Register 3 - Index 46h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CASEOPEN CLEAR	Reserved.	Shut_AUX	Shut_CPU	Shut_SYS	AUXFANIN2	AUXFANIN1	RESERVED
DEFAULT	0	0	1	1	1	1	1	1

BIT	DESCRIPTION	
7	<b>CASEOPEN Clear Control.</b> Writing 1 to this bit will clear CASEOPEN status. This bit will not be self cleared. Please write 0 after the event is cleared. The function is the same as LDA, CR[E6h], bit 5.	
6	<b>Reserved.</b>	
5	<b>Shut_AUX</b>	"1" disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 4 – Index 45h (Bank 0)).
4	<b>Shut_CPU</b>	
3	<b>Shut_SYS</b>	
2	<b>AUXFANIN2. (Pin95)</b>	"1" disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4)).
1	<b>AUXFANIN1. (Pin96)</b>	
0	<b>Reserved.</b>	

### 9.37 Fan Divisor Register I - Index 47h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>CPUFANIN DIV_B1</b>	<b>CPUFANIN DIV_B0</b>	<b>SYSFANIN DIV_B1</b>	<b>SYSFANIN DV_B0</b>	<b>AUXFANIN1 OPV4</b>	<b>AUXFANIN1 C4</b>	<b>AUXFANIN2 OPV5</b>	<b>AUFANIN2 CV5</b>
<b>DEFAULT</b>	1	1	1	1	0	1	0	1

BIT	DESCRIPTION	
7	<b>CPUFANIN DIV_B1.</b>	CPUFANIN Divisor, bits 1-0. (See VBAT Monitor Control Register – Index 5Dh (Bank 0))
6	<b>CPUFANIN DIV_B0.</b>	
5	<b>SYSFANIN DIV_B1.</b>	SYSFANIN Divisor, bits 1-0. (See VBAT Monitor Register – Index 5Dh (Bank 0))
4	<b>SYSFANIN DIV_B0.</b>	
3	<b>AUXFANIN1OPV4. AUXFANIN1 output value</b> , only if bit 2 is set to zero. Otherwise, this bit has no meaning. 1: Pin 96 (AUXFANIN1) generates a logic-high signal. 0: Pin 96 generates a logic-low signal (Default).	
2	<b>AUXFANIN1C4. AUXFANIN1 Input Control.</b> 1: Pin 96 (AUXFANIN1) acts as a fan tachometer input. (Default) 0: Pin 96 acts as a fan control signal, and the output value is set by register bit 3.	
1	<b>AUXFANIN2OPV5. AUXFANIN2 output value</b> , only if bit 0 is set to zero. Otherwise, this bit has no meaning. 1: Pin 95 (AUXFANIN2) generates a logic-high signal. 0: Pin 95 generates a logic-low signal. (Default)	
0	<b>AUXFANIN2C5. AUXFANIN2 Input Control.</b>	

BIT	DESCRIPTION
	1: Pin 95 (AUXFANIN2) acts as a fan tachometer input. (Default) 0: Pin 95 acts as a fan control signal, and the output value is set by bit 1.

### 9.38 Serial Bus Address Register - Index 48h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	SERIAL BUS ADDRESS						
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7	Reserved (Read Only).
6-0	Serial Bus Address <7:1>

### 9.39 CPUFAN/AUXFAN monitor Temperature source select register - Index 49h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	AUXFAN SOURCE SEL[2]	AUXFAN SOURCE SEL[1]	AUXFAN SOURCE SEL[0]	RESERVED	CPUFAN SOURCE SEL[2]	CPUFAN SOURCE SEL[1]	CPUFAN SOURCE SEL[0]
DEFAULT	0	0	1	0	0	0	0	1

BIT	DESCRIPTION
7	Reserved.
6	AUXFAN SOURCE SEL[2]. AUXFAN Control Referred Temperature Source Select. (The selected temp source data will store in Bank2, Index50h.) Bits 6 5 4 0 0 0: Select SYSTIN
5	AUXFAN SOURCE SEL [1]. 0 0 1: Select CPUTIN 0 1 0: Select AUXTIN (Default) 0 1 1: Select AMDTSI

BIT	DESCRIPTION	
4	<b>AUXFAN SOURCE SEL [0].</b>	1 0 0: Select PECI Agent 1 1 0 1: Select PECI Agent 2 1 1 0: Select PECI Agent 3 1 1 1: Select PECI Agent 4
3	<b>Reserved.</b>	
2	<b>CPUFAN SOURCE SEL [2].</b>	<a href="#">CPUFAN Control Referred Temperature Source Select.</a> <a href="#">(The selected temp source data will store in Bank1, Index50h.)</a> <b>Bits</b> <b>2 1 0</b> 0 0 0: Select SYSTIN
1	<b>CPUFAN SOURCE SEL [1].</b>	0 0 1: Select CPUTIN <b>(Default)</b> 0 1 0: Select AUCTIN 0 1 1: Select AMDTSI
0	<b>CPUFAN SOURCE SEL [0].</b>	1 0 0: Select PECI Agent 1 1 0 1: Select PECI Agent 2 1 1 0: Select PECI Agent 3 1 1 1: Select PECI Agent 4

#### 9.40 SYSFAN Monitor Temperature Source Select Register - Index 4Ah (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	SYSFAN SOURCE SEL[2]	SYSFAN SOURCE SEL[2]	SYSFAN SOURCE SEL[2]	<b>RESERVED</b>				
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
-----	-------------

BIT	DESCRIPTION	
7	<b>SYSFAN SOURCE SEL [2].</b>	SYSFAN Control Referred Temperature Source Select. (The selected temp source data will store in Bank0, Index27h.) <b>Bits</b> <b>7 6 5</b> 0 0 0: Select SYSTIN ( <b>Default</b> )
6	<b>SYSFAN SOURCE SEL [1].</b>	0 0 1: Select CPUTIN 0 1 0: Select AUCTIN 0 1 1: Select AMDTSI
5	<b>SYSFAN SOURCE SEL [0].</b>	1 0 0: Select PECl Agent 1 1 0 1: Select PECl Agent 2 1 1 0: Select PECl Agent 3 1 1 1: Select PECl Agent 4
4-0	<b>Reserved.</b>	

#### 9.41 Fan Divisor Register II - Index 4Bh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>AUXFANIN DIV_B1</b>	<b>AUXFANIN DIV_B0</b>	<b>ADCOVSEL</b>		<b>RESERVED</b>			
<b>DEFAULT</b>	1	1	0	0	0	1	0	0

BIT	DESCRIPTION	
7	<b>AUXFANIN DIV_B1.</b>	AUXFANIN Divisor, bits 1-0. (Please see Bank 0, Index 5Dh, Fan Divisor Table)
6	<b>AUXFANIN DIV_B0.</b>	
5-4	<b>ADCOVSEL. A/D Converter Clock Input Select.</b> <b>Bits</b> <b>5 4</b> 0 0: ADC clock select 22.5 KHz. (Default) 0 1: ADC clock select 5.6 KHz. (22.5K/4) 1 0: ADC clock select 1.4 KHz. (22.5K/16) 1 1: ADC clock select 0.35 KHz. (22.5K/64)	
3-2	<b>Reserved.</b> These two bits should be set to 01h, the default value.	
1-0	<b>Reserved.</b>	

#### 9.42 SMI#/OVT# Control Register - Index 4Ch (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 DIV_B2	T2T3_INT MODE	EN_T1 _ONE	DIS_ OVT3	DIS_ OVT2	OVTPOL	RESERVED	
DEFAULT	0	0	0	1	1	0	0	0

BIT	DESCRIPTION
7	<b>AUXFANIN1 DIV_B2.</b>
6	<b>T2T3_INTMode.</b> 1: SMI# output type of Temperature CPUTIN / AUX TIN is in Comparator Interrupt mode. 0: SMI# output type is in Two-Times Interrupt mode. (Default) <i>Note. Set Bank0, Index 40h, bit6~5 to 0 if comparator or two-times interrupt mode is in use</i>
5	<b>EN_T1_ONE.</b> 1: SMI# output type of temperature SYSTIN is One-Time Interrupt Mode. 0: SMI# output type is in Two-Times Interrupt Mode. (Default) <i>Note. Set Bank0, Index 40h, bit4 to 0 if comparator or two-times interrupt mode is in use.</i>
4	<b>DIS_OVT3.</b> 1: Disable temperature sensor AUX TIN over-temperature (OVT) output. (Default) 0: Enable AUX TIN OVT output through pin OVT#.
3	<b>DIS_OVT2.</b> 1: Disable temperature sensor CPUTIN over-temperature (OVT) output. (Default) 0: Enable CPUTIN OVT output through pin OVT#.
2	<b>OVT POL (Over-temperature polarity).</b> 1: OVT# is active high. 0: OVT# is active low (Default).
1-0	<b>Reserved.</b>

#### 9.43 FAN IN/OUT Control Register - Index 4Dh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		FANOPV3	FANINC3	FANOPV2	FANINC2	FANOPV1	FANINC1
DEFAULT	1	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-6	<b>Reserved.</b>
5	<b>FANOPV3. AUXFANIN output value,</b> only if bit 4 is set to zero. 1: Pin 97 (AUXFANIN) generates a logic-high signal. 0: Pin 97 generates a logic-low signal. (Default)
4	<b>FANINC3. AUXFANIN Input Control.</b>

BIT	DESCRIPTION
	1: Pin 97 (AUXFANIN) acts as a fan tachometer input. (Default) 0: Pin 97 acts as a fan control signal, and the output value is set by bit 5.
3	<b>FANOPV2. CPUFANIN output value</b> , only if bit 2 is set to zero. 1: Pin 124 (CPUFANIN) generates a logic-high signal. 0: Pin 124 generates a logic-low signal. (Default)
2	<b>FANINC2. CPUFANIN Input Control</b> . 1: Pin 124 (CPUFANIN) acts as a fan tachometer input. (Default) 0: Pin 124 acts as a fan control signal, and the output value is set by bit 3.
1	<b>FANOPV1. SYSFANIN output value</b> , only if bit 0 is set to zero. 1: Pin 126 (SYSFANIN) generates a logic-high signal. 0: Pin 126 generates a logic-low signal. (Default)
0	<b>FANINC1. SYSFANIN Input Control</b> . 1: Pin 126 (SYSFANIN) acts as a fan tachometer input. (Default) 0: Pin 126 acts as a fan control signal, and the output value is set by bit 1.

#### 9.44 Register 50h ~ 5Fh Bank Select Register - Index 4Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	RESERVED	EN_AUXFANIN1_BP	EN_AUXFANIN1_BP	RESERVED	BANK SEL2	BANK SEL1	BANK SEL0
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	<b>HBACS. HBACS – High Byte Access</b> . 1: Access Index 4Fh high-byte register. (Default) 0: Access Index 4Fh low-byte register.
6	<b>Reserved</b> . This bit should be set to zero.
5	<b>EN_AUXFANIN1_BP. BEEP Output Control for AUXFANIN2</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
4	<b>EN_AUXFANIN1_BP. BEEP output control for AUXFANIN1</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output.
3	<b>Reserved</b> . This bit should be set to zero.
2	<b>BANKSEL2</b> .
1	<b>BANKSEL1</b> .
0	<b>BANKSEL0</b> .
Bank Select for Index Ports 0x50h~0x5Fh. The three-bit binary value corresponds to the bank number. For example, "010" selects bank2.	

#### 9.45 Nuvoton Vendor ID Register - Index 4Fh (Bank 0)

Attribute: Read Only

Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDL							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDH							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	<b>Vendor ID High-Byte</b> , if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	<b>Vendor ID Low-Byte</b> , if Index 4Eh, bit 7 is 0. Default A3h.

#### 9.46 Reserved Register - Index 50h ~ 55h (Bank 0)

#### 9.47 BEEP Control Register 1 - Index 56h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_CPUFANIN_BP	EN_SYSFANIN_BP	EN_CPUTIN_BP	EN_SYSTIN_BP	EN_3VCC_BP	EN_AVCC_BP	EN_VIN0_BP	EN_CPUVCORE_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	<b>EN_CPUFANIN_BP. BEEP output control for CPUFANIN</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
6	<b>EN_SYSFANIN_BP. BEEP output control for SYSFANIN</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
5	<b>EN_CPUTIN_BP. BEEP output control for temperature CPUTIN</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
4	<b>EN_SYSTIN_BP. BEEP output control for temperature SYSTIN</b> if the monitored value

BIT	DESCRIPTION
	exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
3	<b>EN_3VCC_BP. BEEP output control for 3VCC</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
2	<b>EN_AVCC_BP. BEEP output control for AVCC</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
1	<b>EN_VIN0_BP. BEEP output control for VIN0</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
0	<b>EN_CPUVCORE_BP. BEEP output control for CPUVCORE</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)

#### 9.48 BEEP Control Register 2 - Index 57h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_ GBP	Reserved	EN_ AUXTIN _BP	EN_ CASEOPEN _BP	EN_ AUXFANIN _BP	EN_ VIN2 _BP	EN_ VCROE_REFIN _BP	EN_ VIN1 _BP
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	<b>EN_GBP. Global BEEP Control.</b> 1: Enable global BEEP output. (Default) 0: Disable all BEEP output.
6	<b>Reserved</b>
5	<b>EN_AUXTIN_BP. BEEP output control for temperature AUXTIN</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
4	<b>EN_CASEOPEN_BP. BEEP output control for CASEOPEN</b> if the case has been opened. 1: Enable BEEP output. 0: Disable BEEP output. (Default)

BIT	DESCRIPTION
3	<b>EN_AUXFANIN_BP. BEEP output control for AUXFANIN</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
2	<b>EN_VIN2_B. BEEP output control for VIN2</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
1	<b>EN_VCROE_REFIN_BP. BEEP output control for VCROE_REFIN</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
0	<b>EN_VIN1_BP. BEEP output control for VIN1</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)

#### 9.49 Chip ID - Index 58h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CHIPID							
DEFAULT	1	1	0	0	0	0	0	1

BIT	DESCRIPTION
7-0	Nuvoton Chip ID number. Default C1h.

#### 9.50 Fan Divisor Selection Register - Index 59h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 DIV_B2	RESERVED			AUXFANIN2 DIV_B1	AUXFANIN2 DIV_B0	AUXFANIN1 DIV_B1	AUXFANIN1 DIV_B0
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7	<b>AUXFANIN2 DIV_B2 (AUXFANIN2 Divisor bit 2).</b> (See VBAT Monitor Control Register – Index 5Dh (Bank 0))

BIT	DESCRIPTION	
6	Reserved.	
5	Reserved.	
4	Reserved.	
3	AUXFANIN2 DIV_B1.	AUXFANIN2 Divisor, bits 1-0. (See VBAT Monitor Control Register – Index 5Dh (Bank 0))
2	AUXFANIN2 DIV_B0.	
1	AUXFANIN1 DIV_B1.	AUXFANIN1 Divisor, bits 1-0. (See VBAT Monitor Control Register – Index 5Dh (Bank 0))
0	AUXFANIN1 DIV_B0.	

### 9.51 Reserved Register - Index 5Ah ~ 5Ch (Bank 0)

### 9.52 Sensor Type Select and VBAT Monitor Control Register - Index 5Dh (Bank 0)

Attribute: Read/Write  
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN DIV_B2	CPUFANIN DIV_B2	SYSFANIN0 DIV_B2	RESERVED	DIODES3	DIODES2	DIODES1	EN_VBAT_MNT
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION							
7	AUXFANIN DIV_B2. AUXFANIN Divisor bit 2.							
6	CPUFANIN DIV_B2. CPUFANIN Divisor bit 2.							
5	SYSFANIN DIV_B2. SYSFANIN Divisor bit 2.							
	BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
	0	0	0	1	1	0	0	16
	0	0	1	2	1	0	1	32
	0	1	0	4	1	1	0	64
0	1	1	8	1	1	1	128	
4	Reserved.							
3	DIODES 3. Sensor type selection for AUX TIN. 1: Diode sensor. 0: Thermistor sensor. (Default)							
2	DIODES 2. Sensor type selection for CPU TIN. 1: Diode sensor. (Default) 0: Thermistor sensor.							
1	DIODES 1. Sensor type selection for SYS TIN.							

BIT	DESCRIPTION
	1: Diode sensor. 0: Thermistor sensor. (Default)
0	<b>EN_VBAT_MNT.</b> 1: Enable battery voltage monitor. When this bit changes from zero to one, it takes one monitor cycle time to update the VBAT reading value register. 0: Disable battery voltage monitor. (Default)

### 9.53 Current Mode Enable Register - Index 5Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				EN_AUXTIN CURRENT MODE	EN_CPUTIN CURRENT MODE	EN_SYSTIN CURRENT MODE	RESERVED
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7-4	Reserved.
3	<b>EN_AUXTIN CURRENT MODE. (When to enable the current mode, please also set Bank0, Index 5Dh, Bit 3 to '1')</b> 1: Temperature sensing of AUXTIN by Current Mode. 0: Temperature sensing of AUXTIN depends on the setting of Index 5Dh.(Default)
2	<b>EN_CPUTIN CURRENT MODE. (When to enable the current mode, please also set Bank0, Index 5Dh, Bit 2 to '1')</b> 1: Temperature sensing of CPUTIN by Current Mode. (Default) 0: Temperature sensing of CPUTIN depends on the setting of Index 5Dh.
1	<b>EN_SYSTIN CURRENT MODE. (When to enable the current mode, please also set Bank0, Index 5Dh, Bit 1 to '1')</b> 1: Temperature sensing of SYSTIN by Current Mode. 0: Temperature sensing of SYSTIN depends on the setting of Index 5Dh. (Default)
0	Reserved.

### 9.54 Reserved Register - Index 5F ~ 66h (Bank 0)

### 9.55 SYSFANOUT Maximum Output Value Register - Index 67h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Max. Value							
DEFAULT	1	1	1	1	1	1	1	1

In SMART FAN™ III mode, the SYSFANOUT value increases till this value. This value cannot be zero, and it cannot be lower than the SYSFANOUT Stop value.

### 9.56 SYSFANOUT Output Step Value Register - Index 68h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Step							
DEFAULT	0	0	0	0	0	0	0	1

In SMART FAN™ III mode, the SYSFANOUT value decreases or increases by this eight-bit value, when needed.

### 9.57 CPUFANOUT Maximum Output Value Register - Index 69h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Max. Value							
DEFAULT	1	1	1	1	1	1	1	1

In SMART FAN™ III mode, the CPUFANOUT value increases till this value. This value cannot be zero, and it cannot be lower than the CPUFANOUT Stop value.

### 9.58 CPUFANOUT Output Step Value Register - Index 6Ah (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CUPFANOUT Step							
DEFAULT	0	0	0	0	0	0	0	1

In SMART FAN™ III mode, the CPUFANOUT value decreases or increases by this eight-bit value, when needed.

### 9.59 AUXFANOUT Maximum Output Value Register - Index 6Bh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Max. Value							
DEFAULT	1	1	1	1	1	1	1	1

In SMART FAN™ III mode, the AUXFANOUT value increases till this value. This value cannot be zero, and it cannot be lower than the AUXFANOUT Stop value.

### 9.60 AUXFANOUT Output Step Value Register - Index 6Ch (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Step							
DEFAULT	0	0	0	0	0	0	0	1

In SMART FAN™ III mode, the AUXFANOUT value decreases or increases by this eight-bit value, when needed.

### 9.61 Reserved register - Index 6Dh ~ 6Fh (Bank 0)

### 9.62 CPUFANOUT Step Down Time Register - Index 70h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to decrease its value by one step.

(1)For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2)For DC output:

The units are intervals of 0.4 seconds. The default time is 4 seconds.

### 9.63 CPUFANOUT Step Up Time Register - Index 71h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to increase its value by one step.

(1)For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2)For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

### 9.64 AUXFANOUT Step Down Time Register - Index 72h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT takes to decrease its value by one step.

(1)For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2)For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

### 9.65 AUXFANOUT Step Up Time Register - Index 73h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT takes to increase its value by one step.

(1)For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2)For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

### 9.66 Critical Temperature Enable Register - Index 74h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					EN_AUX_CRITICAL	EN_CPU_CRITICAL	EN_SYS_CRITICAL
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Reserved.
2	EN_AUX_CRITICAL (While temperature source exceed critical temperature, AUXFANOUT out maximal value.)

BIT	DESCRIPTION
	1: Enable AUXFANOUT critical temperature protection. 0: Disable AUXFANOUT critical temperature protection. (Default)
1	<b>EN_CPU_CRITICAL (While temperature source exceed critical temperature, CPUFANOUT out maximal value.)</b> 1: Enable CPUFANOUT critical temperature protection. 0: Disable CPUFANOUT critical temperature protection. (Default)
0	<b>EN_SYS_CRITICAL (While temperature source exceed critical temperature, SYSFANOUT out maximal value.)</b> 1: Enable SYSFANOUT critical temperature protection. 0: Disable SYSFANOUT critical temperature protection. (Default)

This register is applied to SMART FAN™ mode I, III, IV.

### 9.67 SYSFANOUT Critical Temperature Register - Index 75h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Critical Temperature							
DEFAULT	0	1	1	0	0	1	0	0

When the function of SYSFANOUT critical temperature sensing is enabled, and the monitored temperature exceeds the threshold temperature, the SYSFANOUT will work at full speed. This register is applied to SMART FAN™ mode I, III, IV.

### 9.68 CPUFANOUT Critical Temperature Register - Index 76h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Critical Temperature							
DEFAULT	0	1	1	0	0	1	0	0

When the function of CPUFANOUT critical temperature sensing is enabled, and the monitored temperature exceeds the threshold temperature, the CPUFANOUT will work at full speed. This register is applied to SMART FAN™ mode I, III, IV.

### 9.69 AUXFANOUT Critical Temperature Register - Index 77h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Critical Temperature							
DEFAULT	0	1	1	0	0	1	0	0

When the function of AUXFANOUT critical temperature sensing is enabled, and the monitored temperature exceeds the threshold temperature, the AUXFANOUT will work at full speed. This register is applied to SMART FAN™ mode I, III, IV.

### 9.70 Reserved register - Index 78h ~ 7Ah (Bank 0)

#### 9.71 SMI# Mask Register 5 - Index 7Bh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			VID	VID (Auto Clear)	AUXFANOUT	CPUFANOUT	SYSFANOUT
DEFAULT	0	0	0	1	1	1	1	1

BIT	DESCRIPTION	
7-5	Reserved.	"1" disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 4 - Index 45h (Bank 0))
4	VID.	
3	VID (Auto Clear).	
2	AUXFANOUT.	
1	CPUFANOUT.	
0	SYSFANOUT.	

#### 9.72 SYSFAN Temperature Source (Low Byte) Register - Index 7Ch (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						

BIT	DESCRIPTION
7	TEMP <0>. Temperature <0> of the SYSFAN temperature source. The nine-bit value is in units of 0.5°C.
6-0	Reserved.

**9.73 Temperature Report Select Register - Index 7Dh (Bank 0)**

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				Temperature Select			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Reserved.
2-0	<b>Temperature source select for report to Bank0 Index7Eh.</b> <b>Bits</b> <b>2 1 0</b> 0 0 0: Select SYSTIN (Default) 0 0 1: Select CPUTIN 0 1 0: Select AUX TIN 0 1 1: Select AMDT SI 1 0 0: Select PE CI Agent 1 1 0 1: Select PE CI Agent 2 1 1 0: Select PE CI Agent 3 1 1 1: Select PE CI Agent 4

**9.74 Temperature Source Report Data Register - Index 7Eh (Bank 0)**

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	Temperature data <8:1> depend on Bank0 Index7D bit2~0 setting.

**9.75 Reserved Register - Index7Fh (Bank 0)**

### 9.76 CPUFAN Temperature Source (High Byte) Register - Index 50h (Bank 1)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	Temperature <8:1> of the CPUFAN temperature source. The nine-bit value is in units of 0.5°C.

### 9.77 CPUFAN Temperature Source (Low Byte) Register - Index 51h (Bank 1)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						

BIT	DESCRIPTION
7	TEMP <0>. Temperature <0> of the CPUFAN temperature source. The nine-bit value is in units of 0.5°C.
6-0	Reserved.

### 9.78 CPUFAN Temperature Source Configuration Register - Index 52h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	Reserved. This bit should be set to zero.
4-3	Fault. Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	Reserved. This bit should be set to zero.
1	OVTMOD. OVT# Mode Select. 0: Compare Mode. (Default) 1: Interrupt Mode.
0	STOP. 0: Monitor CPUFAN temperature source. 1: Stop monitoring CPUFAN temperature source.

### 9.79 CPUFAN Temperature Source Hysteresis (High Byte) Register - Index 53h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	<b>THYST&lt;8:1&gt;</b> . Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

### 9.80 CPUFAN Temperature Source Hysteresis (Low Byte) Register - Index 54h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	<b>THYST&lt;0&gt;</b> . Hysteresis temperature bit 0. The nine-bit value is in units of 0.5°C.
6-0	Reserved.

### 9.81 CPUFAN Temperature Source Over-temperature (High Byte) Register - Index 55h (Bank1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	<b>TOVF&lt;8:1&gt;</b> . Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

### 9.82 CPUFAN Temperature Source Over-temperature (Low Byte) Register - Index 56h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	TOVF<0>. Over-temperature bit 0. The nine-bit value is in units of 0.5°C.
6-0	Reserved.

### 9.83 Reserved Register - Index 57h ~ 5Fh (Bank 1)

### 9.84 AUXFAN/ VIN2 Temperature Source (High Byte) Register - Index 50h (Bank 2)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1> / VIN2							

BIT	DESCRIPTION
7-0	VIN2 reading / TEMP<8:1> of the AUXFAN temperature source. The nine-bit value is in units of 0.5°C.

### 9.85 AUXFAN/ VIN2 Temperature Source (Low Byte) Register - Index 51h (Bank 2)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						

BIT	DESCRIPTION
7	TEMP<0>. Temperature <0> of the AUXFAN temperature source. The nine-bit value is in units of 0.5°C.
6-0	Reserved.

### 9.86 AUXFAN Temperature Source Configuration Register - Index 52h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	<b>Reserved.</b> This bit should be set to zero.
4-3	<b>Fault.</b> Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	<b>Reserved.</b> This bit should be set to zero.
1	<b>OVTMOD. OVT# Mode Select.</b> 0: Compare Mode. (Default) 1: Interrupt Mode.
0	<b>STOP.</b> 0: Monitor AUXFAN temperature source. 1: Stop monitoring AUXFAN temperature source.

### 9.87 AUXFAN Temperature Source Hysteresis (High Byte) Register - Index 53h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	<b>THYST&lt;8:1&gt;.</b> Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

### 9.88 AUXFAN Temperature Source Hysteresis (Low Byte) Register - Index 54h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
-----	-------------

BIT	DESCRIPTION
7	THYST<0>. Hysteresis temperature, bit 0. The nine-bit value is in units of 0.5°C.
6-0	Reserved.

### 9.89 AUXFAN Temperature Source Over-temperature (High Byte) Register - Index 55h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	THYST<8:1>. Over-temperature, bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

### 9.90 AUXFAN Temperature Source Over-temperature (Low Byte) Register - Index 56h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	TOVF<0>. Over-temperature, bit 0. The nine-bit value is in units of 0.5°C.
6-0	Reserved.

### 9.91 Reserved Register - Index 57h ~ 5Fh (Bank 2)

### 9.92 Reserved Register - Index 50h ~ 5Fh (Bank 3)

### 9.93 Interrupt Status Register 3 - Index 50h (Bank 4)

Attribute: [Read Clear](#)

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		AUXFANIN2	AUXFANIN1	RESERVED	TAR3	VBAT	3VSB
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	Reserved.
5	<b>AUXFANIN2.</b> A one indicates the fan count limit of AUXFANIN2 has been exceeded.
4	<b>AUXFANIN1.</b> A one indicates the fan count limit of AUXFANIN1 has been exceeded.
3	Reserved.
2	<b>TAR3.</b> A one indicates that the AUCTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode.
1	<b>VBAT.</b> A one indicates the high or low limit of VBAT has been exceeded.
0	<b>3VSB.</b> A one indicates the high or low limit of 3VSB has been exceeded.

#### 9.94 SMI# Mask Register 4 - Index 51h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			TAR3	RESERVED		VBAT	3VSB
DEFAULT	0	0	0	1	0	0	1	1

BIT	DESCRIPTION
7-5	Reserved.
4	<b>TAR3.</b> A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
3-2	Reserved.
1	<b>VBAT.</b> A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
0	<b>3VSB.</b> A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))

#### 9.95 Reserved Register - Index 52h (Bank 4)

#### 9.96 BEEP Control Register 3 - Index 53h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		EN_USER_BP	RESERVED			EN_VBAT_BP	EN_3VSB_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	Reserved.
5	<b>EN_USER_BP.</b> User-defined BEEP Output Function.

BIT	DESCRIPTION
	0: Make BEEP inactive. (Default) 1: Make BEEP active.
4-2	<b>Reserved.</b>
1	<b>EN_VBAT_BP. BEEP Output Control for VBAT</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)
0	<b>EN_3VSB_BP. BEEP Output Control for 3VSB</b> if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)

### 9.97 SYSTIN Temperature Sensor Offset Register - Index 54h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	<b>SYSTIN Temperature Offset Value.</b> The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

### 9.98 CPUTIN Temperature Sensor Offset Register - Index 55h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	<b>CPUTIN Temperature Offset Value.</b> The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

### 9.99 AUXTIN Temperature Sensor Offset Register - Index 56h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
-----	---	---	---	---	---	---	---	---

NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	<b>AUXTIN Temperature Offset Value.</b> The value in this register is added to the monitored value so that the read value is the sum of the monitored value and this offset value.

### 9.100 Reserved Register - Index 57h-58h (Bank 4)

### 9.101 Real Time Hardware Status Register I - Index 59h (Bank 4)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN_ST	SYSFANIN_ST	CPUTIN_ST	SYSTIN_ST	3VCC_ST	AVCC_ST	VIN0_ST	CPUVCORE_ST
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	<b>CPUFANIN_ST. CPUFANIN Status.</b> 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
6	<b>SYSFANIN_ST. SYSFANIN Status.</b> 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
5	<b>CPUTIN_ST. CPUTIN Temperature Sensor Status.</b> 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
4	<b>SYSTIN_ST. SYSTIN Temperature Sensor Status.</b> 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
3	<b>3VCC_ST. 3VCC Voltage Status.</b> 1: 3VCC voltage is over or under the allowed range. 0: 3VCC voltage is in the allowed range.
2	<b>AVCC_ST. AVCC Voltage Status.</b> 1: AVCC voltage is over or under the allowed range. 0: AVCC voltage is in the allowed range.
1	<b>VIN0_ST. VIN0 Voltage Status.</b> 1: VIN0 voltage is over or under the allowed range. 0: VIN0 voltage is in the allowed range.
0	<b>CPUVCORE_ST. CPUVCORE Voltage Status.</b> 1: CPUVCORE voltage is over or under the allowed range. 0: CPUVCORE voltage is in the allowed range.

**9.102 Real Time Hardware Status Register II - Index 5Ah (Bank 4)**

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2_STG	TAR1_STG	AUXTIN_STG	CASEOPEN_STG	AUXFANIN_STG	AUXFANIN1_STG	TAR4_STG	VIN1_STG
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	<b>TAR2_STG. Smart Fan of CPUFANIN Warning Status.</b> 1: FANCTRL3 selected temp has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: Selected temperature has not reached the warning range.
6	<b>TAR1_STG. Smart Fan of SYSFANIN Warning Status.</b> 1: FANCTRL1 selected temp has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: SYSTIN temperature has not reached the warning range.
5	<b>AUXTIN_STG. AUXTIN Temperature Sensor Status.</b> 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
4	<b>CASEOPEN_STG. CaseOpen Status.</b> 1: Caseopen is detected and latched. 0: Caseopen is not latched.
3	<b>AUXFANIN_STG. AUXFANIN Status.</b> 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
2	<b>AUXFANIN1_STG. AUXFANIN1 Status.</b> 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
1	Reserved.
0	<b>VIN1_STG. VIN1 Voltage Status.</b> 1: VIN1 voltage is over or under the allowed range. 0: VIN1 voltage is in the allowed range.

### 9.103 Real Time Hardware Status Register III - Index 5Bh (Bank 4)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2_STSTS	RESERVED	VCROE_REFIN_STSTS	VIN2_STSTS	RESERVED	TAR3_STSTS	VBAT_STSTS	VSB_STSTS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	<b>AUXFANIN2_STSTS. AUXFANIN2 Status.</b> 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
6	<b>Reserved.</b>
5	<b>VCROE_REFIN_STSTS. VCROE_REFIN Voltage Status.</b> 1: VCROE_REFIN Voltage is over or under the allowed range. 0: VCROE_REFIN Voltage is in the allowed range.
4	<b>VIN2_STSTS. VIN2 Voltage Status.</b> 1: VIN2 voltage is over or under the allowed range. 0: VIN2 voltage is in the allowed range.
3	<b>Reserved.</b>
2	<b>TAR3_STSTS. Smart Fan of AUXFANIN Warning Status.</b> 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: The selected temperature has not reached the warning range.
1	<b>VBAT_STSTS. VBAT Voltage Status.</b> 1: The VBAT voltage is over or under the allowed range. 0: The VBAT voltage is in the allowed range.
0	<b>VSB_STSTS. 3VSB Voltage Status.</b> 1: The 3VSB voltage is over or under the allowed range. 0: The 3VSB voltage is in the allowed range.

### 9.104 Reserved Register - Index 5Ch ~ 5Fh (Bank 4)

### 9.105 Value RAM 2 — Index 50h-5Fh (Bank 5)

ADDRESS A6-A0	DESCRIPTION
50h	3VSB reading
51h	VBAT reading. The reading is meaningless unless EN_VBAT_MN (Bank0 Index 5Dh, bit0) is set.
52h	Reserved
53h	AUXFANIN2 reading Note: This location stores the number of counts of the internal clock per

ADDRESS A6-A0	DESCRIPTION
	revolution.
54h	3VSB High Limit
55h	3VSB Low Limit
56h	VBAT High Limit
57h	VBAT Low Limit
58h – 5Bh	Reserved
5Ch	AUXFANIN2 Fan Count Limit <b>Note:</b> It is the number of counts of the internal clock for the Low Limit of the fan speed.
5Dh – 5Fh	Reserved

#### 9.106 SYSTIN SMI# Shut-down mode High Limit Temperature Register - Index 50h (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSTIN SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	SYSTIN SMI# Shut-down mode High Limit Temperature.

#### 9.107 SYSTIN SMI# Shut-down mode Low Limit Temperature Register - Index 51h (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSTIN SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	SYSTIN SMI# Shut-down mode Low Limit Temperature.

### 9.108 CPU TIN SMI# Shut-down mode High Limit Temperature Register - Index 52h (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPU TIN SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	CPU TIN SMI# Shut-down mode High Limit Temperature.

### 9.109 CPU TIN SMI# Shut-down mode Low Limit Temperature Register - Index 53h (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPU TIN SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	CPU TIN SMI# Shut-down mode Low Limit Temperature.

### 9.110 AUX TIN SMI# Shut-down mode High Limit Temperature Register - Index 54h (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUX TIN SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	AUX TIN SMI# Shut-down mode High Limit Temperature.

### 9.111 AUXTIN SMI# Shut-down mode Low Limit Temperature Register - Index 55h (Bank 6)

Attribute: Read/Write  
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	AUXTIN SMI# Shut-down mode Low Limit Temperature.

### 9.112 Reserved Register - Index 56h ~ 5Fh (Bank 6)

### 9.113 Reserved Register - Index 50h ~ 5Fh (Bank 7)

### 9.114 FANOUT Configure register of PECI Error - Index 50h (Bank 8)

Attribute: Read/Write  
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.					PECI Error Condition		
DEFAULT	0	0	0	0	0	1	0	1

BIT	DESCRIPTION
7-3	Reserved.
2-0	<p><b>PECI Error Condition Bits</b>  <b>2 1 0</b>            0 0 0: FANOUT keeps at its current value            1 1 1: FANOUT will be set to the pre-configured value.</p>

### 9.115 SYSFANOUT pre-configured fan output value for PECI error - Index 51h (Bank 8)

Attribute: Read/Write  
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT pre-configured fan output value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0	
PWM Output	DESCRIPTION	SYSFANOUT PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.								
	DEFAULT	1	1	1	1	1	1	1	1	
DC Output	DESCRIPTION	SYSFANOUT Voltage Control. The output voltage is calculated according to this equation:  <b>OUTPUT Voltage = <math>V_{ref} * \frac{FANOUT}{64}</math></b>						Reserved		
	DEFAULT	1	1	1	1	1	1			

**9.116 CPUFANOUT pre-configured fan output value for PECl error - Index 52h (Bank 8)**

Attribute: Read/Write  
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT pre-configured fan output value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0	
PWM Output	DESCRIPTION	CPUFANOUT PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.								
	DEFAULT	1	1	1	1	1	1	1	1	
DC Output	DESCRIPTION	CPUFANOUT Voltage Control. The output voltage is calculated according to this equation:  <b>OUTPUT Voltage = <math>V_{ref} * \frac{FANOUT}{64}</math></b>						Reserved		
	DEFAULT	1	1	1	1	1	1			

**9.117 AUXFANOUT pre-configured fan output value for PECl error - Index 53h (Bank 8)**

Attribute: Read/Write  
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	AUXFANOUT pre-configured fan output value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	AUXFANOUT PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	1	1	1	1	1	1	1	1
DC Output	DESCRIPTION	AUXFANOUT Voltage Control. The output voltage is calculated according to this equation:  $\text{OUTPUT Voltage} = V_{ref} * \frac{FANOUT}{64}$							Reserved
	DEFAULT	1	1	1	1	1	1	1	

### 9.118 Reserved Register - Index 54h ~ 5Fh (Bank 8)

### 9.119 SYSFAN Configuration Register - Index 50h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Weight Source Sel			Reserved				EN_SYSFANOUT_SM4
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	<b>SYSFAN Weight Source Sel.</b> <b>Bits</b> <b>7 6 5</b> 0 0 0: SYSTIN (Def. ) 0 0 1: CPUTIN 0 1 0: AUXTIN 0 1 1: AMDTSI 1 0 0: PECI1 1 0 1: PECI2 1 1 0: PECI3 1 1 1: PECI4
4-1	<b>Reserved</b>
0	<b>EN_SYSFANOUT_SM4.</b> 0: SYSFANOUT ← FANCTRL 1 (SMART FAN™ I, III) 1: SYSFANOUT ← FANCTRL 2 (SMART FAN™ IV)

### 9.120 FANCTRL 2 (SMART FAN™ IV) Temperature 1 Register(T1) - Index 51h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 2 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 2 (SMART FAN™ IV) Temperature 1 Register (T1).

### 9.121 FANCTRL 2 (SMART FAN™ IV) Temperature 2 Register(T2) - Index 52h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 2 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 2 (SMART FAN™ IV) Temperature 2 Register (T2).

### 9.122 FANCTRL 2 (SMART FAN™ IV) Temperature 3 Register(T3) - Index 53h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 2 (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 2 (SMART FAN™ IV) Temperature 3 Register (T3).

### 9.123 FANCTRL 2 (SMART FAN™ IV) Temperature 4 Register(T4) - Index 54h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 2 (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 2 (SMART FAN™ IV) Temperature 4 Register (T4).

#### 9.124 FANCTRL 2 (SMART FAN™ IV) Temperature 5 Register(T5) - Index 55h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 2 (SMART FAN™ IV) Temperature 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 2 (SMART FAN™ IV) Temperature 5 Register (T5).

#### 9.125 FANCTRL 2 (SMART FAN™ IV) Temperature 6 Register(T6) - Index 56h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 2 (SMART FAN™ IV) Temperature 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 2 (SMART FAN™ IV) Temperature 6 Register (T6).

#### 9.126 FANCTRL 2 (SMART FAN™ IV) DC/PWM 1 Register - Index 57h (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 2 (SMART FAN™ IV) DC/PWM 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 2 (SMART FAN™ IV) DC/PWM 1 Register.

**9.127 FANCTRL 2 (SMART FAN™ IV) DC/PWM 2 Register - Index 58h (Bank 9)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 2 (SMART FAN™ IV) DC/PWM 2							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	FANCTRL 2 (SMART FAN™ IV) DC/PWM 2 Register.

**9.128 FANCTRL 2 (SMART FAN™ IV) DC/PWM 3 Register - Index 59h (Bank 9)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 2 (SMART FAN™ IV) DC/PWM 3							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	FANCTRL 2 (SMART FAN™ IV) DC/PWM 3 Register.

**9.129 FANCTRL 2 (SMART FAN™ IV) DC/PWM 4 Register - Index 5Ah (Bank 9)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 2 (SMART FAN™ IV) DC/PWM 4							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	FANCTRL 2 (SMART FAN™ IV) DC/PWM 4 Register.

**9.130 FANCTRL 2 (SMART FAN™ IV) DC/PWM 5 Register - Index 5Bh (Bank 9)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 2 (SMART FAN™ IV) DC/PWM 5							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 2 (SMART FAN™ IV) DC/PWM 5 Register.

### 9.131 FANCTRL 2 (SMART FAN™ IV) DC/PWM 6 Register - Index 5Ch (Bank 9)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 2 (SMART FAN™ IV) DC/PWM 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 2 (SMART FAN™ IV) DC/PWM 6 Register.

### 9.132 Reserved Register - Index 5Dh ~ 5Fh (Bank 9)

### 9.133 CPUFAN Configuration Register - Index 50h (Bank A)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Weight Source Sel			Reserved				EN_CPUFANOUT_SM4
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	<b>CPUFAN Weight Source Sel.</b> <b>Bits</b> <b>7 6 5</b> 0 0 0: SYSTIN (Def. ) 0 0 1: CPUTIN 0 1 0: AUX TIN 0 1 1: AMDTSI 1 0 0: PEC1 1 0 1: PEC2 1 1 0: PEC3 1 1 1: PEC4
4-1	<b>Reserved</b>
0	<b>EN_CPUFANOUT_SM4.</b> 0: CPUFANOUT ← FANCTRL 3 (SMART FAN™ I, III) 1: CPUFANOUT ← FANCTRL 4 (SMART FAN™ IV)

### 9.134 FANCTRL 4 (SMART FAN™ IV) Temperature 1 Register(T1) - Index 51h (Bank A)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 4 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 4 (SMART FAN™ IV) Temperature 1 Register (T1).

### 9.135 FANCTRL 4 (SMART FAN™ IV) Temperature 2 Register(T2) - Index 52h (Bank A)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 4 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 4 (SMART FAN™ IV) Temperature 2 Register (T2).

### 9.136 FANCTRL 4 (SMART FAN™ IV) Temperature 3 Register(T3) - Index 53h (Bank A)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 4 (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 4 (SMART FAN™ IV) Temperature 3 Register (T3).

### 9.137 FANCTRL 4 (SMART FAN™ IV) Temperature 4 Register(T4) - Index 54h (Bank A)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
-----	---	---	---	---	---	---	---	---

<b>NAME</b>	<b>FANCTRL 4 (SMART FAN™ IV) Temperature 4</b>							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>							
7-0	<b>FANCTRL 4 (SMART FAN™ IV) Temperature 4 Register (T4).</b>							

### 9.138 FANCTRL 4 (SMART FAN™ IV) Temperature 5 Register(T5) - Index 55h (Bank A)

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>FANCTRL 4 (SMART FAN™ IV) Temperature 5</b>							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>							
7-0	<b>FANCTRL 4 (SMART FAN™ IV) Temperature 5 Register (T5).</b>							

### 9.139 FANCTRL 4 (SMART FAN™ IV) Temperature 6 Register(T6) - Index 56h (Bank A)

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>FANCTRL 4 (SMART FAN™ IV) Temperature 6</b>							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>							
7-0	<b>FANCTRL 4 (SMART FAN™ IV) Temperature 6 Register (T6).</b>							

### 9.140 FANCTRL 4 (SMART FAN™ IV) DC/PWM 1 Register - Index 57h (Bank A)

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>FANCTRL 4 (SMART FAN™ IV) DC/PWM 1</b>							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>							
7-0	<b>FANCTRL 4 (SMART FAN™ IV) DC/PWM 1 Register.</b>							

**9.141 FANCTRL 4 (SMART FAN™ IV) DC/PWM 2 Register - Index 58h (Bank A)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 4 (SMART FAN™ IV) DC/PWM 2							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	FANCTRL 4 (SMART FAN™ IV) DC/PWM 2 Register.

**9.142 FANCTRL 4 (SMART FAN™ IV) DC/PWM 3 Register - Index 59h (Bank A)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 4 (SMART FAN™ IV) DC/PWM 3							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	FANCTRL 4 (SMART FAN™ IV) DC/PWM 3 Register.

**9.143 FANCTRL 4 (SMART FAN™ IV) DC/PWM 4 Register - Index 5Ah (Bank A)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 4 (SMART FAN™ IV) DC/PWM 4							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	FANCTRL 4 (SMART FAN™ IV) DC/PWM 4 Register.

**9.144 FANCTRL 4 (SMART FAN™ IV) DC/PWM 5 Register - Index 5Bh (Bank A)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 4 (SMART FAN™ IV) DC/PWM 5							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 4 (SMART FAN™ IV) DC/PWM 5 Register.

### 9.145 FANCTRL 4 (SMART FAN™ IV) DC/PWM 6 Register - Index 5Ch (Bank A)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 4 (SMART FAN™ IV) DC/PWM 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 4 (SMART FAN™ IV) DC/PWM 6 Register.

### 9.146 Reserved Register - Index 5Dh ~ 5Fh (Bank A)

### 9.147 AUXFAN Configuration Register - Index 50h (Bank B)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN Weight Source Sel			Reserved				EN_AUXFANOUT_SM4
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	<b>AUXFAN Weight Source Sel.</b> <b>Bits</b> <b>7 6 5</b> 0 0 0: SYSTIN (Def. ) 0 0 1: CPUTIN 0 1 0: AUXTIN 0 1 1: AMDTSI 1 0 0: PEC1 1 0 1: PEC2 1 1 0: PEC3 1 1 1: PEC4
4-1	<b>Reserved</b>
0	<b>EN_AUXFANOUT_SM4.</b> 0: AUXFANOUT ← FANCTRL 5 (SMART FAN™ I, III) 1: AUXFANOUT ← FANCTRL 6 (SMART FAN™ IV)

### 9.148 FANCTRL 6 (SMART FAN™ IV) Temperature 1 Register(T1) - Index 51h (Bank B)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 6 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 6 (SMART FAN™ IV) Temperature 1 Register (T1).

### 9.149 FANCTRL 6 (SMART FAN™ IV) Temperature 2 Register(T2) - Index 52h (Bank B)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 6 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 6 (SMART FAN™ IV) Temperature 2 Register (T2).

### 9.150 FANCTRL 6 (SMART FAN™ IV) Temperature 3 Register(T3) - Index 53h (Bank B)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 6 (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 6 (SMART FAN™ IV) Temperature 3 Register (T3).

### 9.151 FANCTRL 6 (SMART FAN™ IV) Temperature 4 Register(T4) - Index 54h (Bank B)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
-----	---	---	---	---	---	---	---	---

<b>NAME</b>	<b>FANCTRL 6 (SMART FAN™ IV) Temperature 4</b>							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>							
7-0	<b>FANCTRL 6 (SMART FAN™ IV) Temperature 4 Register (T4).</b>							

### 9.152 FANCTRL 6 (SMART FAN™ IV) Temperature 5 Register(T5) - Index 55h (Bank B)

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>FANCTRL 6 (SMART FAN™ IV) Temperature 5</b>							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>							
7-0	<b>FANCTRL 6 (SMART FAN™ IV) Temperature 5 Register (T5).</b>							

### 9.153 FANCTRL 6 (SMART FAN™ IV) Temperature 6 Register(T6) - Index 56h (Bank B)

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>FANCTRL 6 (SMART FAN™ IV) Temperature 6</b>							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>							
7-0	<b>FANCTRL 6 (SMART FAN™ IV) Temperature 6 Register (T6).</b>							

### 9.154 FANCTRL 6 (SMART FAN™ IV) DC/PWM 1 Register - Index 57h (Bank B)

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>FANCTRL 6 (SMART FAN™ IV) DC/PWM 1</b>							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>							
7-0	<b>FANCTRL 6 (SMART FAN™ IV) DC/PWM 1 Register.</b>							

**9.155 FANCTRL 6 (SMART FAN™ IV) DC/PWM 2 Register - Index 58h (Bank B)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 6 (SMART FAN™ IV) DC/PWM 2							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	FANCTRL 6 (SMART FAN™ IV) DC/PWM 2 Register.

**9.156 FANCTRL 6 (SMART FAN™ IV) DC/PWM 3 Register - Index 59h (Bank B)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 6 (SMART FAN™ IV) DC/PWM 3							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	FANCTRL 6 (SMART FAN™ IV) DC/PWM 3 Register.

**9.157 FANCTRL 6 (SMART FAN™ IV) DC/PWM 4 Register - Index 5Ah (Bank B)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 6 (SMART FAN™ IV) DC/PWM 4							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	FANCTRL 6 (SMART FAN™ IV) DC/PWM 4 Register.

**9.158 FANCTRL 6 (SMART FAN™ IV) DC/PWM 5 Register - Index 5Bh (Bank B)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	FANCTRL 6 (SMART FAN™ IV) DC/PWM 5							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 6 (SMART FAN™ IV) DC/PWM 5 Register.

### 9.159 FANCTRL 6 (SMART FAN™ IV) DC/PWM 6 Register - Index 5Ch (Bank B)

Attribute: Read/Write  
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCTRL 6 (SMART FAN™ IV) DC/PWM 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	FANCTRL 6 (SMART FAN™ IV) DC/PWM 6 Register.

### 9.160 Reserved Register - Index 5Dh ~ 5Fh (Bank B)

### 9.161 Weight value Configuration Register - Index 50h (Bank C)

Attribute: Read/Write  
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					EN_AUXFAN_WEIGHT	EN_CPUFAN_WEIGHT	EN_SYSFAN_WEIGHT
DEFAULT	0	1	1	1	0	0	0	0

BIT	DESCRIPTION
7-3	Reserved
2	<b>EN_AUXFAN_WEIGHT.</b> 0: Disable Weight Value Control for AUXFAN. (Default) 1: Enable Weight Value Control for AUXFAN.
1	<b>EN_CPUFAN_WEIGHT.</b> 0: Disable Weight Value Control for CPUFAN. (Default) 1: Enable Weight Value Control for CPUFAN.
0	<b>EN_SYSFAN_WEIGHT.</b> 0: Disable Weight Value Control for SYSFAN. (Default) 1: Enable Weight Value Control for SYSFAN.

**9.162 SYSFANOUT Temperature Step Register - Index 51h (Bank C)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	SYSFANOUT Temperature Step (SYS_TEMP_STEP)							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	SYSFANOUT Temperature Step (SYS_TEMP_STEP).

**9.163 CPUFANOUT Temperature Step Register - Index 52h (Bank C)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	CPUFANOUT Temperature Step (CPU_TEMP_STEP)							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	CPUFANOUT Temperature Step (CPU_TEMP_STEP).

**9.164 AUXFANOUT Temperature Step Register - Index 53h (Bank C)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	AUXFANOUT Temperature Step (AUX_TEMP_STEP)							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	AUXFANOUT Temperature Step (AUX_TEMP_STEP).

**9.165 SYSFANOUT Weight Step Register - Index 54h (Bank C)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	SYSFANOUT Weight Step (SYS_WEIGHT_STEP)							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	<b>SYSFANOUT Weight Step (SYS_WEIGHT_STEP).</b>

### 9.166 CPUFANOUT Weight Step Register - Index 55h (Bank C)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>CPUFANOUT Weight Step (CPU_WEIGHT_STEP)</b>							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	<b>CPUFANOUT Weight Step (CPU_WEIGHT_STEP).</b>

### 9.167 AUXFANOUT Weight Step Register - Index 56h (Bank C)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>AUXFANOUT Weight Step (AUX_WEIGHT_STEP)</b>							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	<b>AUXFANOUT Weight Step (AUX_WEIGHT_STEP).</b>

### 9.168 SYSFANOUT Temperature Base Register - Index 57h (Bank C)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>SYSFANOUT Temperature Base (SYS_TEMP_BASE)</b>							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	<b>SYSFANOUT Temperature Base (SYS_TEMP_BASE).</b>

### 9.169 CPUFANOUT Temperature Base Register - Index 58h (Bank C)

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	CPUFANOUT Temperature Base (CPU_TEMP_BASE)							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	CPUFANOUT Temperature Base (CPU_TEMP_BASE).

### 9.170 AUXFANOUT Temperature Base Register - Index 59h (Bank C)

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	AUXFANOUT Temperature Base (AUX_TEMP_BASE)							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	AUXFANOUT Temperature Base (AUX_TEMP_BASE).

### 9.171 SYSFANOUT Temperature Step Tolerance Register - Index 5Ah (Bank C)

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	SYSFANOUT Temperature Step Tolerance (SYS_TEMP_STEP_TOL)							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	SYSFANOUT Temperature Step Tolerance (SYS_TEMP_STEP_TOL).

### 9.172 CPUFANOUT Temperature Step Tolerance Register - Index 5Bh (Bank C)

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	CPUFANOUT Temperature Step Tolerance (CPU_TEMP_STEP_TOL)							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	CPUFANOUT Temperature Step Tolerance (CPU_TEMP_STEP_TOL).

### 9.173 AUXFANOUT Temperature Step Tolerance Register - Index 5Ch (Bank C)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Temperature Step Tolerance (AUX_TEMP_STEP_TOL)							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFANOUT Temperature Step Tolerance (AUX_TEMP_STEP_TOL).

### 9.174 Reserved Register - Index 5Dh ~ 5Fh (Bank C)

### 9.175 Reserved Register - Index 50h ~ 51h (Bank D)

### 9.176 SYSFANOUT Critical Temperature Tolerance Register - Index 52h (Bank D)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Critical Temperature Tolerance							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SYSFANOUT Critical Temperature Tolerance

### 9.177 CPUFANOUT Critical Temperature Tolerance Register - Index 53h (Bank D)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Critical Temperature Tolerance							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	CPUFANOUT Critical Temperature Tolerance

**9.178 AUXFANOUT Critical Temperature Tolerance Register - Index 54h  
(Bank D)**

Attribute: Read/Write

Size: 8 bits

<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	AUXFANOUT Critical Temperature Tolerance							
<b>DEFAULT</b>	0	0	0	0	0	0	0	0

<b>BIT</b>	<b>DESCRIPTION</b>
7-0	AUXFANOUT Critical Temperature Tolerance

**9.179 Reserved Register - Index 50h ~ 5Fh (Bank E)**

**9.180 Reserved Register - Index 50h ~ 5Fh (Bank F)**

## 10. SERIAL PERIPHERAL INTERFACE

The W83667HG-A provides a bridge of the Low Pin Count (LPC) Interface to Serial Peripheral Interface (SPI). The signals in the SPI are transmitted through Pin 94 (SCK), Pin 95 (SCE#), Pin 97 (SI), and Pin 98 (SO). In the Super I/O (W83667HG-A), these 4 pins are multi-functional. The SPI functions are activated through strapping. Pin 32 determines whether to enable or disable the SPI functions. In the Super I/O (W83), the SPI functions are activated when Pin 32 is pulled-up to the power source. The function status can be seen/read at CR[24h], bit 1.

The SPI is primarily used to store the BIOS ROM. When booting the computer, the memory read instructions or timing sequences are transmitted from the CPU, the South Bridge, the LPC bus to the Super I/O (W83667HG-A). After receiving the instruction, the Super I/O (W83667HG-A) generates and transmits the correct instructions and memory addresses to the SPI which responds with the corresponding data of the addresses. The data are placed to the LPC bus by the Super I/O (W83667HG-A) and returned to the South Bridge. All of the data are read in this manner. By setting the registers of 10.1.1 SPI Command (Base + 0) and 10.1.2 SPI FIFO (Base + 1), the Super I/O (W83667HG-A) supports all the instructions given, such as erase, read, program, to SPI flash. For more details, please see Table 10-2 Address Map for SPI.

To make it more user-friendly, regularly used SPI instructions/functions can be generated via the LPC I/O read/write commands. That is, the flash devices with SPI can be programmed, erased, or read on the motherboard.

### 10.1 Using the SPI Interface via the LPC

- The allowed range is 8 bytes above the base address. The base address is configured at Configuration Register CR[62h] and CR[63h] in Logical Device 6. For example, if 03h is written to Configuration Register CR[62h], and F8h to Configuration Register CR[63h], 03F8h ~ 03FFh is the allowed range.

Table 10-1 Base Address Setting

Logical Device	Configuration Register	Bit	Function
6	62	7:0	High byte of Base Address
	63	7:0	Low byte of Base Address

- Functions and Definitions

The functions and definitions of the 8 bytes are shown in the following table.

Table 10-2 Address Map for SPI

		Bit Number								
Register file		Abbr.	7	6	5	4	3	2	1	0
Base + 0	Configuration Register	CFG	Counts of Returned Byte						Write	Read
Base + 1	Command Register	CMD	FIFO of 16-byte depth							
	Argument Register (WO)	ARG	FIFO of 16-byte depth							
	Data Register (RO)	DAT	FIFO of 16-byte depth							

### 10.1.1 SPI Command (Base + 0)

Attribute: Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Counts of Returned Byte					RESERVED	WRITE	READ
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~3	<b>Counts of Returned Byte.</b> Expected data bytes from SPI (The count range is 00h~10h).
2	<b>Reserved</b>
1	<b>Write Command</b> (when Counts of Returned Byte is 00h set "1", 01h~10h set "0")
0	<b>Read Command</b> (when Counts of Returned Byte is 01h~10h set "1", 00h set "0")

### 10.1.2 SPI FIFO (Base + 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	<b>Write FIFO.</b> 1 Up to 16 bytes write FIFOs. This register will output the data to SPI flash byte after byte following the configuration.
	<b>Read FIFO</b> 1 Up to 16 bytes read FIFOs. The register receives data from the SPI flash.

- Usages

Write SPI instructions to Base+0. Set up the command, addresses and the data in Base+1.

- Accessing SPI Devices

To control SPI Function, FIFO Register (base + 1) and Configuration Register (base + 0) have to be written in sequence to send data to SPI Flash. If the data is not written to FIFO Register but to Command Register, only the command will be sent to SPI Flash. If the data is written to FIFO Register, it will be transmitted right after the configuration until "FIFO Empty".

\* For more details, please see the W83667HG Programming Guide.

## 11. FLOPPY DISK CONTROLLER

### 11.1 FDC Functional Description

The floppy disk controller (FDC) of the W83667HG-A integrates all of the logic required for floppy disk control. The FDC implements a FIFO which provides better system performance in multi-master systems, and the digital data separator supports data rates up to 2 M bits/sec.

The FDC includes the following blocks: Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core. The rest of this section discusses these blocks through the following topics: FIFO, Data Separator, Write Precompensation, Perpendicular Recording mode, FDC core, FDC commands, and FDC registers.

#### 11.1.1 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM (Request fro Master) and DIO (Data Input / Output) bits in the Main Status Register.

The FIFO is defaulted to disabled mode after any form of reset, which maintains PC/AT hardware compatibility. The default values can be changed through the configure command. The advantage of the FIFO is that it lets the system have a larger DMA latency without causing disk errors. The following tables give several examples of the delays with the FIFO. The data are based upon the following formula:

$$\text{DELAY} = \text{THRESHOLD \#} \times (1 / \text{DATA RATE}) * 8 - 1.5 \mu\text{s}$$

Table 11-1 The Delays of the FIFO

FIFO THRESHOLD	MAXIMUM DELAY UNTIL SERVICING AT 500K BPS
	Data Rate
1 Byte	$1 \times 16 \mu\text{s} - 1.5 \mu\text{s} = 14.5 \mu\text{s}$
2 Byte	$2 \times 16 \mu\text{s} - 1.5 \mu\text{s} = 30.5 \mu\text{s}$
8 Byte	$8 \times 16 \mu\text{s} - 1.5 \mu\text{s} = 6.5 \mu\text{s}$
15 Byte	$15 \times 16 \mu\text{s} - 1.5 \mu\text{s} = 238.5 \mu\text{s}$
FIFO THRESHOLD	MAXIMUM DELAY UNTIL SERVICING AT 1M BPS
	Data Rate
1 Byte	$1 \times 8 \mu\text{s} - 1.5 \mu\text{s} = 6.5 \mu\text{s}$
2 Byte	$2 \times 8 \mu\text{s} - 1.5 \mu\text{s} = 14.5 \mu\text{s}$
8 Byte	$8 \times 8 \mu\text{s} - 1.5 \mu\text{s} = 62.5 \mu\text{s}$
15 Byte	$15 \times 8 \mu\text{s} - 1.5 \mu\text{s} = 118.5 \mu\text{s}$

At the start of a command, the FIFO is always disabled, and command parameters must be sent based upon the RQM and DIO bit settings in the Main Status Register. When the FDC enters the command execution phase, it clears the FIFO off any data to ensure that invalid data are not transferred.

An overrun or underrun terminates the current command and data transfer. Disk writes complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled by the specify command and are initiated by the FDC when the LDRQ pin is activated during a data transfer command.

### **11.1.2 Data Separator**

The function of the data separator is to lock onto incoming serial read data. When a lock is achieved, the serial front-end logic in the chip is provided with a clock that is synchronized with the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial-to-parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The control logic generates RDD and RWD for every pulse input, and any data pulse input is synchronized and then adjusted immediately by error adjustment. A digital integrator keeps track of the speed changes in the input data stream.

### **11.1.3 Write Precompensation**

The write precompensation logic minimizes bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and depends on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known, so, depending on the pattern, the bit is shifted either early or late, relative to the surrounding bits.

### **11.1.4 Perpendicular Recording Mode**

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. Perpendicular mode requires a 1 Mbps data rate for the FDC, and, at this data rate, the FIFO manages the host interface bottleneck due to the high speed of data transfer to and from the disk.

### 11.1.5FDC Core

The W83667HG-A FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor, and the result may be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

#### Command

The microprocessor issues all required information to the controller to perform a specific operation.

#### Execution

The controller performs the specified operation.

#### Result

After the operation is completed, status information and other housekeeping information are provided to the microprocessor.

The next section introduces each of the commands.

### 11.1.6FDC Commands

Command Symbol Descriptions:

C:	Cylinder Number 0 - 256
D:	Data Pattern
DIR:	Step Direction DIR = 0: step out DIR = 1: step in
DS0:	Disk Drive Select 0
DS1:	Disk Drive Select 1
DTL:	Data Length
EC:	Enable Count
EFIFO:	Enable FIFO
EIS:	Enable Implied Seek
EOT:	End of Track
FIFOTHR:	FIFO Threshold
GAP:	Gap Length Selection
GPL:	Gap Length
H:	Head Number
HDS:	Head Number Select
HLT:	Head Load Time
HUT:	Head Unload Time
LOCK:	Lock EFIFO, FIFOTHR, and PTRTRK bits to prevent being affected by software reset
MFM:	MFM or FM Mode
MT:	Multitrack
N:	The number of data bytes written in a sector
NCN:	New Cylinder Number
ND:	Non-DMA Mode
OW:	Overwritten
PCN:	Present Cylinder Number

POLL: Polling Disable  
 PRETRK: Precompensation Start Track Number  
 R: Record  
 RCN: Relative Cylinder Number  
 R/W: Read/Write  
 SC: Sectors per Cylinder  
 SK: Skip deleted data address mark  
 SRT: Step Rate Time  
 ST0: Status Register 0  
 ST1: Status Register 1  
 ST2: Status Register 2  
 ST3: Status Register 3  
 WG: Write gate alters timing of WE

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS		
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes		
	W	0	0	0	0	0	HDS	DS1	DS0			
	W	----- C -----									Sector ID information prior to command execution	
	W	----- H -----										
	W	----- R -----										
	W	----- N -----										
	W	----- EOT -----										
	W	----- GPL -----										
W	----- DTL -----											
Execution										Data transfer between the FDD and system		
Result	R	----- ST0 -----									Status information after command execution	
	R	----- ST1 -----										
	R	----- ST2 -----										
	R	----- C -----									Sector ID information after command execution	
	R	----- H -----										
	R	----- R -----										
	R	----- N -----										

(2) Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command codes  Sector ID information prior to command execution
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				----- C -----					
	W				----- H -----					
	W				----- R -----					
	W				----- N -----					
	W				----- EOT -----					
	W				----- GPL -----					
W				----- DTL -----						
Execution										Data transfer between the FDD and system
Result	R				----- ST0 -----					Status information after command execution
	R				----- ST1 -----					
	R				----- ST2 -----					
	R				----- C -----					Sector ID information after command execution
	R				----- H -----					
	R				----- R -----					
	R				----- N -----					

**(3) Read A Track**

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS	
Command	W	0	MFM	0	0	0	0	1	0	Command codes	
	W	0	0	0	0	0	HDS	DS1	DS0		
	W	----- C -----									Sector ID information prior to command execution
	W	----- H -----									
	W	----- R -----									
	W	----- N -----									
	W	----- EOT -----									
	W	----- GPL -----									
W	----- DTL -----										
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT	
Result	R	----- ST0 -----								Status information after command execution	
	R	----- ST1 -----									
	R	----- ST2 -----									
	R	----- C -----								Sector ID information after command execution	
	R	----- H -----									
	R	----- R -----									
	R	----- N -----									

**(4) Read ID**

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in the Data Register
Result	R	----- ST0 -----								Status information after command execution
	R	----- ST1 -----								
	R	----- ST2 -----								
	R	----- C -----								Disk status after the command has been completed
	R	----- H -----								
	R	----- R -----								
	R	----- N -----								

(5) Verify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command codes  Sector ID information prior to command execution
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	----- C -----								
	W	----- H -----								
	W	----- R -----								
	W	----- N -----								
	W	----- EOT -----								
	W	----- GPL ----- ----- DTL/SC -----								
Execution										No data transfer takes place
Result	R	----- ST0 -----								Status information after command execution
	R	----- ST1 -----								
	R	----- ST2 -----								
	R	----- C -----								Sector ID information after command execution
	R	----- H -----								
	R	----- R -----								
	R	----- N -----								

(6) Version

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

## (7) Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS	
Command	W	MT	MFM	0	0	0	1	0	1	Command codes	
	W	0	0	0	0	0	HDS	DS1	DS0		
	W	----- C -----									Sector ID information prior to Command execution
	W	----- H -----									
	W	----- R -----									
	W	----- N -----									
	W	----- EOT -----									
	W	----- GPL -----									
	W	----- DTL -----									
Execution										Data transfer between the FDD and the system	
Result	R	----- ST0 -----								Status information after Command execution	
	R	----- ST1 -----									
	R	----- ST2 -----									
	R	----- C -----								Sector ID information after Command execution	
	R	----- H -----									
	R	----- R -----									
	R	----- N -----									

## (8) Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS	
Command	W	MT	MFM	0	0	1	0	0	1	Command codes	
	W	0	0	0	0	0	HDS	DS1	DS0		
	W	----- C -----									Sector ID information prior to command execution
	W	----- H -----									
	W	----- R -----									
	W	----- N -----									
	W	----- EOT -----									
	W	----- GPL -----									
	W	----- DTL -----									
Execution										Data transfer between the FDD and the system	
Result	R	----- ST0 -----								Status information after command execution	
	R	----- ST1 -----									
	R	----- ST2 -----									
	R	----- C -----								Sector ID information after command execution	
	R	----- H -----									
	R	----- R -----									
	R	----- N -----									

## (9) Format A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS	
Command	W	0	MFM	0	0	1	1	0	1	Command codes	
	W	0	0	0	0	0	HDS	DS1	DS0		
	W	----- N -----									Bytes per Sector
	W	----- SC -----									
	W	----- GPL -----									Gap 3
	W	----- D -----									Filler Byte
Execution for Each Sector: (Repeat)	W	----- C -----								Input Sector Parameters	
	W	----- H -----									
	W	----- R -----									
	W	----- N -----									
Result	R	----- ST0 -----								Status information after command execution	
	R	----- ST1 -----									
	R	----- ST2 -----									
	R	----- Undefined -----									
	R	----- Undefined -----									
	R	----- Undefined -----									

## (10) Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt

## (11) Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	----- ST0 -----								Status information at the end of each seek operation
	R	----- PCN -----								

## (12) Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	-----SRT -----  ----- HUT -----								
	W	----- HLT -----  ND								

## (13) Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	----- NCN -----								
Execution	R									Head positioned over proper cylinder on the diskette

## (14) Configure

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS	
Command	W	0	0	0	1	0	0	1	1	Configure information	
	W	0	0	0	0	0	0	0	0		
	W	0	EIS	EFIFO	POLL		----	FIFOTHR	----		
	W		-----	PRETRK	-----						
Execution										Internal registers written	

## (15) Relative Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W		-----	RCN	-----					

## (16) Dumpreg

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS	
Command	W	0	0	0	0	1	1	1	0	Registers placed in FIFO	
Result	R	----- PCN-Drive 0-----									
	R	----- PCN-Drive 1-----									
	R	----- PCN-Drive 2-----									
	R	----- PCN-Drive 3-----									
	R	-----SRT-----		-----	HUT	-----					
	R	-----	HLT	-----		ND					
	R	----- SC/EOT-----									
	R	LOCK	0	D3	D2	D1	D0	GAP	WG		
	R	0	EIS	EFIFO	POLL		----	FIFOTHR	-----		
	R	-----PRETRK-----									

## (17) Perpendicular Mode

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
-------	-----	----	----	----	----	----	----	----	----	---------

Command	W	0	0	0	1	0	0	1	0	Command Code
	W	OW	0	D3	D2	D1	D0	GAP	WG	

**(18) Lock**

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	

**(19) Sense Drive Status**

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	----- ST3 -----								Status information about the disk drive

**(20) Invalid**

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	----- Invalid Codes -----								Invalid codes (no operation-FDC goes to standby state)
Result	R	----- ST0 -----								
										ST0 = 80h

## 11.2 Register Descriptions

There are several status, data, and control registers in the W83667HG-A. These registers are defined below, and the rest of this section provides more details about each one of them.

Table 11-2 FDC Registers

ADDRESS OFFSET	REGISTER	
	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

### 11.2.1 Status Register A (SA Register) (Read base address + 0)

Along with the SB register, the SA register is used to monitor several disk-interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	INIT PENDING	DRV 2#	STEP	TRAK0#	HEAD	INDEX#	WP#	DIR
DEFAULT	0	0	NA	1	NA	1	1	NA

BIT	DESCRIPTION
7	<b>INIT PENDING.</b> Indicates the value of the floppy disk interrupt output.
6	<b>DRV2#.</b> 0: A second drive has been installed. 1: A second drive has not been installed.
5	<b>STEP.</b> Indicates the complement of the STEP# output.
4	<b>TRAK0#.</b> Indicates the value of the TRAK# input.
3	<b>HEAD.</b> Indicates the complement of the HEAD# output. 0: Side 0. 1: Side 1.
2	<b>INDEX#.</b> Indicates the value of the INDEX# output.
1	<b>WP#.</b> 0: The disk is write-protected. 1: The disk is not write-protected.
0	<b>DIR.</b> Indicates the direction of head movement. 0: Outward direction. 1: Inward direction.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	INIT PENDING	DRQ	STEP F/F	TRAK0	HEAD#	INDEX	WP	DIR#
DEFAULT	0	0	NA	0	NA	0	0	NA

BIT	DESCRIPTION
7	<b>INIT PENDING.</b> Indicates the value of the floppy disk interrupt output.
6	<b>DRQ.</b> Indicates the value of the DRQ output pin.
5	<b>SETP F/F.</b> indicates the complement of latched STEP# output.
4	<b>TRAK0.</b> Indicates the complement of the TRAK0# input.
3	<b>HEAD#.</b> Indicates the value of the HEAD# output. 0: Side 1. 1: Side 0.
2	<b>INDEX.</b> Indicates the complement of the INDEX# output.
1	<b>WP.</b> 0: The disk is not write-protected. 1: The disk is write-protected.
0	<b>DIR#.</b> Indicates the direction of the head movement. 0: Inward direction. 1: Outward direction.

### 11.2.2 Status Register B (SB Register) (Read base address + 1)

Along with the SA register, the SB register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Drive SEL0	WDTA Toggle	RDTA Toggle	WE	Reserved	MOT EN A
DEFAULT	1	1	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	<b>Reserved.</b>
5	<b>Drive SEL0.</b> Indicates the status of the DO Register, bit 0 (drive-select bit 0).
4	<b>WDATA Toggle.</b> Changes state on every rising edge of the WD# output pin.
3	<b>RDATA Toggle.</b> Changes state on every rising edge of the RDATA# output pin.
2	<b>WE.</b> Indicates the complement of the WE# output pin.
1	<b>Reserved.</b>
0	<b>MOT EN A.</b> Indicates the complement of the MOA# output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DSA#	WD F/F	RDATA F/F	WE F/F	DSD#	DSC#
DEFAULT	0	1	1	0	0	0	1	1

BIT	DESCRIPTION
7-6	<b>Reserved.</b>
5	<b>DSA#.</b> This bit indicates the status of the DSA# output pin.
4	<b>WD F/F.</b> Indicates the complement of the WD# output pin, which is latched on every rising edge of the WD# output pin.
3	<b>RDATA F/F.</b> Indicates the complement of the latched RDATA# output pin.
2	<b>WE F/F.</b> Indicates the complement of the latched WE# output pin.
1	<b>DSD#.</b> 0: Drive D has been selected. 1: Drive D has not been selected.
0	<b>Reserved.</b>

### 11.2.3 Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register that controls drive motors, drive selection, DRQ/IRQ enable, and FDC reset. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			MOTOR ENABLE A	DMA&INT ENABLE	FDC RESET	DRIVE SELECT	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	<b>Reserved.</b>
4	<b>MOTOR ENABLE A.</b> A logical 1 enables Motor A.
3	<b>DMA &amp; INT ENABLE.</b> A logical 1 enables DRQ/IRQ.
2	<b>FDC RESET.</b> Floppy Disk Controller Reset. A logical 0 resets the FDC.
1-0	<b>DRIVE SELECT.</b> <b>Bits</b> <b>1 0</b> 0 0: Select Drive A. 0 1: Select Drive B. 1 0: Select Drive C. 1 1: Select Drive D.

### 11.2.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information for the floppy disk drive.

In normal floppy mode, this register only has bits 0 and 1, and the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						Tape sel 1	Tape sel 0
DEFAULT	NA	NA	NA	NA	NA	NA	0	0

BIT	DESCRIPTION
7-2	RESERVED.
1	Tape sel 1.
0	Tape sel 0.

If the three-mode FDD function is enabled (EN3MODE = 1 in LD0 CRF0, Bit 0), the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Media ID1	Media ID0	Drive Type ID1	Drive Type ID0	Floppy Boot Drive 1	Floppy Boot Drive 0	Tape Sel 1	Tape Sel 0
DEFAULT	0	0	1	1	0	0	0	0

BIT	DESCRIPTION
7	Media ID1. Read only. Reflects the value of LD0, CRF1, bit 5.
6	Media ID0. Read only. Reflects the value of LD0, CRF1, bit 4.
5	Drive Type ID1.
4	Drive Type ID0.
3	Floppy Boot Drive 1. Reflects the value of LD0, CRF1, bit 7.
2	Floppy Boot Drive 0. Reflects the value of LD0, CRF1, bit 6.
1	Tape Sel 1.
0	Tape Sel 0.
Reflect the bit in LD0, CR[F2h]. Which bit is reflected depends on the last drive selected in the PO register.	
Assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved for the floppy disk boot drive.	

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

### 11.2.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RQM	DIO	Non-DMA mode	FDC Busy	RESERVED			FDD 0 Busy
DEFAULT	0	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	<b>Request for Master (RQM).</b> A high on this bit indicates Data Register is ready to send or receive data to or from the processor.
6	<b>DATA INPUT/OUTPUT (DIO).</b> If DIO = HIGH, then the transfer is from Data Register to the processor. If DIO = LOW, the transfer is from processor to Data Register.
5	<b>Non-DMA mode.</b> The FDC is in the non-DMA mode, this bit is set only during the execution phase in non-DMA mode.
4	<b>FDC Busy (CB).</b> A read or write command is in the process when CB = HIGH.
3-1	<b>Reserved.</b>
0	<b>FDD 0 Busy.</b> (DOB = 1) FDD number 0 is in the SEEK mode.

### 11.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. However, in PC-AT and PS/2 Model 30 and PS/2 modes, the data rate is controlled by the CC register, not by the DR register. As a result, the real data rate is determined by the most recent write to either the DR or CC register. The bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	S/W RESET	POWER DOWN	RESERVED	PRECOMP2	PRECOMP1	PRECOMP0	DRATE1	DRATE0
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7	<b>S/W RESET.</b> The software reset bit.
6	<b>POWER DOWN.</b> 0: FDC in normal mode. 1: FDC in power-down mode.
5	<b>RESERVED.</b>
4	<b>PRECOMP 2.</b>
3	<b>PRECOMP 1.</b>
2	<b>PRECOMP 0.</b>
Selects the value of write precompensation. The following tables show the precompensation values for every combination of these bits. Please see the tables below.	

BIT	DESCRIPTION	
1	<b>DRATE 1.</b>	Select the data rate of the FDC and reduced write-current control. <b>Bits</b> <b>1 0</b> 0 0: 500 KB/S (MFM), 250 KB/S (FM), RWC# = 1
0	<b>DRATE 0.</b>	0 1: 300 KB/S (MFM), 150 KB/S (FM), RWC# = 0 1 0: 250 KB/S (MFM), 125 KB/S (FM), RWC# = 0 1 1: 1 MB/S (MFM), Illegal (FM), RWC# = 1

The 2 MB/S data rate for the tape drive is only supported by setting DRATE1 and DRATE0 to 01, as well as setting DRT1 and DRT0 (CRF4 and CRF5 for logical device 0) to 10. Please see the functional description of CRF4 or CRF5 and the data rate table for individual data-rate settings.

PRECOMP	PRECOMPENSATION DELAY	
	250K - 1 Mbps	2 Mbps Tape drive
2 1 0	Default Delays	Default Delays
0 0 0	41.67 ns	20.8 ns
0 0 1	83.34 ns	41.17 ns
0 1 0	125.00 ns	62.5ns
0 1 1	166.67 ns	83.3 ns
1 0 0	208.33 ns	104.2 ns
1 0 1	250.00 ns	125.00 ns
1 1 0	0.00 ns (disabled)	0.00 ns (disabled)
1 1 1		

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 ns
300 KB/S	125 ns
500 KB/S	125 ns
1 MB/S	41.67ns
2 MB/S	20.8 ns

**11.2.7FIFO Register (R/W base address + 5)**

The FIFO register consists of four status registers in a stack, and only one register is presented to the data bus at a time. The FIFO register stores data, commands, and parameters, and it provides disk-drive status information. In addition, data bytes pass through the data register to program or obtain results after a command. In the W83667HG-A, this register is disabled after reset. The FIFO can enable it and change its values through the CONFIGURE command.

BIT	7	6	5	4	3	2	1	0
NAME	IC		SE	EC	NR	HD	US1, US0 Drive Select	

### Status Register 0 (ST0)

BIT	DESCRIPTION
7-6	<b>IC (Interrupt Code).</b> <b>Bits</b> <b>7 6</b> 0 0: Normal termination of the command. 0 1: Abnormal termination of the command. 1 0: Invalid command issue. 1 1: Abnormal termination because the ready signal from FDD changed state during command execution.
5	<b>SE (Seek End).</b> 1: Seek end. 0: Seek error.
4	<b>EC (Equipment Check).</b> 1: When a fault signal is received from the FDD or the track. 0: Signal fails to occur after 77 step pulses. 0: No error.
3	<b>NR (Not Ready).</b> 1: Drive is not ready. 0: Drive is ready.
2	<b>HD Head Address. (The current head address)</b> 1: Head selected. 0: Head selected.
1-0	<b>US 1, US0 Drive Select.</b> <b>Bits</b> <b>1 0</b> 0 0: Drive A selected. 0 1: Drive B selected. 1 0: Drive C selected. 1 1: Drive D selected.

### Status Register 1 (ST1)

BIT	7	6	5	4	3	2	1	0
NAME	EN	Not Used	OE	OR	Not Used	ND	NW	MAM

BIT	DESCRIPTION
7	<b>EN (End of Track).</b> 1 will be written to this bit if the FDC tries to access a sector beyond the final sector or a cylinder.
6	Not Used. This bit is always 0.
5	<b>DE (Data Error).</b> 1 will be written to this bit if the FDC detects a CRC error in either the ID field or the data field.
4	<b>OR (Over Run).</b> 1 will be written to this bit if the FDC is not served by the host system within a certain time interval during data transfer.

BIT	DESCRIPTION
3	Not Used. This bit is always 0.
2	<b>ND (No Data).</b> 1 will be written to this bit if the specified sector cannot be found during execution of a read, write or verify data.
1	<b>NW (Not Writable).</b> 1 will be written to this bit if a write protect signal is detected from the diskette drive during execution of write data.
0	<b>MAM (Missing Address Mark).</b> 1 will be written to this bit if the FDC cannot detect the data address mark or the data address mark has been deleted.

### Status Register 2 (ST2)

BIT	7	6	5	4	3	2	1	0
NAME	NOT USED	CM	DD	WC	SH	SN	BC	MD

BIT	DESCRIPTION
7	Not used. This bit is always 0.
6	<b>CM (Control Mark).</b> 1: During execution of the read data or scan command. 0: No error.
5	<b>DD (Data error in the Data field).</b> 1: If the FDC detects a CRC error in the data field. 0: No error.
4	<b>WC (Wrong Cylinder).</b> 1: Indicates wrong cylinder.
3	<b>SH (Scan Equal Hit).</b> 1: During execution of the Scan command, if the equal condition is satisfied. 0: No error.
2	<b>SN (Scan Not Satisfied).</b> 1: During execution of the Scan command. 0: No error.
1	<b>BC (Bad Cylinder).</b> 1: Bad Cylinder. 0: No error.
0	<b>MD (Missing Address Mark in Data Field).</b> 1: If FDC cannot find a data address mark (or the address mark has been deleted) when reading data from the media. 0: No error.

### Status Register 3 (ST3)

BIT	7	6	5	4	3	2	1	0
NAME	FT	WP	RY	TO	TS	HD	US1	US0

BIT	DESCRIPTION
7	<b>FT.</b> Fault.
6	<b>WP.</b> Write protected.
5	<b>RY.</b> Ready.
4	<b>TO.</b> Track 0.
3	<b>TS.</b> Two-side.
2	<b>HD.</b> Head Address.
1	<b>US1.</b> Unit Select 1.
0	<b>US0.</b> Unit Select 0.

### 11.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit, read-only register used for diagnostic purposes. In PC/XT or PC/AT mode, only bit 7 is checked by the BIOS. When the register is read, bit 7 shows the complement of DSKCHG#, while the other bits remain in tri-state. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0	
<b>NAME</b>	DSKCHG	RESERVED							
<b>DEFAULT</b>	0	NA	NA	NA	NA	NA	NA	NA	

BIT	DESCRIPTION
7	<b>DSKCHG.</b>
6-0	<b>RESERVED.</b> Reserved for the hard disk controller. During a read of this register, these bits are in tri-state.

In PS/2 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	DSKCHG	RESERVED				DRATE1	DRATE0	HIGH DENS#
<b>DEFAULT</b>	0	1	1	1	1	1	0	1

BIT	DESCRIPTION
7	<b>DSKCHG.</b> Indicates the complement of the DSKCHG# input.
6-3	<b>RESERVED.</b> Always 1 during a read.
2	<b>DRATE 1.</b>
1	<b>DRATE 0.</b>
0	<b>HIGHDENS#.</b>

Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 7)) for how the settings correspond to individual data rates.

BIT	DESCRIPTION
	0: 500 KB/S or 1 MB/S data rate (high-density FDD). 1: 250 KB/S or 300 KB/S data rate.

In PS/2 Model 30 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG#	RESERVED			DMAEN	NOPREC	DRATE1	DRATE0
DEFAULT	1	0	0	0	0	0	1	0

BIT	DESCRIPTION
7	<b>DSKCHG.</b> Indicates the status of the DSKCHG# input.
6-4	<b>RESERVED.</b> Always 0 during a read.
3	<b>DMAEN.</b> Indicates the value of DO register, bit 3.
2	<b>NOPREC.</b> Indicates the value of the NOPREC bit in the CC REGISTER.
1	<b>DRATE 1.</b>
0	<b>DRATE 0.</b>
Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address +7)) for how the settings correspond to individual data rates.	

### 11.2.9 Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In PC/AT and PS/2 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						DRATE1	DRATE0
DEFAULT	NA	NA	NA	NAN	NA	NA	1	0

BIT	DESCRIPTION
7-2	<b>RESERVED.</b> Should be set to 0.
1	<b>DRATE 1.</b>
0	<b>DRATE 0.</b>
Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address +7)) for how the settings correspond to individual data rates.	

In the PS/2 Model 30 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					NOPREC	DRATE1	DRATE0

DEFAULT	NA	NA	NA	NA	NA	0	1	0
---------	----	----	----	----	----	---	---	---

BIT	DESCRIPTION	
7-3	<b>RESERVED.</b> Should be set to 0.	
2	<b>NOPREC.</b> Disables the precompensation function. This bit can be set by the software.	
1	<b>DRATE1.</b>	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 7)) for how the settings correspond to individual data rates.
0	<b>DRATE0.</b>	

## 12. UART PORT

### 12.1.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	<b>BDLAB (Baud Rate Divisor Latch Access Bit).</b> When this bit is set to logic 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logic 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	<b>SSE (Set Silence Enable).</b> A logic 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.
5	<b>PBFE (Parity Bit Fixed Enable).</b> When PBE and PBFE of UCR are both set to logic 1, (1) if EPE is logic 1, the parity bit is logical 0 when transmitting and checking; (2) if EPE is logic 0, the parity bit is logical 1 when transmitting and checking.
4	<b>EPE (Even Parity Enable).</b> When PBE is set to logic 1, this bit counts the number of logic 1's in the data word bits and determines the parity bit. When this bit is set to logic 1, the parity bit is set to logic 1 if an even number of logic 1's are sent or checked. When the bit is set to logic 0, the parity bit is logic 1, if an odd number of logic 1's are sent or checked.
3	<b>PBE (Parity Bit Enable).</b> When this bit is set to logic 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.
2	<b>MSBE (Multiple Stop Bit Enable).</b> Defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logic 0, one stop bit is sent and checked. (2) If MSBE is set to logic 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logic 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.
1	<b>DLS1 (Data Length Select Bit 1).</b> Defines the number of data bits that are sent or checked in each serial character.
0	<b>DLS0 (Data Length Select Bit 0).</b> Defines the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits

DLS1	DLS0	DATA LENGTH
1	0	7 bits
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 12-1 Register Summary for UART

Register Address Base		Bit Number								
		0	1	2	3	4	5	6	7	
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable (PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

\*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.

\*\* : These bits are always 0 in 16450 Mode.

### 12.1.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RF EI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	<b>RF EI (RX FIFO Error Indication).</b> In 16450 mode, this bit is always set to logical 0. In 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop0bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	<b>TSRE (Transmitter Shift Register Empty).</b> In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	<b>TBRE (Transmitter Buffer Register Empty).</b> In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, and interrupt is generated to notify the CPU to write next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	<b>SBD (Silent Byte Detected).</b> This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	<b>NSER (No Stop Bit Error).</b> This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	<b>PBER (Parity Bit Error).</b> This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	<b>OER (Overrun Error).</b> This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	<b>RDR (RBR Data Ready).</b> This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

### 12.1.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	<b>Reserved.</b>
4	<b>Internal Loopback Enable.</b> When this bit is set to logic 1, the UART enters diagnostic mode, as follows: (1) SOUT is forced to logic 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) →DSR#, RTS ( bit 1 of HCR) →CTS#, Loopback RI input ( bit 2 of HCR) → RI# and IRQ enable ( bit 3 of HCR) →DCD#. Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.
3	<b>IRQ Enable.</b> The UART interrupt output is enabled by setting this bit to logic 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	<b>Loopback RI Input.</b> This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	<b>RTS (Request to Send).</b> This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	<b>DTR (Data Terminal Ready).</b> This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

### 12.1.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	<b>DCD (Data Carrier Detect).</b> This bit is the inverse of the DCD# input and is equivalent to bit 3 of HCR in Loopback mode.
6	<b>RI (Ring Indicator).</b> This bit is the inverse of the RI# input and is equivalent to bit 2 of HCR in Loopback mode.
5	<b>DSR (Data Set Ready).</b> This bit is the inverse of the DSR# input and is equivalent to bit 0

BIT	DESCRIPTION
	of HCR in Loopback mode.
4	<b>CTS (Clear to Send).</b> This bit is the inverse of the CTS# input and is equivalent to bit 1 of HCR in Loopback mode.
3	<b>TDCD (DCD# Toggling).</b> This bit indicates that the state of the DCD# pin has changed after HSR is read by the CPU.
2	<b>FERI (RI Falling Edge).</b> This bit indicates that the RI# pin has changed from low to high after HSR is read by the CPU.
1	<b>TDSR (DSR# Toggling).</b> This bit indicates that the state of the DSR# pin has changed after HSR is read by the CPU.
0	<b>TCTS (CTS# Toggling).</b> This bit indicates that the state of the CTS# pin has changed after HSR is read by the CPU.

### 12.1.5UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.

BIT	7	6	5	4	3	2	1	0
<b>NAME</b>	<b>MSB</b>	<b>LSB</b>	<b>RESERVED</b>		<b>DMA MODE SELECT</b>	<b>TRANSMITTER FIFO RESET</b>	<b>RECEIVER FIFO RESET</b>	<b>FIFO ENABLE</b>
<b>DEFAULT</b>	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION
7	<b>MSB (RX Interrupt Active Level).</b>
6	<b>LSB (RX Interrupt Active Level).</b>
5-4	<b>RESERVED.</b>
3	<b>DMS MODE SELECT.</b> When this bit is set to logic 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.
2	<b>TRANSMITTER FIFO RESET.</b> Setting this bit to logic 1 resets the TX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.
1	<b>RECEIVER FIFO RESET.</b> Setting this bit to logic 1 resets the RX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.
0	<b>FIFO ENABLE.</b> This bit enables 16550 (FIFO) mode. This bit should be set to logic 1 before other UFR bits are programmed.

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08

1	1	14
---	---	----

**12.1.6 Interrupt Status Register (ISR) (Read only)**

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED		RESERVED		INTERRUPT STATUS BIT 2	INTERRUPT STATUS BIT 1	INTERRUPT STATUS BIT 0	0 IF INTERRUPT PENDING
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	<b>FIFOS ENABLED.</b> Set to logical 1 when UFR, bit 0 = 1.
5-4	<b>RESERVED.</b>
3	<b>INTERRUPT STATUS BIT 2.</b> In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. Please see the table below.
2	<b>INTERRUPT STATUS BIT 1.</b>
1	<b>INTERRUPT STATUS BIT 0.</b>
0	<b>0 IF INTERRUPT PENDING.</b> This bit is logic 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER = 1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FER1 = 1 4. TDCD = 1	Read HSR

\*\* Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

### 12.1.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	RESERVED.
3	<b>EHSRI (Handshake Status Interrupt Enable).</b> Set this bit to logical 1 to enable the handshake status register interrupt.
2	<b>EUSRI (UART Receive Status Interrupt Enable).</b> Set this bit to logical 1 to enable the UART status register interrupt.
1	<b>ETBREI (TBR Empty Interrupt Enable).</b> Set this bit to logical 1 to enable the TBR empty interrupt.
0	<b>ERDRI (RBR Data Ready Interrupt Enable).</b> Set this bit to logical 1 to enable the RBR data ready interrupt.

### 12.1.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to ( $2^{16} - 1$ ). The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (CR0C, bits 7 and 6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER			
Pre-Div: 13 1.8461M Hz	Pre-Div: 1.0 24M Hz	Decimal divisor used to generate 16X clock	Error Percentage
50	650	<b>2304</b>	**
75	975	<b>1536</b>	**
110	1430	<b>1047</b>	0.18%
134.5	1478.5	<b>857</b>	0.099%
150	1950	<b>768</b>	**
300	3900	<b>384</b>	**
600	7800	<b>192</b>	**
1200	15600	<b>96</b>	**
1800	23400	<b>64</b>	**

BAUD RATE FROM DIFFERENT PRE-DIVIDER			
2000	26000	<b>58</b>	0.53%
2400	31200	<b>48</b>	**
3600	46800	<b>32</b>	**
4800	62400	<b>24</b>	**
7200	93600	<b>16</b>	**
9600	124800	<b>12</b>	**
19200	249600	<b>6</b>	**
38400	499200	<b>3</b>	**
57600	748800	<b>2</b>	**
115200	1497600	<b>1</b>	**

\*\* Unless specified, the error percentage for all of the baud rates is 0.16%.

Note: Pre-Divisor is determined by CRF0 of UART A and B.

#### 12.1.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

## 13. PARALLEL PORT

### 13.1 Printer Interface Logic

The W83667HG-A parallel port can be attached to devices that accept eight bits of parallel data at standard TTL level. The W83667HG-A supports the IBM XT/AT compatible parallel port (SPP), the bi-directional parallel port (BPP), the Enhanced Parallel Port (EPP), and the Extended Capabilities Parallel Port (ECP).

The following tables show the pin definitions for different modes of the parallel port.

Table 13-1 Pin Descriptions for SPP, EPP, and ECP Modes

HOST CONNECTOR	PIN NUMBER OF W83667HG-A	PIN ATTRIBUTE	SPP	EPP	ECP
1	36	O	Nstb	nWrite	nSTB, HostClk <sup>2</sup>
2-9	31-26, 24-23	I/O	PD<7:0>	PD<7:0>	PD<7:0>
10	22	I	nACK	Intr	nACK, PeriphClk <sup>2</sup>
11	21	I	BUSY	nWait	BUSY, PeriphAck <sup>2</sup>
12	19	I	PE	PE	PEerror, nAckReverse <sup>2</sup>
13	18	I	SLCT	Select	SLCT, Xflag <sup>2</sup>
14	35	O	Nafd	nDStrb	nAFD, HostAck <sup>2</sup>
15	34	I	nERR	nError	nFault <sup>1</sup> , nPeriphRequest <sup>2</sup>
16	33	O	Ninit	nInit	nINIT <sup>1</sup> , nReverseRqst <sup>2</sup>
17	32	O	nSLIN	nAstrb	nSLIN <sup>1</sup> , ECPMode <sup>2</sup>

Notes:

n<name > : Active Low

1. Compatible Mode

2. High Speed Mode

3. For more information, please refer to the IEEE 1284 standard.

HOST CONNECTOR	PIN NUMBER OF W83667HG-A	PIN ATTRIBUTE	SPP
1	36	O	nSTB
2	31	I/O	PD0
3	30	I/O	PD1
4	29	I/O	PD2
5	28	I/O	PD3
6	27	I/O	PD4
7	26	I/O	PD5
8	24	I/O	PD6
9	23	I/O	PD7
10	22	I	nACK
11	21	I	BUSY
12	19	I	PE
13	18	I	SLCT
14	35	O	nAFD

HOST CONNECTOR	PIN NUMBER OF W83667HG-A	PIN ATTRIBUTE	SPP
15	34	I	nERR
16	33	O	nINIT
17	32	O	nSLIN

### 13.2 Enhanced Parallel Port (EPP)

The following table lists the registers used in the EPP mode and identifies the bit map of the parallel port and EPP registers. Some of the registers are used in other modes as well.

Table 13-2 EPP Register Addresses

A2	A1	A0	REGISTER	NOTE
0	0	0	Data port (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

1. These registers are available in all modes.
2. These registers are available only in EPP mode.

Table 13-3 Address and Bit Map for SPP and EPP Modes

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	BUSY#	ACK#	PE	SLCT	ERROR#	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1	1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Each register (or pair of registers, in some cases) is discussed below.

#### 13.2.1 Data Port (Data Swapper)

The CPU reads the contents of the printer's data latch by reading the data port.

### 13.2.2 Printer Status Buffer

The CPU reads the printer status by reading the printer status buffer. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	BUSY#	ACK#	PE	SLCT	ERROR#	RESERVED		TMOUT
DEFAULT	NA	NA	NA	NA	NA	1	1	0

BIT	DESCRIPTION
7	<b>BUSY#.</b> This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.
6	<b>ACK#.</b> This bit represents the current state of the printer's ACK# signal. A logical 0 means the printer has received a character and is ready to accept another. Normally, this signal is active for approximately 5 $\mu$ s before BUSY# stops.
5	<b>PE.</b> A logical 1 means the printer has detected the end of paper.
4	<b>SLCT.</b> A logical 1 means the printer is selected.
3	<b>ERROR#.</b> A logical 0 means the printer has encountered an error condition.
2-1	<b>RESERVED.</b>
0	<b>TMOUT.</b> This bit is only valid in EPP mode. A logical 1 indicates that a 10- $\mu$ s time-out has occurred on the EPP bus; a logical 0 means that no time-out error has occurred. Writing a logical 1 to this bit clears the time-out status bit; writing a logical 0 has no effect.

### 13.2.3 Printer Control Latch and Printer Control Swapper

The CPU reads the contents of the printer control latch by reading the printer control swapper. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DIR	IRQ ENABLE	SLCT IN	INIT#	AUTO FD	STROBE
DEFAULT	1	1	NA	0	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	<b>RESERVED.</b> These two bits are always read as logical 1 and can be written.
5	<b>DIR (Direction Control Bit).</b> When this bit is logical 1, the parallel port is in the input mode (read). When it is logical 0, the parallel port is in the output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.
4	<b>IRQ ENABLE.</b> A logical 1 allows an interrupt to occur when ACK# changes from low to high.
3	<b>SLCT IN.</b> a logical 1 selects the printer.
2	<b>INIT#.</b> A logical 0 starts the printer (50 microsecond pulse, minimum).
1	<b>AUTO FD.</b> A logical 1 causes the printer to line-feed after a line is printed.

BIT	DESCRIPTION
0	<b>STROBE.</b> A logical 1 generates an active-high pulse for a minimum of 0.5 $\mu$ s to clock data into the printer. Valid data must be presented for a minimum of 0.5 $\mu$ s before and after the strobe pulse.

### 13.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

### 13.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. The bit definitions for each data port are the same and as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

When any EPP data port is accessed, the contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

### 13.2.6 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
NWrite	O	Denotes read or write operation for address or data.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
NWait	I	Inactivated to acknowledge that data transfer is complete. Activated to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer-select status; same as SPP mode.
NDStrb	O	This signal is active low. It denotes a data read or write operation.
Nerror	I	Error; same as SPP mode.
Ninits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
NAStrb	O	This signal is active low. It denotes an address read or write operation.

### 13.2.7 EPP Operation

When EPP mode is selected, the PDx bus is in standard or bi-directional mode when no EPP read, write, or address cycle is being executed. In this situation, all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10  $\mu$ S have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in status bit 0.

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

#### 13.2.7.1. EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

- a. If nWait is active low, the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, proceeds normally, and is completed when nWait goes inactive high.
- b. If nWait is inactive high, the read/write cycle cannot start. It must wait until nWait changes to active low, at which time it starts as described above.

### 13.2.7.2. EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it does not finish until nWait changes from active low to inactive high.

## 13.3 Extended Capabilities Parallel (ECP) Port

This port is software- and hardware-compatible with existing parallel ports, so the W83667HG-A parallel port may be used in standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host-to-peripheral) and reverse (peripheral-to-host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port hardware supports run-length-encoded (RLE) decompression. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. RLE compression is required; the hardware support is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

The W83667HG-A ECP supports the following modes.

Table 13-4 ECP Mode Description

MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CRF0h to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

The mode selection bits are bits 7-5 of the Extended Control Register.

### 13.3.1 ECP Register and Bit Map

The next two tables list the registers used in ECP mode and provide a bit map of the parallel port and ECP registers.

Table 13-5 ECP Register Addresses

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dSr	Base+001h	R	All	Status Register
dCr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR60 and 61, which are determined by configuration register or hardware setting.

Table 13-6 Bit Map of the ECP Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
Dsr	nBusy	nAck	PError	Select	nFault	1	1	1	1
Dcr	1	1	Directio	ackIntrEn	SelectIn	nIntr	Autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
Ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

Each register (or pair of registers, in some cases) is discussed below.

### 13.3.2 Data and ecpAFifo Port

Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input, and the contents of this register are output to PD0-PD7. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. This operation is defined only for the forward direction. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Address/RLE	Address or RLE						

### 13.3.3 Device Status Register (DSR)

These bits are logical 0 during a read of the Printer Status Register. The bits of this status register are defined as follows:

BIT	7	6	5	4	3	2	1	0
NAME	nBusy	nAck	PError	Select	nFault	1	1	1

BIT	DESCRIPTION
7	<b>nBusy.</b> This bit reflects the complement of the Busy input.
6	<b>nAck.</b> This bit reflects the nAck input.
5	<b>PError.</b> This bit reflects the PError input.
4	<b>Select.</b> This bit reflects the Select input.
3	<b>nFault.</b> This bit reflects the nFault input.
2-0	These three bits are not implemented and are always logical 1 during a read.

### 13.3.4 Device Control Register (DCR)

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Director	ackInEn	SelectIn	nInit	Autofd	Strobe
DEFAULT	1	1	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	<b>Reserved.</b> These two bits are always read as logical 1 and cannot be written.
5	<b>Director.</b> If the mode is 000 or 010, this bit has no effect and the direction is always out. In other modes, 0: The parallel port is in the output mode. 1: The parallel port is in the input mode.
4	<b>ackInEn</b> (Interrupt Request Enable). When this bit is set to logical 1, it enables interrupt requests from the parallel port to the CPU on the low-to-high transition on ACK#.
3	<b>SelectIn.</b> This bit is inverted and output to the SLIN# output. 0: The printer is not selected. 1: The printer is selected.
2	<b>nInit.</b> This bit is output to the INIT# output.
1	<b>Autofd.</b> This bit is inverted and output to the AFD# output.
0	<b>Strobe.</b> This bit is inverted and output to the STB# output.

### 13.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. Bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte-aligned.

### 13.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte-aligned.

When the direction bit is 1, data bytes from the peripheral are read via automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO return bytes of ECP data to the system.

### 13.3.7TFIFO (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO is not transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

### 13.3.8CNFGA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates that this is an 8-bit implementation.

### 13.3.9CNFGB (Configuration Register B) Mode = 111

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	COMPRESS	intrVALUE	IRQx2	IRQx1	IRQx0	RESERVED		
DEFAULT	0	0	0	0	0	1	1	1

BIT	DESCRIPTION																	
7	<b>Compress.</b> This bit is read-only. It is logical 0 during a read, which means that this chip does not support hardware RLE compression.																	
6	<b>intrValue.</b> Returns the value on the ISA IRQ line to determine possible conflicts.																	
5	<b>IRQx2.</b>	Reflects the IRQ resource assigned for ECP port.																
		<table border="1"> <thead> <tr> <th>cnfgB[5:3]</th> <th>IRQ resource</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Reflects other IRQ resources selected by PnP register (default)</td> </tr> <tr> <td>001</td> <td>IRQ7</td> </tr> <tr> <td>010</td> <td>IRQ9</td> </tr> <tr> <td>011</td> <td>IRQ10</td> </tr> <tr> <td>100</td> <td>IRQ11</td> </tr> <tr> <td>101</td> <td>IRQ14</td> </tr> <tr> <td>110</td> <td>IRQ15</td> </tr> <tr> <td>111</td> <td>IRQ5</td> </tr> </tbody> </table>	cnfgB[5:3]	IRQ resource	000	Reflects other IRQ resources selected by PnP register (default)	001	IRQ7	010	IRQ9	011	IRQ10	100	IRQ11	101	IRQ14	110	IRQ15
cnfgB[5:3]	IRQ resource																	
000	Reflects other IRQ resources selected by PnP register (default)																	
001	IRQ7																	
010	IRQ9																	
011	IRQ10																	
100	IRQ11																	
101	IRQ14																	
110	IRQ15																	
111	IRQ5																	
4	<b>IRQx1.</b>																	
3	<b>IRQx0.</b>																	
2-0	<b>Reserved.</b> These three bits are logical 1 during a read and can be written.																	

**13.3.10 ECR (Extended Control Register) Mode = all**

This register controls the extended ECP parallel port functions. The bit definitions are follows:

BIT	7	6	5	4	3	2	1	0
NAME	MODE			nErrIntrEn	dmaEn	ServiceIntr	Full	Empty
DEFAULT	0	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-5	<b>Mode.</b> Read/Write. These bits select the mode.
	000 Standard Parallel Port (SPP) mode. The FIFO is reset in this mode.
	001 PS/2 Parallel Port mode. This is the same as SPP mode except that direction may be used to tri-state the data lines. Furthermore, reading the data register returns the value on the data lines, not the value in the data register.
	010 Parallel Port FIFO mode. This is the same as SPP mode except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.
	011 ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral using the ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
	100 EPP Mode. EPP mode is activated if the EPP mode is selected.
	101 Reserved.
	110 Test Mode. The FIFO may be written and read in this mode, but the data is not transmitted on the parallel port.
111 Configuration Mode. The configA and configB registers are accessible at 0x400 and 0x401 in this mode.	
4	<b>nErrIntrEn.</b> Read/Write (Valid only in ECP Mode) 0: Enables the interrupt generated on the falling edge of nFault. This prevents interrupts from being lost in the time between the read of the ECR and the write of the ECR. 1: Disables the interrupt generated on the asserting edge of nFault.
3	<b>dmaEn.</b> Read/Write. 0: Disable DMA unconditionally. 1: Enable DMA.
2	<b>serviceIntr.</b> Read/Write. 0: Enable one of the following cases of interrupts. When one of the serviced interrupts occurs, this bit is set to logical 1 by the hardware. This bit must be reset to logical 0 to re-enable the interrupts. (a) dmaEn = 1: During DMA, this bit is set to logical 1 when terminal count is reached. (b) dmaEn = 0, direction = 0: This bit is set to logical 1 whenever there are writeIntr threshold or more bytes free in the FIFO. (c) dmaEn = 0, direction = 1: This bit is set to logical 1 whenever there are readIntr threshold or more valid bytes to be read from the FIFO. 1: Disable DMA and all of the service interrupts. Writing a logical 1 to this bit does not

BIT	DESCRIPTION
	cause an interrupt.
1	<b>Full.</b> Read Only. 0: The FIFO has at least one free byte. 1: The FIFO is completely full; it cannot accept another byte.
0	<b>Empty.</b> Read Only. 0: The FIFO contains at least one byte of data. 1: The FIFO is completely empty.

### 13.3.11 ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
NStrobe (HostClk)	O	This pin loads data or address into the slave on its asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contain address, data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. In the reverse direction, it indicates whether the data lines contain ECP command information or data. Normal data are transferred when Busy (PeriphAck) is high, and an 8-bit command is transferred when it is low.
PError (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on-line.
NautoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. In the forward direction, this signal indicates whether the data lines contain ECP address or data. Normal data are transferred when nAutoFd (HostAck) is high, and an 8-bit command is transferred when it is low.
nFault (nPeriphReuqest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

### 13.3.12 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits.

- (a) Set direction = 0, enabling the drivers.
- (b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.
- (c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.
- (d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

#### 13.3.12.1. Mode Switching

The software must handle P1284 negotiation and all operations prior to a data transfer in SPP or PS/2 modes (000 or 001). The hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port, only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

In extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode, the software should wait for all the data to be read from the FIFO before changing back to mode 000 or 001.

#### 13.3.12.2. Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high, and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high, and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

#### 13.3.12.3. Data Compression

The W83667HG-A hardware supports RLE decompression and can transfer compressed data to a peripheral. Odd (RLE) compression is not supported in the hardware, however. In order to transfer data in ECP mode, the compression count is written to ecpAFifo and the data byte is written to ecpDFifo.

### 13.3.13 FIFO Operation

The FIFO threshold is set in CR5. All data transferred to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used in Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

### 13.3.14 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA empties or fills the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated, and serviceIntr is asserted, which will disable the DMA.

### 13.3.15 Programmed I/O (NON-DMA) Mode

The ECP and parallel port FIFOs can also be operated using interrupt-driven, programmed I/O. Programmed I/O transfers are

1. To the ecpDFifo at 400H and ecpAFifo at 000H
2. From the ecpDFifo located at 400H
3. To / from the tFifo at 400H.

The host must set dmaEn and serviceIntr to 0 and also must set the direction and state accordingly in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O empties or fills the FIFO using the appropriate direction and mode.

### 14. KEYBOARD CONTROLLER

The W83667HG-A KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

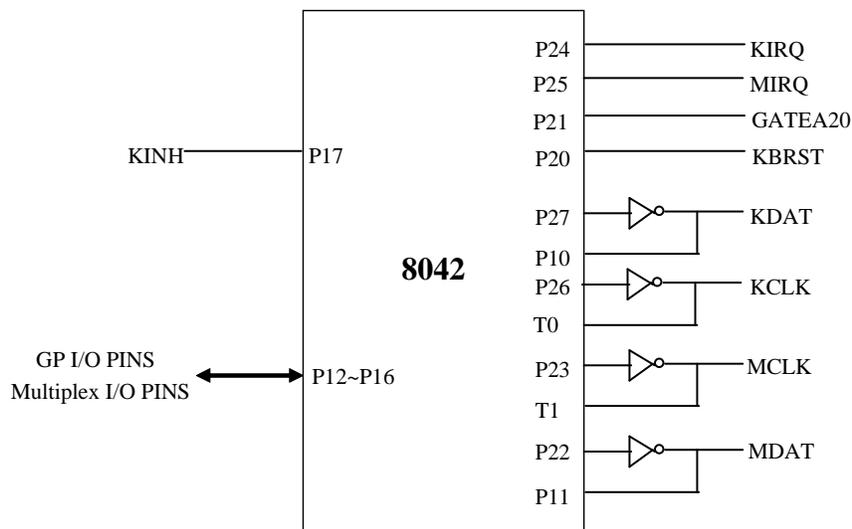


Figure 14-1 Keyboard and Mouse Interface

#### 14.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

#### 14.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

### 14.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

Table 14-1 Bit Map of Status Register

<b>BIT</b>	<b>BUT FUNCTION</b>	<b>DESCRIPTION</b>
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

14.4 Commands

Table 14-2 KBC Command Sets

COMMAND	FUNCTION																		
20h	Read Command Byte of Keyboard Controller																		
60h	Write Command Byte of Keyboard Controller <table border="1" data-bbox="570 600 1156 972"> <thead> <tr> <th>BIT</th> <th>BIT DEFINITION</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>Reserved</td> </tr> <tr> <td>6</td> <td>IBM Keyboard Translate Mode</td> </tr> <tr> <td>5</td> <td>Disable Auxiliary Device</td> </tr> <tr> <td>4</td> <td>Disable Keyboard</td> </tr> <tr> <td>3</td> <td>Reserve</td> </tr> <tr> <td>2</td> <td>System Flag</td> </tr> <tr> <td>1</td> <td>Enable Auxiliary Interrupt</td> </tr> <tr> <td>0</td> <td>Enable Keyboard Interrupt</td> </tr> </tbody> </table>	BIT	BIT DEFINITION	7	Reserved	6	IBM Keyboard Translate Mode	5	Disable Auxiliary Device	4	Disable Keyboard	3	Reserve	2	System Flag	1	Enable Auxiliary Interrupt	0	Enable Keyboard Interrupt
BIT	BIT DEFINITION																		
7	Reserved																		
6	IBM Keyboard Translate Mode																		
5	Disable Auxiliary Device																		
4	Disable Keyboard																		
3	Reserve																		
2	System Flag																		
1	Enable Auxiliary Interrupt																		
0	Enable Keyboard Interrupt																		
A4h	Test Password Returns 0Fah if Password is loaded Returns 0F1h if Password is not loaded																		
A5h	Load Password Load Password until a logical 0 is received from the system																		
A6h	Enable Password Enable the checking of keystrokes for a match with the password																		
A7h	Disable Auxiliary Device Interface																		
A8h	Enable Auxiliary Device Interface																		
A9h	Interface Test <table border="1" data-bbox="570 1371 1214 1608"> <thead> <tr> <th>BIT</th> <th>BIT DEFINITION</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>No Error Detected</td> </tr> <tr> <td>01</td> <td>Auxiliary Device "Clock" line is stuck low</td> </tr> <tr> <td>02</td> <td>Auxiliary Device "Clock" line is stuck high</td> </tr> <tr> <td>03</td> <td>Auxiliary Device "Data" line is stuck low</td> </tr> <tr> <td>04</td> <td>Auxiliary Device "Data" line is stuck low</td> </tr> </tbody> </table>	BIT	BIT DEFINITION	00	No Error Detected	01	Auxiliary Device "Clock" line is stuck low	02	Auxiliary Device "Clock" line is stuck high	03	Auxiliary Device "Data" line is stuck low	04	Auxiliary Device "Data" line is stuck low						
BIT	BIT DEFINITION																		
00	No Error Detected																		
01	Auxiliary Device "Clock" line is stuck low																		
02	Auxiliary Device "Clock" line is stuck high																		
03	Auxiliary Device "Data" line is stuck low																		
04	Auxiliary Device "Data" line is stuck low																		
AAh	Self-test Returns 055h if self-test succeeds																		

COMMAND	FUNCTION												
ABh	Interface Test <table border="1" data-bbox="565 373 1247 611"> <thead> <tr> <th>BIT</th> <th>BIT DEFINITION</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>No Error Detected</td> </tr> <tr> <td>01</td> <td>Keyboard "Clock" line is stuck low</td> </tr> <tr> <td>02</td> <td>Keyboard "Clock" line is stuck high</td> </tr> <tr> <td>03</td> <td>Keyboard "Data" line is stuck low</td> </tr> <tr> <td>04</td> <td>Keyboard "Data" line is stuck high</td> </tr> </tbody> </table>	BIT	BIT DEFINITION	00	No Error Detected	01	Keyboard "Clock" line is stuck low	02	Keyboard "Clock" line is stuck high	03	Keyboard "Data" line is stuck low	04	Keyboard "Data" line is stuck high
BIT	BIT DEFINITION												
00	No Error Detected												
01	Keyboard "Clock" line is stuck low												
02	Keyboard "Clock" line is stuck high												
03	Keyboard "Data" line is stuck low												
04	Keyboard "Data" line is stuck high												
ADh	Disable Keyboard Interface												
A Eh	Enable Keyboard Interface												
C0h	Read Input Port (P1) and send data to the system												
C1h	Continuously puts the lower four bits of Port1 into the STATUS register												
C2h	Continuously puts the upper four bits of Port1 into the STATUS register												
D0h	Send Port 2 value to the system												
D1h	Only set / reset GateA20 line based on system data bit 1												
D2h	Send data back to the system as if it came from the Keyboard												
D3h	Send data back to the system as if it came from Auxiliary Device												
D4h	Output next received byte of data from system to Auxiliary Device												
E0h	Reports the status of the test inputs												
FXh	Pulse only RC (the reset line) low for 6 $\mu$ s if the Command byte is even												

### 14.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

#### 14.5.1KB Control Register (Logic Device 5, CR-F0)

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	RESERVED			P92EN	HGA20	HKBRST#
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	<b>KCLKS1.</b>	Select the KBC clock rate. <b>Bits</b> <b>7 6</b> 0 0: Reserved. 0 1: Reserved.
6	<b>KCLKS0.</b>	1 0: KBC clock input is 12 MHz. 1 1: Reserved.
5-3	<b>RESERVED.</b>	
2	<b>P92EN (Port 92 Enable).</b> 1: Enables Port 92 to control GATEA20 and KBRESET. 0: Disables Port 92 functions.	
1	<b>HGA20 (Hardware GATEA 20).</b> 1: Selects hardware GATE A20 control logic to control GATE A20 signal. 0: Disables GATEA20 control logic functions.	
0	<b>HKBRST# (Hardware Keyboard Reset).</b> 1: Selects hardware KB RESET control logic to control KBRESET signal. 0: Disables hardware KB RESET control logic function.	

When the KBC receives data that follows a "D1" command, the hardware control logic sets or clears GATE A20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an "FE" command, the KBRESET is pulse low for 6  $\mu$ s (Min.) with a 14  $\mu$ s (Min.) delay.

GATE A20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATE A20 and KBRESET are merged with Port92 when the P92EN bit is set.

## 14.5.2Port 92 Control Register (Default Value = 0x24)

BIT	7	6	5	4	3	2	1	0
NAME	RES. (0)		RES. (1)	RES. (0)		RES. (1)	SGA20	PLKBRST#
DEFAULT	0	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-6	RES. (0)
5	RES. (1)
4-3	RES. (0)
2	RES. (1)
1	<b>SGA20 (Special GATE A20 Control)</b> 1: Drives GATE A20 signal to high. 0: Drives GATE A20 signal to low.
0	<b>PLKBRST# (Pulled-low KBRESET).</b> A logical 1 on this bit causes KBRESET to drive low for 6 $\mu$ S(Min.) with a 14 $\mu$ S(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

## 15. POWER MANAGEMENT EVENT

The PME# (pin 65) signal is connected to the South Bridge and is used to wake up the system from S1 ~ S5 sleeping states.

One control bit and four registers in the W83667HG-A are associated with the PME function. The control bit is at Logical Device A, CR[F2h], bit[0] and is for enabling or disabling the PME function. If this bit is set to "0", the W83667HG-A won't output any PME signal when any of the wake-up events has occurred and is enabled. The four registers are divided into PME status registers and PME interrupt registers of wake-up events <sup>Note.1</sup>.

- 1) The PME status registers of wake-up event:
  - At Logical Device A, CR[F3h] and CR[F4h]
  - Each wake-up event has its own status
  - The PME status should be cleared by writing a "1" before enabling its corresponding bit in the PME interrupt registers
- 2) The PME interrupt registers of wake-up event:
  - At Logical Device A, CR[F6h] and CR[F7h]
  - Each wake-up event can be enabled / disabled individually to generate a PME# signal

Note.1 PME wake-up events that the W83667HG-A supports include:

- Mouse IRQ event\*
- Keyboard IRQ event\*
- Printer IRQ event
- Floppy IRQ event
- UART A IRQ event
- UART B IRQ event
- Hardware Monitor IRQ event
- WDTO# event
- RIB (UARTB Ring Indicator) event

Note.2 All the above support both S0 and S1 states. Events with the "\*" mark also support S3 and S5 states.

### 15.1 Power Control Logic

This chapter describes how the W83667HG-A implements its ACPI function via these power control pins: PSIN# (Pin 61), PSOUT# (Pin 60), SUSB# (i.e. SLP\_S3#; Pin 64) and PSON# (Pin 63). The following figure illustrates the relationships.

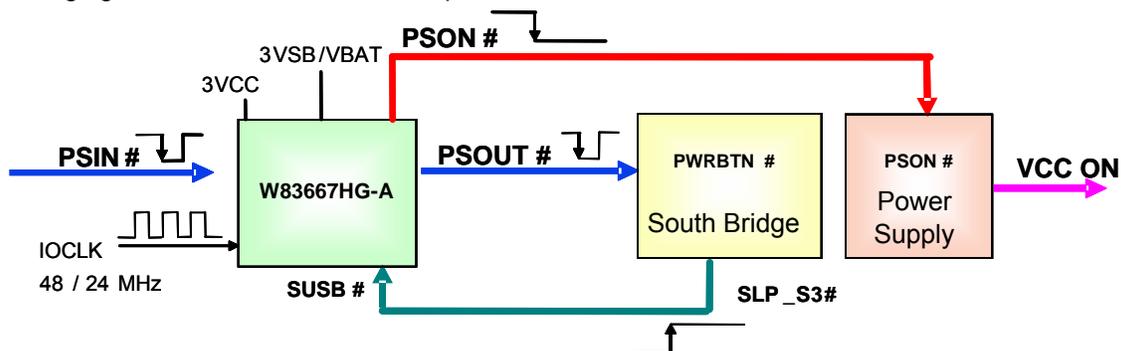


Figure 15-1 Power Control Mechanism

**15.1.1 PSON# Logic**

**15.1.1.1. Normal Operation**

The PSOUT# signal will be asserted low if the PSIN# signal is asserted low. The PSOUT# signal is held low for as long as the PSIN# is held low. The South Bridge controls the SUSB# signal through the PSOUT# signal. The PSON# is directly connected to the power supply to turn on or off the power.

Figure 15.2 shows the power on and off sequences.

The ACPI state changes from S5 to S0, then to S5

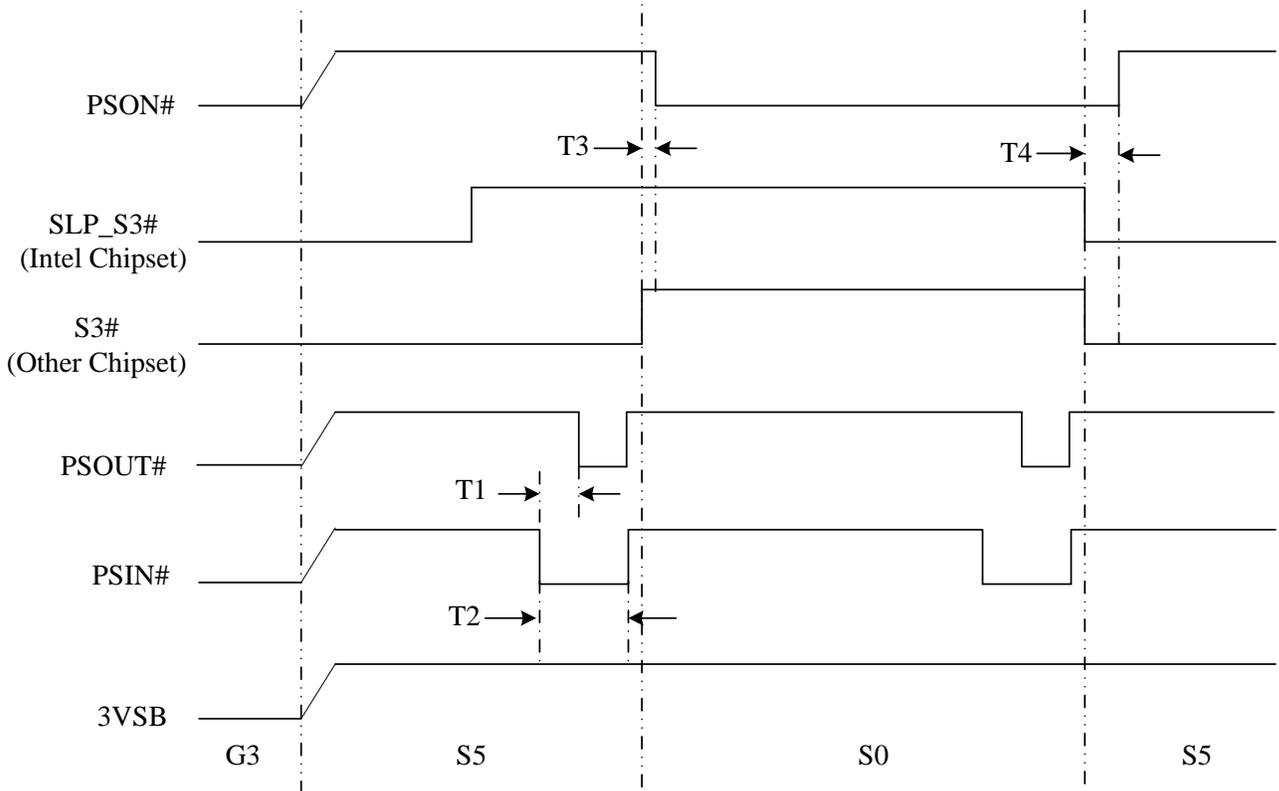


Figure 15-2 Power Sequence from S5 to S0, then Back to S5

**15.1.2 AC Power Failure Resume**

By definition, AC power failure means that the standby power is removed. The power failure resume control logic of the W83667HG-A is used to recover the system to a pre-defined state after AC power failure. Two control bits at Logical Device A, CR[E4h], bits[6:5] indicate the pre-defined state. The definition of these two bits is listed in the following table:

Table 15-1 Bit Map of Logical Device A, CR[E4h], Bits[6:5]

LOGICAL DEVICE A, CR[E4H], BITS[6:5]	DEFINITION
00	System always turns off when it returns from AC power failure
01	System always turns on when it returns from AC power failure
10	System turns off / on when it returns from power failure depending on the state before the power failure. (Please see Note 1)
11	User define the state before the power failure. (The previous state is set at CRE6[4]. Please see Note 2)

Note1. The W83667HG-A detects the state before power failure (on or off) through the SUSB# signal and the 3VCC power. The relation is illustrated in the following two figures.

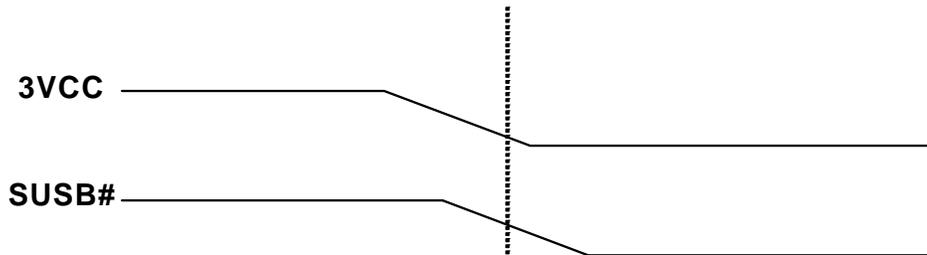


Figure 15-3 The previous state is "on".  
3VCC falls to 2.6V and SUSB# keeps at 2.0V.

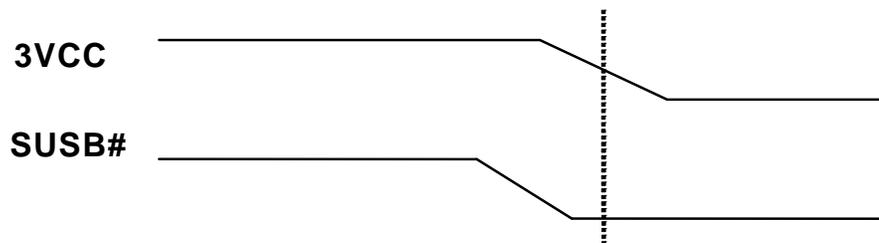


Figure 15-4 The previous state is "off".  
3VCC falls to 2.6V and SUSB# keeps at 0.8V.

Note 2.

Logical Device A, CR[E6h] bit [4]	Definition
0	User define the state to be "on"
1	User define the state to be "off"

To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the W83667HG-A adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be "On" or "Off". According to this setting, the system is returned to the pre-defined state after the AC power recovery.

## 15.2 Wake Up the System by Keyboard and Mouse

The W83667HG-A generates a low pulse through the PSOUT# pin to wake up the system when it detects a key code pressed or mouse button clicked. The following sections describe how the W83667HG-A works.

### 15.2.1 Waken up by Keyboard events

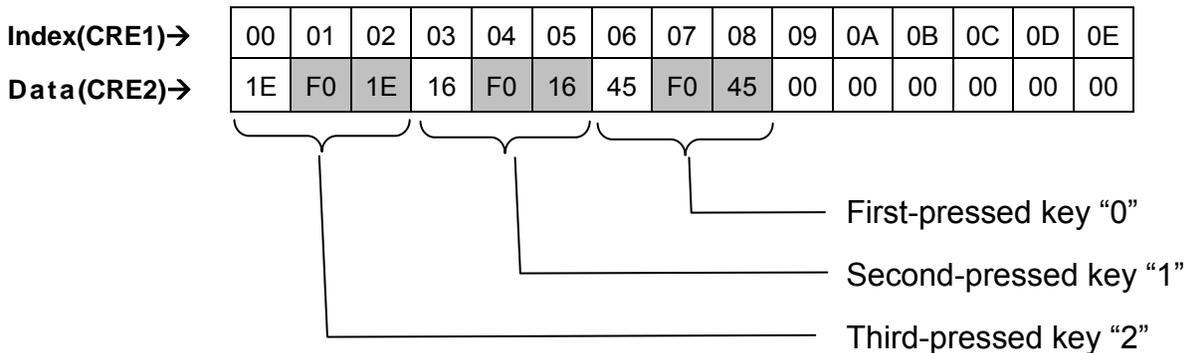
The keyboard Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 6 to "1".

There are two keyboard events can be used for the wake-up

- 1) Any key – Set bit 0 at Logical Device A, CR[E0h] to "1" (Default).
- 2) Specific keys (Password) - Set bit 0 at Logical Device A, CR[E0h] to "0".

Three sets of specific key combinations are stored at Logical Device A. CR[E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh, 0x30h ~ 0x3Eh, 0x40h ~ 0x4Eh) is going to be read or written through CR[E2h]. According to IBM 101/102 keyboard specification, a complete key code contains a 1-byte make code and a 2-byte break code. For example, the make code of "0" is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set "012" as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.



### 15.2.2 Waken up by Mouse events

The mouse Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 5 to "1".

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT\_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

Table 15-2 Definitions of Mouse Wake-Up Events

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any movement.
1	x	0	One click of the left or right button.
0	0	1	One click of the left button.
0	1	1	One click of the right button.
0	0	0	Two clicks of the left button.
0	1	0	Two clicks of the right button.

### 15.3 Resume Reset Logic

The RSMRST# (Pin 101) signal is a reset output and is used as the VSB power on reset signal for the South Bridge.

When the W83667HG-A detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in Figure 16-3 and Table 16-3.

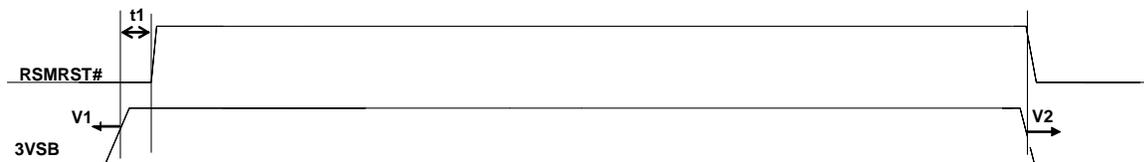


Figure 15-5 Mechanism of Resume Reset Logic

NAME	PARAMETER	MIN.	MAX.	UNIT
V1	3VSB Valid Voltage	-	3.0	V
V2	3VSB Ineffective Voltage	2.4	-	V
t1	Valid 3VSB to RSMRST# inactive	100	200	mS

Table 15-3 Timing and Voltage Parameters of RSMRST#

## 16. SERIALIZED IRQ

The W83667HG-A supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

### 16.1 Start Frame

There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the W83667HG-A drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the W83667HG-A from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.

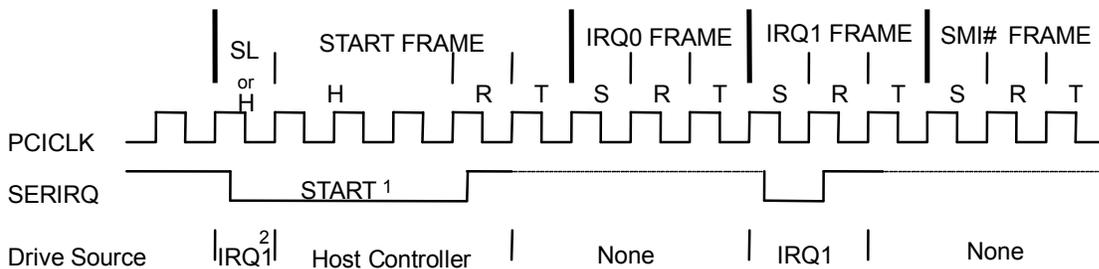


Figure 16-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1

H=Host Control      SL=Slave Control      R=Recovery      T=Turn-around      S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the W83667HG-A because IRQ1 of the W83667HG-A needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

## 16.2 IRQ/Data Frame

Once the Start Frame has been initiated, the W83667HG-A must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the W83667HG-A drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the W83667HG-A device drives the SERIRQ high. During the Turn-around phase, the W83667HG-A device leaves the SERIRQ tri-stated. The W83667HG-A starts to drive the SERIRQ line from the beginning of "IRQ0 FRAME" based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 15.1.

Table 16-1 SERIRQ Sampling Periods

SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	SIGNAL SAMPLED	# OF CLOCKS PAST START	EMPLOYED BY
1	IRQ0	2	Reserved
2	IRQ1	5	Keyboard
3	SMI#	8	H/W Monitor & SMI
4	IRQ3	11	UART B
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	FDC
8	IRQ7	23	LPT
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

### 16.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminate SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.

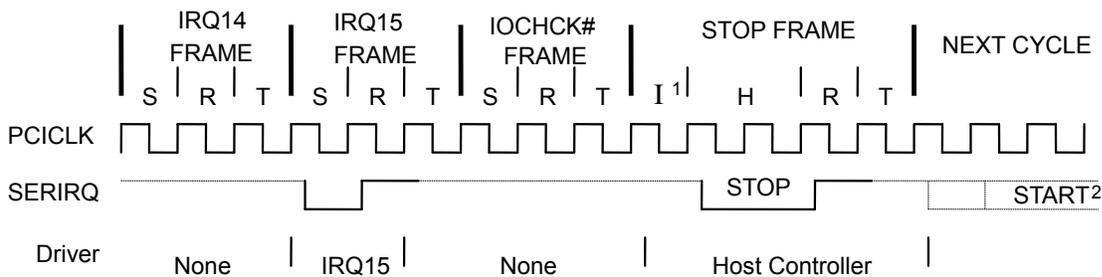


Figure 16-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period

H=Host Control      R=Recovery      T=Turn-around      S=Sample      I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

## 17. WATCHDOG TIMER

### 17.1 WDTO

The Watchdog Timer of the W83667HG-A consists of an 8-bit programmable time-out counter, a control register and a status register. The time-out counter ranges from 1 to 255 minutes in the minute mode, or 1 to 255 seconds in the second mode. The units of Watchdog Timer counter are selected at Logical Device 8, CR[F5h], bit[3]. The time-out value is set at Logical Device 8, CR[F6h]. Writing a value of zero to disable Watchdog-Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog-Timer counter and start counting down.

There are also 7 pins can select to WDTO# event route, which include PWROK0(Pin82), PWROK1(Pin47), PWROK2(Pin42), GP40(Pin74), GP42(Pin72), GP44(Pin70) and GP46(Pin68).

When WDTO# event is occurring, PWROK0, PWROK1 or PWROK2 will trigger a low pulse approx 100mS. And if setting GP46, GP44, GP42 or GP40 to WDTO# event route, when WDTO# event is occurring, GP46, GP44, GP42 or GP40 will trigger a high to low level till WDTO# event is cleared.

### 17.2 VID/BUSSEL's WDTO

The VID/BUSSEL's WDTO is useful only when ASUS function is enabled. And this time-out event is only working during LRESET#(Pin26) is low. The VID/BUSSEL's WDTO is default disabled, BIOS need to set the relative register in advance when using it. Once the VID/BUSSEL's WDTO event occurring, PWROK0~2 can set to the WDTO event route that will trigger a low pulse approx 100mS from each PWROK pin.

## 18. GENERAL PURPOSE I/O

The W83667HG-A provides 40 input/output ports that can be individually configured to perform a simple basic I/O function or alternative, pre-defined function. GPIO port 6 is configured through control registers in logical device 7, and GPIO port 2 ~ 5 in logical device 9. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non -inverse, 1 = inverse). Port value is read/written through data register.

In addition, only GP37, GP50, and GP53 are designed to be able to assert PSOUT# or PME# signal to wake up the system if any of them has any transitions. There are about 16mS debounced circuit inside these 3 GPIOs and it can be disabled by programming respective bit (LD9, CR[FEh] bit 4~6). Users can set what kind of event type, level or edge, and polarity, rising or falling, to perform the wake-up function. The following table gives more detailed register map on GP37, GP50 and GP53.

Table 18-1 Relative Control Registers of GPIO 37, 50 and 53 that Support Wake-Up Function

	<b>EVENTROUTE I (PSOUT#)</b>  <b>0: DISABLE 1: ENABLE</b>	<b>EVENTROUTE II (PME#)</b>  <b>0: DISABLE 1: ENABLE</b>	<b>EVENT DEBOUNCED</b>  <b>0 : ENABLE 1 : DISABLE</b>	<b>EVENT TYPE</b>  <b>0 : EDGE 1: LEVEL</b>	<b>EVENT POLARITY</b>  <b>0 : RISING 1 : FALLING</b>	<b>EVENT STATUS</b>
<b>GP37</b>	LDA, CR[FEh] Bit6	LDA, CR[FEh] Bit2	LD9, CR[FEh] Bit6	LD9, CR[FEh] Bit2	LD9, CR[E6h] Bit7	LD9, CR[E7h] Bit7
<b>GP50</b>	LDA, CR[FEh] Bit4	LDA, CR[FEh] Bit0	LD9, CR[FEh] Bit4	LD9, CR[FEh] Bit0	LD9, CR[F6h] Bit0	LD9, CR[F7h] Bit0
<b>GP53</b>	LDA, CR[FEh] Bit5	LDA, CR[FEh] Bit1	LD9, CR[FEh] Bit5	LD9, CR[FEh] Bit1	LD9, CR[F6h] Bit3	LD9, CR[F7h] Bit3

## 19. VID INPUTS AND OUTPUTS

The W83667HG-A provides individual eight pins for VID input and output function. These pins can be configured by setting Logical Device D, CR [E0h] to CR [E4h]. The configuration is applied to four modes, By-pass mode, Manual mode, Offset mode, and Maximum mode. More details can refer to Logical Device D, CR [E0h] to CR [E4h].

VID operation mode
by-pass mode (default)
offset markup
manual mode
max (manual, VID_IN)

Tables	volt/step
AMD 5-bit	25 mV
AMD 6-bit	25 mV
VRM 10.1 (6-bit)	12.5 mV
VRM 10.2 (7-bit)	6.25 mV
VRM 11.0 (8-bit) (default)	6.25 mV

### 19.1 VID Input Detection

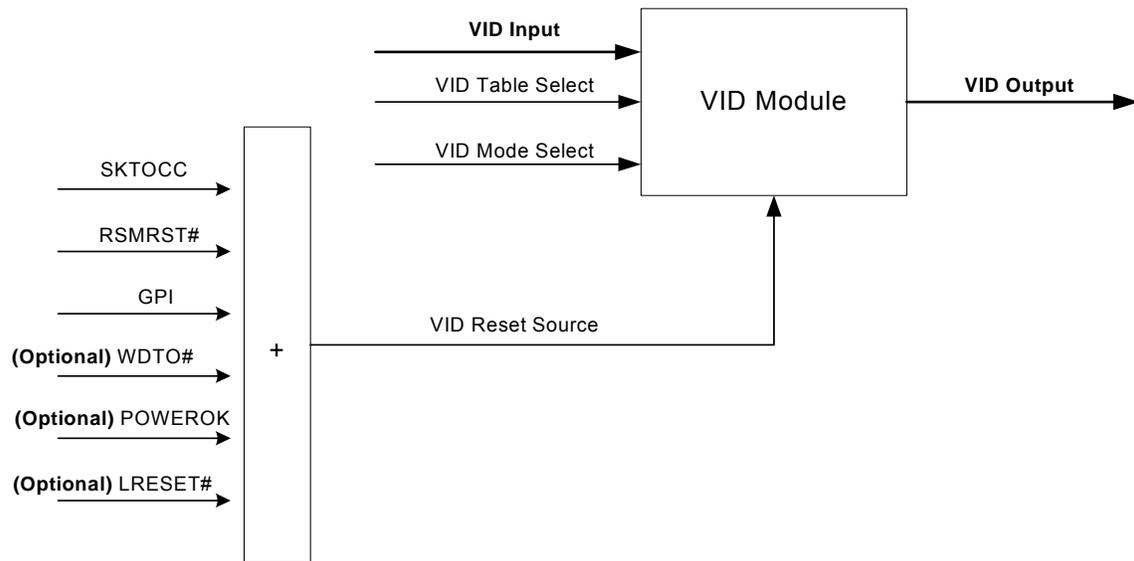
The W83667HG-A supports Intel VRM 9/10/11 and AMD VRM VID detections. VID input level is design for both GTL and AMD DC specification. The transition point is at 0.7V ~ 0.8V.

### 19.2 VID Output Control

The output type of the eight VID pins is open-drain stage. The output data can be read in the data register (Logical Device D, CR[E2h], bit 7 ~ 0).

### 19.3 VID Reset Source

The reset source is illustrated below. SKTOCC and RSMRST# are always effective. WDTO#, POWEROK and LRESET# are optional and can be enable/disable by the respective mask registers.



## 20. PCI RESET BUFFERS

The W83667HG-A has three copies of LRESET# output buffers. LRESET# is LPC Interface Reset, to which PCI Reset is connected. The three copies of LRESET# in the W83667HG-A are designated RSTOUT0#, RSTOUT1#, RSTOUT2#. All of them are powered by a 3VSB power.

RSTOUT0# is an open-drain output buffer of LRESET#. This signal needs an external pulled-up resistor of 3.3V or 5V.

RSTOUT1#, RSTOUT2# are push-pull output buffers of LRESET#. Each of them outputs 3.3V, voltage and the state is low when the 3VSB power is the only power source.

## 21. CONFIGURATION REGISTER

### 21.1 Chip (Global) Control Register

#### CR 02h. (Software Reset; Write Only)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	Write "1" Only	Software RESET.

#### CR 07h. (Logical Device; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Logical Device Number.

#### CR 20h. (Chip ID, High Byte; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = B3h (high byte).

#### CR 21h. (Chip ID, Low Byte; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = 5Xh (low byte). X is the IC version 51h: A Version. 52h: B Version. 53h: C Version. .....

#### CR 22h. (Device Power Down; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	HM Power Down. 0: Powered down. 1: Not powered down.
5	R / W	UARTB Power Down. 0: Powered down. 1: Not powered down.
4	R / W	UARTA Power Down. 0: Powered down. 1: Not powered down.
3	R / W	PRT Power Down. 0: Powered down. 1: Not powered down.
2~1	Reserved.	
0	R / W	FDC Power Down. 0: Powered down. 1: Not powered down.

#### CR 23h. (IPD; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	

BIT	READ / WRITE	DESCRIPTION
0	R / W	IPD (Immediate Power Down). When set to 1, the whole chip is put into power-down mode immediately.

**CR 24h. (Global Option; Default 0100\_00s0b)**

s: value by strapping

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved
6	R / W	CLKSEL => Input clock rate selection = 0 The clock input on pin 18 is 24 MHz. = 1 The clock input on pin 18 is 48 MHz. (Default)
5	R / W	Select output type of AUXFANOUT =0 AUXFANOUT is Push-pull. (Default) =1 AUXFANOUT is Open-drain.
4	R / W	Select output type of SYSFANOUT =0 SYSFANOUT is Open-drain. (Default) =1 SYSFANOUT is Push-pull.
3	R / W	Select output type of CPUFANOUT =0 CPUFANOUT is Open-drain. (Default) =1 CPUFANOUT is Push-pull.
2	Read Only	Reserved. (Always read low.)
1	R / W	ENROM => Enable Serial Peripheral Interface (Pin 94, Pin 95, Pin 97, Pin98) = 0 ROM is disabled after hardware reset. = 1 ROM is enabled after hardware reset. This bit is set or reset by a power-on strapping pin (Pin 32, DTRA#).
0	R / W	PNPCVS => = 0 The compatible PNP address-select registers have default values. = 1 The compatible PNP address-select registers have no default values.

**CR 25h. (Interface Tri-state Enable; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W	UARTBTRI
4	R / W	UARTATRI
3	R / W	PRTTRI
2~1	Reserved.	
0	R / W	FDCTRI.

**CR 26h. (Global Option; Default 0s000000b)** s: value by strapping

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA# (Pin 31).
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4	Reserved.	
3	R / W	DSFDLGRQ => = 0 Enable FDC legacy mode for IRQ and DRQ selection. Then DO register (base address + 2) bit 3 is effective when selecting IRQ. = 1 Disable FDC legacy mode for IRQ and DRQ selection. Then DO register (base address + 2) bit 3 is not effective when selecting IRQ.
2	R / W	DSPRLGRQ => = 0 Enable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is effective when selecting IRQ. = 1 Disable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is not effective when selecting IRQ.
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
0	R / W	DSUBLGRQ => = 0 Enable UART B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

**CR 27h. (Global Option; Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.
6	R / W	Pin 96 Function select 0: GP25 1: AUXFANIN1 (Default)
5	R / W	Pin 95 Function select 0: GP26 (If CR24 bit1 is logic 0) SPI function, SCK# (If CR24 bit1 is logic 1) 1: AUXFANIN2 (Default)

BIT	READ / WRITE	DESCRIPTION
4	R / W	Pin 42 Function select 0: GP97(If CR2C bit0 is logic 0) Parallel Port function (If CR2C bit0 is logic 1) 1: PWROK2. (Default)
3	R / W	Pin 47 Function select 0: GP93(If CR2C bit0 is logic 0) Parallel Port function (If CR2C bit0 is logic 1) 1: PWROK1. (Default)
2	R / W	Pin 43~45, Pin48~50 Function select 0: GP96~GP94, GP92~GP90 (CR2C bit0 is logic 0) Parallel Port function (If CR2C bit0 is logic 1) 1: BUSSEL function.
1	R / W	Pin 51 Function select 0: GP84 (If CR2C bit0 is logic 0) Parallel Port function (If CR2C bit0 is logic 1) 1: BEEP (Default)
0	R / W	Pin 52 Function select 0: GP83(If CR2C bit0 is logic 0) Parallel Port function (If CR2C bit0 is logic 1) 1: PLED (Default) (PLED frequency select: LDB,CRF5,bit7~5)

**CR 28h. (Global Option; Default 20h)**

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2~0	R / W	PRTMODS2 ~ 0 => <b>Bits</b> <b>2 1 0</b> = 0 x x Parallel Port Mode. = 1 x x Reserved.

**CR 29h. (Multi-function Pin Selection; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	Pin 128 function select = 0 OVT# (Default) = 1 SMI#
5-4	Reserved.	

BIT	READ / WRITE	DESCRIPTION
3	R / W	Pins 29 ~ 36 function select = 0 Pins 29 ~ 36 → UART A (Default) = 1 Pins 29 ~ 36 → GPIO6
2-0	Reserved.	

**CR 2Ah. (SPI Configuration; Default 00h)****(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Serial Peripheral Interface Configuration bit. <b>(VSB)</b> <b>Bits</b> <b>7 6</b> = 0 0 Normal read. SPI clock is 16MHz. = 0 1 Fast read. SPI clock is 33MHz. <b>Note: This bit is ignored when CR24, bit 1 is "0" (SPI is disabled).</b>
5-4	Reserved.	
3	R/W	Reserved.
2	R / W	Pins 67 ~ 74 function select = 0 GPIO4 (Default) = 1 UARTB
1	R / W	MS pin function select = 0 MS function. (Default) = 1 GPIO function.
0	R / W	KB pin function select = 0 KB function. (Default) = 1 GPIO function.

\* Normal Read: Read 1-byte data.

Fast Read: Read 4-byte data.

**CR 2Bh. (GP3X multifunction selection, Default 7Fh)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.
6	R / W	Pin 78 Select (reset by RSMRST#) = 0 GP36 = 1 RSTOUT1# (Default)
5	R / W	Pin 79 Select (reset by RSMRST#) = 0 GP35 = 1 RSTOUT0# (Default)

BIT	READ / WRITE	DESCRIPTION
4	R / W	Pin 80 Select (reset by RSMRST#) = 0 GP34 = 1 ATXPGD (Default)
3	R / W	Pin 81 Select (reset by RSMRST#) = 0 GP33 = 1 3VSBSW# (Default) (Note. Enable 3VSBSW# at Logic Device A, CRE4, bit4=1)
2	R / W	Pin 82 Select (reset by RSMRST#) = 0 GP32 = 1 PWROK (Default)
1	R / W	Pin 83 Select (reset by RSMRST#) = 0 GP31 = 1 RESTCON# (Default)
0	R / W	Pin 84 Select (reset by RSMRST#) = 0 GP30 = 1 SUSC# (Default)

**CR 2Ch. (Multi-function Pin Selection; Default 0Ah)****(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Pin 75, 76 Select Bit s 7 6 = 0 0 GP50, GP37 (Default) = 0 1 I <sup>2</sup> C function = 1 0 Reserved. = 1 1 IR function
5	R / W	Pin 38 Select =0 GP24(If CR2C bit0 is logic 0) Parallel Port function (If CR2C bit0 is logic 1) =1 Reserved.
4	Reserved.	
3	R / W	SB-TSI / PECL function select = 0 PECL function. = 1 SB-TSI function (Default)

BIT	READ / WRITE	DESCRIPTION
2	R / W	<b>EN_PWRDN. (VBAT)</b> = 0 Thermal shutdown function is disabled. (Default) = 1 Enable thermal shutdown function. (Set this bit to 1 and the relative OVT# event register: Bank0, CR18 ,Bit6 → SYSTIN OVT# Bank0, CR4C ,Bit4 → AUXTIN OVT# Bank0, CR4C ,Bit3 → CPUTIN OVT# If current temperature exceeds high-limit setting, OVT# event will be triggered and PSON# will inactive immediately. )
1	R / W	<b>GP1X / VID input function select (Pin 116 ~ 123)</b> = 0 GPIO1X. = 1 VID input. (Default)
0	R / W	<b>Enable Parallel Port function</b> =0 GPIO (Default) =1 Parallel Port function <b>Note. If set this bit to 1, CR27 bit4~bit0 and CR2C bit5 must set to 0.</b>

**CR 2Dh. (Multi-function Pin Selection; default 08h)****(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	<b>Pin 101 Select (reset by RSMRST#)</b> = 0 RSMRST# (Default) = 1 GPIO57
6	R / W	<b>Pin 102 Select (reset by RSMRST#)</b> = 0 SKTOCC (Default) = 1 GPIO56
5	R / W	<b>Pin 60 Select (reset by RSMRST#)</b> = 0 PSOUT# (Default) = 1 GPIO55
4	R / W	<b>Pin 61 Select (reset by RSMRST#)</b> = 0 PSIN# (Default) = 1 GPIO54
3	R / W	<b>Pin 62 Select (reset by RSMRST#)</b> = 0 SUSLED(SUSLED frequency select: LogicDevice D,CREC,bit7~5) = 1 GPIO53 (Default)
2	R / W	<b>Pin 63 Select (reset by RSMRST#)</b> = 0 PSON# (Default) = 1 GPIO52
1	R / W	<b>Pin 64 Select (reset by RSMRST#)</b> = 0 SUSB# (Default) = 1 GPIO51

BIT	READ / WRITE	DESCRIPTION
0	R / W	EN_WDT2PWROK (LRESET=0) = 0 Disable PWROK pin drive pulse by VID/BUSSEL's WDTO. (Default) = 1 Enable PWROK pin drive pulse by VID/BUSSEL's WDTO. (Note. The VID/BUSSEL's WDTO timer is located on Logic Device D,CRE7 and CRE8 combination. This bit is only work for ASUS function enable. )

**CR 2Eh. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Test Mode Bits: Reserved for Nuvoton.

**CR 2Fh. (Default ss000011b)** s: value by strapping

BIT	READ / WRITE	DESCRIPTION
7	RO	Pin 34 strapping result. 0: CPUFANOUT drive 50% output 1: CPUFANOUT drive 100% output (If pin34 strapping high_VCC)
6	RO	ASUS Pin 62 strapping result. 0: Disable ASUS 1: Enable ASUS (If pin32 strapping high_VSB)
5-2	Reserved.	
1	R / W	Pin86 ~ Pin93 multi-function select 0: GP7X 1: VIDO (Default)
0	R / W	Enable VRM10 transfer to VRM 11 0: Enable 1: Disable (Default)

## 21.2 Logical Device 0 (FDC)

### CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

### CR 60h, 61h. (Default 03h, F0h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select FDC I/O base address <100h: FF8h> on 8 bytes boundary.

### CR 70h. (Default 06h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for FDC.

### CR 74h. (Default 02h)

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2~0	R / W	These bits select DRQ resource for FDC. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

### CR F0h. (Default 8Eh)

BIT	READ / WRITE	DESCRIPTION
7		<b>BIOS need to write 0 to this bit if FDC function is in use.</b>
6	R / W	This bit determines the polarity of all FDD interface signals. 0: FDD interface signals are active low. 1: FDD interface signals are active high.
5	R / W	When this bit is logic 0, indicates a second drive is installed and is reflected in status register A. (PS2 mode only)
4	R / W	Swap Drive 0, 1 Mode => 0: No Swap. 1: Drive and Motor select 0 and 1 are swapped.
3~2	R / W	Interface Mode. 00: Model 30. 01: PS/2. 10: Reserved. 11: AT Mode

BIT	READ / WRITE	DESCRIPTION	
1	R / W	FDC DMA Mode.	0: Burst Mode is enabled 1: Non-Burst Mode.
0	R / W	Floppy Mode.	0: Normal Floppy Mode. 1: Enhanced 3-mode FDD.

**CR F1h. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION	
7~6	R / W	Boot Floppy.	00: FDD A.      01: Reserved. 10: Reserved.    11: Reserved.
5~4	R / W	Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.	
3~2	R / W	Density Select.	00: Normal.      01 Normal. 10: 1 (Forced to logic 1).    11: 0 (Forced to logic 0).
1	R / W	DISFDDWR => 0: Enable FDD write. 1: Disable FDD write (forces pins WE, WD to stay high).	
0	R / W	SWWP => 0: Normal, use WP to determine whether the FDD is write protected or not. 1: FDD is always write-protected.	

**CR F2h. (Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved	
1~0	R / W	FDD A Drive Type.

**CR F4h. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: Enable FDC Pre-compensation. 1: Disable FDC Pre-compensation.
5	Reserved.	
4~3	R / W	Data Rate Table selection (Refer to TABLE A). 00: Select regular drives and 2.88 format. 01: 3-mode drive.      10: 2 Meg Tape.      11: Reserved.
2	Reserved.	
1~0	R / W	Drive Type selection (Refer to TABLE B).

## CR F5h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Same as FDD0 of CR F5h.

TABLE A

DRIVE RATE TABLE SELECT		DATA RATE		SELECTED DATA RATE		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

**TABLE B**

<b>DTYPE0</b>	<b>DTYPE1</b>	<b>DRV DEN0 (pin 2)</b>	<b>DRIVE TYPE</b>
0	0	SELDEN	4/2/1 MB 3.5" 2/1 MB 5.25" 2/1.6/1 MB 3.5" (3-MODE)
0	1	DRATE1	
1	0	$\overline{\text{SELDEN}}$	
1	1	DRATE0	

### 21.3 Logical Device 1 (Parallel Port)

#### CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

#### CR 60h, 61h. (Default 03h, 78h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select PRT I/O base address. <100h: FFCh> on 4 bytes boundary (EPP not supported) or <100h: FF8h> on 8 bytes boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

#### CR 70h. (Default 07h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for PRT.

#### CR 74h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2~0	R / W	These bits select DRQ resource for PRT. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

#### CR F0h. (Default 3Fh)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6~3	R / W	ECP FIFO Threshold.
2~0	R / W	Parallel Port Mode selection (CR28 bit2 PRTMODS2 = 0). <b>Bits</b> <b>2 1 0</b> 0 0 0: Standard and Bi-direction (SPP) mode. 0 0 1: EPP – 1.9 and SPP mode. 0 1 0: ECP mode. 0 1 1: ECP and EPP – 1.9 mode. 1 0 0: Printer Mode. 1 0 1: EPP – 1.7 and SPP mode. 1 1 0: Reserved. 1 1 1: ECP and EPP – 1.7 mode.

## 21.4 Logical Device 2 (UART A)

### CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

### CR 60h, 61h. (Default 03h, F8h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8 bytes boundary.

### CR 70h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port 1.

### CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4-2	Reserved.	
1~0	R / W	<b>Bits</b> <b>1 0</b> 0 0: UART A clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART A clock source is 2 MHz (24 MHz / 12). 1 0: UART A clock source is 24 MHz (24 MHz / 1). 1 1: <a href="#">Reserved</a>

## 21.5 Logical Device 3 (UART B)

### CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

### CR 60h, 61h. (Default 02h, F8h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 2 I/O base address <100h: FF8h> on eight-byte boundary.

### CR 70h. (Default 03h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port 2.

### CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.
4~2	Reserved.	
1~0	R / W	<b>Bits</b> <b>1 0</b> 0 0: UART B clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART B clock source is 2 MHz (24 MHz / 12). 1 0: UART B clock source is 24 MHz (24 MHz / 1). 1 1: <a href="#">Reserved</a>

### CR F1h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.

BIT	READ / WRITE	DESCRIPTION
6	R / W	IRLOCSEL => IR I/O pins' location selection. 0: Through SINB / SOUTB. 1: Through IRRX / IRTX.
5~3	R / W	IRMODE => IR function mode selection. See the table below.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: SOUTB pin of UART B function or IRTX pin of IR function in normal condition. 1: Inverse SOUTB pin of UART B function or IRTX pin of IR function.
0	R / W	0: SINB pin of UART B function or IRRX pin of IR function in normal condition. 1: Inverse SINB pin of UART B function or IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 $\mu$ S	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	Routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

**Note:** The notation is normal mode in the IR function.

**21.6 Logical Device 5 (Keyboard Controller)****CR 30h. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

**CR 60h, 61h. (Default 00h, 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

**CR 62h, 63h. (Default 00h, 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1 byte boundary.

**CR 70h. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

**CR 72h. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

**CR F0h. (Default 83h)**

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	KBC clock rate selection <b>Bits</b> <b>7 6</b> 0 0: Reserved 0 1: Reserved 1 0: 12MHz. 1 1: Reserved
5~3	Reserved.	

BIT	READ / WRITE	DESCRIPTION
2	R / W	0: Port 92 disabled. 1: Port 92 enabled.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

**21.7 Logical Device 6 (Serial Peripheral Interface)**

**CR 30h. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved.	
1	R / W	0: Serial Peripheral Interface is inactive. 1: Serial Peripheral Interface is active.
0	Reserved.	

**CR 62h, 63h. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Peripheral Interface I/O base address <100h: FF8h> on 1 byte boundary.

## 21.8 Logical Device 7 (GPIO6~GPIO9)

### CR 30h. (Default 18h)

BIT	READ / WRITE	DESCRIPTION	
7-5	Reserved.		
4	R / W	0: GPIO9 is inactive.	1: GPIO9 is active.
3	R / W	0: GPIO8 is inactive.	1: GPIO8 is active.
2	R / W	0: GPIO7 is inactive.	1: GPIO7 is active.
1	R / W	0: GPIO6 is inactive.	1: GPIO6 is active.
0	Reserved.		

### CR E0. (GPIO7 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO7 I/O register 0: The respective GPIO7 PIN is programmed as an output port 1: The respective GPIO7 PIN is programmed as an input port.

### CR E1h. (GPIO7 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO7 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

### CR E2h. (GPIO7 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO7 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

### CR E3h. (Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO7 Event Status Bit 7-0 corresponds to GP77-GP70, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

**CR E4h. (GPIO8 I/O Register; Default EFh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO8 I/O register 0: The respective GPIO8 PIN is programmed as an output port 1: The respective GPIO8 PIN is programmed as an input port.

**CR E5h. (GPIO8 Data Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO8 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

**CR E6h. (GPIO8 Inversion Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO8 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

**CR E7h. (Status Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO8 Event Status Bit 7-0 corresponds to GP87-GP80, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

**CR E8h. (GPIO9 I/O Register; Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO9 I/O register 0: The respective GPIO9 PIN is programmed as an output port 1: The respective GPIO9 PIN is programmed as an input port.

**CR E9h. (GPIO9 Data Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO9 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

**CR EAh. (GPIO9 Inversion Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO9 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

**CR EBh. (Status Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO9 Event Status Bit 7-0 corresponds to GP97-GP90, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

**CR ECh. (GPIO7 Multi-function Select Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO77 1: GPIO77 → BEEP (Set GP77 to output type first)
6	R / W	0: GPIO76 1: GPIO76 → SUSLED (Set GP76 to output type first)
5	R / W	0: GPIO75 1: GPIO75 → BEEP (Set GP75 to output type first)
4	R / W	0: GPIO74 1: GPIO74 → SUSLED (Set GP74 to output type first)
3	R / W	0: GPIO73 1: GPIO73 → BEEP (Set GP73 to output type first)
2	R / W	0: GPIO72 1: GPIO72 → SUSLED (Set GP72 to output type first)
1	R / W	0: GPIO71 1: GPIO71 → BEEP (Set GP71 to output type first)

BIT	READ / WRITE	DESCRIPTION
0	R / W	0: GPIO70 1: GPIO70 → SUSLED (Set GP70 to output type first)

**CR EDh. (GPIO8 Multi-function Select Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO87 1: GPIO87 → SUSLED (Set GP87 to output type first)
6	R / W	0: GPIO86 1: GPIO86 → SUSLED (Set GP86 to output type first)
5	R / W	0: GPIO85 1: GPIO85 → SUSLED (Set GP85 to output type first)
4	R / W	0: GPIO84 1: GPIO84 → SUSLED (Set GP84 to output type first)
3	R / W	0: GPIO83 1: GPIO83 → SUSLED (Set GP83 to output type first)
2	R / W	0: GPIO82 1: GPIO82 → SUSLED (Set GP82 to output type first)
1	R / W	0: GPIO81 1: GPIO81 → SUSLED (Set GP81 to output type first)
0	R / W	0: GPIO80 1: GPIO80 → SUSLED (Set GP80 to output type first)

**CR EEh. (GPIO9 Multi-function Select Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO97 1: GPIO97 → SUSLED (Set GP97 to output type first)
6	R / W	0: GPIO96 1: GPIO96 → SUSLED (Set GP96 to output type first)
5	R / W	0: GPIO95 1: GPIO95 → SUSLED (Set GP95 to output type first)
4	R / W	0: GPIO94 1: GPIO94 → SUSLED (Set GP94 to output type first)
3	R / W	0: GPIO93 1: GPIO93 → SUSLED (Set GP93 to output type first)
2	R / W	0: GPIO92 1: GPIO92 → SUSLED (Set GP92 to output type first)
1	R / W	0: GPIO91 1: GPIO91 → SUSLED (Set GP91 to output type first)

BIT	READ / WRITE	DESCRIPTION
0	R / W	0: GPIO90 1: GPIO90 → SUSLED (Set GP90 to output type first)

**CR F4h. (GPIO6 I/O Register; Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 I/O register 0: The respective GPIO6 PIN is programmed as an output port 1: The respective GPIO6 PIN is programmed as an input port.

**CR F5h. (GPIO6 Data Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

**CR F6h. (GPIO6 Inversion Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

**CR F7h. (Status Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO6 Event Status Bit 7-0 corresponds to GP67-GP60, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

**CR F8h. (GPIO6 Multi-function Select Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO67 1: GPIO67 → PLED (Set GP67 to output type first)
6	R / W	0: GPIO66 1: GPIO66 → PLED (Set GP66 to output type first)

BIT	READ / WRITE	DESCRIPTION
5	R / W	0: GPIO65 1: GPIO65 → PLED (Set GP65 to output type first)
4	R / W	0: GPIO64 1: GPIO64 → PLED (Set GP64 to output type first)
3	R / W	0: GPIO63 1: GPIO63 → PLED (Set GP63 to output type first)
2	R / W	0: GPIO62 1: GPIO62 → PLED (Set GP62 to output type first)
1	R / W	0: GPIO61 1: GPIO61 → PLED (Set GP61 to output type first)
0	R / W	0: GPIO60 1: GPIO60 → PLED (Set GP60 to output type first)

## 21.9 Logical Device 8 (WDTO# & GPIO1)

### CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved.	
1	R / W	0: GPIO1 is inactive.                      1: GPIO1 is active.
0	R / W	0: WDTO# and PLED are inactive.    1: WDTO# is active.

### CR F0h. (GPIO1 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 I/O register 0: The respective GPIO1 PIN is programmed as an output port 1: The respective GPIO1 PIN is programmed as an input port.

### CR F1h. (GPIO1 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

### CR F2h. (GPIO1 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

### CR F3h. (Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO1 Event Status Bit 7-0 corresponds to GP17-GP10, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

**CR F4h. (GPIO1 Multi-function Select Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO17 1: GPIO17 → BEEP (Set GP17 to output type first)
6	R / W	0: GPIO16 1: GPIO16 → PLED (Set GP16 to output type first)
5	R / W	0: GPIO15 1: GPIO15 → BEEP (Set GP15 to output type first)
4	R / W	0: GPIO14 1: GPIO14 → PLED (Set GP14 to output type first)
3	R / W	0: GPIO13 1: GPIO13 → BEEP (Set GP13 to output type first)
2	R / W	0: GPIO12 1: GPIO12 → PLED (Set GP12 to output type first)
1	R / W	0: GPIO11 1: GPIO11 → BEEP (Set GP11 to output type first)
0	R / W	0: GPIO10 1: GPIO10 → PLED (Set GP10 to output type first)

**CR F5h. (WDTO# and KBC P20 Control Mode Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~5	Reserved.	
4	R / W	WDTO# count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is in Seconds Mode, the count mode is 1/1000 sec.) (If bit-3 is in Minutes Mode, the count mode is 1/1000 min.)
3	R / W	Select WDTO# count mode. 0: Second Mode. 1: Minute Mode.
2	R / W	Enable the rising edge of a KBC reset (P20) to issue a time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the WDTO# output low pulse to the KBRST# pin (PIN28) 0: Disable. 1: Enable.
0	Reserved.	

**CR F6h. WDTO# Counter Register; Default 00h (LRESET=1)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	<p>Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watch Dog Counter and start counting down. If CR F7h, bits 7 and 6 are set, any Mouse Interrupt or Keyboard Interrupt event causes the previously-loaded, non-zero value to be reloaded to the Watch Dog Counter and the count down resumes. Reading this register returns the current value in the Watch Dog Counter, not the Watch Dog Timer Time-out value.</p> <p>00h: Time-out Disable                      01h: Time-out occurs after 1 minute only.                      02h: Time-out occurs after 2 second/minutes                      03h: Time-out occurs after 3 second/minutes                      .....                      FFh: Time-out occurs after 255 second/minutes</p> <p>(The deviation is approx 1 second.)</p>

**Note.** When WDTO# event is occurring, PWROK0 (Option), PWROK1 (Option), PWROK2 (Option) will trigger a low pulse approx 100mS. And if setting GP46, GP44, GP42 or GP40 to WDTO# event route, when WDTO# event occurring, GP46, GP44, GP42 or GP40 will trigger a high to low level till WDTO# event is cleared.

**CR F7h. (WDTO# Control & Status Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	<p>Mouse interrupt reset enables watch-dog timer reload                      0: Watchdog timer is not affected by mouse interrupt.                      1: Watchdog timer is reset by mouse interrupt.</p>
6	R / W	<p>Keyboard interrupt reset enables watch-dog timer reload                      0: Watchdog timer is not affected by keyboard interrupt.                      1: Watchdog timer is reset by keyboard interrupt.</p>
5	Write "1" Only	Trigger WDTO# event. This bit is self-clearing.
4	R / W Write "0" Clear	<p>WDTO# status bit                      0: Watchdog timer is running.                      1: Watchdog timer issues time-out event.</p>
3~0	R / W	These bits select the IRQ resource for the WDTO#. (02h for SMI# event.)

### 21.10 Logical Device 9 (GPIO2, GPIO3, GPIO4, GPIO5)

#### CR 30h. (Default 05h)

BIT	READ / WRITE	DESCRIPTION	
7~4	Reserved.		
3	R / W	0: GPIO5 is inactive.	1: GPIO5 is active
2	R / W	0: GPIO4 is inactive.	1: GPIO4 is active.
1	R / W	0: GPIO3 is inactive.	1: GPIO3 is active.
0	R / W	0: GPIO2 is inactive.	1: GPIO2 is active.

#### CR E0h. (GPIO2 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 I/O register 0: The respective GPIO2 PIN is programmed as an output port 1: The respective GPIO2 PIN is programmed as an input port.

#### CR E1h. (GPIO2 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

#### CR E2h. (GPIO2 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

#### CR E3h. (GPIO2 Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO2 Event Status Bit 7-0 corresponds to GP27-GP20, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

**CR E4h. (GPIO3 I/O Register; Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 I/O register 0: The respective GPIO3 PIN is programmed as an output port 1: The respective GPIO3 PIN is programmed as an input port.

**CR E5h. (GPIO3 Data Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

**CR E6h. (GPIO3 Inversion Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

**CR E7h. (GPIO3 Status Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO3 Event Status Bit 7-0 corresponds to GP37-GP30, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Read the status bit clears it to 0.

**CR E8h. (GPIO4 Status Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO4 Event Status Bit 7-0 corresponds to GP47-GP40, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

**CR E9h. (GPIO2 Multi-function Select Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO27 1: GPIO27 → SMI# (Set GP27 to output type first)

BIT	READ / WRITE	DESCRIPTION
6	R / W	0: GPIO26 1: GPIO26 → SUSLED (Set GP26 to output type first)
5	R / W	0: GPIO25 1: GPIO25 → BEEP (Set GP25 to output type first)
4	R / W	0: GPIO24 1: GPIO24 → SUSLED (Set GP24 to output type first)
3	R / W	0: GPIO23 1: GPIO23 → SUSLED (Set GP23 to output type first)
2	R / W	0: GPIO22 1: GPIO22 → SUSLED (Set GP22 to output type first)
1	R / W	0: GPIO21 1: GPIO21 → SUSLED (Set GP21 to output type first)
0	R / W	0: GPIO20 1: GPIO20 → SUSLED (Set GP20 to output type first)

**CR EAh. (GPIO3 Multi-function Select Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO37 1: GPIO37 → SUSLED (Set GP37 to output type first)
6	R / W	0: GPIO36 1: GPIO36 → SUSLED (Set GP36 to output type first)
5	R / W	0: GPIO35 1: GPIO35 → SUSLED (Set GP35 to output type first)
4	R / W	0: GPIO34 1: GPIO34 → SUSLED (Set GP34 to output type first)
3	R / W	0: GPIO33 1: GPIO33 → SUSLED (Set GP33 to output type first)
2	R / W	0: GPIO32 1: GPIO32 → SUSLED (Set GP32 to output type first)
1	R / W	0: GPIO31 1: GPIO31 → SUSLED (Set GP31 to output type first)
0	R / W	0: GPIO30 1: GPIO30 → SUSLED (Set GP30 to output type first)

**CR EBh. (GPIO5 Multi-function Select Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO57 1: GPIO57 → SUSLED (Set GP57 to output type first)

BIT	READ / WRITE	DESCRIPTION
6	R / W	0: GPIO56 1: GPIO56 → SUSLED (Set GP56 to output type first)
5	R / W	0: GPIO55 1: GPIO55 → SUSLED (Set GP55 to output type first)
4	R / W	0: GPIO54 1: GPIO54 → SUSLED (Set GP54 to output type first)
3	R / W	0: GPIO53 1: GPIO53 → SUSLED (Set GP53 to output type first)
2	R / W	0: GPIO52 1: GPIO52 → SUSLED (Set GP52 to output type first)
1	R / W	0: GPIO51 1: GPIO51 → SUSLED (Set GP51 to output type first)
0	R / W	0: GPIO50 1: GPIO50 → SUSLED (Set GP50 to output type first)

**CR F0h. (GPIO4 I/O Register; Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 I/O register 0: The respective GPIO4 PIN is programmed as an output port 1: The respective GPIO4 PIN is programmed as an input port.

**CR F1h. (GPIO4 Data Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

**CR F2h. (GPIO4 Inversion Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

**CR F3h. (GPIO4 Multi-function Select Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
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BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO47 1: GPIO47 → SUSLED (Set GP47 to output type first)
6	R / W	0: GPIO46 1: GPIO46 → WDTO# (Set GP46 to output type first)
5	R / W	0: GPIO45 1: GPIO45 → SUSLED (Set GP45 to output type first)
4	R / W	0: GPIO44 1: GPIO44 → WDTO# (Set GP44 to output type first)
3	R / W	0: GPIO43 1: GPIO43 → SUSLED (Set GP43 to output type first)
2	R / W	0: GPIO42 1: GPIO42 → WDTO# (Set GP42 to output type first)
1	R / W	0: GPIO41 1: GPIO41 → SUSLED (Set GP41 to output type first)
0	R / W	0: GPIO40 1: GPIO40 → WDTO# (Set GP40 to output type first)

**CR F4h. (GPIO5 I/O Register; Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 I/O register 0: The respective GPIO5 PIN is programmed as an output port 1: The respective GPIO5 PIN is programmed as an input port.

**CR F5h. (GPIO5 Data Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.

**CR F6h. (GPIO5 Inversion Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

**CR F7h. (GPIO5 Status Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only Read-Clear	GPIO5 Event Status Bit 7-0 corresponds to GP57-GP50, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

**CR FEh. (Input Detected Type Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: Enable GP37 input de-bouncer 1: Disable GP37 input de-bouncer
5	R / W	0: Enable GP53 input de-bouncer 1: Disable GP53 input de-bouncer
4	R / W	0: Enable GP50 input de-bouncer 1: Disable GP50 input de-bouncer
3	Reserved.	
2	R / W	0: GP37 trigger type: edge 1: GP37 trigger type: level
1	R / W	0: GP53 trigger type: edge 1: GP53 trigger type: level
0	R / W	0: GP50 trigger type: edge 1: GP50 trigger type: level

21.11 Logical Device A (ACPI)

CR E0h. (Default 01h) (VBAT power)

BIT	READ / WRITE	DESCRIPTION																												
7	R / W	DIS_PSIN => Disable the panel switch input to turn on the system power supply. 0: PSIN is wire-AND and connected to PSOUT#. 1: PSIN is blocked and cannot affect PSOUT#.																												
6	R / W	Enable KBC wake-up 0: Disable keyboard wake-up function via PSOUT#. 1: Enable keyboard wake-up function via PSOUT#.																												
5	R / W	Enable Mouse wake-up 0: Disable mouse wake-up function via PSOUT#. 1: Enable mouse wake-up function via PSOUT#.																												
4	R / W	MSRKEY => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the following table for the details.																												
		<table border="1"> <thead> <tr> <th>ENMDAT_UP</th> <th>MSRKEY</th> <th>MSXKEY</th> <th>Wake-up event</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>x</td> <td>1</td> <td>Any button clicked or any movement.</td> </tr> <tr> <td>1</td> <td>x</td> <td>0</td> <td>One click of left or right button.</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>One click of the left button.</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>One click of the right button.</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Two clicks of the left button.</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Two clicks of the right button.</td> </tr> </tbody> </table>	ENMDAT_UP	MSRKEY	MSXKEY	Wake-up event	1	x	1	Any button clicked or any movement.	1	x	0	One click of left or right button.	0	0	1	One click of the left button.	0	1	1	One click of the right button.	0	0	0	Two clicks of the left button.	0	1	0	Two clicks of the right button.
		ENMDAT_UP	MSRKEY	MSXKEY	Wake-up event																									
		1	x	1	Any button clicked or any movement.																									
		1	x	0	One click of left or right button.																									
		0	0	1	One click of the left button.																									
		0	1	1	One click of the right button.																									
0	0	0	Two clicks of the left button.																											
0	1	0	Two clicks of the right button.																											
3	Reserved.																													
2	R / W	Keyboard / Mouse swap enable 0: Normal mode. 1: Keyboard / Mouse ports are swapped.																												
1	R / W	MSXKEY => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.																												
0	R / W	KBXKEY => 0: Only the pre-determined key combination in sequence can wake up the system. 1: Any character received from the keyboard can wake up the system.																												

CR E1h. (KBC Wake-Up Index Register; Default 00h) (VSB power)

BIT	READ / WRITE	DESCRIPTION
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BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up index register. This is the index register of CRE2, which is the access window for the keyboard's pre-determined key key-combination characters. The first set of wake-up keys is in of 0x00 - 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combinations can be read through 0x10 – 0x1E.

**CR E2h. (KBC Wake-Up Data Register; Default FFh) (VSB power)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up data register. This is the data register for the keyboard's pre-determined key-combination characters, which is indexed by CRE1.

**CR E3h. (Event Status Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	Read Only Read-Clear	This status flag indicates VSB power off/on.
4	Read Only Read-Clear	If E4[7] is 1 => 0: When power-loss occurs and the VSB power is on, turn on system power. 1: When power-loss occurs and the VSB power is on, turn off system power. If E4[7] is 0 => This bit is always 0.
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: Thermal shutdown event issued.
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event issued. 1: PSIN event issued.
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: Mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: Keyboard wake-up event issued.

**CR E4h. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	

BIT	READ / WRITE	DESCRIPTION
6~5	R / W	Power-loss control bits. These two bits will determine the system turn on or off after AC resume(G3→S5). <b>Note</b> (VBAT) <b>Bit</b> <b>6 5</b> 0 0: Always turn off. 0 1: Always turn on. (PSON# will active when S3# is high.) 1 0: Pre-state. (System turns On or Off which depends on the state before power loss. Please notice the definition of pre-state is On and Off. See chapter 22.3.2 item 3. If the pre-state On and Off definition are not coincident with the application, use "User defined mode" instead.) 1 1: User defined mode for power loss last-state. (Note. The last-state flag is setting by CRE6[4])
4	R / W	3VSBSW# Enable bit => 0: Disable. (Default) 1: Enable.
3	R / W	Keyboard wake-up options. ( <b>LRESET#</b> ) 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for wake-up events set in CRE0. This bit is cleared when any wake-up event is captured. ( <b>LRESET#</b> ) (Note. This bit is use for KB and MS to generate PSOUT# while VCC valid, for example, wake-up from S1 to S0 via PSOUT#.) 0: Disable.(Default) 1: Enable.
1~0	Reserved.	

**Note.** Whether "Always turn on", "Pre-state", or "User defined mode", the PSON# active condition for system turn on is S3# goes high. For southbridge which S3# default is low when AC resume, refer CRE7h, bit4 to achieve power-loss control application.

#### CR E5h. (GPIOs Reset Source Register; Default 02h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	GP9X_MRST 0: GP9X reset by RSMRST#. 1: GP9X reset by SLPS5.
6	R / W	GP8X_MRST 0: GP8X reset by RSMRST#. 1: GP8X reset by SLPS5.
5	R / W	GP7X_MRST 0: GP7X reset by RSMRST#. 1: GP7X reset by SLPS5.
4	R / W	GP6X_MRST 0: GP6X reset by LRESET#. 1: GP6X reset by PWROK.
3-2	Reserved.	

BIT	READ / WRITE	DESCRIPTION
1	R / W	PWROK source selection. 0: PSON#. 1: SUSB#. (Default)
0	R / W	ATXPGD signal to control PWROK 0: Enable. 1: Disable. (Default)

**CR E6h. (Default 1Ch)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => <b>(VSB)</b> Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the table in CRE0, bit 4 for the details.
6	Read Only	SKTOCC Status. <b>(VBAT)</b> This bit is '1' when pin 102 SKTOCC = 0. (Write CRE7h,bit1=1 to clear this status.)
5	R / W	CASEOPEN Clear Control. <b>(VSB)</b> Write 1 to this bit to clear CASEOPEN status. This bit will clear the status itself.
4	R / W	Power-loss Last State Flag. <b>(VBAT)</b> 0: ON 1: OFF. (Default)
3~1	R / W	PWROK_DEL <b>(VSB)</b> Set PWROK delay time when rising from 3VCC power. <b>Bits</b> <b>3 2 1</b> 0 0 0: 300 ~ 600mS 0 0 1: 330 ~ 670mS 0 1 0: 390 ~ 730mS 0 1 1: 520 ~ 860mS 1 0 0: 200 ~ 300mS 1 0 1: 230 ~ 370mS 1 1 0: 290 ~ 430mS 1 1 1: 420 ~ 560mS
0	R / W	PWROK_TRIG => <b>(VSB)</b> 0: PWROK work normally. (Default) 1: Write 1 will let PWROK keep low or from high to low immediately.

**CR E7h. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
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BIT	READ / WRITE	DESCRIPTION
7	R / W	<b>ENKD3 =&gt; (VSB)</b> Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	<b>ENKD2 =&gt; (VSB)</b> Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.
5	R / W	<b>ENWIN98KEY =&gt; (VSB)</b> Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.
4	R / W	<b>EN_ONPSOUT (VBAT)</b> Disable/Enable to issue a 0.5s delay PSOUT# level when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (For southbridge which S3# default is low when AC resume, like VIA, AMD...etc.) 0: Disable. (Default) 1: Enable.
3	R / W	<b>Select WDTO# reset source (VSB)</b> 0: Watchdog timer is reset by LRESET#. 1: Watchdog timer is reset by PWROK.
2	Reserved.	
1	R / W	<b>SKTOCC Clear Control. (VSB)</b> Write 1 to this bit to clear SKTOCC status (CRE6,bit6). This bit will clear the status itself.
0	R / W	<b>Hardware Monitor RESET source select (VBAT)</b> 0: PWROK. (Default) 1: LRESET#.

**CR E8h. (Reserved)**
**CR E9h. (GPIOs Reset Source Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	<b>GP5X_MRST</b> 0: GP5X reset by RSMRST#. 1: GP5X reset by SLPS5.

BIT	READ / WRITE	DESCRIPTION
6	R / W	GP4X_MRST 0: GP4X reset by RSMRST#. 1: GP4X reset by SLPS5.
5	Reserved.	
4	R / W	GP2X_MRST 0: GP2X reset by RSMRST#. 1: GP2X reset by SLPS5.
3	R / W	GP1X_MRST 0: GP1X reset by LRESET#. 1: GP1X reset by PWROK.
2~1	Reserved.	
0	Reserved.	

**CR F2h. (Default 7Ch) (VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	EN_WDT2PWROK (LRESET=1) = 0     Disable PWROK0,1 or 2 pin drive pulse by WDTO. (Default) = 1     Enable PWROK0,1 or 2 pin drive pulse by WDTO. (Note. The WDTO timer is located on Logic Device 8, CRF6h.)
6~5	Reserved.	
4	R / W	Enable RSTOUT2# function. 0: Disable RSTOUT2#. 1: Enable RSTOUT2#. (Default)
3	R / W	Enable RSTOUT1# function. 0: Disable RSTOUT1#. 1: Enable RSTOUT1#. (Default)
2	R / W	Enable RSTOUT0# function. 0: Disable RSTOUT0#. 1: Enable RSTOUT0#. (Default)
1	Reserved.	
0	R / W	Enable PME# (Power Management Event) : 0: Disable PME#. (Default) 1: Enable PME#.

**CR F3h. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W-Clear	PME status of the Mouse IRQ event. Write 1 to clear this status.

BIT	READ / WRITE	DESCRIPTION
4	R / W-Clear	PME status of the KBC IRQ event. Write 1 to clear this status.
3	R / W-Clear	PME status of the PRT IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the FDC IRQ event. Write 1 to clear this status.
1	R / W-Clear	PME status of the URA IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME status of the URB IRQ event. Write 1 to clear this status.

**CR F4h. (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W-Clear	PME status of the HM IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the WDTO# event. Write 1 to clear this status.
1	Reserved.	
0	R / W-Clear	PME status of the RIB event. Write 1 to clear this status.

**CR F6h. (Default 00h) (VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable KB, MS interrupt of the KBC password event. 1: Enable KB, MS interrupt of the KBC password event. (Need also enable CRE0, Bit5 and Bit6 for use this function.)
6	Reserved.	
5	R / W	0: Disable PME interrupt of the Mouse IRQ event. 1: Enable PME interrupt of the Mouse IRQ event.
4	R / W	0: Disable PME interrupt of the KBC IRQ event. 1: Enable PME interrupt of the KBC IRQ event.
3	R / W	0: Disable PME interrupt of the PRT IRQ event. 1: Enable PME interrupt of the PRT IRQ event.
2	R / W	0: Disable PME interrupt of the FDC IRQ event. 1: Enable PME interrupt of the FDC IRQ event.
1	R / W	0: Disable PME interrupt of the URA IRQ event. 1: Enable PME interrupt of the URA IRQ event.

BIT	READ / WRITE	DESCRIPTION
0	R / W	0: Disable PME interrupt of the URB IRQ event. 1: Enable PME interrupt of the URB IRQ event.

**CR F7h. (Default 00h) (VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W	0: Disable PME interrupt of the HM IRQ event. 1: Enable PME interrupt of the HM IRQ event.
2	R / W	0: Disable PME interrupt of the WDTO# event. 1: Enable PME interrupt of the WDTO# event.
1	Reserved.	
0	R / W	0: Disable PME interrupt of the RIB event. 1: Enable PME interrupt of the RIB event.

**CR FEh. (GPIO37, 50 & 53 Event Route Selection Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.
6	R / W	0: Disable GP37 event route to PSOUT#. 1: Enable GP37 event route to PSOUT#.
5	R / W	0: Disable GP53 event route to PSOUT#. 1: Enable GP53 event route to PSOUT#.
4	R / W	0: Disable GP50 event route to PSOUT#. 1: Enable GP50 event route to PSOUT#.
3	Reserved.	
2	R / W	0: Disable GP37 event route to PME#. 1: Enable GP37 event route to PME#.
1	R / W	0: Disable GP53 event route to PME#. 1: Enable GP53 event route to PME#.
0	R / W	0: Disable GP50 event route to PME#. 1: Enable GP50 event route to PME#.

**CR FFh. (Output Type Selection Register; Default 30h)**

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Reserved.

BIT	READ / WRITE	DESCRIPTION
5	R / W	Select output type of PWROK1 and PWROK2 =0 PWROK1,2 are Push-pull. =1 PWROK1,2 are Open-drain. (Default)
4	R / W	Select output type of PWROK0 =0 PWROK0 is Push-pull. =1 PWROK0 is Open-drain. (Default)
3~0	Reserved.	

## 21.12 Logical Device B (Hardware Monitor & SB-TSI)

### CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

### CR 60h, 61h. (Default 00h, 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the HM base address <100h : FFEh> along a two-byte boundary.

### CR 70h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select the IRQ resource for HM.

### CR E0h. (SB-TSI configuration; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	BANK Select. =0 BANK 0 ( for Polling Mode ) =1 BANK 1 ( for Manual Mode )
6	R / W	MODE Select. = 0 Polling Mode (Default) = 1 Manual Mode
5-3	R / W	SB-TSI SCL output frequency select <b>Bit</b> <b>5 4 3</b> =0 1 0 0.75 MHz =0 1 1 0.375 MHz =1 0 0 187.5 KHz =1 0 1 93.75 KHz =1 1 0 46.875 KHz =1 1 1 23.4375 KHz

BIT	READ / WRITE	DESCRIPTION
2-0	R / W	SB-TSI Address (7 Bit) select. <b>Bit</b> <b>2 1 0</b> =0 0 0    4C =0 0 1    4D =0 1 0    4E =0 1 1    4F =1 0 0    48 =1 0 1    49 =1 1 0    4A =1 1 1    4B

**CR E1h. (BANK 0; Polling Mode STATUS Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6-4	R / W	Update Rate Select. <b>Bit</b> <b>6 5 4</b> = 0 0 0    91.55 Hz = 0 0 1    22.88 Hz = 0 1 0    5.722 Hz = 0 1 1    1.43 Hz = 1 0 0    0.357 Hz = 1 0 1    0.0894 Hz
3	R / W	Enable Polling Mode transmission. =0    Disable (Default) =1    Enable
2	Reserved	
1	R	Polling Mode BUSY signal. =0    Ready to transfer =1    Not ready to transfer
0	Reserved.	

**CR E2h. (BANK 0; CPU Temperature High Byte Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7-0	RO	Integer CPU temperature value.

**CR E3h. (BANK 0; CPU Temperature Low Byte Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
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BIT	READ / WRITE	DESCRIPTION
7-0	RO	Decimal CPU temperature value.

**CR E1h. (BANK 1; Manual Mode STATUS Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R / W	Enable Manual Mode transmission.
2	R / W	Read / Write command select. =0 Write =1 Read
1	RO	Manual Mode BUSY signal =0 Ready to transfer =1 Not ready to transfer
0	Reserved.	

**CR E2h. (BANK 1; Manual Mode INDEX Data Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Manual Mode INDEX Data.

**CR E3h. (BANK 1; Manual Mode Write Data Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Manual Mode Write Data.

**CR E4h. (BANK 1; Manual Mode Receive Data Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7-0	RO	Manual Mode Read Data.

**CR F0h. (Fan Input De-bounce Register; Default C1h)**

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W	1: Enable AUXFANIN2 input de-bounce. 0: Disable AUXFANIN2 input de-bounce. (Default)
4	R / W	1: Enable AUXFANIN1 input de-bounce. 0: Disable AUXFANIN1 input de-bounce. (Default)
3	R / W	1: Enable AUXFANIN input de-bounce. 0: Disable AUXFANIN input de-bounce. (Default)
2	R / W	1: Enable CPUFANIN input de-bounce. 0: Disable CPUFANIN input de-bounce. (Default)

BIT	READ / WRITE	DESCRIPTION
1	R / W	1: Enable SYSFANIN input de-bounce. 0: Disable SYSFANIN input de-bounce. (Default)
0	Reserved.	

**CR F5h. (PLED Frequency configuration and SMBus Input De-bounce Register; Default 10h)**

BIT	READ / WRITE	DESCRIPTION
7~5	R / W	PLED Frequency <b>Bits</b> <b>7 6 5</b> =0 0 0 always high (Default) =0 0 1 always low =0 1 0 4Hz =0 1 1 2Hz =1 0 0 1Hz =1 0 1 1/2Hz =1 1 0 1/4Hz
4~2	Reserved.	
1	R / W	1: Enable SCL input de-bouncer. 0: Disable SCL input de-bouncer. (Default)
0	R / W	1: Enable SDA input de-bouncer. 0: Disable SDA input de-bouncer. (Default)

### 21.13 Logical Device C (PECI)

#### CR E0h. (Agent Configuration Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Agt4EN (Agent 4 Enable Bit) 0: Agent 4 is disabled. 1: Agent 4 is enabled.
6	R / W	Agt3EN (Agent 3 Enable Bit) 0: Agent 3 is disabled. 1: Agent 3 is enabled.
5	R / W	Agt2EN (Agent 2 Enable Bit) 0: Agent 2 is disabled. 1: Agent 2 is enabled.
4	R / W	Agt1EN (Agent 1 Enable Bit) 0: Agent 1 is disabled. 1: Agent 1 is enabled.
3	R / W	RTD4 0: Agent 4 always returns the relative temperature from domain 0. 1: Agent 4 always returns the relative temperature from domain 1.
2	R / W	RTD3 (Agent 3 Return Domain 1 Enable Bit. Functions only when Agt3D1 is set to 1) 0: Agent 3 always returns the relative temperature from domain 0. 1: Agent 3 always returns the relative temperature from domain 1.
1	R / W	RTD2 (Agent 2 Return Domain 1 Enable Bit. Functions only when Agt2D1 is set to 1) 0: Agent 2 always returns the relative temperature from domain 0. 1: Agent 2 always returns the relative temperature from domain 1.
0	R / W	RTD1 (Agent 1 Return Domain 1 Enable Bit. Functions only when Agt1D1 is set to 1) 0: Agent 1 always returns the relative temperature from domain 0. 1: Agent 1 always returns the relative temperature from domain 1.

#### CR E1h. (Agent 1 TBase Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~0	R / W	Agent 1 TBase (Range: 0~127). (Note 1)

**CR E2h. (Agent 2 TBase Register; Default 48h)**

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~0	R / W	Agent 2 TBase (Range: 0~127). (note 1)

**CR E3h. (Agent 3 TBase Register; Default 48h)**

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~0	R / W	Agent 3 TBase (Range: 0~127). (Note 1)

**CR E4h. (Agent 4 TBase Register; Default 48h)**

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~0	R / W	Agent 4 TBase (Range: 0~127). (Note 1)

Note 1: TBase is a temperature reference based on the experiment of processor actual temperature.

**CR E5h. (PECI Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	Agt4D1 (Agent 4 Domain 1 Enable Bit) 0: Agent 4 does not have domain 1. 1: Agent 4 has domain 1.
6	R / W	Agt3D1 (Agent 3 Domain 1 Enable Bit) 0: Agent 3 does not have domain 1. 1: Agent 3 has domain 1.
5	R / W	Agt2D1 (Agent 2 Domain 1 Enable Bit) 0: Agent 2 does not have domain 1. 1: Agent 2 has domain 1.
4	R / W	Agt1D1 (Agent 1 Domain 1 Enable Bit) 0: Agent 1 does not have domain 1. 1: Agent 1 has domain 1.
3	R / W	PECI_1.1a_en 0: Normal PECI transmission. (Default) 1: PECI_1.1a transmission with PECI_AVL and PECI_REQ#.
2	R / W	Force Start PECI_1.1a Transmission 0: Start PECI_1.1a transmission with PECI_AVL high. 1: Start PECI_1.1a transmission without PECI_AVL high.

BIT	READ / WRITE	DESCRIPTION
1	R / W	Return High Temperature 0: The temperature of each agent is returned from domain 0 or domain 1, which is controlled by CRE0 bit 0~3. 1: Return the highest temperature in domain 0 and domain 1 of individual Agent.
0	Reserved.	

**CR E6h. (PECI Module Reset Register ; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~1	R / W	Reserved.
0	R / W	Reset Super-IO internal PECI module circuit. (Reset hardware only, others registers in Logic Device C wouldn't be reset.) Write 1 then 0 to reset PECI module.

**CR E8h. (PECI Warning Flag and PECI Speed Select Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	Read only	<b>Agent 4 Alert Bit</b> (When CR E8[3] is 0) 0: Agent 4 has valid FCS. 1: Agent 4 has invalid FCS in the previous 3 transactions.
		<b>Agent 4 Absent Bit</b> (When CR E8[3] is 1) 0: Agent 4 is detected. 1: Agent 4 cannot be detected.
6	Read only	<b>Agent 3 Alert Bit</b> (When CR E8[3] is 0) 0: Agent 3 has valid FCS. 1: Agent 3 has invalid FCS in the previous 3 transactions.
		<b>Agent 3 Absent Bit</b> (When CR E8[3] is 1) 0: Agent 3 is detected. 1: Agent 3 cannot be detected.
5	Read only	<b>Agent 2 Alert Bit</b> (When CR E8[3] is 0) 0: Agent 2 has valid FCS. 1: Agent 2 has invalid FCS in the previous 3 transactions.
		<b>Agent 2 Absent Bit</b> (When CR E8[3] is 1) 0: Agent 2 is detected. 1: Agent 2 cannot be detected.
4	Read only	<b>Agent 1 Alert Bit</b> (When CR E8[3] is 0) 0: Agent 1 has valid FCS. 1: Agent 1 has invalid FCS in the previous 3 transactions.

BIT	READ / WRITE	DESCRIPTION
		<b>Agent 1 Absent Bit</b> (When CR E8[3] is 1) 0: Agent 1 is detected. 1: Agent 1 cannot be detected.
3~2	R / W	<b>Bank Select.</b> These two bits are used in Bank index selection. The relative data delivered over PECL interface and PECL Agent Absent Bit can be read from the registers below by setting Bank selection. The relative data delivered over PECL interface can be read in CR FE and CR FF, and the PECL warning flag can be read in CR E8 bit 7~4.
1~0	R / W	<b>PECL Speed Select.</b> <b>Bits</b> <b>1 0</b> 0 0: The PECL speed is 1.5 MHz (Default) 0 1: The PECL speed is 750 KHz 1 0: The PECL speed is 375 KHz 1 1: The PECL speed is 187 KHz

**CR E9h. (Reserved)****CR EAh. (PECL\_1.1a Status Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7	Read_Only	PECL_1.1a unavailable alert bit (When CR E8[2] is 0) 0: PECL_1.1a transmission correct. 1: PECL_AVL occurred low during PECL_1.1a transmission and FCS was wrong.
		Agent 4 Alert toggle bit (When CR E8[2] is 1) 0: PECL Alert bit never occurred. 1: PECL Alert bit occurred once. (Read clear)
6	Read_Only	PECL_1.1a transmission timeout bit (When CR E8[2] is 0) 0: PECL_1.1a transmission correct. 1: PECL_AVL is not high when PECL_REQ# is low for 1ms.
		Agent 3 Alert toggle bit (When CR E8[2] is 1) 0: PECL Alert bit never occurred. 1: PECL Alert bit occurred once. (Read clear)
5	Read_Only	PECL_1.1a unavailable start-up status bit (When CR E8[2] is 0) 0: PECL_AVL occurs high when PECL_1.1a transmission is started up. 1: PECL_AVL occurs low when PECL_1.1a transmission is started up.
		Agent 2 Alert toggle bit (When CR E8[2] is 1) 0: PECL Alert bit never occurred. 1: PECL Alert bit occurred once. (Read clear)

BIT	READ / WRITE	DESCRIPTION
4	Read_Only	PECI_1.1a unavailable status bit during PECI_1.1a transmission (When CR E8[2] is 0) 0: PECI_AVL occurs high during PECI_1.1a transmission. 1: PECI_AVL occurs low during PECI_1.1a transmission.
		Agent 2 Alert toggle bit (When CR E8[2] is 1) 0: PECI Alert bit never occurred. 1: PECI Alert bit occurred once. (Read clear)
3	Read_Only	Reserved. (When CR E8[2] is 0)
		PECI_1.1a unavailable alert toggle bit (When CR E8[2] is 1) 0: PECI_1.1a unavailable alert bit never occurred. 1: PECI_1.1a unavailable alert bit occurred once. (Read clear)
2	Read_Only	Reserved. (When CR E8[2] is 0)
		PECI_1.1a transmission timeout toggle bit (When CR E8[2] is 1) 0: PECI_1.1a transmission timeout bit never occurred. 1: PECI_1.1a transmission timeout bit occurred once. (Read clear)
1	Read_Only	Reserved. (When CR E8[2] is 0)
		PECI_1.1a unavailable start-up status bit (When CR E8[2] is 1) 0: PECI_1.1a unavailable start-up status bit never occurred. 1: PECI_1.1a unavailable start-up status bit occurred once. (Read clear)
0	Read_Only	Reserved. (When CR E8[2] is 0)
		PECI_1.1a unavailable status bit during PECI_1.1a transmission (When CR E8[2] is 1) 0: PECI_1.1a unavailable status bit during PECI_1.1a transmission never occurred. 1: PECI_1.1a unavailable status bit during PECI_1.1a transmission occurred once. (Read clear)

**CR ECh. (PECI Transmission Cycle Time Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~3	R / W	Reserved.

BIT	READ / WRITE	DESCRIPTION
2~0	R / W	PECl Transmission cycle time: <b>Bits</b> <b>2 1 0</b> 0 0 0 : Finish one PECl message transmission every 0.0625sec(16Hz) 0 0 1 : Finish one PECl message transmission every 0.125sec(8Hz) 0 1 0 : Finish one PECl message transmission every 0.25sec(4Hz) 0 1 1 : Finish one PECl message transmission every 0.5sec(2Hz) 1 0 0 : Finish one PECl message transmission every 1sec(1Hz) 1 0 1 : Finish one PECl message transmission every 2sec(1/2Hz) 1 1 0 : Finish one PECl message transmission every 4sec(1/4Hz)

**CR Eeh. (Reserved; Default 01h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Reserved

**CR EFh. (Reserved; Default 5Ah)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Reserved

**CR F1h. (Reserved; Default 48h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Reserved

**CR F2h. (Reserved; Default 50h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Reserved

**CR F3h. (Reserved; Default 10h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Reserved

**CR FEh. (PECI Agent Relative High Byte Temperature Register; Default 80h)**

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	<p>This register shows the retrieved High Byte raw data from PECI interface. When Bank Select (CR E8 bit 3~2)</p> <p><b>Bits</b></p> <p><b>3 2</b></p> <p>= 0 0      Agt1RelTemp (High Byte)</p> <p>= 0 1      Agt2RelTemp (High Byte)</p> <p>= 1 0      Agt3RelTemp (High Byte)</p> <p>= 1 1      Agt4RelTemp (High Byte)</p>

**CR FFh. (PECI Agent Relative Low Byte Temperature Register; Default 01h)**

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	<p>This register shows the retrieved High Byte raw data from PECI interface. When Bank Select (CR E8 bit 3~2)</p> <p><b>Bits</b></p> <p><b>3 2</b></p> <p>= 0 0      Agt1RelTemp (Low Byte)</p> <p>= 0 1      Agt2RelTemp (Low Byte)</p> <p>= 1 0      Agt3RelTemp (Low Byte)</p> <p>= 1 1      Agt4RelTemp (Low Byte)</p>

**Note: Logical Device C (PECI) cannot be accessed via SMBus.**

## 21.14 Logical Device D (VID and BUSSEL)

### CR E0h. (VID Manual Mode Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	VID Manual Mode Control Values.

### CR E1h. (VID Offset Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	VID offset value between VID input and VID output. (2's complement format)

### CR E2h. (VID Output Register)

BIT	READ / WRITE	DESCRIPTION
7~0	RO	VID Output Values : When VCC off it keep the last VID output values.

### CR E3h. (VID Input Register)

BIT	READ / WRITE	DESCRIPTION
7~0	RO	VID Input Values

### CR E4h. (VID Configuration Register; Default 07h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	VID Mode Selection <b>Bit</b> <b>7 6</b> = 0 0 By pass mode (Default) = 0 1 Offset markup mode = 1 0 Manual mode = 1 1 Max. mode Note. Max. mode's value is the higher value depend on VID input value(CRE3) compare with manual mode value(CRE0).
5	R / W	SKTOCC_INV (Enable Pin102 SKTOCC high reset VID) <b>(VSB)</b> 0: Disable (Default)( Pin102 SKTOCC low reset VID) 1: Enable (Pin102 SKTOCC high reset VID)
4	R / W	Rolling mode enable (Set Rolling Rate on CR EFh.) 0: Disable Rolling mode 1: Enable Rolling mode
3	R / W	SMI_Auto_Clr enable

BIT	READ / WRITE	DESCRIPTION
2~0	R / W	VID table selection <b>Bits</b> <b>2 1 0</b> = 0 0 0 AMD 5-bit = 0 1 0 AMD 6-bit = 1 0 0 VRM 10.1 (6-bit) = 1 0 1 VRM 10.2 (7-bit) = 1 1 0 VRM 11 (8-bit) = 1 1 1 By Pass Mode (Default)

**CR E5h. (BUSSEL Control Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~5	R / W	BUSSEL Manual Mode Control Values.
4~3	R / W	BUSSEL Mode Selection <b>Bits</b> <b>4 3</b> = 0 0 By pass mode = 0 1 Offset makeup mode = 1 0 Manual mode = 1 1 Max. mode Note. Max. mode's value is the higher value depend on BUSSEL input value(CRE6,bit2~0) compare with manual mode value(CRE5,bit7~5).
2~0	R / W	BUSSEL Offset Control Values. Bit 2= Sign Bit 1: Plus(+) 0:Minus(-) Bit 1~0= BUSSEL Offset Value

**CR E6h. ( BUSSEL In/Out value Register)**

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	RO	BUSSELO2 Output Value
5	RO	BUSSELO1 Output Value
4	RO	BUSSELO0 Output Value
3	Reserved	
2	RO	BUSSELI2 Input Value
1	RO	BUSSELI1 Input Value
0	RO	BUSSELI0 Input Value

**CR E7h. VID/BUSSEL's WDTO Software Reset Clock select Register; Default 00h (LRESET=0)**

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~2	R / W	Clock select of 5 second watch dog timer. <b>Bits</b> <b>3 2</b> = 0 0 clock rate 1/4Hz = 0 1 clock rate 1Hz = 1 0 clock rate 1/2 Hz = 1 1 clock rate 1MHz
1~0	Reserved.	

This register is only useful when LRESET is logic 0. This timer is count by CRE7h and CRE8h combination.

**CR E8h. VID/BUSSEL's WDTO Software Reset 5s counter Register; Default 14h (LRESET=0)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Setting of 5 second watch dog time out counter. Default is 8'h14. (Default 5 second is counted from 1/4Hz*14h, which is 0.25*20=5 )

This register is only useful when LRESET is logic 0. This timer is count by CRE7h and CRE8h combination.

**CR ECh. (SUSLED Control Register; Default 01h)**

BIT	READ / WRITE	DESCRIPTION
7~5	R/W	SUSLED output frequency select <b>Bits</b> <b>7 6 5</b> =0 0 0 always high (Default) =0 0 1 always low =0 1 0 4Hz =0 1 1 2Hz =1 0 0 1Hz =1 0 1 1/2Hz =1 1 0 1/4Hz
4	R / W	SUSLED drops immediately when SUSC# is low 0: Disable (Default) 1: Enable
3~0	Reserved.	

**CR EDh. (VID/BUEESL WDT software Reset switches Register; Default 00h)**

BIT	READ / WRITE	DESCRIPTION
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BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R/W	Watchdog timer software reset for VID and BUSSEL.(Need Enable Global Register CR2Dh,bit0 first.) 0: Disable 1: Enabled (While set this bit to enable, WDT starting count down to 0, then auto clear this bit to disable. )

The VID/BUSSEL's WDTO timer is set by CRE7 and CRE8.

#### CR EEh. (Reset Source Registers; Default 88h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable WDT as the BUSSEL reset source. (Need Enable CREDh,bit0 first.) 0: Disable 1: Enabled
6	R / W	Enable PWROK as the BUSSEL reset source. 0: Disable 1: Enabled
5	R / W	Enable LRESET as the BUSSEL reset source. 0: Disable 1: Enabled
4	R / W	Enable VID_RST# (pin 53) as the BUSSEL reset source. 0: Disable 1: Enabled
3	R / W	Enable WDT as the VID reset source. (Need Enable CREDh,bit0 first.) 0: Disable 1: Enabled
2	R / W	Enable PWROK as the VID reset source. 0: Disable 1: Enable
1	R / W	Enable LRESET as the VID reset source. 0: Disable 1: Enable
0	R/W	Enable VID_RST# (pin 53) as the VID reset source. 0: Disable 1: Enabled

#### CR EFh. (Rolling Rate Registers; Default 00h)

BIT	READ / WRITE	DESCRIPTION
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BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Rolling rate value (Can't input FFh to this register.) Rolling rate = ~400ns * (Rolling rate value+1).

**CR F3h. (SPI Flash ROM size select Registers; Default 04h)**

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2~0	R/W	SPI Flash ROM size select. <b>Bits</b> <b>2 1 0</b> = 0 0 0 1Mbit = 0 0 1 2Mbit = 0 1 0 4Mbit = 0 1 1 8Mbit = 1 0 0 16Mbit (Default) = 1 0 1 32Mbit = 1 1 0 64Mbit

**21.15 Logical Device F (GPIO Push-Pull/OD Select)**
**CR E0h (Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GP1 Push-Pull/OD select 0:Push-Pull 1:Open Drain

**CR E1h (Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GP2 Push-Pull/OD select 0:Push-Pull 1:Open Drain

**CR E2h (Default FDh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GP3 Push-Pull/OD select 0:Push-Pull (Push-Pull is the default for GP31) 1:Open Drain

**CR E3h (Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GP4 Push-Pull/OD select 0:Push-Pull 1:Open Drain

**CR E4h (Default F7h)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GP5 Push-Pull/OD select 0:Push-Pull (Push-Pull is the default for GP53) 1:Open Drain

**CR E5h (Default CBh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GP6 Push-Pull/OD select 0:Push-Pull (Push-Pull is the default for GP62, GP64 and GP65) 1:Open Drain

**CR E6h (Default 3Fh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GP7 Push-Pull/OD select 0:Push-Pull (Push-Pull is the default for GP76 and GP77) 1:Open Drain

**CR E7h (Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GP8 Push-Pull/OD select 0:Push-Pull 1:Open Drain

**CR E8h (Default FFh)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GP9 Push-Pull/OD select 0:Push-Pull 1:Open Drain

**CR E9h (Default 00h)**

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	BANK selection of user definition register. 0000: BANK 0 0001: BANK 1 ... 1111: BANK 15

**CR F0 ~ FFh (Default xxh) BANK 0**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 1**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 2**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 3**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 4**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 5**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 6**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 7**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 8**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 9**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 10**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 11**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 12**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 13**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 14**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

**CR F0 ~ FFh (Default xxh) BANK 15**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	User define register.

## 22. SPECIFICATIONS

### 22.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3VCC+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
TA	Operating Temperature	0 to +70	°C
TSTG	Storage Temperature	-55 to +150	°C

**Note:** Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### 22.2 DC CHARACTERISTICS

( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 5\%$ ,  $V_{SS} = 0\text{V}$ )

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	IBAT			4	$\mu\text{A}$	VBAT = 3.0V
ACPI Stand-by Power Supply Quiescent Current	I <sub>VS</sub> B			2.0	mA	V <sub>SB</sub> = 3.3 V, All ACPI pins are not connected.
VCC Quiescent Current	I <sub>VCC</sub>			35	mA	V <sub>SB</sub> = 3.3 V V <sub>CC</sub> (AVCC)= 3.3 V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
V <sub>TT</sub> Quiescent Current	I <sub>VTT</sub>			1	mA	V <sub>SB</sub> = 3.3 V V <sub>CC</sub> (AVCC)= 3.3 V V <sub>TT</sub> = 1.2V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
<b>I/O<sub>8t</sub> – TTL-level, bi-directional pin with 8mA source-sink capability</b>						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Voltage	V <sub>IL</sub>			0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0			V	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 8 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = - 8 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/O<sub>12t</sub> – TTL-level, bi-directional pin with 12mA source-sink capability</b>						
Input Low Voltage	V <sub>IL</sub>			0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0			V	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -12 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/O<sub>24t</sub> – TTL-level, bi-directional pin with 24mA source-sink capability</b>						
Input Low Voltage	V <sub>IL</sub>			0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0			V	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 24 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -24 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/O<sub>12tp3</sub> – 3.3V TTL-level, bi-directional pin with 12mA source-sink capability</b>						
Input Low Voltage	V <sub>IL</sub>			0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0			V	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -12 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/O<sub>12ts</sub> – TTL-level, Schmitt-trigger, bi-directional pin with 12mA source-sink capability</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	
Hysteresis	V <sub>TH</sub>	0.5	1.2		V	V <sub>CC</sub> =3.3V
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -12 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/O<sub>24ts</sub> – TTL-level, Schmitt-trigger, bi-directional pin with 24mA source-sink capability</b>						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	
Hysteresis	V <sub>TH</sub>	0.5	1.2		V	V <sub>CC</sub> = 3.3V
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 24 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -24 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/O<sub>24tsp3</sub> – 3.3V TTL-level, Schmitt-trigger, bi-directional pin with 24mA source-sink capability</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	
Hysteresis	V <sub>TH</sub>	0.5	1.2		V	V <sub>CC</sub> = 3.3V
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 24 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -24 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/OD<sub>12t</sub> – TTL-level, bi-directional pin and open-drain output with 12mA sink capability</b>						
Input Low Voltage	V <sub>IL</sub>			0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0			V	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/OD<sub>16t</sub> – TTL-level, bi-directional pin and open-drain output with 16mA sink capability</b>						
Input Low Voltage	V <sub>IL</sub>			0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0			V	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 16 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/OD<sub>24t</sub> – TTL-level, bi-directional pin and open-drain output with 24mA sink capability</b>						
Input Low Voltage	V <sub>IL</sub>			0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0			V	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 24 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/O<sub>12tp3</sub> – 3.3V TTL-level, bi-directional pin and open-drain output with 12mA source-sink capability</b>						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Voltage	V <sub>IL</sub>			0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0			V	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -12 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/OD<sub>16ts</sub> – TTL-level, Schmitt-trigger, bi-directional pin and open-drain output with 16mA sink capability</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	
Hystersis	V <sub>TH</sub>	0.5	1.2		V	V <sub>CC</sub> =3.3V
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 16 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/OD<sub>24ts</sub> – TTL level, Schmitt-trigger, bi-directional pin and open-drain output with 24mA sink capability</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	
Hystersis	V <sub>TH</sub>	0.5	1.2		V	V <sub>CC</sub> =3.3V
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 24 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
<b>I/OD<sub>12cs</sub> – CMOS-level, Schmitt-trigger, bi-directional pin and open-drain output with 12mA sink capability</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	V <sub>CC</sub> = 3.3 V
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	V <sub>CC</sub> = 3.3 V
Hystersis	V <sub>TH</sub>	0.5	1.2		V	V <sub>CC</sub> = 3.3 V
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3 V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0 V
<b>I/OD<sub>16cs</sub> – CMOS-level, Schmitt-trigger, bi-directional pin and open-drain output with 16mA sink capability</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	V <sub>CC</sub> = 3.3 V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	V <sub>CC</sub> = 3.3 V
Hysteresis	V <sub>TH</sub>	0.5	1.2		V	V <sub>CC</sub> = 3.3 V
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 16 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3 V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0 V
<b>I/OD<sub>12csd</sub> – CMOS–level, Schmitt-trigger, bi-directional pin with internal pulled-down resistor and open-drain output with 12mA sink capability</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	V <sub>CC</sub> = 3.3 V
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	V <sub>CC</sub> = 3.3 V
Hysteresis	V <sub>TH</sub>	0.5	1.2		V	V <sub>CC</sub> = 3.3 V
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3 V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0 V
<b>I/OD<sub>12csu</sub> – CMOS–level, Schmitt-trigger, bi-directional pin with internal pulled-up resistor and open-drain output with 12mA sink capability</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	V <sub>CC</sub> = 3.3 V
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	V <sub>CC</sub> = 3.3 V
Hysteresis	V <sub>TH</sub>	0.5	1.2		V	V <sub>CC</sub> = 3.3 V
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3 V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0 V
<b>O4 - Output pin with 4mA source-sink capability</b>						
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 4 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -4 mA
<b>O8 – Output pin with 8mA source-sink capability</b>						
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 8 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -8 mA
<b>O12 – Output pin with 12mA source-sink capability</b>						
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 12 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -12 mA
<b>O16 – Output pin with 16mA source-sink capability</b>						
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 16 mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -16 mA
<b>O24 – Output pin with 24mA source-sink capability</b>						
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 24 mA

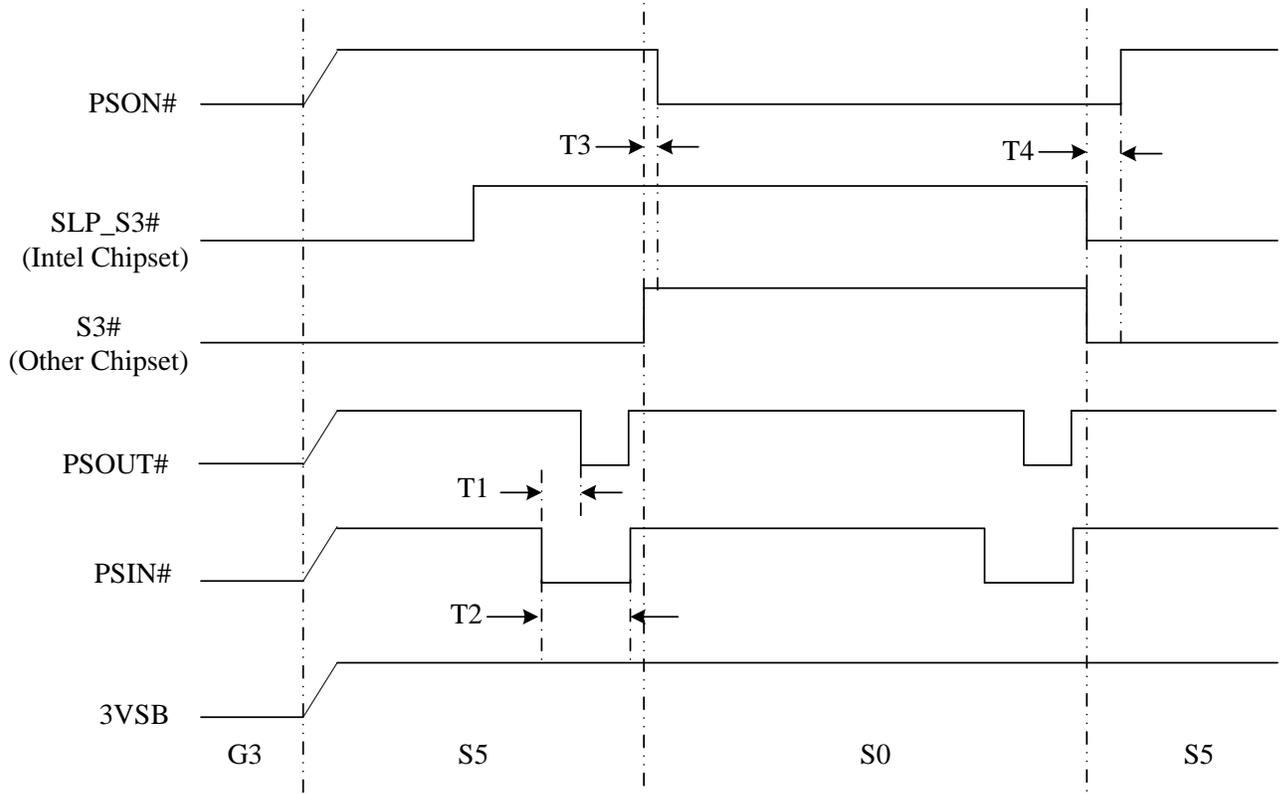
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Output High Voltage	VOH	2.4			V	IOH = -24 mA
<b>O<sub>12p3</sub> – 3.3V output pin with 12mA source-sink capability</b>						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
<b>O<sub>24p3</sub> – 3.3V output pin with 24mA source-sink capability</b>						
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
Output High Voltage	VOH	2.4			V	IOH = -24 mA
<b>OD<sub>12</sub> – Open-drain output pin with 12mA sink capability</b>						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
<b>OD<sub>24</sub> – Open-drain output pin with 24mA sink capability</b>						
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
<b>OD<sub>12p3</sub> – 3.3V open-drain output pin with 12mA sink capability</b>						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
<b>IN<sub>t</sub> – TTL-level input pin</b>						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	μA	VIN = 3.3 V
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
<b>IN<sub>tp3</sub> – 3.3V TTL-level input pin</b>						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	μA	VIN = 3.3V
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
<b>IN<sub>td</sub> – TTL-level input pin with internal pulled-down resistor</b>						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	μA	VIN = 3.3 V
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
<b>IN<sub>tu</sub> – TTL-level input pin with internal pulled-up resistor</b>						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	μA	VIN = 3.3 V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Leakage	ILIL			-10	$\mu\text{A}$	$V_{\text{IN}} = 0\text{ V}$
<b>IN<sub>ts</sub> – TTL-level, Schmitt-trigger input pin</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	$V_{\text{CC}} = 3.3\text{ V}$
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	$V_{\text{CC}} = 3.3\text{ V}$
Hysteresis	V <sub>TH</sub>	0.5	1.2		V	$V_{\text{CC}} = 3.3\text{ V}$
Input High Leakage	ILIH			+10	$\mu\text{A}$	$V_{\text{IN}} = 3.3\text{ V}$
Input Low Leakage	ILIL			-10	$\mu\text{A}$	$V_{\text{IN}} = 0\text{ V}$
<b>IN<sub>tsp3</sub> – 3.3 V TTL-level, Schmitt-trigger input pin</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	$V_{\text{CC}} = 3.3\text{ V}$
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	$V_{\text{CC}} = 3.3\text{ V}$
Hysteresis	V <sub>TH</sub>	0.5	1.2		V	$V_{\text{CC}} = 3.3\text{ V}$
Input High Leakage	ILIH			+10	$\mu\text{A}$	$V_{\text{IN}} = 3.3\text{ V}$
Input Low Leakage	ILIL			-10	$\mu\text{A}$	$V_{\text{IN}} = 0\text{ V}$
<b>IN<sub>c</sub> – CMOS-level input pin</b>						
Input Low Voltage	V <sub>IL</sub>			0.3 V <sub>CC</sub>	V	
Input High Voltage	V <sub>IH</sub>	0.7 V <sub>CC</sub>			V	
Input High Leakage	ILIH			+10	$\mu\text{A}$	$V_{\text{IN}} = V_{\text{CC}} = 3.3\text{ V}$
Input Low Leakage	ILIL			-10	$\mu\text{A}$	$V_{\text{IN}} = 0\text{ V}$
<b>IN<sub>cd</sub> – CMOS-level input pin with internal pulled-down resistor</b>						
Input Low Voltage	V <sub>IL</sub>			0.3 V <sub>CC</sub>	V	
Input High Voltage	V <sub>IH</sub>	0.7 V <sub>CC</sub>			V	
Input High Leakage	ILIH			+10	$\mu\text{A}$	$V_{\text{IN}} = V_{\text{CC}} = 3.3\text{ V}$
Input Low Leakage	ILIL			-10	$\mu\text{A}$	$V_{\text{IN}} = 0\text{ V}$
Input Low Voltage	V <sub>IL</sub>			0.3 V <sub>CC</sub>	V	
<b>IN<sub>cu</sub> – CMOS-level input pin with internal pulled-up resistor</b>						
Input High Voltage	V <sub>IH</sub>	0.7 V <sub>CC</sub>			V	
Input High Leakage	ILIH			+10	$\mu\text{A}$	$V_{\text{IN}} = V_{\text{CC}} = 3.3\text{ V}$
Input Low Leakage	ILIL			-10	$\mu\text{A}$	$V_{\text{IN}} = 0\text{ V}$
<b>IN<sub>cs</sub> – CMOS-level, Schmitt-trigger input pin</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	1.3	1.5	1.7	V	$V_{\text{CC}} = 3.3\text{ V}$

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Hysteresis	V <sub>TH</sub>	1.5	2		V	V <sub>CC</sub> = 3.3V
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0 V
<b>IN<sub>CSU</sub> – CMOS–level, Schmitt-trigger input pin with internal pulled-up resistor</b>						
Input Low Threshold Voltage	V <sub>t-</sub>	0.5	0.8	1.1	V	V <sub>CC</sub> = 3.3V
Input High Threshold Voltage	V <sub>t+</sub>	1.6	2.0	2.4	V	V <sub>CC</sub> = 3.3V
Hysteresis	V <sub>TH</sub>	0.5	1.2		V	V <sub>CC</sub> = 3.3V
Input High Leakage	I <sub>LIH</sub>			+10	μA	V <sub>IN</sub> = 3.3V
Input Low Leakage	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0 V
<b>AOUT – Analog output</b>						
		N.A.				
<b>IN<sub>V1S</sub> – VID input pin for INTEL® VRM10.0, and VRM11 design</b>						
Input Low Voltage	V <sub>IL</sub>			0.4	V	
Input High Voltage	V <sub>IH</sub>	0.6			V	
<b>IN<sub>V2S</sub> – VID input pin for AMD™VRM design</b>						
Input Low Voltage	V <sub>IL</sub>			0.8	V	
Input High Voltage	V <sub>IH</sub>	1.4			V	
<b>I/O<sub>V3</sub> – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® PECl</b>						
Input Low Voltage	V <sub>IL</sub>	0.275V <sub>tt</sub>		0.5V <sub>tt</sub>	V	
Input High Voltage	V <sub>IH</sub>	0.55V <sub>tt</sub>		0.725V <sub>tt</sub>	V	
Output Low Voltage	V <sub>OL</sub>			0.25V <sub>tt</sub>	V	
Output High Voltage	V <sub>OH</sub>	0.75V <sub>tt</sub>			V	
Hysteresis	V <sub>Hys</sub>	0.1V <sub>tt</sub>			V	

22.3 AC CHARACTERISTICS

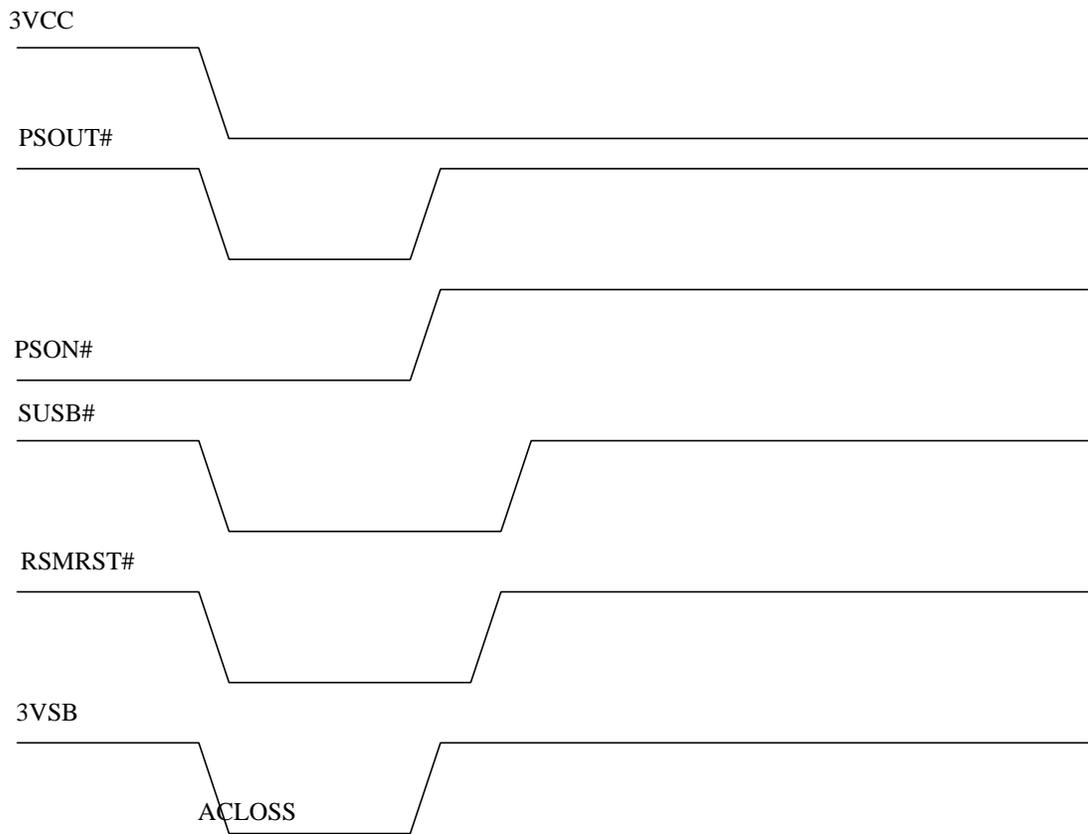
22.3.1 Power On / Off Timing



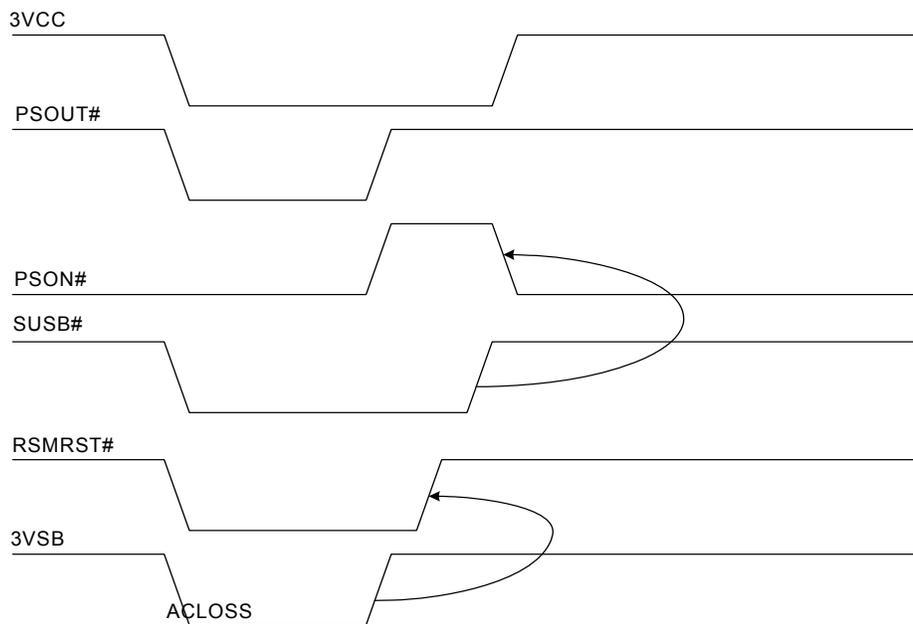
	T1	T2	T3	T4
<b>IDEAL TIMING</b>	64ms	Over 64ms at least	< 10ns	32ms

22.3.2AC Power Failure Resume Timing

1. CRE4 bit [6:5] =00 is selected to “Always Off” state (“OFF” means always being turned off or the previous state is off)



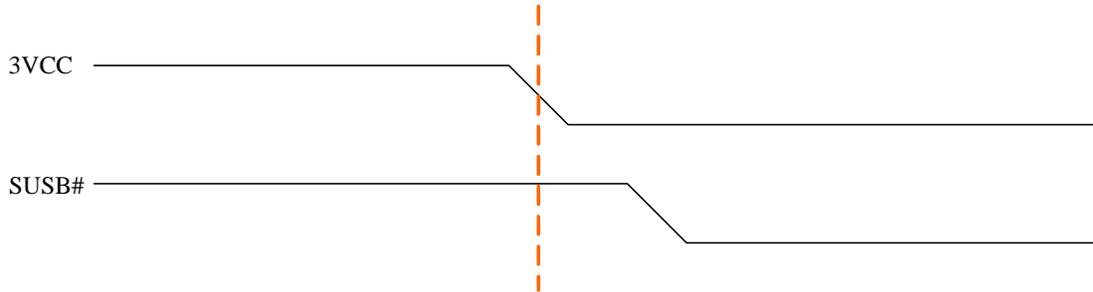
- 2. CRE4 bit [6:5] =01 is selected to “Always On” state  
 (“ON” means always being turned on or the previous state is on)



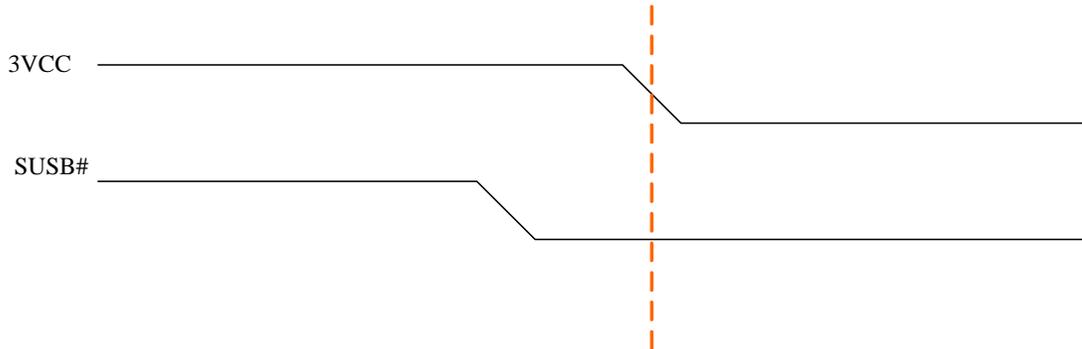
3. CRE4 bit [6:5] =10 is selected to “Pre-state” state

What’s the definition of former state at AC power failure?

- 1) The previous state is “ON”  
VCC falls to 2.6V and SUSB# keeps at VIH 2.0V



- 2) The previous state is “OFF”  
VCC fall to 2.6V and SUSB# keeps at VIL 0.8V



To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the W83667HG-B adds the option of “User define mode” for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be “On” or “Off”. According to this setting, the system chooses the state after the AC power recovery.

Please refer to the descriptions of bit 6~5 of CR E4h and bit 4 of CR E6h in Logical Device A.

**CR E4h**

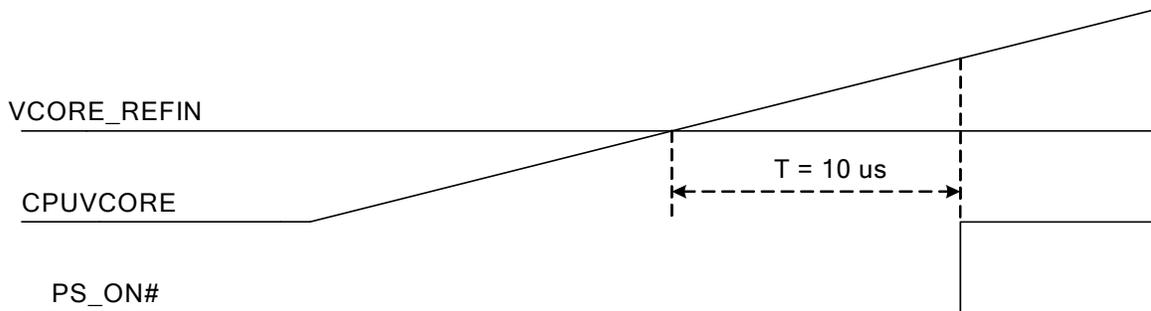
BIT	READ/WRITE	DESCRIPTION
6~5	R / W	Power-loss control bits (VBAT) <b>Bit 6 5</b> 1 1: User defined mode for power loss last-state. (Note. The last-state flag is setting by CRE6[4])

CR E6h

BIT	READ/WRITE	DESCRIPTION
4	R / W	Power-loss Last State Flag. (VBAT) 0: ON 1: OFF. (Default)

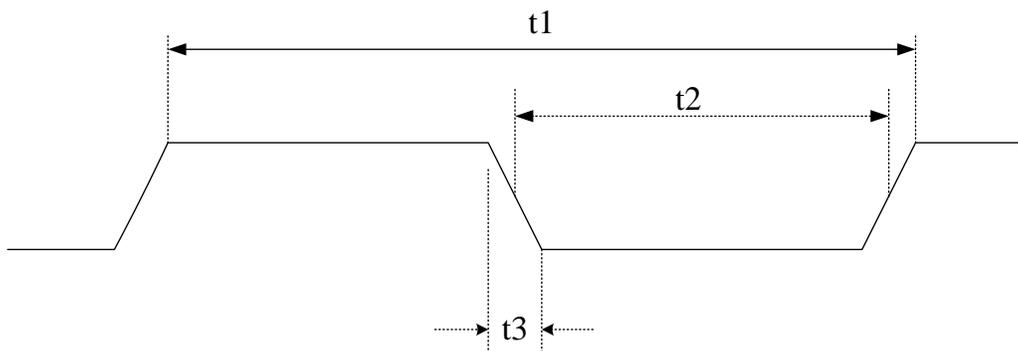
22.3.3 CPUVCORE & VCORE\_REFIN Timing

When CPUVCORE (Tolerance +/- 100mv) is over than VCORE\_REFIN last for 10 $\mu$ s second, PS\_ON# will be immediate locked in the high state. This situation can only reset by RSMRST#.



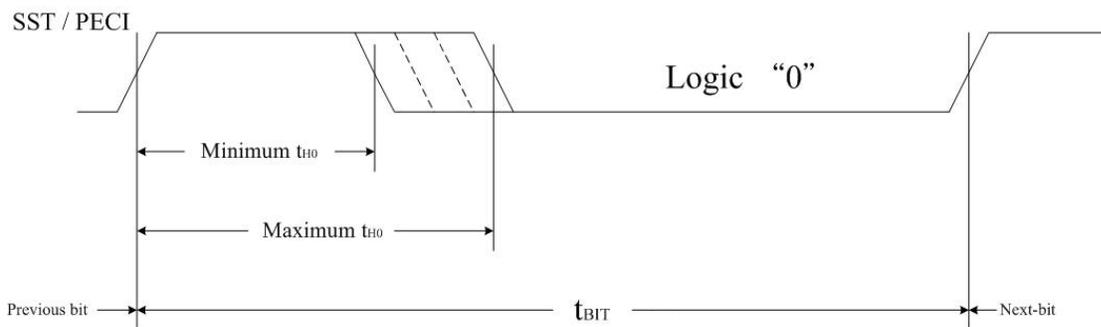
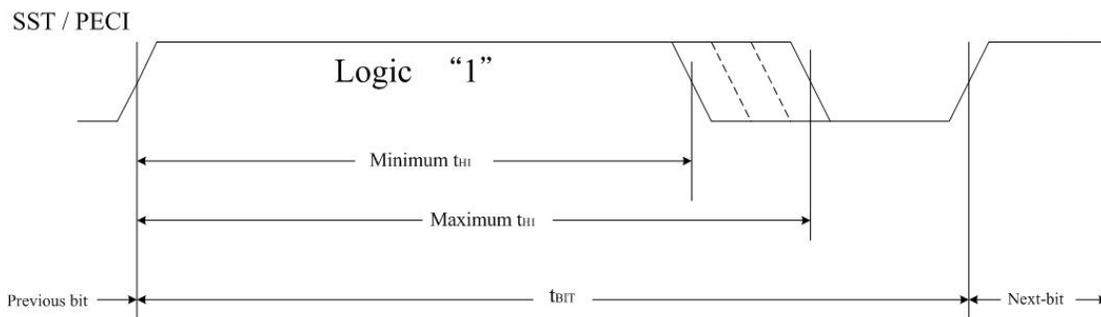
22.3.4 Clock Input Timing

PARAMETER	48MHZ / 24MHZ		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%



PARAMETER	DESCRIPTION	48MHZ / 24MHZ			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		20.8 / 41.7		ns
t2	Clock high time/low time	9 / 19	10 / 21		ns
t3	Clock rising time/falling time (0.4V~2.4V)			3	ns

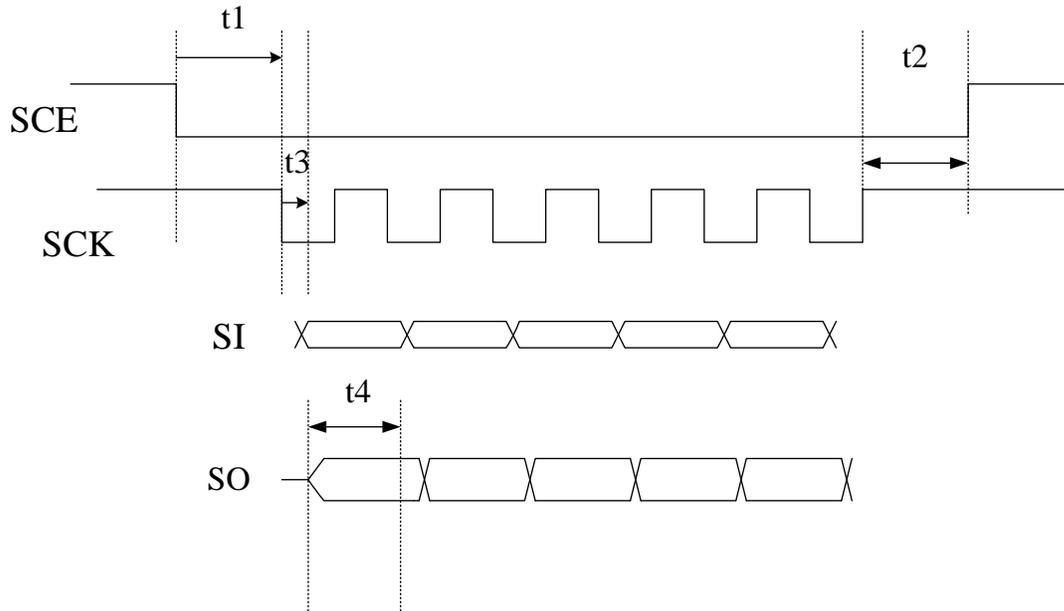
22.3.5 PECl Timing



SYMBOL		MIN	TYP	MAX	UNITS
$t_{BIT}$	Client	0.495		500	$\mu$ S
	Originator	0.495		250	

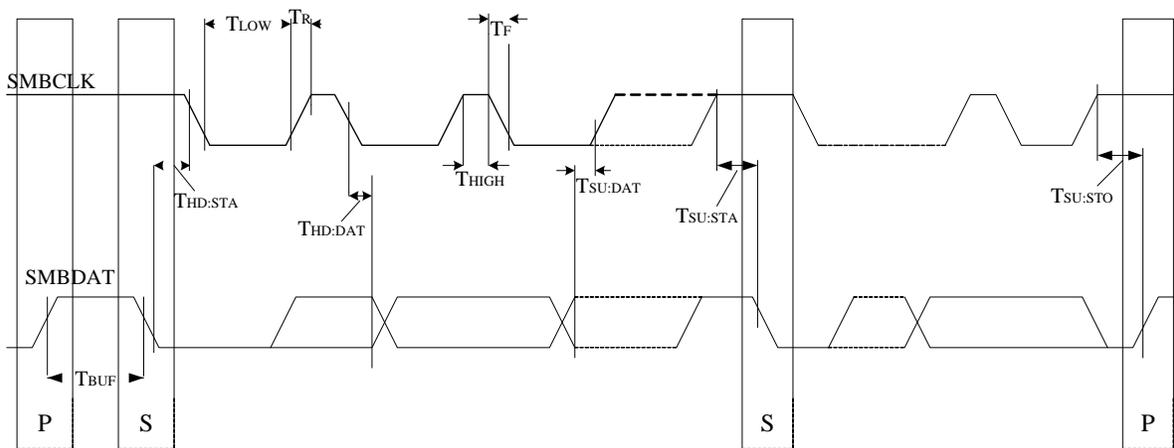
$t_{H1}$	0.6	3/4	0.8	$\times t_{BIT}$
$t_{H0}$	0.2	1/4	0.4	$\times t_{BIT}$

22.3.6SPI Timing



DESCRIPTION	NS	MIN	TYPE	MAX
Enable to first clock falling	t1	25ns	-	35ns
Disable after last clock rising	t2	40ns	-	50ns
Output hold time	t3	-	-	5ns
Input setup time	t4	5ns	-	-
Input hold time	t5	6ns	-	-

## 22.3.7 SMBus Timing



## 22.3.8 Floppy Disk Drive Timing

FDC: Data rate = 1MB, 500KB, 300KB, 250KB/sec.

PARAMETER	SYM.	MIN.	TYP. (NOTE 1)	MAX.	UNIT
DIR# setup time to STEP#	TDST	1.0/1.6 /2.0/4.0			$\mu$ S
DIR# hold time from STEP#	TSTD	24/40 /48/96			$\mu$ S
STEP# pulse width	TSTP	6.8/11.5 /13.8/27. 8	7/11.7 /14/28	7.2/11.9 /14.2/28. 2	$\mu$ S
STEP# cycle width	TSC	NOTE 2	NOTE 2	NOTE 2	mS
INDEX# pulse width	TIDX	125/250 /417/500			nS
RDATA# pulse width	TRD	40			nS
WD# pulse width	TWD	100/185 /225/475	125/210 /250/500	150/235 /275/525	nS

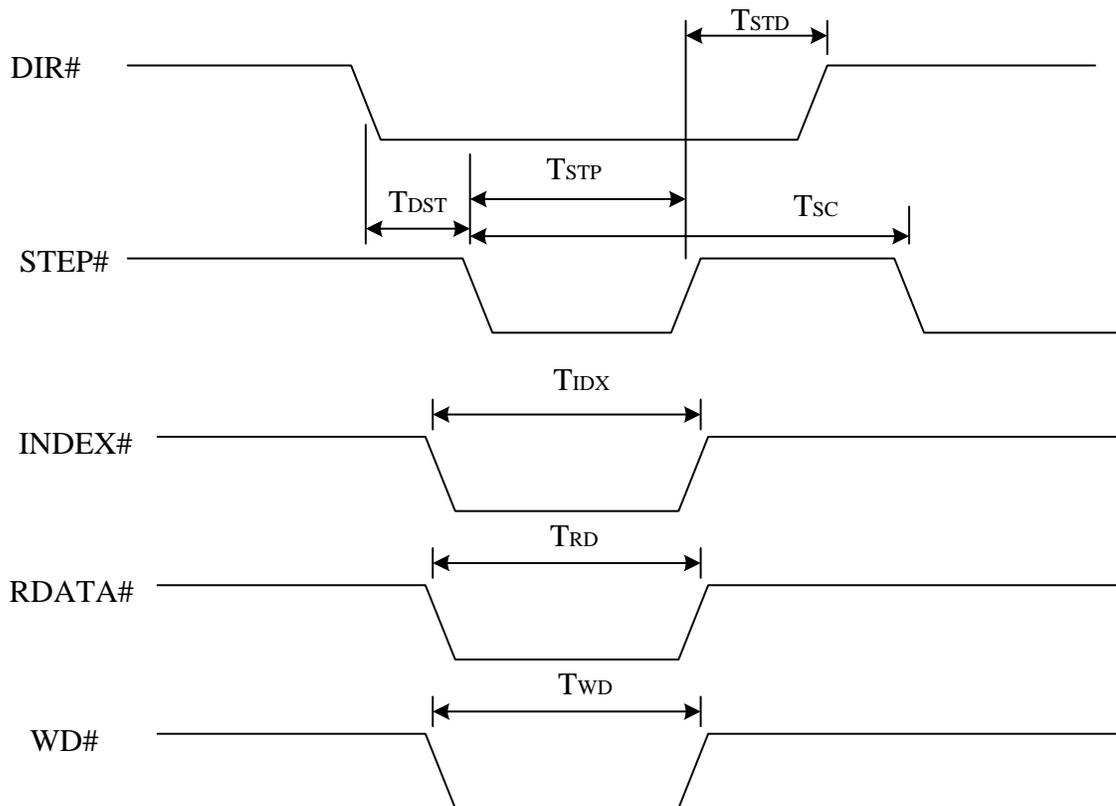
## Notes:

1. Typical values for  $T = 25^{\circ}\text{C}$  and normal supply voltage.
2. Programmable from 0.5 mS through 32 mS as described in step rate table.  
(Please refer to the description of the SPECIFY command set.)

Step Rate Table

DATA RATE SRT	1MB/S	500KB/S	300KB/S	250KB/S
0	8	16	26.7	32
1	7.5	15	25	30
...	...	...	...	...
E	1.0	2	3.33	4
F	0.5	1	1.67	2

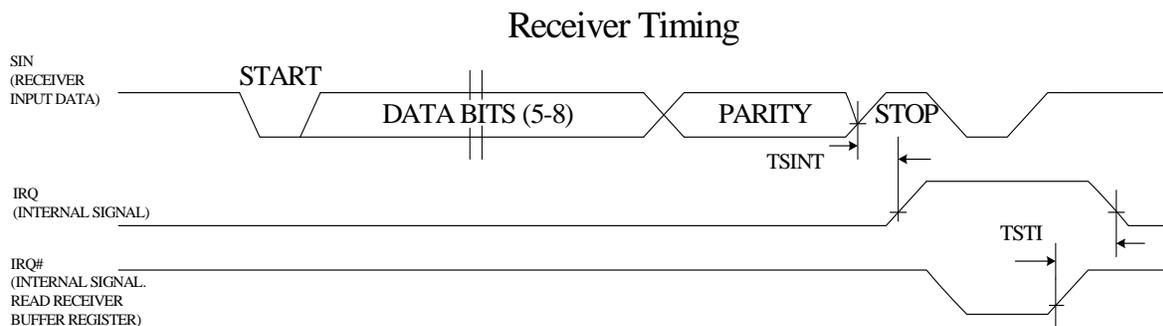
Floppy Disk Driving Timing



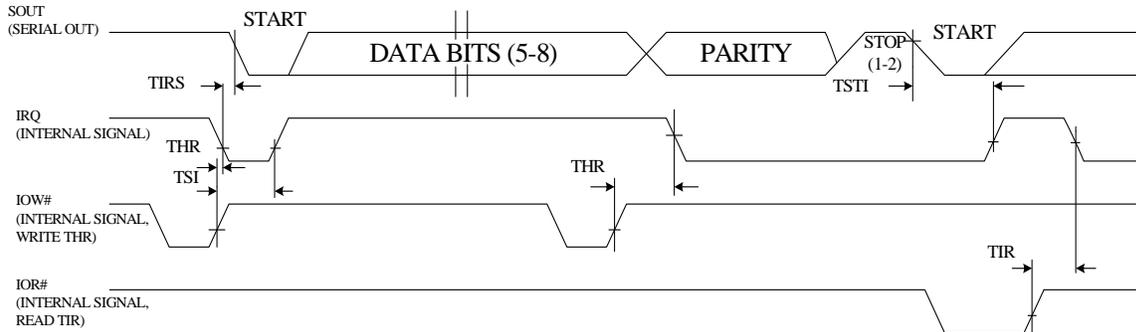
22.3.9UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{\text{IOR}}$ Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial $\overline{\text{IOW}}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from $\overline{\text{IOR}}$ to Reset Interrupt	TIR		8	250	nS
Delay from $\overline{\text{IOR}}$ to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from $\overline{\text{IOR}}$	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		$2^{16}-1$	

UART Receiver Timing



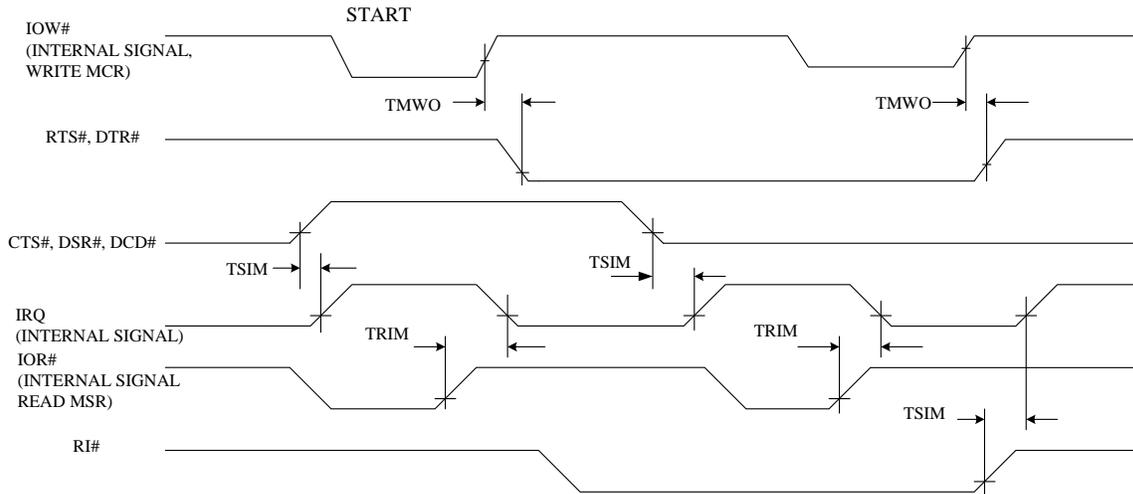
UART Transmitter Timing



22.3.9.1. Modem Control Timing

Modem Control Timing

MODEM Control Timing



22.3.10 Parallel Port Mode Parameters

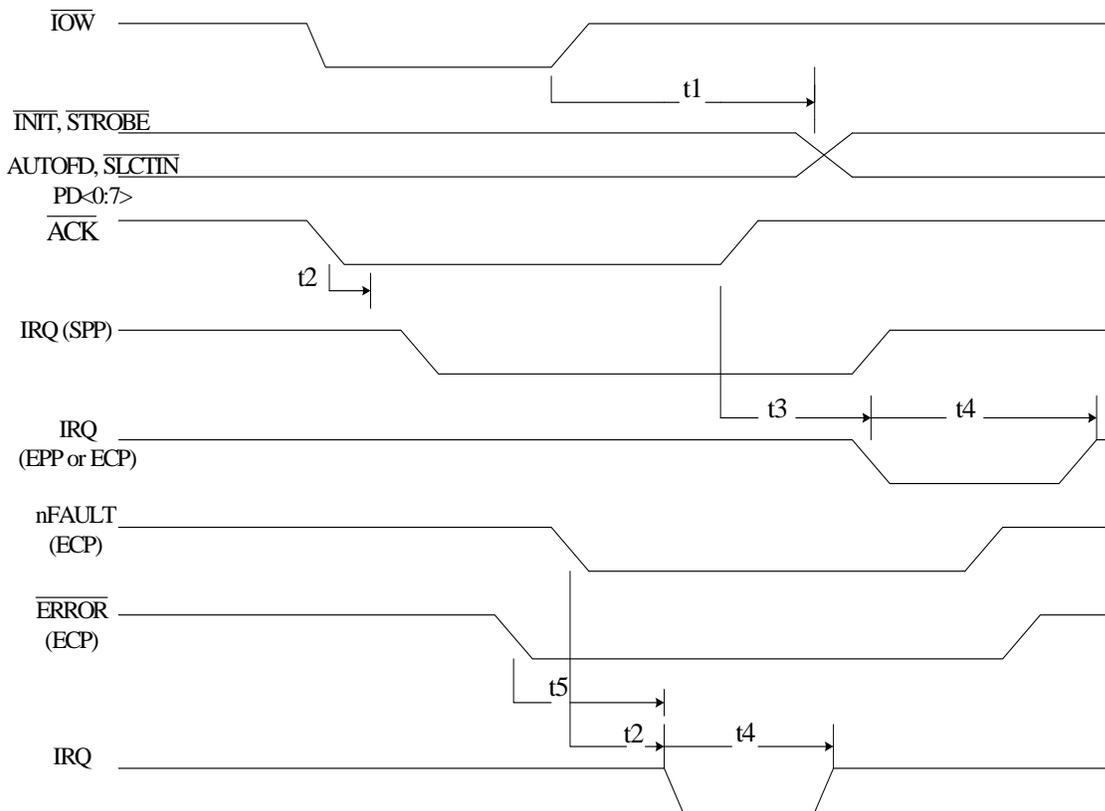
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, INDEX, STROBE, AUTOFD Delay from IOW	t1			100	nS
IRQ Delay from ACK, nFAULT	t2			60	nS
IRQ Delay from IOW	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
ERROR Active to IRQ Active	t5			105	nS

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, INDEX, STROBE, AUTOFD Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$ , nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS

22.3.11 Parallel Port

22.3.11.1. Parallel Port Timing

Parallel Port Timing



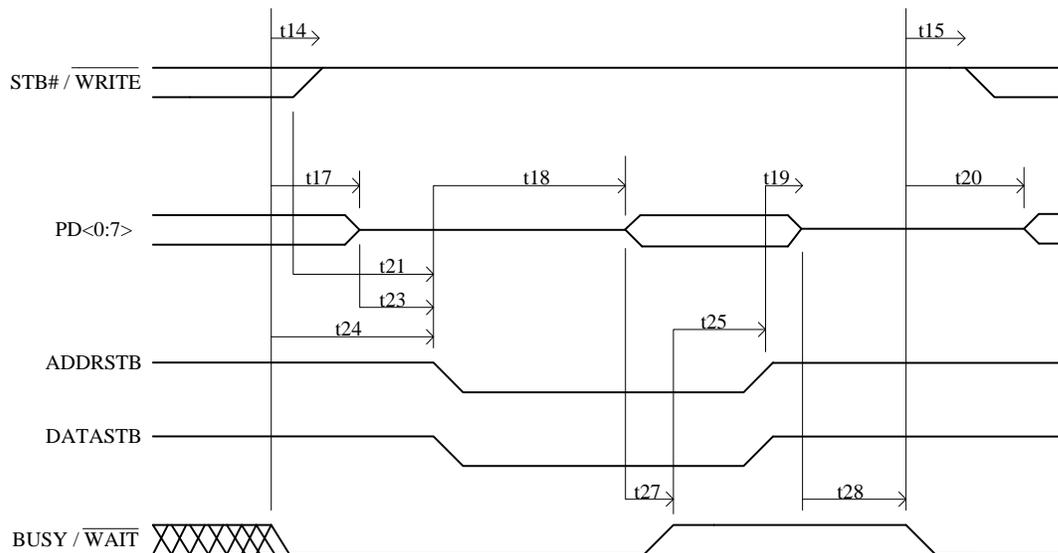
## 22.3.11.2. EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		$\mu\text{S}$
PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOR}}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{\text{IOR}}$ Deasserted	t2	0		nS
$\overline{\text{IOR}}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{\text{IOR}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t4	40		
$\overline{\text{IOR}}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{\text{IOR}}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	$\mu\text{S}$
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{\text{WRITE}}$ Deasserted to $\overline{\text{IOR}}$ Asserted	t13	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{IOR}}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		$\mu\text{S}$

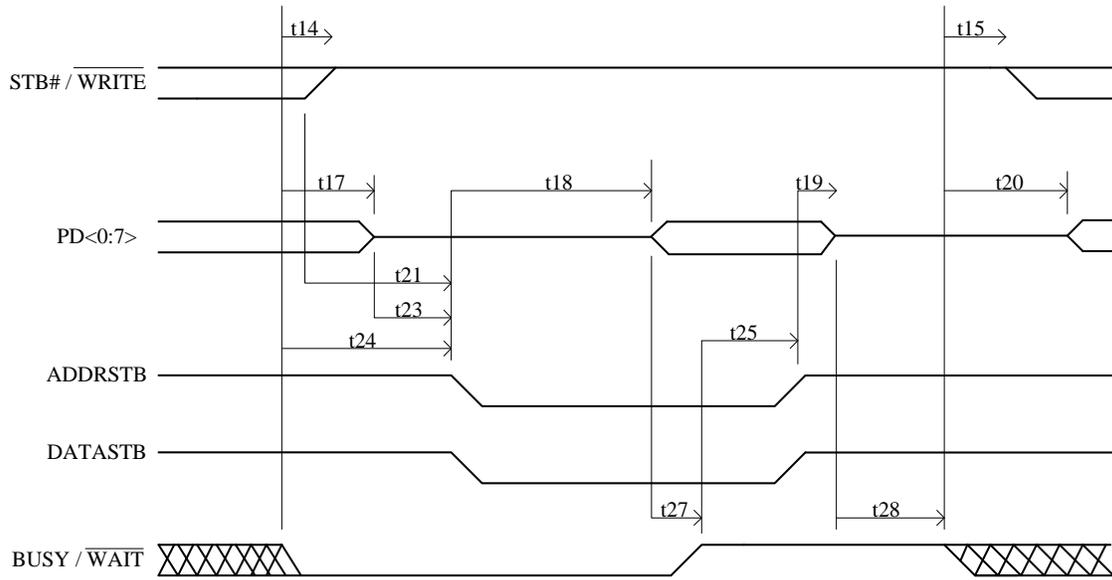
### 22.3.11.3. EPP Data or Address Read Cycle (EPP Version 1.9)

#### EPP Data or Address Read Cycle (EPP Version 1.9)



22.3.11.4. EPP Data or Address Read Cycle (EPP Version 1.7)

EPP Data or Address Read Cycle (EPP Version 1.7)



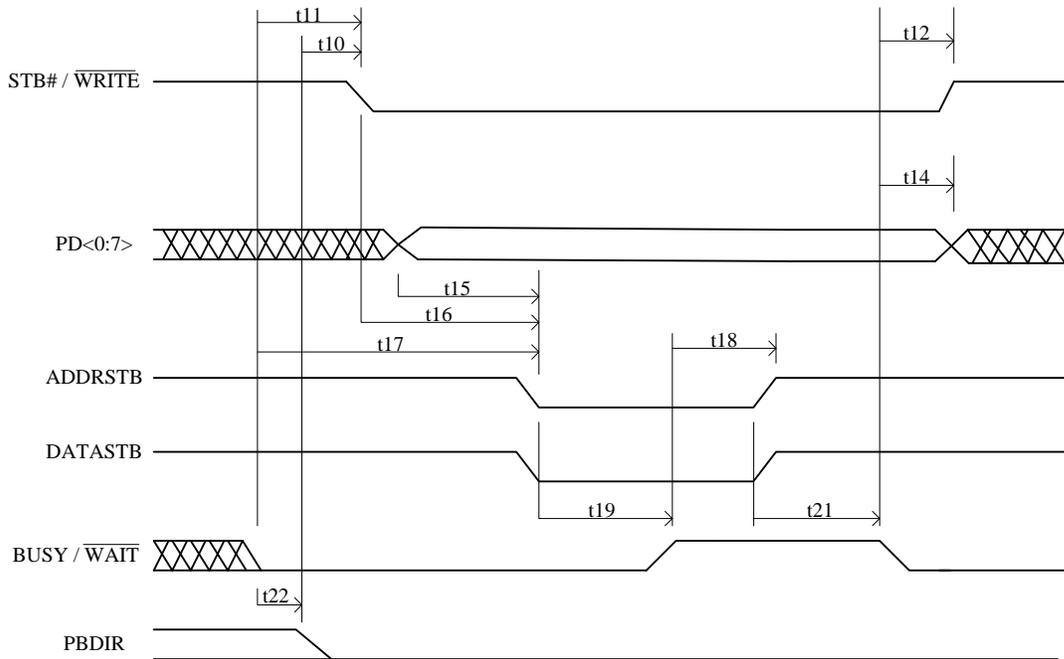
## 22.3.11.5. EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	$\mu\text{S}$
Time out	t20	10	12	$\mu\text{S}$
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	$\mu\text{S}$
Time out	t20	10	12	$\mu\text{S}$

PARAMETER	SYM.	MIN.	MAX.	UNIT
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{WRITE}}$ Deasserted and PD invalid	t22	0		nS
$\overline{\text{WRITE}}$ to Command Asserted	t16	5	35	nS

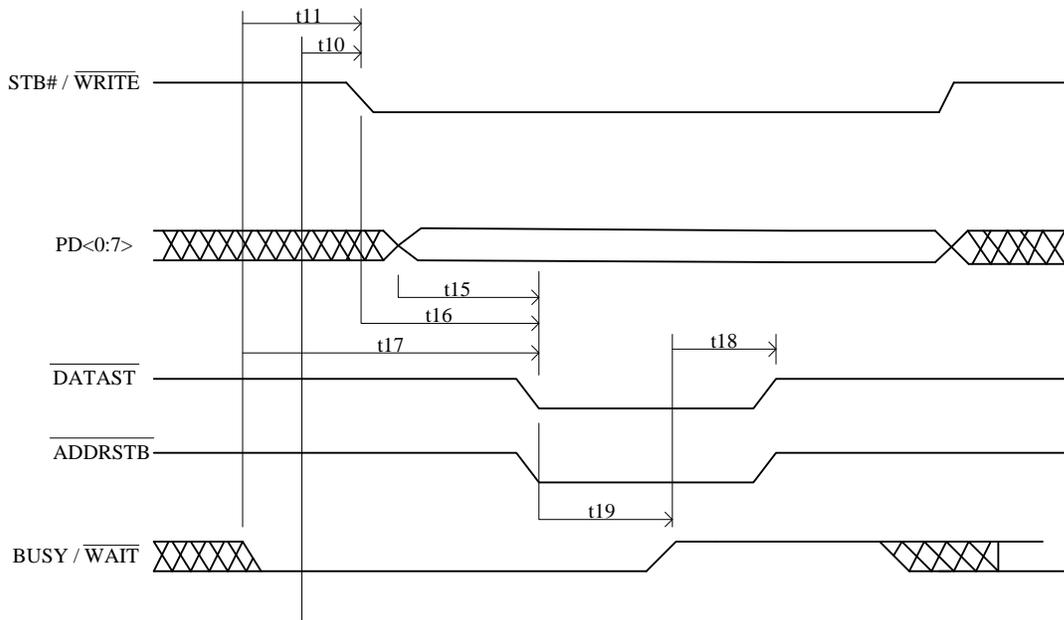
22.3.11.6. EPP Data or Address Write Cycle (EPP Version 1.9)

EPP Data or Address Write Cycle (EPP Version 1.9)



22.3.11.7. EPP Data or Address Write Cycle (EPP Version 1.7)

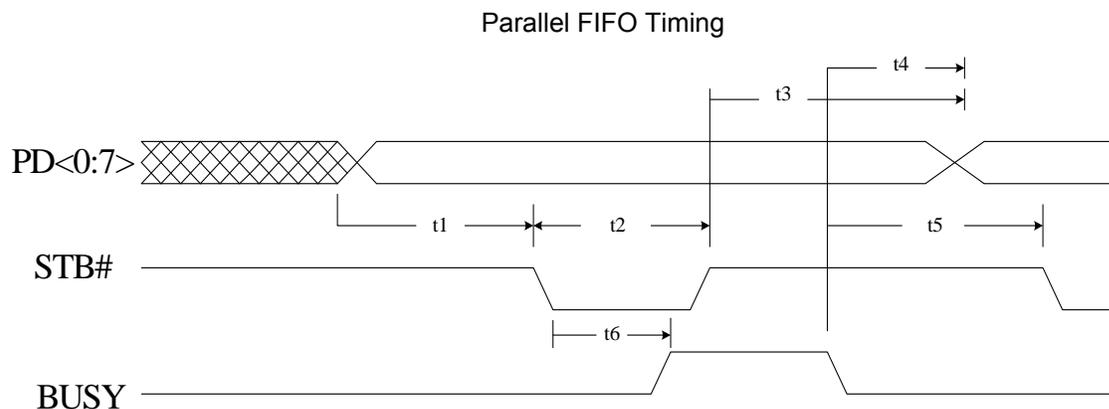
EPP Data or Address Write Cycle (EPP Version 1.7)



22.3.11.8. Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

## 22.3.11.9. Parallel FIFO Timing

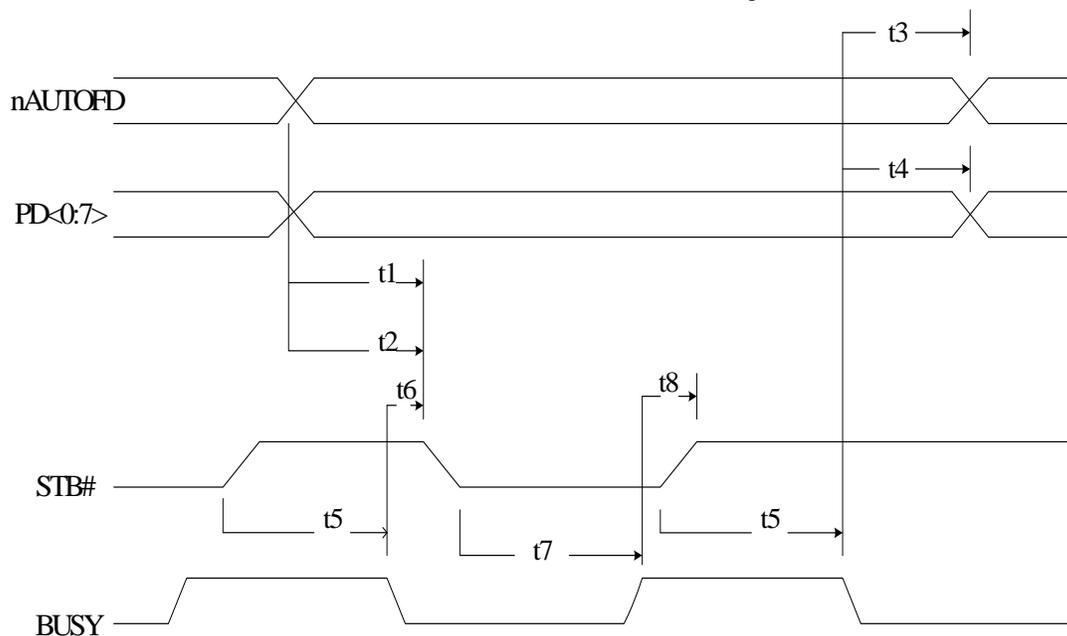


## 22.3.11.10. ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

22.3.11.11. ECP Parallel Port Forward Timing

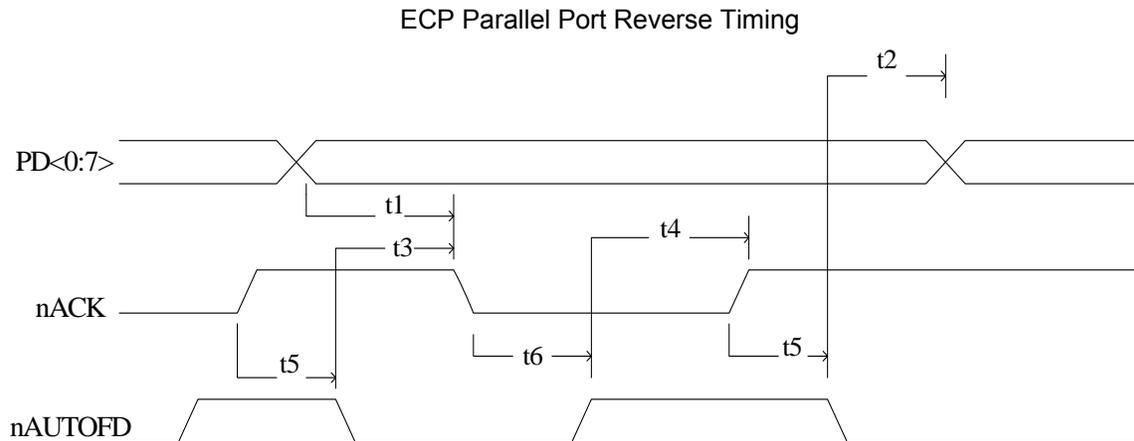
ECP Parallel Port Forward Timing



22.3.11.12. ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

## 22.3.11.13. ECP Parallel Port Reverse Timing

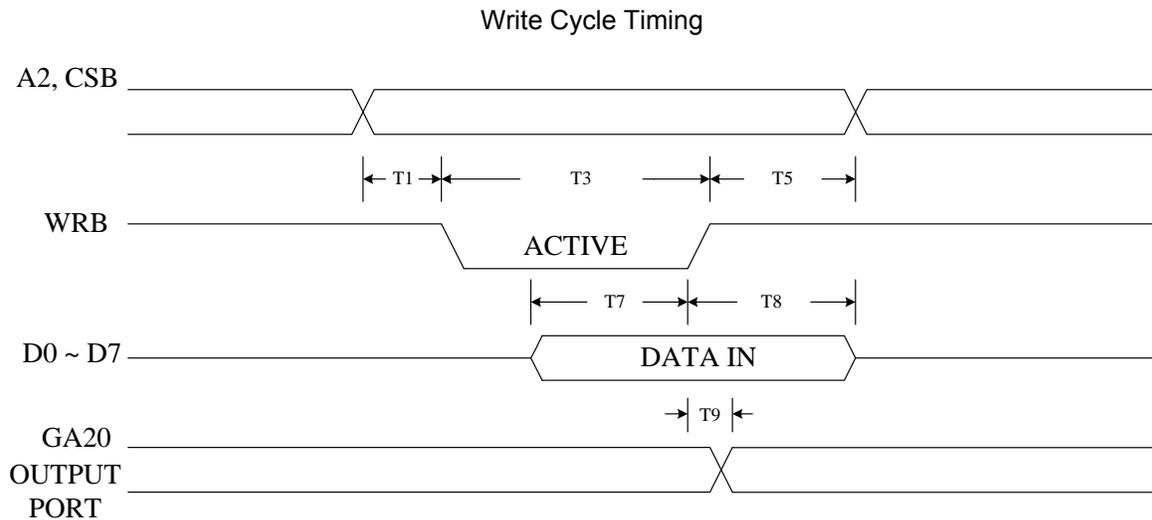


## 22.3.12 KBC Timing Parameters

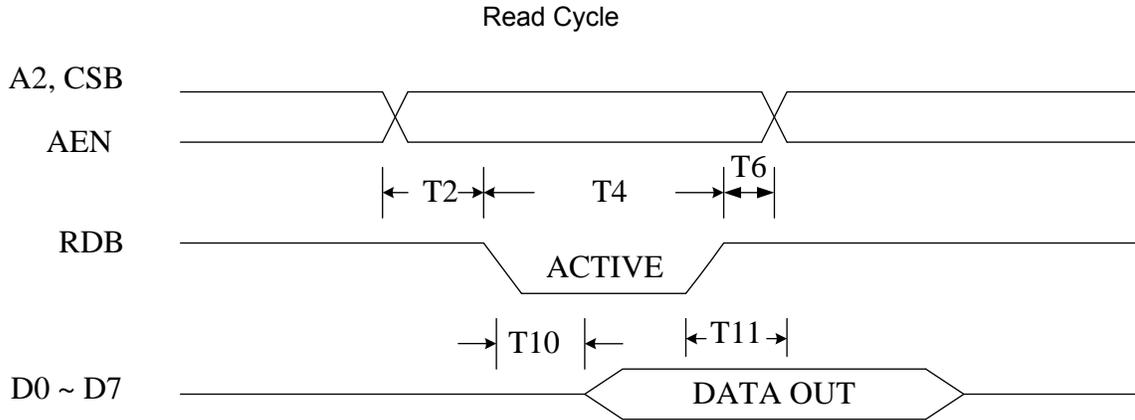
NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	$\mu$ S
T13	K/B Clock Period	20		$\mu$ S
T14	K/B Clock Pulse Width	10		$\mu$ S
T15	Data Valid Before Clock Falling (RECEIVE)	4		$\mu$ S
T16	K/B ACK After Finish Receiving	20		$\mu$ S
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		$\mu$ S

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T21	Input Clock Period (6–16 Mhz)	63	167	nS
T22	Duration of CLK inactive	30	50	$\mu$ S
T23	Duration of CLK active	30	50	$\mu$ S
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	$\mu$ S
T25	Time of inhibit mode	100	300	$\mu$ S
T26	Time from rising edge of CLK to DATA transition	5	T28-5	$\mu$ S
T27	Duration of CLK inactive	30	50	$\mu$ S
T28	Duration of CLK active	30	50	$\mu$ S
T29	Time from DATA transition to falling edge of CLK	5	25	$\mu$ S

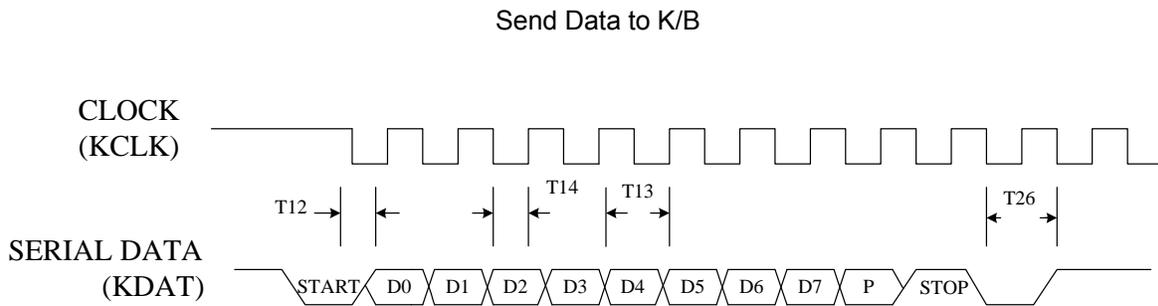
### 22.3.12.1. Writing Cycle Timing



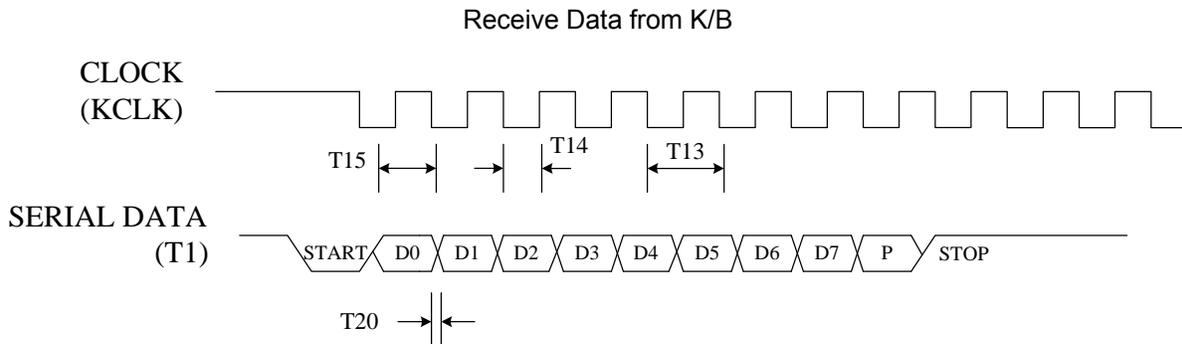
22.3.12.2. Read Cycle Timing



22.3.12.3. Send Data to K/B

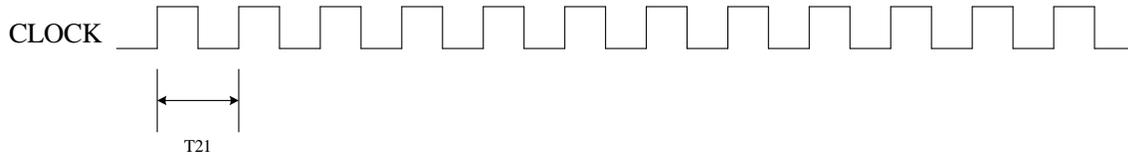


22.3.12.4. Receive Data from K/B



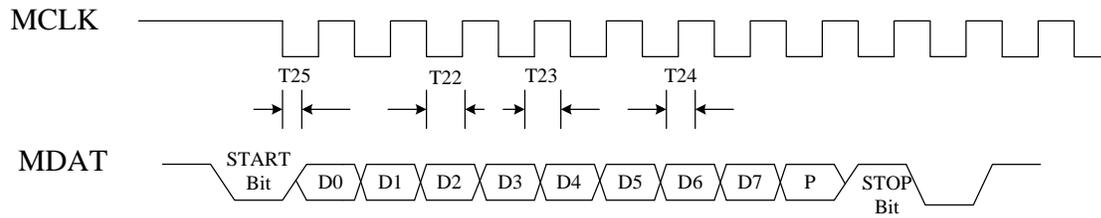
**22.3.12.5. Input Clock**

Input Clock



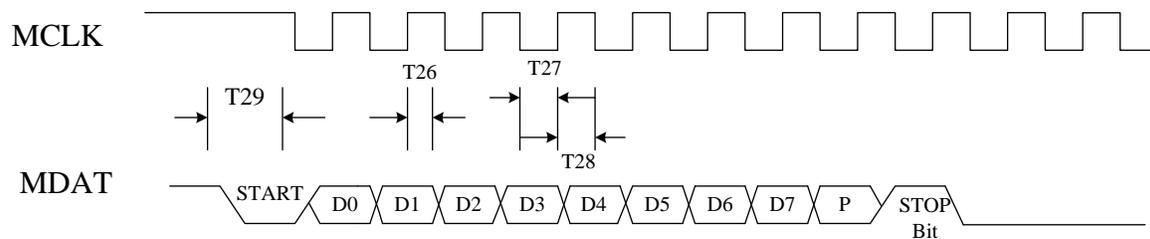
**22.3.12.6. Send Data to Mouse**

Send Data to Mouse



**22.3.12.7. Receive Data from Mouse**

Receive Data from Mouse



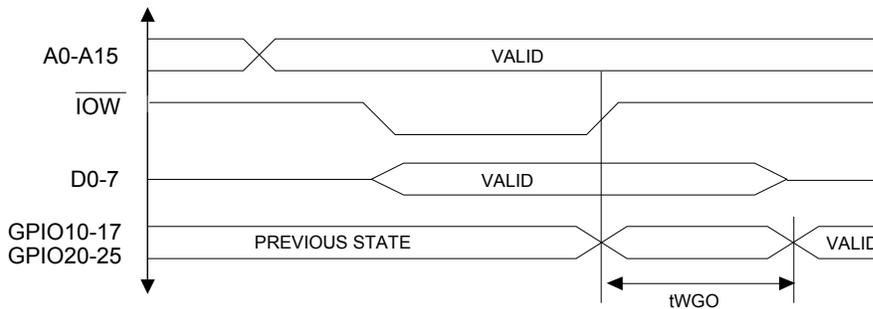
22.3.13 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{WGO}$	Write data to GPIO update		300(Note 1)	ns
$t_{SWP}$	SWITCH pulse width	16		msec

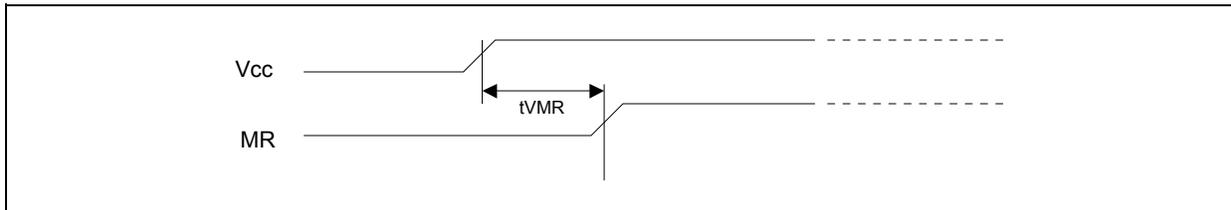
Note: Refer to Microprocessor Interface Timing for Read Timing.

22.3.13.1. GPIO Write Timing

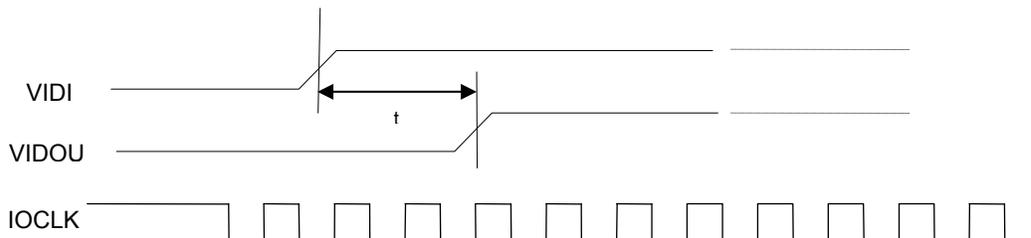
GPIO Write Timing diagram



22.4 LRESET Timing



22.5 VIDIN/out Delay time



SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t$	VIDIN/OUT Delay Time		1	us

23. TOP MARKING SPECIFICATIONS



1st line: Nuvoton logo

2nd line: part number: W83667HG-A (Green package)

3rd line: tracking code 806G9B28201234FA

**806**: packages made in '08, week 06

**G**: assembly house ID; G means GR, A means ASE, etc.

**9**: code version; 9 means code 009

**C**: IC revision; A means version A; B means version B, and C means version C

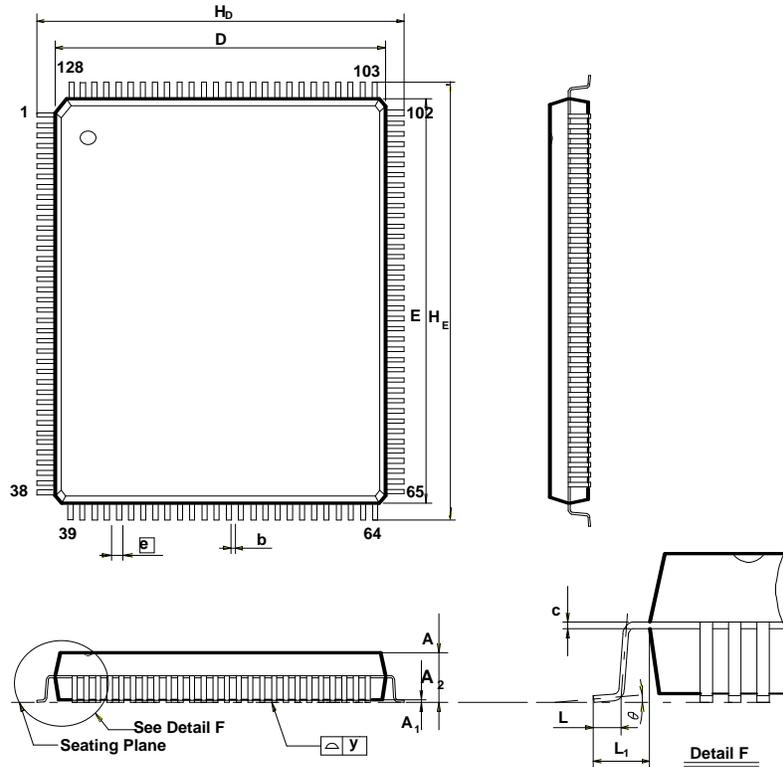
**28201234**: wafer production series lot number

**FA**: Nuvoton internal use.

**24. ORDERING INFORMATION**

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83667HG-A	128Pin QFP (Green package)	Commercial, 0°C to +70°C

25. PACKAGE SPECIFICATION



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	—	—	0.134	—	—	3.40
<b>A<sub>1</sub></b>	0.004	—	—	0.10	—	—
<b>A<sub>2</sub></b>	0.101	0.107	0.113	2.57	2.72	2.87
<b>b</b>	0.006	0.008	0.010	0.15	0.20	0.25
<b>c</b>	0.004	0.006	0.010	0.10	0.15	0.25
<b>D</b>	0.547	0.551	0.555	13.90	14.00	14.10
<b>E</b>	0.783	0.787	0.791	19.90	20.00	20.10
<b>e</b>	—	0.020	—	—	0.50	—
<b>H<sub>D</sub></b>	0.669	0.677	0.685	17.00	17.20	17.40
<b>H<sub>E</sub></b>	0.905	0.913	0.921	23.00	23.20	23.40
<b>L</b>	0.023	0.031	0.039	0.60	0.80	1.00
<b>L<sub>1</sub></b>	0.055	0.063	0.071	1.40	1.60	1.80
<b>y</b>	—	—	0.004	—	—	0.10
<b>θ</b>	0°	—	12°	0°	—	12°

128-pin (QFP, 14x20x2.75mm footprint 3.2mm)

## 26. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.1	06/20/2008	N.A.	Nuvoton internal use.
0.5	08/04/2008	N.A.	Preliminary Release.
0.6	08/15/2008	2, 43, 220, 223, 238, 239, 249, 251, 255, 256, 258, 260, 275, 267,	<ol style="list-style-type: none"> <li>1. Update Chapter 2 Features.</li> <li>2. Update Figure 8-7.</li> <li>3. Correct the default values of CR[30h], CR[61h], CR[63h], CR[70h], and CR[72h] of 21.6 Logical Device 5 (Keyboard Controller).</li> <li>4. Correct the default value of CR[30h] of 21.8 Logical Device 7 (GPIO6 ~ GPIO9).</li> <li>5. Correct the descriptions of CR[70h], CR[E2h], CR[E3h], and CR[E6h] of 21.11 Logical Device A (ACPI).</li> <li>6. Correct the default value of CR[F5h] of 21.12 Logical Device B (Hardware Monitor &amp; SB-TSI).</li> <li>7. Correct the default values of CR[FEh] and CR[FFh] and the description of bit 4-7 of CR[E8h] of 21.14 Logical Device C (PECI).</li> <li>8. Update the descriptions of CR[E6h] and CR[E8h] of 21.14 Logical Device D (VID).</li> <li>9. Update 22.3.1 AC Power on/off Timing.</li> <li>10. Update 22.2 DC Characteristics.</li> </ol>
0.61	09/16/2008	52-53, 63	<ol style="list-style-type: none"> <li>1. Update 8.7.3 SMART FANTM Control.</li> <li>2. Update Figure 8-21 Setting of SMART FAN™ IV.</li> </ol>
0.7	09/19/2008	121, 122, 125, 126, 129, 130, 205, 259, 260	<ol style="list-style-type: none"> <li>1. Update the descriptions of 9.126, 9.140, and 9.154.</li> <li>2. Correct the description of Chapter 20.</li> <li>3. Remove the descriptions of "BUSSEL".</li> </ol>
0.71	10/07/2008	7, 9, 17, 19, 24, 74	<ol style="list-style-type: none"> <li>1. Remove the CIR descriptions.</li> <li>2. Update the description of 9.4 SYSFANOUT Output Value Select Register – Index 01h (Bank 0).</li> </ol>
0.72	12/03/2008	NA	1. Remove SST descriptions.
0.74	03/24/2009	NA	Refine the datasheet
0.75	03/26/2009	NA	Refine the datasheet
1.0	03/27/2009	NA	Refine the datasheet
1.1	05/13/2009	NA	Refine the datasheet

VERSION	DATE	PAGE	DESCRIPTION
1.2	01/08/2010	31,32,45,50,52, 64,86,88,106,11 9,201,218,219,2 42,254,259	<ol style="list-style-type: none"> <li>1. Add 6.1 PSON# Block Diagram.</li> <li>2. Add PWROK Block Diagram.</li> <li>3. Add 8.3.3.4 Relative Register of Temperature Sensing.</li> <li>4. Add Table 8-8 Fan Speed Control related registers.</li> <li>5. Add Table 8-9 SMART FAN Mode selection and Table 8-10 Select temperature source for each fan control output.</li> <li>6. Update Table 8-16 SMART FAN™ IV Control Mode Relative Register.</li> <li>7. Update Bank0 Index40 Bit6~4 description.</li> <li>8. Update Bank0 Index41, 42, 45 "Interrupt Status Register" attribute to Read Clear.</li> <li>9. Add Bank0 Index 7D and 7E. (Temperature report registers.)</li> <li>10. Reserve Bank6 Index56~5Fh.</li> <li>11. Update Table 18-1 GPIO support wake-up function.</li> <li>12. Reserve Logic Device 2 (UARTA) CRF0h bit1~0=11(clock source is 14.769MHz).</li> <li>13. Reserve Logic Device 3 (UARTB) CRF0h bit1~0=11(clock source is 14.769MHz).</li> <li>14. Update Logic Device A CRE6h Bit0 description.</li> <li>15. Release Logic Device C CRE6h PECl reset register.</li> <li>16. Update Logic Device D CRE1h description (VID Offset Reg).</li> <li>17. Update Logic Device D CRE4h bit5 description.</li> </ol>

### Important Notice

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