1. Overview

The **Vortex86MX+** is a high performance and fully static 32-bit X86 processor with the compatibility of Windows based, Linux and most popular 32-bit RTOS. It also integrates 32KB write through 4-way L1 cache, 256KB write through/write back 4-way L2 cache, PCI rev. 2.1 32-bit bus interface at 33 MHz, DDR2, ROM controller, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), Fast Ethernet, FIFO UART, USB2.0 Host and IDE controller within a single 720-pin BGA package to form a system-on-a-chip **(SOC)**. It provides an ideal solution for the embedded system and communications products (such as thin client, NAT router, home gateway, access point and tablet PC) to bring about desired performance.

2. Features

- **X86 Processor Core**
  - 6-stage pipeline
- **Floating point unit support**
  - Extends CPU instruction set to include Trigonometric, Logarithmic and Exponential
  - Implements ANSI/IEEE standard 754-1985 for binary Floating-Point Architecture
- **Embedded I / D Separated L1 Cache**
  - 16K I-Cache, 16K D-Cache
- **Embedded L2 Cache**
  - 4-wary 256KB L2 Cache
  - Write through or write back policy
- **DDRII Control Interface**
  - 32 bits data bus
  - DDRII clock support up to 400MHz
  - DDRII size support up to 1Gbytes
- **IDE Controller**
  - Supports 2 channels Ultra-DMA 100 (Disk x 4)
  - Primary channel support SD card
- **LPC (Low Pin Count) Bus Interface**
- **GPU Control Unit**
  - VGA controller
  - 2D Graphics engine support
  - UMA architecture
- **MAC Controller x 1**
- **PCI Control Interface**
  - Up to 3 sets PCI master device
  - 3.3V I / O
- **HDA Controller**
- **DMA Controller**
- **Interrupt Controller**
- **Counter / Timers**
  - 2 sets of 8254 timer controller
  - Timer output is 5V tolerance I/O on 2nd Timer
- **Real Time Clock**
  - Less than 2uA (3.0V) power comsuption in Internal RTC Mode while chip is power-off.
- **FIFO UART Port x 3 (3 sets COM Port)**
  - Compatible with 16C550 / 16C552
  - Default internal pull-up
  - Supports the programmable baud rate generator with the data rate from 50 to 460.8K bps
  - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
  - Support TXD_En Signal on COM1
  - Port 80h output data could be sent to COM1 by software programming
- **Parallel Port x 1**
  - Supports SPP/EPP/ECP mode
- **General Programmable I/O**
  - Supports 40 programmable I / O pins
  - Each GPIO pin can be individually configured to be

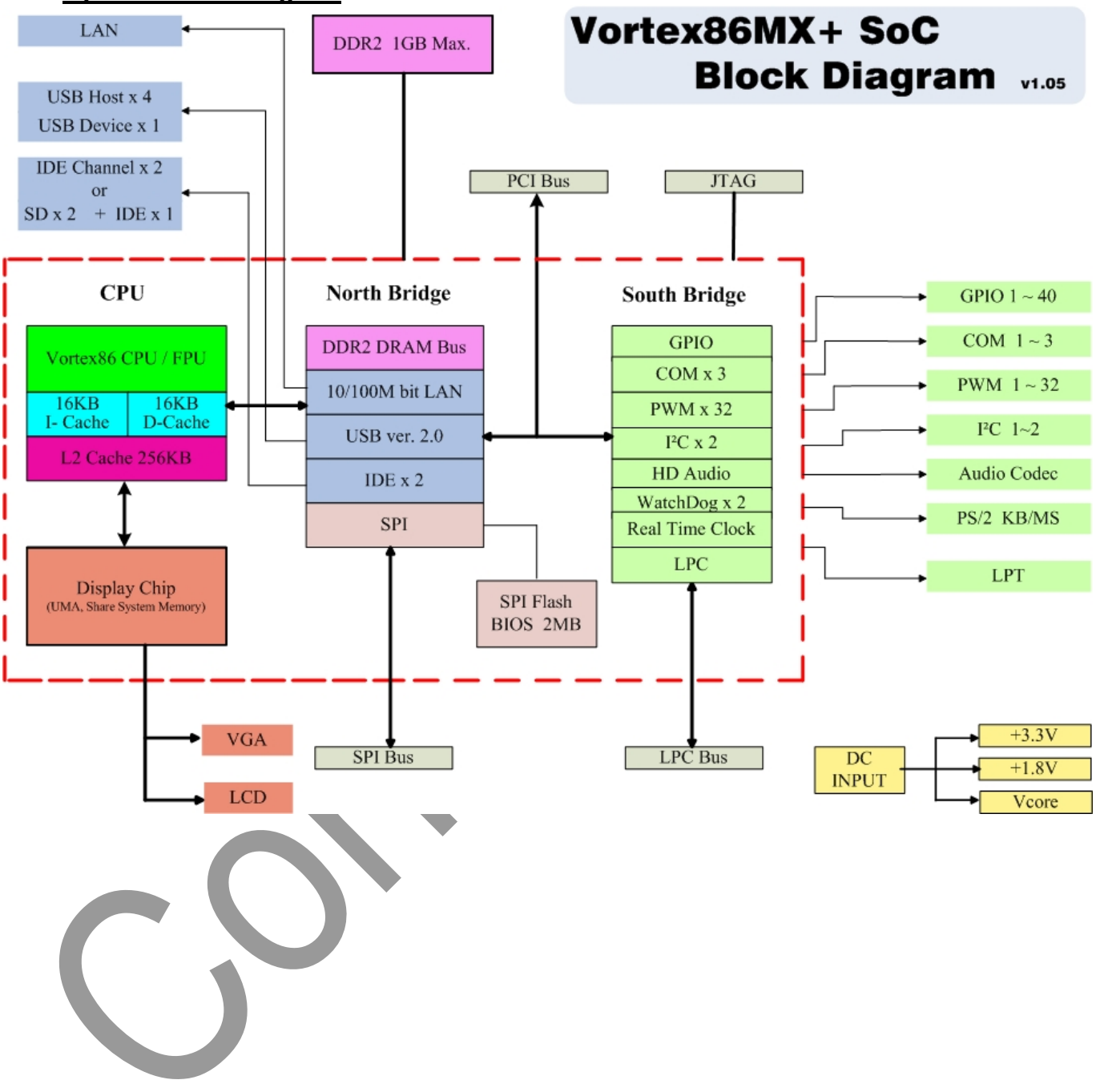
an input/output pin
  - GPIO_P0 and GPIO_P1 with interrupt support (input/output)

- **USB 2.0 Host Support**
  - Supports HS, FS and LS
  - 4 port
- **USB 1.1 Device Support**
  - 1 port
  - Supports FS with 3 programmable endpoint
- **PS / 2 Keyboard and Mouse Interface Support**
  - Compatible with 8042 controller
- **Speaker out**
- **Embedded 2MB Flash**
  - For BIOS storage
- **I^2C bus x 2**
  - Compliant w/t V2.1
  - Some master code (general call, START and CBUS) not support.
- **Servo Control interface support**
- **General Shift interface support**
- **JTAG Interface supported for S.W. debugging**
- **Input clock**
  - 14.318 MHz
  - 32.768 KHz
- **Output clock**
  - 24 MHz
  - 25 MHz
  - PCI clock
  - DDRII clock
- **Operating Voltage Range**
  - Core voltage: 1.0 V ~ 1.2V
  - I / O voltage: 1.8V ± 5% , 3.3 V ± 10 %
- **Operating temperature**
  - TBD
- **Package Type**
  - 31x31mm, 720 Ball BGA

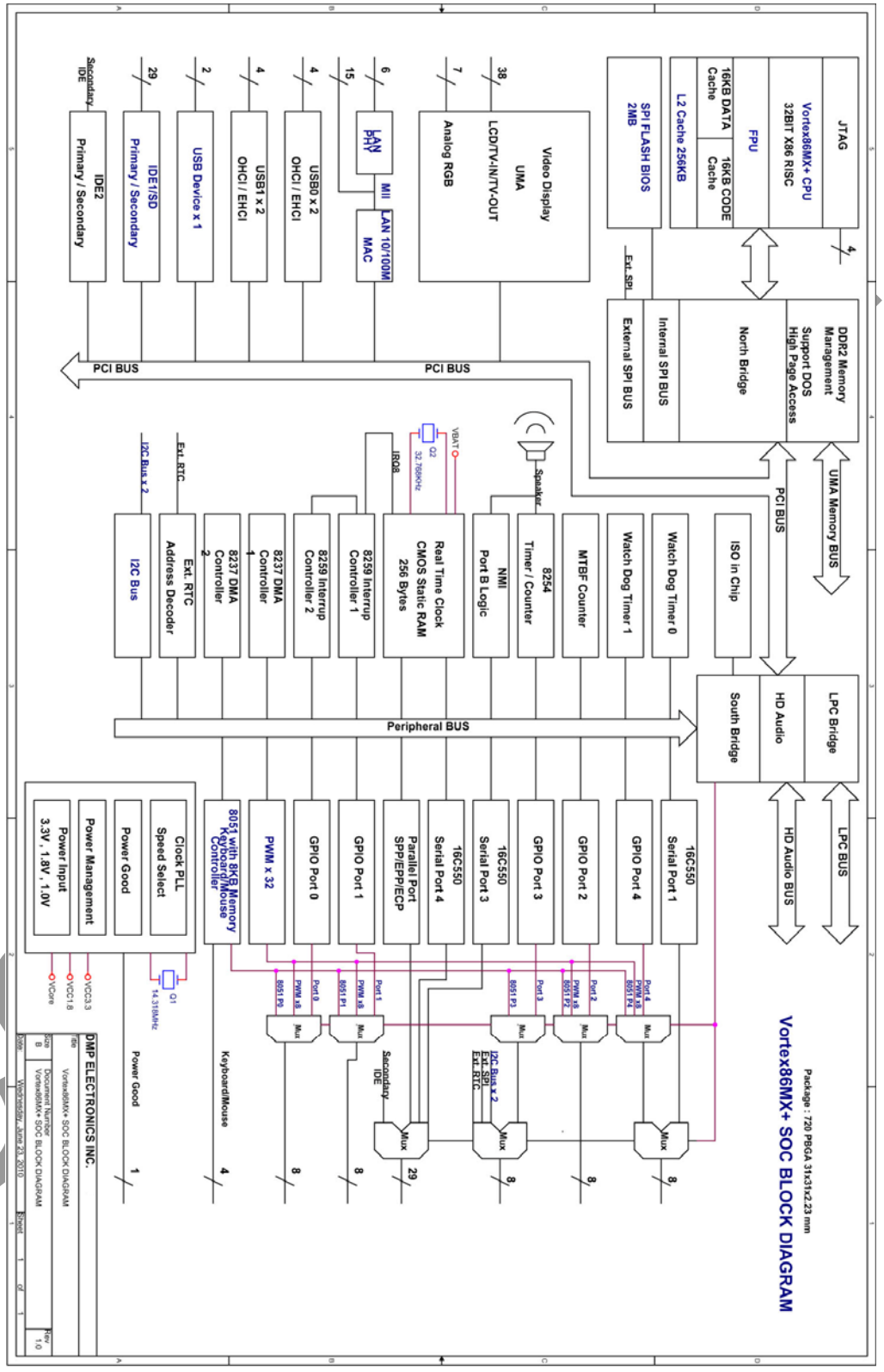
Note for Vortex86MX+ internal 8051 microcontroller:
There is one 8051 microcontroller inside of Vortex86MX+, this 8051 already used for Keyboard/Mouse simulation and Addressing line 20 for memory management. When those GPIO pins are set as 8051 mode, they can only be used as matrix keyboard controller and can not be used for other purpose. And when those GPIO pins are set as PWM or GPIO mode, they can be used as normal PWM or GPIO pin. Please also refer to “2.2 Function Block Diagram” on page 12 to see the modes of each GPIO Port.

3. Block Diagram

3.1. System Block Diagram



3.2. Functions Block Diagram



3.3. PCI Device List

ID SEL	AD 11	AD 12	AD 13	AD 14	AD 15	AD16	AD 17	AD 18	AD 19	AD 20	AD 21	AD22		AD 23	AD 24	AD 25	AD 26	
Device#	0	1	2	3	4	5	6	7	8	9		10	11	12	13	14	15	
Function0	NB	PCI Device						SB	MAC		USB OHCI	USB1 OHCI	IDE	VGA	HD AUDIO	USB Device		
Function1	NB1										USB EHCI	USB1 EHCI						

4. PIN Function List

4.1. BGA Ball Map

	A	B	C
1	A1_NC	G_IOR	G_IOG
2	VSS	AVSS_DACR18	AVSS_DACG18
3	VSS	AVDD_DACR18	AVDD_DACG18
4	VSS	VSS	VSS
5	VSS	VSS	VSS
6	VSS	VSS	VSS
7	G_XIN_14318	I_XIN_25M	VSS
8	SPI_CS#	VSS	E_SPI_DO/GPIO_P3[2]/8051_GPIO_P3[2]/GSF_CH2
9	SPI_DO	SPI_DI	E_SPI_CLK/GPIO_P3[1]/8051_GPIO_P3[1]/GSF_CH1
10	SPI_CK	VSS	LINK/ACTIVE
11	MDC	COL	CLK25MOUT
12	RXD[3]	RXC	VSS
13	AVDD_PLL33	VDD33	RXD[1]
14	XIN_14318	XOUT_14318	VSS
15	AVDD1_EPHYTX33	AVSS1_EPHYTX33	AVSS_PLL33
16	RXP	RXN	ATSTN
17	TXP	TXN	AVDD_EPHYRX33
18	AVDD_USB18	VSS	VSS
19	USB_DM	USB_DP	AVSS_USB18
20	USB1_DM	USB1_DP	AVSS1_USB18
21	AVDD1_USB18	AVDD2_USB18	VSS
22	USB2_DM	USB2_DP	AVSS2_USB18
23	USB3_DM	USB3_DP	AVSS3_USB18
24	AVDD3_USB18	VSS	VSS
25	VDD_BAT	VSS_BAT	VSS
26	RTC_XOUT	RTC_XIN	VSS
27	VSS	VSS	GPIO_P2[6]/8051_GPIO_P2[6]/SERVO[22]
28	GPIO_P3[5]/8051_GPIO_P3[5]/I2C_SDA	GPIO_P3[6]/8051_GPIO_P3[6]/I2C1_SCL	GPIO_P2[3]/8051_GPIO_P2[3]/SERVO[19]
29	VSS	VDD33	VSS
30	A30_NC	VSS	GPIO_P3[7]/8051_GPIO_P3[7]/I2C1_SDA

G	F	E	D
G_FPDI[10]/G_TVD[10]	G_FPDI[9]/G_TVD[8]	VSS	G_IOB
VDD33	G_DDC1_CLK	VSS	AVSS_DACB18
G_FPDI[9]/G_TVD[9]	G_TVCLKIN	VSS	AVDD_DACB18
G_ENBLT	VSS	G_DDC1_DAT	G_DDC_DAT
G_ENVDD	G_GPIO[2]	G_GPIO[3]	G_HSYNC
G_VSYNC	AVSS_DACBG18	VDD_DAC10	VSS
	G_REXT	VSS	VSS
	AVDD_DACBG18	E_SPI_CS#/GPIO_P3[0]/8051_GPIO_P3[0]/GSF_CH0	VDD33
	VDD33	VSS	E_SPI_DI/GPIO_P3[3]/8051_GPIO_P3[3]/GSF_CLK
	VSS	PADHOLDB	DUPLEX
	RXDV	VSS	PADWPB
	MDIO	RXD[0]	VDD33
	VSS	TXD[0]	TXC
	RXD[2]	TXD[1]	TXD[2]
	TXD[3]	VSS	TXEN
	AVDD_EPHYPLL33	AVSS_EPHYPLL33	ATSTP
	ISET	VSS	AVSS_EPHYRX33
	AVDD_EPHYBG33	AVSS_EPHYBG33	UD_DP
	VDE18	VSS	UD_DM
	AVDD_USB33	AVSS_USBPLL18	AVDD_USBPLL18
	VSS	REXT	VSS
	AVDD1_USB33	AVSS1_USBPLL18	AVDD1_USBPLL18
	VSS	REXT1	VSS
	VSS	VSS	VSS
GPIO_P1[5]/8051_GPIO_P1[5]/SERVO[13]	VDD33	VSS	RTC_PS
VSS	GPIO_P2[7]/8051_GPIO_P2[7]/SERVO[23]	GPIO_P3[4]/8051_GPIO_P3[4]/I2C_SCL	VDD33
GPIO_P1[7]/8051_GPIO_P1[7]/SERVO[15]	GPIO_P1[3]/8051_GPIO_P1[3]/SERVO[11]	GPIO_P2[4]/8051_GPIO_P2[4]/SERVO[20]	GPIO_P2[5]/8051_GPIO_P2[5]/SERVO[21]
GPIO_P0[7]/8051_GPIO_P0[7]/SERVO[7]	VSS	GPIO_P2[2]/8051_GPIO_P2[2]/SERVO[18]	GPIO_P2[1]/8051_GPIO_P2[1]/SERVO[17]
GPIO_P0[5]/8051_GPIO_P0[5]/SERVO[5]	VSS	GPIO_P1[6]/8051_GPIO_P1[6]/SERVO[14]	GPIO_P2[0]/8051_GPIO_P2[0]/SERVO[16]

L	K	J	H
G_FPD[1]/G_TVD[1]	VDD33	G_FPD[6]/G_TVD[6]	G_FPD[4]/G_TVD[4]
VSS	G_FPD[7]/G_TVD[7]	G_FPD[5]/G_TVD[5]	G_FPD[11]/G_TVD[11]
G_FPD[13]/G_CAPD[1]	G_FPD[0]/G_TVD[0]	G_FPD[19]/G_CAPD[7]	G_FPD[22]/G_CAPVS
G_FPD[15]/G_CAPD[3]	G_FPD[16]/G_CAPD[4]	VSS	G_FPD[23]/G_CAPCLK
VSS	G_FPD[17]/G_CAPD[5]	G_FPD[20]/G_CAPFILD	G_DDC_CLK
G_FPD[18]/G_CAPD[6]	G_FPD[21]/G_CAPHS	G_ENVEE	VDD33

VSS	VSS		
AVSS_VDISPLL18	AVDD_VDISPLL18		
AVSS_CPUPLL18	AVDD_CPUPLL18		
AVSS_DDRPLL18	AVDD_DDRPLL18		
VSS	VSS		
VSS	VSS		
VSS	VSS		
VSS	VDD33		
VDE18	VSS		
VSS	VDE18		
VDE18	VSS		
VSS	VDE18		

PE/IDE_SDD[9]	VSS	VDE18	GPIO_P1[1]/8051_GPIO_P1[1]/SERVO[9]
DTR3#/IDE_SDACK#	VDD33	SOUT3	GPIO_P1[4]/8051_GPIO_P1[4]/SERVO[12]
CTS4#/IDE_SIOW#	RI3#/IDE_SIORDY	DSR3#/IDE_SCBLID#	VSS
VDD33	CTS1#/GPIO_P4[7]/8051_GPIO_P4[7]/SERVO[31]	SIN3	GPIO_P0[3]/8051_GPIO_P0[3]/SERVO[3]
RI1#/GPIO_P4[3]/8051_GPIO_P4[3]/SERVO[27]	DTR1#/GPIO_P4[5]/8051_GPIO_P4[5]/SERVO[29]	VSS	GPIO_P0[2]/8051_GPIO_P0[2]/SERVO[2]
SIN4	SOUT4	GPIO_P0[0]/8051_GPIO_P0[0]/SERVO[0]	GPIO_P0[1]/8051_GPIO_P0[1]/SERVO[1]

R	P	N	M
VSS	MD[11]	VSS	G_FPD[3]/G_TVD[3]
MD[10]	MD[9]	VSS	G_FPD[2]/G_TVD[2]
MD[8]	VSS	G_FP1DET/G_TVDET	G_FP1CLK/G_TVCLKO
MD[3]	MD[2]	VSS	G_FPD[12]/G_CAPD[0]
MD[1]	VSS	G_FP1HS/G_TVHS	G_FPD[14]/G_CAPD[2]
VSS	VDD33	G_FP1DE/G_TVDE	G_FP1VS/G_TVVS

VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VDD33	VSS	VDD33	VSS
VSS	VDE18	VDE18	VSS
VDD33	VSS	VSS	VSS
VSS	VDE18	VDE18	VSS
VDD33	VDE18	VSS	VDE18

VSS	IDE_PINT	IDE_PA[0]	VDE18
IDE_PIORDY	PD[4]/IDE_SDD[4]	VSS	INIT#/IDE_SDD[13]
IDE_PA[1]	PD[2]/IDE_SDD[2]	PD[6]/IDE_SDD[6]	PD[3]/IDE_SDD[3]
CTS3#/IDE_SIOR#	VSS	PD[7]/IDE_SDD[7]	BUSY/IDE_SDD[10]
VSS	SIN1/GPIO_P4[4]/8051_GPIO_P4[4]/SERVO[28]	DSR1#/GPIO_P4[6]/8051_GPIO_P4[6]/SERVO[30]	VSS

AC	AB	AA	Y	W	V	U	T
VDD_DDR18	DRAMCLK	VSS	MD[15]	MD[14]	VSS	DQS#[1]	DQS[1]
MA[9]	DRAMCLK#	MA[7]	VSS	MD[12]	MD[13]	VDD_DDR18	DQM[1]
MA[2]	VSS	MA[4]	MA[11]	VDD_DDR18	MD[5]	MD[4]	VSS
VSS	MA[6]	MA[8]	MA[13]	MD[6]	VSS	DQS[0]	DQS#[0]
VDD_DDR18	MA[14]	MA[12]	VDD_DDR18	MD[7]	DQM[0]	MD[0]	VDD_DDR18
VDD10	VSS	VDD10	VDD10	VSS	VREF	VDD_DDR18	OCDBIAS

VDD10	VSS	VDD10	VDD10	VDD_DDR18	VDD33		
VDD10	VSS	VSS	VDD10	VSS	VSS		
VDD10	VSS	VSS	VDD10	VSS	VSS		
VDD10	VDD10	VDD10	VDD10	VSS	VDD33		
VDD_DDR18	VSS	VSS	VSS	VSS	VSS		
VDD33	VSS	VDD33	VSS	VDD33	VDD33		
VSS	VSS	VSS	VSS	VSS	VSS		
VSS	VSS	VSS	VSS	VSS	VSS		
VSS	VSS	VSS	VSS	VSS	VSS		
VSS	VSS	VSS	VSS	VSS	VSS		
VSS	VSS	VSS	VSS	VSS	VSS		
VSS	VSS	VSS	VSS	VSS	VSS		

INTD#	PWRGOOD	VSS	H_SDI	H_SDO	VDD33	IDE_PDD[6]/SD_CD	IDE_PDD[7]/SD_WP
INTB#	INTC#	INTA#	VSS	H_RST#	IDE_PDD[5]/SD_DATA[1]	IDE_PDD[11]/SD1_CLK	VDD33
IDE_PDD[3]/SD_CLK	IDE_PDD[10]/SD1_CMD	IDE_PDACK#	IDE_PCBLID#	H_SYNC	H_BCLK	IDE_PDD[13]/SD1_DATA[1]	IDE_PIOW#/SD_RW
VDD33	IDE_PCS1#	SLCT/IDE_SDD[8]	VSS	AFD#/IDE_SDD[15]	RTS3#/IDE_SRST#	VDD33	DCD3#/IDE_SDRQ
SLIN#/IDE_SDD[12]	VSS	ERR#/IDE_SDD[14]	RI4#/IDE_SA[1]	DTR4#/IDE_SA[0]	VSS	MSCLK	SPEAKER
VSS	CLK24MOUT	RTS4#/IDE_SINT	VSS	DCD4#/IDE_SA[2]	DSR4#/IDE_SCS1#	STB#/IDE_SCS0#	MSDAT

AK	AJ	AH	AG	AF	AE	AD
AK1_NC	ODT[0]	CKE	VDD_DDR18	BA[2]	MA[1]	MA[3]
DRAMCLK1#	VSS	WE#	BA[0]	ODT[1]	VSS	CAS#
VSS	DRAMCLK1	CS0#	VDD_DDR18	BA[1]	MA[10]	MA[5]
MD[27]	VSS	MD[25]	MD[17]	VSS	RAS#	MA[0]
VSS	MD[26]	MD[18]	VSS	MD[16]	VSS	CS1#
DQM[3]	VDD_DDR18	MD[24]	MD[19]	VDD_DDR18	VDD10	VSS
DQS[3]	VSS	VSS	DQS[2]	DQM[2]	VSS	
DQS#[3]	VSS	VREF1	DQS#[2]	VDD_DDR18	VDD10	
VSS	MD[28]	MD[23]	VSS	MD[20]	VSS	
MD[29]	VDD_DDR18	MD[31]	MD[22]	VDD_DDR18	VDD10	
VSS	MD[30]	VSS	OCDBIAS1	MD[21]	VSS	
VSS	VSS	VSS	VSS	VSS	VDD10	
GNT#[0]	PCICLK[2]	PCICLK[1]	VSS	VDD33	VDD10	
VDD33	VSS	TDO	TDI	PCICLK[0]	VSS	
GNT#[2]	GNT#[1]	VDD33	TCK	REQ#[1]	REQ#[0]	
AD[0]	VSS	VSS	TMS	VSS	REQ#[2]	
VDD33	AD[1]	CBE#[1]	AD[30]	AD[26]	AD[31]	
AD[2]	PAR	STOP#	AD[27]	VSS	AD[28]	
AD[3]	VSS	DEVSEL#	CBE#[3]	AD[29]	VDD33	
AD[4]	TRDY#	VSS	AD[23]	AD[25]	PCIRST#	
AD[5]	AD[21]	AD[24]	AD[19]	VSS	AD[22]	
AD[6]	VSS	AD[16]	AD[18]	AD[20]	VDD33	
AD[7]	FRAME#	VDD33	CBE#[2]	AD[17]	LDRQ#	
AD[8]	AD[15]	AD[14]	IRDY#	VSS	KBDAT/A20GATE#	
CBE#[0]	VSS	AD[13]	AD[12]	LAD[1]	VSS	VDD33
AD[10]	AD[11]	VDD33	VSS	SERIRQ	KBCLK/KBRST#	VSS
LAD[0]	AD[9]	LAD[2]	LAD[3]	IDE_PDD[8]/SD1_DATA[2]	LFRAME#	IDE_PDD[0]/SD_DATA[2]
IDE_PDD[1]/SD_DATA[3]	VDD33	IDE_PDD[9]/SD1_DATA[3]	IDE_PDD[12]/SD1_DATA[0]	VSS	IDE_PDD[2]/SD_CMD	IDE_PDD[4]/SD_DATA[0]
IDE_PDD[15]/SD1_WP	IDE_PDD[14]/SD1_CD	VSS	IDE_PIOR#/SD1_RW	IDE_PCS0#	VSS	PD[5]/IDE_SDD[5]

4.2. PIN Out Table

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
A1	A1_NC	G1	G_FPD[10]/G_TVD[10]	T1	DQS[1]	AE1	MA[1]
A2	VSS	G2	VDD33	T2	DQM[1]	AE2	VSS
A3	VSS	G3	G_FPD[9]/G_TVD[9]	T3	VSS	AE3	MA[10]
A4	VSS	G4	G_ENBLT	T4	DQS#[0]	AE4	RAS#
A5	VSS	G5	G_ENVDD	T5	VDD_DDR18	AE5	VSS
A6	VSS	G6	G_VSYNC	T6	OCDBIAS	AE6	VDD10
A7	G_XIN_14318	G25	GPIO_P1[5]/8051_GPIO_P1[5]/SERVO[13]	T10	VDD33	AE7	VSS
A8	SPI_CS#	G26	VSS	T11	VSS	AE8	VDD10
A9	SPI_DO	G27	GPIO_P1[7]/8051_GPIO_P1[7]/SERVO[15]	T12	VSS	AE9	VSS
A10	SPI_CK	G28	GPIO_P0[7]/8051_GPIO_P0[7]/SERVO[7]	T13	VDD33	AE10	VDD10
A11	MDC	G29	GPIO_P0[5]/8051_GPIO_P0[5]/SERVO[5]	T14	VSS	AE11	VSS
A12	RXD[3]	G30	GPIO_P0[4]/8051_GPIO_P0[4]/SERVO[4]	T15	VDD33	AE12	VDD10
A13	AVDD_PLL33	H1	G_FPD[4]/G_TVD[4]	T16	VSS	AE13	VDD10
A14	XIN_14318	H2	G_FPD[11]/G_TVD[11]	T17	VSS	AE14	VSS
A15	AVDD1_EPHYTX33	H3	G_FPD[22]/G_CAPVS	T18	VSS	AE15	REQ#[0]
A16	RXP	H4	G_FPD[23]/G_CAPCLK	T19	VSS	AE16	REQ#[2]
A17	TXP	H5	G_DDC_CLK	T20	VSS	AE17	AD[31]
A18	AVDD_USB18	H6	VDD33	T21	VSS	AE18	AD[28]
A19	USB_DM	H25	GPIO_P1[1]/8051_GPIO_P1[1]/SERVO[9]	T25	IDE_PDD[7]/SD_WP	AE19	VDD33
A20	USB1_DM	H26	GPIO_P1[4]/8051_GPIO_P1[4]/SERVO[12]	T26	VDD33	AE20	PCIRST#
A21	AVDD1_USB18	H27	VSS	T27	IDE_PIOW#/SD_RW	AE21	AD[22]
A22	USB2_DM	H28	GPIO_P0[3]/8051_GPIO_P0[3]/SERVO[3]	T28	DCD3#/IDE_SDRQ	AE22	VDD33
A23	USB3_DM	H29	GPIO_P0[2]/8051_GPIO_P0[2]/SERVO[2]	T29	SPEAKER	AE23	LDRQ#
A24	AVDD3_USB18	H30	GPIO_P0[1]/8051_GPIO_P0[1]/SERVO[1]	T30	MSDAT	AE24	KBDAT/A20GATE#
A25	VDD_BAT	J1	G_FPD[6]/G_TVD[6]	U1	DQS#[1]	AE25	VSS
A26	RTC_XOUT	J2	G_FPD[5]/G_TVD[5]	U2	VDD_DDR18	AE26	KBCLK/KBRST#
A27	VSS	J3	G_FPD[19]/G_CAPD[7]	U3	MD[4]	AE27	LFRAME#
A28	GPIO_P3[5]/8051_GPIO_P3[5]/I2C_SDA	J4	VSS	U4	DQS[0]	AE28	IDE_PDD[2]/SD_CMD
A29	VSS	J5	G_FPD[20]/G_CAPFILD	U5	MD[0]	AE29	VSS
A30	A30_NC	J6	G_ENVEE	U6	VDD_DDR18	AE30	PD[1]/IDE_SDD[1]
B1	G_IOR	J25	VDE18	U10	VDD_DDR18	AF1	BA[2]
B2	AVSS_DACR18	J26	SOUT3	U11	VSS	AF2	ODT[1]

B3	AVDD_DACR18	J27	DSR3#/IDE_SCBLID#	U12	VSS	AF3	BA[1]
B4	VSS	J28	SIN3	U13	VSS	AF4	VSS
B5	VSS	J29	VSS	U14	VSS	AF5	MD[16]
B6	VSS	J30	GPIO_P0[0]/8051_GPIO_P0[0]/SERVO[0]	U15	VDD33	AF6	VDD_DDR18
B7	I_XIN_25M	K1	VDD33	U16	VSS	AF7	DQM[2]
B8	VSS	K2	G_FPD[7]/G_TVD[7]	U17	VSS	AF8	VDD_DDR18
B9	SPI_DI	K3	G_FPD[0]/G_TVD[0]	U18	VSS	AF9	MD[20]
B10	VSS	K4	G_FPD[16]/G_CAPD[4]	U19	VSS	AF10	VDD_DDR18
B11	COL	K5	G_FPD[17]/G_CAPD[5]	U20	VSS	AF11	MD[21]
B12	RXC	K6	G_FPD[21]/G_CAPHS	U21	VSS	AF12	VSS
B13	VDD33	K10	VSS	U25	IDE_PDD[6]/SD_CD	AF13	VDD33
B14	XOUT_14318	K11	AVDD_VDISPLL18	U26	IDE_PDD[11]/SD1_CLK	AF14	PCICLK[0]
B15	AVSS1_EPHYTX33	K12	AVDD_CPUPLL18	U27	IDE_PDD[13]/SD1_DATA[1]	AF15	REQ#[1]
B16	RXN	K13	AVDD_DDRPLL18	U28	VDD33	AF16	VSS
B17	TXN	K14	VSS	U29	MSCLK	AF17	AD[26]
B18	VSS	K15	VSS	U30	STB#/IDE_SCS0#	AF18	VSS
B19	USB_DP	K16	VSS	V1	VSS	AF19	AD[29]
B20	USB1_DP	K17	VDD33	V2	MD[13]	AF20	AD[25]
B21	AVDD2_USB18	K18	VSS	V3	MD[5]	AF21	VSS
B22	USB2_DP	K19	VDE18	V4	VSS	AF22	AD[20]
B23	USB3_DP	K20	VSS	V5	DQM[0]	AF23	AD[17]
B24	VSS	K21	VDE18	V6	VREF	AF24	VSS
B25	VSS_BAT	K25	VSS	V10	VDD10	AF25	LAD[1]
B26	RTC_XIN	K26	VDD33	V11	VDD10	AF26	SERIRQ
B27	VSS	K27	RI3#/IDE_SIORDY	V12	VDD10	AF27	IDE_PDD[8]/SD1_DATA[2]
B28	GPIO_P3[6]/8051_GPIO_P3[6]/I2C1_SCL	K28	CTS1#/GPIO_P4[7]/8051_GPIO_P4[7]/SERVO[31]	V13	VDD10	AF28	VSS
B29	VDD33	K29	DTR1#/GPIO_P4[5]/8051_GPIO_P4[5]/SERVO[29]	V14	VSS	AF29	IDE_PCS0#
B30	VSS	K30	SOUT4	V15	VSS	AF30	PD[0]/IDE_SDD[0]
C1	G_IOG	L1	G_FPD[1]/G_TVD[1]	V16	VSS	AG1	VDD_DDR18
C2	AVSS_DACG18	L2	VSS	V17	VSS	AG2	BA[0]
C3	AVDD_DACG18	L3	G_FPD[13]/G_CAPD[1]	V18	VSS	AG3	VDD_DDR18
C4	VSS	L4	G_FPD[15]/G_CAPD[3]	V19	VSS	AG4	MD[17]
C5	VSS	L5	VSS	V20	VSS	AG5	VSS
C6	VSS	L6	G_FPD[18]/G_CAPD[6]	V21	VSS	AG6	MD[19]
C7	VSS	L10	VSS	V25	VDD33	AG7	DQS[2]

C8	E_SPI_DO/GPIO_P3[2]/8051_GPIO_P3[2]/GSF_CH2	L11	AVSS_VDISPLL18	V26	IDE_PDD[5]/SD_DATA[1]	AG8	DQS#[2]
C9	E_SPI_CLK/GPIO_P3[1]/8051_GPIO_P3[1]/GSF_CH1	L12	AVSS_CPUPLL18	V27	H_BCLK	AG9	VSS
C10	LINK/ACTIVE	L13	AVSS_DDRPLL18	V28	RTS3#/IDE_SRST#	AG10	MD[22]
C11	CLK25MOUT	L14	VSS	V29	VSS	AG11	OCDBIAS1
C12	VSS	L15	VSS	V30	DSR4#/IDE_SCS1#	AG12	VSS
C13	RXD[1]	L16	VSS	W1	MD[14]	AG13	VSS
C14	VSS	L17	VSS	W2	MD[12]	AG14	TDI
C15	AVSS_PLL33	L18	VDE18	W3	VDD_DDR18	AG15	TCK
C16	ATSTN	L19	VSS	W4	MD[6]	AG16	TMS
C17	AVDD_EPHYRX33	L20	VDE18	W5	MD[7]	AG17	AD[30]
C18	VSS	L21	VSS	W6	VSS	AG18	AD[27]
C19	AVSS_USB18	L25	PE/IDE_SDD[9]	W10	VDD10	AG19	CBE#[3]
C20	AVSS1_USB18	L26	DTR3#/IDE_SDACK#	W11	VSS	AG20	AD[23]
C21	VSS	L27	CTS4#/IDE_SIOW#	W12	VSS	AG21	AD[19]
C22	AVSS2_USB18	L28	VDD33	W13	VDD10	AG22	AD[18]
C23	AVSS3_USB18	L29	RI1#/GPIO_P4[3]/8051_GPIO_P4[3]/SERVO[27]	W14	VSS	AG23	CBE#[2]
C24	VSS	L30	SIN4	W15	VDD33	AG24	IRDY#
C25	VSS	M1	G_FPD[3]/G_TVD[3]	W16	VSS	AG25	AD[12]
C26	VSS	M2	G_FPD[2]/G_TVD[2]	W17	VSS	AG26	VSS
C27	GPIO_P2[6]/8051_GPIO_P2[6]/SERVO[22]	M3	G_FP1CLK/G_TVCLKO	W18	VSS	AG27	LAD[3]
C28	GPIO_P2[3]/8051_GPIO_P2[3]/SERVO[19]	M4	G_FPD[12]/G_CAPD[0]	W19	VSS	AG28	IDE_PDD[12]/SD1_DATA[0]
C29	VSS	M5	G_FPD[14]/G_CAPD[2]	W20	VSS	AG29	IDE_PIOR#/SD1_RW
C30	GPIO_P3[7]/8051_GPIO_P3[7]/I2C1_SDA	M6	G_FP1VS/G_TVVS	W21	VSS	AG30	IDE_PA[2]
D1	G_IOB	M10	VSS	W25	H_SDO	AH1	CKE
D2	AVSS_DACB18	M11	VSS	W26	H_RST#	AH2	WE#
D3	AVDD_DACB18	M12	VSS	W27	H_SYNC	AH3	CS0#
D4	G_DDC_DAT	M13	VSS	W28	AFD#/IDE_SDD[15]	AH4	MD[25]
D5	G_HSYNC	M14	VSS	W29	DTR4#/IDE_SA[0]	AH5	MD[18]
D6	VSS	M15	VSS	W30	DCD4#/IDE_SA[2]	AH6	MD[24]
D7	VSS	M16	VSS	Y1	MD[15]	AH7	VSS
D8	VDD33	M17	VSS	Y2	VSS	AH8	VREF1
D9	E_SPI_DI/GPIO_P3[3]/8051_GPIO_P3[3]/GSF_CLK	M18	VSS	Y3	MA[11]	AH9	MD[23]
D10	DUPLEX	M19	VSS	Y4	MA[13]	AH10	MD[31]
D11	PADWPB	M20	VSS	Y5	VDD_DDR18	AH11	VSS
D12	VDD33	M21	VDE18	Y6	VDD10	AH12	VSS

D13	TXC	M25	VDE18	Y10	VSS	AH13	PCICLK[1]
D14	TXD[2]	M26	INIT#/IDE_SDD[13]	Y11	VSS	AH14	TDO
D15	TXEN	M27	PD[3]/IDE_SDD[3]	Y12	VSS	AH15	VDD33
D16	ATSTP	M28	BUSY/IDE_SDD[10]	Y13	VDD10	AH16	VSS
D17	AVSS_EPHYRX33	M29	VSS	Y14	VSS	AH17	CBE#[1]
D18	UD_DP	M30	TXD_EN1	Y15	VSS	AH18	STOP#
D19	UD_DM	N1	VSS	Y16	VSS	AH19	DEVSEL#
D20	AVDD_USBPLL18	N2	VSS	Y17	VSS	AH20	VSS
D21	VSS	N3	G_FP1DET/G_TVDET	Y18	VSS	AH21	AD[24]
D22	AVDD1_USBPLL18	N4	VSS	Y19	VSS	AH22	AD[16]
D23	VSS	N5	G_FP1HS/G_TVHS	Y20	VSS	AH23	VDD33
D24	VSS	N6	G_FP1DE/G_TVDE	Y21	VSS	AH24	AD[14]
D25	RTC_PS	N10	VSS	Y25	H_SDI	AH25	AD[13]
D26	VDD33	N11	VSS	Y26	VSS	AH26	VDD33
D27	GPIO_P2[5]/8051_GPIO_P2[5]/SERVO[21]	N12	VSS	Y27	IDE_PCBLID#	AH27	LAD[2]
D28	GPIO_P2[1]/8051_GPIO_P2[1]/SERVO[17]	N13	VSS	Y28	VSS	AH28	IDE_PDD[9]/SD1_DATA[3]
D29	GPIO_P2[0]/8051_GPIO_P2[0]/SERVO[16]	N14	VSS	Y29	RI4#/IDE_SA[1]	AH29	VSS
D30	GPIO_P1[2]/8051_GPIO_P1[2]/SERVO[10]	N15	VSS	Y30	VSS	AH30	IDE_PDRQ
E1	VSS	N16	VSS	AA1	VSS	AJ1	ODT[0]
E2	VSS	N17	VDD33	AA2	MA[7]	AJ2	VSS
E3	VSS	N18	VDE18	AA3	MA[4]	AJ3	DRAMCLK1
E4	G_DDC1_DAT	N19	VSS	AA4	MA[8]	AJ4	VSS
E5	G_GPIO[3]	N20	VDE18	AA5	MA[12]	AJ5	MD[26]
E6	VDD_DAC10	N21	VSS	AA6	VDD10	AJ6	VDD_DDR18
E7	VSS	N25	IDE_PA[0]	AA10	VDD10	AJ7	VSS
E8	E_SPI_CS#/GPIO_P3[0]/8051_GPIO_P3[0]/GSF_CH0	N26	VSS	AA11	VDD10	AJ8	VSS
E9	VSS	N27	PD[6]/IDE_SDD[6]	AA12	VDD10	AJ9	MD[28]
E10	PADHOLDB	N28	PD[7]/IDE_SDD[7]	AA13	VDD10	AJ10	VDD_DDR18
E11	VSS	N29	DSR1#/GPIO_P4[6]/8051_GPIO_P4[6]/SERVO[30]	AA14	VDD_DDR18	AJ11	MD[30]
E12	RXD[0]	N30	DCD1#/GPIO_P4[0]/8051_GPIO_P4[0]/SERVO[24]	AA15	VDD33	AJ12	VSS
E13	TXD[0]	P1	MD[11]	AA16	VSS	AJ13	PCICLK[2]
E14	TXD[1]	P2	MD[9]	AA17	VSS	AJ14	VSS
E15	VSS	P3	VSS	AA18	VSS	AJ15	GNT#[1]
E16	AVSS_EPHYPLL33	P4	MD[2]	AA19	VSS	AJ16	VSS
E17	VSS	P5	VSS	AA20	VSS	AJ17	AD[1]

E18	AVSS_EPHYBG33	P6	VDD33	AA21	VSS	AJ18	PAR
E19	VSS	P10	VSS	AA25	VSS	AJ19	VSS
E20	AVSS_USBPLL18	P11	VSS	AA26	INTA#	AJ20	TRDY#
E21	REXT	P12	VSS	AA27	IDE_PDACK#	AJ21	AD[21]
E22	AVSS1_USBPLL18	P13	VSS	AA28	SLCT/IDE_SDD[8]	AJ22	VSS
E23	REXT1	P14	VSS	AA29	ERR#/IDE_SDD[14]	AJ23	FRAME#
E24	VSS	P15	VSS	AA30	RTS4#/IDE_SINT	AJ24	AD[15]
E25	VSS	P16	VSS	AB1	DRAMCLK	AJ25	VSS
E26	GPIO_P3[4]/8051_GPIO_P3[4]/I2C_SCL	P17	VSS	AB2	DRAMCLK#	AJ26	AD[11]
E27	GPIO_P2[4]/8051_GPIO_P2[4]/SERVO[20]	P18	VDE18	AB3	VSS	AJ27	AD[9]
E28	GPIO_P2[2]/8051_GPIO_P2[2]/SERVO[18]	P19	VSS	AB4	MA[6]	AJ28	VDD33
E29	GPIO_P1[6]/8051_GPIO_P1[6]/SERVO[14]	P20	VDE18	AB5	MA[14]	AJ29	IDE_PDD[14]/SD1_CD
E30	GPIO_P1[0]/8051_GPIO_P1[0]/SERVO[8]	P21	VDE18	AB6	VSS	AJ30	IDE_PRST#
F1	G_FPD[8]/G_TVD[8]	P25	IDE_PINT	AB25	PWRGOOD	AK1	AK1_NC
F2	G_DDC1_CLK	P26	PD[4]/IDE_SDD[4]	AB26	INTC#	AK2	DRAMCLK1#
F3	G_TVCLKIN	P27	PD[2]/IDE_SDD[2]	AB27	IDE_PDD[10]/SD1_CMD	AK3	VSS
F4	VSS	P28	VSS	AB28	IDE_PCS1#	AK4	MD[27]
F5	G_GPIO[2]	P29	SIN1/GPIO_P4[4]/8051_GPIO_P4[4]/SERVO[28]	AB29	VSS	AK5	VSS
F6	AVSS_DACBG18	P30	RTS1#/GPIO_P4[2]/8051_GPIO_P4[2]/SERVO[26]	AB30	CLK24MOUT	AK6	DQM[3]
F7	G_REXT	R1	VSS	AC1	VDD_DDR18	AK7	DQS[3]
F8	AVDD_DACBG18	R2	MD[10]	AC2	MA[9]	AK8	DQS#[3]
F9	VDD33	R3	MD[8]	AC3	MA[2]	AK9	VSS
F10	VSS	R4	MD[3]	AC4	VSS	AK10	MD[29]
F11	RXDV	R5	MD[1]	AC5	VDD_DDR18	AK11	VSS
F12	MDIO	R6	VSS	AC6	VDD10	AK12	VSS
F13	VSS	R10	VSS	AC25	INTD#	AK13	GNT#[0]
F14	RXD[2]	R11	VSS	AC26	INTB#	AK14	VDD33
F15	TXD[3]	R12	VSS	AC27	IDE_PDD[3]/SD_CLK	AK15	GNT#[2]
F16	AVDD_EPHYPLL33	R13	VSS	AC28	VDD33	AK16	AD[0]
F17	ISET	R14	VSS	AC29	SLIN#/IDE_SDD[12]	AK17	VDD33
F18	AVDD_EPHYBG33	R15	VSS	AC30	VSS	AK18	AD[2]
F19	VDE18	R16	VSS	AD1	MA[3]	AK19	AD[3]
F20	AVDD_USB33	R17	VDD33	AD2	CAS#	AK20	AD[4]
F21	VSS	R18	VSS	AD3	MA[5]	AK21	AD[5]
F22	AVDD1_USB33	R19	VDD33	AD4	MA[0]	AK22	AD[6]
F23	VSS	R20	VSS	AD5	CS1#	AK23	AD[7]

F24	VSS	R21	VDD33	AD6	VSS	AK24	AD[8]
F25	VDD33	R25	VSS	AD25	VDD33	AK25	CBE#[0]
F26	GPIO_P2[7]/8051_GPIO_P2[7]/SERVO[23]	R26	IDE_PIORDY	AD26	VSS	AK26	AD[10]
F27	GPIO_P1[3]/8051_GPIO_P1[3]/SERVO[11]	R27	IDE_PA[1]	AD27	IDE_PDD[0]/SD_DATA[2]	AK27	LAD[0]
F28	VSS	R28	CTS3#/IDE_SIOR#	AD28	IDE_PDD[4]/SD_DATA[0]	AK28	IDE_PDD[1]/SD_DATA[3]
F29	VSS	R29	VSS	AD29	PD[5]/IDE_SDD[5]	AK29	IDE_PDD[15]/SD1_WP
F30	GPIO_P0[6]/8051_GPIO_P0[6]/SERVO[6]	R30	SOUT1/GPIO_P4[1]/8051_GPIO_P4[1]/SERVO[25]	AD30	ACK#/IDE_SDD[11]	AK30	AK30_NC

4.3. Pin List Table

Function	Symbol	PIN Sum
SYSTEM	PWRGOOD, CLK25MOUT, XOUT_14318, XIN_14318, SPEAKER, CLK24MOUT	6 PINs
DDRII Interface	DRAMCLK, DRAMCLK#, DRAMCLK1, DRAMCLK1#,RAS#, CAS#, WE#, CKE,CS1#, CS0#, DQM[3:0], DQS[3:0], DQS#[3:0], ODT[1], ODT[0], OCDBIAS, OCDBIAS1, VREF, VREF1, BA[2:0],MD[31:0], MA[14:0]	78 PINs
USB Interface	USB_DP,USB_DM, USB1_DP, USB1_DM, USB2_DP, USB2_DM, USB3_DP, USB3_DM REXT1, REXT	10 PINs
PCI Bus Interface	REQ#[2:0],GNT#[2:0],PCIRST#,PCICLK[0], PCICLK[1],PCICLK[2],AD[31:0],CBE#[3:0], FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, INTA#, INTB#, INTC#, INTD#	56 PINs
SPI Interface	SPI_CS#, SPI_CLK/STRAP_JTAG, SPI_DO, SPI_DI	4 PINs
External SPI/ GPIO port 3[3-0]/ 8051 GPIO port 3[3-0]/ General Shift Interface	E_SPI_CS#/GPIO_P3[0]/8051_GPIO_P3[0]/GSF_CH0, E_SPI_CLK/GPIO_P3[1]/8051_GPIO_P3[1]/GSF_CH1, E_SPI_DO/GPIO_P3[2]/8051_GPIO_P3[2]/GSF_CH2, E_SPI_DI/GPIO_P3[3]/8051_GPIO_P3[3]/GSF_CLK	4 PINs
LPC Bus Interface	SERIRQ, LAD[3:0], LFRAME#, LDRQ#	7 PINs
KBD / MOUSE Interface	KBCLK/KBRST#, KBDAT/A20GATE#, MSCLK, MSDAT	4 PINs
RTC Interface	RTC_PS, RTC_XOUT, RTC_XIN	3 PINs
GPIO PORT 3[7-4]/ 8051 GPIO PORT 3[7-4]/ I2C Interface	GPIO_P3[7]/8051_GPIO_P3[7]/I2C1_SDA, GPIO_P3[6]/8051_GPIO_P3[6]/I2C1_SCL, GPIO_P3[5]/8051_GPIO_P3[5]/I2C_SDA, GPIO_P3[4]/8051_GPIO_P3[4]/I2C_SCL	4 PINs
COM1/ GPIO PORT 4/ 8051 GPIO PORT 4/ SERVO[31:24] Interface	SIN1/GPIO_P4[4]/8051_GPIO_P4[4]/SERVO[28], SOUT1/GPIO_P4[1]/8051_GPIO_P4[1]/SERVO[25], RTS1#/GPIO_P4[2]/8051_GPIO_P4[2]/SERVO[26], CTS1#/GPIO_P4[7]/8051_GPIO_P4[7]/SERVO[31], DSR1#/GPIO_P4[6]/8051_GPIO_P4[6]/SERVO[30], DCD1#/GPIO_P4[0]/8051_GPIO_P4[0]/SERVO[24], RI1#/GPIO_P4[3]/8051_GPIO_P4[3]/SERVO[27], DTR1#/GPIO_P4[5]/8051_GPIO_P4[5]/SERVO[29], TXD_EN1	9 PINs
COM 3,4	SIN3, SOUT3, SIN4, SOUT4	4 PINs
Primary IDE/SD Interface	IDE_PDD[0]/SD_DATA[2], IDE_PDD[1]/SD_DATA[3], IDE_PDD[2]/SD_CMD, IDE_PDD[3]/SD_CLK, IDE_PDD[4]/SD_DATA[0], IDE_PDD[5]/SD_DATA[1], IDE_PDD[6]/SD_CD, IDE_PDD[7]/SD_WP, IDE_PDD[8]/SD1_DATA[2], IDE_PDD[9]/SD1_DATA[3], IDE_PDD[10]/SD1_CMD, IDE_PDD[11]/SD1_CLK, IDE_PDD[12]/SD1_DATA[0], IDE_PDD[13]/SD1_DATA[1], IDE_PDD[14]/SD1_CD,	29 PINs

Function	Symbol	PIN Sum
	IDE_PDD[15]/SD1_WP, IDE_PRST#, IDE_PDRQ, IDE_PIOW#/SD_RW, IDE_PIOR#/SD1_RW, IDE_PIORDY, IDE_PDACK#, IDE_PINT, IDE_PA[2:0], IDE_PCBLID#, IDE_PCS0#, IDE_PCS1#	
Secondary IDE/COM3, COM4 PRINT1 Interface	PD/IDE_SDD[7:0], SLCT/IDE_SDD[8], PE/IDE_SDD[9], BUSY/IDE_SDD[10], ACK#/IDE_SDD[11], SLIN#/IDE_SDD[12], INIT#/IDE_SDD[13], ERR#/IDE_SDD[14], AFD#/IDE_SDD[15], RTS3#/IDE_SRST#, DCD3#/IDE_SDRQ, CTS4#/IDE_SIOW#, CTS3#/IDE_SIOR#, RI3#/IDE_SIORDY, DTR3#/IDE_SDACK#, RTS4#/IDE_SINT, RI4#/IDE_SA[1], DSR3#/IDE_SCBLID#, DTR4#/IDE_SA[0], DCD4#/IDE_SA[2], STB#/IDE_SCS0#, DSR4#/IDE_SCS1#	29 PINs
GPIO Interface	GPIO_P0[7:0] /8051_GPIO_P0[7:0]/SERVO[7:0],GPIO_P1[7:0] /8051_GPIO_P1[7:0]/SERVO[15:8], GPIO_P2[7:0]/8051_GPIO_P2[7:0]/SERVO[23:16]	24 PINs
Ethernet Interface	LINK/ACTIVE, DUPLEX, ISET, ATSTP, ATSTN, TXN, TXP, RXN, RXP MDC,MDIO, COL, RXC, RXD[3:0], RXDV, TXC, TXD[3:0], TXEN	24 PINs
USB Device	UD_DP, UD_DM	2 PINs
JTAG Interface	TDO, TMS, TCK, TDI	4 PINs
HAD Interface	HDA_BCLK, HDA_SYNC, HDA_SDO, HDA_SDI, HDA_RST#	5 PINs
VGA DVO Interface	G_FPD[0]/G_TVD[0], G_FPD[1]/G_TVD[1], G_FPD[2]/G_TVD[2], G_FPD[3]/G_TVD[3], G_FPD[4]/G_TVD[4], G_FPD[5]/G_TVD[5], G_FPD[6]/G_TVD[6], G_FPD[7]/G_TVD[7], G_FPD[8]/G_TVD[8], G_FPD[9]/G_TVD[9], G_FPD[10]/G_TVD[10], G_FPD[11]/G_TVD[11], G_FP1DE/G_TVDE, G_FP1HS/G_TVHS, G_FP1VS/G_TVVS, G_FP1CLK/G_TVCLKO, G_TVCLKIN, G_FP1DET/G_TVDET, G_FPD[12]/G_CAPD[0], G_FPD[13]/G_CAPD[1], G_FPD[14]/G_CAPD[2], G_FPD[15]/G_CAPD[3], G_FPD[16]/G_CAPD[4], G_FPD[17]/G_CAPD[5], G_FPD[18]/G_CAPD[6], G_FPD[19]/G_CAPD[7], G_FPD[20]/G_CAPFILD, G_FPD[21]/G_CAPHS, G_FPD[22]/G_CAPVS, G_FPD[23]/G_CAPCLK, G_ENVDD, G_ENBLT, G_ENVEE	33 PINs
VGA DAC Interface	G_REXT, G_IOR, G_IOG, G_IOB, G_VSYNC, G_HSYNC	6 PINs
VGA GPIO Interface	G_GPIO[2], G_GPIO[3]	2 PINs
VGA I2C Interface	G_DDC1_CLK, G_DDC1_DAT, G_DDC_CLK, G_DDC_DAT	4 PINs
VGA Power Interface	AVDD_DACR18, AVSS_DACR18, AVDD_DACG18, AVSS_DACG18, AVDD_DACB18, AVSS_DACB18, AVDD_DACBG18, AVSS_DACBG18, AVDD_VDISPLL18, AVSS_VDISPLL18, VDD_DAC10	11 PINs
INTERNAL SPI CONTROL	SPIFL_WP#, SPIFL_HOLd#	2 PINs
1 V Power	VDD10 (19 PINs)	19 PINs
1.8V Power	VDE18 (13 PINs), VDD_DDR18(16 PINs), AVDD_USB18, AVSS_USB18, AVDD_USBPLL18,AVSS_USBPLL18, AVDD3_USB18, AVDD2_USB18, AVDD1_USB18, AVSS3_USB18, AVSS2_USB18, AVSS1_USB18, AVDD1_USBPLL18, AVSS1_USBPLL18, AVDD_DDRPLL18, AVSS_DDRPLL18, AVDD_CPUPLL18, AVSS_CPUPLL18	45 PINs
Battery Power	VDD_BAT, VSS_BAT	2 PINs
3.3V Power	AVDD_PLL33, AVSS_PLL33, VDD33(38 PINs), AVSS_EPHYPLL33, AVDD_EPHYPLL33,	50 PINs

Function	Symbol	PIN Sum
	AVSS_EPHYBG33, AVDD_EPHYBG33, AVDD1_EPHYTX33, AVSS1_EPHYTX33, AVDD_EPHYRX33, AVSS_EPHYRX33,AVDD1_USB33, AVDD_USB33	
Digital Ground	VSS	234 PINs
NC pin	NC	4 PINs

4.4. Signal Description

This chapter provides a detailed description of SoC signals. A signal with the symbol "#" at the end of itself indicates that this pin is low active. Otherwise, it is high active.

The following notations are used to describe the signal types:

I Input pin

O Output pin

OD Output pin with open-drain

I/O Bi-directional Input/Output pin

- **System (6 PINs)**

PIN No.	Symbol	Type	Description
AB25	PWRGOOD	I	***Power-Good Input.*** This signal comes from Power Good of the power supply to indicate that the power is available. The SoC uses this signal to generate reset sequence for the system.
C11	CLK25MOUT	O	***25MHz Clock output.***
AB30	CLK24MOUT	O	***24MHz Clock output***
B14	XOUT_14318	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator).
A14	XIN_14318	I	***Crystal-in.*** 14.318MHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).
T29	SPEAKER	O	***Speaker Output.*** This pin is used to control the Speaker Output and should be connected to the Speaker
	STRAP_EPS	I	***Ethernet PHY Select*** Pull it low to select internal PHY. Pull it high to select External PHY. Tri-state to select Internal PHY AFE-test Mode. Default internal tri-state.

- **DDRII Interface (78 PINs)**

PIN No.	Symbol	Type	Description
AB1 AJ3	DRAMCLK DRAMCLK1	O	***Clock output.*** This pin provides the fundamental timing for the DDRII controller.
AB2 AK2	DRAMCLK# DRAMCLK1#	O	***Clock output.*** This pin provides the fundamental timing for the DDRII controller.
AE4	RAS#	O	***Row Address Strobe.*** When asserted, this signal latches row address on positive edge of the DDRII clock. This signal also allows row access and pre-charge.
AD2	CAS#	O	***Column Address Strobe.*** When asserted, this signal latches column address on the positive edge of the DDRII clock. This signal also allows column access and pre-charge.

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>AH2</td><td>WE#</td><td>O</td><td>Memory Write Enable. This pin is used as a write enable for the memory data bus.</td></tr>
<tr><td>AH1</td><td>CKE</td><td>O</td><td>Clock Enable. CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers.</td></tr>
<tr><td>AD5,AH3</td><td>CS1# CS0#</td><td>O</td><td>Chip Select CS1# & CS0#. These two pins activate the DDRII devices. First Bank of DDRII accepts any command when the CS0# pin is active low. Second Bank of DDRII accepts any command when the CS1# pin is active low.</td></tr>
<tr><td>AK6,AF7,T2,V5</td><td>DQM[3:0]</td><td>O</td><td>Data Mask DQM[3:0]. These pins act as synchronized output enables during read cycles and byte masks during write cycles.</td></tr>
<tr><td>AK7,AG7,T1,U4</td><td>DQS[3:0]</td><td>I/O</td><td>Data Strobe DQS[3:0] for DDRII only. Output with write data, input with the read data for source synchronous operation.</td></tr>
<tr><td>AK8,AG8,U1,T4</td><td>DQS#[3:0]</td><td>I/O</td><td>Data Strobe DQS#[3:0] for DDRII only. Output with write data, input with the read data for source synchronous operation.</td></tr>
<tr><td rowspan="2">AJ1</td><td>ODT[0]</td><td>O</td><td>On Die Termination Control for DDRII only. ODT(registered HIGH) enables on die termination resistance internal to the DDR2 SDRAM.</td></tr>
<tr><td>STRAP_IDESC</td><td>I</td><td>Pulled low: 33 PINS is for Secondary IDE.
Pulled high: 33 PINS is for COM3/4 and Parallel Port. Default internal pull-high.</td></tr>
<tr><td rowspan="2">AF2</td><td>ODT[1]</td><td>O</td><td>On Die Termination Control for DDRII only. ODT(registered HIGH) enables on die termination resistance internal to the DDR2 SDRAM.</td></tr>
<tr><td>STRAP1_DDR</td><td>I</td><td>DRAM Freq Option (ODT[1])
DDRII clock select..
<table>
<tr><th>ODT[1],PGNT[2:0]</th><th>Frequency(MHz)</th></tr>
<tr><td>4’b0000</td><td>166</td></tr>
<tr><td>4’b0001</td><td>200</td></tr>
<tr><td>4’b0010</td><td>233</td></tr>
<tr><td>4’b0011</td><td>266</td></tr>
<tr><td>4’b0100</td><td>300</td></tr>
<tr><td>4’b0101</td><td>333</td></tr>
<tr><td>4’b0110</td><td>366</td></tr>
<tr><td>4’b0111</td><td>400</td></tr>
</table></td></tr>
<tr><td>T6
AG11</td><td>OCDBIAS
OCDBIAS1</td><td>I</td><td>OCD BIAS for DDRII only. The OCD bias circuit generates a bias level voltage that makes the reference resistance for driver impedance calibration an appropriate value</td></tr>
<tr><td>V6
AH8</td><td>VREF
VREF1</td><td>I</td><td>Reference voltage for DDRII only. Reference voltage for inputs for SSTL interface.</td></tr>
<tr><td>AF1,AF3,AG2</td><td>BA[2:0]</td><td>O</td><td>Bank Address BA[2:0]. These pins are connected to DDRII as bank address pins.</td></tr>
</table>

PIN No.	Symbol	Type	Description
AH10,AJ11,AK10,AJ9,AK4,AJ5,AH4,AH6,AH9,AG10,AF11,AF9,AG6,AH5,AG4,AF5,Y1,W1,V2,W2,P1,R2,P2,R3,W5,W4,V3,U3,R4,P4,R5,U5	MD[31:0]	I/O	***Memory Data MD[31:0].*** These pins are connected to the DDRII data bus.
AD4,AE1,AC3,AD1,AA3,AA2,AB4,AD3,AA4,AC2,AE3,Y3,AA5,Y4AB5	MA[14:0]	O	***Memory Address MA[14-0].*** Normally, these pins are used as the row and column address for DDRII.

- **USB Interface (10 PINs)**

PIN No.	Symbol	Type	Description
B19 A19	USB_DP USB_DM	I/O	Universal Serial Bus Controller 0 Port 0. These are the serial data pair for USB Port 0. 15kΩ pull down resistors are connected to DP and DM internally.
B20 A20	USB1_DP USB1_DM	I/O	Universal Serial Bus Controller 0 Port 1. These are the serial data pair for USB Port 1. 15kΩ pull down resistors are connected to DP and DM internally.
B22 A22	USB2_DP USB2_DM	I/O	Universal Serial Bus Controller 1 Port 0. These are the serial data pair for USB Port 2. 15kΩ pull down resistors are connected to DP and DM internally.
B23 A23	USB3_DP USB3_DM	I/O	Universal Serial Bus Controller 1 Port 1. These are the serial data pair for USB Port 3. 15kΩ pull down resistors are connected to DP and DM internally.
E23	REXT1	I	Universal Serial Bus Controller 1 External Reference Resistance 470Ω ±1%
E21	REXT	I	Universal Serial Bus Controller 0 External Reference Resistance 470Ω ±1%

- **PCI Bus Interface (56 PINs)**

PIN No.	Symbol	Type	Description
AE16,AF15,AE15	REQ#[2:0]	I	***PCI Bus Request.*** These signals are the PCI bus request signals used as inputs by the internal PCI arbiter.

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td rowspan="2">AK15,AJ15,AK13</td><td>GNT#[2:0]</td><td>O</td><td>PCI Bus Grant. These signals are the PCI bus grant output signals generated by the internal PCI arbiter.</td></tr>
<tr><td>STRAP_DDR</td><td>I</td><td>DDRII Clock Table
<table>
<tr><td>PGNT[2:0]</td><td>Frequency(MHz)</td></tr>
<tr><td>3’b000</td><td>166</td></tr>
<tr><td>3’b001</td><td>200</td></tr>
<tr><td>3’b010</td><td>233</td></tr>
<tr><td>3’b011</td><td>266</td></tr>
<tr><td>3’b100</td><td>300</td></tr>
<tr><td>3’b101</td><td>333</td></tr>
<tr><td>3’b110</td><td>366</td></tr>
<tr><td>3’b111</td><td>400</td></tr>
</table></td></tr>
<tr><td>AE20</td><td>PCIRST#</td><td>O</td><td>PCI Reset. This pin is used to reset PCI devices. When it is asserted low, all the PCI devices will be reset.</td></tr>
<tr><td>AF14
AH13
AJ13</td><td>PCICLK[0]
PCICLK[1]
PCICLK[2]</td><td>O</td><td>PCI Clock Output. This clock is used by all of the SoC logic that is in the PCI clock domain.</td></tr>
<tr><td>AE17,AG17,AF19,AE18,AG18,AF17,AF20,AH21,AG20,AE21,AJ21,AF22,AG21,AG22,AF23,AH22,AJ24,AH24,AH25,AG25,AJ26,AK26,AJ27,AK24,AK23,AK22,AK21,AK20,AK19,AK18,AJ17,AK16</td><td>AD[31:0]</td><td>I/O</td><td>PCI Address and Data. The standard PCI address and data lines. The address is driven with PCI Frame assertion and data is driven or received in the following clocks.</td></tr>
<tr><td>AG19,AG23,AH17,AK25</td><td>CBE#[3:0]</td><td>I/O</td><td>Bus Command and Byte Enables. During the address phase, CBE#[3:0] define the Bus Command. During the data phase, CBE#[3:0] define the Byte Enables.</td></tr>
<tr><td>AJ23</td><td>FRAME#</td><td>I/O</td><td>PCI Frame. This pin is driven by a PCI master to indicate the beginning and duration of a PCI transaction.</td></tr>
<tr><td>AG24</td><td>IRDY#</td><td>I/O</td><td>PCI Initiator Ready. This pin is asserted low by the master to indicate that it is able to transfer the current data transfer. A data was transferred if both IRDY# and TRDY# are asserted low during the rising edge of the PCI clock.</td></tr>
</table>

PIN No.	Symbol	Type	Description
AJ20	TRDY#	I/O	***PCI Target Ready*****.** This pin is asserted low by the target to indicate that it is able to receive the current data transfer. A data was transferred if both IRDY# and TRDY# are asserted low during the rising edge of the PCI clock.
AH19	DEVSEL#	I/O	***Device Select.*** This pin is driven by the devices which have decoded the addresses belonging to them.
AH18	STOP#	I/O	***PCI Stop.*** This pin is asserted low by the target to indicate that it is unable to receive the current data transfer.
AJ18	PAR	I/O	***PCI Parity*****.** This pin is driven to even parity by PCI master over the AD[31:0] and CBE#[3:0] bus during address and write data phases. It should be pulled high through a weak external pull-up resistor. The target drives parity during data read.
AA26	INTA#	I/O	***PCI INTA#.*** PCI interrupt input A. It connects to PCI INTA# when normal modes of PCI Interrupts are supported.
AC26	INTB#	I/O	***PCI INTB#.*** PCI interrupt input B. It connects to PCI INTB# when normal modes of PCI Interrupts are supported.
AB26	INTC#	I/O	***PCI INTC#.*** PCI interrupt input C. It connects to PCI INTC# when normal modes of PCI Interrupts are supported.
AC25	INTD#	I/O	***PCI INTD#.*** PCI interrupt input D. It connects to PCI INTD# when normal modes of PCI Interrupts are supported.

- **SPI Interface (4 Balls)**

Ball No.	Symbol	Type	Description
A8	SPI_CS#	O	***SPI Chip Select***
	STRAP_BMS	I	***Boot Mode Select*** Pull it high to select Normal boot(Reset 250ms). Default internal pull-high. Pull it low to select Fast boot.
A10	SPI_CLK	O	***SPI Clock***
	STRAP_ JTAG	I	***JTAG enable*** ***Pull it high to enable JTAG. default internal pull-hig***
A9	SPI_DO	O	***SPI Data Ouput / Output pin, connected with input of flash.***
B9	SPI_DI	I	***SPI Data Input / Input pin, connected with output of flash.***

- **EXTERNAL SPI/GPIO PORT3[3-0]/8051 GPIO PORT3[3-0]/General Shifter Interface (4 PINs)**

PIN No.	Symbol	Type	Description
E8	E_SPI_CS#	O	***External SPI Chip Select***
	GPIO_P3[0]	I/O	***General-Purpose Input/Output Port 3 bit 0.***
	8051_GPIO_P3[0]	I/O	***8051 General-Purpose Input/Output Port 3 bit 0.***
	GSF_CH0	I/O	***General Shifter Channel 0***
C9	E_SPI_CLK	O	***External SPI Clock***

PIN No.	Symbol	Type	Description
	GPIO_P3[1]	I/O	***General-Purpose Input/Output Port 3 bit 1***
	8051_GPIO_P3[1]	I/O	***8051 General-Purpose Input/Output Port 3 bit 1***
	GSF_CH1	I/O	***General Shifter Channel 1***
C8	E_SPI_DO	O	***External SPI Data Ouput it connects to device SDI input.***
	GPIO_P3[2]	I/O	***General-Purpose Input/Output Port 3 bit 2***
	8051_GPIO_P3[2]	I/O	***8051 General-Purpose Input/Output Port 3 bit 2***
	GSF_CH2	I/O	***General Shifter Channel 2***
D9	E_SPI_DI	I	***External SPI Data Input t it connects to device SDO output.***
	GPIO_P3[3]	I/O	***General-Purpose Input/Output Port 3 bit 3***
	8051_GPIO_P3[3]	I/O	***8051 General-Purpose Input/Output Port 3 bit 3***
	GSF_CLK	O	***General Shifter reference Clock***

- **LPC Bus Interface (7 PINs)**

PIN No.	Symbol	Type	Description
AF26	SERIRQ	I/O	***Serial Interrupt Request.*** This pin is used to support the serial interrupt protocol of common architecture.
AG27,AH27,AF25 ,AK27	LAD[3:0]	I/O	***LPC Command, Address and Data LAD[3:0].*** These pins are used to be command/address/data pins of Low-Pin-Count Function.
AE27	LFRAME#	O	***Low Pin Count FRAME# Signal.*** This signal is used as a frame signal of low pin count protocol..
AE23	LDRQ#	I	***Low Pin Count DMA Request Signal.*** This signal is used as a DMA request signal of low pin count protocol.

- **KBD/MOUSE Interface (4 PINs)**

PIN No.	Symbol	Type	Description
AE26	KBCLK	I/O	**Keyboard Clock**. This pin is keyboard clock when used internal 8042.
	KBRST#	I	**Keyboard Reset**. This pin is Keyboard reset when used external 8042.
AE24	KBDAT	I/O	**Keyboard Data**. This pin is keyboard data when used internal 8042.
	A20GATE#	I	**Address Bit 20 Mask**. This pin is A20 mask when used external 8042.
U29	MSCLK	I/O	**Mouse Clock**. This pin is mouse clock when used internal 8042.
T30	MSDAT	I/O	**Mouse Data**. This pin is mouse data when used internal 8042.

- **RTC Interface (3 PINs)**

PIN No.	Symbol	Type	Description
D25	RTC_PS	I	***RTC Battery Power Sense.***
A26	RTC_XOUT	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator)
B26	RTC_XIN	I	***Crystal-in.*** 32.768KHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).

- **GPIO PORT3[7-4]/8051 GPIO PORT3[7-4]/I2C Interface (4 PINs)**

PIN No.	Symbol	Type	Description
C30	GPIO_P3[7]	I/O	***General-Purpose Input/Output Port 3 bit 7.***
	8051_GPIO_P3[7]	I/O	***8051 General-Purpose Input/Output Port 3 bit 7.***
	I2C1_SDA	I/O	***I2C1 Serial Data.***
B28	GPIO_P3[6]	I/O	***General-Purpose Input/Output Port 3 bit 6.***
	8051_GPIO_P3[6]	I/O	***8051 General-Purpose Input/Output Port 3 bit 6.***
	I2C1_SCL	I/O	***I2C1 Serial Clock.***
A28	GPIO_P3[5]	I/O	***General-Purpose Input/Output Port 3 bit 5.***
	8051_GPIO_P3[5]	I/O	***8051 General-Purpose Input/Output Port 3 bit 5.***
	I2C_SDA	I/O	***I2C0 Serial Data.***
E26	GPIO_P3[4]	I/O	***General-Purpose Input/Output Port 3 bit 4.***
	8051_GPIO_P3[4]	I/O	***8051 General-Purpose Input/Output Port 3 bit 4.***
	I2C_SCL	I/O	***I2C0 Serial Clock.***

- **COM1/PORT4/8051 PORT 4/SERVO[31:24] Interface (9 PINs)**

PIN No.	Symbol	Type	Description
P29	SIN1	I	***Receive Data.*** FIFO UART receiver serial data input signal.
	GPIO_P4[4]	I/O	***General-Purpose Input/Output Port 4 bit 4.***
	8051_GPIO_P4[4]	I/O	***8051 General-Purpose Input/Output Port 4 bit 4.***
	SERVO[28]	O	***SERVO[28].***
R30	SOUT1	O	***Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	GPIO_P4[1]	I/O	***General-Purpose Input/Output Port 4 bit 1.***
	8051_GPIO_P4[1]	I/O	***8051 General-Purpose Input/Output Port 4 bit 1.***
	SERVO[25]	O	***SERVO[25].***
P30	RTS1#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS1# signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	GPIO_P4[2]	I/O	***General-Purpose Input/Output Port 4 bit 2.***
	8051_GPIO_P4[2]	I/O	***8051 General-Purpose Input/Output Port 4 bit 2.***
	SERVO[26]	O	***SERVO[26].***

PIN No.	Symbol	Type	Description
K28	CTS1#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS1# signal by reading bit 4 of Modem Status Register (MSR). A CTS1# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS1# changes the state. The CTS1# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS1#.*
	GPIO_P4[7]	I/O	***General-Purpose Input/Output Port 4 bit 7.***
	8051_GPIO_P4[7]	I/O	***8051 General-Purpose Input/Output Port 4 bit 7.***
	SERVO[31]	O	***SERVO[31].***
N29	DSR1#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR1# signal by reading bit5 of the Modem Status Register (MSR). A DSR1# signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR1# changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR1#.*
	GPIO_P4[6]	I/O	***General-Purpose Input/Output Port 4 bit 6.***
	8051_GPIO_P4[6]	I/O	***8051 General-Purpose Input/Output Port 4 bit 6.***
	SERVO[30]	O	***SERVO[30].***
N30	DCD1#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD1# signal by reading bit 7 of the Modem Status Register (MSR). A DCD1# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD1# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD1#.*
	GPIO_P4[0]	I/O	***General-Purpose Input/Output Port 4 bit 0.***
	8051_GPIO_P4[0]	I/O	***8051 General-Purpose Input/Output Port 4 bit 0.***
	SERVO[24]	O	***SERVO[24].***

PIN No.	Symbol	Type	Description
L29	RI1#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI1# signal by reading bit 6 of the Modem Status Register (MSR). An RI1# signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI1# changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI1#.*
	GPIO_P4[3]	I/O	***General-Purpose Input/Output Port 4 bit 3.***
	8051_GPIO_P4[3]	I/O	***8051 General-Purpose Input/Output Port 4 bit 3.***
	SERVO[27]	O	***SERVO[27].***
K29	DTR1#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR1# signal to be inactive during the loop-mode operation.
	GPIO_P4[5]	I/O	***General-Purpose Input/Output Port 4 bit 5.***
	8051_GPIO_P4[5]	I/O	***8051 General-Purpose Input/Output Port 4 bit 5.***
	SERVO[29]	O	***SERVO[29].***
M30	TXD_EN1	O	***COM1 TX Status.*** This pin will be high when COM1 is trnamitting.

- **COM3, 4 (4 PIN)**

PIN No.	Symbol	Type	Description
J28	SIN3	I	***COM3 Receive Data.*** FIFO UART receiver serial data input signal.
J26	SOUT3	O	***COM3 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
L30	SIN4	I	***COM4 Receive Data.*** FIFO UART receiver serial data input signal.
K30	SOUT4	O	***COM4 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.

- **Primary IDE/SD Interface (29 PINs)**

PIN No.	Symbol	Type	Description
AJ30	**IDE_PRST#**	O	***IDE Primary Channel Reset.***
AD27	IDE_PDD[0]	I/O	***IDE Primary Channel Data Bus Data 0.***
	SD_DATA[2]	I/O	***SD0 Data Bus Data 2.***
AK28	IDE_PDD[1]	I/O	***IDE Primary Channel Data Bus Data 1.***
	SD_DATA[3]	I/O	***SD0 Data Bus Data 3.***
AE28	IDE_PDD[2]	I/O	***IDE Primary Channel Data Bus Data 2.***
	SD_CMD	I/O	***SD0 Command/Response.***

PIN No.	Symbol	Type	Description
AC27	IDE_PDD[3]	I/O	***IDE Primary Channel Data Bus Data 3.***
	SD_CLK	O	***SD0 Clock.***
AD28	IDE_PDD[4]	I/O	***IDE Primary Channel Data Bus Data 4.***
	SD_DATA[0]	I/O	***SD0 Data Bus Data 0.***
V26	IDE_PDD[5]	I/O	***IDE Primary Channel Data Bus Data 5.***
	SD_DATA[1]	I/O	***SD0 Data Bus Data 1.***
U25	IDE_PDD[6]	I/O	***IDE Primary Channel Data Bus Data 6.***
	SD_CD	I	***SD0 Card Detect.***
T25	IDE_PDD[7]	I/O	***IDE Primary Channel Data Bus Data 7.***
	SD_WP	I	***SD0 Write Protect.***
AF27	IDE_PDD[8]	I/O	***IDE Primary Channel Data Bus Data 8.***
	SD1_DATA[2]	I/O	***SD1 Data Bus Data 2.***
AH28	IDE_PDD[9]	I/O	***IDE Primary Channel Data Bus Data 9.***
	SD1_DATA[3]	I/O	***SD1 Data Bus Data 3.***
AB27	IDE_PDD[10]	I/O	***IDE Primary Channel Data Bus Data 10.***
	SD1_CMD	I/O	***SD1 Command/Response.***
U26	IDE_PDD[11]	I/O	***IDE Primary Channel Data Bus Data 11.***
	SD1_CLK	O	***SD1 Clock.***
AG28	IDE_PDD[12]	I/O	***IDE Primary Channel Data Bus Data 12.***
	SD1_DATA[0]	I/O	***SD1 Data Bus Data 0.***
U27	IDE_PDD[13]	I/O	***IDE Primary Channel Data Bus Data 13.***
	SD1_DATA[1]	I/O	***SD1 Data Bus Data 1.***
AJ29	IDE_PDD[14]	I/O	***IDE Primary Channel Data Bus Data 14.***
	SD1_CD	I	***SD1 Card Detect.***
AK29	IDE_PDD[15]	I/O	***IDE Primary Channel Data Bus Data 15.***
	SD1_WP	I	***SD1 Write Protect.***
AH30	**IDE_PDRQ**	I	***IDE Primary Channel DMA Request.***
T27	**IDE_PIOW#**	O	***IDE Primary Channel IO Write Strobe.***
	SD_RW	O	***SD Read/Write status. High active***
AG29	**IDE_PIOR#**	O	***IDE Primary Channel IO Read Strobe.***
	SD1_RW	O	***SD1 Read/Write status. High active***
R26	**IDE_PIORDY**	I	***IDE Primary Channel IO Channel Ready.***
AA27	**IDE_PDACK#**	O	***IDE Primary Channel DMA Acknowledge.***
P25	**IDE_PINT**	I	***IDE Primary Channel Interrupt.***
AG30,R27,N25	**IDE_PA[2:0]**	O	***IDE Primary Channel Device Address***
Y27	**IDE_PCBLID#**	I	***IDE Primary Channel Cable Assembly Type Identifier.***
AB28	**IDE_PCS1#**	O	***IDE Primary Channel Chip Select.***
AF29	**IDE_PCS0#**	O	***IDE Primary Channel Chip Select.***

- **Secondary IDE /COM3,4,PRINT1 Interface (29 PINs)**

PIN No.	Symbol	Type	Description
N28,N27,AD29,P26,M27,P27,AE30,AF30	PD[7:0]	I/O	***Parallel port data bus bit .*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[7:0]	I/O	***IDE Secondary Channel Data Bus.***
AA28	SLCT	I	***SLCT.*** An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	IDE_SDD[8]	I/O	***IDE Secondary Channel Data Bus.***
L25	PE	I	***PE.*** An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[9]	I/O	***IDE Secondary Channel Data Bus.***
M28	BUSY	I	***BUSY.*** An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	IDE_SDD[10]	I/O	***IDE Secondary Channel Data Bus.***
AD30	ACK#	I	***ACK#.*** An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[11]	I/O	***IDE Secondary Channel Data Bus.***
AC29	SLIN#	OD	***SLIN#.*** Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[12]	I/O	***IDE Secondary Channel Data Bus.***
M26	INIT#	OD	***INIT#.*** Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[13]	I/O	***IDE Secondary Channel Data Bus.***
AA29	ERR#	I	***ERR#.*** An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[14]	I/O	***IDE Secondary Channel Data Bus.***
W28	AFD#	OD	***AFD#.*** An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[15]	I/O	***IDE Secondary Channel Data Bus.***

PIN No.	Symbol	Type	Description
V28	RTS3#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	IDE_SRST#	O	***IDE Secondary Channel Reset.***
T28	DCD3#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD3# signal by reading bit 7 of the Modem Status Register (MSR). A DCD3# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD3# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD3#.*
	IDE_SDRQ	I	***IDE Secondary Channel DMA Request.***
L27	CTS4#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	IDE_SIOW#	O	***IDE Secondary Channel IO Write Strobe.***
R28	CTS3#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	IDE_SIOR#	O	***IDE Secondary Channel IO Read Strobe.***

PIN No.	Symbol	Type	Description
K27	RI3#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
	IDE_SIORDY	I	***IDE Secondary Channel IO Channel Ready.***
L26	DTR3#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	IDE_SDACK#	O	***IDE Secondary Channel DMA Acknowledge.***
AA30	RTS4#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	IDE_SINT	I	***IDE Secondary Channel Interrupt.***
Y29	RI4#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
	IDE_SA[1]	O	***IDE Secondary Channel Device Address.***
J27	DSR3#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*
	IDE_SCBLID#	I	***IDE Secondary Channel Cable Assembly Type Identifier.***

PIN No.	Symbol	Type	Description
W29	DTR4#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	IDE_SA[0]	O	***IDE Secondary Channel Device Address.***
W30	DCD4#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD4# signal by reading bit 7 of the Modem Status Register (MSR). A DCD4# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD4# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD4#.*
	IDE_SA[2]	O	***IDE Secondary Channel Device Address.***
U30	STB#	OD	***STB#.*** An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SCS0#	O	***IDE Secondary Channel Chip Select.***
V30	DSR4#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#.***
	IDE_SCS1#	O	***IDE Secondary Channel Chip Select.***

- **GPIO Interface (24 PINs)**

PIN No.	Symbol	Type	Description
G28,F30,G29,G30, H28,H29,H30,J30	GPIO_P0[7:0]	I/O	***General-Purpose Input/Output Port 0[7:0].*** Those pins can be programmed input or output individually.
	8051_GPIO_P0[7:0]	I/O	***8051 General-Purpose Input/Output Port 0[7:0].***
	SERVO[7:0]	O	***SERVO[7:0].***
G27,E29,G25,H26, F27,D30,H25,E30	GPIO_P1[7:0]	I/O	***General-Purpose Input/Output Port 1[7:0].*** Those pins can be programmed input or output individually.
	8051_GPIO_P1[7:0]	I/O	***8051 General-Purpose Input/Output Port 1[7:0].***

	SERVO[15:8]	O	***SERVO[15:8].***
F26,C27,D27,E27,C28,E28,D28,D29	GPIO_P2[7:0]	I/O	***General-Purpose Input/Output Port 2[7:0] .*** Those pins can be programmed input or output individually.
	8051_GPIO_P2[7:0]	I/O	***8051 General-Purpose Input/Output Port 2[7:0].***
	SERVO[23:16]	O	***SERVO[23:16].***

- **Ethernet Interface (24 PINs)**

PIN No.	Symbol	Type	Description
C10	LINK/ACTIVE	O	***LINK/ACTIVE:*** Link/active status
D10	DUPLEX	O	***DUPLEX:*** Duplex status
F17	ISET	I	***ISET:*** External resistor connecting pin for BIAS
D16	ATSTP	I/O	***ATSTP:*** Variable Gain Amplifier and ADC testing pin for input and output (positive)
C16	ATSTN	I/O	***ATSTN:*** Variable Gain Amplifier and ADC testing pin for input and output (negative)
B17	TXN	O	***TXN:*** 10B-T/100BT transmitting output pin/ reveiving input pin (positive)
A17	TXP	O	***TXP:*** 10B-T/100BT transmitting output pin/ reveiving input pin (negative)
B16	RXN	I	***RXN:*** 10B-T/100BT reveiving input pin/ transmitting output pin (positive)
A16	RXP	I	***RXP:*** 10B-T/100BT reveiving input pin/ transmitting output pin (negative)
A11	MDC	O	***MDC:*** MII management data clock is sourced by the SoC to the external PHY devices as a timing reference for the transfer of information on the MDIO signal.
F12	MDIO	I/O	***MDIO***: MII management data input/output transfers control information and status between the external PHY and SoC.
B11	COL	I	***COL:*** This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
B12	RXC	I	***RXC:*** Supports the receive clock supplied by the external PMD device. This clock should always be active.
A12,F14,C13,E12	**RXD[3:0]**	I	***RXD[3:0]:*** Four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal.
F11	RXDV	I	***RXDV:*** Data valid is asserted by an external PHY when the received data is present on the **RXD[3:0]** lines and is de-asserted at the end of the packet. This signal should be synchronized with the RXC signal.
D13	TXC	I	***TXC:*** Supports the transmit clock supplied by the external PMD device. This clock should always be active.
F15,D14,E14,E13	**TXD[3:0]**	O	***TXD[3:0]:*** Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal.

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td></td><td>STRAP_CPU</td><td>I</td><td>CPU Clock select.
<table>
<tr><th>TXD[3:0]</th><th>CPU Clock (MHz)</th></tr>
<tr><td>4’b0000</td><td>500</td></tr>
<tr><td>4’b0001</td><td>600</td></tr>
<tr><td>4’b0010</td><td>700</td></tr>
<tr><td>4’b0011</td><td>833</td></tr>
<tr><td>4’b0100</td><td>866</td></tr>
<tr><td>4’b0101</td><td>900</td></tr>
<tr><td>4’b0110</td><td>933</td></tr>
<tr><td>4’b0111</td><td>966</td></tr>
<tr><td>4’b1000</td><td>1000</td></tr>
<tr><td>4’b1001</td><td>1033</td></tr>
<tr><td>4’b1010</td><td>1066</td></tr>
<tr><td>4’b1011</td><td>1100</td></tr>
<tr><td>4’b1100</td><td>1133</td></tr>
<tr><td>4’b1101</td><td>1166</td></tr>
<tr><td>4’b1110</td><td>1200</td></tr>
<tr><td>4’b1111</td><td>800</td></tr>
</table></td></tr>
<tr><td>D15</td><td>TXEN</td><td>O</td><td>TXEN: This pin functions as Transmit Enable. It indicates that a transmission to an external PHY device is active on the MII port.</td></tr>
</table>

- **USB Device (2 PINs)**

PIN No.	Symbol	Type	Description
D18 D19	UD_DP UD_DM	I/O	***Universal Serial Bus Device Controller Port.*** These are the serial data pair for USB Device. Need add 1.5kΩ pull up resistors to UD_DP externally.

- **JTAG Interface (4 PINs)**

PIN No.	Symbol	Type	Description
AH14	TDO	O	***TDO:*** JTAG Test Data Output pin.
AG16	TMS	I	***TMS:*** JTAG Test Mode Select pin.
AG15	TCK	I	***TCK:*** JTAG Test Clock Input pin.
AG14	TDI	I	***TDI:*** JTAG Test Data Input pin.

- **HDA Interface (5 PINs)**

PIN No.	Symbol	Type	Description
V27	H_BCLK	O	Global Link 24.00-MHz clock
W27	H_SYNC	O	Global 48 kHz Frame Sync and outbound tag signal
W25	H_SDO	O	Bussed Serial Data Output(s)
Y25	H_SDI	I/O	Point-to-point Serial Data Input(s). Controller has a weak pull down
W26	H_RST#	O	Global active low reset

- **VGA DVO Interface (33 PINs)**

PIN No.	Symbol	Type	Description
K3	G_FPD[0]	O	DVO data bus
	G_TVD[0]	O	TV output data bus
L1	G_FPD[1]	O	DVO data bus
	G_TVD[1]	O	TV output data bus
M2	G_FPD[2]	O	DVO data bus
	G_TVD[2]	O	TV output data bus
M1	G_FPD[3]	O	DVO data bus
	G_TVD[3]	O	TV output data bus
H1	G_FPD[4]	O	DVO data bus
	G_TVD[4]	O	TV output data bus
J2	G_FPD[5]	O	DVO data bus
	G_TVD[5]	O	TV output data bus
J1	G_FPD[6]	O	DVO data bus
	G_TVD[6]	O	TV output data bus
	G_STRAP[1]	I	Bypass clock mode 0:normal clock operation 1:Bypass all clock with test clock input(Test Mode)
K2	G_FPD[7]	O	DVO data bus
	G_TVD[7]	O	TV output data bus
	G_STRAP[2]	I	PCI debug enable 0: Disable 1: Enable
F1	G_FPD[8]	O	DVO data bus
	G_TVD[8]	O	TV output data bus
	G_STRAP[3]	I	DVP2 port/Capture port select Default : Pull-down 0: DVP2 1: Capture
G3	G_FPD[9]	O	DVO data bus
	G_TVD[9]	O	TV output data bus
	G_STRAP[4]	I	DAC external source enable. 1: data from external pad. 0: data from internal BIST
G1	G_FPD[10]	O	DVO data bus
	G_TVD[10]	O	TV output data bus
H2	G_FPD[11]	O	DVO data bus
	G_TVD[11]	O	TV output data bus
N6	G_FP1DE	O	DVO data enable
	G_TVDE	O	TV output data enable
	G_STRAP[5]	I	PCI VGA config Pr-fetch status 0: Pre-fetch bit = 0 1: Pre-fetch bit = 1

PIN No.	Symbol	Type	Description
N5	G_FP1HS	O	DVO hsync
	G_TVHS	O	TV hsync
	G_STRAP[6]	I	DAC, PLL test enable
M6	G_FP1VS	O	DVO vsync
	G_TVVS	O	TV vsync
	G_STRAP[7]	I	DVP1 port/TV port select 0:DVP1 1:TV
M3	G_FP1CLK	O	DVO output clock
	G_TVCLKO	O	TV output clock
F3	G_TVCLKIN	I	TV input clock
N3	G_FP1DET	I	DVO device detect
	G_TVDET	I	TV device detect
M4	G_FPD[12]	O	DVO data bus
	G_CAPD[0]	I	Capture input data bus
L3	G_FPD[13]	O	DVO data bus
	G_CAPD[1]	I	Capture input data bus
M5	G_FPD[14]	O	DVO data bus
	G_CAPD[2]	I	Capture input data bus
L4	G_FPD[15]	O	DVO data bus
	G_CAPD[3]	I	Capture input data bus
K4	G_FPD[16]	O	DVO data bus
	G_CAPD[4]	I	Capture input data bus
K5	G_FPD[17]	O	DVO data bus
	G_CAPD[5]	I	Capture input data bus
L6	G_FPD[18]	O	DVO data bus
	G_CAPD[6]	I	Capture input data bus
J3	G_FPD[19]	O	DVO data bus
	G_CAPD[7]	I	Capture input data bus
J5	G_FPD[20]	O	DVO data bus
	G_CAPFILD	I	Capture Fild
K6	G_FPD[21]	O	DVO data bus
	G_CAPHS	I	Capture hsync
H3	G_FPD[22]	O	DVO data bus
	G_CAPVS	I	Capture vsync
H4	G_FPD[23]	O	DVO data bus
	G_CAPCLK	I	Capture input clock
G5	G_ENVDD	O	Panel Power Sequence signal. "ENVDD"
G4	G_ENBLT	O	Panel Power Sequence signal."Enable Backlight"
J6	G_ENVEE	O	Panel Power Sequence signal. "ENVEE"

- **VGA DAC Interface (6 PINs)**

PIN No.	Symbol	Type	Description
F7	G_REXT	I	RESET DAC Signal. An external resistor is connected between REXT and GND to determine the reference current. Default is 511 Ohm.
B1	G_IOR	O	Analog Red
C1	G_IOG	O	Analog Green
D1	G_IOB	O	Analog Blue
G6	G_VSYNC	O	CRT VSYNC
D5	G_HSYNC	O	CRT HSYNC

- **VGA GPIO Interface (2 PINs)**

PIN No.	Symbol	Type	Description
F5	G_GPIO[2]	IO	General I/O Port:clock
E5	G_GPIO[3]	IO	General I/O Port:data
	G_STRAP[0]	I	Hardware strapping bus

- **VGA I2C Interface (4 PINs)**

PIN No.	Symbol	Type	Description
H5	G_DDC_CLK	IOD	First DDC Clock.
D4	G_DDC_DAT	IOD	First DDC Data.
F2	G_DDC1_CLK	IOD	Second DDC serial clock.
E4	G_DDC1_DAT	IOD	Second DDC serial data.

- **VGA Power Interface (11 PINs)**

PIN No.	Symbol	Type	Description
E6	VDD_DAC10	I	1V digital power of DAC Power
B3	AVDD_DACR18	I	DAC Power Pin for RED Channel, 1.8V
B2	AVSS_DACR18	I	DAC Ground Pin for RED Channel
C3	AVDD_DACG18	I	DAC Power Pin for GREEN Channel, 1.8V
C2	AVSS_DACG18	I	DAC Ground Pin for GREEN Channel
D3	AVDD_DACB18	I	DAC Power Pin for BLUE Channel, 1.8V
D2	AVSS_DACB18	I	DAC Ground Pin for BLUE Channel
F8	AVDD_DACBG18	I	DAC Power Pin for Bandgap, 1.8V
F6	AVSS_DACBG18	I	DAC Ground Pin for Bandgap, 1.8V
K11	AVDD_VDISPLL18	I	VGA Display PLL Analog Power
L11	AVSS_VDISPLL18	I	VGA Display PLL Ground

- **INTERNAL SPI CONTROL (2 PINs)**

PIN No.	Symbol	Type	Description
D11	SPIFL_WP#	I	***Write- protect pin of SPI embedded flash, must pull high to 3.3V by a 10K ohm resistor.***
E10	SPIFL_HOLd#	I	***Hold pin of SPI embedded flash, must pull high to 3.3V by a 10K ohm resistor.***

- **1V POWER (19 PINs)**

PIN No.	Symbol	Type	Description
V10,V11,V12,V13,W10,W13,Y6,Y13,AA6,AA10,AA11,AA12,AA13,AC6,AE6,AE8,AE10,AE12,AE13	VDD10 (19 PINs)	I	Core power

- **1.8V POWER (45 PINs)**

PIN No.	Symbol	Type	Description
F19,J25,K19,K21,L18,L20,M21,M25,N18,N20,P18,P20,P21	VDE18 (13 PINs)	I	1.8V SB Vcore Power
T5,U2,U6,U10,W3,Y5,AA14,AC1,AC5,AF6,AF8,AF10,AG1,AG3,AJ6,AJ10	VDD_DDR18(16 PINs)	I	1.8V DDR Power
A24 B21 A21 A18	AVDD3_USB18 AVDD2_USB18 AVDD1_USB18 AVDD_USB18	I	Analog Power USB 1.8 V Power
C23 C22 C20 C19	AVSS3_USB18 AVSS2_USB18 AVSS1_USB18 AVSS_USB18	I	Analog ground USB 1.8 V ground
E22 E20	AVSS1_USBPLL18 AVSS_USBPLL18	I	USB PLL Ground
D22 D20	AVDD1_USBPLL18 AVDD_USBPLL18	I	USB PLL Power
K13	AVDD_DDRPLL18	I	DRAM PLL Analog Power

PIN No.	Symbol	Type	Description
L13	AVSS_DDRPLL18	I	DRAM PLL Analog Ground
K12	AVDD_CPUPLL18	I	CPU PLL Analog Power
L12	AVSS_CPUPLL18	I	CPU PLL Analog Ground

- **Battery POWER (2 PINs)**

PIN No.	Symbol	Type	Description
A25	**VDD_BAT**	I	Battery power for RTC
B25	**VSS_BAT**	I	Battery ground for RTC

- **3.3V Power (50 PINs)**

PIN No.	Symbol	Type	Description
A13	**AVDD_PLL33**	I	Analog power SB PLL Power
C15	**AVSS_PLL33**	I	Analog ground SB PLL Ground
B13,B29,D8,D12,D26,F9,F25,G2,H6,K1,K17,K26,L28,N17,P6,R17,R19,R21,T10,T13,T15,T26,U15,U28,V25,W15,AA15,AC28,AD25,AE19,AE22,AF13,AH15,AH23,AH26,AJ28,AK14,AK17	VDD33 (38 PINs)	I	Analog power CPU I / O PAD Power SB I/O PAD Power
E16	AVSS_EPHYPLL33	I	Analog Ground, E-PHY PLL
F16	AVDD_EPHYPLL33	I	Analog power, E-PHY PLL
E18	AVSS_EPHYBG33	I	Analog ground, E-PHY BandGap
F18	AVDD_EPHYBG33	I	Analog power, E-PHY BandGap
C17	AVDD_EPHYRX33	I	Analog power, E-PHY for TX
D17	AVSS_EPHYRX33	I	Analog ground, E-PHY for TX
A15	AVDD1_EPHYTX33	I	Analog power, E-PHY for RX
B15	AVSS1_EPHYTX33	I	Analog ground, E-PHY for RX
F22	AVDD1_USB33	I	USB Analog power
F20	AVDD_USB33	I	USB Analog power

- **Digital Ground (234 PINs)**

PIN No.	Symbol	Type	Description

PIN No.	Symbol	Type	Description
A2,A3,A4,A5,A6,A27,A29,B4,B5,B6,B8,B10,B18,B24,B27,B30,C4,C5,C6,C7,C12,C14,C18,C21,C24,C25,C26,C29,D6,D7,D21,D23,D24,E1,E2,E3,E7,E9, E11,E15,E17,E19,E24,E25,F4,F10,F13,F21,F23,F24,F28,F29,G26,H27,J4,J29,K10,K14,K15,K16,K18,K20,K25,L2,L5,L10,L14,L15,L16,L17,L19,L21,M10,M11,M12,M13,M14,M15,M16,M17,M18,M19,M20,M29,N1,N2,N4,N10,N11,N12,N13,N14,N15,N16,N19,N21,N26,P3,P5,P10,P11,P12,P13,P14,P15,P16,P17,P19,P28,R1,R6,R10,R11,R12,R13,R14,R15,R16,R18,R20,R25,R29,T3,T11,T12,T14,T16,T17,T18,T19,T20,T21,U11,U12,U13,U14,U16,U17,U18,U19,U20,U21,V1,V4,V14,V15,V16,V17,V18,V19,V20,V21,V29,W6,W11,W12,W14,W16,W17,W18,W19,W20,W21,Y2,Y10,Y11,Y12,Y14,Y15,Y16,Y17,Y18,Y19,Y20,Y21,Y26,Y28,Y30,AA1,AA16,AA17,AA18,AA19,AA20,AA21,AA25,AB3,AB6,AB29,AC4,AC30,AD6,AD26,AE2,AE5,AE7,AE9,AE11,AE1	VSS	I	Digital Ground

PIN No.	Symbol	Type	Description
4,AE25,AE29,AF4,AF12,AF16,AF18,AF21,AF24,AF28,AG5,AG9,AG12,AG13,AG26,AH7,AH11,AH12,AH16,AH20,AH29,AJ2,AJ4,AJ7,AJ8,AJ12,AJ14,AJ16,AJ19,AJ22,AJ25,AK3,AK5,AK9,AK11,AK12			

- **NC pin (4 PINs)**

PIN No.	Symbol	Type	Description
A1,A30,AK1,AK30	NC	I	NC

4.5. PIN Capacitance Description

North-Bridge:

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance	1.94304	2.05082	2.08563	pF
C_{BID}	3.3V Bi-directional Capacitance	2.18057(max loading= 40)	2.21818(max loading=40)	2.2269(max loading= 40)	pF

VGA:

Symbol	Parameter	Min.	Max.	Unit
C_{BID}	3.3V Bi-directional Capacitance	2(max loading= 40)	2.5(max loading= 40)	pF

South-Bridge:

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance	3.144	3.143	3.216	pF
C_{BID}	3.3V Bi-directional Capacitance	3.179	3.116	3.099	pF

4.6. PIN Pull-up / Pull-down Description

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
PWRGOOD	I	--	--	--	Y	Y	--	
CLK25MOUT	O	Note10	--	--	--	--	Note10	
CLK24MOUT	O	Note10	--	--	--	--	Note10	
XOUT_14318	O	--	--	--	--	--	--	
XIN_14318	I	--	--	--	--	--	--	
SPEAKER	O	8mA	--	--	--	--	S	
DRAMCK	O	13.4mA	Note14	Note14	N	N	FIX	DDR2 signal
DRAMCLK#	O	13.4mA	Note14	Note14	N	N	FIX	DDR2 signal
RAS#	O	13.4mA	Note13	Note13	N	N	FIX	DDR2 signal
CAS#	O	13.4mA	Note13	Note13	N	N	FIX	DDR2 signal
WE#	O	13.4mA	Note13	Note13	N	N	FIX	DDR2 signal
CKE	O	13.4mA	Note13	Note13	N	N	FIX	DDR2 signal
CS1# CS0#	O	13.4mA	Note13	Note13	N	N	FIX	DDR2 signal

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
DQM[3:0]	O	13.4mA	Note13	Note13	N	N	FIX	DDR2 signal
DQS[3:0]	I/O	13.4mA	Note14	Note14	N	N	FIX	DDR2 signal
DQS#[3:0]	I/O	13.4mA	Note14	Note14	N	N	FIX	DDR2 signal
ODT[1:0]	O	13.4mA	Note13	Note13	N	N	FIX	DDR2 signal
OCDBIAS	I				N	N	FIX	DDR2 signal
VREF	I				N	N	FIX	DDR2 signal
BA[2:0]	O	13.4mA	Note13	Note13	N	N	FIX	DDR2 signal
MD[31:0]	I/O	13.4mA	Note14	Note14	N	N	FIX	DDR2 signal
MA[14:0]	O	13.4mA	Note13	Note13	N	N	FIX	DDR2 signal
USB_DP	I/O	--	--	--	--	--	--	Note5
USB_DM	I/O	--	--	--	--	--	--	Note5
USB1_DP	I/O	--	--	--	--	--	--	Note5
USB1_DM	I/O	--	--	--	--	--	--	Note5
USB2_DP	I/O	--	--	--	--	--	--	Note5
USB2_DM	I/O	--	--	--	--	--	--	Note5
USB3_DM	I/O	--	--	--	--	--	--	Note5
USB3_DP	I/O	--	--	--	--	--	--	Note5
REXT1	I	--	--	--	--	--	--	Note5
REXT	I	--	--	--	--	--	--	Note5
REQ#[2:0]	I	--	Y	--	--	N	--	Note2
GNT#[2:0]	O	--	--	--	--	--	--	Note2
PCIRST#	O	Note9	--	--	--	--	Note9	--
PCICLK[2:0]	O	Note12	--	--	--	--	--	Note2
AD[31:0]	I/O	Note11	--	--	Y	N	Note11	--
CBE#[3:0]	I/O	Note11	Y	--	Y	N	Note11	--
FRAME#	I/O	Note11	Y	--	Y	N	Note11	--
IRDY#	I/O	Note11	Y	--	Y	N	Note11	--
TRDY#	I/O	Note11	Y	--	Y	N	Note11	--
DEVSEL#	I/O	Note11	Y	--	Y	N	Note11	--
STOP#	I/O	Note11	Y	--	Y	N	Note11	--
PAR	I/O	Note11	Y	--	Y	N	Note11	--
INTA#	I/O	16mA	Y	--	Y	N	F	--
INTB#	I/O	16mA	Y	--	Y	N	F	--
INTC#	I/O	16mA	Y	--	Y	N	F	--
INTD#	I/O	16mA	Y	--	Y	N	F	--
SPI_CS	O	8mA	--	--	--	Y	S	
SPI_CLK	O	8mA	--	--	--	Y	S	
SPI_DO	O	8mA	--	--	--	Y	S	
SPI_DI	I		--	--	--	Y	S	
E_SPI_CS	O	Note9	--	--	--	Y	S	
E_SPI_CLK	O	Note9	--	--	--	Y	S	
E_SPI_DO	O	Note9	--	--	--	Y	S	
E_SPI_DI	I	Note9	--	--	--	Y	S	
GPIO_P0[7:0]	I/O	Note9	Note1	--	Y	Y	F	
GPIO_P1[7:0]	I/O	Note9	Note1	--	Y	Y	F	
GPIO_P2[7:0]	I/O	Note9	Note1	--	Y	Y	F	

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
GPIO_P3[3:0]	I/O	Note9	Note1	--	Y	Y	F	
GPIO_P3[7:4]	I/O	Note9	Note1	--	Y	Y	S	
GPIO_P4[7:0]	I/O	Note9	Note1	--	N	Y	S	
8051_GPIO_P0[7:0]	I/O	Note9	Note1	--	Y	Y	F	
8051_GPIO_P1[7:0]	I/O	Note9	Note1	--	Y	Y	F	
8051_GPIO_P2[7:0]	I/O	Note9	Note1	--	Y	Y	F	
8051_GPIO_P3[3:0]	I/O	Note9	Note1	--	Y	Y	F	
8051_GPIO_P3[7:4]	I/O	Note9	Note1	--	Y	Y	S	
8051_GPIO_P4[7:0]	I/O	Note9	Note1	--	N	Y	S	
GSF_CH0	I/O	Note9	Note1	--	Y	Y	F	
GSF_CH1	I/O	Note9	Note1	--	Y	Y	F	
GSF_CH2	I/O	Note9	Note1	--	Y	Y	F	
GSF_CLK	O	Note9	--	--	--	--	F	
SERIRQ	I/O	Note9	Note4	--	Y	N	Note9	--
LAD[3:0]	I/O	Note9	Note4	--	Y	N	Note9	--
LFRAME#	O	Note9	Note4	--	Y	--	Note9	--
LDRQ#	I	--	Note4	--	Y	N	--	--
KBRST#	I	--	Y	--	N	Y	S	
A20GATE#	I	--	Y	--	N	Y	S	
KBCLK	I/O	16mA	Y	--	N	Y	S	
KBDAT	I/O	16mA	Y	--	N	Y	S	
MSCLK	I/O	16mA	Y	--	N	Y	S	
MSDAT	I/O	16mA	Y	--	N	Y	S	
RTC_PS	I	--	--	--	--	--	--	
RTC_XOUT	O	--	--	--	--	--	--	
RTC_XIN	I	--	--	--	--	--	--	
I2C1_SDA	I/O	Note9	Y	--	Y	Y	S	
I2C1_SCL	I/O	Note9	Y	--	Y	Y	S	
I2C_SDA	I/O	Note9	Y	--	Y	Y	S	
I2C_SCL	I/O	Note9	Y	--	Y	Y	S	
SIN1/SIN3/SIN4	I	--	--	--	N	Y	--	
SOUT1	O	Note9	--	--	--	--	S	
SOUT3/SOUT4	O	8mA	--	--	--	--	S	
RTS1#	O	Note9	--	--	--	--	S	
RTS3#	O	8mA	--	--	--	--	S	
RTS4#	O	8mA	--	Y	--	--	S	
CTS1#/CTS3#/CTS4#	I	--	Y	--	--	Y	--	
DSR1#/DSR3#/DSR4#	I	--	Y	--	--	Y	--	
DCD1#/DCD3#/DCD4#	I	--	Y	--	--	Y	--	
RI1#/RI3#/RI4#	I	--	Y	--	--	Y	--	
DTR1#/DTR3#/DTR4#	O	8mA	--	--	--	--	S	
TXD_EN1	O	8mA	--	--	--	--	S	
SERVO[23:0]	O	Note9					F	
SERVO[32:24]	O	Note9					S	
IDE_PRST#	O	Note3	--	--	--	--	F	
IDE_PDD[15:0]	I/O	Note3	--	Y	--	Y	F	
IDE_PDRQ	I	--	--	Y	--	Y	--	
IDE_PIOW#	O	Note3	--	--	--	--	F	
IDE_PIOR#	O	Note3	--	--	--	--	F	
IDE_PIORDY	I	--	Y	--	--	Y	--	
IDE_PDACK#	O	Note3	--	--	--	--	F	
IDE_PINT	I	--	--	Y	--	Y	--	

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
IDE_PA[2:0]	O	Note3	--	--	--	--	F	
IDE_PCBLID#	I	--	Y	--	--	Y	--	
IDE_PCS1#	O	Note3	--	--	--	--	F	
IDE_PCS0#	O	Note3	--	--	--	--	F	
IDE_SRST#	O	Note3	--	--	--	--	F	
IDE_SDD[15:0]	I/O	Note3	--	Y	--	Y	F	
IDE_SDRQ	I	--	--	Y	--	Y	--	
IDE_SIOW#	O	Note3	Y	--	--	--	F	
IDE_SIOR#	O	Note3	--	--	--	--	F	
IDE_SIORDY	I	--	Y	--	--	Y	--	
IDE_SDACK#	O	Note3	--	--	--	--	F	
IDE_SINT	I	--	--	Y	--	Y	--	
IDE_SA[2:1]	O	Note3	Y	--	--	--	F	
IDE_SA[0]	O	Note3	--	--	--	--	F	
IDE_SCBLID#	I	--	Y	--	--	Y	--	
IDE_SCS1#	O	Note3	Y	--	--	--	F	
IDE_SCS0#	O	Note3	--	--	--	--	F	
SD_DATA[3:0]	I/O		Y					
SD_CMD	I/O		Y					
SD_CLK	O			Y				
SD_CD	I		Y					
SD_WP	I		Y					
SD_RW	O		Y					
SD1_DATA[3:0]	I/O		Y					
SD1_CMD	I/O		Y					
SD1_CLK	O			Y				
SD1_CD	I		Y					
SD1_WP	I		Y					
SD1_RW	O		Y					
PD[7:0]	I/O	12mA	--	--	--	Y	S	
SLCT	I	--	Y	--	Y	Y	--	
PE	I	--	Y	--	Y	Y	--	
BUST	I	--	Y	--	Y	Y	--	
ACK#	I	--	Y	--	Y	Y	--	
SLIN#	OD	12mA	--	--	--	--	S	
INIT#	OD	12mA	--	--	--	--	S	
ERR#	I	--	Y	--	Y	Y	--	
AFD#	OD	12mA	--	--	--	--	S	
STB#	OD	12mA	--	--	--	--	S	
LINK/ACTIVE	O	8mA	--	--	--	--	S	
DUPLEX	O	8mA	--	--	--	--	S	
ISET	I	--	--	--	--	--	--	Note6
ATSTP	I/O	--	--	--	--	--	--	Note7
ATSTN	I/O	--	--	--	--	--	--	Note7
TXN	I/O	--	--	--	--	--	--	
TXP	I/O	--	--	--	--	--	--	
RXN	I/O	--	--	--	--	--	--	
RXP	I/O	--	--	--	--	--	--	
MDC	O	6mA	--	Y	--	--	--	
MDIO	I/O	6mA	Y	--	--	--	--	
COL	I	--	--	--	Y	--	--	
RXC	I	--	--	--	Y	--	--	
RXD[3:0]	I	--	--	--	Y	--	--	
RXDV	I	--	--	--	Y	--	--	
TXC	I	--	--	--	Y	--	--	

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
TXD[3:0]	I/O	6mA	--	--	--	--	--	
TXEN	O	6mA	--	--	--	--	--	
UD_DP	I/O	Note8	--	--	Note8	Y	Note8	
UD_DM	I/O	Note8	--	--	Note8	Y	Note8	
TDO	O	8mA	--	--	Y	N	S	
TMS	I	8mA	Y	--	Y	N	S	
TCK	I	8mA	Y	--	Y	N	S	
TDI	I	8mA	Y	--	Y	N	S	
H_BCLK	O	8mA	--	--	--	--	S	
H_SYNC	O	8mA	--	--	--	--	S	
H_SDO	O	8mA	--	--	--	--	S	
H_SDI	I/O	8mA	--	Y	Y	N	S	
H_RST#	O	8mA	--	--	--	--	S	
G_FPD[23:0]	IO	--	--	--	--	N	FIX	
G_FP1DE	O	--	--	--	--	N	FIX	
G_FP1HS	O	--	--	--	--	N	FIX	
G_FP1VS	O	--	--	--	--	N	FIX	
G_FP1CLK	O	--	--	--	--	N	FIX	
G_TVCLKIN	I	--	--	--	--	N	--	
G_FP1DET	I	--	--	--	--	N	FIX	
G_ENVDD	O	--	--	--	--	N	FIX	
G_ENBLT	O	--	--	--	--	N	FIX	
G_ENVEE	O	--	--	--	--	N	FIX	
G_REXT	I	--	--	--	--	N	--	DAC signal
G_IOR	O	--	--	--	--	N	--	DAC signal
G_IOG	O	--	--	--	--	N	--	DAC signal
G_IOB	O	--	--	--	--	N	--	DAC signal
G_VSYNC	O	8mA	--	--	--	N	--	
G_HSYNC	O	8mA	--	--	--	N	--	
G_GPIO[3:2]	I/O	8mA	--	--	--	N	--	
G_DDC1_CLK	I/OD	8mA	--	--	--	N	--	
G_DDC1_DAT	I/OD	8mA	--	--	--	N	--	
G_DDC_CLK	I/OD	8mA	--	--	--	N	--	
G_DDC_DAT	I/OD	8mA	--	--	--	N	--	

Definition:
--: Not need to specify
Y: Yes
N: No
F: Fast
S: Slow
The pull-up/pull-down resistance is 75KΩ

Note1: Enable pull-up by setting GPIO pin as input mode. Otherwise, no need to pull up.
Note2: A PCI type IO pad
Note3: This pin can be programmed through IDE Driving Current Register (2~12mA)
Note4: Programmable, default is pull-up.
Note5: USB analog IO pad
Note6: BIAS external resistor connecting pin

Note7: VGA and ADC test pin
Note8: Programmable by USB device config register 40h.
Note9: Programmable through South config register 48h.
Note10: Programmable through South config register 44h.
Note11: Programmable through South config register 48h & North config register 44h
Note12: Programmable by North Function 0 config register 44h
Note13: define by North config2 FCh
Note14: define by North config2 F8h
Note15 define by VGA register 3X5.50[1:0], 3X5.51,3X5.52,3X5.53.
Note16 define by VGA register 3X5.4F[1:0].

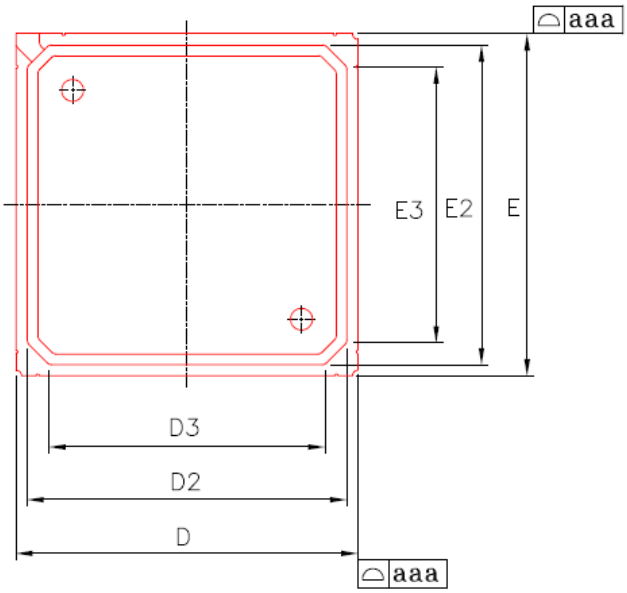
4.7. The Registers only reset by power-good

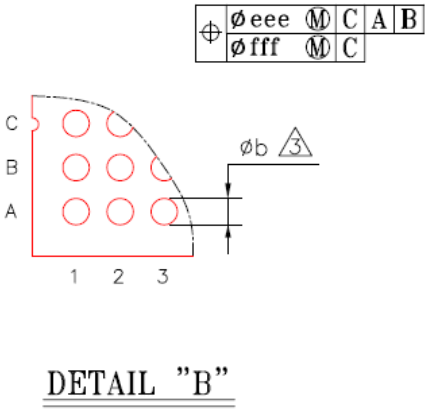
These registers are only reset by PowerGood

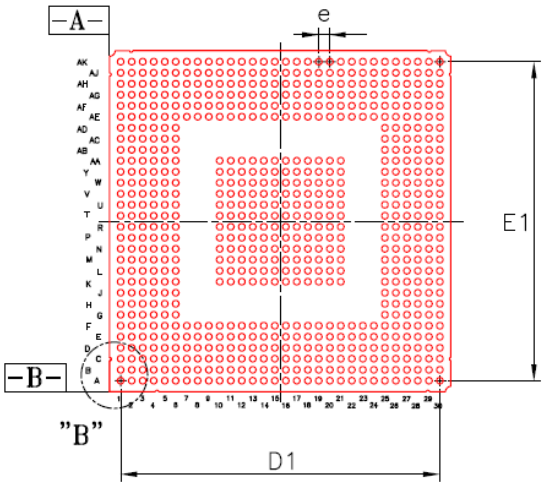
1. GPIO_0~4 Direction register
2. GPIO_0~4 Data register
3. South Configuration Register 60h~63h
4. South Configuration Register 64h~67h
5. South Configuration Register 68h~6Bh
6. South Configuration Register 6Ch
7. WatchDog Timer_0 3Ch Indirect access register
8. WatchDog Timer_1 6Dh register

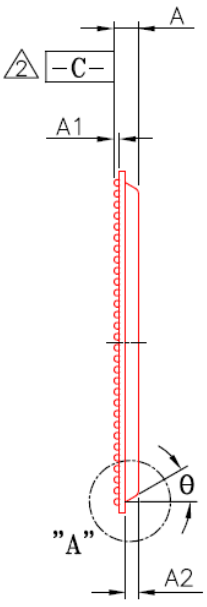
20. Package Information

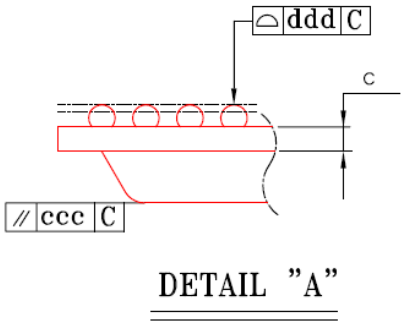
720LD PBGA (31 x 31mm)











Symbol	dimension in mm			dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	2.23	2.43	---	0.088	0.096
A1	0.40	0.50	0.60	0.016	0.020	0.024
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	0.50	0.60	0.70	0.020	0.024	0.028
c	0.51	0.56	0.61	0.020	0.022	0.024
D	30.80	31.00	31.20	1.213	1.220	1.228
D1	---	29.00	---	---	1.142	---
D2	28.80	29.00	29.20	1.134	1.142	1.150
D3	---	25.00	---	---	0.984	---
E	30.80	31.00	31.20	1.213	1.220	1.228
E1	---	29.00	---	---	1.142	---
E2	28.80	29.00	29.20	1.134	1.142	1.150
E3	---	25.00	---	---	0.984	---
e	---	1.00	---	---	0.039	---
aaa	0.20			0.008		
ccc	0.25			0.010		
ddd	0.15			0.006		
eee	0.25			0.010		
fff	0.10			0.004		
θ	30° TYP			30° TYP		