1. Overview

The **Vortex86EX** is a low-power, good performance and fully static 32-bit X86 processor with the compatibility of Windows based, Linux and most popular 32-bit RTOS. It also integrates 16KB write through 4-way L1 cache, 128KB write through/write back 4-way L2 cache, PCIE bus in at 2.5 GHz, DDR3, CrossBar Interface, ROM controller, ISA, I2C, SPI, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), Fast Ethernet, FIFO UART, USB2.0 Host, USB Device, PCIe Device, SD/SATA and CAN controller within a single 288-pin LBGA package to form a system-on-a-chip **(SOC)**. It provides an ideal solution for the low-cost and power-effeicency embedded system to bring about desired performance.

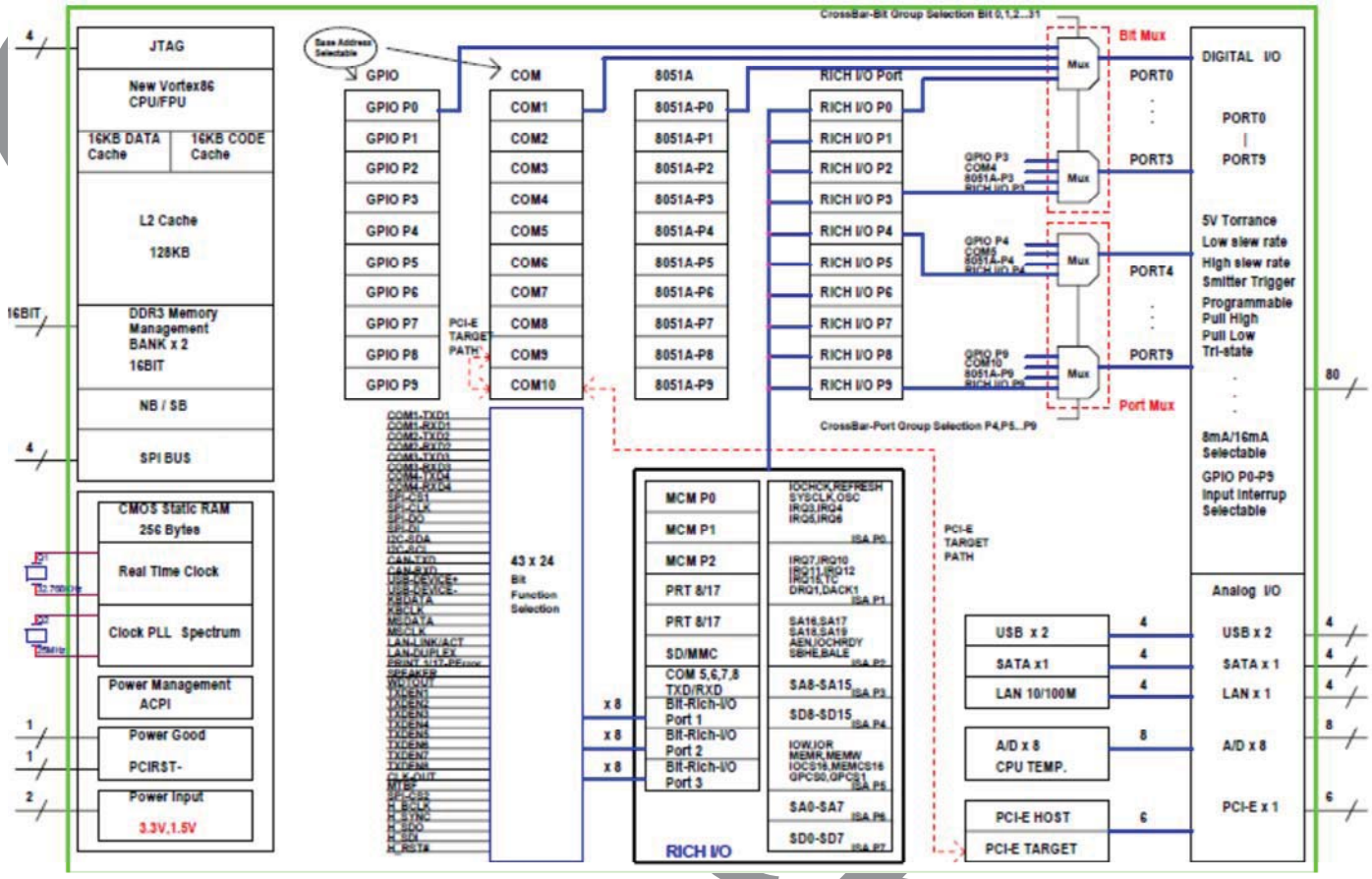
2. Features

- **X86 Processor Core**
  - 6-stage pipeline
- **Floating point unit support**
  - Extends CPU instruction set to include Trigonometric, Logarithmic and Exponential
  - Implements ANSI/IEEE standard 754-1985 for binary Floating-Point Architecture
- **Branch prediction unit**
  - Branch target buffer
- **Translation Lookaside buffer**
  - 32 I/D translation lookaside buffer
- **Embedded I / D Separated L1 Cache**
  - 16K I-Cache, 16K D-Cache
- **Embedded L2 Cache**
  - 4-way 128KB L2 Cache
  - Write through or write back policy
- **DDRIII Control Interface**
  - 16 bits data bus
  - 2 rank
  - DDRIII clock support up to 300MHz
  - DRAM size maximum support up to 2GB
- **CrossBar Interface**
  - 10 CrossBar port for digital function select. (each port is 8 pins, total 80 pins)
  - CrossBar Port0-3 support CrossBar-Bit group selection
  - CrossBar Port4-9 support CrossBar-Port group selection
- **SD Interface**
  - SD x 1 at IDE Primary Channel
- **SATA Interface**
  - SATA 1.5G (1 Port) at IDE Secondary Channel
- **Ethernet MAC Controller + PHY**
- **PCIE Control Interface**
  - Up to 1 set PCIE device
- **PCIE Target Interface**
- **USB 2.0 Host Support**
  - Supports HS, FS and LS
  - 2 ports
- **USB 1.1 Device Support**
  - 1 port
  - Supports FS with 3 programmable endpoint
- **HDA Controller**
  - 1 input stream, 1 output stream
- **ADC Interface x 8**
- **I^2C bus**
  - Compliant w/t V2.1
  - Some master code (general call, START and CBUS) not support.
- **SPI Boot Interface**
  - For boot up function from SPI flash
  - Half duplex
  - Support SPI Flash Size up to 128MB
- **Full Duplex SPI Controller**
  - Some master code (general call, START and CBUS) not support.
  - Support SPI Device x2 (Chip Select x2)

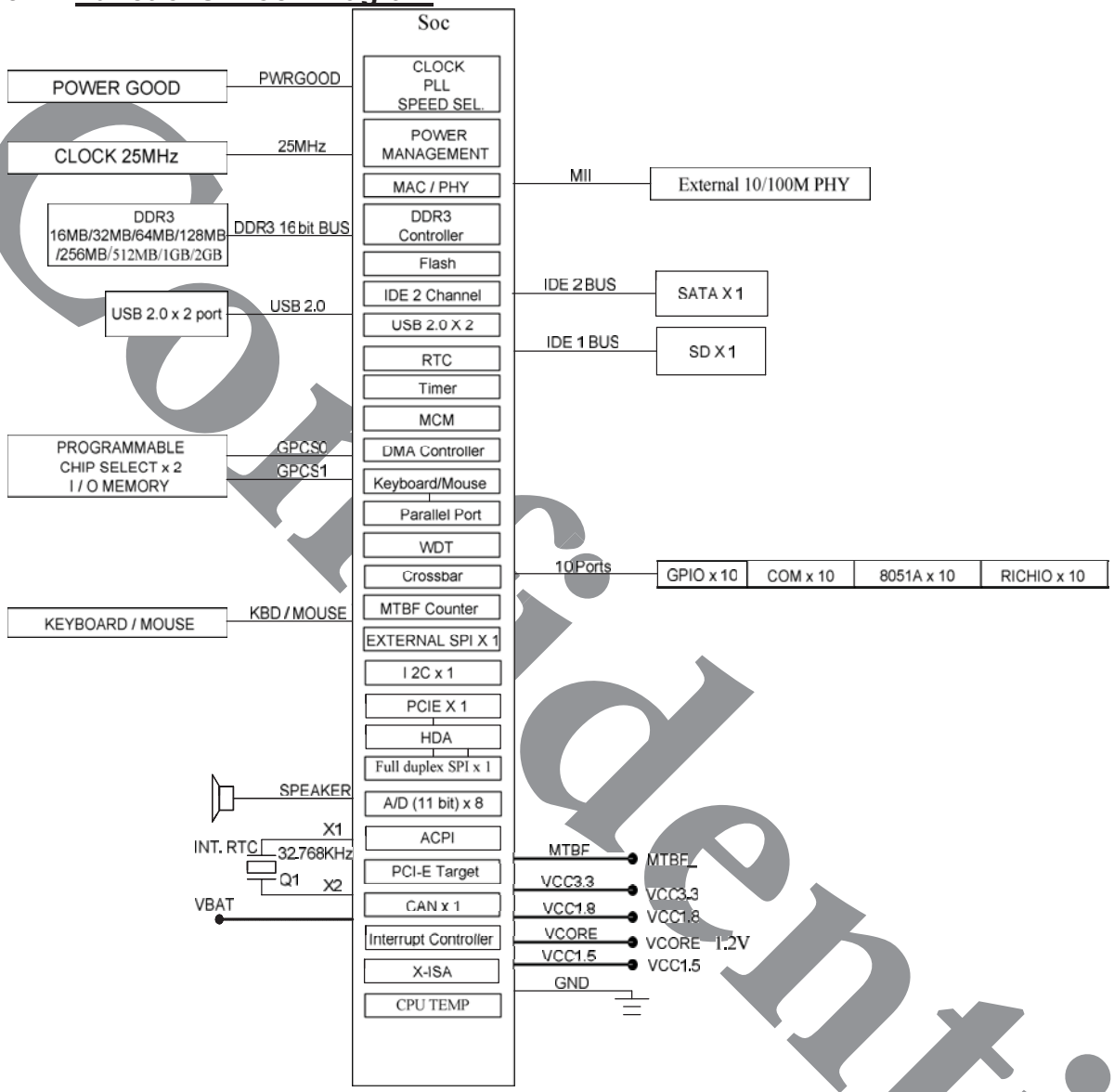
- **CAN Bus Controller**
  - Compatible with the CAN2.0A/2.0B
  - Support 1 CAN Bus channel
- **Motor Control Interface Support**
  - 1groups of controller, 4 controllers per group
  - Each controller can configure to PWM/Servo/Sensor Interface mode
  - Controller interconnect to the other with routing network in the same group
- **X-ISA Bus Interface**
  - Subset ISA Bus (remove some ISA Bus pins)
  - AT clock programmable
  - 8/16 Bit ISA device with Zero-Wait-State
  - Generate refresh signals to ISA interface during DRAM refresh cycle
  - Support Max ISA Clock 33M
  - Support 1 channel ISA DMA
  - Support ISA IRQ x 9
- **DMA Controller**
- **Interrupt Controller**
- **MTBF Counter**
- **Counter / Timers**
  - 1 sets of 8254 timer controller
- **Real Time Clock**
  - Less than 2.5uA (3.0V) power consumption in Internal RTC Mode while chip is power-off.
- **FIFO UART Port x 10 (10 sets COM Port)**
  - Compatible with 16C550 / 16C552
  - Default internal pull-up
  - Supports the programmable baud rate generator with the data rate from 50 to 6M bps
  - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
  - Support TXD_En Signal on COM1-8
  - Port 80h output data could be sent to COM1 by software programming
  - Support half-duplex mode
  - Enhanced low IO access latency
- **Parallel Port**
  - Supports SPP/EPP/ECP mode
- **General Programmable I/O**
  - Supports 80 programmable I / O pins
  - Each GPIO pin can be individually configured to be an input/output pin
  - GPIO_P0~GPIO_P9 can be program by 8051A
  - All GPIO port with interrupt support (input/output)
- **PS / 2 Keyboard and Mouse Interface Support**
  - Compatible with 8042 controller
- **Speaker out**
- **JTAG Interface supported for S.W. debugging**
- **Input clock**
  - 25 MHz
  - 32.768 KHz
- **Output clock**
  - one clock output select from 14.318MHz /24MHz /25MHz/ ISA Clock
- **Operating Voltage Range**
  - Core voltage: 1.2 V ± 5%
  - I / O voltage: 1.5V ± 5%, 1.8V ± 5 %, 3.3 V ± 10 %
- **Operating temperature**
  - -40℃ ~ 85℃
- **Package Type**
  - 16x16mm TFBGA-288

3. Block Diagram

3.1. System Block Diagram



3.2. Functions Block Diagram



3.3. PCI Device List

ID SEL	AD11	AD12	AD13 - AD17	AD18	AD19	AD20	AD21	AD22	AD23	AD24	AD25	AD26	AD27	AD28
Device#	0	1	2 – 6	7	8	9	10	11	12	13	14	15	16	17
Function	NB	PCIE0		SB	MAC		USB 2.0 HOST		IDE		HDA	USB Device	MC & SPI	CAN
Fun0	NB0			SB0			OHCI						MC	
Fun1	NB1			SB1			EHCI						SPI	

PS. 1. USB 2.0 Host Controller supports 2 port

2 PCIE0, Interrupt Routing: INTA, INTB, INTC, INTD

4. PIN Function List

4.1. BGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	AVDD_USB12	AVSS_USBPLL12	PCIRST#	ISA_RST	PORT9[7]	PORT9[6]	PORT9[5]	PORT0[3]	PORT7[2]	PORT7[3]	PORT7[0]	PORT6[2]	PORT6[1]	PORT5[3]	PORT5[1]	PORT4[7]	PORT4[5]	PORT4[3]	VSS
B	USB2_DP	USB2_DM	AVSS_USBBAS33	USB2_EXT12K	POWER_GOOD	PORT9[3]	PORT9[1]	PORT0[2]	PORT7[4]	PORT7[5]	PORT7[1]	PORT6[4]	PORT6[0]	PORT5[2]	VSS	PORT4[6]	VDD33	PORT4[2]	PORT3[3]
C	AVDD_USB33	AVSS_USB33	AVDD_USBBAS33	USB1_EXT12K	PORT9[4]	PORT9[0]	VSS	PORT0[0]	PORT0[4]	VDD33	PORT6[7]	PORT6[5]	PORT5[6]	VDD33	PORT4[4]	PORT3[7]	PORT3[6]	VSS	PORT3[1]
D	USB1_DP	USB1_DM	AVDD_USBPLL12	VDD18_1	PCIE_MSEL	PORT9[2]	PORT0[1]	PORT0[6]	PORT7[7]	PORT7[6]	PORT6[6]	PORT5[7]	PORT5[4]	PORT5[0]	PORT4[0]	PORT3[5]	PORT3[4]	PORT3[2]	PORT3[0]
E	ADC_IN4	ADC_IN1	NC_Ball	SPI_CK	TCK_0	TDO_0	TDI_0	PORT0[7]	PORT0[5]	VSS	PORT6[3]	PORT5[5]	VSS	PORT4[1]	PORT2[6]	PORT2[5]	VDD33	PORT2[3]	PORT2[1]
F	ADC_IN5	ADC_IN2	ADC_IN0	SPI_CS	VSS										PORT2[7]	PORT2[4]	PORT2[2]	VSS	PORT2[0]
G	ADC_IN7	ADC_IN6	ADC_IN3	TMS_0	SPI_DO										VSS	PORT1[7]	PORT1[5]	PORT1[4]	PORT1[3]
H	RTC_CLK	RTC_XO	RTC_VSS	RTC_VDE	SPI_DI										PORT1[6]	PORT1[2]	VDD33	PORT1[1]	PORT1[0]

	P	N	M	L	K	J
1	PCIE1_RXIP	PCIE1_REFCLKN	AVSS_SATA	SATA_TXOP	SATA_RXIP	SATA_REFCLKP
2	PCIE1_RXIN	PCIE1_REFCLKP	AVDD_SATA12	SATA_TXON	SATA_RXIN	SATA_REFCLKN
3	REG_VCTRL18	AVSS_PERX12	AVDD_PERX12	AVSS_SATARX12	AVDD_SATARX12	AVDD_ADC33
4	AVSS_EPHYBG18	AVSS_PEPLL12	AVDD_PEPLL12	AVSS_SATAPLL12	AVDD_SATAPLL12	AVSS_ADC33
5	VDD12	AVDD_PE33	AVDD_TEMP18	AVDD_SATA33	AVSS_TEMP18	RTC_NMR
6						
7						
8						
9				VDD12	VSS	VDD12
10				VDD12		VDD12
11				VDD12	VSS	VDD12
12						
13						
14						
15	MA13	MA1	VSS	PORT8[0]	VSS	PORT8[6]
16	MA12	MA14	VDD15	MA6	PORT8[1]	PORT8[5]
17	MA11	MA4	MA8	RST	PORT8[2]	PORT8[7]
18	WE	BA1	VSS	BA0	VSS	PORT8[4]
19	MA15	BA2	VDD15	MA0	VDD33	PORT8[3]

W	V	U	T	R	
EPHY_TXN	EPHY_TXP	AVSS_EPHYTX18	AVSS_PE	PCIE1_TXOP	1
EPHY_RXN	EPHY_RXP	REG_AVSS33	AVDD_PE12	PCIE1_TXON	2
AVDD_EPHYPLL18	AVSS_EPHYPLL18	REG_AVDD33	REG_FB12	REG_FB18	3
XIN	XOUT	REG_VCTRL12	AVDD_EPHYBG18	EPHY_ISET	4
SATA_PHY_CLK_P	SATA_PHY_CLK_N	VSS	VDD18	VDD33_1	5
PLLCK100_0_P	PLLCK100_0_N	DIF_VDD18	AVDD_SBPLL18	VSS	6
PLLCK100_1_P	PLLCK100_1_N	DIF_VSS18	AVSS_SBPLL18	VDD12	7
DIF_VDD12	DIF_VSS12	AVDD_NBPLL18	AVSS_NBPLL18	VREF	8
VDD15	VSS	VDD15	ZQ0	VSS	9
DQ08	DQ10	DQ11	VSS	DQ00	10
DQ09	DQS1P	DQ01	DQ02	DQ03	11
DQS1N	VSS	DQS0P	VSS	VDD15	12
VDD15	DM1	DQS0N	DM0	TEST_ODT1	13
DQ12	VSS	DQ04	DQ06	CS1	14
DQ13	DQ15	DQ05	DQ07	VSS	15
SDRAMCLK0N	DQ14	MA3	MA5	VDD15	16
SDRAMCLK0P	VSS	MA2	MA9	MA7	17
TEST_ODT0	RAS	VSS	CAS	VSS	18
VSS	CS0	CKE0	MA10	VDD15	19

4.2. PIN Out Table

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
A1	AVDD_USB12	D16	PORT3[5]	K11	VSS	T5	VDD18
A2	AVSS_USBPLL12	D17	PORT3[4]	K15	VSS	T6	AVDD_SBPLL18
A3	PCIRST#	D18	PORT3[2]	K16	PORT8[1]	T7	AVSS_SBPLL18
A4	ISA_RST	D19	PORT3[0]	K17	PORT8[2]	T8	AVSS_NBPLL18
A5	PORT9[7]	E1	ADC_IN4	K18	VSS	T9	ZQ0
A6	PORT9[6]	E2	ADC_IN1	K19	VDD33	T10	VSS
A7	PORT9[5]	E3	NC_Ball	L1	SATA_TXOP	T11	DQ02
A8	PORT0[3]	E4	SPI_CK	L2	SATA_TXON	T12	VSS
A9	PORT7[2]	E5	TCK_0	L3	AVSS_SATARX12	T13	DM0
A10	PORT7[3]	E6	TDO_0	L4	AVSS_SATAPLL12	T14	DQ06
A11	PORT7[0]	E7	TDI_0	L5	AVDD_SATA33	T15	DQ07
A12	PORT6[2]	E8	PORT0[7]	L9	VDD12	T16	MA5
A13	PORT6[1]	E9	PORT0[5]	L10	VDD12	T17	MA9
A14	PORT5[3]	E10	VSS	L11	VDD12	T18	CAS
A15	PORT5[1]	E11	PORT6[3]	L15	PORT8[0]	T19	MA10
A16	PORT4[7]	E12	PORT5[5]	L16	MA6	U1	AVSS_EPHYTX18
A17	PORT4[5]	E13	VSS	L17	RST	U2	REG_AVSS33
A18	PORT4[3]	E14	PORT4[1]	L18	BA0	U3	REG_AVDD33
A19	VSS	E15	PORT2[6]	L19	MA0	U4	REG_VCTRL12
B1	USB2_DP	E16	PORT2[5]	M1	AVSS_SATA	U5	VSS
B2	USB2_DM	E17	VDD33	M2	AVDD_SATA12	U6	DIF_VDD18
B3	AVSS_USBBAS33	E18	PORT2[3]	M3	AVDD_PERX12	U7	DIF_VSS18
B4	USB2_EXT12K	E19	PORT2[1]	M4	AVDD_PEPLL12	U8	AVDD_NBPLL18
B5	POWER_GOOD	F1	ADC_IN5	M5	AVDD_TEMP18	U9	VDD15
B6	PORT9[3]	F2	ADC_IN2	M15	VSS	U10	DQ11
B7	PORT9[1]	F3	ADC_IN0	M16	VDD15	U11	DQ01
B8	PORT0[2]	F4	SPI_CS	M17	MA8	U12	DQS0P

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
B9	PORT7[4]	F5	VSS	M18	VSS	U13	DQS0N
B10	PORT7[5]	F15	PORT2[7]	M19	VDD15	U14	DQ04
B11	PORT7[1]	F16	PORT2[4]	N1	PCIE1_REFCLKN	U15	DQ05
B12	PORT6[4]	F17	PORT2[2]	N2	PCIE1_REFCLKP	U16	MA3
B13	PORT6[0]	F18	VSS	N3	AVSS_PERX12	U17	MA2
B14	PORT5[2]	F19	PORT2[0]	N4	AVSS_PEPLL12	U18	VSS
B15	VSS	G1	ADC_IN7	N5	AVDD_PE33	U19	CKE0
B16	PORT4[6]	G2	ADC_IN6	N15	MA1	V1	EPHY_TXP
B17	VDD33	G3	ADC_IN3	N16	MA14	V2	EPHY_RXP
B18	PORT4[2]	G4	TMS_0	N17	MA4	V3	AVSS_EPHYPLL18
B19	PORT3[3]	G5	SPI_DO	N18	BA1	V4	XOUT
C1	AVDD_USB33	G15	VSS	N19	BA2	V5	SATA_PHY_CLK_N
C2	AVSS_USB33	G16	PORT1[7]	P1	PCIE1_RXIP	V6	PLLCK100_0_N
C3	AVDD_USBBAS33	G17	PORT1[5]	P2	PCIE1_RXIN	V7	PLLCK100_1_N
C4	USB1_EXT12K	G18	PORT1[4]	P3	REG_VCTRL18	V8	DIF_VSS12
C5	PORT9[4]	G19	PORT1[3]	P4	AVSS_EPHYBG18	V9	VSS
C6	PORT9[0]	H1	RTC_CLK	P5	VDD12	V10	DQ10
C7	VSS	H2	RTC_XO	P15	MA13	V11	DQS1P
C8	PORT0[0]	H3	RTC_VSS	P16	MA12	V12	VSS
C9	PORT0[4]	H4	RTC_VDE	P17	MA11	V13	DM1
C10	VDD33	H5	SPI_DI	P18	WE	V14	VSS
C11	PORT6[7]	H15	PORT1[6]	P19	MA15	V15	DQ15
C12	PORT6[5]	H16	PORT1[2]	R1	PCIE1_TXOP	V16	DQ14
C13	PORT5[6]	H17	VDD33	R2	PCIE1_TXON	V17	VSS
C14	VDD33	H18	PORT1[1]	R3	REG_FB18	V18	RAS
C15	PORT4[4]	H19	PORT1[0]	R4	EPHY_ISET	V19	CS0
C16	PORT3[7]	J1	SATA_REFCLKP	R5	VDD33_1	W1	EPHY_TXN
C17	PORT3[6]	J2	SATA_REFCLKN	R6	VSS	W2	EPHY_RXN
C18	VSS	J3	AVDD_ADC33	R7	VDD12	W3	AVDD_EPHYPLL18

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
C19	PORT3[1]	J4	AVSS_ADC33	R8	VREF	W4	XIN
D1	USB1_DP	J5	RTC_NMR	R9	VSS	W5	SATA_PHY_CLK_P
D2	USB1_DM	J9	VDD12	R10	DQ00	W6	PLLCK100_0_P
D3	AVDD_USBPLL12	J10	VDD12	R11	DQ03	W7	PLLCK100_1_P
D4	VDD18_1	J11	VDD12	R12	VDD15	W8	DIF_VDD12
D5	PCIE_MSEL	J15	PORT8[6]	R13	TEST_ODT1	W9	VDD15
D6	PORT9[2]	J16	PORT8[5]	R14	CS1	W10	DQ08
D7	PORT0[1]	J17	PORT8[7]	R15	VSS	W11	DQ09
D8	PORT0[6]	J18	PORT8[4]	R16	VDD15	W12	DQS1N
D9	PORT7[7]	J19	PORT8[3]	R17	MA7	W13	VDD15
D10	PORT7[6]	K1	SATA_RXIP	R18	VSS	W14	DQ12
D11	PORT6[6]	K2	SATA_RXIN	R19	VDD15	W15	DQ13
D12	PORT5[7]	K3	AVDD_SATARX12	T1	AVSS_PE	W16	SDRAMCLK0N
D13	PORT5[4]	K4	AVDD_SATAPLL12	T2	AVDD_PE12	W17	SDRAMCLK0P
D14	PORT5[0]	K5	AVSS_TEMP18	T3	REG_FB12	W18	TEST_ODT0
D15	PORT4[0]	K9	VSS	T4	AVDD_EPHYBG18	W19	VSS

4.3. Pin List Table

Function	Symbol	PIN Sum
SYSTEM	PWRGOOD, XOUT_25, XIN_25, PCIRST#, STRAP_PE_HTS	5 PINs
DDRIII Interface	DRAMRST#, DRAMCLK, DRAMCLK#, RAS#, CAS#, WE#, CKE, CS1#, CS0#, DQM[1:0], DQS[1:0], DQS#[1:0], ODT[1], ODT[0], BA[2:0],MD[15:0], MA[15:0], ZQ, VREF	54 PINs
CrossBar Interface	CBAR_P0[7:0], CBAR_P1[7:0], CBAR_P2[7:0], CBAR_P3[7:0], CBAR_P4[7:0], CBAR_P5[7:0], CBAR_P6[7:0], CBAR_P7[7:0], CBAR_P8[7:0], CBAR_P9[7:0], CBAR_DEVRST	81 PINs
USB Interface	USB_DP,USB_DM, USB1_DP, USB1_DM, USB_REXT, USB_REXT1	6 PINs
PCIE Bus Interface	PE0_CLKP, PE0_CLKN, PE0_TXP, PE0_TXN, PE0_RXP, PE0_RXN, , DIF0_PCIE_PLLCLK100_P, DIF0_PCIE_PLLCLK100_N, DIF1_CLK100_P, DIF1_CLK100_N	10 PINs
SATA Interface	SATA_CLKP, SATA_CLKN, SATA_TXP, SATA_TXN, SATA_RXP, SATA_RXN, DIF1_SATA_PHY_CLK_P, DIF1_SATA_PHY_CLK_N	8 PINs
Ethernet Interface	ISET, TXN, TXP, RXN, RXP	5 PINs
SPI Interface	SPI_CS#/ STRAP_BMS, SPI_CK/STRAP_JTAG, SPI_DO/STRAP_HDM, SPI_DI	4 PINs

Function	Symbol	PIN Sum
RTC Interface	RTC_PS, RTC_XOUT, RTC_XI	3 PINs
JTAG Interface	TDO, TMS, TCK, TDI	4 PINs
ADC Interface	ADC_IN0, ADC_IN1, ADC_IN2, ADC_IN3, ADC_IN4, ADC_IN5, ADC_IN6, ADC_IN7,	8 PINs
Embedded Regulator	REG_AVDD33, REG_AVSS33, REG_VCTRL18, REG_FB18, REG_VCTRL12, REG_FB12	6 PINs
USB Power Interface	AVDD_USB33, AVSS_USB33, AVDD_USB12, AVDD_USBBAS33, AVSS_USBBAS33, AVDD_USBPLL12, AVSS_USBPLL12	7 PINs
PCIE Power Interface	AVDD_PE33, AVDD_PE12, AVSS_PE, AVDD_PEPLL12, AVSS_PEPLL12, AVDD_PERX12, AVSS_PERX12	7 PINs
SATA Power Interface	AVDD_SATA33, AVDD_SATA12, AVSS_SATA, AVDD_SATAPLL12, AVSS_SATAPLL12, AVDD_SATARX12, AVSS_SATARX12	7 PINs
Ethernet Power	AVDD_EPHYPLL18, AVSS_EPHYPLL18, AVDD_EPHYBG18, AVSS_EPHYBG18, AVSS_EPHYTX18	5 PINs
ADC Power	AVDD_ADC33, AVSS_ADC33, AVDD_TEMP18, AVSS_TEMP18	4 PINs
System PLL Power	AVDD_NBPLL18, AVSS_NBPLL18, AVDD_SBPLL18, AVSS_SBPLL18	4 PINs
Battery Power	RTC_VDD33, RTC_VSS	2 PINs
Differential PAD Power	DIF_VDD18, DIF_VSS18, DIF_VDD12, DIF_VSS12	4 PINs
NC	NC	1 PIN
1.2V Power	VDD12 (8 PINs)	8 PINs
1.5 Power	VDD15 (8 PINs)	8 PINs
1.8V Power	VDD18 (2 PINs)	2 PINs
3.3V Power	VDD33(7 PINs)	7 PINs
Digital Ground	VSS (28 PINs)	28 PINs

4.4. Signal Description

This chapter provides a detailed description of SoC signals. A signal with the symbol "#" at the end of itself indicates that this pin is low active. Otherwise, it is high active.

The following notations are used to describe the signal types:

I Input pin
O Output pin
OD Output pin with open-drain
I/O Bi-directional Input/Output pin

¿ **System (5 PINs)**

PIN No.	Symbol	Type	Description
B5	PWRGOOD	I	***Power-Good Input.*** This signal comes from Power Good of the power supply to indicate that the power is available. The SoC uses this signal to generate reset sequence for the system.
V4	XOUT_25	O	***Crystal-out.*** Frequency output from the inverting amplifier (oscillator).
W4	XIN_25	I	***Crystal-in.*** 25MHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).
A3	PCIRST#	O	***PCI Reset.*** This pin is used to reset PCI devices. When it is asserted low, all the PCI devices will be reset.
D5	STRAP_PE_HTS	I	***PCIe Host / Target Select. Strap pin for PCIe Interface is selected to Host or Target mode.*** ***Pull low ot PCIe Target.*** ***Pull high to PCIe Host. (default internal pull-high)***

¿ **DDRIII Interface (54 PINs)**

PIN No.	Symbol	Type	Description
L17	DRAMRST#	O	***Active Low Asynchronous Reset.*** Reset is active when RESET# is LOW, and otherwise. RESET# must be set as HIGH during normal operation.
W17 W16	DRAMCLK DRAMCLK1	O	***Clock output.*** This pin provides the fundamental timing for the DDRII controller.
V18	RAS#	O	***Row Address Strobe.*** When asserted, this signal latches row address on positive edge of the DDRII clock. This signal also allows row access and pre-charge.
T18	CAS#	O	***Column Address Strobe.*** When asserted, this signal latches column address on the positive edge of the DDRII clock. This signal also allows column access and pre-charge.
P18	WE#	O	***Memory Write Enable.*** This pin is used as a write enable for the memory data bus.

PIN No.	Symbol	Type	Description
U19	CKE	O	***Clock Enable.*** CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers.
R14 V19	CS1# CS0#	O	***Chip Select CS1# & CS0#.*** These two pins activate the DDRIII devices. First Bank of DDRIII accepts any command when the CS0# pin is active low. Second Bank of DDRIII accepts any command when the CS1# pin is active low.
V13, T13	DQM[1:0]	O	***Data Mask DQM[1:0].*** These pins act as synchronized output enables during read cycles and byte masks during write cycles.
V11, U12	DQS[1:0]	I/O	***Data Strobe DQS[1:0] for DDRIII only.*** Output with write data, input with the read data for source synchronous operation.
W12, U13	DQS#[1:0]	I/O	***Data Strobe DQS#[1:0] for DDRIII only.*** Output with write data, input with the read data for source synchronous operation.
W18	ODT[0]	O	***On Die Termination Control for DDRII only.*** ODT(registered HIGH) enables on die termination resistance internal to the DDR3 SDRAM.
R13	ODT[1]	O	***On Die Termination Control for DDRII only.*** ODT(registered HIGH) enables on die termination resistance internal to the DDR3 SDRAM.
T9	ZQ	O	***Reference Voltage for DDRIII only***. Reference Pin for ZQ calibration
R8	VREF	I	***Reference voltage for DDRIII only.*** Reference voltage for inputs for SSTL interface.
N19, N18, L18	BA[2:0]	O	***Bank Address BA[2:0].*** These pins are connected to DDRIII as bank address pins.
V15, V16, W15, W14, U10, V10, W11, W10, T15, T14, U15, U14, R11, T11, U11, R10	MD[15:0]	I/O	***Memory Data MD[15:0].*** These pins are connected to the DDRIII data bus.
P19, N16, P15, P16, P17, T19, T17, M17, R17, L16, T16, N17, U16, U17, N15, L19	MA[15:0]	O	***Memory Address MA[15-0].*** Normally, these pins are used as the row and column address for DDRIII.

¿ **CrossBar Interface (81 PINs)**

PIN No.	Symbol	Type	Description
E8, D8, E9, C9, A8, B8, D7, C8	CBAR_P0[7:0]	I/O	***CrossBar Port 0[7:0].*** PIN function is select by CrossBar mechanism. This port support CrossBar-Bit select by group.

PIN No.	Symbol	Type	Description
G16, H15, G17, G18, G19, H16, H18, H19	CBAR_P1[7:0]	I/O	***CrossBar Port 1[7:0].*** PIN function is select by CrossBar mechanism. This port support CrossBar-Bit select by group.
F15, E15, E16, F16, E18, F17, E19, F19	CBAR_P2[7:0]	I/O	***CrossBar Port 2[7:0].*** PIN function is select by CrossBar mechanism. This port support CrossBar-Bit select by group.
C16, C17, D16, D17, B19, D18, C19, D19	CBAR_P3[7:0]	I/O	***CrossBar Port 3[7:0].*** PIN function is select by CrossBar mechanism. This port support CrossBar-Bit select by group.
A16, B16, A17, C15, A18, B18, E14, D15	CBAR_P4[7:0]	I/O	***CrossBar Port 4[7:0].*** PIN function is select by CrossBar mechanism. This port only support CrossBar-Port select by group.
D12, C13, E12, D13, A14, B14, A15, D14	CBAR_P5[7:0]	I/O	***CrossBar Port 5[7:0].*** PIN function is select by CrossBar mechanism. This port only support CrossBar-Port select by group.
C11, D11, C12, B12, E11, A12, A13, B13	CBAR_P6[7:0]	I/O	***CrossBar Port 6[7:0].*** PIN function is select by CrossBar mechanism. This port only support CrossBar-Port select by group.
D9, D10, B10, B9, A10, A9, B11, A11	CBAR_P7[7:0]	I/O	***CrossBar Port 7[7:0].*** PIN function is select by CrossBar mechanism. This port only support CrossBar-Port select by group.
J17, J15, J16, J18, J19, K17, K16, L15	CBAR_P8[7:0]	I/O	***CrossBar Port 8[7:0].*** PIN function is select by CrossBar mechanism. This port only support CrossBar-Port select by group.
A5, A6, A7, C5, B6, D6, B7, C6	CBAR_P9[7:0]	I/O	***CrossBar Port 9[7:0].*** PIN function is select by CrossBar mechanism. This port only support CrossBar-Port select by group.
A4	CBAR_DEVRST	O	***CrossBar Device Reset*** This reset signal is manual controled by software for device accessed in CrossBar.

¿ **USB Interface (6 PINs)**

PIN No.	Symbol	Type	Description
D1 D2	USB_DP USB_DM	I/O	Universal Serial Bus Controller 0 Port 0. These are the serial data pair for USB Port 0. 15kΩ pull down resistors are connected to DP and DM internally.
B1 B2	USB1_DP USB1_DM	I/O	Universal Serial Bus Controller 0 Port 1. These are the serial data pair for USB Port 1. 15kΩ pull down resistors are connected to DP and DM internally.
C4	USB_REXT	I	Universal Serial Bus Controller 0 External Reference Resistance 12kΩ ±1%

PIN No.	Symbol	Type	Description
B4	USB_REXT1	I	Universal Serial Bus Controller 1 External Reference Resistance 12kΩ ±1%

¿ **PCIE Bus Interface (10 PINs)**

PIN No.	Symbol	Type	Description
P1 P2	PE0_RXP PE0_RXN	I	PCI-E Differential serial data input. P: positive; N:negative
R1 R2	PE0_TXP PE0_TXN	O	PCI-E Differential serial data output. P: positive; N: negative
N2 N1	PE0_CLKP PE0_CLKN	I	PCI-E Differential reference clock. P: positive; N: negative
W6 V6	DIF0_PCIE_PLLCLK 100_P DIF0_PCIE_PLLCLK 100_N	O	PCI-E Differential Clock 100MHz from Internal PLL P: positive; N: negative
W7 V7	DIF1_CLK100_P DIF1_CLK100_N	O	PCI-E Differential Clock 100MHz to Port0 P: positive; N: negative

¿ **Serial ATA Interface (8 PINs)**

PIN No.	Symbol	Type	Description
L1 L2	SATA_TXP SATA_TXN	O	***Serial ATA Device Controller TX Port. These are the serial ATA Transmiter pair for Serial ATA Device.***
K1 K2	SATA _RXP SATA _RXN	I	***Serial ATA Device Controller RX Port. These are the serial ATA Reveive pair for Serial ATA Device.***
J1 J2	SATA_CLKP SATA_CLKN	I	***Differential PLL Reference Clock Pair.***
W5 V5	DIF1_SATA_PHY_C LK_P DIF1_SATA_PHY_C LK_N	O	***Differential Clock Pair from Internal PLL.***

¿ **Ethernet Interface (5 PINs)**

PIN No.	Symbol	Type	Description
R4	ISET	I	***ISET:*** External resistor 6.02kΩ ±1%connecting pin for BIAS.
W1	TXN	O	***TXN:*** 10B-T/100BT transmitting output pin/ reveiving input pin (positive)
V1	TXP	O	***TXP:*** 10B-T/100BT transmitting output pin/ reveiving input pin (negative)
W2	RXN	I	***RXN:*** 10B-T/100BT reveiving input pin/ transmitting output pin (positive)
V2	RXP	I	***RXP:*** 10B-T/100BT reveiving input pin/ transmitting output pin (negative)

¿ **SPI Interface (4 PINs)**

Ball No.	Symbol	Type	Description
F4	SPI_CS#	O	***SPI Chip Select***
	STRAP_BMS	I	***Boot Mode Select*** Pull it high to select Normal boot(Reset 250ms). Default internal pull-high. Pull it low to select Fast boot.
E4	SPI_CK	O	***SPI Clock***
	STRAP_ JTAG	I	***JTAG enable*** Pull it high to enable JTAG. (default internal pull-high)
G5	SPI_DO	O	***SPI Data Ouput / Output pin, connected with input of flash.***
	STRAP_HDM	I	***Flash Strap Hardware Default Mode.*** Pull it high to ignore flash strap data. Use hardware default safe setting. Pull it low to get flash strap data for hardware setting. (default internal pull-low)
H5	SPI_DI	I	***SPI Data Input / Input pin, connected with output of flash.***

¿ **RTC Interface (3 PINs)**

PIN No.	Symbol	Type	Description
J5	RTC_PS	I	***RTC Battery Power Sense.***
H2	RTC_XOUT	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator)
H1	RTC_XI	I	***Crystal-in.*** 32.768KHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).

¿ **ADC Interface (8 PINs)**

PIN No.	Symbol	Type	Description
G1, G2, F1, E1, G3, F2, E2,F3	ADC_IN[7:0]	I	***ADC Analog Input***

¿ **JTAG Interface (4 PINs)**

PIN No.	Symbol	Type	Description
E6	TDO	O	***TDO:*** JTAG Test Data Output pin.
G4	TMS	I	***TMS:*** JTAG Test Mode Select pin.
E5	TCK	I	***TCK:*** JTAG Test Clock Input pin.
E7	TDI	I	***TDI:*** JTAG Test Data Input pin.

¿ **Embedded Regulator (6 PINs)**

PIN No.	Symbol	Type	Description
U3	REG_AVDD33	I	***Analogue Power***: Embedded Regulator 3.3V PAD Power.
U2	REG_AVSS33	I	***Analogue Ground*** Embedded Regulator 3.3V PAD Ground

P3	REG_VCTRL18	O	***Voltage Control for 1.8 Regulator***
R3	REG_FB18	I	***Feedback from 1.8V Regulator***
U4	REG_VCTRL12	O	***Voltage Control for 1.2 Regulator***
T3	REG_FB12	I	***Feedback from 1.2V Regulator***

¿ **USB Power (7 PINs)**

PIN No.	Symbol	Type	Description
C1	AVDD_USB33	I	***Analogue Power***: USB 3.3V Power
C2	AVSS_USB33	I	***Analogue Ground***: USB 3.3V Ground
A1	AVDD_USB12	I	***Analogue Power***: USB 1.2V Power
C3	AVDD_USBBAS33	I	***Analogue Power***: USB Base Voltage 3.3V Power
B3	AVSS_USBBAS33	I	***Analogue Ground***: USB Base Voltage 3.3V Ground
D3	AVDD_USBPLL12	I	***Analogue Power***: USB PLL Power
A2	AVSS_USBPLL12	I	***Analogue Ground***: USB PLL Ground

¿ **PCIE Power (7 PINs)**

PIN No.	Symbol	Type	Description
N5	AVDD_PE33	I	***Analogue Power*** PCIE 3.3V Power
T2	AVDD_PE12	I	***Analogue Power*** PCIE 1.2V Power
T1	AVSS_PE	I	***Analogue Ground*** PCIE Analogue Ground
M3	AVDD_PERX12	I	***Analogue Power*** PCIE Receiver 1.2V Power
N3	AVSS_PERX12	I	***Analogue Ground*** PCIE Receiver 1.2V Ground
M4	AVDD_PEPLL12	I	***Analogue Power*** PCIE PLL 1.2V Power
N4	AVSS_PEPLL12	I	***Analogue Ground*** PCIE Analogue PLL 1.2V Ground

¿ **SATA Power (7 PINs)**

PIN No.	Symbol	Type	Description
L5	AVDD_SATA33	I	***Analogue Power*** *SATA PHY*: 3.3V Analogue Power
M2	AVDD_SATA12	I	***Analogue Power*** *SATA PHY*: 1.2V Analogue Power
M1	AVSS_SATA	I	***Analogue Ground*** *SATA PHY*: Analogue Ground
K3	AVDD_SATARX12	I	***Analogue Power*** *SATA PHY*: Receiver 1.2V Analogue Power
L13	AVSS_SATARX12	I	***Analogue Ground*** *SATA PHY*: Receiver Analogue Ground
K4	AVDD_SATAPLL12	I	***Analogue Power*** *SATA PHY*: PLL 1.2V Analogue Power
L14	AVSS_SATAPLL12	I	***Analogue Ground*** *SATA PHY*: PLL Analogue Ground

¿ **Ethernet Power (5 PINs)**

PIN No.	Symbol	Type	Description
W3	AVDD_EPHYPLL18	I	***Analogue Power*** Internal Ethernet PHY PLL 1.8V Power
V3	AVSS_EPHYPLL18	I	***Analogue Ground*** Internal Ethernet PHY PLL 1.8V Ground
T4	AVDD_EPHYBG18	I	***Analogue Power*** Internal Ethernet PHY Band Gap 1.8V Power
P4	AVSS_EPHYBG18	I	***Analogue Ground*** Internal Ethernet PHY Band Gap 1.8V Ground
U1	AVSS_EPHYTX18	I	***Analogue Ground*** Internal Ethernet PHY TX 1.8V Ground

¿ **ADC Power (4 PINs)**

PIN No.	Symbol	Type	Description
J3	AVDD_ADC33	I	***Analogue Power***: ADC 3.3V Power
J4	AVSS_ADC33	I	***Analogue Ground***: ADC 3.3V Ground
M5	AVDD_TEMP18		***Analogue Power***: Temperature Sensor 1.8V Power
K5	AVSS_TEMP18		***Analogue Ground***: Temperature Sensor 1.8V Ground

¿ **System PLL Power (4 PINs)**

PIN No.	Symbol	Type	Description
U8	AVDD_NBPLL18	I	***Analogue Power***: CPU/DRAM PLL Analog Power
T8	AVSS_NBPLL18	I	***Analogue Ground***: CPU/DRAM PLL Analog Ground
T6	AVDD_SBPLL18	I	***Analogue Power***: SB System PLL Analog Power
T7	AVSS_SBPLL18	I	***Analogue Ground***: SB System PLL Analog Ground

¿ **Battery POWER (2 PINs)**

PIN No.	Symbol	Type	Description
H4	RTC_VDD33	I	***Battery power for RTC***
H3	RTC_VSS	I	***Battery ground for RTC***

¿ **Differential PAD Power (4 PINs)**

PIN No.	Symbol	Type	Description
W8	DIF_VDD12	I	***Differential PAD 1.2V Power***
V8	DIF_VSS12	I	***Differential PAD 1.2V Ground***
U6	DIF_VDD18	I	***Differential PAD 1.8V Power***
U7	DIF_VSS18	I	***Differential PAD 1.8V Ground***

¿ **1.2V POWER (8 PINs)**

PIN No.	Symbol	Type	Description
J10, J11, J9, L10, L11, L9, R5, R7	VDD12	I	***Core power***

¿ **1.5V POWER (8 PINs)**

PIN No.	Symbol	Type	Description
M16, M19, R12, R16, R19, U9, W13, W9	VDD15	I	***1.5V DDR Power***

¿ **1.8V POWER (2 PINs)**

PIN No.	Symbol	Type	Description
T5, D4	VDD18	I	***1.8V Power***

¿ **3.3V Power (7 PINs)**

PIN No.	Symbol	Type	Description

PIN No.	Symbol	Type	Description
B17, C10, C14, E17, H17, K19, R5	VDD33	I	***I/O PAD Power***

¿ **Digital Ground (28 PINs)**

PIN No.	Symbol	Type	Description
A19, B15, C18, C7, E10, E13, F18, F5, G15, K11, K15, K18, K9, M15, M18, R15, R18, R6, R9, T10, T12, U18, U5, V12, V14, V17, V9, W19	VSS	I	***Digital Ground***

4.5. PIN Capacitance Description (TBA)

4.6. PIN Pull-up / Pull-down Description (TBA)

4.7. The Registers only reset by power-good

These registers are only reset by PowerGood

1. GPIO_0~9 Direction register
2. GPIO_0~9 Data register
3. GPIO Port Config Registers
4. WatchDog Timer_0 3Ch Indirect access register
5. WatchDog Timer_1 ADh register