1. Overview

The **Vortex86DX2** is a high performance and fully static 32-bit X86 processor with the compatibility of Windows based, Linux and most popular 32-bit RTOS. It also integrates 32KB write through 4-way L1 cache, 256KB write through/write back 4-way L2 cache, PCIE bus in at 2.5 GHz, DDR2, ROM controller, ISA, I2C, SPI, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), Fast Ethernet, FIFO UART, USB2.0 Host and IDE/SATA controller within a single 720-pin BGA package to form a system-on-a-chip **(SOC)**. It provides an ideal solution for the embedded system and communications products (such as thin client, NAT router, home gateway, access point and tablet PC) to bring about desired performance.

2. Features

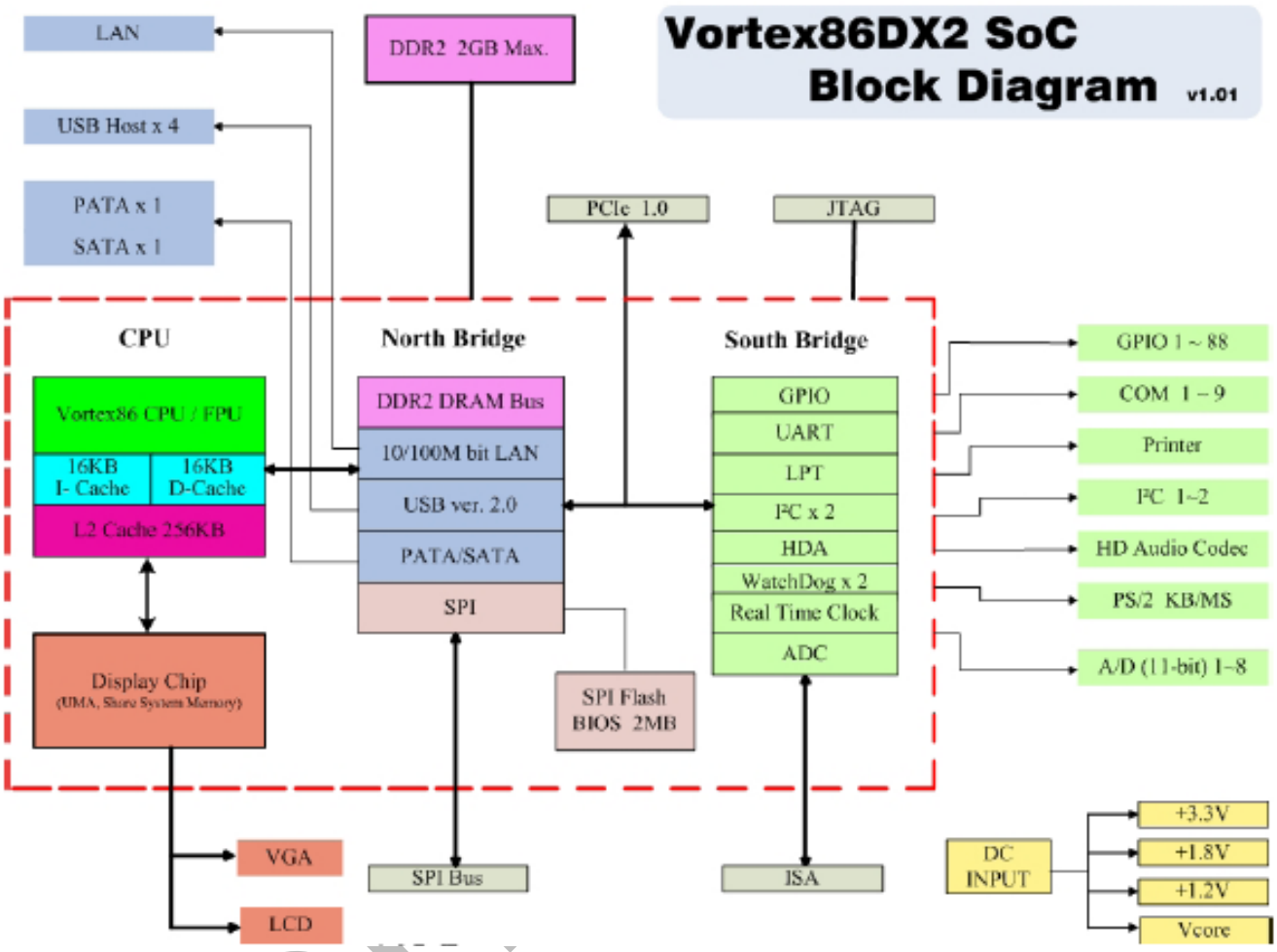
- **x86 Processor Core**
  - 6-stage pipeline
  - Max. Speed: 1GHz (Note 5)
- **Floating point unit support**
  - Extends CPU instruction set to include Trigonometric, Logarithmic and Exponential
  - Implements ANSI/IEEE standard 754-1985 for binary Floating-Point Architecture
- **Embedded I / D Separated L1 Cache**
  - 16K I-Cache, 16K D-Cache
- **Embedded L2 Cache**
  - 4-way 256KB L2 Cache
  - Write through or write back policy
- **DDRII Control Interface**
  - 32 bits data bus
  - DDRII clock support up to 366MHz
  - DDRII size support up to 2Gbytes
- **GPU Control Unit**
  - VGA controller
  - 2D Graphics engine support
  - UMA architecture
- **MAC Controller x 1**
- **Embedded 2MB Flash**
  - For BIOS storage
- **JTAG Interface** (Note 3)
- **IDE Controller**
  - PATA 100(HDD x 2) or SD x 2 at Primary Channel
  - SATA 1.5G (1 Port) at Secondary Channel
- **PCIE Control Interface x 2**
  - Up to 2 sets PCIE device
  - 3.3V I / O
- **USB 2.0 Host Support**
  - Supports HS, FS and LS
  - 4 port
- **USB 1.1 Device Support** (Note 1)
  - 1 port
  - Supports FS with 3 programmable endpoint
- **HDA Controller**
- **ISA Bus Interface**
  - AT clock programmable
  - 8/16 Bit ISA device with Zero-Wait-State
  - Generate refresh signals to ISA interface during DRAM refresh cycle
  - Support Max ISA Clock 33M
- **DMA Controller**
- **Interrupt Controller**
- **Counter / Timers**
  - 2 sets of 8254 timer controller
  - Timer output is 5V tolerance I/O on 2nd Timer
- **Real Time Clock**
  - Less than 2.5uA (3.0V) power consumption in Internal RTC Mode while chip is power-off.

- **PS / 2 Keyboard and Mouse Interface Support**
  - Compatible with 8042 controller
- **FIFO UART Port x 9 (9 sets COM Port)**
  - Compatible with 16C550 / 16C552
  - Default internal pull-up
  - Supports the programmable baud rate generator with the data rate from 50 to 6M bps
  - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
  - Support TXD_EN Signal on COM1/2/3/4
  - Port 80h output data could be sent to COM1 by software programming
- **Parallel Port x 1**
  - Supports SPP/EPP/ECP mode
- **Speaker out**
- **General Programmable I/O**
  - Supports 88 programmable I / O pins
  - Each GPIO pin can be individually configured to be an input/output pin
  - GPIO_P0~GPIO_P4 can be program by 8051A
  - GPIO_P0~GPIO_PA can be program by 8051B
  - GPIO_P0 and GPIO_P1 with interrupt support (input/output)
- **Redundant System Support**
- **I^2C bus x 2** (Note 2)
  - Compliant w/t V2.1
- **MTBF Counter**
- **ADC Interface x 8**
  - Effective Number of Bit=10 bits
- **Motion Control Interface Support**
  - 3 groups of controller, 4 controllers per group
  - Each controller can configure to PWM/Servo/Sensor Interface mode
  - Controller interconnect to the other with routing network in the same group
  - 8051 Internal Motion Control Support
- **General Shift Interface Support**
  - 3 channel
- **Full Duplex SPI bus x 2**
- **Input clock**
  - 14.318 MHz
  - 32.768 KHz
- **Output clock**
  - 24 MHz
  - 25 MHz
  - PCI clock
  - DDRII clock
- **Operating Voltage Range**
  - Core voltage: 1.0 V ± 5%, 1.2 V ± 5%
  - I / O voltage: 1.8V ± 5% , 3.3 V ± 10 %
- **Operating temperature**
  - -40℃ ~ 85℃ (Note 4)
- **Package Type**
  - 31x31mm, 720 Ball PBGA

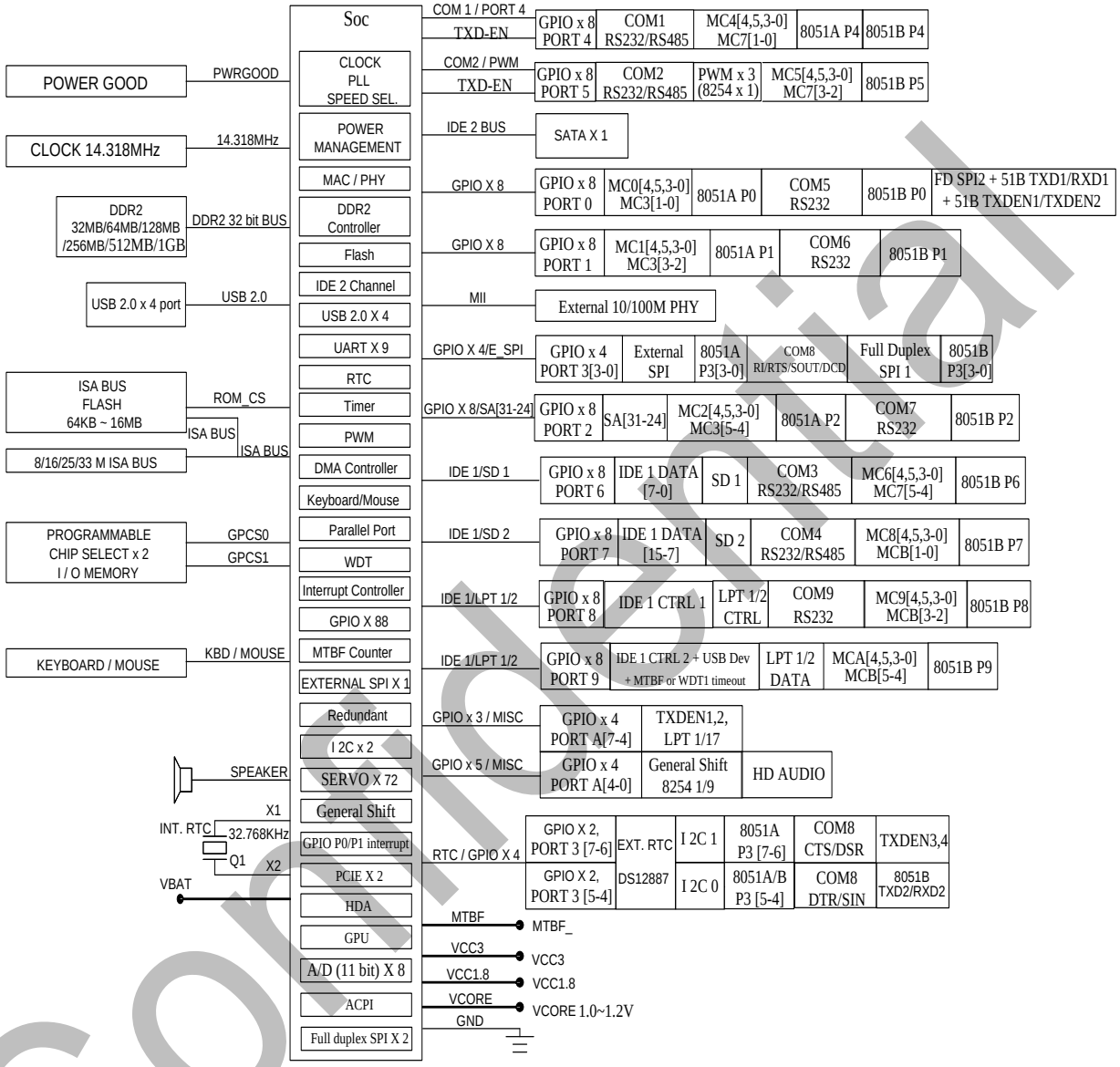
Note 1: USB Device support Linux gadget driver only.
Note 2: Some master code (general call, START and CBUS) not support.
Note 3: This is DMP's own defined JTAG, only support DMP's JTAG tool.
Note 4: Industrial Temperature -40℃ ~ 85℃ support in condition of CPU=800MHz, DRAM=300MHz.
Note 5: Unless the board is designed with a cooling fan, or DMP don't suggest to use 1GHz. We suggest the maximum CPU is 933MHz and DRAM is 333MHz for fanless (with heatsink) design using Vortex86DX2.

3. Block Diagram

3.1. System Block Diagram



3.2. Functions Block Diagram



3.3. PCI Device List

ID SEL	AD11	AD12	AD13	AD14	AD15	AD16	AD17	AD18	AD19	AD20	AD21	AD22	AD23	AD24	AD25	AD26	AD27
Device#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Function	NB	PCIE0	PCIE1					SB	MAC		USB 2.0 HOST		IDE	VGA	HD AUDIO	USB Device	
Fun0	NB0							SB0			OHCI						MC
Fun1	NB1							SB1			EHCI						8051B
Fun2																	SPI0
Fun3																	SPI1

PS. 1. USB 2.0 Host Controller supports 4 port

2. PCIE0, Interrupt Routing: INTA, INTB, INTC, INTD

PCIE1, Interrupt Routing: INTB, INTC, INTD, INTA

4. PIN Function List

4.1. BGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
A	A1_NC	STRAP_DDR[1]	IDE_PDD[11]/GPIO_P7[3]/SD1_CLK/MC8[3]/8051B_GPIO_P7[3]/RI4#	IDE_PDD[13]/GPIO_P7[5]/SD1_DATA[1]/MC8[4]/8051B_GPIO_P7[5]/DTR4#	IDE_PDD[9]/GPIO_P7[1]/SD1_DATA[3]/MC8[1]/8051B_GPIO_P7[1]/SOUT4	SIN6/GPIO_P1[4]/8051A_GPIO_P1[4]/MC1[5]/8051B_GPIO_P1[4]	RTC_XI	RTC_VSS	AFE_VCCDL12	ATSTN	AFE_TXVSSA	TXP	AFE_RXVCCA18	RXP	AFE_VCCD18	DIF_VD12IO	DIF3_CLK100_P	DIF_VD12IO	DIF2_CLK100_P	DIF1_SATA_PHY_CLK_P	DIF_VD12IO	PE0_TXP	AVSS_PE	PE0_RXP	AVSS_PEPLL12	PE1_RXP	AVSS1_PERX12	AVSS3_USBPLL12	AVDD3_USBPLL12	A30_NC
B	STRAP_DDR[0]	VSS	IDE_PDD[10]/GPIO_P7[2]/SD1_CMD/MC8[2]/8051B_GPIO_P7[2]/RTS4#	IDE_PDD[12]/GPIO_P7[4]/SD1_DATA[0]/MC8[5]/8051B_GPIO_P7[4]/SIN4	VSS	CTS6#/GPIO_P1[7]/8051A_GPIO_P1[7]/MC3[3]/8051B_GPIO_P1[7]	RTC_XOUT	VSS	AFE_VSSDL	ATSTP	AFE_VCCAPLL18	TXN	AFE_RXVSSA	RXN	AFE_VSSD	DIF_VS12IO	DIF3_CLK100_N	DIF_VS12IO	DIF2_CLK100_N	DIF1_SATA_PHY_CLK_N	DIF_VS12IO	PE0_TXN	AVDD_PE12	PE0_RXN	AVDD1_PEPLL12	PE1_RXN	AVDD1_PERX12	AVDD3_USB12	USB3_DP	USB3_DM

	D	C
1	RTC_IRQ8#/GPIO_P3[4]/8051A_GPIO_P3[4]/8051B_SIN2/8051B_GPIO_P3[4]/SIN8/I2C_SCL	STRAP_DDR[2]
2	RTC_AS/GPIO_P3[7]/8051A_GPIO_P3[7]/COM4_TXDEN/CTS8#/I2C1_SDA	PCIRST#
3	TDI	TMS
4	VSS	IDE_PDD[8]/GPIO_P7[0]/SD1_DATA[2]/MCB[0]/8051B_GPIO_P7[0]/DCD4#
5	IDE_PDD[14]/GPIO_P7[6]/SD1_CD/MCB[0]/8051B_GPIO_P7[6]/DSR4#	IDE_PDD[15]/GPIO_P7[7]/SD1_WP/MCB[1]/8051B_GPIO_P7[7]/CTS4#
6	DSR6#/GPIO_P1[6]/8051A_GPIO_P1[6]/MC3[2]/8051B_GPIO_P1[6]	RI6#/GPIO_P1[3]/8051A_GPIO_P1[3]/MC1[3]/8051B_GPIO_P1[3]
7	RTC_VDD33	RTC_PS
8	KBDAT	KBCLK
9	MSDAT	MSCLK
10	PWM2_CLK/GPIO_P5[4]/MC5[5]/8051B_GPIO_P5[4]/SIN2	VSS
11	PWM2_OUT/GPIO_P5[5]/MC5[4]/8051B_GPIO_P5[5]/DTR2#	PWM1_GATE/GPIO_P5[7]/MC7[3]/8051B_GPIO_P5[7]/CTS2#
12	PWM_GATE/GPIO_P5[6]/MC7[2]/8051B_GPIO_P5[6]/DSR2#	AFE_VSSAPLL
13	PWM1_OUT/GPIO_P5[2]/MC5[2]/8051B_GPIO_P5[2]/RTS2#	ISET
14	PWM1_CLK/GPIO_P5[3]/MC5[3]/8051B_GPIO_P5[3]/RI2#	AFE_VSSABG
15	PWM_OUT/GPIO_P5[1]/MC5[1]/8051B_GPIO_P5[1]/SOUT2	AFE_VCCABG18
16	VTEMP_TST	VCC18A_PLL5
17	ADC_VSS33A	VSS18A_PLL5
18	ADC_VSS33A_VREFN	VCC18A_PLL7
19	ADC_IN1	VSS18A_PLL7
20	ADC_IN2	VSS
21	VCC18D_TEMP	VSS18D_TEMP
22	DIF0_PCIE_PLLCLK100_N	DIF_VS12IO
23	DIF0_PCIE_PLLCLK100_P	DIF_VD12IO
24	AVDD_PERX12	AVSS_PERX12
25	AVSS1_PEPLL12	AVDD1_PE33
26	AVDD1_PE12	AVSS1_PE
27	PE1_TXN	PE1_TXP
28	USB_REXT3	AVDD2_USBBAS33
29	AVSS2_USBPLL12	AVSS3_USB33
30	AVDD2_USBPLL12	AVDD3_USB33

	E	F
1	E_SPI_DO/GPIO_P3[2]/8051A_GPIO_P3[2]/MC_SPI1_DO/8051B_GPIO_P3[2]/RTS8#	E_SPI_CS#/GPIO_P3[0]/8051A_GPIO_P3[0]/MC_SPI1_CS#/8051B_GPIO_P3[0]/DCD8#
2	VSS	RTC_RD#/GPIO_P3[6]/8051A_GPIO_P3[6]/COM3_TXDEN/DSR8#/I2C1_SCL
3	TCK	TDO
4	IDE_PDD[3]/GPIO_P6[3]/SD_CLK/MC6[3]/8051B_GPIO_P6[3]/RI3#	IDE_PDD[5]/GPIO_P6[5]/SD_DATA[1]/MC6[4]/8051B_GPIO_P6[5]/DTR3#
5	DCD6#/GPIO_P1[0]/8051A_GPIO_P1[0]/MC1[0]/8051B_GPIO_P1[0]	VSS
6	SOUT6/GPIO_P1[1]/8051A_GPIO_P1[1]/MC1[1]/8051B_GPIO_P1[1]	I_XIN_25M
7	VSS	RTS6#/GPIO_P1[2]/8051A_GPIO_P1[2]/MC1[2]/8051B_GPIO_P1[2]
8	DTR6#/GPIO_P1[5]/8051A_GPIO_P1[5]/MC1[4]/8051B_GPIO_P1[5]	IDE_PA[0]/GPIO_P8[1]/MC9[1]/8051B_GPIO_P8[1]/SOUT9/PE
9	IDE_PIOR#/GPIO_P8[4]/SD1_ACTIVE/MC9[5]/8051B_GPIO_P8[4]/SIN9/SLCIN	IDE_PA[2]/GPIO_P8[3]/MC9[3]/8051B_GPIO_P8[3]/RI9#/ACK#
10	VSS	IDE_PA[1]/GPIO_P8[2]/MC9[2]/8051B_GPIO_P8[2]/RTS9#/BUSY
11	IDE_PINT/GPIO_P8[0]/MC9[0]/8051B_GPIO_P8[0]/DCD9#/SLCT	IDE_PIOW#/GPIO_P8[5]/SD_ACTIVE/MC9[4]/8051B_GPIO_P8[5]/DTR9#/INIT#
12	PWM_CLK/GPIO_P5[0]/MC5[0]/8051B_GPIO_P5[0]/DCD2#	IDE_PCS0#/GPIO_P8[6]/MCB[2]/8051B_GPIO_P8[6]/DSR9#/ERR#
13	VSS	IDE_PCS1#/GPIO_P8[7]/MCB[3]/8051B_GPIO_P8[7]/CTS9#/AFD#
14	H_BCLK/GPIO_PA[4]/GSF_CLK	H_SDO/GPIO_PA[2]/GSF_CH1
15	VSS	H_RST#/GPIO_PA[0]/PWM2_GATE
16	ADC_VSS33D	ADC_VCC33D
17	ADC_VCC33A	ADC_IN3
18	ADC_VCC33A_VREFP	ADC_IN0
19	ADC_IN7	ADC_IN6
20	ADC_IN5	ADC_IN4
21	VSS18A_TEMP	VCC18A_TEMP
22	VSS	DCD7#/GPIO_P2[0]/8051A_GPIO_P2[0]/MC2[0]/8051B_GPIO_P2[0]/ISA_SA[24]
23	RTS7#/GPIO_P2[2]/8051A_GPIO_P2[2]/MC2[2]/8051B_GPIO_P2[2]/ISA_SA[26]	CTS7#/GPIO_P2[7]/8051A_GPIO_P2[7]/MC3[5]/8051B_GPIO_P2[7]/ISA_SA[31]
24	PE0_CLKN	SOUT7/GPIO_P2[1]/8051A_GPIO_P2[1]/MC2[1]/8051B_GPIO_P2[1]/ISA_SA[25]
25	PE0_CLKP	VSS
26	RI7#/GPIO_P2[3]/8051A_GPIO_P2[3]/MC2[3]/8051B_GPIO_P2[3]/ISA_SA[27]	SIN7/GPIO_P2[4]/8051A_GPIO_P2[4]/MC2[5]/8051B_GPIO_P2[4]/ISA_SA[28]
27	DTR7#/GPIO_P2[5]/8051A_GPIO_P2[5]/MC2[4]/8051B_GPIO_P2[5]/ISA_SA[29]	VSS
28	AVDD2_USB12	USB_REXT2
29	USB2_DP	AVSS2_USB33
30	USB2_DM	AVDD2_USB33

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
G	TXD[2]	E_SPI_CLK/GPIO_P3[1]/8051A_GPIO_P3[1]/MC_SPI1_CLK/8051B_GPIO_P3[1]/SOUT8/ 8051B_SOUT2	RTC_WR#/GPIO_P3[5]/8051A_GPIO_P3[5]/8051B_SOUT2/8051B_GPIO_P3[5]/DTR8#/I2C _SDA	IDE_PDD[4]/GPIO_P6[4]/SD_DATA[0]/MC6[5]/8051B_GPIO_P6[4]/SIN3	PADWPB	VSS																		DSR7#/GPIO_P2[6]/8051A_GPIO_P2[6]/MC3[4]/8051B_GPIO_P2[6]/ISA_SA[30]	IDE_PIORDY/GPIO_P9[5]/MCA[4]/8051B_GPIO_P9[5]/PD[5]	MTBF/GPIO_P9[7]/MCB[5]/8051B_GPIO_P9[7]/WDT_RSTB/PD[7]	AVSS2_USBBAS33	AVSS1_USBPLL12	AVDD1_USBPLL12
H	TXD[1]	VSS	E_SPI_DI/GPIO_P3[3]/8051A_GPIO_P3[3]/MC_SPI1_DI/8051B_GPIO_P3[3]/RI8#	IDE_PDD[1]/GPIO_P6[1]/SD_DATA[3]/MC6[1]/8051B_GPIO_P6[1]/SOUT3	VSS	G_XIN_14318																		IDE_PDACK#/GPIO_P9[4]/MCA[5]/8051B_GPIO_P9[4]/PD[4]	VSS	IDE_PCBLID#/GPIO_P9[3]/MCA[3]/8051B_GPIO_P9[3]/PD[3]	AVDD1_USB12	USB1_DP	USB1_DM

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
J	TXD[3]	DUPLEX	VDD33	RXD[2]	RXD[0]	TXEN																								
K	TXD[0]	VSS	RXD[3]	RXD[1]	VSS	MDC				SPI_DI	SPI_CS#/ROM_CS#/ STRAP_BMS	IDE_PDD[7]/GPIO_P6[7]/SD_WP/MC7[5]/8051B_GPIO_P6[7]/CTS3#	IDE_PDD[6]/GPIO_P6[6]/SD_CD/MC7[4]/8051B_GPIO_P6[6]/DSR3#	TX_DEN2/GPIO_PA[6]	H_SYNC/GPIO_PA[3]/GSF_CH2	H_SDI/GPIO_PA[1]/GSF_CH0	VSS	VDD12	VDD12	VDD33	VDD33					UD_DM/GPIO_P9[0]/MCA[0]/8051B_GPIO_P9[0]/PD[0]	UD_DP/GPIO_P9[1]/MCA[1]/8051B_GPIO_P9[1]/PD[1]	VSS	USB_REXT1	AVSS_USBPLL12	AVDD_USBPLL12

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
J	TXD[3]	DUPLEX	VDD33	RXD[2]	RXD[0]	TXEN																								
K	TXD[0]	VSS	RXD[3]	RXD[1]	VSS	MDC				SPI_DI	SPI_CS#/ROM_CS#/ STRAP_BMS	IDE_PDD[7]/GPIO_P6[7]/SD_WP/MC7[5]/8051B_GPIO_P6[7]/CTS3#	IDE_PDD[6]/GPIO_P6[6]/SD_CD/MC7[4]/8051B_GPIO_P6[6]/DSR3#	TX_DEN2/GPIO_PA[6]	H_SYNC/GPIO_PA[3]/GSF_CH2	H_SDI/GPIO_PA[1]/GSF_CH0	VSS	VDD12	VDD12	VDD33	VDD33					UD_DM/GPIO_P9[0]/MCA[0]/8051B_GPIO_P9[0]/PD[0]	UD_DP/GPIO_P9[1]/MCA[1]/8051B_GPIO_P9[1]/PD[1]	VSS	USB_REXT1	AVSS_USBPLL12	AVDD_USBPLL12

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
L	TXC	RXC	LINK/ACTIVE	RXDV	MDIO	COL				SPI_CK	SPI_DO	IDE_PDD[2]/GPIO_P6[2]/SD_CMD/MC6[2]/8051B_GPIO_P6[2]/RTS3#	IDE_PDD[0]/GPIO_P6[0]/SD_DATA[2]/MC6[0]/8051B_GPIO_P6[0]/DCD3#	TX_DEN1/GPIO_PA[7]	STB#/GPIO_PA[5]	VSS	VSS	VDD12	VDD12	VDD12	VDD33				VSS	DSR5#/GPIO_P0[6]/8051A_GPIO_P0[6]/MC3[0]/8051B_GPIO_P0[6]/8051B_SIN1	CTS5#/GPIO_P0[7]/8051A_GPIO_P0[7]/MC3[1]/8051B_GPIO_P0[7]/8051B_SOUT1	AVDD_USB12	USB_DP	USB_DM
M	VSS	VSS	PWRGOOD	VSS	PADHOLDB	VSS				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD12	VDD12	VDD33				RTS5#/GPIO_P0[2]/8051A_GPIO_P0[2]/MC0[2]/8051B_GPIO_P0[2]/MC_SPI2_DO	SOUT5/GPIO_P0[1]/8051A_GPIO_P0[1]/MC0[1]/8051B_GPIO_P0[1]/MC_SPI2_CLK	VSS	USB_REXT	AVSS_USB33	AVDD_USB33

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
N	G_IOR	AVSS_DACR18	AVDD_DACR18	G_FPD[14]	G_GPIO[3]	G_GPIO[2]				VDD33	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD12	VDD12	VDD12				DCD5#/GPIO_P0[0]/8051A_GPIO_P0[0]/MC0[0]/8051B_GPIO_P0[0]/MC_SPI2_CS#	SIN1/GPIO_P4[4]/8051A_GPIO_P4[4]/MC4[5]/8051B_GPIO_P4[4]	RI5#/GPIO_P0[3]/8051A_GPIO_P0[3]/MC0[3]/8051B_GPIO_P0[3]/MC_SPI2_DI	AVSS_USBBAS33	VSS	SATA_CLKN
P	G_IOG	AVSS_DACG18	AVDD_DACG18	VDD_DAC10	AVSS_VDISPLL18	AVDD_VDISPLL18				VDD33	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD12	VDD12				RI1#/GPIO_P4[3]/8051A_GPIO_P4[3]/MC4[3]/8051B_GPIO_P4[3]	VSS	DTR5#/GPIO_P0[5]/8051A_GPIO_P0[5]/MC0[4]/8051B_GPIO_P0[5]/8051B_TXDEN1	VSS	AVDD_SATA33	SATA_CLKP

	U	T	R
1	VSS	G_REXT	G_IOB
2	G_ENVEE	AVSS_DACBG18	AVSS_DACB18
3	G_FPD[23]	AVDD_DACBG18	AVDD_DACB18
4	G_FP1DE	G_FPD[20]	VSS
5	G_FPD[9]	AVSS_DDRPLL18	AVSS_CPUPLL18
6	VSS	AVDD_DDRPLL18	AVDD_CPUPLL18
7			
8			
9			
10	VDD18	VDD18	VSS
11	VDD18	VDD18	VSS
12	VDD18	VDD18	VSS
13	VDD18	VDD18	VSS
14	VDD18	VDD18	VDD18
15	VSS	VSS	VSS
16	VSS	VSS	VSS
17	VSS	VSS	VSS
18	VSS	VSS	VSS
19	VSS	VSS	VSS
20	MEMCS16#	IOW#	VSS
21	EXT_GPCS#	IOR#	VSS
22			
23			
24			
25	IOCS16#	DTR1#/GPIO_P4[5]/8051A_GPIO_P4[5]/MC4[4]/8051B_GPIO_P4[5]	CTS1#/GPIO_P4[7]/8051A_GPIO_P4[7]/MC7[1]/8051B_GPIO_P4[7]
26	DACK#[6]	DSR1#/GPIO_P4[6]/8051A_GPIO_P4[6]/MC7[0]/8051B_GPIO_P4[6]	SOUT1/GPIO_P4[1]/8051A_GPIO_P4[1]/MC4[1]/8051B_GPIO_P4[1]
27	IRQ[11]	DACK#[0]	RTS1#/GPIO_P4[2]/8051A_GPIO_P4[2]/MC4[2]/8051B_GPIO_P4[2]
28	RST_DRV	VSS	DCD1#/GPIO_P4[0]/8051A_GPIO_P4[0]/MC4[0]/8051B_GPIO_P4[0]
29	AVDD_SATARX12	SATA_RXN	AVSS_SATAPLL12
30	AVSS_SATARX12	SATA_RXP	AVDD_SATAPLL12

AH	AG	AF	AE	AD	AC	AB	AA	Y	W	V	
MD[9]	VSS	MD[2]	VSS	G_FP1HS	G_FPD[0]	G_FPD[11]	G_FPD[16]	G_ENVDD	G_FPD[22]	G_HSYNC	1
MD[8]	DQS[0]	MD[1]	G_FPD[1]	G_FP1CLK	VSS	VDD33	G_FPD[13]	VSS	VDD33	G_FPD[19]	2
VSS	DQS#[0]	DVDD18	VSS	G_FPD[4]	G_FPD[8]	G_FPD[12]	VSS	G_FPD[6]	G_DDC1_DAT	G_DDC1_CLK	3
MD[7]	MD[3]	MD[0]	G_FP1DET	G_ENBLT	G_FP1VS	G_VSYNC	G_FPD[21]	G_DDC_CLK	G_FPD[10]	VSS	4
MD[5]	VSS	DQM[0]	DVDD18	VSS	G_FPD[15]	G_FPD[2]	VSS	G_DDC_DAT	G_FPD[3]	G_TVCLKIN	5
MD[6]	MD[4]	VSS	OCDBIAS	VDD33	G_FPD[7]	VDD33	G_FPD[18]	G_FPD[5]	VDD33	G_FPD[17]	6
MD[14]	VSS	DVDD18	VDD10								7
MA[13]	MA[8]	MA[12]	VDD10								8
MA[11]	MA[6]	MA[14]	VSS								9
MA[2]	VSS	CS1#	VDD10				VSS	VSS	VSS	VSS	10
MA[5]	MA[0]	VSS	VREF				VSS	VSS	VDD10	VSS	11
MA[10]	RAS#	VSS	DVDD18				VDD10	VDD10	VDD10	VSS	12
BA[0]	DVDD18	ODT[1]	BA[1]				VDD10	VDD10	VDD10	VSS	13
DVDD18	ODT[0]	CKE	CS0#				VDD10	VDD10	VDD10	VSS	14
MD[17]	MD[24]	VSS	DVDD18				VDD10	VDD10	VSS	VSS	15
MD[19]	MD[26]	MD[25]	DVDD18				VSS	VSS	VSS	VSS	16
DVDD18	MD[27]	VSS	DQM[3]				VDD33	VDD33	VSS	VSS	17
DQM[2]	MD[28]	DQS#[3]	DQS[3]				VDD33	VDD33	VSS	VSS	18
MD[23]	MD[29]	VSS	MD[30]				VDD33	VDD33	VSS	VSS	19
VSS	DVDD18	MD[31]	DVDD18				VSS	IOCHRDY	TC	SMEMR#	20
SD[11]	SD[10]	VSS	OCDBIAS1				VSS	DRQ[3]	DRQ[6]	SBHE#	21
SD[9]	SD[8]	IRQ[4]	IRQ[9]								22
SD[5]	IRQ[3]	DACK#[5]	DRQ[2]								23
SD[3]	SD[2]	0WS#	OSC14318								24
DACK#[1]	DACK#[2]	VSS	DACK#[7]	GPCS1#	BALE	MEMW#	SYSCLK	AEN	IRQ[5]	VSS	25
SA[4]	MEMR#	DRQ[1]	DRQ[5]	DRQ[0]	IRQ[12]	IRQ[10]	VSS	REFRESH#	SD[15]	GPCS0#	26
VSS	SA[9]	SA[13]	VSS	SA[17]	DRQ[7]	IRQ[15]	SD[14]	SMEMW#	IOCHCK#	SD[13]	27
SA[7]	SA[11]	SA[16]	LA[18]	LA[21]	IRQ[14]	VSS	IRQ[7]	IRQ[6]	EXTSYSFAILIN#	VSS	28
VSS	SA[18]	LA[19]	LA[22]	VSS	LA[23]	SPEAKER	DACK#[3]	EXT_SWITCH_FAIL#	AVDD_SATA12	SATA_TXN	29
SA[15]	SA[19]	LA[17]	LA[20]	CLK24MOUT	VSS	CLK25MOUT	SYSFAILOUT#	VSS	AVSS_SATA	SATA_TXP	30

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
AJ	MD[10]	MD[11]	DQM[1]	DVDD18	MD[12]	DVDD18	VSS	DRAMCLK	MA[4]	MA[9]	CAS#	VSS	WE#	DRAMCLK1	MD[16]	VSS	DQS#[2]	MD[21]	VSS	SD[12]	XOUT_14318	VSS	SD[4]	SD[0]	VSS	SA[1]	SA[5]	SA[8]	SA[14]	SA[10]
AK	AK1_NC	VSS	DQS#[1]	DQS[1]	VSS	MD[13]	MD[15]	DRAMCLK#	MA[7]	VSS	MA[3]	MA[1]	BA[2]	DRAMCLK#1	VSS	MD[18]	DQS[2]	MD[20]	MD[22]	VSS	XIN_14318	SD[6]	SD[7]	SD[1]	SA[2]	SA[0]	SA[3]	SA[6]	SA[12]	AK30_NC

4.2. PIN Out Table

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
A1	A1_NC	G1	TXD[2]	T1	G_REXT	AE1	VSS
A2	STRAP_DDR[1]	G2	E_SPI_CLK/GPIO_P3[1]/8051A_GPIO_P3[1]/MC_SPI1_CLK/8051B_GPIO_P3[1]/SOUT8/8051B_SOUT2	T2	AVSS_DACBG18	AE2	G_FPD[1]
A3	IDE_PDD[11]/GPIO_P7[3]/SD1_CLK/MC8[3]/8051B_GPIO_P7[3]/RI4#	G3	RTC_WR#/GPIO_P3[5]/8051A_GPIO_P3[5]/8051B_SOUT2/8051B_GPIO_P3[5]/DTR8#/I2C_SDA	T3	AVDD_DACBG18	AE3	VSS
A4	IDE_PDD[13]/GPIO_P7[5]/SD1_DATA[1]/MC8[4]/8051B_GPIO_P7[5]/DTR4#	G4	IDE_PDD[4]/GPIO_P6[4]/SD_DATA[0]/MC6[5]/8051B_GPIO_P6[4]/SIN3	T4	G_FPD[20]	AE4	G_FP1DET
A5	IDE_PDD[9]/GPIO_P7[1]/SD1_DATA[3]/MC8[1]/8051B_GPIO_P7[1]/SOUT4	G5	PADWPB	T5	AVSS_DDRPLL18	AE5	DVDD18
A6	SIN6/GPIO_P1[4]/8051A_GPIO_P1[4]/MC1[5]/8051B_GPIO_P1[4]	G6	VSS	T6	AVDD_DDRPLL18	AE6	OCDBIAS
A7	RTC_XI	G25	DSR7#/GPIO_P2[6]/8051A_GPIO_P2[6]/MC3[4]/8051B_GPIO_P2[6]/ISA_SA[30]	T10	VDD18	AE7	VDD10
A8	RTC_VSS	G26	IDE_PIORDY/GPIO_P9[5]/MCA[4]/8051B_GPIO_P9[5]/PD[5]	T11	VDD18	AE8	VDD10
A9	AFE_VCCDL12	G27	MTBF/GPIO_P9[7]/MCB[5]/8051B_GPIO_P9[7]/WDT_RSTB/PD[7]	T12	VDD18	AE9	VSS
A10	ATSTN	G28	AVSS2_USBBAS33	T13	VDD18	AE10	VDD10
A11	AFE_TXVSSA	G29	AVSS1_USBPLL12	T14	VDD18	AE11	VREF
A12	TXP	G30	AVDD1_USBPLL12	T15	VSS	AE12	DVDD18
A13	AFE_RXVCCA18	H1	TXD[1]	T16	VSS	AE13	BA[1]
A14	RXP	H2	VSS	T17	VSS	AE14	CS0#
A15	AFE_VCCD18	H3	E_SPI_DI/GPIO_P3[3]/8051A_GPIO_P3[3]/MC_SPI1_DI/8051B_GPIO_P3[3]/RI8#	T18	VSS	AE15	DVDD18
A16	DIF_VD12IO	H4	IDE_PDD[1]/GPIO_P6[1]/SD_DATA[3]/MC6[1]/8051B_GPIO_P6[1]/SOUT3	T19	VSS	AE16	DVDD18
A17	DIF3_CLK100_P	H5	VSS	T20	IOW#	AE17	DQM[3]
A18	DIF_VD12IO	H6	G_XIN_14318	T21	IOR#	AE18	DQS[3]
A19	DIF2_CLK100_P	H25	IDE_PDACK#/GPIO_P9[4]/MCA[5]/8051B_GPIO_P9[4]/PD	T25	DTR1#/GPIO_P4[5]/8051A_GPIO_P4[5]/MC4[4]/8051B_GP	AE19	MD[30]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
			[4]		IO_P4[5]		
A20	DIF1_SATA_PHY_CLK_P	H26	VSS	T26	DSR1#/GPIO_P4[6]/8051A_GPIO_P4[6]/MC7[0]/8051B_GPIO_P4[6]	AE20	DVDD18
A21	DIF_VD12IO	H27	IDE_PCBLID#/GPIO_P9[3]/MCA[3]/8051B_GPIO_P9[3]/PD[3]	T27	DACK#[0]	AE21	OCDBIAS1
A22	PE0_TXP	H28	AVDD1_USB12	T28	VSS	AE22	IRQ[9]
A23	AVSS_PE	H29	USB1_DP	T29	SATA_RXN	AE23	DRQ[2]
A24	PE0_RXP	H30	USB1_DM	T30	SATA_RXP	AE24	OSC14318
A25	AVSS_PEPLL12	J1	TXD[3]	U1	VSS	AE25	DACK#[7]
A26	PE1_RXP	J2	DUPLEX	U2	G_ENVEE	AE26	DRQ[5]
A27	AVSS1_PERX12	J3	VDD33	U3	G_FPD[23]	AE27	VSS
A28	AVSS3_USBPLL12	J4	RXD[2]	U4	G_FP1DE	AE28	LA[18]
A29	AVDD3_USBPLL12	J5	RXD[0]	U5	G_FPD[9]	AE29	LA[22]
A30	A30_NC	J6	TXEN	U6	VSS	AE30	LA[20]
B1	STRAP_DDR[0]	J25	IDE_PDRQ/GPIO_P9[6]/MCB[4]/8051B_GPIO_P9[6]/PD[6]	U10	VDD18	AF1	MD[2]
B2	VSS	J26	SIN5/GPIO_P0[4]/8051A_GPIO_P0[4]/MC0[5]/8051B_GPIO_P0[4]/8051B_TXDEN2	U11	VDD18	AF2	MD[1]
B3	IDE_PDD[10]/GPIO_P7[2]/SD1_CMD/MC8[2]/8051B_GPIO_P7[2]/RTS4#	J27	IDE_PRST#/GPIO_P9[2]/MCA[2]/8051B_GPIO_P9[2]/PD[2]	U12	VDD18	AF3	DVDD18
B4	IDE_PDD[12]/GPIO_P7[4]/SD1_DATA[0]/MC8[5]/8051B_GPIO_P7[4]/SIN4	J28	AVDD_USBBAS33	U13	VDD18	AF4	MD[0]
B5	VSS	J29	AVSS1_USB33	U14	VDD18	AF5	DQM[0]
B6	CTS6#/GPIO_P1[7]/8051A_GPIO_P1[7]/MC3[3]/8051B_GPIO_P1[7]	J30	AVDD1_USB33	U15	VSS	AF6	VSS
B7	RTC_XOUT	K1	TXD[0]	U16	VSS	AF7	DVDD18
B8	VSS	K2	VSS	U17	VSS	AF8	MA[12]
B9	AFE_VSSDL	K3	RXD[3]	U18	VSS	AF9	MA[14]
B10	ATSTP	K4	RXD[1]	U19	VSS	AF10	CS1#
B11	AFE_VCCAPLL18	K5	VSS	U20	MEMCS16#	AF11	VSS
B12	TXN	K6	MDC	U21	EXT_GPCS#	AF12	VSS
B13	AFE_RXVSSA	K10	SPI_DI	U25	IOCS16#	AF13	ODT[1]
B14	RXN	K11	SPI_CS#/ROM_CS#/STRAP_BMS	U26	DACK#[6]	AF14	CKE
B15	AFE_VSSD	K12	IDE_PDD[7]/GPIO_P6[7]/SD_WP/MC7[5]/8051B_GPIO_P6[7]/CTS3#	U27	IRQ[11]	AF15	VSS
B16	DIF_VS12IO	K13	IDE_PDD[6]/GPIO_P6[6]/SD_CD/MC7[4]/8051B_GPIO_P6[6]/DSR3#	U28	RST_DRV	AF16	MD[25]
B17	DIF3_CLK100_N	K14	TX_DEN2/GPIO_PA[6]	U29	AVDD_SATARX12	AF17	VSS
B18	DIF_VS12IO	K15	H_SYNC/GPIO_PA[3]/GSF_CH2	U30	AVSS_SATARX12	AF18	DQS#[3]
B19	DIF2_CLK100_N	K16	H_SDI/GPIO_PA[1]/GSF_CH0	V1	G_HSYNC	AF19	VSS
B20	DIF1_SATA_PHY_CLK_N	K17	VSS	V2	G_FPD[19]	AF20	MD[31]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
B21	DIF_VS12IO	K18	VDD12	V3	G_DDC1_CLK	AF21	VSS
B22	PE0_TXN	K19	VDD12	V4	VSS	AF22	IRQ[4]
B23	AVDD_PE12	K20	VDD33	V5	G_TVCLKIN	AF23	DACK#[5]
B24	PE0_RXN	K21	VDD33	V6	G_FPD[17]	AF24	0WS#
B25	AVDD1_PEPLL12	K25	UD_DM/GPIO_P9[0]/MCA[0]/ 8051B_GPIO_P9[0]/PD[0]	V10	VSS	AF25	VSS
B26	PE1_RXN	K26	UD_DP/GPIO_P9[1]/MCA[1]/ 8051B_GPIO_P9[1]/PD[1]	V11	VSS	AF26	DRQ[1]
B27	AVDD1_PERX12	K27	VSS	V12	VSS	AF27	SA[13]
B28	AVDD3_USB12	K28	USB_REXT1	V13	VSS	AF28	SA[16]
B29	USB3_DP	K29	AVSS_USBPLL12	V14	VSS	AF29	LA[19]
B30	USB3_DM	K30	AVDD_USBPLL12	V15	VSS	AF30	LA[17]
C1	STRAP_DDR[2]	L1	TXC	V16	VSS	AG1	VSS
C2	PCIRST#	L2	RXC	V17	VSS	AG2	DQS[0]
C3	TMS	L3	LINK/ACTIVE	V18	VSS	AG3	DQS#[0]
C4	IDE_PDD[8]/GPIO_P7[0]/SD1_DATA[2]/MC8[0]/8051B_GPIO_P7[0]/DCD4#	L4	RXDV	V19	VSS	AG4	MD[3]
C5	IDE_PDD[15]/GPIO_P7[7]/ SD1_WP/MCB[1]/8051B_GPIO_P7[7]/CTS4#	L5	MDIO	V20	SMEMR#	AG5	VSS
C6	RI6#/GPIO_P1[3]/8051A_GPIO_P1[3]/MC1[3]/8051B_ GPIO_P1[3]	L6	COL	V21	SBHE#	AG6	MD[4]
C7	RTC_PS	L10	SPI_CK	V25	VSS	AG7	VSS
C8	KBCLK	L11	SPI_DO	V26	GPCS0#	AG8	MA[8]
C9	MSCLK	L12	IDE_PDD[2]/GPIO_P6[2]/SD_CMD/MC6[2]/8051B_GPIO_P6[2]/RTS3#	V27	SD[13]	AG9	MA[6]
C10	VSS	L13	IDE_PDD[0]/GPIO_P6[0]/SD_DATA[2]/MC6[0]/8051B_GPIO_P6[0]/DCD3#	V28	VSS	AG10	VSS
C11	PWM1_GATE/GPIO_P5[7]/ MC7[3]/8051B_GPIO_P5[7] /CTS2#	L14	TX_DEN1/GPIO_PA[7]	V29	SATA_TXN	AG11	MA[0]
C12	AFE_VSSAPLL	L15	STB#/GPIO_PA[5]	V30	SATA_TXP	AG12	RAS#
C13	ISET	L16	VSS	W1	G_FPD[22]	AG13	DVDD18
C14	AFE_VSSABG	L17	VSS	W2	VDD33	AG14	ODT[0]
C15	AFE_VCCABG18	L18	VDD12	W3	G_DDC1_DAT	AG15	MD[24]
C16	VCC18A_PLL5	L19	VDD12	W4	G_FPD[10]	AG16	MD[26]
C17	VSS18A_PLL5	L20	VDD12	W5	G_FPD[3]	AG17	MD[27]
C18	VCC18A_PLL7	L21	VDD33	W6	VDD33	AG18	MD[28]
C19	VSS18A_PLL7	L25	VSS	W10	VSS	AG19	MD[29]
C20	VSS	L26	DSR5#/GPIO_P0[6]/8051A_GPIO_P0[6]/MC3[0]/8051B_GPIO_P0[6]/8051B_SIN1	W11	VDD10	AG20	DVDD18
C21	VSS18D_TEMP	L27	CTS5#/GPIO_P0[7]/8051A_GPIO_P0[7]/MC3[1]/8051B_GPIO_P0[7]/8051B_SOUT1	W12	VDD10	AG21	SD[10]
C22	DIF_VS12IO	L28	AVDD_USB12	W13	VDD10	AG22	SD[8]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
C23	DIF_VD12IO	L29	USB_DP	W14	VDD10	AG23	IRQ[3]
C24	AVSS_PERX12	L30	USB_DM	W15	VSS	AG24	SD[2]
C25	AVDD1_PE33	M1	VSS	W16	VSS	AG25	DACK#[2]
C26	AVSS1_PE	M2	VSS	W17	VSS	AG26	MEMR#
C27	PE1_TXP	M3	PWRGOOD	W18	VSS	AG27	SA[9]
C28	AVDD2_USBBAS33	M4	VSS	W19	VSS	AG28	SA[11]
C29	AVSS3_USB33	M5	PADHOLDB	W20	TC	AG29	SA[18]
C30	AVDD3_USB33	M6	VSS	W21	DRQ[6]	AG30	SA[19]
D1	RTC_IRQ8#/GPIO_P3[4]/8051A_GPIO_P3[4]/8051B_SIN2/8051B_GPIO_P3[4]/SIN8/I2C_SCL	M10	VSS	W25	IRQ[5]	AH1	MD[9]
D2	RTC_AS/GPIO_P3[7]/8051A_GPIO_P3[7]/COM4_TXDEN/CTS8#/I2C1_SDA	M11	VSS	W26	SD[15]	AH2	MD[8]
D3	TDI	M12	VSS	W27	IOCHCK#	AH3	VSS
D4	VSS	M13	VSS	W28	EXTSYSFAILIN#	AH4	MD[7]
D5	IDE_PDD[14]/GPIO_P7[6]/SD1_CD/MCB[0]/8051B_GPIO_P7[6]/DSR4#	M14	VSS	W29	AVDD_SATA12	AH5	MD[5]
D6	DSR6#/GPIO_P1[6]/8051A_GPIO_P1[6]/MC3[2]/8051B_GPIO_P1[6]	M15	VSS	W30	AVSS_SATA	AH6	MD[6]
D7	RTC_VDD33	M16	VSS	Y1	G_ENVDD	AH7	MD[14]
D8	KBDAT	M17	VSS	Y2	VSS	AH8	MA[13]
D9	MSDAT	M18	VSS	Y3	G_FPD[6]	AH9	MA[11]
D10	PWM2_CLK/GPIO_P5[4]/MC5[5]/8051B_GPIO_P5[4]/SIN2	M19	VDD12	Y4	G_DDC_CLK	AH10	MA[2]
D11	PWM2_OUT/GPIO_P5[5]/MC5[4]/8051B_GPIO_P5[5]/DTR2#	M20	VDD12	Y5	G_DDC_DAT	AH11	MA[5]
D12	PWM_GATE/GPIO_P5[6]/MC7[2]/8051B_GPIO_P5[6]/DSR2#	M21	VDD33	Y6	G_FPD[5]	AH12	MA[10]
D13	PWM1_OUT/GPIO_P5[2]/MC5[2]/8051B_GPIO_P5[2]/RTS2#	M25	RTS5#/GPIO_P0[2]/8051A_GPIO_P0[2]/MC0[2]/8051B_GPIO_P0[2]/MC_SPI2_DO	Y10	VSS	AH13	BA[0]
D14	PWM1_CLK/GPIO_P5[3]/MC5[3]/8051B_GPIO_P5[3]/RI2#	M26	SOUT5/GPIO_P0[1]/8051A_GPIO_P0[1]/MC0[1]/8051B_GPIO_P0[1]/MC_SPI2_CLK	Y11	VSS	AH14	DVDD18
D15	PWM_OUT/GPIO_P5[1]/MC5[1]/8051B_GPIO_P5[1]/SOUT2	M27	VSS	Y12	VDD10	AH15	MD[17]
D16	VTEMP_TST	M28	USB_REXT	Y13	VDD10	AH16	MD[19]
D17	ADC_VSS33A	M29	AVSS_USB33	Y14	VDD10	AH17	DVDD18
D18	ADC_VSS33A_VREFN	M30	AVDD_USB33	Y15	VDD10	AH18	DQM[2]
D19	ADC_IN1	N1	G_IOR	Y16	VSS	AH19	MD[23]
D20	ADC_IN2	N2	AVSS_DACR18	Y17	VDD33	AH20	VSS
D21	VCC18D_TEMP	N3	AVDD_DACR18	Y18	VDD33	AH21	SD[11]
D22	DIF0_PCIE_PLLCLK100_N	N4	G_FPD[14]	Y19	VDD33	AH22	SD[9]
D23	DIF0_PCIE_PLLCLK100_P	N5	G_GPIO[3]	Y20	IOCHRDY	AH23	SD[5]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
D24	AVDD_PERX12	N6	G_GPIO[2]	Y21	DRQ[3]	AH24	SD[3]
D25	AVSS1_PEPLL12	N10	VDD33	Y25	AEN	AH25	DACK#[1]
D26	AVDD1_PE12	N11	VSS	Y26	REFRESH#	AH26	SA[4]
D27	PE1_TXN	N12	VSS	Y27	SMEMW#	AH27	VSS
D28	USB_REXT3	N13	VSS	Y28	IRQ[6]	AH28	SA[7]
D29	AVSS2_USBPLL12	N14	VSS	Y29	EXT_SWITCH_FAIL#	AH29	VSS
D30	AVDD2_USBPLL12	N15	VSS	Y30	VSS	AH30	SA[15]
E1	E_SPI_DO/GPIO_P3[2]/8051A_GPIO_P3[2]/MC_SPI1_DO/8051B_GPIO_P3[2]/RTS8#	N16	VSS	AA1	G_FPD[16]	AJ1	MD[10]
E2	VSS	N17	VSS	AA2	G_FPD[13]	AJ2	MD[11]
E3	TCK	N18	VSS	AA3	VSS	AJ3	DQM[1]
E4	IDE_PDD[3]/GPIO_P6[3]/SD_CLK/MC6[3]/8051B_GPIO_P6[3]/RI3#	N19	VDD12	AA4	G_FPD[21]	AJ4	DVDD18
E5	DCD6#/GPIO_P1[0]/8051A_GPIO_P1[0]/MC1[0]/8051B_GPIO_P1[0]	N20	VDD12	AA5	VSS	AJ5	MD[12]
E6	SOUT6/GPIO_P1[1]/8051A_GPIO_P1[1]/MC1[1]/8051B_GPIO_P1[1]	N21	VDD12	AA6	G_FPD[18]	AJ6	DVDD18
E7	VSS	N25	DCD5#/GPIO_P0[0]/8051A_GPIO_P0[0]/MC0[0]/8051B_GPIO_P0[0]/MC_SPI2_CS#	AA10	VSS	AJ7	VSS
E8	DTR6#/GPIO_P1[5]/8051A_GPIO_P1[5]/MC1[4]/8051B_GPIO_P1[5]	N26	SIN1/GPIO_P4[4]/8051A_GPIO_P4[4]/MC4[5]/8051B_GPIO_P4[4]	AA11	VSS	AJ8	DRAMCLK
E9	IDE_PIOR#/GPIO_P8[4]/SD1_ACTIVE/MC9[5]/8051B_GPIO_P8[4]/SIN9/SLCIN	N27	RI5#/GPIO_P0[3]/8051A_GPIO_P0[3]/MC0[3]/8051B_GPIO_P0[3]/MC_SPI2_DI	AA12	VDD10	AJ9	MA[4]
E10	VSS	N28	AVSS_USBBAS33	AA13	VDD10	AJ10	MA[9]
E11	IDE_PINT/GPIO_P8[0]/MC9[0]/8051B_GPIO_P8[0]/DCD9#/SLCT	N29	VSS	AA14	VDD10	AJ11	CAS#
E12	PWM_CLK/GPIO_P5[0]/MC5[0]/8051B_GPIO_P5[0]/DCD2#	N30	SATA_CLKN	AA15	VDD10	AJ12	VSS
E13	VSS	P1	G_IOG	AA16	VSS	AJ13	WE#
E14	H_BCLK/GPIO_PA[4]/GSF_CLK	P2	AVSS_DACG18	AA17	VDD33	AJ14	DRAMCLK1
E15	VSS	P3	AVDD_DACG18	AA18	VDD33	AJ15	MD[16]
E16	ADC_VSS33D	P4	VDD_DAC10	AA19	VDD33	AJ16	VSS
E17	ADC_VCC33A	P5	AVSS_VDISPLL18	AA20	VSS	AJ17	DQS#[2]
E18	ADC_VCC33A_VREFP	P6	AVDD_VDISPLL18	AA21	VSS	AJ18	MD[21]
E19	ADC_IN7	P10	VDD33	AA25	SYSCLK	AJ19	VSS
E20	ADC_IN5	P11	VSS	AA26	VSS	AJ20	SD[12]
E21	VSS18A_TEMP	P12	VSS	AA27	SD[14]	AJ21	XOUT_14318
E22	VSS	P13	VSS	AA28	IRQ[7]	AJ22	VSS
E23	RTS7#/GPIO_P2[2]/8051A_GPIO_P2[2]/MC2[2]/8051B_GPIO_P2[2]/ISA_SA[26]	P14	VSS	AA29	DACK#[3]	AJ23	SD[4]
E24	PE0_CLKN	P15	VSS	AA30	SYSFAILOUT#	AJ24	SD[0]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
E25	PE0_CLKP	P16	VSS	AB1	G_FPD[11]	AJ25	VSS
E26	RI7#/GPIO_P2[3]/8051A_GPIO_P2[3]/MC2[3]/8051B_GPIO_P2[3]/ISA_SA[27]	P17	VSS	AB2	VDD33	AJ26	SA[1]
E27	DTR7#/GPIO_P2[5]/8051A_GPIO_P2[5]/MC2[4]/8051B_GPIO_P2[5]/ISA_SA[29]	P18	VSS	AB3	G_FPD[12]	AJ27	SA[5]
E28	AVDD2_USB12	P19	VSS	AB4	G_VSYNC	AJ28	SA[8]
E29	USB2_DP	P20	VDD12	AB5	G_FPD[2]	AJ29	SA[14]
E30	USB2_DM	P21	VDD12	AB6	VDD33	AJ30	SA[10]
F1	E_SPI_CS#/GPIO_P3[0]/8051A_GPIO_P3[0]/MC_SPI1_CS#/8051B_GPIO_P3[0]/DCD8#	P25	RI1#/GPIO_P4[3]/8051A_GPIO_P4[3]/MC4[3]/8051B_GPIO_P4[3]	AB25	MEMW#	AK1	AK1_NC
F2	RTC_RD#/GPIO_P3[6]/8051A_GPIO_P3[6]/COM3_TXDEN/DSR8#/I2C1_SCL	P26	VSS	AB26	IRQ[10]	AK2	VSS
F3	TDO	P27	DTR5#/GPIO_P0[5]/8051A_GPIO_P0[5]/MC0[4]/8051B_GPIO_P0[5]/8051B_TXDEN1	AB27	IRQ[15]	AK3	DQS#[1]
F4	IDE_PDD[5]/GPIO_P6[5]/SD_DATA[1]/MC6[4]/8051B_GPIO_P6[5]/DTR3#	P28	VSS	AB28	VSS	AK4	DQS[1]
F5	VSS	P29	AVDD_SATA33	AB29	SPEAKER	AK5	VSS
F6	I_XIN_25M	P30	SATA_CLKP	AB30	CLK25MOUT	AK6	MD[13]
F7	RTS6#/GPIO_P1[2]/8051A_GPIO_P1[2]/MC1[2]/8051B_GPIO_P1[2]	R1	G_IOB	AC1	G_FPD[0]	AK7	MD[15]
F8	IDE_PA[0]/GPIO_P8[1]/MC9[1]/8051B_GPIO_P8[1]/SOUT9/PE	R2	AVSS_DACB18	AC2	VSS	AK8	DRAMCLK#
F9	IDE_PA[2]/GPIO_P8[3]/MC9[3]/8051B_GPIO_P8[3]/RI9#/ACK#	R3	AVDD_DACB18	AC3	G_FPD[8]	AK9	MA[7]
F10	IDE_PA[1]/GPIO_P8[2]/MC9[2]/8051B_GPIO_P8[2]/RTS9#/BUSY	R4	VSS	AC4	G_FP1VS	AK10	VSS
F11	IDE_PIOW#/GPIO_P8[5]/SD_ACTIVE/MC9[4]/8051B_GPIO_P8[5]/DTR9#/INIT#	R5	AVSS_CPUPLL18	AC5	G_FPD[15]	AK11	MA[3]
F12	IDE_PCS0#/GPIO_P8[6]/MCB[2]/8051B_GPIO_P8[6]/DSR9#/ERR#	R6	AVDD_CPUPLL18	AC6	G_FPD[7]	AK12	MA[1]
F13	IDE_PCS1#/GPIO_P8[7]/MCB[3]/8051B_GPIO_P8[7]/CTS9#/AFD#	R10	VSS	AC25	BALE	AK13	BA[2]
F14	H_SDO/GPIO_PA[2]/GSF_CH1	R11	VSS	AC26	IRQ[12]	AK14	DRAMCLK#1
F15	H_RST#/GPIO_PA[0]/PWM2_GATE	R12	VSS	AC27	DRQ[7]	AK15	VSS
F16	ADC_VCC33D	R13	VSS	AC28	IRQ[14]	AK16	MD[18]
F17	ADC_IN3	R14	VDD18	AC29	LA[23]	AK17	DQS[2]
F18	ADC_IN0	R15	VSS	AC30	VSS	AK18	MD[20]
F19	ADC_IN6	R16	VSS	AD1	G_FP1HS	AK19	MD[22]
F20	ADC_IN4	R17	VSS	AD2	G_FP1CLK	AK20	VSS
F21	VCC18A_TEMP	R18	VSS	AD3	G_FPD[4]	AK21	XIN_14318
F22	DCD7#/GPIO_P2[0]/8051A_GPIO_P2[0]/MC2[0]/8051B_GPIO_P2[0]/ISA_SA[24]	R19	VSS	AD4	G_ENBLT	AK22	SD[6]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
F23	CTS7#/GPIO_P2[7]/8051A_GPIO_P2[7]/MC3[5]/8051B_GPIO_P2[7]/ISA_SA[31]	R20	VSS	AD5	VSS	AK23	SD[7]
F24	SOUT7/GPIO_P2[1]/8051A_GPIO_P2[1]/MC2[1]/8051B_GPIO_P2[1]/ISA_SA[25]	R21	VSS	AD6	VDD33	AK24	SD[1]
F25	VSS	R25	CTS1#/GPIO_P4[7]/8051A_GPIO_P4[7]/MC7[1]/8051B_GPIO_P4[7]	AD25	GPCS1#	AK25	SA[2]
F26	SIN7/GPIO_P2[4]/8051A_GPIO_P2[4]/MC2[5]/8051B_GPIO_P2[4]/ISA_SA[28]	R26	SOUT1/GPIO_P4[1]/8051A_GPIO_P4[1]/MC4[1]/8051B_GPIO_P4[1]	AD26	DRQ[0]	AK26	SA[0]
F27	VSS	R27	RTS1#/GPIO_P4[2]/8051A_GPIO_P4[2]/MC4[2]/8051B_GPIO_P4[2]	AD27	SA[17]	AK27	SA[3]
F28	USB_REXT2	R28	DCD1#/GPIO_P4[0]/8051A_GPIO_P4[0]/MC4[0]/8051B_GPIO_P4[0]	AD28	LA[21]	AK28	SA[6]
F29	AVSS2_USB33	R29	AVSS_SATAPLL12	AD29	VSS	AK29	SA[12]
F30	AVDD2_USB33	R30	AVDD_SATAPLL12	AD30	CLK24MOUT	AK30	AK30_NC

4.3. Pin List Table

Function	Symbol	PIN Sum
SYSTEM	PWRGOOD, CLK25MOUT, XOUT_14318, XIN_14318, SPEAKER, CLK24MOUT, PCIRST#, STRAP_DDR (GNT) x 3 PINs	10 PINs
Internal Connection	I_XIN_25M, G_XIN_14318	2 PINs
DDRII Interface	DRAMCLK, DRAMCLK#, DRAMCLK1, DRAMCLK#1,RAS#, CAS#, WE#, CKE,CS1#, CS0#, DQM[3:0], DQS[3:0], DQS#[3:0], ODT[1], ODT[0], OCDBIAS, OCDBIAS1, VREF, BA[2:0],MD[31:0], MA[14:0]	77 PINs
USB Interface	USB_DP,USB_DM, USB1_DP, USB1_DM, USB2_DP, USB2_DM, USB3_DP, USB3_DM USB_REXT, USB_REXT1, USB_REXT2, USB_REXT3	12 PINs
ISA Bus Interface	IOCHCK#, SD[15:0], IOCHRDY, AEN, SA[19:0], SBHE#, LA[23:17], MEMR#, MEMW#, RST_DRV, IRQ[15:14], IRQ[12:9], IRQ[7:3], DRQ[7:5], DRQ[3:0], 0WS#, SMEMR#, SMEMW#, IOW#, IOR#, DACK#[7:5], DACK#[3:0], REFRESH#, SYSCLK, TC, BALE, MEMCS16#,IOCS16#, OSC14318	87 PINs
Chip Selection	GPCS0#/ STRAP_PLL, GPCS1#/ STRAP_PLL1_SEL	2 PINs
SPI Interface	SPI_CS#/ROM_CS#/ STRAP_BMS, SPI_CK/STRAP_JTAG, SPI_DO/STRAP_FLASH_SEL, SPI_DI	4 PINs
Redundant	EXTSYSFAILIN#, SYSFAILOUT#, EXT_SWITCH_FAIL#, EXT_GPCS#	4 PINs
KBD / MOUSE Interface	KBCLK/KBRST#, KBDAT/A20GATE#, MSCLK, MSDAT	4 PINs
RTC Interface	RTC_PS, RTC_XOUT, RTC_XI	3 PINs
PCIE Bus Interface	PE0_CLKP, PE0_CLKN, PE0_TXP, PE0_TXN, PE0_RXP, PE0_RXN, PE1_TXP, PE1_TXN, PE1_RXP, PE1_RXN, DIF0_PCIE_PLLCLK100_P,	16 PINs

Function	Symbol	PIN Sum
	DIF0_PCIE_PLLCLK100_N, DIF2_CLK100_P, DIF2_CLK100_N, DIF3_CLK100_P, DIF3_CLK100_N	
INTERNAL SPI CONTROL	PADWPB, PADHOLDB	2 PINs
JTAG Interface	TDO, TMS, TCK, TDI	4 PINs
GPIO P0/ MC3[1-0], MC0[4, 5, 3-0]/ 8051A P0/ COM5/ 8051B P0/ 8051B [TXD1, RXD1]/ 8051B[TXDEN1, TXDEN2]/ FD-SPI2	DCD5#/GPIO_P0[0]/8051A_GPIO_P0[0]/MC0[0]/8051B_GPIO_P0[0]/MC_SPI2_CS#, SOUT5/GPIO_P0[1]/8051A_GPIO_P0[1]/MC0[1]/8051B_GPIO_P0[1]/MC_SPI2_CLK, RTS5#/GPIO_P0[2]/8051A_GPIO_P0[2]/MC0[2]/8051B_GPIO_P0[2]/MC_SPI2_DO, RI5#/GPIO_P0[3]/8051A_GPIO_P0[3]/MC0[3]/8051B_GPIO_P0[3]/MC_SPI2_DI, SIN5/GPIO_P0[4]/8051A_GPIO_P0[4]/MC0[5]/8051B_GPIO_P0[4]/8051B_TXDEN2, DTR5#/GPIO_P0[5]/8051A_GPIO_P0[5]/MC0[4]/8051B_GPIO_P0[5]/8051B_TXDEN1, DSR5#/GPIO_P0[6]/8051A_GPIO_P0[6]/MC3[0]/8051B_GPIO_P0[6]/8051B_SIN1, CTS5#/GPIO_P0[7]/8051A_GPIO_P0[7]/MC3[1]/8051B_GPIO_P0[7]/8051B_SOUT1	8 PINs
GPIO P1/ MC3[3-2], MC1[4, 5, 3-0]/ 8051A P1/ COM6/ 8051B P1	DCD6#/GPIO_P1[0]/8051A_GPIO_P1[0]/MC1[0]/8051B_GPIO_P1[0], SOUT6/GPIO_P1[1]/8051A_GPIO_P1[1]/MC1[1]/8051B_GPIO_P1[1], RTS6#/GPIO_P1[2]/8051A_GPIO_P1[2]/MC1[2]/8051B_GPIO_P1[2], RI6#/GPIO_P1[3]/8051A_GPIO_P1[3]/MC1[3]/8051B_GPIO_P1[3], SIN6/GPIO_P1[4]/8051A_GPIO_P1[4]/MC1[5]/8051B_GPIO_P1[4], DTR6#/GPIO_P1[5]/8051A_GPIO_P1[5]/MC1[4]/8051B_GPIO_P1[5], DSR6#/GPIO_P1[6]/8051A_GPIO_P1[6]/MC3[2]/8051B_GPIO_P1[6], CTS6#/GPIO_P1[7]/8051A_GPIO_P1[7]/MC3[3]/8051B_GPIO_P1[7]	8 PINs
GPIO P2/ SA[31-24]/ MC3[5-4], MC2[4, 5, 3-0]/ 8051A P2[7-0]/ COM7/ 8051B P2	DCD7#/GPIO_P2[0]/8051A_GPIO_P2[0]/MC2[0]/8051B_GPIO_P2[0]/ISA_SA[24], SOUT7/GPIO_P2[1]/8051A_GPIO_P2[1]/MC2[1]/8051B_GPIO_P2[1]/ISA_SA[25], RTS7#/GPIO_P2[2]/8051A_GPIO_P2[2]/MC2[2]/8051B_GPIO_P2[2]/ISA_SA[26], RI7#/GPIO_P2[3]/8051A_GPIO_P2[3]/MC2[3]/8051B_GPIO_P2[3]/ISA_SA[27], SIN7/GPIO_P2[4]/8051A_GPIO_P2[4]/MC2[5]/8051B_GPIO_P2[4]/ISA_SA[28], DTR7#/GPIO_P2[5]/8051A_GPIO_P2[5]/MC2[4]/8051B_GPIO_P2[5]/ISA_SA[29], DSR7#/GPIO_P2[6]/8051A_GPIO_P2[6]/MC3[4]/8051B_GPIO_P2[6]/ISA_SA[30], CTS7#/GPIO_P2[7]/8051A_GPIO_P2[7]/MC3[5]/8051B_GPIO_P2[7]/ISA_SA[31]	8 PINs
GPIO P3[3-0]/ 8051A P3[3-0]/ FD-SPI1/ 8051B P3[3-0]/ COM8[RI, RTS, SOUT, DCD]/ Ext SPI	E_SPI_CS#/GPIO_P3[0]/8051A_GPIO_P3[0]/MC_SPI1_CS#/8051B_GPIO_P3[0]/DCD8#, E_SPI_CLK/GPIO_P3[1]/8051A_GPIO_P3[1]/MC_SPI1_CLK/8051B_GPIO_P3[1]/SOUT8/ 8051B_SOUT2, E_SPI_DO/GPIO_P3[2]/8051A_GPIO_P3[2]/MC_SPI1_DO/8051B_GPIO_P3[2]/RTS8#, E_SPI_DI/GPIO_P3[3]/8051A_GPIO_P3[3]/MC_SPI1_DI/8051B_GPIO_P3[3]/RI8#	4 PINs
GPIO P3[7-4]/ I2C/I2C1/ TXDEN[4-3]/ 8051B TXD2, RXD2/ 8051B P3[5-4]/ 8051A P3[7-4]/ COM8[CTS, DSR, DTR, SIN]/ Ext RTC	RTC_IRQ8#/GPIO_P3[4]/8051A_GPIO_P3[4]/8051B_SIN2/8051B_GPIO_P3[4]/SIN8/I2C_SCL, RTC_WR#/GPIO_P3[5]/8051A_GPIO_P3[5]/8051B_SOUT2/8051B_GPIO_P3[5]/DTR8#/I2C_SDA, RTC_RD#/GPIO_P3[6]/8051A_GPIO_P3[6]/COM3_TXDEN/DSR8#/I2C1_SCL, RTC_AS/GPIO_P3[7]/8051A_GPIO_P3[7]/COM4_TXDEN/CTS8#/I2C1_SDA	4 PINs
COM1/ GPIO P4/ MC7[1-0], MC4[4,5,3-0]/ 8051A P4/ 8051B P4	DCD1#/GPIO_P4[0]/8051A_GPIO_P4[0]/MC4[0]/8051B_GPIO_P4[0], SOUT1/GPIO_P4[1]/8051A_GPIO_P4[1]/MC4[1]/8051B_GPIO_P4[1], RTS1#/GPIO_P4[2]/8051A_GPIO_P4[2]/MC4[2]/8051B_GPIO_P4[2], RI1#/GPIO_P4[3]/8051A_GPIO_P4[3]/MC4[3]/8051B_GPIO_P4[3], SIN1/GPIO_P4[4]/8051A_GPIO_P4[4]/MC4[5]/8051B_GPIO_P4[4], DTR1#/GPIO_P4[5]/8051A_GPIO_P4[5]/MC4[4]/8051B_GPIO_P4[5], DSR1#/GPIO_P4[6]/8051A_GPIO_P4[6]/MC7[0]/8051B_GPIO_P4[6], CTS1#/GPIO_P4[7]/8051A_GPIO_P4[7]/MC7[1]/8051B_GPIO_P4[7]	8 PINs

Function	Symbol	PIN Sum
COM2/ PWM/ GPIO P5/ MC7[3-2], MC5[4,5,3-0] 8051B P5	PWM_CLK/GPIO_P5[0]/MC5[0]/8051B_GPIO_P5[0]/DCD2#, PWM_OUT/GPIO_P5[1]/MC5[1]/8051B_GPIO_P5[1]/SOUT2, PWM1_OUT/GPIO_P5[2]/MC5[2]/8051B_GPIO_P5[2]/RTS2#, PWM1_CLK/GPIO_P5[3]/MC5[3]/8051B_GPIO_P5[3]/RI2#, PWM2_CLK/GPIO_P5[4]/MC5[5]/8051B_GPIO_P5[4]/SIN2, PWM2_OUT/GPIO_P5[5]/MC5[4]/8051B_GPIO_P5[5]/DTR2#, PWM_GATE/GPIO_P5[6]/MC7[2]/8051B_GPIO_P5[6]/DSR2#, PWM1_GATE/GPIO_P5[7]/MC7[3]/8051B_GPIO_P5[7]/CTS2#	8 PINs
IDE PDD[7-0]/ SD/ COM3/ GPIO P6/ MC7[5-4], MC6[4,5,3-0]/ 8051B P6	IDE_PDD[0]/GPIO_P6[0]/SD_DATA[2]/MC6[0]/8051B_GPIO_P6[0]/DCD3#, IDE_PDD[1]/GPIO_P6[1]/SD_DATA[3]/MC6[1]/8051B_GPIO_P6[1]/SOUT3, IDE_PDD[2]/GPIO_P6[2]/SD_CMD/MC6[2]/8051B_GPIO_P6[2]/RTS3#, IDE_PDD[3]/GPIO_P6[3]/SD_CLK/MC6[3]/8051B_GPIO_P6[3]/RI3#, IDE_PDD[4]/GPIO_P6[4]/SD_DATA[0]/MC6[5]/8051B_GPIO_P6[4]/SIN3, IDE_PDD[5]/GPIO_P6[5]/SD_DATA[1]/MC6[4]/8051B_GPIO_P6[5]/DTR3#, IDE_PDD[6]/GPIO_P6[6]/SD_CD/MC7[4]/8051B_GPIO_P6[6]/DSR3#, IDE_PDD[7]/GPIO_P6[7]/SD_WP/MC7[5]/8051B_GPIO_P6[7]/CTS3#	8 PINs
IDE PDD[15-8] SD1/ COM4/ GPIO P7/ MCB[1-0], MC8[4, 5, 3-0]/ 8051B P7	IDE_PDD[8]/GPIO_P7[0]/SD1_DATA[2]/MC8[0]/8051B_GPIO_P7[0]/DCD4#, IDE_PDD[9]/GPIO_P7[1]/SD1_DATA[3]/MC8[1]/8051B_GPIO_P7[1]/SOUT4, IDE_PDD[10]/GPIO_P7[2]/SD1_CMD/MC8[2]/8051B_GPIO_P7[2]/RTS4#, IDE_PDD[11]/GPIO_P7[3]/SD1_CLK/MC8[3]/8051B_GPIO_P7[3]/RI4#, IDE_PDD[12]/GPIO_P7[4]/SD1_DATA[0]/MC8[5]/8051B_GPIO_P7[4]/SIN4, IDE_PDD[13]/GPIO_P7[5]/SD1_DATA[1]/MC8[4]/8051B_GPIO_P7[5]/DTR4#, IDE_PDD[14]/GPIO_P7[6]/SD1_CD/MCB[0]/8051B_GPIO_P7[6]/DSR4#, IDE_PDD[15]/GPIO_P7[7]/SD1_WP/MCB[1]/8051B_GPIO_P7[7]/CTS4#	8 PINs
IDE CTRL 1/ LPT 1/2 Control COM9/ GPIO P8/ MCB[3-2], MC9[4, 5, 3-0]/ 8051B P8	IDE_PINT/GPIO_P8[0]/MC9[0]/8051B_GPIO_P8[0]/DCD9#/SLCT, IDE_PA[0]/GPIO_P8[1]/MC9[1]/8051B_GPIO_P8[1]/SOUT9/PE, IDE_PA[1]/GPIO_P8[2]/MC9[2]/8051B_GPIO_P8[2]/RTS9#/BUSY, IDE_PA[2]/GPIO_P8[3]/MC9[3]/8051B_GPIO_P8[3]/RI9#/ACK#, IDE_PIOR#/GPIO_P8[4]/SD1_ACTIVE/MC9[5]/8051B_GPIO_P8[4]/SIN9/SLCIN, IDE_PIOW#/GPIO_P8[5]/SD_ACTIVE/MC9[4]/8051B_GPIO_P8[5]/DTR9#/INIT#, IDE_PCS0#/GPIO_P8[6]/MCB[2]/8051B_GPIO_P8[6]/DSR9#/ERR#, IDE_PCS1#/GPIO_P8[7]/MCB[3]/8051B_GPIO_P8[7]/CTS9#/AFD#	8 PINs
USB Device/ IDE Control 2/ MTBF/ WDT_RSTB/ GPIO P9/ MCB[5-4],MCA[4,5,3-0]/ 8051B P9/ LPT Data[7-0]	UD_DM/GPIO_P9[0]/MCA[0]/8051B_GPIO_P9[0]/PD[0], UD_DP/GPIO_P9[1]/MCA[1]/8051B_GPIO_P9[1]/PD[1], IDE_PRST#/GPIO_P9[2]/MCA[2]/8051B_GPIO_P9[2]/PD[2], IDE_PCBLID#/GPIO_P9[3]/MCA[3]/8051B_GPIO_P9[3]/PD[3], IDE_PDACK#/GPIO_P9[4]/MCA[5]/8051B_GPIO_P9[4]/PD[4], IDE_PIORDY/GPIO_P9[5]/MCA[4]/8051B_GPIO_P9[5]/PD[5], IDE_PDRQ/GPIO_P9[6]/MCB[4]/8051B_GPIO_P9[6]/PD[6], MTBF/GPIO_P9[7]/MCB[5]/8051B_GPIO_P9[7]/WDT_RSTB/PD[7]	8 PINs
HD Audio/ Parallel Port control 1/ COM 1 control/ COM 2 control/ GPIO PORT A/ PWM2 gate/ General Shift Interface	H_RST#/GPIO_PA[0]/PWM2_GATE, H_SDI/GPIO_PA[1]/GSF_CH0, H_SDO/GPIO_PA[2]/GSF_CH1, H_SYNC/GPIO_PA[3]/GSF_CH2, H_BCLK/GPIO_PA[4]/GSF_CLK, STB#/GPIO_PA[5], TX_DEN2/GPIO_PA[6], TX_DEN1/GPIO_PA[7]	8 PINs
SATA Interface	SATA_CLKP, SATA_CLKN, SATA_TXP, SATA_TXN, SATA_RXP, SATA_RXN, DIF1_SATA_PHY_CLK_P, DIF1_SATA_PHY_CLK_N	8 PINs
Ethernet Interface	LINK/ACTIVE, DUPLEX, ISET, ATSTP, ATSTN, TXN, TXP, RXN, RXP MDC,MDIO, COL, RXC, RXD[3:0], RXDV, TXC, TXD[3:0], TXEN	24 PINs
ADC Interface	ADC_IN0, ADC_IN1, ADC_IN2, ADC_IN3, ADC_IN4, ADC_IN5, ADC_IN6, ADC_IN7, VTEMP_TST	9 PINs
VGA DVO Interface	G_FPD[0]/G_TVD[0], G_FPD[1]/G_TVD[1], G_FPD[2]/G_TVD[2], G_FPD[3]/G_TVD[3], G_FPD[4]/G_TVD[4], G_FPD[5]/G_TVD[5], G_FPD[6]/G_TVD[6], G_FPD[7]/G_TVD[7], G_FPD[8]/G_TVD[8], G_FPD[9]/G_TVD[9], G_FPD[10]/G_TVD[10], G_FPD[11]/G_TVD[11], G_FP1DE/G_TVDE, G_FP1HS/G_TVHS, G_FP1VS/G_TVVS, G_FP1CLK/G_TVCLKO, G_TVCLKIN, G_FP1DET/G_TVDET, G_FPD[12]/G_CAPD[0], G_FPD[13]/G_CAPD[1],	33 PINs

Function	Symbol	PIN Sum
	G_FPD[14]/G_CAPD[2], G_FPD[15]/G_CAPD[3], G_FPD[16]/G_CAPD[4], G_FPD[17]/G_CAPD[5], G_FPD[18]/G_CAPD[6], G_FPD[19]/G_CAPD[7], G_FPD[20]/G_CAPFILD, G_FPD[21]/G_CAPHS, G_FPD[22]/G_CAPVS, G_FPD[23]/G_CAPCLK, G_ENVDD, G_ENBLT, G_ENVEE	
VGA DAC Interface	G_REXT, G_IOR, G_IOG, G_IOB, G_VSYNC, G_HSYNC	6 PINs
VGA GPIO Interface	G_GPIO[2], G_GPIO[3]	2 PINs
VGA I2C Interface	G_DDC1_CLK, G_DDC1_DAT, G_DDC_CLK, G_DDC_DAT	4 PINs
VGA Power Interface	AVDD_DACR18, AVSS_DACR18, AVDD_DACG18, AVSS_DACG18, AVDD_DACB18, AVSS_DACB18, AVDD_DACBG18, AVSS_DACBG18, AVDD_VDISPLL18, AVSS_VDISPLL18, VDD_DAC10	11 PINs
PCIE Power Interface	AVDD1_PE33, AVDD_PE12, AVDD1_PE12, AVDD_PERX12, AVSS_PERX12, AVDD1_PERX12, AVSS1_PERX12, AVDD1_PEPLL12, AVSS1_PEPLL12, AVSS_PEPLL12, AVSS_PE, AVSS1_PE	12 PINs
SATA Power Interface	AVSS_SATA, AVDD_SATA12, AVSS_SATARX12, AVDD_SATARX12, AVDD_SATAPLL12, AVSS_SATAPLL12, AVDD_SATA33	7 PINs
USB Power Interface	AVDD_USB33, AVSS_USB33, AVDD1_USB33, AVSS1_USB33, AVDD2_USB33, AVSS2_USB33, AVDD3_USB33, AVSS3_USB33, AVDD_USBBAS33, AVSS_USBBAS33, AVDD2_USBBAS33, AVSS2_USBBAS33, AVDD_USB12, AVDD1_USB12, AVDD2_USB12, AVDD3_USB12, AVDD_USBPLL12, AVSS_USBPLL12, AVDD1_USBPLL12, AVSS1_USBPLL12, AVDD2_USBPLL12, AVSS2_USBPLL12, AVDD3_USBPLL12, AVSS3_USBPLL12	24 PINs
ADC Power Interface	ADC_VCC33A_VREFP, ADC_VSS33A, ADC_VSS33D, VCC18A_TEMP, VCC18D_TEMP, VCC18A_PLL5, VCC18A_PLL7	7 PINs
Battery Power	RTC_VDD33, RTC_VSS	2 PINs
1.0V Power	VDD10 (15 PINs)	15 PINs
1.2V Power	VDD12 (12 PINs), DIF_VD12IO (4 PINs), DIF_VS12IO (4 PINs), AFE_VCCDL12	21 PINs
1.8V Power	VDD18 (11 PINs), DVDD18(13 PINs), AVDD_DDRPLL18, AVSS_DDRPLL18, AVDD_CPUPLL18, AVSS_CPUPLL18, AFE_VCCABG18, AFE_VCCAPLL18, AFE_VCCD18, AFE_RXVCCA18	32 PINs
3.3V Power	VDD33(18 PINs)	18 PINs
Digital Ground	VSS	153 PINs
Analogue Ground	AFE_VSSDL, AFE_TXVSSA, AFE_RXVSSA, AFE_VSSD, AFE_VSSAPLL, AFE_VSSABG, ADC_VSS33A_VREFN, ADC_VSS33A, ADC_VSS33D, VSS18A_TEMP, VSS18D_TEMP, VSS18A_PLL5, VSS18A_PLL7	13 PINs
NC pin	NC	4 PINs

4.4. Signal Description

This chapter provides a detailed description of SoC signals. A signal with the symbol "#" at the end of itself indicates that this pin is low active. Otherwise, it is high active.

The following notations are used to describe the signal types:

I Input pin

O Output pin

OD Output pin with open-drain

I/O Bi-directional Input/Output pin

- **System (10 PINs)**

PIN No.	Symbol	Type	Description
M3	PWRGOOD	I	***Power-Good Input.*** This signal comes from Power Good of the power supply to indicate that the power is available. The SoC uses this signal to generate reset sequence for the system.
AB30	CLK25MOUT	O	***25MHz Clock output.***
AD30	CLK24MOUT	O	***24MHz Clock output***
AJ21	XOUT_14318	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator).
AK21	XIN_14318	I	***Crystal-in.*** 14.318MHz frequency input, within a tolerance range of ± 30 ppm to the amplifier (oscillator).
AB29	SPEAKER	O	***Speaker Output.*** This pin is used to control the Speaker Output and should be connected to the Speaker
	STRAP_EPS	I	***Ethernet PHY Select*** Pull it low to select internal PHY. Pull it high to select External PHY. Tri-state to select Internal PHY AFE-test Mode. Default internal tri-state.
C1,A2,B1	STRAP_DDR(GNT)	I	***DDRII Clock Table*** STRAP_DDR (PGNT) [2:0] / Frequency(MHz) 3'b000 / 166 3'b001 / 200 3'b010 / 233 3'b011 / 266 3'b100 / 300 3'b101 / 333 3'b110 / 366 3'b111 / 400 (not suggest)
C2	PCIRST#	I	***PCI Reset.*** The 1.8V PCI Reset pin, is used to reset PCI devices. When it is asserted low, all the PCI devices will be reset.

- **Internal Connection between NB and SB (2 PIN)**

PIN No.	Symbol	Type	Description
F6	I_XIN_25M	O	***Internal connect pin.*** This signal is used to connect with the associated NB and SB pins.
H6	G_XIN_14318	O	***Internal connect pin.*** This signal is used to connect with the associated NB and SB pins.

- **PCI Bus Interface (4 PINs)**

- **DDRII Interface (77 PINs)**

PIN No.	Symbol	Type	Description
AJ8 AJ14	DRAMCLK DRAMCLK1	O	***Clock output.*** This pin provides the fundamental timing for the DDRII controller.
AK8 AK14	DRAMCLK# DRAMCLK#1	O	***Clock output.*** This pin provides the fundamental timing for the DDRII controller.
AG12	RAS#	O	***Row Address Strobe.*** When asserted, this signal latches row address on positive edge of the DDRII clock. This signal also allows row access and pre-charge.
AJ11	CAS#	O	***Column Address Strobe.*** When asserted, this signal latches column address on the positive edge of the DDRII clock. This signal also allows column access and pre-charge.
AJ13	WE#	O	***Memory Write Enable.*** This pin is used as a write enable for the memory data bus.
AF14	CKE	O	***Clock Enable.*** CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers.
AF10 AE14	CS1# CS0#	O	***Chip Select CS1# & CS0#.*** These two pins activate the DDRII devices. First Bank of DDRII accepts any command when the CS0# pin is active low. Second Bank of DDRII accepts any command when the CS1# pin is active low.
AE17,AH18, AJ3,AF5	DQM[3:0]	O	***Data Mask DQM[3:0].*** These pins act as synchronized output enables during read cycles and byte masks during write cycles.

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>AE18,AK17,
AK4,AG2</td><td>DQS[3:0]</td><td>I/O</td><td>Data Strobe DQS[3:0] for DDRII only. Output with write data, input with the read data for source synchronous operation.</td></tr>
<tr><td>AF18,AJ17,
AK3,AG3</td><td>DQS#[3:0]</td><td>I/O</td><td>Data Strobe DQS#[3:0] for DDRII only. Output with write data, input with the read data for source synchronous operation.</td></tr>
<tr><td>AG14</td><td>ODT[0]</td><td>O</td><td>On Die Termination Control for DDRII only. ODT(registered HIGH) enables on die termination resistance internal to the DDR2 SDRAM.</td></tr>
<tr><td rowspan="2">AF13</td><td>ODT[1]</td><td>O</td><td>On Die Termination Control for DDRII only. ODT(registered HIGH) enables on die termination resistance internal to the DDR2 SDRAM.</td></tr>
<tr><td>STRAP1_DDR</td><td>I</td><td>DRAM Freq Option (ODT[1])
DDRII clock select.
<table>
<tr><td>ODT[1],PGNT[2:0]</td><td>Frequency(MHz)</td></tr>
<tr><td>4’b0000</td><td>166</td></tr>
<tr><td>4’b0001</td><td>200</td></tr>
<tr><td>4’b0010</td><td>233</td></tr>
<tr><td>4’b0011</td><td>266</td></tr>
<tr><td>4’b0100</td><td>300</td></tr>
<tr><td>4’b0101</td><td>333</td></tr>
<tr><td>4’b0110</td><td>366</td></tr>
<tr><td>4’b0111</td><td>400 (not suggest)</td></tr>
</table></td></tr>
<tr><td>AE6
AE21</td><td>OCDBIAS
OCDBIAS1</td><td>I</td><td>OCD BIAS for DDRII only. The OCD bias circuit generates a bias level voltage that makes the reference resistance for driver impedance calibration an appropriate value</td></tr>
<tr><td>AE11</td><td>VREF</td><td>I</td><td>Reference voltage for DDRII only. Reference voltage for inputs for SSTL interface.</td></tr>
<tr><td>AK13,AE13,
AH13</td><td>BA[2:0]</td><td>O</td><td>Bank Address BA[2:0]. These pins are connected to DDRII as bank address pins.</td></tr>
<tr><td>AF20,AE19,AG19,AG18,AG17,AG16,AF16,AG15,AH19,AK19,AJ18,AK18,AH16,AK16,AH15,AJ15,AK7,AH7,AK6,AJ5,AJ2,AJ1,AH1,AH2,AH4,AH6,AH5,AG6,AG4,AF1,AF2,AF4</td><td>MD[31:0]</td><td>I/O</td><td>Memory Data MD[31:0]. These pins are connected to the DDRII data bus.</td></tr>
</table>

PIN No.	Symbol	Type	Description
AF9,AH8,AF8,AH9,AH12,AJ10,AG8,AK9,AG9,AH11,AJ9,AK11,AH10,AK12,AG11	MA[14:0]	O	***Memory Address MA[14-0].*** Normally, these pins are used as the row and column address for DDRII.

- **USB Interface (12 PINs)**

PIN No.	Symbol	Type	Description
L29 L30	USB_DP USB_DM	I/O	Universal Serial Bus Controller 0 Port 0. These are the serial data pair for USB Port 0. 15kΩ pull down resistors are connected to DP and DM internally.
H29 H30	USB1_DP USB1_DM	I/O	Universal Serial Bus Controller 0 Port 1. These are the serial data pair for USB Port 1. 15kΩ pull down resistors are connected to DP and DM internally.
E29 E30	USB2_DP USB2_DM	I/O	Universal Serial Bus Controller 1 Port 0. These are the serial data pair for USB Port 2. 15kΩ pull down resistors are connected to DP and DM internally.
B29 B30	USB3_DP USB3_DM	I/O	Universal Serial Bus Controller 1 Port 1. These are the serial data pair for USB Port 3. 15kΩ pull down resistors are connected to DP and DM internally.
M28	USB_REXT	I	Universal Serial Bus Controller 0 External Reference Resistance 12kΩ ±1%
K28	USB_REXT1	I	Universal Serial Bus Controller 1 External Reference Resistance 12kΩ ±1%
F28	USB_REXT2	I	Universal Serial Bus Controller 2 External Reference Resistance 12kΩ ±1%
D28	USB_REXT3	I	Universal Serial Bus Controller 3 External Reference Resistance 12kΩ ±1%

- **ISA Bus Interface (87 PINs)**

PIN No.	Symbol	Type	Description
W27	IOCHCK#	I	**I/O Channel Check**. Provides the system board with parity (error) information about memory or devices on the I/O channel.
W26,AA27,V27,AJ20,AH21,AG21,AH22,AG22,AK23,AK22,AH23,AJ23,AH24,AG24,AK24,AJ24	SD[15:0]	I/O	**ISA high and low byte slot data bus**. These are the system data lines. These signals read data and vectors into CPU during memory or I/O read cycles or interrupt acknowledge cycles and outputs data from CPU during memory or I/O write cycles.
Y20	IOCHRDY	I/O	**ISA system ready**. This input signal is used to extend the ISA command

PIN No.	Symbol	Type	Description
			width for the CPU and DMA cycles.
Y25	AEN	O	**ISA address enable**. This active high output indicates that the system address is enabled during the DMA refresh cycles.
AF28,AH30,AJ29,AF27,AK29,AG28,AJ30,AG27,AJ28,AH28,AK28,AJ27,AH26,AK27,AK25,AJ26,AK26	SA[16:0]	I/O	**ISA slot address bus.** These signals are high impedance during hold acknowledge.
AG30,AG29,AD27	SA[19:17]	I/O	**ISA slot address bus.** ISA slot address bus for 62-pin slot.
V21	SBHE#	I/O	**ISA Bus high enable.** In master cycle, it is an input polarity signal and is driven by the master device.
AC29,AE29,AD28,AE30,AF29,AE28,AF30	LA[23:17]	I/O	**ISA latched address bus**. These are input signal during ISA master cycle.
AG26	MEMR#	I/O	**ISA memory read**. This signal is an input during ISA master cycle.
AB25	MEMW#	I/O	**ISA memory write**. This signal is an input during ISA master cycle.
U28	RST_DRV	O	**Driver Reset**. This output signal is driven active during system power up.
AB27,AC28 AC26,U27,AB26,AE22 AA28,Y28,W25,AF22,AG23	IRQ[15:14], IRQ[12:9], IRQ[7:3]	I	**Interrupt request signals**. These are interrupt request input signals.
AC27,W21,AE26 Y21,AE23,AF26,AD26	DRQ[7:5], DRQ[3:0]	I	**DMA device request**. These are DMA request input signals.
AF24	0WS#	I	**ISA zero wait state**. This is the ISA device zero-wait state indicator signal. This signal terminates the CPU ISA command immediately.
V20	SMEMR#	O	**ISA system memory read**. This signal indicates that the memory read cycle is for an address below 1M byte address.
Y27	SMEMW#	O	**ISA system memory write**. This signal indicates that the memory write cycle is for an address below 1M byte address.
T20	IOW#	O	**ISA I/O write**. This signal is an input during ISA master cycle.
T21	IOR#	O	**ISA I/O read**. This signal is an input during ISA master cycle.
AE25,U26,AF23 AA29,AG25,AH25,T27	DACK#[7:5], DACK#[3:0]	O	**DMA device acknowledge signals**. These are DMA acknowledge demultiplex select signals. Input function is for hardware setting.
Y26	REFRESH#	O	**Refresh cycle indicator**. ISA master uses this signal to notify DRAM needs

PIN No.	Symbol	Type	Description
			refresh. During the memory controller's self-acting refresh cycle, M6117D drives this signal to the I/O channels.
AA25	SYSCLK	O	**System Clock Output**. This signal clocks the ISA bus.
W20	TC	O	**DMA end of process**. This is the DMA channel terminal count indicating signal.
AC25	BALE	O	**Bus address latch enable**. BALE indicates the presence of a valid address at I/O slots.
U20	MEMCS16#	I/O	ISA 16-bit memory device select indicator signal.
U25	IOCS16#	I/O	ISA 16-bit I/O device select indicator signal.
AE24	OSC14318	O	14.318MHz clock out

- **Chip Selection Interface (2 PINs)**

PIN No.	Symbol	Type	Description
V26	GPCS0#	O	**General-Purpose Chip Select 0**.
	STRAP_PLL	I	**PLL mode select** Pull it high to select Normal mode. Default internal pull-high. Pull it low to test mode. Please set STRAP_PLL pull-high when SB fun0 48h[7] and SB fun0 C0h[30] set to 1. Others setting need pull STRAP_PLL to low.
AD25	GPCS1#	O	**General-Purpose Chip Select 1**.
	STRAP_PLL1_SEL	I	**PLL 14.318MHz clock source select** Pull it high to select internal PLL. Default internal pull-high. Pull it low to select 14.318Mhz clock source from XIN_14318.

- **SPI Interface (4 Balls)**

Ball No.	Symbol	Type	Description
K11	ROM_CS#	O	***ROM Chip Select.*** This pin is used as a ROM chip select.
	SPI_CS#	O	***SPI Chip Select***
	STRAP_BMS	I	***Boot Mode Select*** Pull it high to select Normal boot (Reset 250ms). Default internal pull-high. Pull it low to select Fast boot.
L10	SPI_CK	O	***SPI Clock***
	STRAP_ JTAG	I	***JTAG enable*** ***Pull it high to enable JTAG. default internal pull-high***
L11	SPI_DO	O	***SPI Data Output / Output pin, connected with input of flash.***
	STRAP_FLASH_SEL	I	***Fl*ash select** **Pull it high to select Internal SPI (default internal pull-high)** **Pull it low to select flash-8bits**
K10	SPI_DI	I	***SPI Data Input / Input pin, connected with output of flash.***

- **Redundant (4 PIN)**

PIN No.	Symbol	Type	Description
W28	EXTSYSFAILIN#	I	**External system fail input**. This pin is the system fail in for redundant.
AA30	SYSFAILOUT#	O	**System fail output**. This pin is the system fail out for redundant.
Y29	EXT_SWITCH_FAIL#	I	**External switch fail**. This pin is the switch input for redundant.
U21	EXT_GPCS#	I	**External GPCS input**. This pin is the GPCS in for redundant.

- **KBD/MOUSE Interface (4 PINs)**

PIN No.	Symbol	Type	Description
C8	KBCLK	I/O	**Keyboard Clock**. This pin is keyboard clock when used internal 8042.
	KBRST#	I	**Keyboard Reset**. This pin is Keyboard reset when used external 8042.
D8	KBDAT	I/O	**Keyboard Data**. This pin is keyboard data when used internal 8042.
	A20GATE#	I	**Address Bit 20 Mask**. This pin is A20 mask when used external 8042.
C9	MSCLK	I/O	**Mouse Clock**. This pin is mouse clock when used internal 8042.
D9	MSDAT	I/O	**Mouse Data**. This pin is mouse data when used internal 8042.

- **RTC Interface (3 PINs)**

PIN No.	Symbol	Type	Description
C7	RTC_PS	I	***RTC Battery Power Sense.***
B7	RTC_XOUT	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator)
A7	RTC_XI	I	***Crystal-in.*** 32.768KHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).

- **PCIE Bus Interface (16 PINs)**

PIN No.	Symbol	Type	Description
A24 B24	PE0_RXP PE0_RXN	I	PCI-E Differential serial data input. P: positive; N:negative
A22 B22	PE0_TXP PE0_TXN	O	PCI-E Differential serial data output. P: positive; N: negative
A26 B26	PE1_RXP PE1_RXN	I	PCI-E Differential serial data input. P: positive; N: negative
C27 D27	PE1_TXP PE1_TXN	O	PCI-E Differential serial data output. P: positive; N: negative
E25 E24	PE0_CLKP PE0_CLKN	I	PCI-E Differential reference clock. P: positive; N: negative

PIN No.	Symbol	Type	Description
D23 D22	DIF0_PCIE_PLLCLK100_P DIF0_PCIE_PLLCLK100_N	O	PCI-E Differential Clock 100MHz from Internal PLL P: positive; N: negative
A19 B19	DIF2_CLK100_P DIF2_CLK100_N	O	PCI-E Differential Clock 100MHz to Port1 P: positive; N: negative
A17 B17	DIF3_CLK100_P DIF3_CLK100_N	O	PCI-E Differential Clock 100MHz to Port2 P: positive; N: negative

- **INTERNAL SPI CONTROL (2 PINs)**

PIN No.	Symbol	Type	Description
G5	PADWPB	I	***Write- protect pin of SPI embedded flash, must pull high to 3.3V by a 10K ohm resistor.***
M5	PADHOLDB	I	***Hold pin of SPI embedded flash, must pull high to 3.3V by a 10K ohm resistor.***

- **JTAG Interface (4 PINs)**

PIN No.	Symbol	Type	Description
F3	TDO	O	***TDO:*** JTAG Test Data Output pin.
C3	TMS	I	***TMS:*** JTAG Test Mode Select pin.
E3	TCK	I	***TCK:*** JTAG Test Clock Input pin.
D3	TDI	I	***TDI:*** JTAG Test Data Input pin.

- **GPIO P0[7:0]/MC3[1:0],MC0[4,5,3:0]/ 8051A P0[7:0]/COM5/8051B P0[7:0]/8051B[TXD1,RXD1]/8051B[TXDEN1,TXDEN2]/FD-SPI2 (8 PINs)**

PIN No.	Symbol	Type	Description
L27	CTS5#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	GPIO_P0[7]	I/O	***General-Purpose Input/Output Port 0 [7].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[7]	I/O	***8051A General-Purpose Input/Output Port 0[7].***

PIN No.	Symbol	Type	Description
	MC3[1]	I/O	***Motion Controller 3 [1].***
	8051B_GPIO_P0[7]	I/O	***8051B General-Purpose Input/Output Port 0[7].***
	8051B_SOUT1	O	***8051B COM1 Transmit Data***
L26	DSR5#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*
	GPIO_P0[6]	I/O	***General-Purpose Input/Output Port 0 [6].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[6]	I/O	***8051A General-Purpose Input/Output Port 0[6].***
	MC3[0]	I/O	***Motion Controller 3 [0].***
	8051B_GPIO_P0[6]	I/O	***8051B General-Purpose Input/Output Port 0[6].***
	8051B_SIN1	I	***8051B COM1 Receive Data.***
P27	DTR5#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	GPIO_P0[5]	I/O	***General-Purpose Input/Output Port 0 [5].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[5]	I/O	***8051A General-Purpose Input/Output Port 0[5].***
	MC0[4]	I/O	***Motion Controller 0 [4].***
	8051B_GPIO_P0[5]	I/O	***8051B General-Purpose Input/Output Port 0[5].***
	8051B_TXDEN1	I/O	***8051B COM1 TX Status.*** This pin will be high when 8051B COM1 is transmitting.
J26	SIN5	I	***COM5 Receive Data.*** FIFO UART receiver serial data input signal.
	GPIO_P0[4]	I/O	***General-Purpose Input/Output Port 0 [4].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[4]	I/O	***8051A General-Purpose Input/Output Port 0[4].***
	MC0[5]	I/O	***Motion Controller 0 [5].***
	8051B_GPIO_P0[4]	I/O	***8051B General-Purpose Input/Output Port 0[4].***
	8051B_TXDEN2	I/O	***8051B COM2 TX Status.*** This pin will be high when 8051B COM2 is transmitting.

PIN No.	Symbol	Type	Description
N27	RI5#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
	GPIO_P0[3]	I/O	***General-Purpose Input/Output Port 0 [3].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[3]	I/O	***8051A General-Purpose Input/Output Port 0[3].***
	MC0[3]	I/O	***Motion Controller 0[3].***
	8051B_GPIO_P0[3]	I/O	***8051B General-Purpose Input/Output Port 0[3].***
	MC_SPI2_DI	I	***Full Duplex SPI 2 Data Input t it connects to device SDO output.***
M25	RTS5#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	GPIO_P0[2]	I/O	***General-Purpose Input/Output Port 0 [2].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[2]	I/O	***8051A General-Purpose Input/Output Port 0[2].***
	MC0[2]	I/O	***Motion Controller 0 [2].***
	8051B_GPIO_P0[2]	I/O	***8051B General-Purpose Input/Output Port 0[2].***
	MC_SPI2_DO	O	***Full Duplex SPI 2 Data Output. It connects to device SDI input.***
M26	SOUT5	O	***COM5 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	GPIO_P0[1]	I/O	***General-Purpose Input/Output Port 0 [1].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[1]	I/O	***8051A General-Purpose Input/Output Port 0[1].***
	MC0[1]	I/O	***Motion Controller 0 [1].***
	8051B_GPIO_P0[1]	I/O	***8051B General-Purpose Input/Output Port 0[1].***
	MC_SPI2_CLK	O	***Full Duplex SPI 2 Clock.***

PIN No.	Symbol	Type	Description
N25	DCD5#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*
	GPIO_P0[0]	I/O	***General-Purpose Input/Output Port 0 [0].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[0]	I/O	***8051A General-Purpose Input/Output Port 0[0].***
	MC0[0]	I/O	***Motion Controller 0[0].***
	8051B_GPIO_P0[0]	I/O	***8051B General-Purpose Input/Output Port 0[0].***
	MC_SPI2_CS#	O	***Full Duplex SPI 2 Chip Select.***

- **GPIO P1[7:0]/MC3[3:2],MC1[4,5,3:0]/ 8051A P1[7:0]/COM6/8051B P1[7:0] (8 PINs)**

PIN No.	Symbol	Type	Description
B6	CTS6#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	GPIO_P1[7]	I/O	***General-Purpose Input/OutputPort1 [7].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[7]	I/O	***8051A General-Purpose Input/Output Port1[7].***
	MC3[3]	I/O	***Motion Controller 3[3].***
	8051B_GPIO_P1[7]	I/O	***8051B General-Purpose Input/Output Port1[7].***
D6	DSR6#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*
	GPIO_P1[6]	I/O	***General-Purpose Input/OutputPort1 [6].*** This pin can be programmed input or output individually.

PIN No.	Symbol	Type	Description
	8051A_GPIO_P1[6]	I/O	***8051A General-Purpose Input/Output Port 1[6].***
	MC3[2]	I/O	***Motion Controller 3 [2].***
	8051B_GPIO_P1[6]	I/O	***8051B General-Purpose Input/Output Port 1[6].***
E8	DTR6#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	GPIO_P1[5]	I/O	***General-Purpose Input/Output Port1 [5].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[5]	I/O	***8051A General-Purpose Input/Output Port1[5].***
	MC1[4]	I/O	***Motion Controller 1 [4].***
	8051B_GPIO_P1[5]	I/O	***8051B General-Purpose Input/Output Port1[5].***
A6	SIN6	I	***COM6 Receive Data.*** FIFO UART receiver serial data input signal.
	GPIO_P1[4]	I/O	***General-Purpose Input/Output Port1 [4].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[4]	I/O	***8051A General-Purpose Input/Output Port1[4].***
	MC1[5]	I/O	***Motion Controller 1 [5].***
	8051B_GPIO_P1[4]	I/O	***8051B General-Purpose Input/Output Port1[4].***
C6	RI6#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
	GPIO_P1[3]	I/O	***General-Purpose Input/Output Port1 [3].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[3]	I/O	***8051A General-Purpose Input/Output Port1[3].***
	MC1[3]	I/O	***Motion Controller 1 [3].***
	8051B_GPIO_P1[3]	I/O	***8051B General-Purpose Input/Output Port1[3].***
F7	RTS6#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	GPIO_P1[2]	I/O	***General-Purpose Input/Output Port1 [2].*** This pin can be programmed input or output individually.

PIN No.	Symbol	Type	Description
	8051A_GPIO_P1[2]	I/O	***8051A General-Purpose Input/Output Port1[2].***
	MC1[2]	I/O	***Motion Controller 1 [2].***
	8051B_GPIO_P1[2]	I/O	***8051B General-Purpose Input/Output Port1[2].***
E6	SOUT6	O	***COM5 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	GPIO_P1[1]	I/O	***General-Purpose Input/Output Port1 [1].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[1]	I/O	***8051A General-Purpose Input/Output Port1[1].***
	MC1[1]	I/O	***Motion Controller 1 [1].***
	8051B_GPIO_P1[1]	I/O	***8051B General-Purpose Input/Output Port1[1].***
E5	DCD6#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*
	GPIO_P1[0]	I/O	***General-Purpose Input/Output Port1 [0].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[0]	I/O	***8051A General-Purpose Input/Output Port1[0].***
	MC1[0]	I/O	***Motion Controller 1 [0].***
	8051B_GPIO_P1[0]	I/O	***8051B General-Purpose Input/Output Port 1[0].***

- **GPIO P2[7:0]/SA[31:24]/MC3[5:4],MC2[4,5,3:0]/ 8051A P2[7:0]/COM7/8051B P2[7:0] (8 PINs)**

PIN No.	Symbol	Type	Description
F23	CTS7#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	GPIO_P2[7]	I/O	***General-Purpose Input/Output Port2[7].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[7]	I/O	***8051A General-Purpose Input/Output Port2[7].***
	MC3[5]	I/O	***Motion Controller 3 [5].***
	8051B_GPIO_P2[7]	I/O	***8051B General-Purpose Input/Output Port 2[7].***

PIN No.	Symbol	Type	Description
	ISA_SA[31]	I/O	***ISA Extension Address bit 31***
G25	DSR7#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*
	GPIO_P2[6]	I/O	***General-Purpose Input/OutputPort2 [6].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[6]	I/O	***8051A General-Purpose Input/Output Port 2[6].***
	MC3[4]	I/O	***Motion Controller 3 [4].***
	8051B_GPIO_P2[6]	I/O	***8051B General-Purpose Input/Output Port 2[6].***
	ISA_SA[30]	I/O	***ISA Extension Address bit 30***
E27	DTR7#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	GPIO_P2[5]	I/O	***General-Purpose Input/Output Port2 [5].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[5]	I/O	***8051A General-Purpose Input/Output Port 2[5].***
	MC2[4]	I/O	***Motion Controller 2 [4].***
	8051B_GPIO_P2[5]	I/O	***8051B General-Purpose Input/Output Port 2[5].***
	ISA_SA[29]	I/O	***ISA Extension Address bit 29***
F26	SIN7	I	***COM7 Receive Data.*** FIFO UART receiver serial data input signal.
	GPIO_P2[4]	I/O	***General-Purpose Input/Output Port2 [4].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[4]	I/O	***8051A General-Purpose Input/Output Port2[4].***
	MC2[5]	I/O	***Motion Controller 2 [5].***
	8051B_GPIO_P2[4]	I/O	***8051B General-Purpose Input/Output Port2[4].***
	ISA_SA[28]	I/O	***ISA Extension Address bit 28***

PIN No.	Symbol	Type	Description
E26	RI7#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
	GPIO_P2[3]	I/O	***General-Purpose Input/Output Port 2 [3].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[3]	I/O	***8051A General-Purpose Input/Output Port 2[3].***
	MC2[3]	I/O	***Motion Controller 2 [3].***
	8051B_GPIO_P2[3]	I/O	***8051B General-Purpose Input/Output Port 2[3].***
	ISA_SA[27]	I/O	***ISA Extension Address bit 27***
E23	RTS7#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	GPIO_P2[2]	I/O	***General-Purpose Input/Output Port 2[2].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[2]	I/O	***8051A General-Purpose Input/Output Port1[2].***
	MC2[2]	I/O	***Motion Controller 2 [2].***
	8051B_GPIO_P2[2]	I/O	***8051B General-Purpose Input/Output Port 2[2].***
	ISA_SA[26]	I/O	***ISA Extension Address bit 26***
F24	SOUT7	O	***COM7 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	GPIO_P2[1]	I/O	***General-Purpose Input/Output Port 2[1].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[1]	I/O	***8051A General-Purpose Input/Output Port 2[1].***
	MC2[1]	I/O	***Motion Controller 2 [1].***
	8051B_GPIO_P2[1]	I/O	***8051B General-Purpose Input/Output Port 2[1].***
	ISA_SA[25]	I/O	***ISA Extension Address bit 25***

PIN No.	Symbol	Type	Description
F22	DCD7#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*
	GPIO_P2[0]	I/O	***General-Purpose Input/Output Port 2 [0].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[0]	I/O	***8051A General-Purpose Input/Output Port 2[0].***
	MC2[0]	I/O	***Motion Controller 2 [0].***
	8051B_GPIO_P2[0]	I/O	***8051B General-Purpose Input/Output Port 2[0].***
	ISA_SA[24]	I/O	***ISA Extension Address bit 24***

- **GPIO PORT3[7-4]/I2C/I2C1/TXDEN[4:3]/ 8051B P3[5:4]/8051A P3[7:4]/COM8[CTS,DSR,DTR,SIN]/Ext RTC(4 PINs)**

PIN No.	Symbol	Type	Description
D2	RTC_AS	O	***RTC Address Strobe.*** This pin is used as the RTC Address Strobe and should be connected to the RTC.
	GPIO_P3[7]	I/O	***General-Purpose Input/Output Port 3 bit 7.***
	8051A_GPIO_P3[7]	I/O	***8051A General-Purpose Input/Output Port 3 bit 7.***
	COM4_TXDEN	O	***COM4 TX Status.*** This pin will be high when COM4 is transmitting.
	CTS8#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	I2C1_SDA	I/O	***I2C1 Serial Data.***
F2	RTC_RD#	O	***RTC Read Command.*** This pin is used as the RTC Read Command and should be connected to the RTC.
	GPIO_P3[6]	I/O	***General-Purpose Input/Output Port 3 bit 6.***
	8051A_GPIO_P3[6]	I/O	***8051A General-Purpose Input/Output Port 3 bit 6.***
	COM3_TXDEN	O	***COM3 TX Status.*** This pin will be high when COM3 is transmitting.
	DSR8#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake

PIN No.	Symbol	Type	Description
			signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR# signal by reading bit5 of the Modem Status Register (MSR). A DSR1# signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR1# changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR#.*
	I2C1_SCL	I/O	***I2C1 Serial Clock.***
G3	RTC_WR#	O	***RTC Write Command.*** This pin is used as the RTC Write Command and should be connected to the RTC.
	GPIO_P3[5]	I/O	***General-Purpose Input/Output Port 3 bit 5.***
	8051A_GPIO_P3[5]	I/O	***8051A General-Purpose Input/Output Port 3 bit 5.***
	8051B_SOUT2	O	***8051B COM2 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	8051B_GPIO_P3[5]	I/O	***8051B General-Purpose Input/Output Port 3 bit 5.***
	DTR8#	I	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR1# signal to be inactive during the loop-mode operation.
	I2C_SDA	I/O	***I2C0 Serial Data.***
D1	RTC_IRQ8#	I	***RTC Interrupt Input.*** This pin is used as the RTC Interrupt input.
	GPIO_P3[4]	I/O	***General-Purpose Input/Output Port 3 bit 4.***
	8051A_GPIO_P3[4]	I/O	***8051A General-Purpose Input/Output Port 3 bit 4.***
	8051B_SIN2	I	***8051B COM2 Receive Data.*** FIFO UART receiver serial data input signal.
	8051B_GPIO_P3[4]	I/O	***8051B General-Purpose Input/Output Port 3 bit 4.***
	SIN8	I/O	***COM8 Receive Data.*** FIFO UART receiver serial data input signal.
	I2C_SCL	I/O	***I2C0 Serial Clock.***

- **GPIO PORT3[3-0]/8051A GPIO P3[3-0]/Full Duplex SPI1/8051B GPIO P3[3-0]/COM8[RI,RTS,SOUT,DCD]/External SPI (4 PINs)**

PIN No.	Symbol	Type	Description
H3	E_SPI_DI	I	***External SPI Data Input t it connects to device SDO output.***
	GPIO_P3[3]	I/O	***General-Purpose Input/Output Port 3 bit 3***
	8051A_GPIO_P3[3]	I/O	***8051A General-Purpose Input/Output Port 3 bit 3***
	MC_SPI1_DI	I	***Full Duplex SPI 1 Data Input t it connects to device SDO output.***
	8051B_GPIO_P3[3]	I/O	***8051B General-Purpose Input/Output Port 3 bit 3***
	RI8#	I/O	***Ring Indicator.*** This active low input is for the UART ports. A handshake

PIN No.	Symbol	Type	Description
			signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
E1	E_SPI_DO	O	***External SPI Data Output. It connects to device SDI input.***
	GPIO_P3[2]	I/O	***General-Purpose Input/Output Port 3 bit 2***
	8051A_GPIO_P3[2]	I/O	***8051A General-Purpose Input/Output Port 3 bit 2***
	MC_SPI1_DO	O	***Full Duplex SPI 1 Data Output. It connects to device SDI input.***
	8051B_GPIO_P3[2]	I/O	***8051B General-Purpose Input/Output Port 3 bit 2***
	RTS8#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
G2	E_SPI_CLK	O	***External SPI Clock***
	GPIO_P3[1]	I/O	***General-Purpose Input/Output Port 3 bit 1***
	8051A_GPIO_P3[1]	I/O	***8051A General-Purpose Input/Output Port 3 bit 1***
	MC_SPI1_CLK	O	***Full Duplex SPI 1 SPI Clock.***
	8051B_GPIO_P3[1]	I/O	***8051B General-Purpose Input/Output Port 3 bit 1***
	SOUT8	O	***COM8 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	8051B_SOUT2	O	***8051B COM2 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
F1	E_SPI_CS#	O	***External SPI Chip Select***
	GPIO_P3[0]	I/O	***General-Purpose Input/Output Port 3 bit 0.***
	8051A_GPIO_P3[0]	I/O	***8051A General-Purpose Input/Output Port 3 bit 0.***
	MC_SPI1_CS#	O	***Full Duplex SPI 1 Chip Select.***
	8051B_GPIO_P3[0]	I/O	***8051B General-Purpose Input/Output Port 3 bit 0***
	DCD8#	I/O	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*

- **COM1/PORT4[7:0]/ MC7[1:0],MC4[4,5,3:0] /8051A PORT 4[7:0]/8051B PORT 4[7:0] (8 PINs)**

PIN No.	Symbol	Type	Description
R25	CTS1#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS1# signal by reading bit 4 of Modem Status Register (MSR). A CTS1# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS1# changes the state. The CTS1# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS1#.*
	GPIO_P4[7]	I/O	***General-Purpose Input/Output Port 4 bit 7.***
	8051A_GPIO_P4[7]	I/O	***8051A General-Purpose Input/Output Port 4 bit 7.***
	MC7[1]	I/O	***Motion Controller 7 [1].***
	8051B_GPIO_P4[7]	I/O	***8051B General-Purpose Input/Output Port 4 bit 7.***
T26	DSR1#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR1# signal by reading bit5 of the Modem Status Register (MSR). A DSR1# signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR1# changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR1#.*
	GPIO_P4[6]	I/O	***General-Purpose Input/Output Port 4 bit 6.***
	8051A_GPIO_P4[6]	I/O	***8051A General-Purpose Input/Output Port 4 bit 6.***
	MC7[0]	I/O	***Motion Controller 7 [0].***
	8051B_GPIO_P4[6]	I/O	***8051B General-Purpose Input/Output Port 4 bit 6.***
T25	DTR1#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR1# signal to be inactive during the loop-mode operation.
	GPIO_P4[5]	I/O	***General-Purpose Input/Output Port 4 bit 5.***
	8051A_GPIO_P4[5]	I/O	***8051A General-Purpose Input/Output Port 4 bit 5.***
	MC4[4]	I/O	***Motion Controller 4 [4].***
	8051B_GPIO_P4[5]	I/O	***8051B General-Purpose Input/Output Port 4 bit 5.***
N26	SIN1	I	***Receive Data.*** FIFO UART receiver serial data input signal.
	GPIO_P4[4]	I/O	***General-Purpose Input/Output Port 4 bit 4.***
	8051A_GPIO_P4[4]	I/O	***8051A General-Purpose Input/Output Port 4 bit 4.***

PIN No.	Symbol	Type	Description
	MC4[5]	I/O	***Motion Controller 4 [5].***
	8051B_GPIO_P4[4]	I/O	***8051B General-Purpose Input/Output Port 4 bit 4.***
P25	RI1#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI1# signal by reading bit 6 of the Modem Status Register (MSR). An RI1# signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI1# changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI1#.*
	GPIO_P4[3]	I/O	***General-Purpose Input/Output Port 4 bit 3.***
	8051A_GPIO_P4[3]	I/O	***8051A General-Purpose Input/Output Port 4 bit 3.***
	MC4[3]	I/O	***Motion Controller 4 [3].***
	8051B_GPIO_P4[3]	I/O	***8051B General-Purpose Input/Output Port 4 bit 3.***
R27	RTS1#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS1# signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	GPIO_P4[2]	I/O	***General-Purpose Input/Output Port 4 bit 2.***
	8051A_GPIO_P4[2]	I/O	***8051A General-Purpose Input/Output Port 4 bit 2.***
	MC4[2]	I/O	***Motion Controller 4 [2].***
	8051B_GPIO_P4[2]	I/O	***8051B General-Purpose Input/Output Port 4 bit 2.***
R26	SOUT1	O	***Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	GPIO_P4[1]	I/O	***General-Purpose Input/Output Port 4 bit 1.***
	8051A_GPIO_P4[1]	I/O	***8051A General-Purpose Input/Output Port 4 bit 1.***
	MC4[1]	I/O	***Motion Controller 4 [1].***
	8051B_GPIO_P4[1]	I/O	***8051B General-Purpose Input/Output Port 4 bit 1.***
R28	DCD1#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD1# signal by reading bit 7 of the Modem Status Register (MSR). A DCD1# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD1# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD1#.*
	GPIO_P4[0]	I/O	***General-Purpose Input/Output Port 4 bit 0.***

PIN No.	Symbol	Type	Description
	8051A_GPIO_P4[0]	I/O	***8051A General-Purpose Input/Output Port 4 bit 0.***
	MC4[0]	I/O	***Motion Controller 4 [0].***
	8051B_GPIO_P4[0]	I/O	***8051B General-Purpose Input/Output Port 4 bit 0.***

- **COM2/PWM/PORT5[7:0]/MC7[3:2],MC5[4,5,3 :0]/8051B PORT 5[7:0] (8 PINs)**

PIN No.	Symbol	Type	Description
C11	PWM1_GATE	I	***PWM Timer1 Gate.*** This pin is PWM timer1 gate mask when SB register C0h bit2 is 1 (PINs for PWM).
	GPIO_P5[7]	I/O	***General-Purpose Input/Output Port 5 bit 7.***
	MC7[3]	I/O	***Motion Controller 7 [3].***
	8051B_GPIO_P5[7]	I/O	***8051B General-Purpose Input/Output Port 5 bit 7.***
	CTS2#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS2# signal by reading bit 4 of Modem Status Register (MSR). A CTS2# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS1# changes the state. The CTS2# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS2#.*
D12	PWM_GATE	I	***PWM Timer Gate.*** This pin is PWM timer gate mask when SB register C0h bit2 is 1 (PINs for PWM).
	GPIO_P5[6]	I/O	***General-Purpose Input/Output Port 5 bit 6.***
	MC7[2]	I/O	***Motion Controller 7 [2].***
	8051B_GPIO_P5[6]	I/O	***8051B General-Purpose Input/Output Port 5 bit 6.***
	DSR2#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR2# signal by reading bit5 of the Modem Status Register (MSR). A DSR2# signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR2# changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR2#.*
D11	PWM2_OUT	O	***PWM Timer2 Output.*** This pin is PWM timer1 output when SB register C0h bit2 is 1 (PINs for PWM).
	GPIO_P5[5]	I/O	***General-Purpose Input/Output Port 5 bit 5.***
	MC5[4]	I/O	***Motion Controller 5 [4].***
	8051B_GPIO_P5[5]	I/O	***8051B General-Purpose Input/Output Port 5 bit 5.***

PIN No.	Symbol	Type	Description
	DTR2#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR2# signal to be inactive during the loop-mode operation.
D10	PWM2_CLK	I	***PWM Timer2 Clock.*** This pin is PWM timer2 external clock input when SB register C0h bit2 is 1 (PINs for PWM).
	GPIO_P5[4]	I/O	***General-Purpose Input/Output Port 5 bit 4.***
	MC5[5]	I/O	***Motion Controller 5 [5].***
	8051B_GPIO_P5[4]	I/O	***8051B General-Purpose Input/Output Port 5 bit 4.***
	SIN2	I	***Receive Data.*** FIFO UART receiver serial data input signal.
D14	PWM1_CLK	I	***PWM Timer1 Clock.*** This pin is PWM timer1 external clock input when SB register C0h bit2 is 1 (PINs for PWM).
	GPIO_P5[3]	I/O	***General-Purpose Input/Output Port 5 bit 3.***
	MC5[3]	I/O	***Motion Controller 5 [3].***
	8051B_GPIO_P5[3]	I/O	***8051B General-Purpose Input/Output Port 5 bit 3.***
	RI2#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI2# signal by reading bit 6 of the Modem Status Register (MSR). An RI2# signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI2# changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI2#.*
D13	PWM1_OUT	O	***PWM Timer1 Output.*** This pin is PWM timer1 output when SB register C0h bit2 is 1 (PINs for PWM).
	GPIO_P5[2]	I/O	***General-Purpose Input/Output Port 5 bit 2.***
	MC5[2]	I/O	***Motion Controller 5 [2].***
	8051B_GPIO_P5[2]	I/O	***8051B General-Purpose Input/Output Port 5 bit 2.***
	RTS2#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS1# signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
D15	PWM_OUT	O	***PWM Timer Output.*** This pin is PWM timer output when SB register C0h bit2 is 1 (PINs for PWM).
	GPIO_P5[1]	I/O	***General-Purpose Input/Output Port 5 bit 1.***

PIN No.	Symbol	Type	Description
	MC5[1]	I/O	***Motion Controller 5 [1].***
	8051B_GPIO_P5[1]	I/O	***8051B General-Purpose Input/Output Port 5 bit 1.***
	SOUT2	O	***Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
E12	PWM_CLK	I	***PWM Timer Clock.*** This pin is PWM timer external clock input when SB register C0h bit2 is 1 (PINs for PWM).
	GPIO_P5[0]	I/O	***General-Purpose Input/Output Port 5 bit 0.***
	MC5[0]	I/O	***Motion Controller 5 [0].***
	8051B_GPIO_P5[0]	I/O	***8051B General-Purpose Input/Output Port 5 bit 0.***
	DCD2#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD2# signal by reading bit 7 of the Modem Status Register (MSR). A DCD2# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD2# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD2#.*

- **Primary IDE Data[7:0]/SD Interface/COM3/GPIO P6[7:0]/MC7[5:4],MC6[4,5,3:0]/8051B P6[7:0] (8 PINs)**

PIN No.	Symbol	Type	Description
K12	IDE_PDD[7]	I/O	***IDE Primary Channel Data Bus Data 7.***
	GPIO_P6[7]	I/O	***General-Purpose Input/Output Port 6[7].*** This pin can be programmed input or output individually.
	SD_WP	I	***SD0 Write Protect.***
	MC7[5]	I/O	***Motion Controller 7 [5].***
	8051B_GPIO_P6[7]	I/O	***8051B General-Purpose Input/Output Port 6[7].***
	CTS3#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
K13	IDE_PDD[6]	I/O	***IDE Primary Channel Data Bus Data 6.***
	GPIO_P6[6]	I/O	***General-Purpose Input/Output Port 6[6].*** This pin can be programmed input or output individually.
	SD_CD	I	***SD0 Card Detect.***
	MC7[4]	I/O	***Motion Controller 7 [4].***

PIN No.	Symbol	Type	Description
	8051B_GPIO_P6[6]	I/O	***8051B General-Purpose Input/Output Port 6[6].***
	DSR3#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*
F4	IDE_PDD[5]	I/O	***IDE Primary Channel Data Bus Data 5.***
	GPIO_P6[5]	I/O	***General-Purpose Input/Output Port 6[5].*** This pin can be programmed input or output individually.
	SD_DATA[1]	I/O	***SD0 Data Bus Data 1.***
	MC6[4]	I/O	***Motion Controller 6 [4].***
	8051B_GPIO_P6[5]	I/O	***8051B General-Purpose Input/Output Port 6[5].***
	DTR3#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
G4	IDE_PDD[4]	I/O	***IDE Primary Channel Data Bus Data 4.***
	GPIO_P6[4]	I/O	***General-Purpose Input/Output Port 6[4].*** This pin can be programmed input or output individually.
	SD_DATA[0]	I/O	***SD0 Data Bus Data 0.***
	MC6[5]	I/O	***Motion Controller 6 [5].***
	8051B_GPIO_P6[4]	I/O	***8051B General-Purpose Input/Output Port 6[4].***
	SIN3	I	***COM3 Receive Data.*** FIFO UART receiver serial data input signal.
E4	IDE_PDD[3]	I/O	***IDE Primary Channel Data Bus Data 3.***
	GPIO_P6[3]	I/O	***General-Purpose Input/Output Port 6[3].*** This pin can be programmed input or output individually.
	SD_CLK	O	***SD0 Clock.***
	MC6[3]	I/O	***Motion Controller 6 [3].***
	8051B_GPIO_P6[3]	I/O	***8051B General-Purpose Input/Output Port 6[3].***

PIN No.	Symbol	Type	Description
	RI3#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
L12	IDE_PDD[2]	I/O	***IDE Primary Channel Data Bus Data 2.***
	GPIO_P6[2]	I/O	***General-Purpose Input/Output Port 6[2].*** This pin can be programmed input or output individually.
	SD_CMD	I/O	***SD0 Command/Response.***
	MC6[2]	I/O	***Motion Controller 6 [2].***
	8051B_GPIO_P6[2]	I/O	***8051B General-Purpose Input/Output Port 6[2].***
	RTS3#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
H4	IDE_PDD[1]	I/O	***IDE Primary Channel Data Bus Data 1.***
	GPIO_P6[1]	I/O	***General-Purpose Input/Output Port 6[1].*** This pin can be programmed input or output individually.
	SD_DATA[3]	I/O	***SD0 Data Bus Data 3.***
	MC6[1]	I/O	***Motion Controller 6 [1].***
	8051B_GPIO_P6[1]	I/O	***8051B General-Purpose Input/Output Port 6[1].***
	SOUT3	O	***COM3 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
L13	IDE_PDD[0]	I/O	***IDE Primary Channel Data Bus Data 0.***
	GPIO_P6[0]	I/O	***General-Purpose Input/Output Port 6[0].*** This pin can be programmed input or output individually.
	SD_DATA[2]	I/O	***SD0 Data Bus Data 2.***
	MC6[0]	I/O	***Motion Controller 6 [0].***
	8051B_GPIO_P6[0]	I/O	***8051B General-Purpose Input/Output Port 6[0].***

PIN No.	Symbol	Type	Description
	DCD3#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*

- **Primary IDE Data[15:8]/SD1 Interface/COM4/GPIO P7[7:0]/MCB[1:0],MC8[4,5,3:0]/8051B P7[7:0] (8 PINs)**

PIN No.	Symbol	Type	Description
C5	IDE_PDD[15]	I/O	***IDE Primary Channel Data Bus Data 15.***
	GPIO_P7[7]	I/O	***General-Purpose Input/Output Port 7[7].*** This pin can be programmed input or output individually.
	SD1_WP	I	***SD1 Write Protect.***
	MCB[1]	I/O	***Motion Controller B [1].***
	8051B_GPIO_P7[7]	I/O	***8051B General-Purpose Input/Output Port 7[7].***
	CTS4#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
D5	IDE_PDD[14]	I/O	***IDE Primary Channel Data Bus Data 14.***
	GPIO_P7[6]	I/O	***General-Purpose Input/Output Port 7[6].*** This pin can be programmed input or output individually.
	SD1_CD	I	***SD1 Card Detect.***
	MCB[0]	I/O	***Motion Controller B [0].***
	8051B_GPIO_P7[6]	I/O	***8051B General-Purpose Input/Output Port 7[6].***

PIN No.	Symbol	Type	Description
	DSR4#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*
A4	IDE_PDD[13]	I/O	***IDE Primary Channel Data Bus Data 13.***
	GPIO_P7[5]	I/O	***General-Purpose Input/Output Port 7[5].*** This pin can be programmed input or output individually.
	SD1_DATA[1]	I/O	***SD1 Data Bus Data 1.***
	MC8[4]	I/O	***Motion Controller 8 [4].***
	8051B_GPIO_P7[5]	I/O	***8051B General-Purpose Input/Output Port 7[5].***
	DTR4#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
B4	IDE_PDD[12]	I/O	***IDE Primary Channel Data Bus Data 12.***
	GPIO_P7[4]	I/O	***General-Purpose Input/Output Port 7[4].*** This pin can be programmed input or output individually.
	SD_DATA[0]	I/O	***SD0 Data Bus Data 0.***
	MC8[5]	I/O	***Motion Controller 8 [5].***
	8051B_GPIO_P7[4]	I/O	***8051B General-Purpose Input/Output Port 7[4].***
	SIN4	I	***COM4 Receive Data.*** FIFO UART receiver serial data input signal.
A3	IDE_PDD[11]	I/O	***IDE Primary Channel Data Bus Data 11.***
	GPIO_P7[3]	I/O	***General-Purpose Input/Output Port 7[3].*** This pin can be programmed input or output individually.
	SD1_CLK	O	***SD1 Clock.***
	MC8[3]	I/O	***Motion Controller 8 [3].***
	8051B_GPIO_P7[3]	I/O	***8051B General-Purpose Input/Output Port 7[3].***
	RI4#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*

PIN No.	Symbol	Type	Description
B3	IDE_PDD[10]	I/O	***IDE Primary Channel Data Bus Data 10.***
	GPIO_P7[2]	I/O	***General-Purpose Input/Output Port 7[2].*** This pin can be programmed input or output individually.
	SD1_CMD	I/O	***SD1 Command/Response.***
	MC8[2]	I/O	***Motion Controller 8 [2].***
	8051B_GPIO_P7[2]	I/O	***8051B General-Purpose Input/Output Port 7[2].***
	RTS4#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
A5	IDE_PDD[9]	I/O	***IDE Primary Channel Data Bus Data 9.***
	GPIO_P7[1]	I/O	***General-Purpose Input/Output Port 7[1].*** This pin can be programmed input or output individually.
	SD1_DATA[3]	I/O	***SD1 Data Bus Data 3.***
	MC8[1]	I/O	***Motion Controller 8 [1].***
	8051B_GPIO_P7[1]	I/O	***8051B General-Purpose Input/Output Port 7[1].***
	SOUT4	O	***COM4 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
C4	IDE_PDD[8]	I/O	***IDE Primary Channel Data Bus Data 8.***
	GPIO_P7[0]	I/O	***General-Purpose Input/Output Port 7[0].*** This pin can be programmed input or output individually.
	SD1_DATA[2]	I/O	***SD1 Data Bus Data 2.***
	MC8[0]	I/O	***Motion Controller 8 [0].***
	8051B_GPIO_P7[0]	I/O	***8051B General-Purpose Input/Output Port 7[0].***
	DCD4#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*

- **Primary IDE CTRL1/LTP CTRL1/COM9/GPIO P8[7:0]/MCB[3:2],MC9[4,5,3:0]/8051B P8[7:0] (8 PINs)**

PIN No.	Symbol	Type	Description
F13	IDE_PCS1#	O	***IDE Primary Channel Chip Select.***
	GPIO_P8[7]	I/O	***General-Purpose Input/Output Port 8[7].*** This pin can be programmed input or output individually.
	MCB[3]	I/O	***Motion Controller B [3].***
	8051B_GPIO_P8[7]	I/O	***8051B General-Purpose Input/Output Port 8[7].***
	CTS9#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	AFD#	OD	***AFD#.*** An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
F12	IDE_PCS0#	O	***IDE Primary Channel Chip Select.***
	GPIO_P8[6]	I/O	***General-Purpose Input/Output Port 8[6].*** This pin can be programmed input or output individually.
	MCB[2]	I/O	***Motion Controller B [2].***
	8051B_GPIO_P8[6]	I/O	***8051B General-Purpose Input/Output Port 8[6].***
	DSR9#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*
	ERR#	I	***ERR#.*** An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
F11	IDE_PIOW#	O	***IDE Primary Channel IO Write Strobe.***
	GPIO_P8[5]	I/O	***General-Purpose Input/Output Port 8[5].*** This pin can be programmed input or output individually.
	SD_ACTIVE	O	***SD Read/Write status. High active***
	MC9[4]	I/O	***Motion Controller 9 [4].***
	8051B_GPIO_P8[5]	I/O	***8051B General-Purpose Input/Output Port 8[5].***

PIN No.	Symbol	Type	Description
	DTR9#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	INIT#	OD	***INIT#.*** Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
E9	IDE_PIOR#	O	***IDE Primary Channel IO Read Strobe.***
	GPIO_P8[4]	I/O	***General-Purpose Input/Output Port 8[4].*** This pin can be programmed input or output individually.
	SD1_ACTIVE	O	***SD1 Read/Write status. High active***
	MC9[5]	I/O	***Motion Controller 9 [5].***
	8051B_GPIO_P8[4]	I/O	***8051B General-Purpose Input/Output Port 8[4].***
	SIN9	I	***COM9 Receive Data.*** FIFO UART receiver serial data input signal.
	SLCIN	OD	***SLIN#.*** Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
F9	IDE_PA[2]	O	***IDE Primary Channel Device Address***
	GPIO_P8[3]	I/O	***General-Purpose Input/Output Port 8[3].*** This pin can be programmed input or output individually.
	MC9[3]	I/O	***Motion Controller 9 [3].***
	8051B_GPIO_P8[3]	I/O	***8051B General-Purpose Input/Output Port 8[3].***
	ACK#	I	***ACK#.*** An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	RI9#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
F10	IDE_PA[1]	O	***IDE Primary Channel Device Address***
	GPIO_P8[2]	I/O	***General-Purpose Input/Output Port 8[2].*** This pin can be programmed input or output individually.
	MC9[2]	I/O	***Motion Controller 9 [2].***
	8051B_GPIO_P8[2]	I/O	***8051B General-Purpose Input/Output Port 8[2].***

PIN No.	Symbol	Type	Description
	RTS9#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	BUSY	I	***BUSY.*** An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
F8	IDE_PA[0]	O	***IDE Primary Channel Device Address***
	GPIO_P8[1]	I/O	***General-Purpose Input/Output Port 8[1].*** This pin can be programmed input or output individually.
	MC9[1]	I/O	***Motion Controller 9 [1].***
	8051B_GPIO_P8[1]	I/O	***8051B General-Purpose Input/Output Port 8[1].***
	SOUT9	O	***COM9 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	PE	I	***PE.*** An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
E11	IDE_PINT	I	***IDE Primary Channel Interrupt.***
	GPIO_P8[0]	I/O	***General-Purpose Input/Output Port 8[0].*** This pin can be programmed input or output individually.
	MC9[0]	I/O	***Motion Controller 9 [0].***
	8051B_GPIO_P8[0]	I/O	***8051B General-Purpose Input/Output Port 8[0].***
	DCD9#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*
	SLCT	I	***SLCT.*** An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.

- **USB Device/Primary IDE CTRL 2/MTBF/WDT_RSTB/GPIO P9[7:0]/MCB[5:4],MCA[4,5,3:0]/8051B P9[7:0]/ LPT DATA[7:0] (8 PINs)**

PIN No.	Symbol	Type	Description
G27	MTBF	O	***MTBF Flag output.***
	GPIO_P9[7]	I/O	***General-Purpose Input/Output Port 9[7].*** This pin can be programmed input or output individually.
	MCB[5]	I/O	***Motion Controller B [5].***
	8051B_GPIO_P9[7]	I/O	***8051B General-Purpose Input/Output Port 9[7].***
	WDT_RSTB	O	***Watchdog 1 Timeout Signal.***
	PD[7]	I/O	***Parallel port data bus bit 7.*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
J25	IDE_PDRQ	I	***IDE Primary Channel DMA Request.***
	GPIO_P9[6]	I/O	***General-Purpose Input/Output Port 9[6].*** This pin can be programmed input or output individually.
	MCB[4]	I/O	***Motion Controller B [4].***
	8051B_GPIO_P9[6]	I/O	***8051B General-Purpose Input/Output Port 9[6].***
	PD[6]	I/O	***Parallel port data bus bit 6.*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
G26	IDE_PIORDY	I	***IDE Primary Channel IO Channel Ready.***
	GPIO_P9[5]	I/O	***General-Purpose Input/Output Port 9[5].*** This pin can be programmed input or output individually.
	MCA[4]	I/O	***Motion Controller A [4].***
	8051B_GPIO_P9[5]	I/O	***8051B General-Purpose Input/Output Port 9[5].***
	PD[5]	I/O	***Parallel port data bus bit 5.*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
H25	IDE_PDACK#	O	***IDE Primary Channel DMA Acknowledge.***
	GPIO_P9[4]	I/O	***General-Purpose Input/Output Port 9[4].*** This pin can be programmed input or output individually.
	MCA[5]	I/O	***Motion Controller A [5].***
	8051B_GPIO_P9[4]	I/O	***8051B General-Purpose Input/Output Port 9[4].***
	PD[4]	I/O	***Parallel port data bus bit 4.*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
H27	IDE_PCBLID#	I	***IDE Primary Channel Cable Assembly Type Identifier.***
	GPIO_P9[3]	I/O	***General-Purpose Input/Output Port 9[3].*** This pin can be programmed input or output individually.
	MCA[3]	I/O	***Motion Controller A [3].***
	8051B_GPIO_P9[3]	I/O	***8051B General-Purpose Input/Output Port 9[3].***
	PD[3]	I/O	***Parallel port data bus bit 3.*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
J27	IDE_PRST#	O	***IDE Primary Channel Reset.***

PIN No.	Symbol	Type	Description
	GPIO_P9[2]	I/O	***General-Purpose Input/Output Port 9[2].*** This pin can be programmed input or output individually.
	MCA[2]	I/O	***Motion Controller A [2].***
	8051B_GPIO_P9[2]	I/O	***8051B General-Purpose Input/Output Port 9[2].***
	PD[2]	I/O	***Parallel port data bus bit 2 .*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
K26	UD_DP	I/O	***Universal Serial Bus Device Controller Port Data+.*** These are the serial data pair for USB Device. Need add 1.5kΩ pull up resistors to UD_DP externally.
	GPIO_P9[1]	I/O	***General-Purpose Input/Output Port 9[1].*** This pin can be programmed input or output individually.
	MCA[1]	I/O	***Motion Controller A [1].***
	8051B_GPIO_P9[1]	I/O	***8051B General-Purpose Input/Output Port 9[1].***
	PD[1]	I/O	***Parallel port data bus bit 1 .*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
K25	UD_DM	I/O	***Universal Serial Bus Device Controller Data-.*** These are the serial data pair for USB Device.
	GPIO_P9[0]	I/O	***General-Purpose Input/Output Port 9[0].*** This pin can be programmed input or output individually.
	MCA[0]	I/O	***Motion Controller A [0].***
	8051B_GPIO_P9[0]	I/O	***8051B General-Purpose Input/Output Port 9[0].***
	PD[0]	I/O	***Parallel port data bus bit 0 .*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

- **GPIOA[7:5]/COM1-2 TXDEN + LPT CTRL(1) (3 PINs)**

PIN No.	Symbol	Type	Description
L14	TX_DEN1	O	***COM1 TX Status.*** This pin will be high when COM1 is transmitting.
	GPIO_PA[7]	I/O	***General-Purpose Input/Output Port A[7].*** Those pins can be programmed input or output individually.
K14	TX_DEN2	O	***COM2 TX Status.*** This pin will be high when COM2 is transmitting.
	GPIO_PA[6]	I/O	***General-Purpose Input/Output Port A[6].*** Those pins can be programmed input or output individually.
L15	STB#	OD	***STB#.*** An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO_PA[5]	I/O	***General-Purpose Input/Output Port A[5] .*** Those pins can be programmed input or output individually.

- **GPIOA[4:0]/General Shift Geretator+8254 Signal/HD Audio (5 PINs)**

PIN No.	Symbol	Type	Description
E14	H_BCLK	O	**Global Link 24.00-MHz clock**
	GPIO_PA[4]	I/O	***General-Purpose Input/Output PortA[4].*** Those pins can be programmed input or output individually.
	GSF_CLK	O	***General Shifter reference Clock***
K15	H_SYNC	O	**Global 48 kHz Frame Sync and outbound tag signal**
	GPIO_PA[3]	I/O	***General-Purpose Input/Output PortA[3].*** Those pins can be programmed input or output individually.
	GSF_CH2	I/O	***General Shifter Channel 2***
F14	H_SDO	O	**Bussed Serial Data Output(s)**
	GPIO_PA[2]	I/O	***General-Purpose Input/Output PortA[2] .*** Those pins can be programmed input or output individually.
	GSF_CH1	I/O	***General Shifter Channel 1***
K16	H_SDI	I/O	**Point-to-point Serial Data Input(s).** Controller has a weak pull down
	GPIO_PA[1]	I/O	***General-Purpose Input/Output Port A[1]*** *. Those pins can be programmed input or output individually.*
	GSF_CH0	I/O	***General Shifter Channel 0***
F15	H_RST#	O	**Global active low reset**
	GPIO_PA[0]	I/O	***General-Purpose Input/Output Port A[0]*** *. Those pins can be programmed input or output individually.*
	PWM2_GATE	I	***PWM Timer2 Gate.*** This pin is PWM timer2 gate mask when SB register C0h bit2 is 1 (PINs for PWM).

- **ADC Interface (9 PINs)**

PIN No.	Symbol	Type	Description
E19,F19,E20,F20 ,F17,D20,D19, F18	ADC_IN[7:0]	I	***ADC Analog Input***
D16	VTEMP_TST	O	***Temperature Sensor Test Mode Output***

- **Serial ATA Interface (8 PINs)**

PIN No.	Symbol	Type	Description
V30 V29	SATA_TXP SATA_TXN	O	***Serial ATA Device Controller TX Port. These are the serial ATA Transmitter pair for Serial ATA Device.***
T30 T29	SATA _RXP SATA _RXN	I	***Serial ATA Device Controller RX Port. These are the serial ATA Receive pair for Serial ATA Device.***

P30 N30	SATA_CLKP SATA_CLKN	I	***Differential PLL Reference Clock Pair.***
A20 B20	DIF1_SATA_PHY_CLK_P DIF1_SATA_PHY_CLK_N	O	***Differential Clock Pair from Internal PLL.***

- **Ethernet Interface (24 PINs)**

PIN No.	Symbol	Type	Description
L3	LINK/ACTIVE	O	***LINK/ACTIVE:*** Link/active status
J2	DUPLEX	O	***DUPLEX:*** Duplex status
C13	ISET	I	***ISET:*** External resistor 6.02kΩ ±1%connecting pin for BIAS
B10	ATSTP	I/O	***ATSTP:*** Variable Gain Amplifier and ADC testing pin for input and output (positive)
A10	ATSTN	I/O	***ATSTN:*** Variable Gain Amplifier and ADC testing pin for input and output (negative)
B12	TXN	O	***TXN:*** 10B-T/100BT transmitting output pin/ receiving input pin (negative)
A12	TXP	O	***TXP:*** 10B-T/100BT transmitting output pin/ receiving input pin (positive)
B14	RXN	I	***RXN:*** 10B-T/100BT receiving input pin/ transmitting output pin (negative)
A14	RXP	I	***RXP:*** 10B-T/100BT receiving input pin/ transmitting output pin (positive)
K6	MDC	O	***MDC:*** MII management data clock is sourced by the SoC to the external PHY devices as a timing reference for the transfer of information on the MDIO signal.
L5	MDIO	I/O	***MDIO:*** MII management data input/output transfers control information and status between the external PHY and SoC.
L6	COL	I	***COL:*** This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
L2	RXC	I	***RXC:*** Supports the receive clock supplied by the external PMD device. This clock should always be active. Need add 4.7kΩ pull down resistors externally.
K3,J4,K4,J5	RXD[3:0]	I	***RXD[3:0]:*** Four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal.
L4	RXDV	I	***RXDV:*** Data valid is asserted by an external PHY when the received data is present on the **RXD[3:0]** lines and is de-asserted at the end of the packet. This signal should be synchronized with the RXC signal. Need add 4.7kΩ pull down resistors externally.
L1	TXC	I	***TXC:*** Supports the transmit clock supplied by the external PMD device. This clock should always be active.

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td rowspan="2">J1,G1,H1,K1</td><td>TXD[3:0]</td><td>O</td><td>TXD[3:0]: Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal.</td></tr>
<tr><td>STRAP_CPU</td><td>I</td><td>CPU Clock select (default 800Mhz).
<table>
<tr><th>TXD[3:0]</th><th>CPU Clock (MHz)</th></tr>
<tr><td>4’b0000</td><td>500</td></tr>
<tr><td>4’b0001</td><td>600</td></tr>
<tr><td>4’b0010</td><td>700</td></tr>
<tr><td>4’b0011</td><td>833</td></tr>
<tr><td>4’b0100</td><td>866</td></tr>
<tr><td>4’b0101</td><td>900</td></tr>
<tr><td>4’b0110</td><td>933</td></tr>
<tr><td>4’b0111</td><td>966 (not suggest)</td></tr>
<tr><td>4’b1000</td><td>1000 (not suggest)</td></tr>
<tr><td>4’b1001</td><td>1033 (not suggest)</td></tr>
<tr><td>4’b1010</td><td>1066 (not suggest)</td></tr>
<tr><td>4’b1011</td><td>1100 (not suggest)</td></tr>
<tr><td>4’b1100</td><td>1133 (not suggest)</td></tr>
<tr><td>4’b1101</td><td>1166 (not suggest)</td></tr>
<tr><td>4’b1110</td><td>1200 (not suggest)</td></tr>
<tr><td>4’b1111</td><td>800</td></tr>
</table></td></tr>
<tr><td>J6</td><td>TXEN</td><td>O</td><td>TXEN: This pin functions as Transmit Enable. It indicates that a transmission to an external PHY device is active on the MII port.</td></tr>
</table>

- **VGA DVO Interface (33 PINs)**

PIN No.	Symbol	Type	Description
AC1	G_FPD[0]	O	DVO data bus
	G_TVD[0]	O	TV output data bus
AE2	G_FPD[1]	O	DVO data bus
	G_TVD[1]	O	TV output data bus
AB5	G_FPD[2]	O	DVO data bus
	G_TVD[2]	O	TV output data bus
W5	G_FPD[3]	O	DVO data bus
	G_TVD[3]	O	TV output data bus
AD3	G_FPD[4]	O	DVO data bus
	G_TVD[4]	O	TV output data bus
Y6	G_FPD[5]	O	DVO data bus
	G_TVD[5]	O	TV output data bus
Y3	G_FPD[6]	O	DVO data bus
	G_TVD[6]	O	TV output data bus

PIN No.	Symbol	Type	Description
	G_STRAP[1]	I	Bypass clock mode 0:normal clock operation 1:Bypass all clock with test clock input(Test Mode)
AC6	G_FPD[7]	O	DVO data bus
	G_TVD[7]	O	TV output data bus
	G_STRAP[2]	I	PCI debug enable 0: Disable 1: Enable
AC3	G_FPD[8]	O	DVO data bus
	G_TVD[8]	O	TV output data bus
	G_STRAP[3]	I	DVP2 port/Capture port select Default : Pull-down 0: DVP2 1: Capture
U5	G_FPD[9]	O	DVO data bus
	G_TVD[9]	O	TV output data bus
	G_STRAP[4]	I	DAC external source enable. 1: data from external pad. 0: data from internal BIST
W4	G_FPD[10]	O	DVO data bus
	G_TVD[10]	O	TV output data bus
AB1	G_FPD[11]	O	DVO data bus
	G_TVD[11]	O	TV output data bus
U4	G_FP1DE	O	DVO data enable
	G_TVDE	O	TV output data enable
	G_STRAP[5]	I	PCI VGA config Pr-fetch status 0: Pre-fetch bit = 0 1: Pre-fetch bit = 1
AD1	G_FP1HS	O	DVO hsync
	G_TVHS	O	TV hsync
	G_STRAP[6]	I	DAC, PLL test enable
AC4	G_FP1VS	O	DVO vsync
	G_TVVS	O	TV vsync
	G_STRAP[7]	I	DVP1 port/TV port select 0:DVP1 1:TV
AD2	G_FP1CLK	O	DVO output clock
	G_TVCLKO	O	TV output clock
V5	G_TVCLKIN	I	TV input clock
AE4	G_FP1DET	I	DVO device detect
	G_TVDET	I	TV device detect
AB3	G_FPD[12]	O	DVO data bus
	G_CAPD[0]	I	Capture input data bus
AA2	G_FPD[13]	O	DVO data bus
	G_CAPD[1]	I	Capture input data bus

PIN No.	Symbol	Type	Description
N4	G_FPD[14]	O	DVO data bus
	G_CAPD[2]	I	Capture input data bus
AC5	G_FPD[15]	O	DVO data bus
	G_CAPD[3]	I	Capture input data bus
AA1	G_FPD[16]	O	DVO data bus
	G_CAPD[4]	I	Capture input data bus
V6	G_FPD[17]	O	DVO data bus
	G_CAPD[5]	I	Capture input data bus
AA6	G_FPD[18]	O	DVO data bus
	G_CAPD[6]	I	Capture input data bus
V2	G_FPD[19]	O	DVO data bus
	G_CAPD[7]	I	Capture input data bus
T4	G_FPD[20]	O	DVO data bus
	G_CAPFILD	I	Capture Fild
AA4	G_FPD[21]	O	DVO data bus
	G_CAPHS	I	Capture hsync
W1	G_FPD[22]	O	DVO data bus
	G_CAPVS	I	Capture vsync
U3	G_FPD[23]	O	DVO data bus
	G_CAPCLK	I	Capture input clock
Y1	G_ENVDD	O	Panel Power Sequence signal. "ENVDD"
AD4	G_ENBLT	O	Panel Power Sequence signal. "Enable Backlight"
U2	G_ENVEE	O	Panel Power Sequence signal. "ENVEE"

- **VGA DAC Interface (6 PINs)**

PIN No.	Symbol	Type	Description
T1	G_REXT	I	RESET DAC Signal. An external resistor is connected between REXT and GND to determine the reference current. Default is 511 Ohm.
N1	G_IOR	O	Analog Red
P1	G_IOG	O	Analog Green
R1	G_IOB	O	Analog Blue
AB4	G_VSYNC	O	CRT VSYNC
V1	G_HSYNC	O	CRT HSYNC

- **VGA GPIO Interface (2 PINs)**

PIN No.	Symbol	Type	Description
N6	G_GPIO[2]	IO	General I/O Port:clock

PIN No.	Symbol	Type	Description
N5	G_GPIO[3]	IO	General I/O Port:data
	G_STRAP[0]	I	Hardware strapping bus

- **VGA I2C Interface (4 PINs)**

PIN No.	Symbol	Type	Description
Y4	G_DDC_CLK	IOD	First DDC Clock.
Y5	G_DDC_DAT	IOD	First DDC Data.
V3	G_DDC1_CLK	IOD	Second DDC serial clock.
W3	G_DDC1_DAT	IOD	Second DDC serial data.

- **VGA Power Interface (11 PINs)**

PIN No.	Symbol	Type	Description
P4	VDD_DAC10	I	1V digital power of DAC Power
N3	AVDD_DACR18	I	DAC Power Pin for RED Channel, 1.8V
N2	AVSS_DACR18	I	DAC Ground Pin for RED Channel
P3	AVDD_DACG18	I	DAC Power Pin for GREEN Channel, 1.8V
P2	AVSS_DACG18	I	DAC Ground Pin for GREEN Channel
R3	AVDD_DACB18	I	DAC Power Pin for BLUE Channel, 1.8V
R2	AVSS_DACB18	I	DAC Ground Pin for BLUE Channel
T3	AVDD_DACBG18	I	DAC Power Pin for Bandgap, 1.8V
T2	AVSS_DACBG18	I	DAC Ground Pin for Bandgap, 1.8V
P6	AVDD_VDISPLL18	I	VGA Display PLL Analog Power
P5	AVSS_VDISPLL18	I	VGA Display PLL Ground

- **PCIE Power Interface (12 PINs)**

PIN No.	Symbol	Type	Description
C25	AVDD1_PE33	I	***Analogue Power*** PCIE 3.3V Power
B23	AVDD_PE12	I	***Analogue Power*** PCIE 1.2V Power
D26	AVDD1_PE12	I	***Analogue Power*** PCIE 1.2V Power
D24	AVDD_PERX12	I	***Analogue Power*** PCIE Receiver 1.2V Power
C24	AVSS_PERX12	I	***Analogue Ground*** PCIE Receiver 1.2V Ground
B27	AVDD1_PERX12	I	***Analogue Power*** PCIE Receiver 1.2V Power

PIN No.	Symbol	Type	Description
A27	AVSS1_PERX12	I	***Analogue Ground*** PCIE Receiver 1.2V Ground
A25	AVSS_PEPLL12	I	***Analogue Ground*** PCIE Analogue PLL 1.2V Ground
B25	AVDD1_PEPLL12	I	***Analogue Power*** PCIE PLL 1.2V Power
D25	AVSS1_PEPLL12	I	***Analogue Ground*** PCIE Analogue PLL 1.2V Ground
A23	AVSS_PE	I	PCIE Analogue Ground
C26	AVSS1_PE	I	PCIE Analogue Ground

- **SATA Power Interface (7 PINs)**

PIN No.	Symbol	Type	Description
W30	AVSS_SATA	I	***SATA PHY***: Analogue Ground
W29	AVDD_SATA12	I	***SATA PHY***: 1.2V Analogue Power
U30	AVSS_SATARX12	I	***SATA PHY***: Receiver Analogue Ground
U29	AVDD_SATARX12	I	***SATA PHY***: Receiver 1.2V Analogue Power
R30	AVDD_SATAPLL12	I	***SATA PHY***: PLL 1.2V Analogue Power
R29	AVSS_SATAPLL12	I	***SATA PHY***: PLL Analogue Ground
P29	AVDD_SATA33	I	***SATA PHY***: 3.3V Analogue Power

- **USB Power Interface (24 PINs)**

PIN No.	Symbol	Type	Description
M30	AVDD_USB33	I	***Analogue Power***: USB 3.3V Power
M29	AVSS_USB33	I	***Analogue Ground***: USB 3.3V Ground
J30	AVDD1_USB33	I	***Analogue Power***: USB 3.3V Power
J29	AVSS1_USB33	I	***Analogue Ground***: USB 3.3V Ground
F30	AVDD2_USB33	I	***Analogue Power***: USB 3.3V Power
F29	AVSS2_USB33	I	***Analogue Ground***: USB 3.3V Ground
C30	AVDD3_USB33	I	***Analogue Power***: USB 3.3V Power
C29	AVSS3_USB33	I	***Analogue Ground***: USB 3.3V Ground
J28	AVDD_USBBAS33	I	***Analogue Power***: USB Base Voltage 3.3V Power
N28	AVSS_USBBAS33	I	***Analogue Ground***: USB Base Voltage 3.3V Ground
C28	AVDD2_USBBAS33	I	***Analogue Power***: USB Base Voltage 3.3V Power
G28	AVSS2_USBBAS33	I	***Analogue Ground***: USB Base Voltage 3.3V Ground

PIN No.	Symbol	Type	Description
L28	AVDD_USB12	I	***Analogue Power***: USB 1.2V Power
H28	AVDD1_USB12	I	***Analogue Power***: USB 1.2V Power
E28	AVDD2_USB12	I	***Analogue Power***: USB 1.2V Power
B28	AVDD3_USB12	I	***Analogue Power***: USB 1.2V Power
K30	AVDD_USBPLL12	I	USB PLL Power
K29	AVSS_USBPLL12	I	USB PLL Ground
G30	AVDD1_USBPLL12	I	USB PLL Power
G29	AVSS1_USBPLL12	I	USB PLL Ground
D30	AVDD2_USBPLL12	I	USB PLL Power
D29	AVSS2_USBPLL12	I	USB PLL Ground
A29	AVDD3_USBPLL12	I	USB PLL Power
A28	AVSS3_USBPLL12	I	USB PLL Ground

- **ADC Power Interface (7 PINs)**

PIN No.	Symbol	Type	Description
E18	ADC_VCC33A_VREFP	I	ADC 3.3V Power
E17	ADC_VCC33A	I	ADC 3.3V Analogue Power
F16	ADC_VCC33D	I	ADC 3.3V Digital Power
F21	VCC18A_TEMP	I	Temperature Sensor 1.8V Power
D21	VCC18D_TEMP	I	Temperature Sensor 1.8V Power
C16	VCC18A_PLL5	I	Internal PLL 1.8V Power
C18	VCC18A_PLL7	I	Internal PLL 1.8V Power

- **Battery POWER (2 PINs)**

PIN No.	Symbol	Type	Description
D7	RTC_VDD33	I	Battery power for RTC
A8	RTC_VSS	I	Battery ground for RTC

- **1V POWER (15 PINs)**

PIN No.	Symbol	Type	Description
AE7,AE8,AE10,W11, W12,W13,W14,Y12,Y 13,Y14,Y15,AA12,AA 13,AA14,AA15	VDD10 (15 PINs)	I	CPU Core power

- **1.2V POWER (21 PINs)**

PIN No.	Symbol	Type	Description
K18,K19,L18,L19,L20,M19,M20,N19,N20,N21,P20,P21	VDD12 (12 PINs)	I	SB Core power
A16,A18,A21,C23	DIF_VD12IO (4 PINs)	I	Differential PAD 1.2V Power
B16,B18,B21,C22	DIF_VS12IO (4 PINs)	I	Differential PAD Ground
A9	AFE_VCCDL12	I	Internal Ethernet PHY Digital Logic Cell Core Power

- **1.8V POWER (32 PINs)**

PIN No.	Symbol	Type	Description
T10,T11,T12,T13,T14,U10,U11,U12,U13,U14,R14	VDD18 (11 PINs)	I	1.8V SB Analogue Power
AE5,AE12,AE15,AE16,AE20,AF3,AF7,AG13,AG20,AH14,AH17,AJ4,AJ6	DVDD18(13 PINs)	I	1.8V DDR Power
T6	AVDD_DDRPLL18	I	DRAM PLL Analog Power
T5	AVSS_DDRPLL18	I	DRAM PLL Analog Ground
R6	AVDD_CPUPLL18	I	CPU PLL Analog Power
R5	AVSS_CPUPLL18	I	CPU PLL Analog Ground
C15	AFE_VCCABG18	I	Internal Ethernet PHY Band Gap 1.8V Power
B11	AFE_VCCAPLL18	I	Internal Ethernet PHY PLL 1.8V Power
A15	AFE_VCCD18	I	Internal Ethernet PHY 1.8V Power
A13	AFE_RXVCCA18	I	Internal Ethernet PHY Receiver 1.8V Power

- **3.3V Power (18 PINs)**

PIN No.	Symbol	Type	Description
J3,K20,K21,W2,W6,L21,M21,Y17,Y18,Y19,N10,AA17,AA18,AA19,P10,AB2,AB6,AD6	VDD33 (18 PINs)	I	I/O PAD Power

- **Digital Ground (153 PINs)**

PIN No.	Symbol	Type	Description

PIN No.	Symbol	Type	Description
B2,B5,B8,C10,C20,D4,E2,E7,E10,E13,E15,E22,F5,F25,F27,AD29,AE1,AE3,G6,AE9,T15,T16,T17,T18,T19,H2,H5,H26,K2,K5,K17,K27,L16,L17,L25,M1,M2,M4,M6,M10,M11,M12,M13,M14,M15,M16,M17,M18,M27,N11,N12,N13,N14,N15,N16,N17,N18,N29,P11,P12,P13,P14,P15,P16,P17,P18,P19,P26,P28,R4,R10,R11,R12,R13,R15,R16,R17,R18,R19,R20,R21,T28,U1,U6,U15,U16,U17,U18,U19,V4,V10,V11,V12,V13,V14,V15,V16,V17,V18,V19,V25,V28,W10,W15,W16,W17,W18,W19,Y2,Y10,Y11,Y16,Y30,AA3,AA5,AA10,AA11,AA16,AA20,AA21,AA26,AB28,AC2,AC30,AD5,AE27,AF6,AF11,AF12,AF15,AF17,AF19,AF21,AF25,AG1,AG5,AG7,AG10,AH3,AH20,AH27,AH29,AJ7,AJ12,AJ16,AJ19,AJ22,AJ25,AK2,AK5,AK1	VSS	I	Digital Ground

PIN No.	Symbol	Type	Description
0,AK15,AK20			

- **Analogue Ground (13 PINs)**

PIN No.	Symbol	Type	Description
B9	AFE_VSSDL	I	Analogue Ground
A11	AFE_TXVSSA	I	Analogue Ground
B13	AFE_RXVSSA	I	Analogue Ground
B15	AFE_VSSD	I	Analogue Ground
C12	AFE_VSSAPLL	I	Analogue Ground
C14	AFE_VSSABG	I	Analogue Ground
D18	ADC_VSS33A_VREFN	I	Analogue Ground
D17	ADC_VSS33A	I	Analogue Ground
E16	ADC_VSS33D	I	Analogue Ground
E21	VSS18A_TEMP	I	Analogue Ground
C21	VSS18D_TEMP	I	Analogue Ground
C17	VSS18A_PLL5	I	Analogue Ground
C19	VSS18A_PLL7	I	Analogue Ground

- **NC pin (4 PINs)**

PIN No.	Symbol	Type	Description
A1	A1_NC	I	NC
A30	A30_NC	I	NC
AK1	AK1_NC	I	NC
AK30	AK30_NC	I	NC

4.5. PIN Capacitance Description

North-Bridge:

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance	1.94304	2.05082	2.08563	pF
C_{BID}	3.3V Bi-directional Capacitance	2.18057(max loading=40)	2.21818(max loading=40)	2.2269(max loading=40)	pF

VGA:

Symbol	Parameter	Min.	Max.	Unit
C_{BID}	3.3V Bi-directional Capacitance	2(max loading=40)	2.5(max loading=40)	pF

South-Bridge:

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance	3.144	3.143	3.216	pF
C_{BID}	3.3V Bi-directional Capacitance	3.179	3.116	3.099	pF