1. Overview

The **Vortex86DX** is a high performance and fully static 32-bit X86 processor with the compatibility of Windows based, Linux and most popular 32-bit RTOS. It also integrates 32KB write through 4-way L1 cache, 4-way 256KB L2 cache, PCI rev. 2.1 32-bit bus interface at 33 MHz, DDR2, ROM controller, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), Fast Ethernet, FIFO UART, USB2.0 Host and IDE controller within a single 581-pin BGA package to form a System-on--Chip **(SoC)**. It provides an ideal solution for the embedded system and communications products (such as thin client, NAT router, home gateway, access point and tablet PC) to bring about desired performance.

2. Features

- **x86 Compatible Processor Core**
  - 600MHz ~ 1GHz
  - 6 stage pipeline
- **Floating point unit support**
- **Embedded I / D Separated L1 Cache**
  - 16K I-Cache, 16K D-Cache
- **Embedded L2 Cache**
  - 4-way 256KB L2 Cache
  - Write through or write back policy
- **DDRII Control Interface**
  - 16 bits data bus
  - DDRII clock support up to 333MHz
  - DDRII size support up to 512Mbytes
- **IDE Controller**
  - Support 2 channels Ultra-DMA 100 (Disk x 4)
  - Primary channel support SD card
- **LPC (Low Pin Count) Bus Interface**
  - Support 2 programable registers to decode LPC address
- **MAC Controller x 1**
- **PCI Control Interface**
  - Up to 3 sets PCI master device
  - 3.3V I / O
- **ISA Bus Interface**
  - AT clock programmable
  - 8/16 Bit ISA device with Zero-Wait-State
  - Generate refresh signals to ISA interface during DRAM refresh cycle
- **DMA Controller**
- **Interrupt Controller**
- **Counter / Timers**
  - 2 sets of 8254 timer controller
  - Timer output is 5V tolerance I/O on 2nd Timer
- **MTBF Counter**
- **Real Time Clock**
  - Less than 2uA (3.0V) power comsuption in Internal RTC Mode while chip is power-off.
- **FIFO UART Port x 5 (5 sets COM Port)**
  - Compatible with 16C550 / 16C552
  - Default internal pull-up
  - Supports the programmable baud rate generator with the data rate from 50 to 460.8K bps
  - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
  - Support TXD_En Signal on COM1/COM2
  - Port 80h output data could be sent to COM1 by software programming
- **Parallel Port x 1**
  - Support SPP/EPP/ECP mode

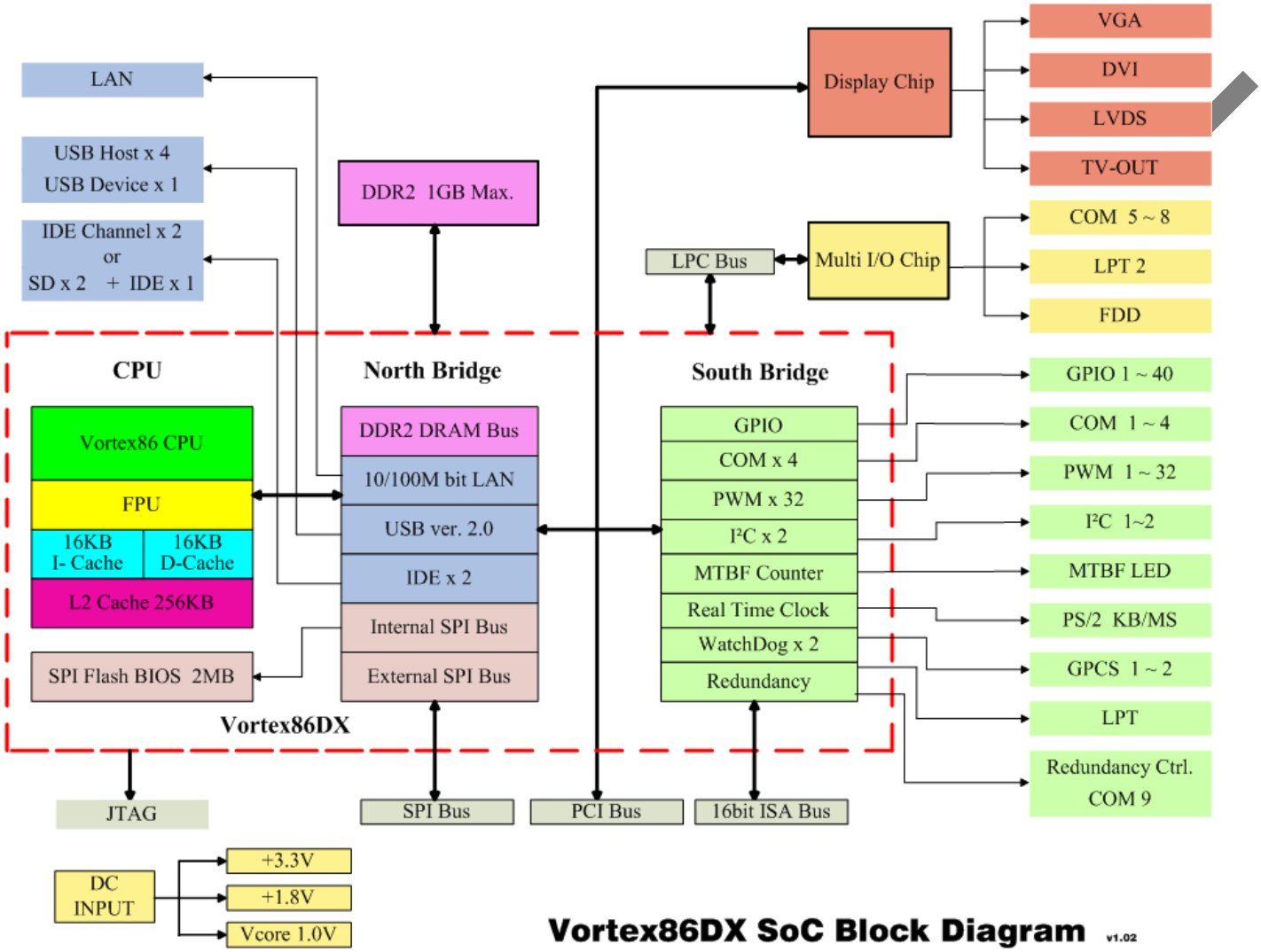
- **General Chip Selector**
  - 2 sets extended Chip Selector
  - I / O-map or Memory-map could be configurable
  - I / O Addressing: From 2 byte to 64 K byte
  - Memory Address: From 512 byte to 4G Byte
- **General Programmable I/O**
  - Supports 40 programmable I / O pins
  - Each GPIO pin can be individually configured to be an input/output pin
  - GPIO_P0~GPIO_P3 can be program by 8051
  - GPIO_P0 and GPIO_P1 with interrupt support (input/output)
- **USB 2.0 Host Support**
  - Supports HS, FS and LS
  - 4 port
- **USB 1.1 Device Support**
  - 1 port
  - Supports FS with 3 programmable endpoint
- **PS / 2 Keyboard and Mouse Interface Support**
  - Compatible with 8042 controller
- **Redundant System Support**
- **Speaker out**
- **Embedded 2MB Flash**
  - For BIOS storage
  - The Flash could be disable & use external Flash ROM
- **I^2C bus x 2**
  - Compliant w/t V2.1 **(Note 1)**
- **Servo Control interface support**
- **General Shift interface support**
- **JTAG Interface supported for S.W. debugging**
- **Input clock**
  - 14.318 MHz
  - 32.768 KHz
- **Output clock**
  - 24 MHz
  - 25 MHz
  - PCI clock
  - ISA clock
  - DDRII clock
- **Operating Voltage Range**
  - Core voltage: 0.95 V ~ 1.15V
  - I / O voltage: 1.8V ± 5% , 3.3 V ± 10 %
- **Operating temperature**
  - -40℃ ~ 85℃ **(Note 2)**
- **Package Type**
  - 27x27, 581 Ball BGA

Note 1: The I^2C bus is without the support of several mater code which are general call, START and CBUS

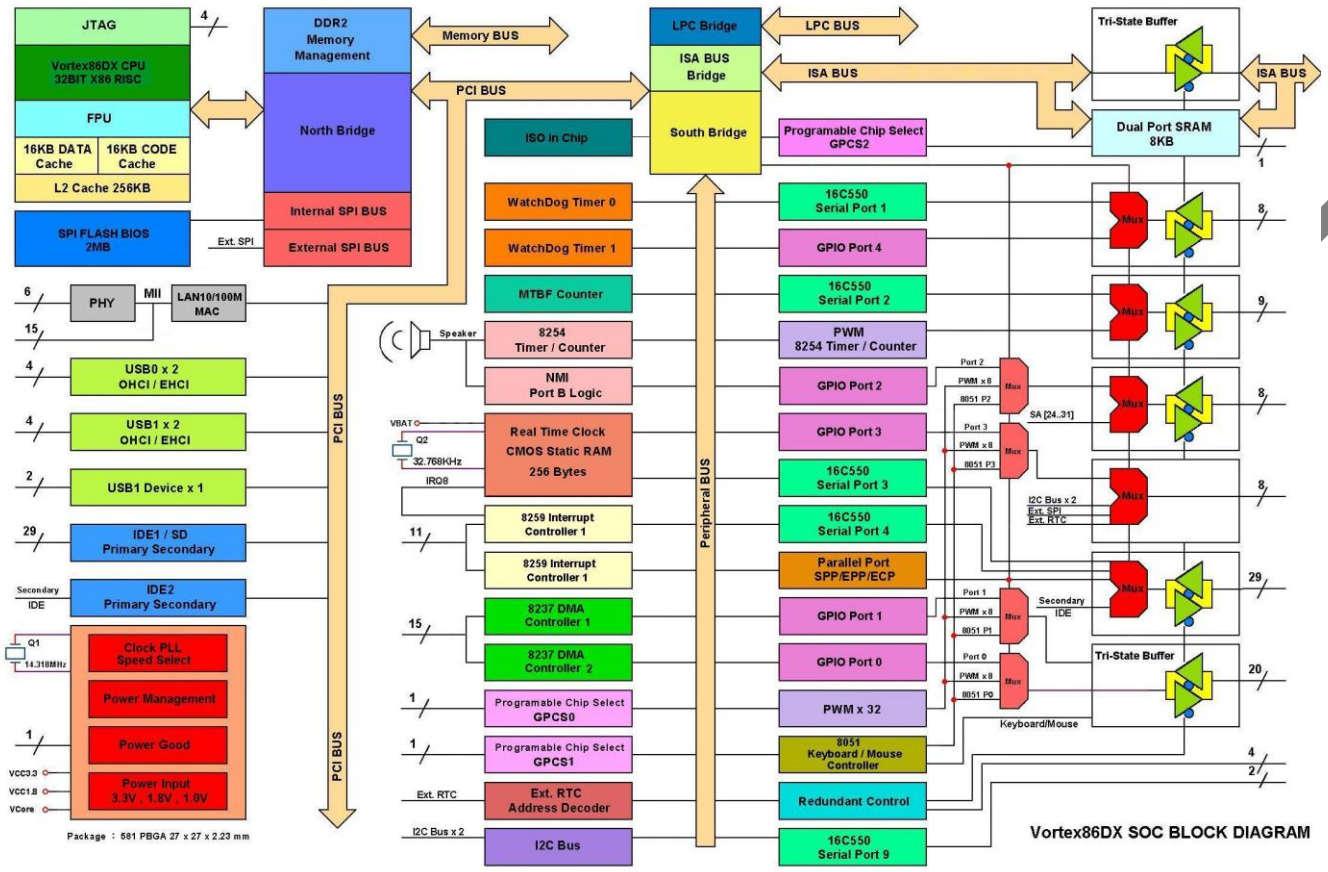
Note 2: The operating temperature of -40℃ ~ 85℃ is mainly for 600MHz, for higher CPU frequency, it will need a passive heatsik for heat dissipation.

3. Block Diagram

3.1. System Block Diagram



3.2. Functions Block Diagram



3.3. PCI Device List

ID SEL	AD 11	AD 12	AD 13	AD 14	AD 15	AD16	AD 17	AD 18	AD 19	AD 20	AD 21	AD 22	AD 23	AD 24	AD 25	AD 26	
Device#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Function0	NB	PCI Device					SB	MAC		USB OHCI	USB1 OHCI	IDE			USB Device		
Function1	NB1									USB EHCI	USB1 EHCI						

4. PIN Function List

4.1. BGA Ball Map

Top View

GND_R3 (VSS): F15,F16,F17,J13,K13,L13,M12,M13,N10,N11,N12,N13,N14,N15,N16

GNDK (VSS): E7,E8,E17,J10,J11,J12,K9,K10,K11,K12,L9,L10,L11,L12,M9,M10,M11

GNDO (VSS): D5,D6,E5,E6,F4,F5,F6,F7,G5

Vss_core (VSS): T16,T17,T18,U11,U12,U13,U14,U15,U16,V4,V11,V12,AB4,AB5,AB6,AC10,AC11,AC12

Vss_io (VSS): P17,P18,R11,R12,R15,R16,R17,R18,T9,T10,T13,T14,T15,U9,U17,V9,V17,W5,W6,AB21,AB22,AB23,AC20

VCC3V (VDD33): E18,F18,J15,K15,L15,M15,M16,P10,P11,P12,P13,P14

VCCK (VDD10): F8,F13,F14,G4,J14,K14,L14,M14,N9,P9

VCCO (VDD18): C4,C5,C6,C7,D4,D7,D8,E4

Vdd_core (VDD18): T11,T12,U10,V10,AA21,AA22,AA23,AC4,AC5,AC6

Vdd_io (VDD33): N17,N18,P15,P16,R9,R10,R13,R14,V3,W3,W4,AA4,AA5,AA6,AC21,AC22,AC23

NC Pin : A1,A2,A4,A8,A26,B1,B2,B7,B8,C1,C2,C8,D2,D3,D9,D10,E9,E10,G2,G3,J3,M6,N6,U21,U22,V21,V22,Y24,AA24,AF1,AF26

Signal Pin :

4.2. PIN Out Table

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
A1	NC	F17	VSS	P2	IDE_PA[1]	AA14	SD[4]
A2	NC	F18	VDD33	P3	IDE_PIORDY	AA15	LA[20]
A3	ODT[1]	F19	INTB#	P4	IDE_PDD[10]/ SD1_CMD	AA16	SD[3]
A4	NC	F20	INTC#	P5	IDE_PDD[12]/ SD1_DATA[0]	AA17	GPIO_P0[6]/ 8051_GPIO_P0[6]/ SERVO[6]
A5	VREF_0	F21	ATSTN	P6	CTS4#/IDE_SIOW#	AA18	GPIO_P0[7]/ 8051_GPIO_P0[7]/ SERVO[7]
A6	DQS#[0]	F22	ATSTP	P9	VDD10	AA19	GPIO_P1[7]/ 8051_GPIO_P1[7]/ SERVO[15]
A7	DQS[0]	F23	VDD33	P10	VDD33	AA20	GPIO_P2[7]/ 8051_GPIO_P2[7]/ SERVO[23]/SA[31]
A8	NC	F24	CBE#[0]	P11	VDD33	AA21	VDD18
A9	DRAMCLK#	F25	AD[9]	P12	VDD33	AA22	VDD18
A10	MA[0]	F26	AD[10]	P13	VDD33	AA23	VDD18
A11	MA[1]/ STRAP[1]	G1	RI3#/IDE_SIORDY	P14	VDD33	AA24	NC
A12	MA[10]/ STRAP[10]	G2	SOUT3	P15	VDD33	AA25	MTBF
A13	MD[6]	G3	SIN3	P16	VDD33	AA26	PWRGOOD
A14	MD[5]	G4	VDD10	P17	VSS	AB1	RST_DRV
A15	MD[2]	G5	VSS	P18	VSS	AB2	SA[14]
A16	MD[3]	G6	TDO	P21	VDD_BAT	AB3	DACK#[1]
A17	MD[4]	G7	TCK	P22	RTC_RD#/GPIO_P3[6]/ 8051_GPIO_P3[6]/ I2C1_SCL	AB4	VSS
A18	PCICLK[1]	G21	ROM_CS#/ SPICS#/STRAP_BMS	P23	AVSS_USB18	AB5	VSS
A19	PCICLK[0]	G22	CBE#[1]	P24	AVDD_USB33	AB6	VSS
A20	PCICLK[2]	G23	AD[11]	P25	AVSS_USBPLL18	AB7	SA[10]
A21	AD[29]	G24	PAR	P26	REXT	AB8	AEN
A22	AD[28]	G25	AD[7]	R1	IDE_PDRQ	AB9	SA[17]
A23	AD[27]	G26	AD[5]	R2	IDE_PA[0]	AB10	DACK#[5]
A24	AD[26]	H1	DSR3#/IDE_SCBLID#	R3	IDE_PIOW#/SD_RW#	AB11	SA[4]
A25	AD[25]	H2	CTS3#/IDE_SIOR#	R4	IDE_PDD[5]/ SD_DATA[1]	AB12	DRQ[0]
A26	NC	H3	RTS3#/IDE_SRST#	R5	IDE_PDD[2]/ SD_CMD	AB13	SA[2]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
B1	NC	H4	AVDD1_PLL18	R6	DCD4#/IDE_SA[2]	AB14	IRQ[9]
B2	NC	H5	AVSS_PLL18	R9	VDD33	AB15	LA[18]
B3	ODT[0]	H6	TDI	R10	VDD33	AB16	IOR#
B4	CS1#	H21	AD[8]	R11	VSS	AB17	GPIO_P1[1]/ 8051_GPIO_P1[1]/ SERVO[9]
B5	VREF_1	H22	AD[12]	R12	VSS	AB18	GPIO_P1[3]/ 8051_GPIO_P1[3]/ SERVO[11]
B6	OCDBIAS	H23	INTA#	R13	VDD33	AB19	GPIO_P2[0]/ 8051_GPIO_P2[0]/ SERVO[16]/SA[24]
B7	NC	H24	AD[0]	R14	VDD33	AB20	GPIO_P2[6]/ 8051_GPIO_P2[6]/ SERVO[22]/SA[30]
B8	NC	H25	AD[4]	R15	VSS	AB21	VSS
B9	DRAMCK	H26	AD[3]	R16	VSS	AB22	VSS
B10	MA[3]/ STRAP[3]	J1	INIT#/IDE_SDD[13]	R17	VSS	AB23	VSS
B11	MA[5]/ STRAP[5]	J2	DCD3#/IDE_SDRQ	R18	VSS	AB24	AVDD_PLL33
B12	MA[6]/ STRAP[6]	J3	NC	R21	VSS_BAT	AB25	CLK24MOUT
B13	MA[14]	J4	AVDD_PLL18	R22	RTC_IRQ[8]#/GPIO_P3[4]/ 8051_GPIO_P3[4]/ I2C_SCL	AB26	CLK25MOUT
B14	DQM[0]	J5	AVSS1_PLL18	R23	AVDD3_USB18	AC1	IRQ[6]
B15	MD[7]	J6	SOUT9	R24	AVDD_USB18	AC2	SA[6]
B16	MD[1]	J9	TMS	R25	USB3_DM	AC3	SA[0]
B17	MD[0]	J10	VSS	R26	USB3_DP	AC4	VDD18
B18	REQ#[1]	J11	VSS	T1	IDE_PDACK#	AC5	VDD18
B19	REQ#[2]	J12	VSS	T2	IDE_PCS0#	AC6	VDD18
B20	AD[30]	J13	VSS	T3	IDE_PDD[0]/ SD_DATA[2]	AC7	SA[8]
B21	AD[20]	J14	VDD10	T4	IDE_PDD[6]/ SD_CD	AC8	IRQ[12]
B22	AD[18]	J15	VDD33	T5	IDE_PDD[1]/ SD_DATA[3]	AC9	DRQ[2]
B23	AD[16]	J16	MDC	T6	DSR4#/IDE_SCS1#	AC10	VSS
B24	CBE#[2]	J17	TXD[2]	T9	VSS	AC11	VSS
B25	CBE#[3]	J18	TXD[3]	T10	VSS	AC12	VSS
B26	AD[24]	J21	TXC	T11	VDD18	AC13	SBHE#
C1	NC	J22	AD[6]	T12	VDD18	AC14	SD[2]
C2	NC	J23	AVDD_EPHYPLL33	T13	VSS	AC15	LA[23]
C3	CKE	J24	ISET	T14	VSS	AC16	GPCS0#

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
C4	VDD18	J25	AD[2]	T15	VSS	AC17	GPIO_P0[1]/ 8051_GPIO_P0[1]/ SERVO1
C5	VDD18	J26	AD[1]	T16	VSS	AC18	GPIO_P1[2]/ 8051_GPIO_P1[2]/ SERVO[10]
C6	VDD18	K1	IDE_PA[2]	T17	VSS	AC19	GPIO_P1[6]/ 8051_GPIO_P1[6]/ SERVO[14]
C7	VDD18	K2	PD[0]/IDE_SDD[0]	T18	VSS	AC20	VSS
C8	NC	K3	PD[3]/IDE_SDD[3]	T21	RTC_WR#/GPIO_P3[5]/ 8051_GPIO_P3[5]/ I2C_SDA	AC21	VDD33
C9	MA[2]	K4	PD[7]/IDE_SDD[7]	T22	RTC_PS	AC22	VDD33
C10	MA[4]/ STRAP[4]	K5	PD[6]/IDE_SDD[6]	T23	LAD[0]	AC23	VDD33
C11	MA[7] STRAP[7]	K6	SIN9	T24	AVSS3_USB18	AC24	AVSS_PLL33
C12	BA[2]	K9	VSS	T25	USB2_DM	AC25	DTR2#/PWM2_OUT
C13	WE#	K10	VSS	T26	USB2_DP	AC26	DCD2#/PWM_CLK
C14	MD[13]	K11	VSS	U1	IDE_PCBLID#	AD1	IRQ[4]
C15	MD[11]	K12	VSS	U2	IDE_PDD[4]/ SD_DATA[0]	AD2	SA[13]
C16	MD[9]	K13	VSS	U3	IDE_PDD[8]/ SD1_DATA[2]	AD3	SA[11]
C17	MD[14]	K14	VDD10	U4	IDE_PDD[7]/ SD_WP	AD4	DRQ[1]
C18	REQ#[0]	K15	VDD33	U5	IDE_PDD[11]/ SD1_CLK	AD5	SA[18]
C19	GNT#[0]	K16	MDIO	U6	RTS4#/IDE_SINT	AD6	SA[7]
C20	AD[31]	K17	TXD[1]	U9	VSS	AD7	IRQ[5]
C21	AD[21]	K18	TXD[0]	U10	VDD18	AD8	0WS#
C22	AD[19]	K21	TXEN	U11	VSS	AD9	DACK#[0]
C23	AD[17]	K22	DUPLEX	U12	VSS	AD10	SD[13]
C24	FRAME#	K23	AVSS_EPHYPLL33	U13	VSS	AD11	DACK#[6]
C25	IRDY#	K24	AVDD_EPHYRX33	U14	VSS	AD12	SD[8]
C26	TRDY#	K25	TXN	U15	VSS	AD13	LA[22]
D1	UD_DP	K26	TXP	U16	VSS	AD14	SD[6]
D2	NC	L1	STB#/IDE_SCS0#	U17	VSS	AD15	LA[19]
D3	NC	L2	PD[1]/IDE_SDD[1]	U18	LFRAME#	AD16	GPCS1#
D4	VDD18	L3	AFD#/IDE_SDD[15]	U21	EXTSYSFAILIN#	AD17	GPIO_P0[0]/ 8051_GPIO_P0[0]/ SERVO[0]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
D5	VSS	L4	ACK#/IDE_SDD[11]	U22	SYSFAILOUT#	AD18	GPIO_P2[3]/ 8051_GPIO_P2[3]/ SERVO[19]/SA[27]
D6	VSS	L5	PD[5]/IDE_SDD[5]	U23	LAD[1]	AD19	GPIO_P1[5]/ 8051_GPIO_P1[5]/ SERVO[13]
D7	VDD18	L6	PE/IDE_SDD[9]	U24	AVDD1_USB33	AD20	GPIO_P2[5]/ 8051_GPIO_P2[5]/ SERVO[21]/SA[29]
D8	VDD18	L9	VSS	U25	AVSS1_USBPLL18	AD21	TXD_EN1
D9	NC	L10	VSS	U26	REXT1	AD22	RI1#/GPIO_P4[3]/ 8051_GPIO_P4[3]/ SERVO[27]
D10	NC	L11	VSS	V1	IDE_PIOR#/SD1_RW#	AD23	DTR1#/GPIO_P4[5]/ 8051_GPIO_P4[5]/ SERVO[29]
D11	MA[9]/ STRAP[9]	L12	VSS	V2	IDE_PDD[15]/ SD1_WP	AD24	RI2#/PWM1_CLK
D12	BA[0]	L13	VSS	V3	VDD33	AD25	RTS2#/PWM1_OUT
D13	RAS#	L14	VDD10	V4	VSS	AD26	CTS2#/PWM1_GATE
D14	DQS#[1]	L15	VDD33	V5	RI4#/IDE_SA[1]	AE1	MEMCS16#
D15	MD[12]	L16	COL	V6	DTR4#/IDE_SA[0]	AE2	IRQ[3]
D16	MD[15]	L17	RXD[1]	V9	VSS	AE3	IOCS16#
D17	DQM[1]	L18	RXD[0]	V10	VDD18	AE4	BALE
D18	GNT#[1]	L21	RXDV	V11	VSS	AE5	SA[9]
D19	GNT#[2]	L22	LINK/ACTIVE	V12	VSS	AE6	IRQ[10]
D20	AD[23]	L23	AVSS_EPHYTX33	V13	KBCLK/KBRST#	AE7	IRQ[7]
D21	VSS	L24	AVDD1_EPHYTX33	V14	MSCLK	AE8	IOCHRDY
D22	TEST2	L25	RXN	V15	MSDATA	AE9	LA[17]
D23	TEST0	L26	RXP	V16	KBDATA/A20GATE#	AE10	SD[9]
D24	DEVSEL#	M1	IDE_PRST#	V17	VSS	AE11	SD[10]
D25	STOP#	M2	PD[2]/IDE_SDD[2]	V18	LDRQ#	AE12	MEMW#
D26	PCIRST#	M3	SLIN#/IDE_SDD[12]	V21	EXT_GPCS#	AE13	SA[5]
E1	UD_DM	M4	PD[4]/IDE_SDD[4]	V22	EXT_SWITCH_FAIL#	AE14	LA[21]
E2	TEST7	M5	BUSY/IDE_SDD[10]	V23	LAD[2]	AE15	DRQ[7]
E3	TEST5	M6	SOUT4	V24	AVDD1_USBPLL18	AE16	SD[15]
E4	VDD18	M9	VSS	V25	RTC_XOUT	AE17	GPIO_P0[4]/ 8051_GPIO_P0[4]/ SERVO[4]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
E5	VSS	M10	VSS	V26	RTC_XIN	AE18	GPIO_P0[5]/ 8051_GPIO_P0[5]/ SERVO[5]
E6	VSS	M11	VSS	W1	IDE_PCS1#	AE19	GPIO_P1[4]/ 8051_GPIO_P1[4]/ SERVO[12]
E7	VSS	M12	VSS	W2	IDE_PDD[14]/ SD1_CD	AE20	GPIO_P2[4]/ 8051_GPIO_P2[4]/ SERVO[20]/SA[28]
E8	VSS	M13	VSS	W3	VDD33	AE21	SIN1/GPIO_P4[4]/ 8051_GPIO_P4[4]/ SERVO[28]
E9	NC	M14	VDD10	W4	VDD33	AE22	SOUT1/GPIO_P4[1]/ 8051_GPIO_P4[1]/ SERVO[25]
E10	NC	M15	VDD33	W5	VSS	AE23	CTS1#/GPIO_P4[7]/ 8051_GPIO_P4[7]/ SERVO[31]
E11	MA[11]/ STRAP[11]	M16	VDD33	W6	VSS	AE24	SOUT2/PWM_OUT
E12	CAS#	M17	RXD[2]	W21	E_SPI_CS#/GPIO_P3[0]/ 8051_GPIO_P3[0]/ GSF_CH0	AE25	TXD_EN2/PWM2_GATE
E13	CS0#	M18	RXD[3]	W22	E_SPI_CLK/GPIO_P3[1]/ 8051_GPIO_P3[1]/ GSF_CH1	AE26	DSR2#/PWM_GATE
E14	MD[10]	M21	RXC	W23	LAD[3]	AF1	NC
E15	MD[8]	M22	AVSS_EPHYBG33	W24	SERIRQ	AF2	IRQ[14]
E16	DQS[1]	M23	AVDD_EPHYBG33	W25	AVSS2_USB18	AF3	IRQ[11]
E17	VSS	M24	AVSS1_EPHYTX33	W26	AVDD2_USB18	AF4	IRQ[15]
E18	VDD33	M25	USB1_DM	Y1	SD[1]	AF5	TC
E19	INTD#	M26	USB1_DP	Y2	IOW#	AF6	REFRESH#
E20	AD[22]	N1	IDE_PDD[3]/ SD_CLK	Y3	DACK#[3]	AF7	DACK#[7]
E21	SPIFL_WP#	N2	IDE_PINT	Y4	SD[5]	AF8	OSC14318
E22	TEST1	N3	IDE_PDD[9]/ SD1_DATA[3]	Y5	DRQ[3]	AF9	MEMR#
E23	SPIFL_Hold#	N4	ERR#/IDE_SDD[14]	Y6	SD[7]	AF10	SYSCLK
E24	AD[15]	N5	SLCT/IDE_SDD[8]	Y21	E_SPI_DO/GPIO_P3[2]/ 8051_GPIO_P3[2]/ GSF_CH2	AF11	DRQ[6]

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
E25	AD[14]	N6	SIN4	Y22	E_SPI_DI/GPIO_P3[3]/ 8051_GPIO_P3[3]/ GSF_CLK	AF12	SA[1]
E26	AD[13]	N9	VDD10	Y23	SPEAKER/STRAP_EPS	AF13	DACK#[2]
F1	DTR3#/IDE_SDACK#	N10	VSS	Y24	NC	AF14	SD[11]
F2	TEST8	N11	VSS	Y25	XIN_14318	AF15	SD[12]
F3	TEST6	N12	VSS	Y26	XOUT_14318	AF16	SD[14]
F4	VSS	N13	VSS	AA1	SA[15]	AF17	GPIO_P0[2]/ 8051_GPIO_P0[2]/ SERVO2
F5	VSS	N14	VSS	AA2	SA[12]	AF18	GPIO_P0[3]/ 8051_GPIO_P0[3]/ SERVO3
F6	VSS	N15	VSS	AA3	SA[16]	AF19	GPIO_P1[0]/ 8051_GPIO_P1[0]/ SERVO[8]
F7	VSS	N16	VSS	AA4	VDD33	AF20	GPIO_P2[2]/ 8051_GPIO_P2[2]/ SERVO[18]/SA[26]
F8	VDD10	N17	VDD33	AA5	VDD33	AF21	GPIO_P2[1]/ 8051_GPIO_P2[1]/ SERVO[17]/SA[25]
F9	MA[8]/ STRAP[8]	N18	VDD33	AA6	VDD33	AF22	RTS1#/GPIO_P4[2]/ 8051_GPIO_P4[2]/ SERVO[26]
F10	MA[12]/ STRAP[12]	N21	RTC_AS/GPIO_P3[7]/ 8051_GPIO_P3[7]/ I2C1_SDA	AA7	SD[0]	AF23	DSR1#/GPIO_P4[6]/ 8051_GPIO_P4[6]/ SERVO[30]
F11	MA[13]/ STRAP[13]	N22	AVDD1_USB18	AA8	SMEMW#	AF24	DCD1#/GPIO_P4[0]/ 8051_GPIO_P4[0]/ SERVO[24]
F12	BA[1]	N23	AVDD_USBPLL18	AA9	SA[19]	AF25	SIN2/PWM2_CLK
F13	VDD10	N24	AVSS1_USB18	AA10	SMEMR#	AF26	NC
F14	VDD10	N25	USB_DM	AA11	DRQ[5]		
F15	VSS	N26	USB_DP	AA12	SA[3]		
F16	VSS	P1	IDE_PDD[13]/ SD1_DATA[1]	AA13	IOCHCK#		

4.3. Pin List Table

Function	Symbol	PIN Sum
SYSTEM	PWRGOOD, CLK25MOUT, XOUT_14318, XIN_14318, MTBF, CLK24MOUT, SPEAKER	7 PINs
DDRII	DRAMCK, DRAMCLK#, RAS#, CAS#, WE#, CKE,CS1#, CS0#, DQM[1:0], DQS[1:0], DQS#[1:0], ODT[1:0], OCDBIAS, VREF_0, VREF_1, BA[2:0],MD[15:0], MA[14:0]	53 PINs
USB Interface	USB_DP[3:0],USB_DM[3:0],REXT[1:0]	10 PINs
PCI	REQ#[2:0],GNT#[2:0],PCIRST#,PCICLK[0], PCICLK[1],PCICLK[2],AD[31:0],CBE#[3:0], FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#,PAR, INTA#, INTB#, INTC#, INTD#	56 PINs
External SPI/ GPIO port 3[3:0]/ 8051 GPIO port 3[3:0]/ General Shift	E_SPI_CS/GPIO_P3[0]/8051_GPIO_P3[0]/GSF_CH0, E_SPI_CLK/GPIO_P3[1]/8051_GPIO_P3[1]/GSF_CH1, E_SPI_DO/GPIO_P3[2]/8051_GPIO_P3[2]/GSF_CH2, E_SPI_DI/GPIO_P3[3]/8051_GPIO_P3[3]/GSF_CLK	4 PINs
ISA BUS	IOCHCK#, SD[15:0], IOCHRDY, AEN, SA[19:0], SBHE#, LA[23:17], MEMR#, MEMW#, RST_DRV, IRQ[15:14], IRQ[12:9], IRQ[7:3], DRQ[7:5], DRQ[3:0], 0WS#, SMEMR#, SMEMW#, IOW#, IOR#, DACK#[7:5], DACK#[3:0], REFRESH#, SYSCLK, TC, BALE, MEMCS16#,IOCS16#, OSC14318	87 PINs
Chip Selection	GPCS0#, GPCS1# , ROM_CS#	3 PINs
Redundant	EXTSYSFAILIN#, SYSFAILOUT#, EXT_SWITCH_FAIL#, EXT_GPCS#	4 PINs
KBD / MOUSE	KBCLK/KBRST#, KBDATA/A20GATE#, MSCLK, MSDATA	4 PINs
RTC/ GPIO PORT 3[7-4]/ 8051 GPIO PORT 3[7-4]/ I2C	RTC_AS/GPIO_P3[7]/8051_GPIO_P3[7]/I2C1_SDA, RTC_RD#/GPIO_P3[6]/8051_GPIO_P3[6]/I2C1_SCL, RTC_WR#/GPIO_P3[5]/8051_GPIO_P3[5]/I2C_SDA, RTC_IRQ8#/GPIO_P3[4]/8051_GPIO_P3[4]/I2C_SCL, RTC_PS, RTC_XOUT, RTC_XIN	7 PINs
COM1/ GPIO PORT 4/ 8051 GPIO PORT 4/ SERVO[31:24]	SIN1/GPIO_P4[4]/8051_GPIO_P4[4]/SERVO[28], SOUT1/GPIO_P4[1]/8051_GPIO_P4[1]/SERVO[25], RTS1#/GPIO_P4[2]/8051_GPIO_P4[2]/SERVO[26], CTS1#/GPIO_P4[7]/8051_GPIO_P4[7]/SERVO[31] , DSR1#/GPIO_P4[6]/8051_GPIO_P4[6]/SERVO[30], DCD1#/GPIO_P4[0]/8051_GPIO_P4[0]/SERVO[24] , RI1#/GPIO_P4[3]/8051_GPIO_P4[3]/SERVO[27] , DTR1#/GPIO_P4[5]/8051_GPIO_P4[5]/SERVO[29], TXD_EN1	9 PINs
COM2/ PWM	SIN2 / PWM2_CLK, SOUT2 / PWM_OUT, RTS2# / PWM1_OUT, CTS2# / PWM1_GATE, DSR2# / PWM0_GATE, DCD2# / PWM_CLK, RI2# / PWM1_CLK, DTR2# / PWM2_OUT, TXD_EN2 / PWM2_GATE	9 PINs
COM 3,4,9	SIN3, SOUT3, SIN4, SOUT4, SIN9, SOUT9	6 PINs
Primary IDE/SD	IDE_PDD[0]/SD_DATA[2], IDE_PDD[1]/SD_DATA[3], IDE_PDD[2]/SD_CMD, IDE_PDD[3]/SD_CLK, IDE_PDD[4]/SD_DATA[0], IDE_PDD[5]/SD_DATA[1], IDE_PDD[6]/SD_CD, IDE_PDD[7]/SD_WP, IDE_PDD[8]/SD1_DATA[2],	29 PINs

Function	Symbol	PIN Sum
	IDE_PDD[9]/SD1_DATA[3], IDE_PDD[10]/SD1_CMD, IDE_PDD[11]/SD1_CLK, IDE_PDD[12]/SD1_DATA[0], IDE_PDD[13]/SD1_DATA[1], IDE_PDD[14]/SD1_CD, IDE_PDD[15]/SD1_WP, IDE_PRST#, IDE_PDRQ, IDE_PIOW#/SD_RW#, IDE_PIOR#/SD1_RW#, IDE_PIORDY, IDE_PDACK#, IDE_PINT, PA[2 :0], IDE_PCBLID#, IDE_PCS0#, IDE_PCS1#	
Secondary IDE/COM3, COM4 and Parallel Port	PD/IDE_SDD[7 :0], SLCT/IDE_SDD[8], PE/IDE_SDD[9], BUSY/IDE_SDD[10], ACK#/IDE_SDD[11], SLIN#/IDE_SDD[12], INIT#/IDE_SDD[13], ERR#/IDE_SDD[14], AFD#/IDE_SDD[15], RTS3#/IDE_SRST#, DCD3#/IDE_SDRQ, CTS4#/IDE_SIOW#, CTS3#/IDE_SIOR#, RI3#/IDE_SIORDY, DTR3#/IDE_SDACK#, RTS4#/IDE_SINT, RI4#/IDE_SA[1], DSR3#/IDE_SCBLID#, DTR4#/IDE_SA[0], DCD4#/IDE_SA[2], STB#/IDE_SCS0#, DSR4#/IDE_SCS1#	29 PINs
LPC	SERIRQ, LAD[3:0], LFRAME#, LDRQ#	7 PINs
GPIO PORT 0,1,2/ 8051 GPIO PORT 0, 1, 2/ SERVO[23:0]/ SA[31:24]	GPIO_P0[7:0] /8051_GPIO_P0[7:0]/SERVO[7:0],GPIO_P1[7:0] /8051_GPIO_P1[7:0]/SERVO[15:8], GPIO_P2[0]/8051_GPIO_P2[0]/SERVO[16]/SA[24], GPIO_P2[1]/8051_GPIO_P2[1]/SERVO[17]/SA[25], GPIO_P2[2]/8051_GPIO_P2[2]/SERVO[18]/SA[26], GPIO_P2[3]/8051_GPIO_P2[3]/SERVO[19]/SA[27], GPIO_P2[4]/8051_GPIO_P2[4]/SERVO[20]/SA[28], GPIO_P2[5]/8051_GPIO_P2[5]/SERVO[21]/SA[29], GPIO_P2[6]/8051_GPIO_P2[6]/SERVO[22]/SA[30], GPIO_P2[7]/8051_GPIO_P2[7]/SERVO[23]/SA[31]	24 PINs
Ethernet	LINK/ACTIVE, DUPLEX, ISET, ATSTP, ATSTN, TXN, TXP, RXN, RXP MDC,MDIO, COL, RXC, RXD[0], RXD[1], RXD[2], RXD[3], RXDV, TXC, TXD[0], TXD[1], TXD[2], TXD[3], TXEN	24 PINs
USB Device	UD_DP, UD_DM	2 PINs
JTAG	TDO, TMS, TCK, TDI	4 PINs
TEST PIN	TEST[8:5], TEST[2:0]	7 PINs
SPIL Embedded flash control PIN	SPIFL_WP#, SPIFL_Hold#	2 PINs
1 V Power	VDD10 : 10 PINS	10 PINs
1.8V Power	VDD18(DDRII power): 8 PINs, VDD18(SB Core power): 10 PINs, AVDD_USB18, AVSS_USB18, AVDD_USBPLL18,AVSS_USBPLL18, AVDD1_PLL18, AVDD_PLL18, AVSS1_PLL18, AVSS_PLL18	34 PINs
Battery Power	VDD_BAT, VSS_BAT : 2 PINs	2 PINs
3.3V Power	AVDD_PLL33, AVSS_PLL33, VDD33(CPU IO pad power) : 12 PINs, VDD33(SB IO pad power) : 18 PINs, AVSS_EPHYPLL33, AVDD_EPHYPLL33, AVSS_EPHYBG33, AVDD_EPHYBG33, AVDD1_EPHYTX33, AVSS1_EPHYTX33, AVDD_EPHYRX33, AVSS_EPHYRX33,AVDD1_USB33, AVDD_USB33	42 PINs
Digital Ground	VSS : PINs	83 PINs

4.4. Signal Description

This chapter provides a detailed description of SoC signals. A signal with the symbol "#" at the end of itself indicates that this pin is low active. Otherwise, it is high active.

The following notations are used to describe the signal types:

I Input pin

O Output pin

OD Output pin with open-drain

I/O Bi-directional Input/Output pin

- **System (7 PINs)**

PIN No.	Symbol	Type	Description
AA26	PWRGOOD	I	***Power-Good Input.*** This signal comes from Power Good of the power supply to indicate that the power is available. The SoC uses this signal to generate reset sequence for the system.
AB26	CLK25MOUT	O	***25MHz Clock output.***
Y26	XOUT_14318	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator).
Y25	XIN_14318	I	***Crystal-in.*** 14.318MHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).
AA25	MTBF	O	***MTBF Flag output.***
AB25	CLK24MOUT	O	***24MHz Clock output***
Y23	SPEAKER	O	***Speaker Output.*** This pin is used to control the Speaker Output and should be connected to the Speaker
	STRAP_EPS	I	***Ethernet PHY Select*** Pull it low to select internal PHY. Pull it high to select External PHY. Tri-state to select Internal PHY AFE-test Mode. Default internal tri-state.

- **DDRII Interface (53 PINs)**

PIN No.	Symbol	Type	Description
B9	DRAMCK	O	***Clock output.*** This pin provides the fundamental timing for the DDRII controller.
A9	DRAMCLK#	O	***Clock output.*** This pin provides the fundamental timing for the DDRII controller.
D13	RAS#	O	***Row Address Strobe.*** When asserted, this signal latches row address on positive edge of the DDRII clock. This signal also allows row access and pre-charge.
E12	CAS#	O	***Column Address Strobe.*** When asserted, this signal latches column address on the positive edge of the DDRII clock. This signal also allows column access and pre-charge.

PIN No.	Symbol	Type	Description
C13	WE#	O	***Memory Write Enable.*** This pin is used as a write enable for the memory data bus.
C3	CKE	O	***Clock Enable.*** CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers.
B4, E13	CS1# CS0#	O	***Chip Select CS1# & CS0#.*** These two pins activate the DDRII devices. First Bank of DDRII accepts any command when the CS0# pin is active low. Second Bank of DDRII accepts any command when the CS1# pin is active low.
D17, B14	DQM[1:0]	O	***Data Mask DQM[1:0].*** These pins act as synchronized output enables during read cycles and byte masks during write cycles.
E16, A7	DQS[1:0]	I/O	***Data Strobe DQS[1:0] for DDRII only.*** Output with write data, input with the read data for source synchronous operation.
D14, A6	DQS#[1:0]	I/O	***Data Strobe DQS#[1:0] for DDRII only.*** Output with write data, input with the read data for source synchronous operation.
A3, B3	ODT[1:0]	O	***On Die Termination Control for DDRII only.*** ODT(registered HIGH) enables on die termination resistance internal to the DDR2 SDRAM.
B6	OCDBIAS	I	***OCD BIAS for DDRII only.*** The OCD bias circuit generates a bias level voltage that makes the reference resistance for driver impedance calibration an appropriate value
A5	VREF_0	I	***Reference voltage for DDRII only.*** Reference voltage for inputs for SSTL interface.
B5	VREF_1	O	***Reference voltage for DDRII only.*** Reference voltage for inputs for SSTL interface.
C12, F12,D12	BA[2:0]	O	***Bank Address BA[2:0].*** These pins are connected to DDRII as bank address pins.
D16, C17, C14, D15, C15, E14, C16, E15, B15, A13, A14, A17, A16, A15, B16, B17	MD[15:0]	I/O	***Memory Data MD[15:0].*** These pins are connected to the DDRII data bus.
A10	MA[0]	O	***Memory Address MA[0].*** Normally, these pins are used as the row and column address for DDRII.
A11	MA[1]	O	***Memory Address MA[1].*** Normally, these pins are used as the row and column address for DDRII.
	STRAP[1]	I	***STRAP[1].*** Pull it high to enable GPIO2. Default pull high. Pull it low to enable Address[31:24].
C9	MA[2]	O	***Memory Address MA[2].*** Normally, these pins are used as the row and column address for DDRII.

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td rowspan="2">B10</td><td>MA[3]</td><td>O</td><td>Memory Address MA[3]. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>STRAP[3]</td><td>I</td><td>STRAP[3]. PLL_TEST_OUT_EN_, Default pull low.
Pull it high to enable PLL_TEST_OUT_EN_.
Pull it low to disable PLL_TEST_OUT_EN_.</td></tr>
<tr><td rowspan="2">C10</td><td>MA[4]</td><td>O</td><td>Memory Address MA[4]. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>STRAP[4]</td><td>I</td><td>STRAP[4]. DDRII clock select, Default tri-state. About the DDRII clock strap table, please reference STRAP[10].</td></tr>
<tr><td rowspan="2">C11,B12,B11</td><td>MA[7:5]</td><td>O</td><td>Memory Address MA[7:5]. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>STRAP[7:5]</td><td>I</td><td>STRAP[7:5]. CPU Clock select, default tri-state.
<table>
<tr><th>STRAP[7,6,5]</th><th>CPU Clock (MHz)</th></tr>
<tr><td>3’b11z</td><td>Bypass mode</td></tr>
<tr><td>3’b101</td><td>SYN_DISABLE_
(CPU clock same to DDRII Clock)</td></tr>
<tr><td>3’b100</td><td>500</td></tr>
<tr><td>3’b110</td><td>600</td></tr>
<tr><td>3’b111</td><td>700</td></tr>
<tr><td>3’bzzz</td><td>800 (default)</td></tr>
<tr><td>3’bzz0</td><td>833</td></tr>
<tr><td>3’bzz1</td><td>866</td></tr>
<tr><td>3’bz0z</td><td>900</td></tr>
<tr><td>3’bz00</td><td>933</td></tr>
<tr><td>3’bz01</td><td>966</td></tr>
<tr><td>3’bz1z</td><td>1000</td></tr>
<tr><td>3’bz10</td><td>1033</td></tr>
<tr><td>3’bz11</td><td>1066</td></tr>
<tr><td>3’b0zz</td><td>1100</td></tr>
<tr><td>3’b0z0</td><td>1133</td></tr>
<tr><td>3’b0z1</td><td>1166</td></tr>
<tr><td>3’b00z</td><td>1200</td></tr>
<tr><td>3’b000</td><td>1233</td></tr>
<tr><td>3’b001</td><td>1266</td></tr>
<tr><td>3’b01z</td><td>1300</td></tr>
<tr><td>3’b010</td><td>1333</td></tr>
<tr><td>3’b011</td><td>1366</td></tr>
<tr><td>3’b1zz</td><td>1400</td></tr>
<tr><td>3’b1z0</td><td>1433</td></tr>
<tr><td>3’b1z1</td><td>1466</td></tr>
<tr><td>3’b10z</td><td>1500</td></tr>
</table></td></tr>
<tr><td rowspan="2">F9</td><td>MA[8]</td><td>O</td><td>Memory Address MA[8]. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>STRAP[8]</td><td>I</td><td>STRAP[8]. Pull it high to enable JTAG. Default internal pull-high.</td></tr>
<tr><td>D11</td><td>MA[9]</td><td>O</td><td>Memory Address MA[9]. Normally, these pins are used as the row and column address for DDRII.</td></tr>
</table>

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td></td><td>STRAP[9]</td><td>I</td><td>STRAP[9]. Pulled low: 33 PINS is for Secondary IDE.
Pulled high: 33 PINS is for COM3/4 and Parallel Port. Default internal pull-high.</td></tr>
<tr><td rowspan="2">A12</td><td>MA[10]</td><td>O</td><td>Memory Address MA[10]. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>STRAP[10]</td><td>I</td><td>STRAP[10]. DDRII clock select, Default tri-state.
<table>
<tr><td>STRAP[10,4]</td><td>Frequency(MHz)</td></tr>
<tr><td>2’b01</td><td>166 (VortexDX default)</td></tr>
<tr><td>2’b1z</td><td>200</td></tr>
<tr><td>2’b10</td><td>233</td></tr>
<tr><td>2’b00</td><td>266</td></tr>
<tr><td>2’b0z</td><td>300</td></tr>
<tr><td>2’bz1</td><td>333</td></tr>
<tr><td>2’bz0</td><td>366</td></tr>
<tr><td>2’bzz</td><td>400 (default)</td></tr>
</table></td></tr>
<tr><td rowspan="2">E11</td><td>MA[11]</td><td>O</td><td>Memory Address MA[11]. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>STRAP[11]</td><td>I</td><td>STRAP[11]. Pulled low is Internal RTC. Default internal pull-low.
Pulled high is External RTC</td></tr>
<tr><td rowspan="2">F10</td><td>MA[12]</td><td>O</td><td>Memory Address MA[12]. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>STRAP[12]</td><td>I</td><td>STRAP[12]. 0 : flash-8bits
1 : Internal SPI. Default internal pull-high.</td></tr>
<tr><td rowspan="2">F11</td><td>MA[13]</td><td>O</td><td>Memory Address MA[13]. Normally, these pins are used as the row and column address for DDRII.</td></tr>
<tr><td>STRAP[13]</td><td>I</td><td>STRAP[13]. 0 : High speed PCI clock
1 : Normal speed PCI clock. Default internal pull-high.</td></tr>
<tr><td>B13</td><td>MA[14]</td><td>O</td><td>Memory Address MA[14]. Normally, these pins are used as the row and column address for DDRII.</td></tr>
</table>

- **USB Interface (10 PINs)**

PIN No.	Symbol	Type	Description
N26 N25	USB_DP USB_DM	I/O	Universal Serial Bus Controller 0 Port 0. These are the serial data pair for USB Port 0. 15kΩ pull down resistors are connected to DP and DM internally.
M26 M25	USB1_DP USB1_DM	I/O	Universal Serial Bus Controller 0 Port 1. These are the serial data pair for USB Port 1. 15kΩ pull down resistors are connected to DP and DM internally.
T26	USB2_DP	I/O	Universal Serial Bus Controller 1 Port 0. These are the serial data pair

PIN No.	Symbol	Type	Description
T25	USB2_DM		for USB Port 2. 15kΩ pull down resistors are connected to DP and DM internally.
R26 R25	USB3_DP USB3_DM	I/O	Universal Serial Bus Controller 1 Port 1. These are the serial data pair for USB Port 3. 15kΩ pull down resistors are connected to DP and DM internally.
U26	REXT1	I	Universal Serial Bus Controller 1 External Reference Resistance 470Ω ±1%
P26	REXT	I	Universal Serial Bus Controller 0 External Reference Resistance 470Ω ±1%

- **PCI Bus Interface (56 PINs)**

PIN No.	Symbol	Type	Description
B19, B18, C18	REQ#[2:0]	I	***PCI Bus Request.*** These signals are the PCI bus request signals used as inputs by the internal PCI arbiter.
D19, D18 ,C19	GNT#[2:0]	O	***PCI Bus Grant.*** These signals are the PCI bus grant output signals generated by the internal PCI arbiter.
D26	PCIRST#	O	***PCI Reset.*** This pin is used to reset PCI devices. When it is asserted low, all the PCI devices will be reset.
A19 A18 A20	PCICLK[0] PCICLK[1] PCICLK[2]	O	***PCI Clock Output.*** This clock is used by all of the SoC logic that is in the PCI clock domain.
C20, B20, A21 A22, A23, A24, A25, B26, D20, E20, C21, B21, C22, B22, C23, B23, E24, E25, E26, H22, G23, F26, F25, H21, G25, J22, G26, H25, H26, J25, J26, H24	AD[31:0]	I/O	***PCI Address and Data.*** The standard PCI address and data lines. The address is driven with PCI Frame assertion and data is driven or received in the following clocks.
B25, B24, G22, F24	CBE#[3:0]	I/O	***Bus Command and Byte Enables.*** During the address phase, CBE#[3:0] define the Bus Command. During the data phase, CBE#[3:0] define the Byte Enables.
C24	FRAME#	I/O	***PCI Frame*****.** This pin is driven by a PCI master to indicate the beginning and duration of a PCI transaction.
C25	IRDY#	I/O	***PCI Initiator Ready.*** This pin is asserted low by the master to indicate that it is able to transfer the current data transfer. A data was transferred if both IRDY# and TRDY# are asserted low during the rising edge of the PCI clock.

PIN No.	Symbol	Type	Description
C26	TRDY#	I/O	***PCI Target Ready*****.** This pin is asserted low by the target to indicate that it is able to receive the current data transfer. A data was transferred if both IRDY# and TRDY# are asserted low during the rising edge of the PCI clock.
D24	DEVSEL#	I/O	***Device Select.*** This pin is driven by the devices which have decoded the addresses belonging to them.
D25	STOP#	I/O	***PCI Stop.*** This pin is asserted low by the target to indicate that it is unable to receive the current data transfer.
G24	PAR	I/O	***PCI Parity*****.** This pin is driven to even parity by PCI master over the AD[31:0] and CBE#[3:0] bus during address and write data phases. It should be pulled high through a weak external pull-up resistor. The target drives parity during data read.
H23	INTA#	I	***PCI INTA#.*** PCI interrupt input A. It connects to PCI INTA# when normal modes of PCI Interrupts are supported.
F19	INTB#	I	***PCI INTB#.*** PCI interrupt input B. It connects to PCI INTB# when normal modes of PCI Interrupts are supported.
F20	INTC#	I	***PCI INTC#.*** PCI interrupt input C. It connects to PCI INTC# when normal modes of PCI Interrupts are supported.
E19	INTD#	I	***PCI INTD#.*** PCI interrupt input D. It connects to PCI INTD# when normal modes of PCI Interrupts are supported.

- **EXTERNAL SPI/GPIO PORT[3-0]/8051 GPIO PORT[3-0]/General Shifter Interface (4 PINs)**

PIN No.	Symbol	Type	Description
W21	E_SPI_CS#	O	***External SPI Chip Select***
	GPIO_P3[0]	I/O	***General-Purpose Input/Output Port 3 bit 0.***
	8051_GPIO_P3[0]	I/O	***8051 General-Purpose Input/Output Port 3 bit 0.***
	GSF_CH0	I/O	***General Shifter Channel 0***
W22	E_SPI_CLK	O	***External SPI Clock***
	GPIO_P3[1]	I/O	***General-Purpose Input/Output Port 3 bit 1***
	8051_GPIO_P3[1]	I/O	***8051 General-Purpose Input/Output Port 3 bit 1***
	GSF_CH1	I/O	***General Shifter Channel 1***
Y21	E_SPI_DO	O	***External SPI Data Ouput it connects to device SDI input.***
	GPIO_P3[2]	I/O	***General-Purpose Input/Output Port 3 bit 2***
	8051_GPIO_P3[2]	I/O	***8051 General-Purpose Input/Output Port 3 bit 2***
	GSF_CH2	I/O	***General Shifter Channel 2***
Y22	E_SPI_DI	I	***External SPI Data Input t it connects to device SDI output.***
	GPIO_P3[3]	I/O	***General-Purpose Input/Output Port 3 bit 3***
	8051_GPIO_P3[3]	I/O	***8051 General-Purpose Input/Output Port 3 bit 3***
	GSF_CLK	O	***General Shifter reference Clock***

- **ISA Bus Interface (87 PINs)**

PIN No.	Symbol	Type	Description
AA13	IOCHCK#	I	**I/O Channel Check**. Provides the system board with parity (error) information about memory or devices on the I/O channel.
AE16, AF16, AD10, AF15, AF14, AE11, AE10, AD12,Y6, AD14, Y4, AA14, AA16, AC14, Y1, AA7	SD[15:0]	I/O	**ISA high and low byte slot data bus**. These are the system data lines. These signals read data and vectors into CPU during memory or I/O read cycles or interrupt acknowledge cycles and outputs data from CPU during memory or I/O write cycles.
AE8	IOCHRDY	I/O	**ISA system ready**. This input signal is used to extend the ISA command width for the CPU and DMA cycles.
AB8	AEN	O	**ISA address enable**. This active high output indicates that the system address is enabled during the DMA refresh cycles.
AA3, AA1, AB2, AD2,AA2, AD3, AB7, AE5, AC7, AD6, AC2, AE13, AB11, AA12, AB13 AF12, AC3	SA[16:0]	I/O	**ISA slot address bus.** These signals are high impedance during hold acknowledge.
AA9, AD5, AB9	SA[19:17]	I/O	**ISA slot address bus.** ISA slot address bus for 62-pin slot.
AC13	SBHE#	I/O	**ISA Bus high enable.** In master cycle, it is an input polarity signal and is driven by the master device.
AC15, AD13, AE14, AA15, AD15, AB15, AE9	LA[23:17]	I/O	**ISA latched address bus**. These are input signal during ISA master cycle.
AF9	MEMR#	I/O	**ISA memory read**. This signal is an input during ISA master cycle.
AE12	MEMW#	I/O	**ISA memory write**. This signal is an input during ISA master cycle.
AB1	RST_DRV	O	**Driver Reset**. This output signal is driven active during system power up.
AF4, AF2, AC8, AF3, AE6, AB14, AE7, AC1, AD7, AD1, AE2	IRQ[15:14], IRQ[12:9], IRQ[7:3]	I	**Interrupt request signals**. These are interrupt request input signals.
AE15, AF11, AA11, Y5, AC9, AD4, AB12	DRQ[7:5], DRQ[3:0]	I	**DMA device request**. These are DMA request input signals.
AD8	0WS#	I	**ISA zero wait state**. This is the ISA device zero-wait state indicator signal. This signal terminates the CPU ISA command immediately.
AA10	SMEMR#	O	**ISA system memory read**. This signal indicates that the memory read cycle is for an address below 1M byte address.
AA8	SMEMW#	O	**ISA system memory write**. This signal indicates that the memory write cycle is for an address below 1M byte address.
Y2	IOW#	O	**ISA I/O write**. This signal is an input during ISA master cycle.

PIN No.	Symbol	Type	Description
AB16	IOR#	O	**ISA I/O read**. This signal is an input during ISA master cycle.
AF7, AD11, AB10, Y3, AF13, AB3, AD9	**DACK#[7:5]**, **DACK#[3:0]**	O	**DMA device acknowledge signals**. These are DMA acknowledge demultiplex select signals. Input function is for hardware setting.
AF6	REFRESH#	O	**Refresh cycle indicator**. ISA master uses this signal to notify DRAM needs refresh. During the memory controller's self-acting refresh cycle, M6117D drives this signal to the I/O channels.
AF10	SYSCLK	O	**System Clock Output**. This signal clocks the ISA bus.
AF5	TC	O	**DMA end of process**. This is the DMA channel terminal count indicating signal.
AE4	BALE	O	**Bus address latch enable**. BALE indicates the presence of a valid address at I/O slots.
AE1	MEMCS16#	I/O	ISA 16-bit memory device select indicator signal.
AE3	IOCS16#	I/O	ISA 16-bit I/O device select indicator signal.
AF8	**OSC14318**	O	14.318MHz clock out

- **Chip Selection Interface (3 PINs)**

PIN No.	Symbol	Type	Description
AC16	GPCS0#	O	**General-Purpose Chip Select 0**.
AD16	GPCS1#	O	**General-Purpose Chip Select 1**.
G21	ROM_CS#	O	***ROM Chip Select.*** This pin is used as a ROM chip select.
	SPICS#	O	***SPI Chip Select.*** This pin is used as SPI flash chip select.
	STRAP_BMS	I	***Boot Mode Select*** Pull it high to select Normal boot(Reset 250ms). Default internal pull-high. Pull it low to select Fast boot.

- **Redundant (4 PINs)**

PIN No.	Symbol	Type	Description
U21	**EXTSYSFAILIN#**	I	**External system fail input**. This pin is the system fail in for redundant.
U22	**SYSFAILOUT#**	O	**System fail output**. This pin is the system fail out for redundant.
V22	**EXT_SWITCH_FAIL#**	I	**External switch fail**. This pin is the switch input for redundant.
V21	**EXT_GPCS#**	I	**External GPCS input**. This pin is the GPCS in for redundant.

- **KBD/MOUSE Interface (4 PINs)**

PIN No.	Symbol	Type	Description
V13	KBCLK	I/O	**Keyboard Clock**. This pin is keyboard clock when used internal 8042.
	KBRST#	I	**Keyboard Reset**. This pin is Keyboard reset when used external 8042.
V16	KBDAT	I/O	**Keyboard Data**. This pin is keyboard data when used internal 8042.
	A20GATE#	I	**Address Bit 20 Mask**. This pin is A20 mask when used external 8042.

PIN No.	Symbol	Type	Description
V14	MSCLK	I/O	**Mouse Clock**. This pin is mouse clock when used internal 8042.
V15	MSDAT	I/O	**Mouse Data**. This pin is mouse data when used internal 8042.

- **RTC/GPIO PORT3[7-4]/8051 GPIO PORT3[7-4]/I2C Interface (7 PINs)**

PIN No.	Symbol	Type	Description
N21	RTC_AS	O	***RTC Address Strobe.*** This pin is used as the RTC Address Strobe and should be connected to the RTC.
	GPIO_P3[7]	I/O	***General-Purpose Input/Output Port 3 bit 7.***
	8051_GPIO_P3[7]	I/O	***8051 General-Purpose Input/Output Port 3 bit 7.***
	I2C1_SDA	I/O	***I2C1 Serial Data.***
P22	RTC_RD#	O	***RTC Read Command.*** This pin is used as the RTC Read Command and should be connected to the RTC.
	GPIO_P3[6]	I/O	***General-Purpose Input/Output Port 3 bit 6.***
	8051_GPIO_P3[6]	I/O	***8051 General-Purpose Input/Output Port 3 bit 6.***
	I2C1_SCL	I/O	***I2C1 Serial Clock.***
T21	RTC_WR#	O	***RTC Write Command.*** This pin is used as the RTC Write Command and should be connected to the RTC.
	GPIO_P3[5]	I/O	***General-Purpose Input/Output Port 3 bit 5.***
	8051_GPIO_P3[5]	I/O	***8051 General-Purpose Input/Output Port 3 bit 5.***
	I2C_SDA	I/O	***I2C0 Serial Data.***
R22	RTC_IRQ[8]#	I	***RTC Interrupt Input.*** This pin is used as the RTC Interrupt input.
	GPIO_P3[4]	I/O	***General-Purpose Input/Output Port 3 bit 4.***
	8051_GPIO_P3[4]	I/O	***8051 General-Purpose Input/Output Port 3 bit 4.***
	I2C_SCL	I/O	***I2C0 Serial Clock.***
T22	RTC_PS	I	***RTC Battery Power Sense.***
V25	RTC_XOUT	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator)
V26	RTC_XIN	I	***Crystal-in.*** 32.768KHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).

- **COM1/PORT4/8051 PORT 4/SERVO[31:24] Interface (9 PINs)**

PIN No.	Symbol	Type	Description
AE21	SIN1	I	***Receive Data.*** FIFO UART receiver serial data input signal.
	GPIO_P4[4]	I/O	***General-Purpose Input/Output Port 4 bit 4.***

PIN No.	Symbol	Type	Description
	8051_GPIO_P4[4]	I/O	***8051 General-Purpose Input/Output Port 4 bit 4.***
	SERVO[28]	O	***SERVO[28].***
AE22	SOUT1	O	***Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	GPIO_P4[1]	I/O	***General-Purpose Input/Output Port 4 bit 1.***
	8051_GPIO_P4[1]	I/O	***8051 General-Purpose Input/Output Port 4 bit 1.***
	SERVO[25]	O	***SERVO[25].***
AF22	RTS1#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS1# signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	GPIO_P4[2]	I/O	***General-Purpose Input/Output Port 4 bit 2.***
	8051_GPIO_P4[2]	I/O	***8051 General-Purpose Input/Output Port 4 bit 2.***
	SERVO[26]	O	***SERVO[26].***
AE23	CTS1#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS1# signal by reading bit 4 of Modem Status Register (MSR). A CTS1# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS1# changes the state. The CTS1# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS1#.*
	GPIO_P4[7]	I/O	***General-Purpose Input/Output Port 4 bit 7.***
	8051_GPIO_P4[7]	I/O	***8051 General-Purpose Input/Output Port 4 bit 7.***
	SERVO[31]	O	***SERVO[31].***
AF23	DSR1#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR1# signal by reading bit5 of the Modem Status Register (MSR). A DSR1# signal states the change from low to high after the last MSR read sets bit1 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR1# changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR1#.*
	GPIO_P4[6]	I/O	***General-Purpose Input/Output Port 4 bit 6.***
	8051_GPIO_P4[6]	I/O	***8051 General-Purpose Input/Output Port 4 bit 6.***
	SERVO[30]	O	***SERVO[30].***

PIN No.	Symbol	Type	Description
AF24	DCD1#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD1# signal by reading bit 7 of the Modem Status Register (MSR). A DCD1# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD1# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD1#.*
	GPIO_P4[0]	I/O	***General-Purpose Input/Output Port 4 bit 0.***
	8051_GPIO_P4[0]	I/O	***8051 General-Purpose Input/Output Port 4 bit 0.***
	SERVO[24]	O	***SERVO[24].***
AD22	RI1#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI1# signal by reading bit 6 of the Modem Status Register (MSR). An RI1# signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI1# changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI1#.*
	GPIO_P4[3]	I/O	***General-Purpose Input/Output Port 4 bit 3.***
	8051_GPIO_P4[3]	I/O	***8051 General-Purpose Input/Output Port 4 bit 3.***
	SERVO[27]	O	***SERVO[27].***
AD23	DTR1#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR1# signal to be inactive during the loop-mode operation.
	GPIO_P4[5]	I/O	***General-Purpose Input/Output Port 4 bit 5.***
	8051_GPIO_P4[5]	I/O	***8051 General-Purpose Input/Output Port 4 bit 5.***
	SERVO[29]	O	***SERVO[29].***
AD21	TXD_EN1	O	***COM1 TX Status.*** This pin will be high when COM1 is trnamitting.

- **COM2/PWM Interface (9 PINs)**

PIN No.	Symbol	Type	Description
AF25	SIN2	I	***COM2 Receive Data.*** FIFO UART receiver serial data input signal.
	PWM2_CLK	I	***PWM Timer2 Clock.*** This pin is PWM timer2 external clock input when SB register C0h bit2 is 1 (PINs for PWM).
AE24	SOUT2	O	***COM2 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.

PIN No.	Symbol	Type	Description
	PWM_OUT	O	***PWM Timer Output.*** This pin is PWM timer output when SB register C0h bit2 is 1 (PINs for PWM).
AD25	RTS2#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	PWM1_OUT	O	***PWM Timer1 Output.*** This pin is PWM timer1 output when SB register C0h bit2 is 1 (PINs for PWM).
AD26	CTS2#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS2# signal by reading bit 4 of Modem Status Register (MSR). A CTS2# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS2# changes the state. The CTS2# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS2#.*
	PWM1_GATE	I	***PWM Timer1 Gate.*** This pin is PWM timer1 gate mask when SB register C0h bit2 is 1 (PINs for PWM).
AE26	DSR2#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR2# signal by reading bit5 of the Modem Status Register (MSR). A DSR2# signal states the change from low to high after the last MSR read sets bit1 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR2# changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR2#.*
	PWM_GATE	I	***PWM Timer Gate.*** This pin is PWM timer gate mask when SB register C0h bit2 is 1 (PINs for PWM).
AC26	DCD2#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD2# signal by reading bit 7 of the Modem Status Register (MSR). A DCD2# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD2# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD2#.*
	PWM_CLK	I	***PWM Timer Clock.*** This pin is PWM timer external clock input when SB register C0h bit2 is 1 (PINs for PWM).

PIN No.	Symbol	Type	Description
AD24	**RI2#**	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
	PWM1_CLK	I	***PWM Timer1 Clock.*** This pin is PWM timer1 external clock input when SB register C0h bit2 is 1 (PINs for PWM).
AC25	**DTR2#**	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	PWM2_OUT	O	***PWM Timer2 Output.*** This pin is PWM timer1 output when SB register C0h bit2 is 1 (PINs for PWM).
AE25	TXD_EN2	O	***COM2 TX Status.*** This pin will be high when COM2 is trnamitting.
	PWM2_GATE	I	***PWM Timer2 Gate.*** This pin is PWM timer2 gate mask when SB register C0h bit2 is 1 (PINs for PWM).

- **COM3, 4, 9 (6 PINs)**

PIN No.	Symbol	Type	Description
G3	SIN3	I	***COM3 Receive Data.*** FIFO UART receiver serial data input signal.
G2	SOUT3	O	***COM3 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
N6	SIN4	I	***COM4 Receive Data.*** FIFO UART receiver serial data input signal.
M6	SOUT4	O	***COM4 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
K6	SIN9	I	***COM9 Receive Data.*** FIFO UART receiver serial data input signal.
J6	SOUT9	O	***COM9 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.

- **Primary IDE/SD Interface (29 PINs)**

PIN No.	Symbol	Type	Description
M1	**IDE_PRST#**	O	***IDE Primary Channel Reset.***
T3	IDE_PDD[0]	I/O	***IDE Primary Channel Data Bus Data 0.***
	SD_DATA[2]	I/O	***SD0 Data Bus Data 2.***
T5	IDE_PDD[1]	I/O	***IDE Primary Channel Data Bus Data 1.***
	SD_DATA[3]	I/O	***SD0 Data Bus Data 3.***

PIN No.	Symbol	Type	Description
R5	IDE_PDD[2]	I/O	***IDE Primary Channel Data Bus Data 2.***
	SD_CMD	I/O	***SD0 Command/Response.***
N1	IDE_PDD[3]	I/O	***IDE Primary Channel Data Bus Data 3.***
	SD_CLK	O	***SD0 Clock.***
U2	IDE_PDD[4]	I/O	***IDE Primary Channel Data Bus Data 4.***
	SD_DATA[0]	I/O	***SD0 Data Bus Data 0.***
R4	IDE_PDD[5]	I/O	***IDE Primary Channel Data Bus Data 5.***
	SD_DATA[1]	I/O	***SD0 Data Bus Data 1.***
T4	IDE_PDD[6]	I/O	***IDE Primary Channel Data Bus Data 6.***
	SD_CD	I	***SD0 Card Detect.***
U4	IDE_PDD[7]	I/O	***IDE Primary Channel Data Bus Data 7.***
	SD_WP	I	***SD0 Write Protect.***
U3	IDE_PDD[8]	I/O	***IDE Primary Channel Data Bus Data 8.***
	SD1_DATA[2]	I/O	***SD1 Data Bus Data 2.***
N3	IDE_PDD[9]	I/O	***IDE Primary Channel Data Bus Data 9.***
	SD1_DATA[3]	I/O	***SD1 Data Bus Data 3.***
P4	IDE_PDD[10]	I/O	***IDE Primary Channel Data Bus Data 10.***
	SD1_CMD	I/O	***SD1 Command/Response.***
U5	IDE_PDD[11]	I/O	***IDE Primary Channel Data Bus Data 11.***
	SD1_CLK	O	***SD1 Clock.***
P5	IDE_PDD[12]	I/O	***IDE Primary Channel Data Bus Data 12.***
	SD1_DATA[0]	I/O	***SD1 Data Bus Data 0.***
P1	IDE_PDD[13]	I/O	***IDE Primary Channel Data Bus Data 13.***
	SD1_DATA[1]	I/O	***SD1 Data Bus Data 1.***
W2	IDE_PDD[14]	I/O	***IDE Primary Channel Data Bus Data 14.***
	SD1_CD	I	***SD1 Card Detect.***
V2	IDE_PDD[15]	I/O	***IDE Primary Channel Data Bus Data 15.***
	SD1_WP	I	***SD1 Write Protect.***
R1	**IDE_PDRQ**	I	***IDE Primary Channel DMA Request.***
R3	**IDE_PIOW#**	O	***IDE Primary Channel IO Write Strobe.***
	SD_RW#	O	***SD Read/Write status. High active***
V1	**IDE_PIOR#**	O	***IDE Primary Channel IO Read Strobe.***
	SD1_RW#	O	***SD1 Read/Write status. High active***
P3	**IDE_PIORDY**	I	***IDE Primary Channel IO Channel Ready.***
T1	**IDE_PDACK#**	O	***IDE Primary Channel DMA Acknowledge.***
N2	**IDE_PINT**	I	***IDE Primary Channel Interrupt.***
K1, P2, R2	**IDE_PA[2:0]**	O	***IDE Primary Channel Device Address***
U1	**IDE_PCBLID#**	I	***IDE Primary Channel Cable Assembly Type Identifier.***

PIN No.	Symbol	Type	Description
W1	**IDE_PCS1#**	O	***IDE Primary Channel Chip Select.***
T2	**IDE_PCS0#**	O	***IDE Primary Channel Chip Select.***

- **Secondary IDE /COM3,4,PRINT1 Interface (29 PINs)**

PIN No.	Symbol	Type	Description
K4, K5, L5, M4, K3, M2, L2, K2	PD[7:0]	I/O	***Parallel port data bus bit .*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[7:0]	I/O	***IDE Secondary Channel Data Bus.***
N5	SLCT	I	***SLCT.*** An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	IDE_SDD[8]	I/O	***IDE Secondary Channel Data Bus.***
L6	PE	I	***PE.*** An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[9]	I/O	***IDE Secondary Channel Data Bus.***
M5	BUSY	I	***BUSY.*** An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	IDE_SDD[10]	I/O	***IDE Secondary Channel Data Bus.***
L4	ACK#	I	***ACK#.*** An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[11]	I/O	***IDE Secondary Channel Data Bus.***
M3	SLIN#	OD	***SLIN#.*** Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[12]	I/O	***IDE Secondary Channel Data Bus.***
J1	INIT#	OD	***INIT#.*** Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[13]	I/O	***IDE Secondary Channel Data Bus.***
N4	ERR#	I	***ERR#.*** An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[14]	I/O	***IDE Secondary Channel Data Bus.***
L3	AFD#	OD	***AFD#.*** An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SDD[15]	I/O	***IDE Secondary Channel Data Bus.***

PIN No.	Symbol	Type	Description
H3	RTS3#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	IDE_SRST#	O	***IDE Secondary Channel Reset.***
J2	DCD3#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD3# signal by reading bit 7 of the Modem Status Register (MSR). A DCD3# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD3# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD3#.*
	IDE_SDRQ	I	***IDE Secondary Channel DMA Request.***
P6	CTS4#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	IDE_SIOW#	O	***IDE Secondary Channel IO Write Strobe.***
H2	CTS3#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	IDE_SIOR#	O	***IDE Secondary Channel IO Read Strobe.***

PIN No.	Symbol	Type	Description
G1	RI3#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
	IDE_SIORDY	I	***IDE Secondary Channel IO Channel Ready.***
F1	DTR3#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	IDE_SDACK#	O	***IDE Secondary Channel DMA Acknowledge.***
U6	RTS4#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	IDE_SINT	I	***IDE Secondary Channel Interrupt.***
V5	RI4#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
	IDE_SA[1]	O	***IDE Secondary Channel Device Address.***
H1	DSR3#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*
	IDE_SCBLID#	I	***IDE Secondary Channel Cable Assembly Type Identifier.***

PIN No.	Symbol	Type	Description
V6	DTR4#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	IDE_SA[0]	O	***IDE Secondary Channel Device Address.***
R6	DCD4#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD4# signal by reading bit 7 of the Modem Status Register (MSR). A DCD4# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD4# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD4#.*
	IDE_SA[2]	O	***IDE Secondary Channel Device Address.***
L1	STB#	OD	***STB#.*** An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	IDE_SCS0#	O	***IDE Secondary Channel Chip Select.***
T6	DSR4#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*
	IDE_SCS1#	O	***IDE Secondary Channel Chip Select.***

- **LPC Bus Interface (7 PINs)**

PIN No.	Symbol	Type	Description
W24	SERIRQ	I/O	***Serial Interrupt Request.*** This pin is used to support the serial interrupt protocol of common architecture.
W23, V23, U23, T23	LAD[3:0]	I/O	***LPC Command, Address and Data LAD[3:0].*** These pins are used to be command/address/data pins of Low-Pin-Count Function.
U18	**LFRAME#**	O	***Low Pin Count FRAME# Signal.*** This signal is used as a frame signal of low pin count protocol..
V18	**LDRQ#**	I	***Low Pin Count DMA Request Signal.*** This signal is used as a DMA request signal of low pin count protocol.

- **GPIO Interface (24 PINs)**

PIN No.	Symbol	Type	Description
AA18, AA17, AE18, AE17, AF18, AF17, AC17, AD17,	GPIO_P0[7:0]	I/O	***General-Purpose Input/Output Port 0[7:0].*** Those pins can be programmed input or output individually.
	8051_GPIO_P0[7:0]	I/O	***8051 General-Purpose Input/Output Port 0[7:0].***
	SERVO[7:0]	O	***SERVO[7:0].***
AA19, AC19, AD19, AE19, AB18, AC18, AB17, AF19	GPIO_P1[7:0]	I/O	***General-Purpose Input/Output Port 1[7:0].*** Those pins can be programmed input or output individually.
	8051_GPIO_P1[7:0]	I/O	***8051 General-Purpose Input/Output Port 1[7:0].***
	SERVO[15:8]	O	***SERVO[15:8].***
AA20, AB20, AD20, AE20, AD18, AF20, AF21, AB19	GPIO_P2[7:0]	I/O	***General-Purpose Input/Output Port 2[7:0]*** . Those pins can be programmed input or output individually.
	8051_GPIO_P2[7:0]	I/O	***8051 General-Purpose Input/Output Port 2[7:0].***
	SERVO[23:16]	O	***SERVO[23:16].***
	SA[31:24]	O	***ISA Address[31:24].***

- **Ethernet Interface (24 PINs)**

PIN No.	Symbol	Type	Description
L22	LINK/ACTIVE	O	***LINK/ACTIVE:*** Link/active status
K22	DUPLEX	O	***DUPLEX:*** Duplex status
J24	ISET	I	***ISET:*** External resistor connecting pin for BIAS
F22	ATSTP	I/O	***ATSTP:*** Variable Gain Amplifier and ADC testing pin for input and output (positive)
F21	ATSTN	I/O	***ATSTN:*** Variable Gain Amplifier and ADC testing pin for input and output (negative)
K25	TXN	O	***TXN:*** 10B-T/100BT transmitting output pin/ reveiving input pin (positive)
K26	TXP	O	***TXP:*** 10B-T/100BT transmitting output pin/ reveiving input pin (negative)
L25	RXN	I	***RXN:*** 10B-T/100BT reveiving input pin/ transmitting output pin (positive)
L26	RXP	I	***RXP:*** 10B-T/100BT reveiving input pin/ transmitting output pin (negative)
J16	MDC	O	***MDC:*** MII management data clock is sourced by the SoC to the external PHY devices as a timing reference for the transfer of information on the MDIO signal.
K16	MDIO	I/O	***MDIO:*** MII management data input/output transfers control information and status between the external PHY and SoC.
L16	COL	I	***COL:*** This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
M21	RXC	I	***RXC:*** Supports the receive clock supplied by the external PMD device.

PIN No.	Symbol	Type	Description
			This clock should always be active.
M18, M17, L17, L18	**RXD[3:0]**	I	***RXD[3:0]:*** Four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal.
L21	RXDV	I	***RXDV:*** Data valid is asserted by an external PHY when the received data is present on the **RXD[3:0]** lines and is de-asserted at the end of the packet. This signal should be synchronized with the RXC signal.
J21	TXC	I	***TXC:*** Supports the transmit clock supplied by the external PMD device. This clock should always be active.
J18, J17, K17, K18	**TXD[3:0]**	O	***TXD[3:0]:*** Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal.
K21	TXEN	O	***TXEN:*** This pin functions as Transmit Enable. It indicates that a transmission to an external PHY device is active on the MII port.

- **USB Device (2 PINs)**

PIN No.	Symbol	Type	Description
D1 E1	UD_DP UD_DM	I/O	***Universal Serial Bus Device Controller Port.*** These are the serial data pair for USB Device. Need add 1.5kΩ pull up resistors to UD_DP externally.

- **JTAG Interface (4 PINs)**

PIN No.	Symbol	Type	Description
G6	TDO	O	***TDO:*** JTAG Test Data Output pin.
J9	TMS	I	***TMS:*** JTAG Test Mode Select pin.
G7	TCK	I	***TCK:*** JTAG Test Clock Input pin.
H6	TDI	I	***TDI:*** JTAG Test Data Input pin.

- **SPI Embedded Flash Control PIN (2 PINs)**

PIN No.	Symbol	Type	Description
E21	SPIFL_WP#	I/O	Write- protect pin of embedded flash, must pull high to 3.3V by a 10K ohm resistor.
E23	SPIFL_Hold#	I/O	hold pin of embedded flash, must pull high to 3.3V by a 10K ohm resistor.

- **TEST PIN (7 PINs)**

PIN No.	Symbol	Type	Description
F2,E2,F3,E3, D22,E22,D23	TEST[8:5]; TEST[2:0]	I/O	For Testing used.

- **1V POWER (10 PINs)**

PIN No.	Symbol	Type	Description
F8,F13,F14,G4,J14, K14,L14,N9,M14,P9	VDD10 (10 PINs)	I	Core power

- **1.8V POWER (34 PINs)**

PIN No.	Symbol	Type	Description
C4,C5,C6,C7, D4,D7,D8,E4	VDD18 (8 PINs)	I	DDRII Power
AA21,AA22, AA23,AC4, AC5,AC6,T11, T12,U10,V10	VDD18 (10 PINs)	I	SB Core power
R23 W26 N22 R24	AVDD3_USB18 AVDD2_USB18 AVDD1_USB18 AVDD_USB18	I	Analog Power USB 1.8 V Power
T24 W25 N24 P23	AVSS3_USB18 AVSS2_USB18 AVSS1_USB18 AVSS_USB18	I	Analog ground USB 1.8 V ground
U25 P25	AVSS1_USBPLL18 AVSS_USBPLL18	I	USB PLL Ground
V24 N23	AVDD1_USBPLL18 AVDD_USBPLL18	I	USB PLL Power
H4 J4	AVDD1_PLL18 AVDD_PLL18	I	Analog Power CPU PLL Power
J5 H5	AVSS1_PLL18 AVSS_PLL18	I	Analog ground CPU PLL Ground

- **Battery POWER (2 PINs)**

PIN No.	Symbol	Type	Description
P21	**VDD_BAT**	I	Battery power for RTC
R21	**VSS_BAT**	I	Battery ground for RTC

- **3.3V Power (81 PINs)**

PIN No.	Symbol	Type	Description
AB24	**AVDD_PLL33**	I	Analog power

PIN No.	Symbol	Type	Description
			SB PLL Power
AC24	**AVSS_PLL33**	I	Analog ground SB PLL Ground
E18, F18, J15, K15, L15, M15, M16, P10, P11, P12, P13, P14	VDD33 (12 PINs)	I	Analog power CPU I / O PAD Power
AA4, AA5, AA6, AC21, AC22, AC23, N17, N18, P15, P16, R9, R10, R13, R14, V3, W3, W4, F23	VDD33 (18 PINs)	I	I/O power SB I/O PAD Power
K23	AVSS_EPHYPLL33	I	Analog Ground, E-PHY PLL
J23	AVDD_EPHYPLL33	I	Analog power, E-PHY PLL
M22	AVSS_EPHYBG33	I	Analog ground, E-PHY BandGap
M23	AVDD_EPHYBG33	I	Analog power, E-PHY BandGap
K24	AVDD_EPHYRX33	I	Analog power, E-PHY for RX
L23	AVSS_EPHYRX33	I	Analog ground, E-PHY for RX
L24	AVDD1_EPHYTX33	I	Analog power, E-PHY for TX
M24	AVSS1_EPHYTX33	I	Analog ground, E-PHY for TX
U24	AVDD1_USB33	I	USB Analog power
P24	AVDD_USB33	I	USB Analog power

- **Digital Ground (83 PIN)**

PIN No.	Symbol	Type	Description
D21, P17, P18, R11, R12, R15, R16, R17, R18, T9, T10, T13, T14, T15, U9, U17, V9, V17, W5, W6, AB21, AB22, AB23, AC20, F15, F16, F17, J13, K13, L13, M12, M13, N10, N11, N12, N13, N14, N15, N16, T16, T17, T18, U11, U12, U13, U14, U15, U16, V4, V11, V12, AB4, AB5, AB6,	VSS	I	Digital Ground

PIN No.	Symbol	Type	Description
AC10, AC11, AC12, D5, D6, E5, E6, F4, F5, F6, F7, G5, E7, E8, E17, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11			

4.5. PIN Capacitance Description

North-Bridge:

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance	1.94304	2.05082	2.08563	pF
C_{BID}	3.3V Bi-directional Capacitance	2.18057(max loading= 40)	2.21818(max loading=4 0)	2.2269(max loading= 40)	pF

South-Bridge:

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance	3.144	3.143	3.216	pF
C_{BID}	3.3V Bi-directional Capacitance	3.179	3.116	3.099	pF