# DATA BUFFER

## DESCRIPTION

The VL82C332 Data Buffer is part of a custom, three chip set which allows extremely high performance and integration in 386DX processor based, PC/AT®-compatible, personal computer designs. When used with VLSI Technology's VL82C330 System Controller and VL82C331 ISA Bus Controller, the set is called the VL82C386 chip set.

The VL82C332 performs all of the data buffering functions required for a 386DX-based PC/AT-type system. Under the control of the CPU, the Data Buffer chip routes data to and from the CPU bus, the MD bus, the XD bus, and the slots (SD bus). For an on-board DRAM read, the data is latched in the MD latch allowing the VL82C330 System Controller to be programmed for early CAS terminations. The parity is checked for MD bus read operations and any errors are reported during the next on-board memory read cycle. When reading from ROM, the XD bus or the SD bus, the data can be converted from 8-bits wide to 16-, 24- or 32-bits wide or from 16 bits to 32 bits at the 16/32 latch. The data is latched with –LATLO and –LATHI for synchronization with the CPU. The data conversion is accomplished without the use of the bus size 16 (–BS16) input to the 386DX allowing it to remain in pipelined mode.

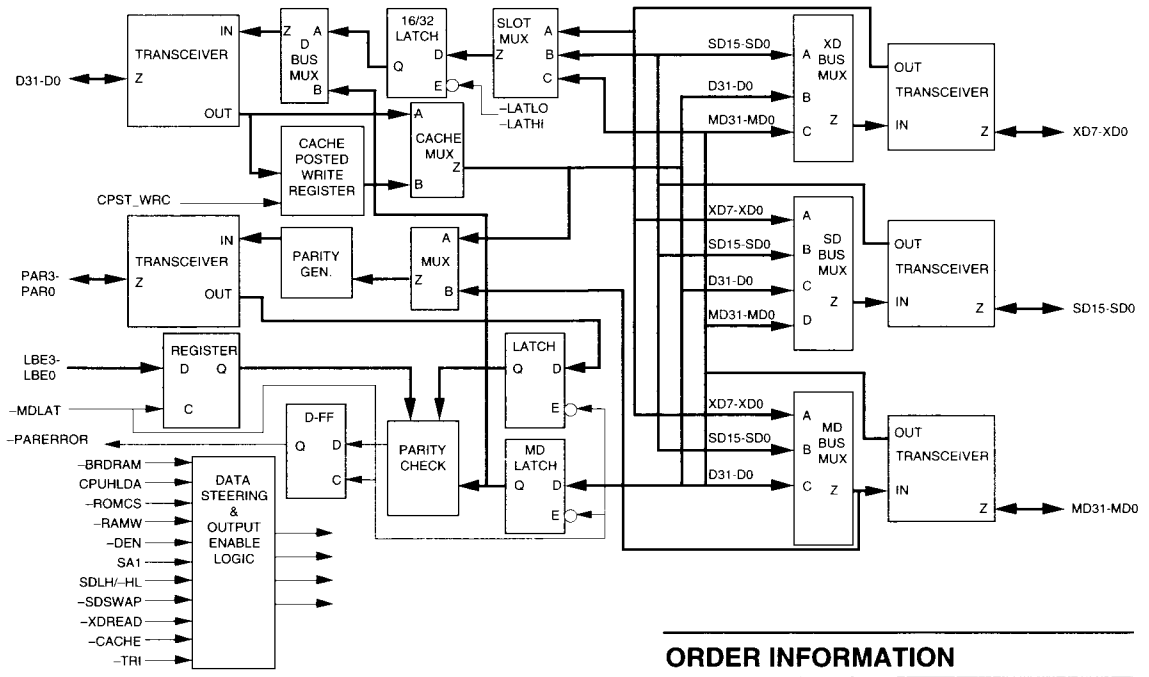
CPU writes to any of the three buses are accomplished in several different ways. The VL82C332 supports posted writes from a Cache Controller or non-posted writes to the MD bus. Parity is generated for all data written to the MD bus. The VL82C332 provides the data conversion necessary for 32- or 16-bit writes to 16- or 8-bit devices on the XD or SD buses.

In non-cached systems, system board DRAM can be placed on the CPU's D bus. This provides extra timing margin when the MD bus delay through the VL82C332 is removed from the critical path.

Under the control of DMA or a Bus Master, the VL82C332 will allow 8- or 16-bit data to be routed to and from the XD and the MD buses. The chip also is capable of performing high-to-low and low-to-high byte swaps on the SD bus. For transfers between two peripherals on the slot bus, the outputs of the VL82C332 will be disabled. The chip also provides the feature of a single input, –TRI, to disable all of its outputs for board level testability.

4

## BLOCK DIAGRAM



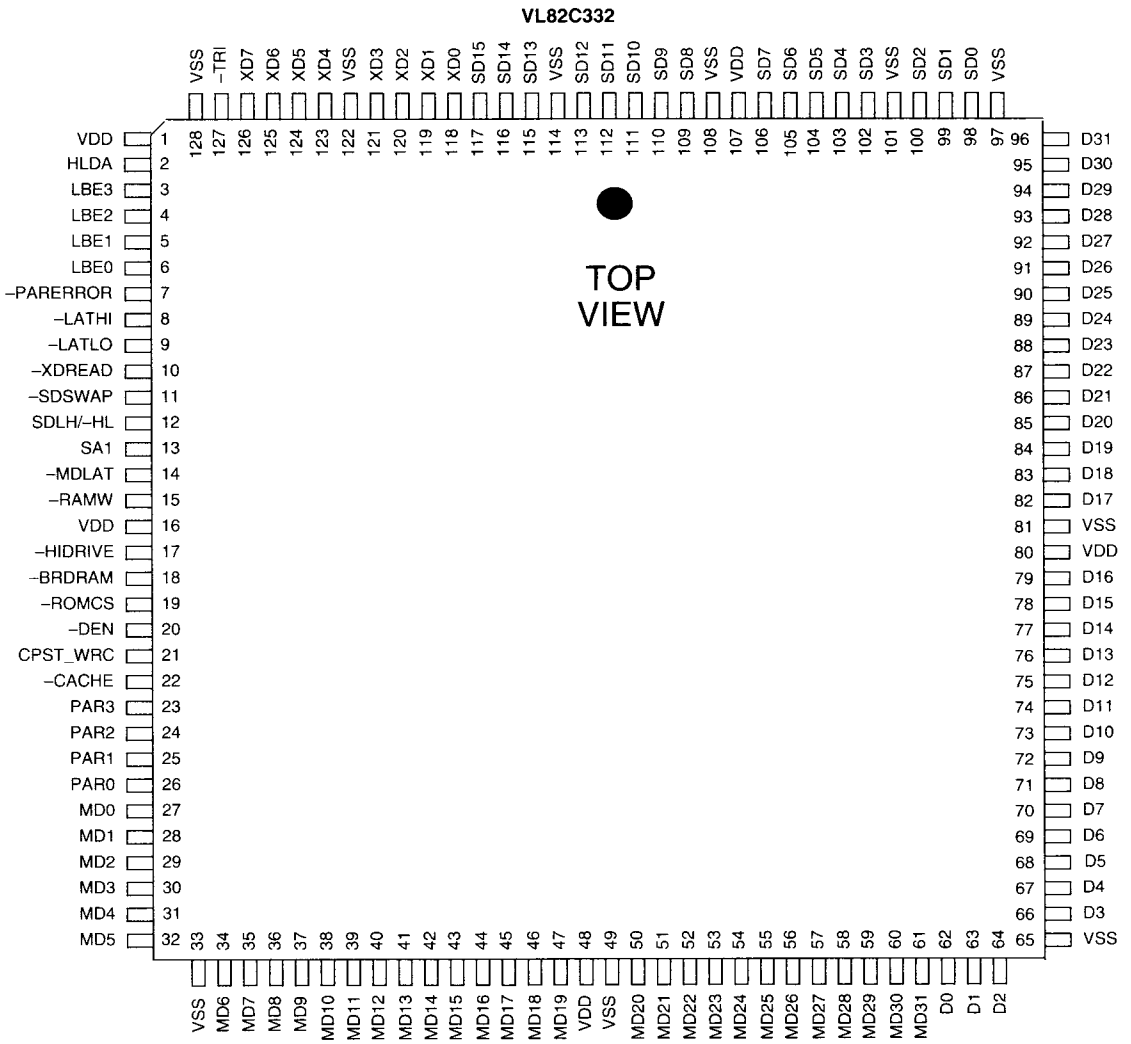

## ORDER INFORMATION

| Part Number | Package |
|---|---|
| VL82C332-FC | Plastic Flat Pack |

**Note:** Operating temperature range is 0°C to +70°C.

PC/AT is a register trademark of IBM Corp.

## PIN DIAGRAM


VL82C332
TOP VIEW
1 VDD
2 HLDA
3 LBE3
4 LBE2
5 LBE1
6 LBE0
7 –PARERROR
8 –LATHI
9 –LATLO
10 –XDREAD
11 –SDSWAP
12 SDLH/–HL
13 SA1
14 –MDLAT
15 –RAMW
16 VDD
17 –HIDRIVE
18 –BRDRAM
19 –ROMCS
20 –DEN
21 CPST_WRC
22 –CACHE
23 PAR3
24 PAR2
25 PAR1
26 PAR0
27 MD0
28 MD1
29 MD2
30 MD3
31 MD4
32 MD5
33 VSS
34 MD6
35 MD7
36 MD8
37 MD9
38 MD10
39 MD11
40 MD12
41 MD13
42 MD14
43 MD15
44 MD16
45 MD17
46 MD18
47 MD19
48 VDD
49 VSS
50 MD20
51 MD21
52 MD22
53 MD23
54 MD24
55 MD25
56 MD26
57 MD27
58 MD28
59 MD29
60 MD30
61 MD31
62 D0
63 D1
64 D2
65 VSS
66 D3
67 D4
68 D5
69 D6
70 D7
71 D8
72 D9
73 D10
74 D11
75 D12
76 D13
77 D14
78 D15
79 D16
80 VDD
81 VSS
82 D17
83 D18
84 D19
85 D20
86 D21
87 D22
88 D23
89 D24
90 D25
91 D26
92 D27
93 D28
94 D29
95 D30
96 D31
97 VSS
98 SD0
99 SD1
100 SD2
101 VSS
102 SD3
103 SD4
104 SD5
105 SD6
106 SD7
107 VDD
108 VSS
109 SD8
110 SD9
111 SD10
112 SD11
113 SD12
114 VSS
115 SD13
116 SD14
117 SD15
118 XD0
119 XD1
120 XD2
121 XD3
122 VSS
123 XD4
124 XD5
125 XD6
126 XD7
127 –TRI
128 VSS

## SIGNAL DESCRIPTIONS

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| **CPU INTERFACE** | | | |
| HLDA | 2 | I-TTL | CPU Hold Acknowledge, active high - This is the hold acknowledge pin directly from the CPU. It indicates the CPU has given up the bus for either a DMA Master or a Slot Bus Master. It is used in the steering logic to determine data routing. |
| D31-D0 | 96-82, 79-66, 64-62 | IO-TTL | CPU Data Bus - This is the data bus directly connected to the CPU. It is also referred to as the local data bus. This bus is output enabled by the –DEN signal. |
| **CACHE INTERFACE** | | | |
| CPST_WRC | 21 | I-TTL | Posted Cache Write Clock - This clock signal is driven by the Cache Controller and is needed to latch the write data during a posted cache write cycle. The data is latched on the rising edge of this signal. The latch inside of the Data Buffer is bypassed if the –CACHE input is high. Also, when –CACHE is high, the state of CPST_WRC determines on which bus (D or MD) system DRAM is accessed. When high, DRAM is accessed on the D bus. When low, DRAM is accessed on the MD bus. |
| –CACHE | 22 | I-TPU | Cache Enable, active low - This signal is used to enable the cache posted write register. When there is not a cache in the system, data bypasses the register. When –CACHE is inactive (high) the state of the CPST_WRC pin determines whether the system DRAM is on the CPU's D bus or on the MD bus. |
| **SYSTEM CONTROLLER INTERFACE** | | | |
| –MDLAT | 14 | I-TTL | Memory Data Latch - This latching signal serves two purposes simultaneously and is only activated during on-board memory read and write cycles. As a memory data latch, this transparent low signal allows read data to flow through to the CPU's local bus. As a parity clock, it samples the byte enables, –RAMW, and parity bits to be used for parity checking. Any parity errors will be reported on the next on-board memory read cycle. |
| –RAMW | 15 | I-TTL | RAM Write, active low - This signal is supplied by the System Controller to indicate that a memory write cycle is occurring. It is used internally to direct the parity logic and to enable the MD bus outputs. |
| –ROMCS | 19 | I-TTL | ROM Chip Select - This signal tells the Data Buffer when the ROM is to be accessed so that it can latch the data and convert it from 16 or 8 bits to 32 bits. This signal is driven by the System Controller. |
| –BRDRAM | 18 | I-TTL | Board Memory Selected, active low - This signal is driven by the System Controller and indicates when on-board DRAM is being accessed. |
| –DEN | 20 | I-TTL | Data Enable, active low - This is a control signal generated by the System Controller. It is used as an output enable for the D bus. |
| LBE3-LBE0 | 3-6 | I-TTL | Latch Byte Enables 3 through 0 - These signals are driven by the System Controller. They are used internally to enable the appropriate bytes for parity checking. |
| –PARERROR | 7 | O | Parity Error, active low - This signal is the result of a parity check on the appropriate bytes being read from memory. It is generated on the falling edge of –MDLAT. |
| **BUS CONTROLLER INTERFACE** | | | |
| SA1 | 13 | I-TTL | System Address Bus bit 1 - This input will be driven by the Bus Controller or by the controlling DMA or Bus Master. This signal is used for 16- to 32-bit conversion. When low, this signal indicates the low word is to be used. |

## SIGNAL DESCRIPTIONS (Cont.)

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| SDLH/–HL | 12 | I-TTL | System Data Bus Low-to-High/High-to-Low Swap - This signal is driven by the Bus Controller. It is used to establish the direction of byte swaps. |
| –SDSWAP | 11 | I-TTL | System Data Bus Byte Swap Enable, active low - This signal is driven by the Bus Controller. It is the qualifying signal needed for SDLH/–HL. |
| –XDREAD | 10 | I-TTL | Peripheral Data Bus (XD Bus) Read, active low - This signal is driven by the Bus Controller and it determines the direction of the XD bus data flow. When this signal is high, the XD Bus is output enabled. |
| –LATHI | 8 | I-TTL | High Byte Latch - This signal is needed to latch the high byte to the local data bus until the CPU is ready to sample the bus. When SA1 is low, the high byte is latched into both the 1 byte and the 3 byte of the 16/32 latch. When SA1 is high, the high byte is only latched into the 3 byte. This signal is driven by the Bus Controller. |
| –LATLO | 9 | I-TTL | Low Byte Latch - This signal is needed to latch the low byte to the local data bus until the CPU is ready to sample the bus. When SA1 is low, the low byte is latched into both the 0 byte and the 2 byte of the 16/32 latch. When SA1 is high, the high byte is only latched into the 2 byte. This signal is driven by the Bus Controller. |
| **BUFFER INTERFACE** | | | |
| MD31-MD0 | 61-50, 47-34, 32-27 | IO-TTL | Memory Data Bus - This bus connects to the on-board DRAM and BIOS ROM. It is used to transfer data to/from memory during memory write/read bus cycles. |
| SD15-SD0 | 117-115, 103-109, 106-102, 100-98 | IO-TTL | System Data Bus - This bus connects directly to the slots. It is used to transfer data to/from local and system devices. |
| XD7-XD0 | 126-123, 121-118 | IO-TTL | Peripheral Data Bus - This bus is connected to the Bus Controller and the System Controller. These I/O's are used to read and write to on-board 8-bit peripherals. |
| PAR3-PAR0 | 23-26 | IO-TTL | Parity Bits 3 through 0 - These bits are generated by the parity generation circuitry located on the Data Buffer chip. They are written to memory along with their corresponding bytes during memory write operations. During memory read operations, these bits become inputs and are used along with their respective data bytes to determine if a parity error has occurred. The check of each byte is enabled only when their respective LBE3-LBE0 bits are active. |
| –HIDRIVE | 17 | I-TPU | High Drive Enable - This pin is a wire option. When this pin is low, the SD bus will sink 24 mA of current. When this pin is high, the SD bus will sink 12 mA. |
| **TEST MODE PIN** | | | |
| –TRI | 127 | I-TPU | Three-state - This pin is used to drive all outputs to a high impedance state. When –TRI is low, all outputs and bidirectional pins are three-stated. |
| **POWER BUS CONNECTION** | | | |
| VDD | 1, 16. 48, 80, 107 | PWR | Power connection, nominally +5 volts. These pins should each have 0.1 µF bypass capacitors. |
| VSS | 33, 49, 65, 81, 97, 101, 108, 114, 122, 126 | GND | Ground connection, 0 volts. |

**SIGNAL TYPE LEGEND**

| Signal Code | Signal Type |
|---|---|
| I-TTL | TTL level input |
| I-TPU | Input with 30k ohm pull-up resistor |
| IO-TTL | TTL level input/ouput |
| O | CMOS and TTL level compatible output |
| GND | Ground |
| PWR | Power |

## FUNCTIONAL DESCRIPTION

### BUS OPERATIONS

The VL82C332 Data Buffer separates the data bus into four distinct buses:

- D bus,
- MD bus,
- SD bus, and
- XD bus.

The D bus is the CPU's data bus. The MD bus is the memory data bus which connects to the on-board DRAM and the BIOS ROM. The SD bus is the 16-bit slot bus and the XD bus is an 8-bit bus for on-board peripherals such as the VL82C330 System Controller and the VL82C331 Bus Controller. These buses can be controlled by either the CPU, a DMA Controller or a Bus Master. Tables 1 and 2 show all possible bus steering modes provided by the VL82C332.

### CACHE CONTROLLER INTERFACE

The cache controller interface is made up of a 32-bit register and a 64-to-32 MUX as shown in the block diagram. When a Cache Controller is not implemented, the –CACHE input pin should be tied high. This will set the MUX such that the cache posted write register is bypassed. When a cache is implemented, –CACHE should be tied low and the CPST_WRC input is used to post the write data into the register. The register latches data on the rising edge of the CPST_WRC input.

### MD, D Bus System DRAM Selection

When the –CACHE input pin is tied low, system DRAM must be on the MD bus. However, when –CACHE is tied high, system DRAM may be placed on the MD bus or the CPU's D bus. The selection is made by the state of CPST_WRC. When tied low, DRAM is on the MD bus. When CPST_WRC is tied high, system DRAM is on the D bus. Since system board bus selection is hardwired on the system board, these pins can not be dynamically controlled in non-cache systems. They must be permanently tied to the proper level.

### PARITY GENERATION AND DETECTION CIRCUIT

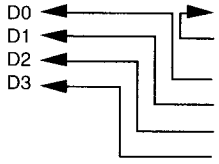
The parity check portion of the chip checks the parity of all data read from the on-board DRAM. During a DRAM read cycle, –MDLAT goes low making the MD latch transparent and latching out the parity check result, for the previous on-board memory read cycle. When –MDLAT returns high, data is latched into the MD latch. The parity check uses the Latched Byte Enable (LBE) signals from the System Controller to qualify each byte of the 32-bit word.

The parity generator provides parity generation for both CPU and DMA/Master writes to on-board DRAM. A 64 to 32 MUX is used to select whether the input to the parity generator is from the CPU or from a DMA/Master transfer. The result is output as one bit per data byte on the PAR3-PAR0 pins.

## TABLE 1. BUS STATES WHEN PIN 21 = GROUND

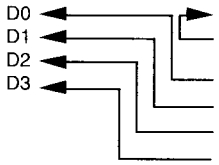
Bus states for DRAM on the MD bus, ROM on the MD bus. Cache posted writes are supported.

A



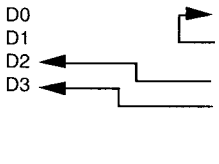

CPU read of DRAM

B



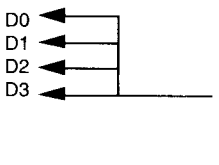

CPU read of:
- 32-bit ROM
- 16-bit ROM, byte 0, byte 1, or low word
- 8-bit ROM, byte 0

C



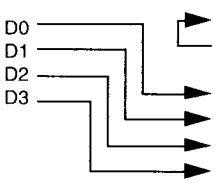

CPU read of:
- 16-bit ROM, byte 2, byte 3, or high word
- 8-bit ROM, byte 2

D



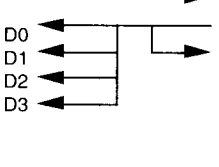

CPU read of:
- 8-bit ROM read, byte 1 or 3
- SA1=0, XD=MD1
- SA1=1, XD=MD3

E



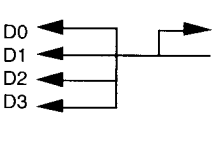

CPU write to DRAM
Cache posted write to DRAM

F



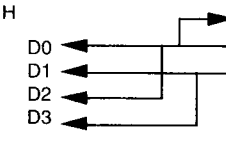

CPU read of XD bus

G



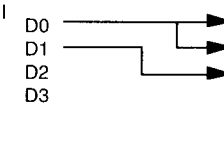

CPU read of 8-bit peripheral on SD bus, byte 1 or 3

H



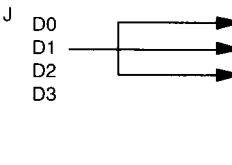

CPU read of:
- 16-bit peripheral on SD bus, low or high word
- 8-bit peripheral, byte 0 or 2

I



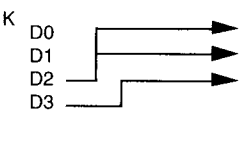

CPU write to:
- XD bus, byte 0
- SD bus, 8-bit peripheral, byte 0
- SD bus, 16-bit peripheral, byte 0 or 1 or low word

J



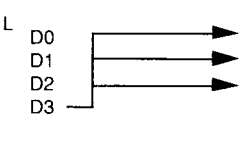

CPU write to:
- XD bus, byte 1
- SD bus, 8-bit peripheral, byte 1

K



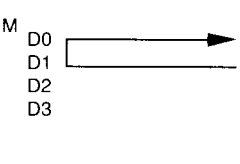

CPU write to:
- XD bus, byte 2
- SD bus, 8-bit peripheral, byte 2
- SD bus, 16-bit peripheral, byte 2 or 3 or high word

L




CPU write to:
- XD bus, byte 3
- SD bus, 8-bit peripheral, byte 3

M




16-bit DMA
- 16-bit slot memory, read I/O write, word I/O read/ 16-bit slot memory, write, word

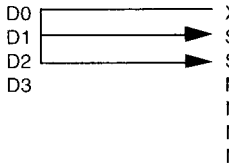
8-bit DMA
- 8- or 16-bit slot memory / I/O write to SDL or XD, byte 0 I/O read / 8- or 16-bit slot memory, write, byte 0

CPU read/write to coprocessor

## TABLE 1. BUS STATES WHEN PIN 21 = GROUND (Cont.)

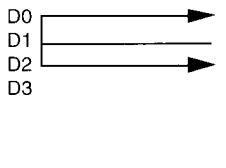
Bus states for DRAM on the MD bus, ROM on the MD bus. Cache posted writes are supported.

N



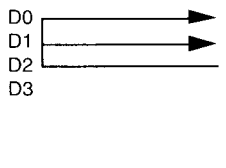

8-bit DMA
I/O read / 8- or 16-bit slot memory write, byte 0
I/O read / 16-bit slot memory write, byte 1

O



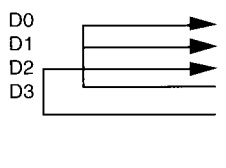

8-bit DMA
I/O read / 16-bit slot memory write, byte 1

P



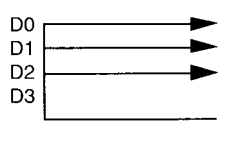

8-bit DMA
16-bit slot memory read / I/O write to SDL or XD, byte 1

Q



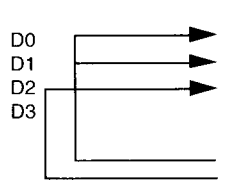

16-bit DMA
On-board memory read / I/O write, low word
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 0

R



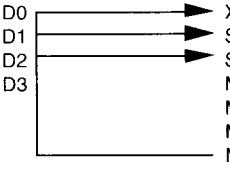

8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 1

S



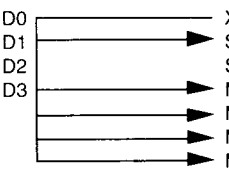

16-bit DMA
On-board memory read / I/O write, high word
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 2

T



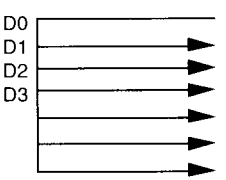

8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 3

U



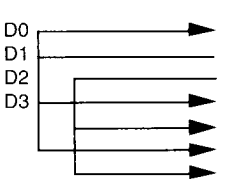

8-bit DMA
XD bus I/O read / on-board memory write, byte 0 or 2

V



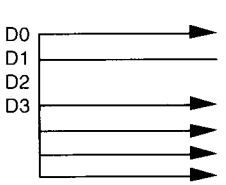

8-bit DMA
XD bus I/O read / on-board memory write, byte 1 or 3

W




16-bit DMA
SD bus I/O read / on-board memory write, low or high word
8-bit DMA
SD bus I/O read / on-board memory write, byte 0 or 2

X



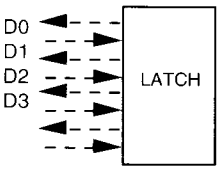

8-bit DMA
SD bus I/O read / on-board memory write, byte 1 or 3

4

## TABLE 2. BUS STATES WHEN PIN 21 = VDD

Bus states for DRAM on the D bus, ROM on the MD bus. Cache posted writes are not supported.

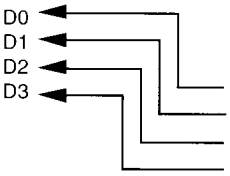
A




XD SDL SDH MD0 MD1 MD2 MD3

CPU read of DRAM.
D bus output enabled only after CAS goes inactive.

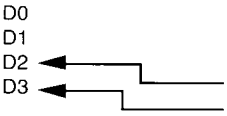
B




XD SDL SDH MD0 MD1 MD2 MD3

CPU read of:
32-bit ROM
16-bit ROM, byte 0, byte 1, or low word
8-bit ROM, byte 0

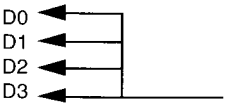
C




XD SDL SDH MD0 MD1 MD2 MD3

CPU read of:
16-bit ROM, byte 2, byte 3, or high word
8-bit ROM, byte 2

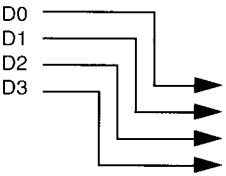
D




XD SDL SDH MD0 MD1 MD2 MD3

CPU read of:
8-bit ROM read, byte 1 or 3

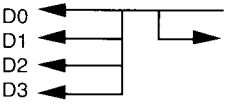
E




XD SDL SDH MD0 MD1 MD2 MD3

CPU write to DRAM
Cache posted write to DRAM

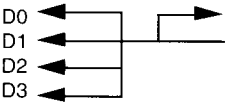
F U




XD SDL SDH MD0 MD1 MD2 MD3

CPU read of XD bus
8-bit DMA
XD bus I/O read / on-board memory write, byte 0 or 2

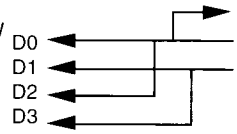
G X




XD SDL SDH MD0 MD1 MD2 MD3

CPU read of :
8-bit peripheral on SD bus, byte 1 or 3
8-bit DMA
SD bus I/O read / on-board memory write, byte1 or 3

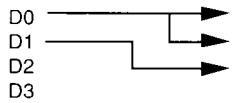
H W




XD SDL SDH MD0 MD1 MD2 MD3

CPU read of:
16-bit peripheral on SD bus, low or high word
8-bit peripheral, byte 0 or 2
16-bit DMA, SD bus I/O read / on-board memory write, low or high word
8-bit DMA, SD bus I/O read / on-board memory write, byte 0 or 2

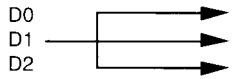
I Q




XD SDL SDH MD0 MD1 MD2 MD3

CPU write to:
XD bus, byte 0
SD bus, 8-bit peripheral, byte 0
SD bus, 16-bit peripheral, byte 0 or 1 or low word
16-bit DMA
On-board memory read / I/O write, low word
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 0

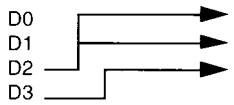
J R




XD SDL SDH MD0 MD1 MD2 MD3

CPU write to:
XD bus, byte 1
SD bus, 8-bit peripheral, byte 1
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 1

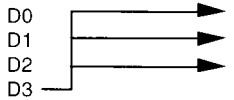
K S




XD SDL SDH MD0 MD1 MD2 MD3

CPU write to:
XD bus, byte 2
SD bus, 8-bit peripheral, byte 2
SD bus, 16-bit peripheral, byte 2 or 3 or high word
16-bit DMA
On-board memory read / I/O write, high word
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 2

L T




XD SDL SDH MD0 MD1 MD2 MD3

CPU write to:
XD bus, byte 3
SD bus, 8-bit peripheral, byte 3
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 3

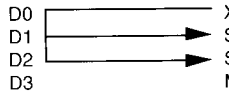
## TABLE 2. BUS STATES WHEN PIN 21 = VDD (Cont.)

Bus states for DRAM on the D bus, ROM on the MD bus. Cache posted writes are not supported.

M

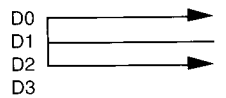

16-bit DMA
16-bit slot memory, read
I/O write, word I/O read/
16-bit slot memory, write, word
8-bit DMA
8- or 16-bit slot memory / I/O write to SDL or XD, byte 0 I/O read / 8- or 16-bit slot memory, write, byte 0
CPU read/write to coprocessor

N



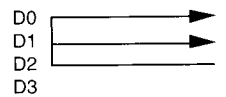

8-bit DMA
I/O read / 8- or 16-bit slot memory write, byte 0
I/O read / 16-bit slot memory write, byte 1

O



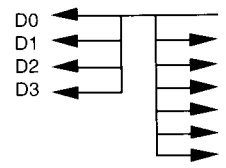

8-bit DMA
I/O read / 16-bit slot memory write, byte 1

P



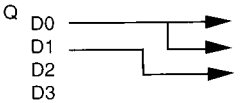

8-bit DMA
16-bit slot memory read / I/O write to SDL or XD, byte 1

V



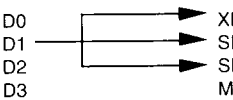

8-bit DMA
XD bus I/O read / on-board memory write, byte 1 or 3

Q



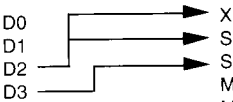

16-bit DMA
On-board memory read / I/O write, low word
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 0

R



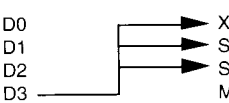

8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 1

S



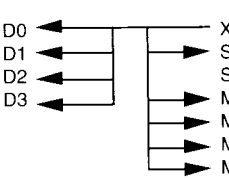

16-bit DMA
On-board memory read / I/O write, high word
8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 2

T



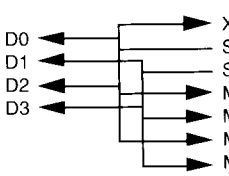

8-bit DMA
On-board memory read / I/O write to SDL or XD, byte 3

U



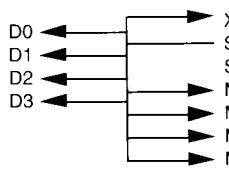

8-bit DMA
XD bus I/O read / on-board memory write, byte 0 or 2

W




16-bit DMA
SD bus I/O read / on-board memory write, low or high word
8-bit DMA
SD bus I/O read / on-board memory write, byte 0 or 2

X




8-bit DMA
SD bus I/O read / on-board memory write, byte 1 or 3

4

## IN-CIRCUIT TESTING

ICT mode is not enabled in the current VL82C332 production parts. Since the VL82C332 is basically a matrix of multiplexers and I/O drivers, it is still possible to perform In-Circuit Test by application of an appropriate set of test vectors. This method is described below.

Future versions of the VL82C332 may have a true ICT mode. If so, the method described below may still be used as an option.

The values on the bidirectional buses are indicated as outputs by **boldface** type. They are inputs, otherwise. This distinction is used to tell whether to drive the indicated value on the bus or read it from the bus. A value of "u" indicates an output that is still "unknown".

## BLOCK 1 -

Uses states A, C and D, and tests the following:

MD BUS (HI, LO), –ROMCS (HI, LO) | D BUS (HI, LO), –BRDRAM (HI, LO) | LBE BUS (HI, LO) SDLH/–HL (HI, LO) | –PARERROR (HI, LO), –RAMW (HI) | –MDLAT (HI, LO), –DEN (LO)

| V E C T O R # | MD : : : : : : : : | D : : : : : : : : | SD H | SD L | XD : | PA R | LB E | ---C THCP RIAS IDCT :RH_ :IEW :V:R :E:C : | ---- PMLL ADAA RLTT EALH RTOI R::: O::: R::: | H--- LDRB DEAR ANMD ::WR :::A ::HP ::L: :::: | -SS- RADS O1LD M:HS C:/W S:-A ::HP ::L: :::: | - X D R E A D : : |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **STATE A: VERIFY THE PARITY ERROR AND LBE SIGNALS WORK.** | | | | | | | | | | | | |
| 1 | 13579BDF | **uuuuuuuu** | 00 | 00 | **00** | 0 | 8 | 1010 | u111 | 0010 | 1011 | 1 |
| 2 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 8 | 8 | 1010 | u011 | 0010 | 1011 | 1 |
| **STATE A: LATCH IN PARITY ERROR ON BYTE 3.** | | | | | | | | | | | | |
| 3 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 8 | 4 | 1010 | u111 | 0010 | 1011 | 1 |
| 4 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 4 | 4 | 1010 | 0011 | 0010 | 1011 | 1 |
| **STATE A: LATCH IN PARITY ERROR ON BYTE 2.** | | | | | | | | | | | | |
| 5 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 4 | 2 | 1010 | 0111 | 0010 | 1011 | 1 |
| 6 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 2 | 2 | 1010 | 0011 | 0010 | 1011 | 1 |
| **STATE A: LATCH IN PARITY ERROR ON BYTE 1.** | | | | | | | | | | | | |
| 7 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 2 | 1 | 1010 | 0111 | 0010 | 1011 | 1 |
| 8 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 1 | 1 | 1010 | 0011 | 0010 | 1011 | 1 |
| **STATE A: LATCH IN PARITY ERROR ON BYTE 0.** | | | | | | | | | | | | |
| 9 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 1 | 0 | 1010 | 0111 | 0010 | 1011 | 1 |
| 10 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 0 | 0 | 1010 | 0011 | 0010 | 1011 | 1 |
| **STATE A: LATCH IN GOOD PARITY ON ALL BYTES.** | | | | | | | | | | | | |
| 11 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 0 | F | 1010 | 0111 | 0010 | 1011 | 1 |
| 12 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 0 | F | 1010 | 1011 | 0010 | 1011 | 1 |
| 13 | 13579BDF | **13579BDF** | 00 | 00 | **00** | 0 | F | 1010 | 1111 | 0010 | 1011 | 1 |
| **STATE A: CHANGE MD BUS AND SEE THAT D BUS DOES NOT CHANGE.** | | | | | | | | | | | | |
| 14 | FDB97531 | **13579BDF** | 00 | 00 | **00** | 0 | F | 1010 | 1111 | 0010 | 1011 | 1 |
| **STATE D: –ROMCS AND SDLH/–HL BYTE OF MD BUS GO TO ALL BYTES OF D BUS.** | | | | | | | | | | | | |
| 15 | FDB97531 | **31313131** | 00 | 00 | **75** | 0 | F | 1010 | 1100 | 0011 | 0000 | 1 |
| **STATE C: RAISE SDLH/–HL, BYTES 1, 0 OF MD BUS GO TO BYTES 3, 2 OF D BUS.** | | | | | | | | | | | | |
| 16 | FDB97531 | **75313131** | 00 | 00 | **00** | 0 | F | 1010 | 1100 | 0011 | 0010 | 1 |
| 17 | FDB97531 | **75313131** | 00 | 00 | **00** | 0 | F | 1010 | 1111 | 0011 | 0010 | 1 |

## BLOCK 2 -

Uses states F, G and H, and tests the following:

SDH BUS (HI, LO) SDL BUS (HI, LO) XD BUS (HI, LO) –LATLO (HI, LO) –LATHI (HI, LO)
SA1 (HI, LO) –SDSWAP (HI, LO) –XDREAD(HI, LO) HLDA (LO)

| V E C T O R # | M D : : : : : : : : | D : : : : : : : : | S D H : : : : : : | S D L : : : : : : | X D : : : : : : : | P A R : : : : : : | L B E : : : : : : | ---C THCP RIAS IDCT :RH_ :IEW :V:R :E:C :::: | ---- PMLL ADAA RLTT EALH RTOI R::: O::: R::: | H--- LDRB DEAR ANMD ::WR ::::A ::::M :::: :::: | -SS- RADS O1LD M:HS C:/W S:-A ::HP ::L: :::: | - X D R E A D 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 18 | FFFFFFFF | **AA55AA55** | AA | 55 | **55** | 0 | F | 1010 | 1100 | 0011 | 1011 | 1 |
| 19 | FFFFFFFF | **55AA55AA** | 55 | AA | **AA** | 0 | F | 1010 | 1100 | 0011 | 1011 | 1 |

**STATE H: FORCE –LATLO, –LATHI AND SA1 HIGH.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 20 | FFFFFFFF | **55AA55AA** | 55 | AA | **AA** | 0 | F | 1010 | 1111 | 0011 | 1111 | 1 |

**STATE H: CHANGE SD BUSES. D BUS SHOULD NOT CHANGE.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 21 | FFFFFFFF | **55AA55AA** | 33 | CC | **CC** | 0 | F | 1010 | 1111 | 0011 | 1111 | 1 |

**STATE H: FORCE LATLO AND LATHI LOW. TWO HIGH BYTES OF D BUS SHOULD CHANGE.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 22 | FFFFFFFF | **33CC55AA** | 33 | CC | **CC** | 0 | F | 1010 | 1100 | 0011 | 1111 | 1 |

**STATE H: FORCE SA1 LOW. TWO LOW BYTES OF D BUS SHOULD CHANGE.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 23 | FFFFFFFF | **33CC33CC** | 33 | CC | **CC** | 0 | F | 1010 | 1100 | 0011 | 1011 | 1 |

**STATE G: FORCE –SDSWAP LOW. D BUS SHOULD CARRY SDL ON ALL BYTES.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 24 | FFFFFFFF | **CCCCCCCC** | 33 | CC | **CC** | 0 | F | 1010 | 1100 | 0011 | 1010 | 1 |

**STATE F: FORCE –XDREAD LOW. D BUS SHOULD CARRY XD ON ALL BYTES.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 25 | FFFFFFFF | **55555555** | CC | 55 | **55** | F | F | 1010 | 1100 | 0011 | 1011 | 0 |

4

## BLOCK 3 -

Uses state E and tests the following:

PAR BUS (HI, LO) –CACHE (HI, LO) CPST_WRC (HI, LO) –RAMW (LO) –DEN (HI)

| | V | M | D | S | S | X | P | L | ---C | ---- | H--- | -SS- | - |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | E | D | : | D | D | D | A | B | THCP | PMLL | LDRB | RADS | X |
| | C | : | : | H | L | : | R | E | RIAS | ADAA | DEAR | O1LD | D |
| | T | : | : | : | : | : | : | : | IDCT | RLTT | ANMD | M:HS | R |
| | O | : | : | : | : | : | : | : | :RH_ | EALH | ::WR | C:/W | E |
| | R | : | : | : | : | : | : | : | :IEW | RTOI | :::A | S:-A | A |
| | | : | : | : | : | : | : | : | :V:R | R::: | :::M | ::HP | D |
| | # | : | : | : | : | : | : | : | :E:C | O::: | :::: | ::L: | : |
| | | ┌ : ─┐ | ┌ : ─┐ | ┌┐ | ┌┐ | :┌┐ | :┌┐ | :┌┐ | :::: | R::: | :::: | :::: | : |

**STATE E: TESTS MD BUS AND PAR BUSES.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 26 | **55555555** | 55555555 | 00 | 00 | **00** | F | F | 1010 | 1111 | 0100 | 1011 | 1 |
| 27 | **AAAAAAAA** | AAAAAAAA | 00 | 00 | **00** | F | F | 1010 | 1111 | 0100 | 1011 | 1 |
| 28 | **ABAAAAAA** | ABAAAAAA | 00 | 00 | **00** | 7 | F | 1010 | 1111 | 0100 | 1011 | 1 |
| 29 | **ABABAAAA** | ABABAAAA | 00 | 00 | **00** | 3 | F | 1010 | 1111 | 0100 | 1011 | 1 |

**STATE E: TEST CPST_WRC AND –CACHE PINS.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 30 | **uuuuuuuu** | ABABABAA | 00 | 00 | **00** | u | F | 1000 | 1111 | 0100 | 1011 | 1 |

**STATE E: RAISE CPST_WRC TO CLOCK IN DATA ON D BUS.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | **ABABABAA** | ABABABAA | 00 | 00 | **00** | 1 | F | 1001 | 1111 | 0100 | 1011 | 1 |

**STATE E: FORCE CPST_WRC LOW, CHANGE D BUS, STATE OF D BUS SHOULD NOT APPEAR ON MD BUS.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 32 | **ABABABAA** | ABABABAB | 00 | 00 | **00** | 1 | F | 1000 | 1111 | 0100 | 1011 | 1 |

**STATE E: RAISE CPST_WRC AGAIN TO SEE NEW DATA ON MD BUS.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 33 | **ABABABAB** | ABABABAB | 00 | 00 | **00** | 0 | F | 1001 | 1111 | 0100 | 1011 | 1 |
| 34 | **AAAAAAAA** | AAAAAAAA | 00 | 00 | **00** | F | F | 1011 | 1111 | 0100 | 1011 | 1 |

## BLOCK 4 -

Uses state N and tests the following: HLDA (HI)

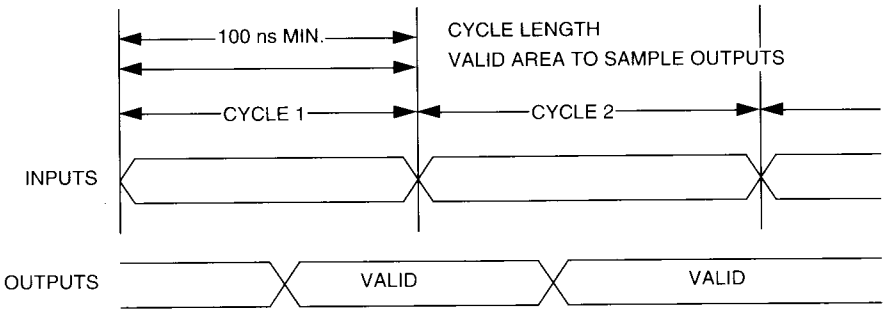
| | V | M | D | S | S | X | P | L | ---C | ---- | H--- | -SS- | - |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | E | D | : | D | D | D | A | B | THCP | PMLL | LDRB | RADS | X |
| | C | : | : | H | L | : | R | E | RIAS | ADAA | DEAR | O1LD | D |
| | T | : | : | : | : | : | : | : | IDCT | RLTT | ANMD | M:HS | R |
| | O | : | : | : | : | : | : | : | :RH_ | EALH | ::WR | C:/W | E |
| | R | : | : | : | : | : | : | : | :IEW | RTOI | :::A | S:-A | A |
| | | : | : | : | : | : | : | : | :V:R | R::: | :::M | ::HP | D |
| | # | : | : | : | : | : | : | : | :E:C | O::: | :::: | ::L: | : |
| | | ┌ : ─┐ | ┌ : ─┐ | ┌┐ | ┌┐ | :┌┐ | :┌┐ | :┌┐ | :::: | R::: | :::: | :::: | : |

**STATE N: XD TO SDL BUS AND SDH BUS.**

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 35 | FFFFFFFF | FFFFFFFF | **55** | **55** | 55 | F | F | 1011 | 1111 | 1111 | 1001 | 0 |
| 36 | FFFFFFFF | FFFFFFFF | **AA** | **AA** | AA | F | F | 1011 | 1111 | 1111 | 1010 | 0 |

## TEST PATTERN TIMING CONSTRAINTS

The patterns should be applied with a vector period of 100 ns. or more. with all inputs driven at the start of the cycle and all outputs sampled 60 ns or more after the beginning of the cycle, but at least 10 ns before the end of the cycle.




## SPECIAL CASE SIGNALS

The only pins not tested with the test vectors described below are –TRI (low) and –HIDRIVE (high, low). The best way to test these is as follows.

–TRI (low):

Force –XDREAD high and –TRI low. If the XD bus is high impedance then –TRI (low) works correctly.

–HIDRIVE (high, low):

Set a current source in the range of 10 to 15 mA on one of the SD bus pins. Use a pattern that will drive a low onto the SD bus pin in question. Put a high value on the –HIDRIVE pin and test the VOL value on that SD bus pin. Then change the–HIDRIVE pin to a low. The VOL value on the SD bus pin should drop by at least 100.0 mV.

The first group of signals shown below are the buses:

- MD,
- D,
- SDH (SD high byte),
- SDL (SD low byte),
- XD,
- PAR, and
- LBE.

All these buses are shown in hexadecimal format. The next group of signals are all the individual inputs and the –PARERROR output. These signals are shown in binary format. The last group of signals, starting after –SDSWAP, are the Output Enable signals for the bidirectional buses. The two 32-bit buses have an Output Enable for each byte, but all four Output Enable (OE) signals for a given bus will transition together. The PAR bus uses the same Output Enable signals as the MD bus. All output enables are active low indicating that the VL82C332 is driving the bus anytime the Output Enable signal is low.

The values on the bidirectional buses indicate what is to be driven in if the corresponding OE signal is high, or what to sample on the outputs when the OE signal is low. A value of "u" indicates an output that is still "unknown".

## AC CHARACTERISTICS: TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0 V

| Symbol | Parameter | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| tD1 | D31-D0 to MD31-MD0, PAR3-PAR0 Delay | 3 | 20 | ns | CL=50 pF |
| tD2 | CPST_WRC to MD31-MD0, PAR3-PAR0 Delay | 3 | 27 | ns | CL=50 pF |
| tD3 | –MDLAT Low to D31-D0 Delay | 3 | 25 | ns | CL=50 pF |
| tD4 | –MDLAT Low to –PARERROR | 3 | 25 | ns | CL=50 pF |
| tD5 | –LATLO, –LATHI Low to D31-D0 Delay | 3 | 25 | ns | CL=50 pF |
| tD6 | D31-D0 to XD7-XD0 Delay | 3 | 35 | ns | CL=50 pF |
| tD7 | D31-D0 to SD15-SD0 Delay | 3 | 30 | ns | CL=200 pF Note 1 |
| tD8 | XD7-XD0 to MD31-MD0, PAR3-PAR0 Delay | 3 | 25 | ns | CL=50 pF |
| tD9 | XD7-XD0 to D31-D0 Delay | 3 | 25 | ns | CL=50 pF |
| tD10 | XD7-XD0 to SD15-SD0 Delay | 3 | 30 | ns | CL=200 pF Note 1 |
| tD11 | SD15-SD0 to XD7-XD0 Delay | 3 | 35 | ns | CL=50 pF |
| tD12 | SD15-SD0 to MD31-MD0, PAR3-PAR0 Delay | 3 | 25 | ns | CL=50 pF |
| tD13 | SD15-SD0 to D31-D0 Delay | 3 | 25 | ns | CL=50 pF |
| tD14 | SD15-SD8 to SD7-SD0 Delay | 3 | 30 | ns | CL=200 pF Note 1 |
| tD15 | SD7-SD0 to SD15-SD8 Delay | 3 | 30 | ns | CL=200 pF Note 1 |
| tD16 | MD31-MD0 to XD7-XD0 Delay | 3 | 35 | ns | CL=50 pF |
| tD17 | MD31-MD0 to SD15-SD0 Delay | 3 | 22 | ns | CL=200 pF Note 1 |
| tD18 | MD31-MD0 to D31-D0 Delay | 3 | 20 | ns | CL=50 pF |
| tD19 | MD15-MD0 to D31-D0 Delay | 3 | 25 | ns | CL=50 pF |
| tD20 | CONTROL to SD15-SD0 Delay | 3 | 35 | ns | CL=200 pF Note 1 |
| tD21 | CONTROL to XD7-XD0 Delay | 3 | 25 | ns | CL=50 pF |
| tD22 | CONTROL to MD31-MD0 Delay | 3 | 20 | ns | CL=50 pF |
| tD23 | CONTROL to D31-D0 Delay | 3 | 20 | ns | CL=50 pF |
| tSU24 | MD31-MD0 to –MDLAT Setup Time | 3 | | ns | |
| tH25 | MD31-MD0 from –MDLAT Hold Time | 4 | | ns | |
| tSU26 | D31-D0 to –MDLAT Setup Time | 3 | | ns | |
| tH27 | D31-D0 from –MDLAT Hold Time | 4 | | ns | |
| tSU28 | LBE3-LBE0, –RAMW to –MDLAT Setup TIme | –1 | | ns | |
| tH29 | LBE3-LBE0, –RAMW from –MDLAT Hold TIme | 10 | | ns | |
| tSU30 | PAR3-PAR0 to –MDLAT Setup Time | 3 | | ns | |
| tH31 | PAR3-PAR0 from –MDLAT Hold Time | 4 | | ns | |
| tSU32 | MD15-MD0 to –LATLO, –LATHI Setup Time | 10 | | ns | |
| tH33 | MD15-MD0 from –LATLO, –LATHI Hold Time | 2 | | ns | |
| tSU34 | SD15-SD0 to –LATLO, –LATHI Setup Time | 10 | 20 | ns | |

## AC CHARACTERISTICS (Cont.): TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0 V

| Symbol | Parameter | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| tH35 | SD15-SD0 from –LATLO, –LATHI Hold Time | 2 | | ns | |
| tSU36 | XD7-XD0 to –LATLO, –LATHI Setup Time | 10 | | ns | |
| tH37 | XD7-XD0 from –LATLO, –LATHI Hold Time | 2 | | ns | |
| tSU38 | D31-D0 to CPST_WRC Setup Time | 5 | | ns | |
| tH39 | D31-D0 from CPST_WRC Hold Time | 5 | | ns | |
| t40 | –MDLAT Pulse Width | 10 | | ns | |
| t41 | –LATLO, –LATHI Pulse Width | 15 | | ns | |
| t42 | CPST_WRC Pulse Width | 15 | | ns | |

**Note 1:** These specifications are with –HIDRIVE active.

**FIGURE 1.**

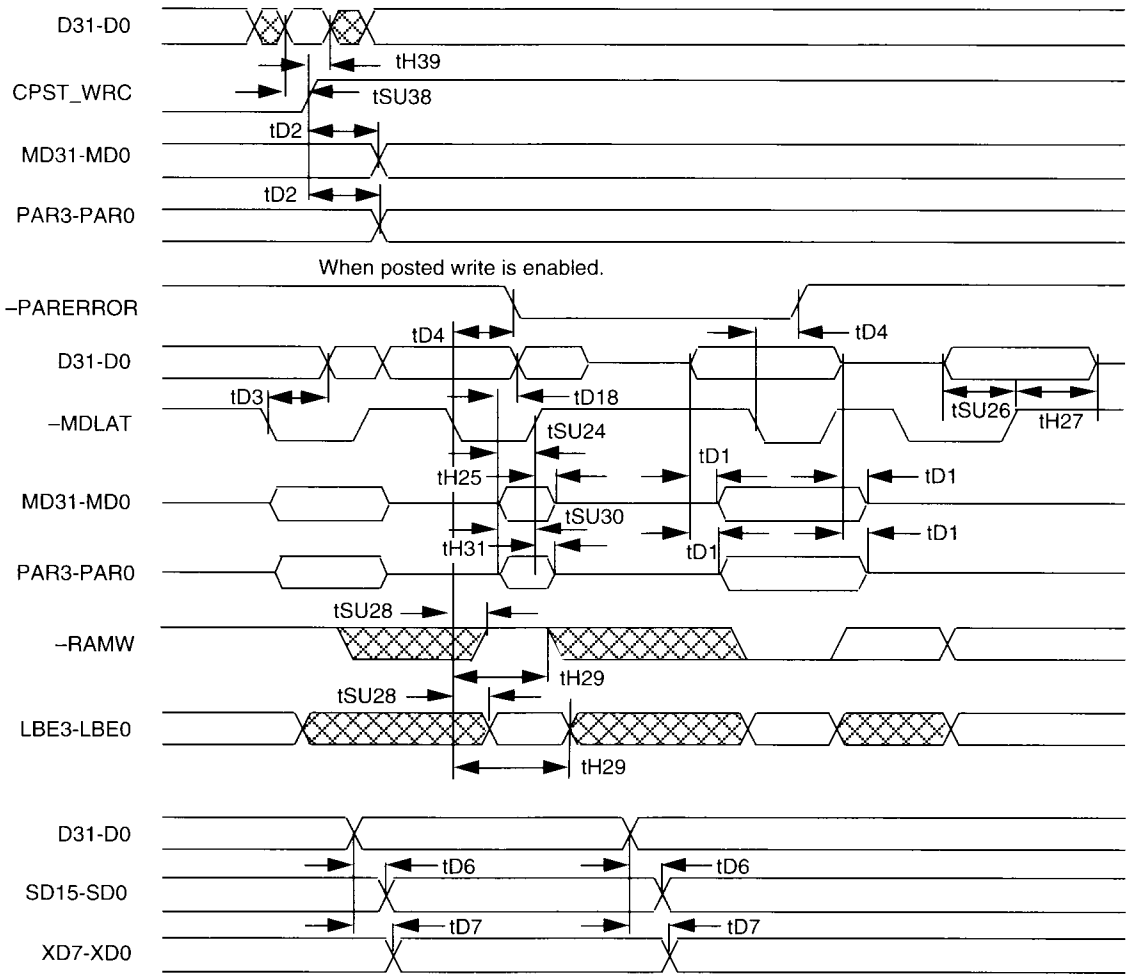

D31-D0
tH39
CPST_WRC
tSU38
tD2
MD31-MD0
tD2
PAR3-PAR0
When posted write is enabled.
–PARERROR
tD4
tD4
D31-D0
tD3
tD18
tSU26
tH27
–MDLAT
tSU24
tD1
tH25
tD1
MD31-MD0
tSU30
tD1
tH31
tD1
PAR3-PAR0
tSU28
–RAMW
tH29
tSU28
LBE3-LBE0
tH29
D31-D0
tD6
tD6
SD15-SD0
tD7
tD7
XD7-XD0

**FIGURE 2.**

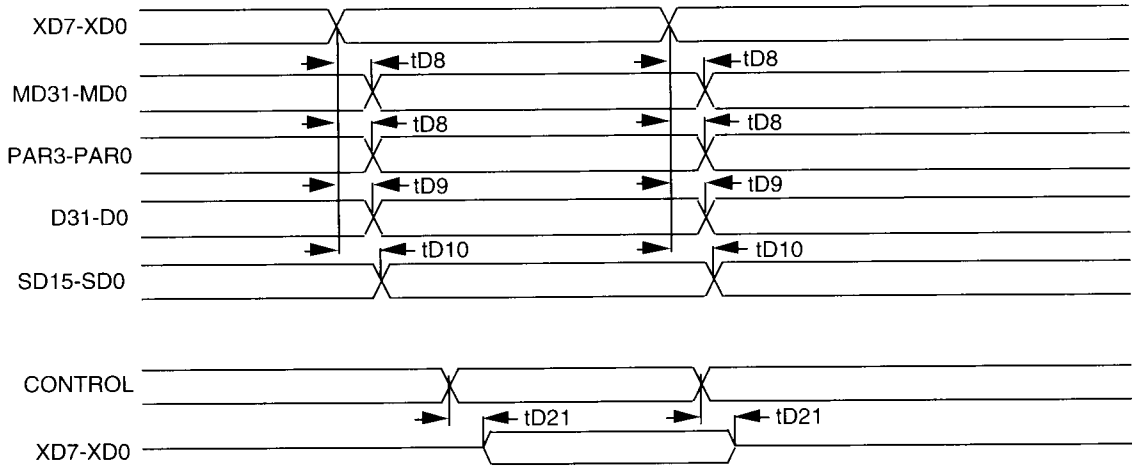



**FIGURE 3.**

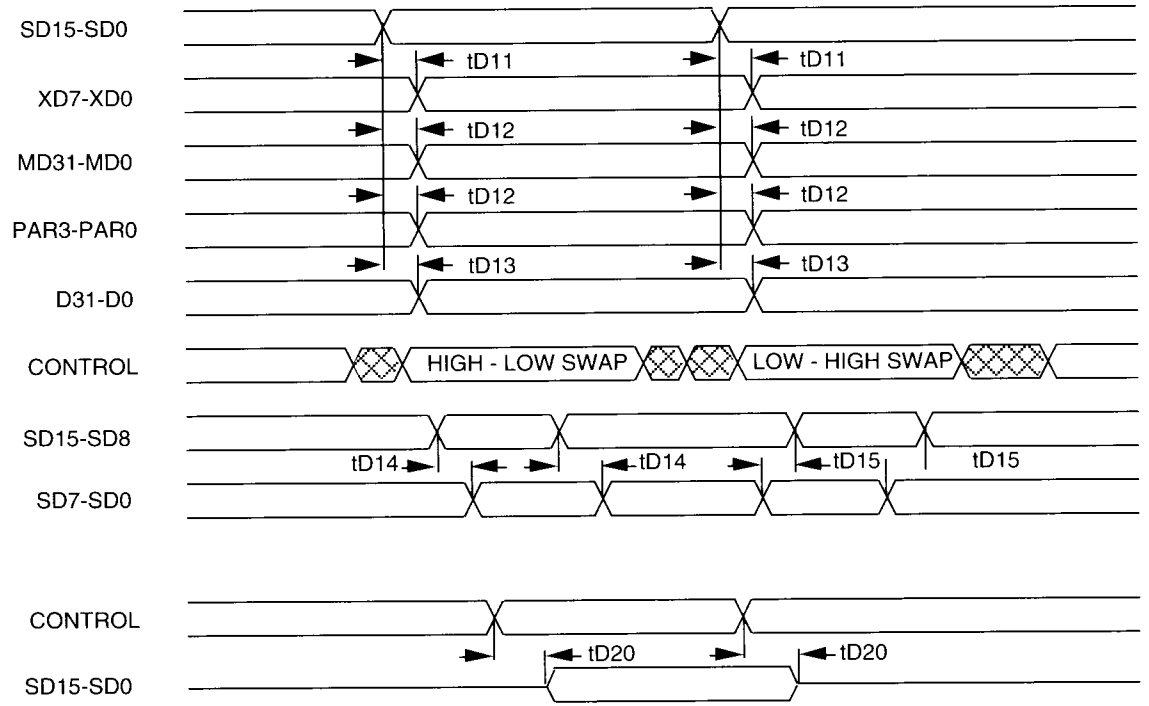



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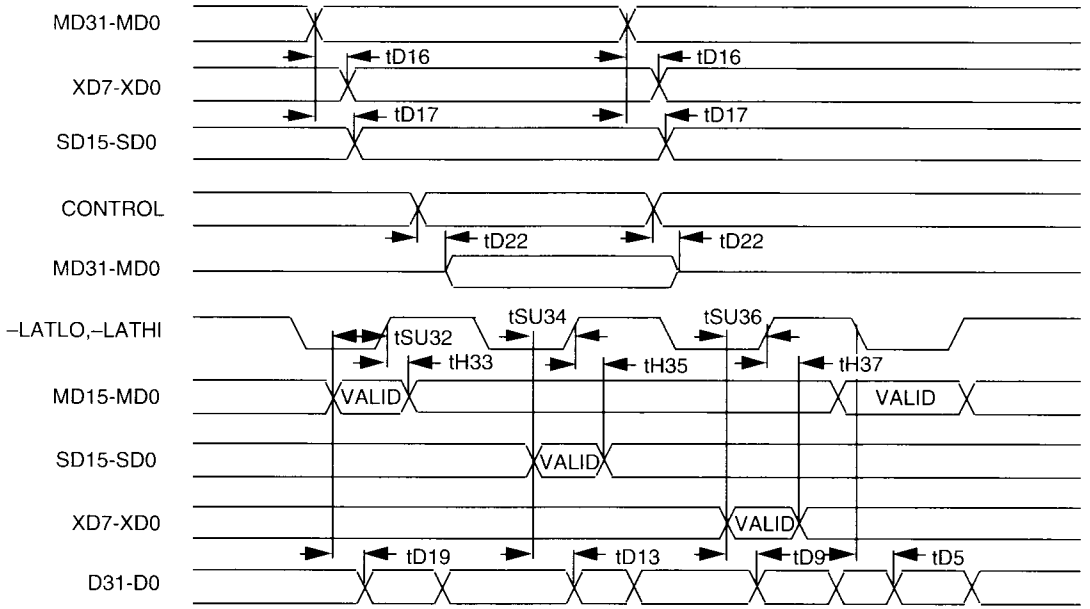
**FIGURE 4.**




**Note:** tD5 is shown with data being sourced from the MD bus. This could also be the SD or XD buses.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Ambient Operating Temperature | −10°C to +70°C |
| Storage Temperature | −65°C to +150°C |
| Supply Voltage to Ground | −0.5 V to 7.0 V |
| Applied Output Voltage | −0.5 V to VDD + 0.3 V |
| Applied Input Voltage | −0.5 V to VDD + 0.3 V |
| Power Dissipation | 500 mW |

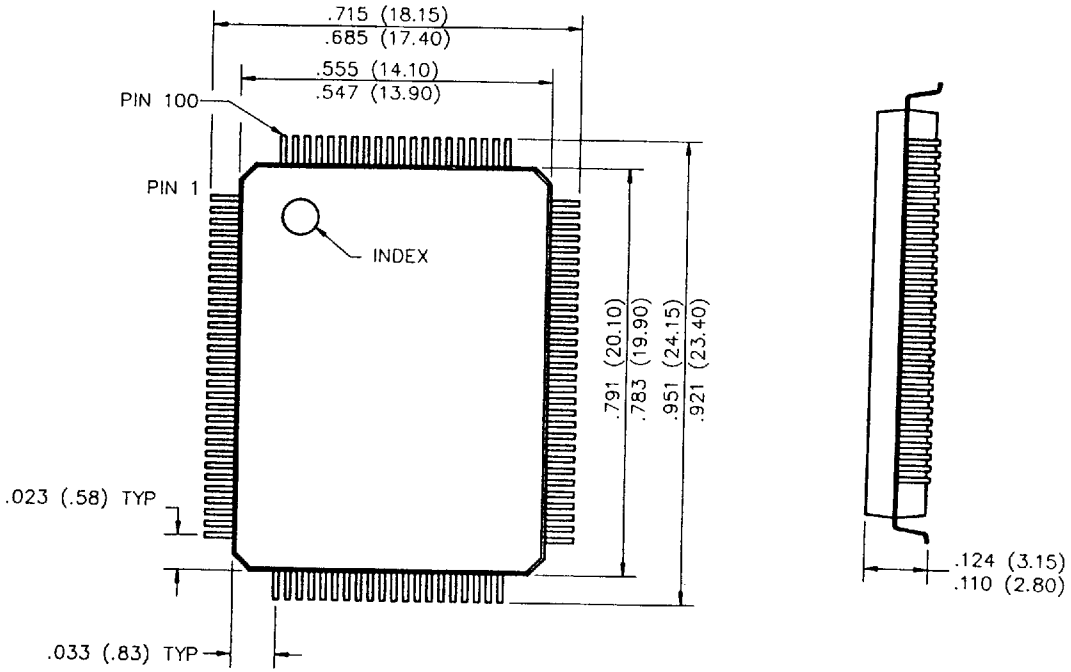
Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

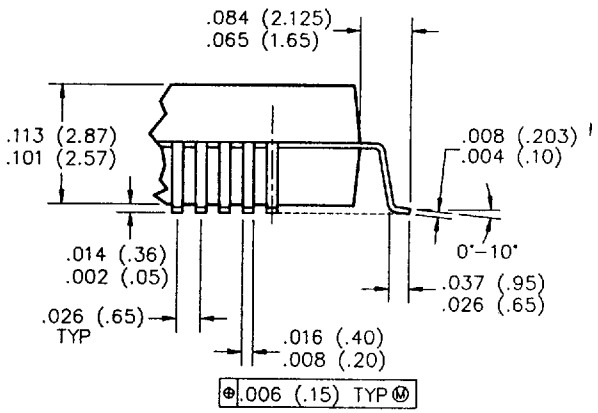
## DC CHARACTERISTICS: TA = 0°C TO +70°C, VDD = 5 V ±5%, VSS = 0 V

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| VIL | Input Low Voltage | −0.5 | 0.8 | V | |
| VIH | Input High Voltage | 2.0 | VDD | V | |
| VOL | Output Low Voltage | | 0.45 | V | |
| VOH | Output High Voltage | 2.4 | | V | |
| IDD | Static Current | | 500 | µA | |
| IDD | Dynamic Current | | 1.5 | mA/MHz | Frequency is data dependant |
| IIL | Input Leakage | | ±10 | µA | |
| IOZ | Three-state Leakage | | ±20 | µA | |

**100-PIN PLASTIC QUAD FLAT PACK**

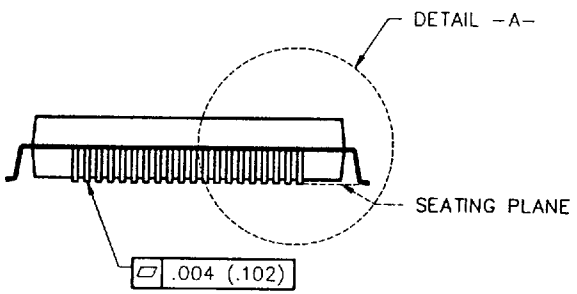
V L S I TECHNOLOGY INC




DETAIL –A–

NOTES:
1. CONTROLLING DIMENSION IS MM.

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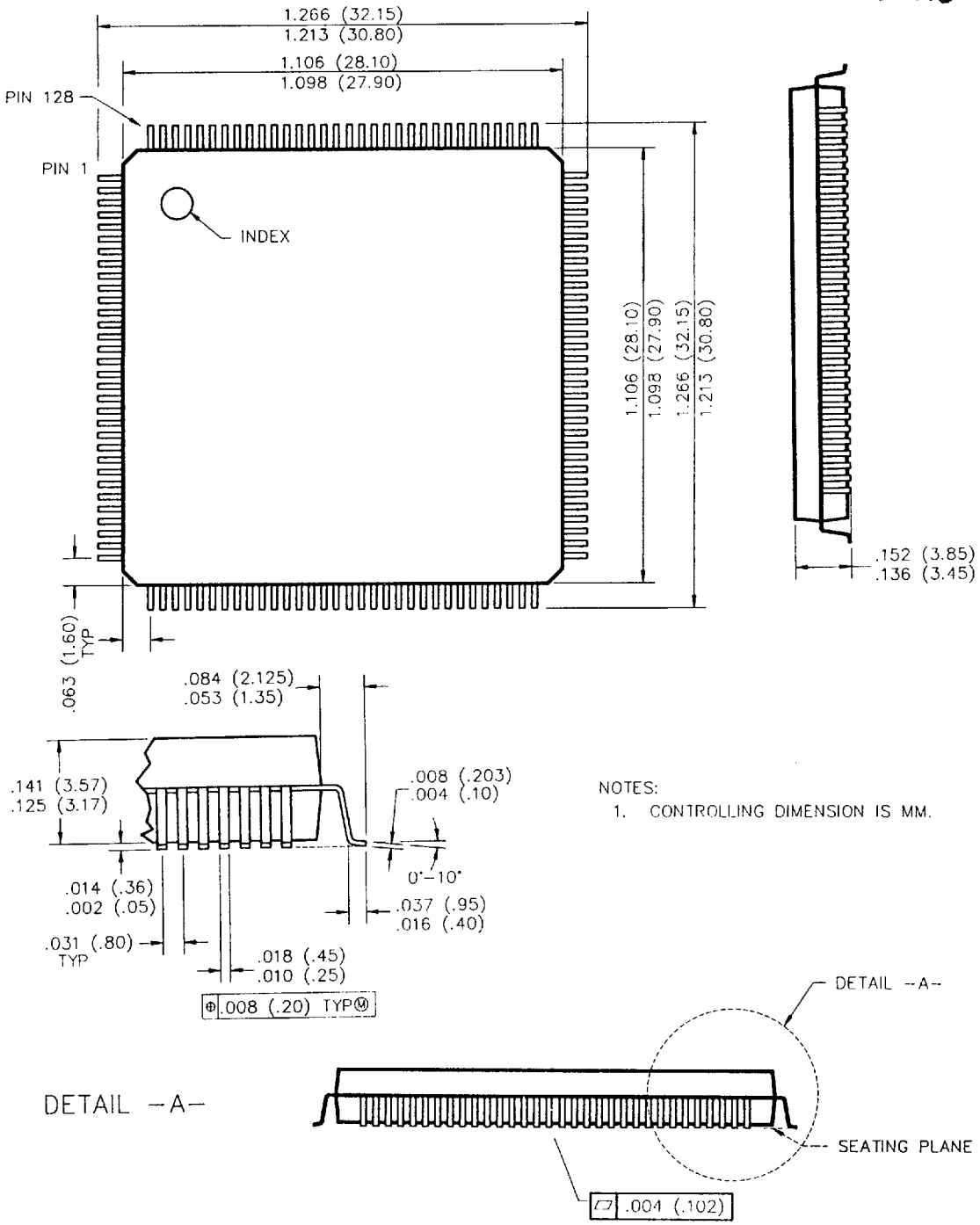
**128-PIN PLASTIC FLAT PACK**

V L S I TECHNOLOGY INC T-90-20

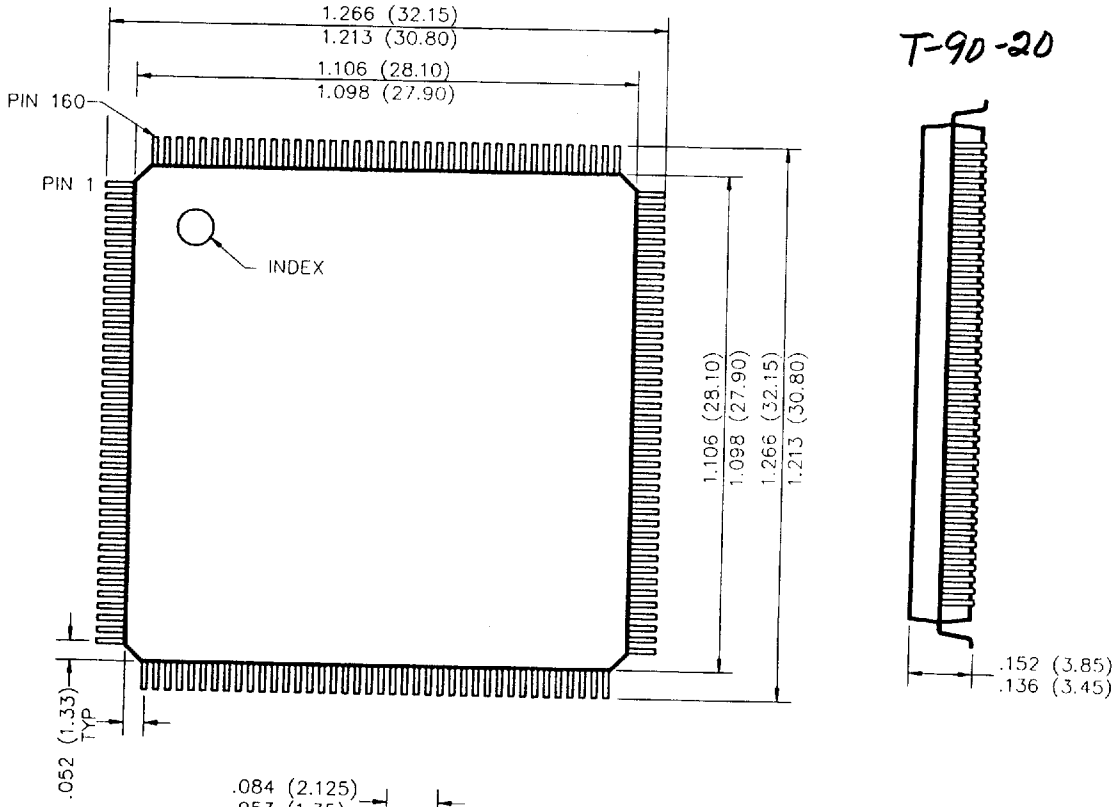


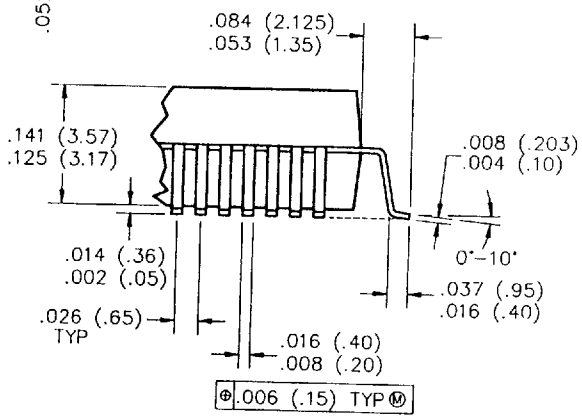

NOTES:
1. CONTROLLING DIMENSION IS MM.

**160-PIN PLASTIC QUAD FLAT PACK**

V L S I TECHNOLOGY INC

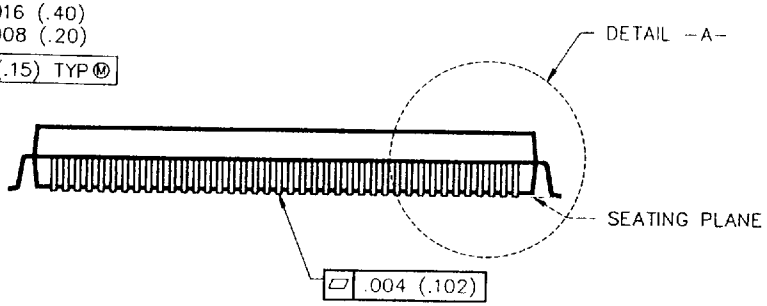
T-90-20




NOTES:
1. CONTROLLING DIMENSION IS MM.

DETAIL –A–

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