VL82C331

ISA BUS CONTROLLER

DESCRIPTION

The VL82C331 ISA Bus Controller replaces several of the LSI controllers used in PC/AT®-type designs with one single 160-lead quad flat pack. The Bus Controller provides the functions of DMA, page address register, timer, interrupt control, Port B logic, slot bus refresh address generation, and real-time clock.

The VL82C331 directly drives the refresh addresses onto the AT slot address bus during refresh cycles in response to a refresh cycle command from the System Controller. To avoid problems with sensitive slot bus add-in cards, the VL82C331 features "bus quiet" mode. When no valid slot bus accesses are occurring, the SA bus data and control lines do not change states. Rather, they retain their previous logic state. Built-in sleep mode features work together with System Controller sleep features to provide a low power system idle state for extension of battery life in portable systems.

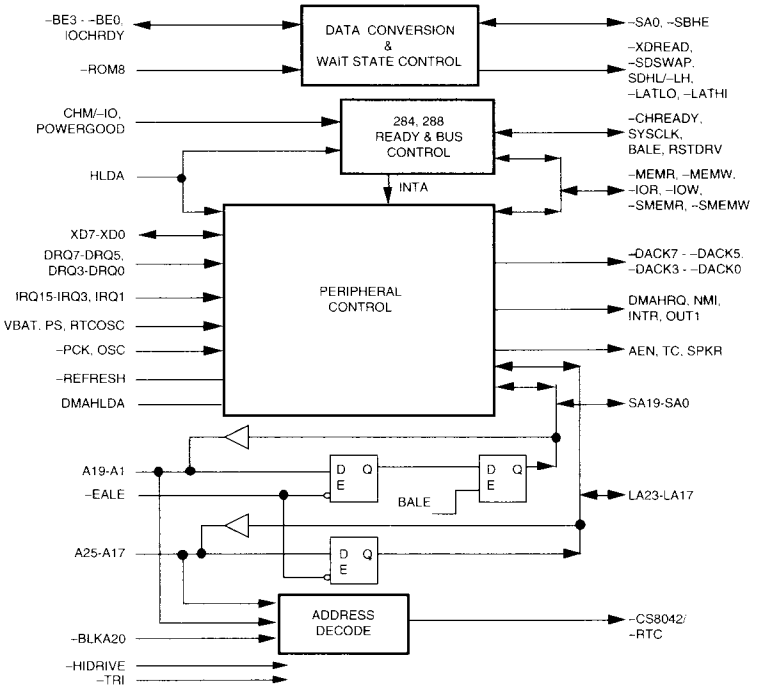
The upgraded DMA channels provide a superset of AT functionality by allowing DMA to the entire 64 Mbyte memory range of the VL82C386 chip set. Additional functionality is provided via DMA wait state, clock, and –MEMR timing programmability.

A –HIDRIVE pin can be externally strapped to provide for 12 or 24 mA drive to the slot bus. If left open, an internal pull-up causes the drive current to default to 12 mA. This allows systems designed with one to four slots to select a lower drive level and reduce bus ringing. A –ROM8 pin selects the bus and bus size to use for BIOS ROM accesses. The choices are 8- or 16-bit wide ROMs.

A three-state test control pin has been added for board level testability.

The VL82C331 features several VLSI Technology megacells, implemented in 1.5-micron CMOS technology, and is intended to work in 286-, 386SX-, or 386DX-based systems with CPU clock speeds up to 33 MHz and bus speeds up to 16 MHz.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C331-FC	Plastic Flat Pack

Note: Operating temperature range is 0°C to +70°C.

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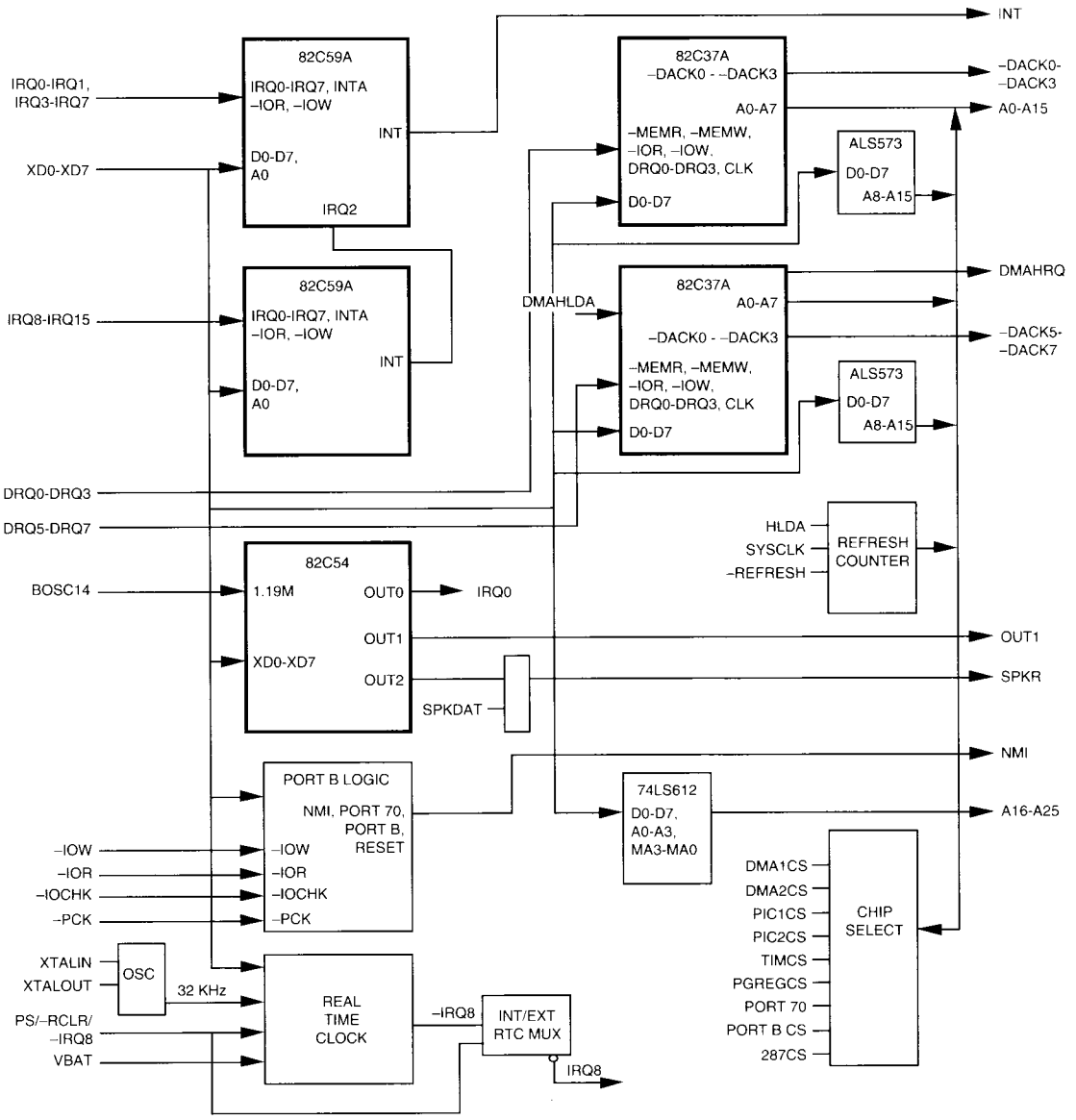
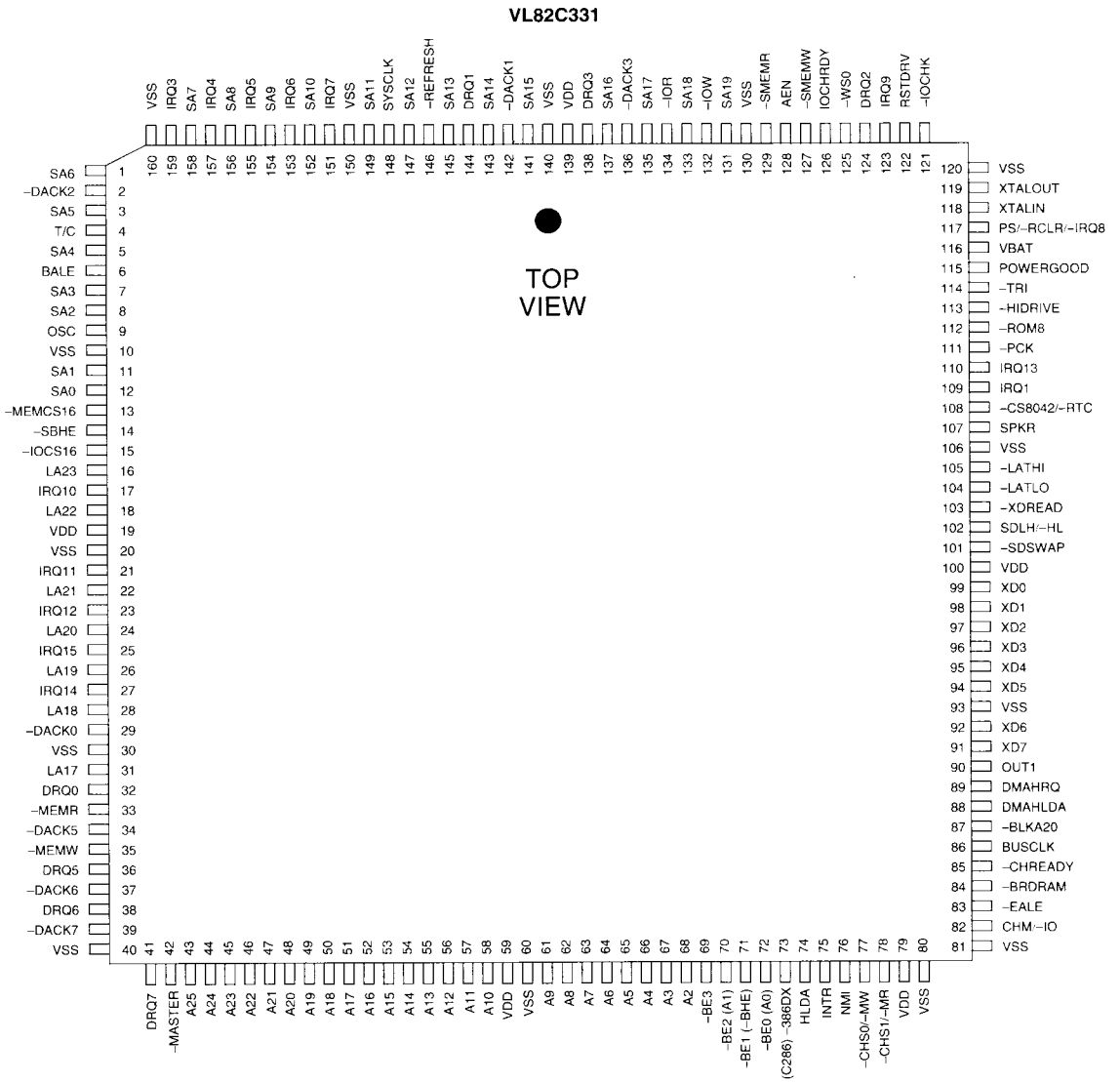
PERIPHERAL CONTROL BLOCK DIAGRAM



PIN DIAGRAM



Pin names surrounded by parenthesis indicate 286/386SX mode.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE			
A25, A24	43, 44	O-TS	Address bus - These pins are outputs during DMA, master, or standard refresh modes. They are high impedance at all other times. A25 and A24 are driven from the alternate 612 registers during DMA and refresh cycles and are driven low during master cycles.
A23-A2	45-58, 61-68	IO-TTL	Address bus - These pins are outputs during DMA, master, or standard refresh modes. They are inputs at all other times. As inputs, they are passed to the SA and LA buses and A15-A2 are used to address I/O registers internal to the bus control chip. As outputs, they are driven from different sources depending on which mode the VL82C331 is in. While in refresh mode, these pins are driven from the 612 and refresh address counter. While in DMA mode, they are driven from the 612 and DMA Controller subsection. If the VL82C331 is in master mode, the pins A23-A17 are driven from the inputs LA23-LA17 and the pins A16-A2 are driven from the inputs SA16-SA2.
–BE3	69	IO-TPU	Byte Enable 3, active low - This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other byte enable signals to generate SA1, SA0, and –SBHE. As an output in 386DX mode SA1, SA0, and –SBHE are used to determine the value of –BE3. This pin should be left unconnected when using this part in 286/386SX mode.
–BE2 (A1)	70	IO-TTL	Byte Enable 2, active low, or A1 - This pin has a dual function depending on the state of the (C286) –386DX input. If (C286) –386DX is high (286/386SX mode), then the pin is treated as address bit 1. If (C286) –386DX is low (386DX mode), the pin is treated as –BE2. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other byte enable signals to generate SA1, SA0, and –SBHE. As an output in 386DX mode, SA1, SA0, and –SBHE are used to determine the value of –BE2. When in 286/386SX mode, it is interpreted as address A1 and passed to SA1. As an output in 286/386SX mode it is driven from the SA1 input.
–BE1 (–BHE)	71	IO-TTL	Byte Enable 1 or Byte High Enable, active low - This pin has a dual function depending on the state of the (C286) –386DX input. If (C286) –386DX is high (286/386SX mode), then the pin is treated as –BHE. If (C286) –386 is low (386DX mode), the pin is treated as –BE1. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other byte enable signals to generate SA1, SA0, and –SBHE. As an output in 386DX mode, SA1, SA0, and –SBHE are used to determine the value of –BE1. When in 286/386SX mode, it is interpreted as –BHE and passed to –SBHE. As an output in 286/386SX mode, it is driven from the –SBHE input.
–BE0 (A0)	72	IO-TTL	Byte Enable 0, active low, or A0 - This pin has a dual function depending on the state of the (C286) –386DX input. If (C286) –386DX is high (286 mode), then the pin is treated as address bit 0. If (C286) –386DX is low (386DX mode), the pin is treated as –BE0. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other Byte Enable signals to generate SA1, SA0, and –SBHE. As an output in 386DX mode, SA1, SA0, and –SBHE are used to determine the value of –BE0. When in 286/386SX mode, it is interpreted as A0 and passed to SA0. As an output in 286/386SX mode, it is driven from the SA0 input.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
(C286)–386DX	73	I-TPU	CPU is 286/386SX or 386DX - This pin defines the type of address bus to which the Bus Controller chip is interfaced. If the pin is tied high, the address bus is assumed to be emulating 286/386SX signals. In this mode, A25, A24, and –BE3 would be left unconnected. The pins –BE2 (A1), –BE1 (–BHE) and –BE0 (A0) would take on the 286/386SX functions. If the pin is tied low, A25, A24 can be used to generate up to 64 Mbyte addressing for DMA, and the byte enable pins will take on the normal 386DX addressing functions. This pin has an internal pull-up to cause the chip to default to 286/386SX mode if left unconnected. This pin is a hard wiring option and must not be changed dynamically during operation. When strapped for 286/386SX mode, the VL82C331 is assumed to be interfaced to the VL82C320 System Controller which in turn may be strapped for 286 or 386SX operation.
HLDA	74	I-TTL	Hold Acknowledge - This is the hold acknowledge pin directly from the CPU. It is used to control direction on address and command pins. When HLDA is low, the VL82C331 is defined as being in the CPU mode. In the CPU mode, the local address bus (A bus) pins are inputs. The system address bus (SA and LA) pins along with the command pins (–MEMR, –MEMW, –IOR and –IOW) are outputs. When HLDA is high, the VL82C331 can be in DMA, refresh, or master modes. In both DMA and refresh modes, the commands and all address buses (A, SA and LA) are outputs. In master mode, the commands and system address bus (SA and LA) pins are inputs and the local address bus (A bus) pins are outputs. The SA bus is passed directly to the A bus except bits 17, 18, and 19 are ignored. LA23-LA17 is passed directly to A23-A17.
INTR	75	O	Interrupt Request - INTR is used to interrupt the CPU and is generated by the 8259 megacells any time a valid interrupt request input is received.
NMI	76	O	Non-Maskable Interrupt - This output is used to drive the NMI input to the CPU. This signal is asserted by either a parity error (indicated by –PCK being asserted after the ENPARCK bit in Port B has been asserted), or an I/O channel error (indicated by –IOCHCK being asserted after the ENIOCK bit in Port B has been asserted). The NMI output is enabled by writing a 0 to bit D7 of I/O port 70h. NMI is disabled on reset.
SYSTEM CONTROLLER INTERFACE			
–CHS0/–MW	77	IO-TTL	Channel Status 0 or active low Memory Write - This input is used along with –CHS1 and CHM/–IO to determine what type of bus cycle the Bus Controller is to perform. This input has the same meaning and timing requirements as the S0 signal for a 286 microprocessor. –CHS0 going active indicates a write cycle unless –CHS1 is also active. When both status inputs are active it indicates an interrupt acknowledge cycle. This input is synchronized to the BUSCLK input. Activation of HLDA reverses this signal to become an output to the System Controller. It is then a –MEMW signal for DMA or Bus Master access to system memory.
–CHS1/–MR	78	IO-TTL	Channel Status 1 or active low Memory Read - This input is used along with –CHS0 and CHM/–IO to determine the bus cycle type. This input has the same meaning and timing requirements as the S1 signal for a 286 microprocessor. –CHS1 going active indicates a read cycle unless –CHS0 is also active. When both status inputs are active it indicates an interrupt acknowledge cycle. This input is synchronized to the BUSCLK input. Activation of HLDA reverses this signal to become an output to the System Controller. It is then a –MEMR signal for DMA or Bus Master access to system memory.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
CHM/–IO	82	I-TTL	Channel Memory or active low I/O select - This input is used along with –CHS0 and –CHS1 to determine the bus cycle type. This input has the same meaning and timing requirements as the M/–IO signal for a 286/386SX microprocessor. CHM/–IO is sampled anytime –CHS0 or –CHS1 is active. If sampled high, it indicates a memory read or write cycle. If sampled low, an I/O read or write cycle should be executed. This input is synchronized to the BUSCLK input.
–EALE	83	I-TPU	Early Address Latch Enable, active low - This input is used to latch the A23-A2 and byte enable signals. The latches are open when –EALE is low and hold their value when –EALE is high. The latched addresses are fed directly to the LA23-LA17 bus to provide more address setup time on the bus before a command goes active. The lower latched addresses are latched again with an internal ALE signal as soon as –CHS0 or –CHS1 is sampled active and fed to the SA19-SA0 and –SBHE outputs. In a 386DX system, this input is connected directly to the –ADS output from the CPU. In a 286/386SX system, this input is connected to the –EALE output from the VL82C320 System Controller.
–BRDRAM	84	I-TTL	On-board DRAM, active low - An input from the System Controller indicating that the on-board DRAM is being addressed.
–CHREADY	85	O	Channel Ready, active low - This output is maintained in the active state when no bus accesses are active. This indicates that the VL82C331 is ready to accept a new command. During normal bus accesses, –CHREADY is negated as soon as a valid bus requested is sampled on the –CHS0 and –CHS1 inputs. It is asserted again to indicate that the VL82C331 is ready to complete the current cycle. The bus command signals are then terminated on the next falling edge of the BUSCLK input.
BUSCLK	86	I-CMOS	Bus Clock - This is the main clock input for the VL82C331. It runs at twice the frequency desired for the SYSCLK output. All inputs are synchronous with the falling edge of this input.
–BLKA20	87	I-TTL	Block A20, active low - This input is used while HLDA is low to force the LA20 outputs low anytime it is active. When –BLKA20 is negated LA20 is generated from A20.
DMAHRQ	89	O	Hold Request - This output is generated by the DMA Controller any time a valid DMA request is received. It is connected to the DMAHRQ pin on the System Controller.
DMAHLDA	88	I-TTL	DMA Hold Acknowledge - An input from the System Controller which indicates that the current hold acknowledge state is for the DMA Controller or other Bus Master.
OUT1	90	O	Output 1 - Indicates a refresh request to the System Controller. This is the 15 μs output of timer channel 1.
ROM INTERFACE			
–ROM8	112	I-TPU	8/16 bit ROM select - This input indicates the width of the ROM BIOS. If –ROM8 is low, the VL82C331 chip generates 8- to 16-bit conversions for ROM accesses. Data buffer controls are generated assuming the ROM is on the MD bus in 386DX systems and on the XD bus in 286/386SX systems. If –ROM8 is high, data buffer controls are generated assuming 16-bit wide ROMs are on the MD bus in 386DX systems or the D bus in 286/386SX systems.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
BUS INTERFACE			
–IOR	134	IO-TTL	I/O Read, active low - This signal is an input when HLDA is high and –MASTER is low. It is an output at all other times. When HLDA is low, –IOR is driven from the 288 Bus Controller megacell. When HLDA is high and –MASTER is high, it is driven by the 8237 DMA Controller megacells. This pin requires an external 10k ohm pull-up resistor.
–IOW	132	IO-TTL	I/O Write, active low - This signal is an input when HLDA is high and –MASTER is low. It is an output at all other times. When HLDA is low, –IOW is driven from the 288 Bus Controller megacell. When HLDA is high and –MASTER is high, it is driven by the 8237 DMA Controller megacells. This pin requires an external 10k ohm pull-up resistor.
–MEMR	33	IO-TTL	Memory Read, active low - This signal is an input when HLDA is high and –MASTER is low. It is an output at all other times. When HLDA is low, –MEMR is driven from the 288 Bus Controller megacell. When HLDA is high and –MASTER is high, it is driven by the 8237 DMA Controller megacells. This signal does not pulse low for DMA addresses above 16 Mbytes. DMA above 16 Mbytes is only performed to the system board, never to the slot bus. This pin requires an external 10k ohm pull-up resistor.
–MEMW	35	IO-TTL	Memory Write, active low - This signal is an input when HLDA is high and –MASTER is low. It is an output at all other times. When HLDA is low, –MEMW is driven from the 288 Bus Controller megacell. When HLDA is high and –MASTER is high, it is driven by the 8237 DMA Controller megacells. This pin requires an external 10k ohm pull-up resistor.
–SMEMR	129	O-TS	Memory Read, active low - –SMEMR is asserted on memory read cycles to addresses below 1 Mbyte and all refresh cycles. It is three-stated for all addresses above 1 Mbyte. This pin requires an external 10k ohm pull-up resistor.
–SMEMW	127	O-TS	Memory Write, active low - –SMEMW is asserted on memory write cycles to addresses below 1 Mbyte. It is three-stated for all addresses above 1 Mbyte. This pin requires an external 10k ohm pull-up resistor.
LA23-LA17	16, 18, 22, 24, 26, 28 31	IO-TTL	Latchable Address bus - This bus is an input when HLDA is high and –MASTER is low. It is an output bus at all other times. When HLDA is low, the LA bus is driven by the latched values from the A bus. When HLDA is high and –MASTER is high, the LA bus is driven by the 612 memory mapper for DMA cycles and normal refresh. The LA bus is latched internally with the –EALE input.
SA19-SA17	131, 133, 135	O-TS	System Address bus - This bus is three-stated when HLDA is high and –MASTER is low. It is an output bus at all other times. When HLDA is low, the SA bus is driven by the latched values from the A bus. When HLDA is high and –MASTER is high, the SA bus is driven by the 8237 DMA Controller megacells or refresh address generator. The SA bus will become valid in the middle of the status cycle generated by the –CHS0 and –CHS1 inputs. They are latched with an internally generated ALE signal.
SA16-SA0	137, 141, 143 145, 147, 149, 152, 154, 156 158, 1, 3, 5, 7, 8, 11, 12	IO-TTL	System Address bus - This bus an input when HLDA is high and –MASTER is low. It is an output bus at all other times. When HLDA is low, the SA bus is driven by the latched values from the A bus. When HLDA is high and –MASTER is high, the SA bus is driven by the 8237 DMA Controller megacells or refresh address generator. The SA bus will become valid in the middle of the status cycle generated by the –CHS0 and –CHS1 inputs. They are latched with an internally generated ALE signal.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–SBHE	14	IO-TTL	System Byte High Enable, active low - This pin is controlled the same way as the SA bus. It is generated from a decode of the –BE inputs in CPU mode. It is forced low for 16-bit DMA cycles and forced to the opposite value of SA0 for 8-bit DMA cycles.
–REFRESH	146	IT-OD	Refresh signal, active low - This I/O signal is pulled low whenever a de-coupled refresh command is received from the System Controller. It is used as an input to sense refresh requests from external sources such as the System Controller for coupled refresh cycles or Bus Masters. It is used internally to clock the refresh address counter and select a location in the memory mapper which drives A23-A17. –REFRESH is an open drain output capable of sinking 24 mA.
SYSCLK	148	O	System Clock - This output is half the frequency of the BUSCLK input. The bus control outputs BALE and the –IOR, –IOW, –MEMR and –MEMW are synchronized to SYSCLK.
OSC	9	I-TTL	Oscillator - This is the buffered input of the external 14.318 MHz oscillator.
RSTDRV	122	O	Reset Drive, active high - This output is a system reset generated from the POWERGOOD input. RSTDRV is synchronized to the BUSCLK input.
BALE	6	O	Buffered Address Latch Enable, active high - A pulse which is generated at the beginning of any bus cycle initiated from the CPU. BALE is forced high anytime HLDA is high.
AEN	128	O	Address Enable - This output goes high anytime the inputs HLDA and –MASTER are both high.
T/C	4	O	Terminal Count - This output indicates that one of the DMA channels terminal count has been reached. This signal directly drives the system bus.
–DACK7- –DACK5, –DACK3 - –DACK0	39, 37, 34, 136, 2, 142, 29	O	DMA Acknowledge, active low - These outputs are the acknowledge signals for the corresponding DMA requests. The active polarity of these lines is set active low on reset. Since the 8237 megacells are internally cascaded together, the polarity of the –DACK signals must not be changed. This signal directly drives the system bus.
DRQ7-DRQ5 DRQ3-DRQ0	41, 38, 36, 138, 124, 144, 32	I-TSPU	DMA Request - These asynchronous inputs are used by an external device to indicate when they need service from the internal DMA Controllers. DRQ0-DRQ3 are used for transfers from 8-bit I/O adapters to/from system memory. DRQ5-DRQ7 are used for transfers from 16-bit I/O adapters to/from system memory. DRQ4 is not available externally as it is used to cascade the two DMA Controllers together.
IRQ15-IRQ9 IRQ7-IRQ3, IRQ1	25, 27, 110, 23, 21, 17, 123, 151, 153, 155, 157, 159, 109	I-TSPU	Interrupt Request - These are the asynchronous interrupt request inputs for the 8259 megacells. IRQ0 and IRQ2 are not available as external inputs to the chip, but are used internally. IRQ0 is connected to the output of the 8254 counter 0. IRQ2 is used to cascade the two 8259 megacells together. All IRQ input pins are active high.
–MASTER	42	I-TTL	Master, active low - This input is used by an external device to disable the internal DMA controllers and get access to the system bus. When asserted it indicates that an external Bus Master has control of the bus.
–MEMCS16	13	I-TTL	Memory Chip Select 16 bit - This input is used to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16-to-8 conversion is done anytime the Sytem Controller requests a 16-bit memory cycle and –MEMCS16 is sampled high.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–IOCS16	15	I-TTL	I/O Chip Select 16 bit - This input is used to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16-to-8 conversion is done anytime the System Controller requests a 16-bit I/O cycle and –IOCS16 is sampled high.
–IOCHK	121	I-TTL	I/O Channel Check, active low - This input is used to indicate that an error has taken place on the I/O bus. If I/O checking is enabled, an –IOCHK assertion by a peripheral device generates an NMI to the processor. The state of the –IOCHK signal is read as data bit D6 of the Port B register.
IOCHRDY	126	I-TTL	I/O Channel Ready - This input is pulled low in order to extend the read or write cycles of any bus access initiated by the CPU, DMA Controllers or Refresh Controller. The default number of wait states for cycles initiated by the CPU are four wait states for 8-bit peripherals, one wait state for 16-bit peripherals and three wait states for ROM cycles. One DMA wait state is inserted as the default for all DMA cycles. Any peripheral that cannot present read data, or strobe-in write data in this amount of time must use IOCHRDY to extend these cycles.
–WS0	125	I-TTL	Wait State 0, active low - This input is pulled low by a peripheral on the S bus to terminate a CPU controlled bus cycle earlier than the default values defined internally on the chip.
POWERGOOD	115	I-TSPU	System power-on reset - This input signals that power to the board is stable. A Schmitt-trigger input is used. This allows the input to be connected directly to an RC network.
PERIPHERAL INTERFACE			
–CS8042/–RTC	108	O	Chip Select for 8042, active low - This output is active any time an SA address is decoded at 60h or 64h. It is intended to be connected to the chip select of the Keyboard Controller. If BUSCTL6 = 1, this pin is also active for RTC accesses at 70h and 71h. This is for use when the internal RTC is disabled and an external RTC is used.
XTALIN	118	I-CMOS	Crystal Input - An internal oscillator input for the real-time clock crystal. It requires a 32.768 KHz external crystal or stand-alone oscillator.
XTALOUT	119	O	Crystal Output - An internal oscillator output for the real-time clock crystal. See XTALIN. This pin is a "no connect" when an external oscillator is used.
PS/ –RCLR/ –IRQ8	117	I-CSPU	Power Sense, active high - Used to reset the status of the Valid RAM and Time (VRT) bit. This bit is used to indicate that the power has failed, and that the contents of the RTC may not be valid. This pin is connected to an external RC network. When BUSCTL6 = 1, this pin becomes –IRQ8 input for use with an external RTC. However, the –IRQ8 signal remains electrically connected to the RTC's PS and –RCLR inputs. Therefore, generation of an active –IRQ8 signal by an external RTC will clear the VL82C331's RTC CMOS RAM.
VBAT	116	I	Voltage Battery - Connected to the RTC hold-up battery.
SPKR	107	O	Speaker - This output drives an externally buffered speaker. This signal is created by gating the output of Timer 2. Bit 1 of Port B, 61H, is used to enable the speaker output, and bit 0 is used to gate the output of the timer.
DATA BUFFER INTERFACE			
XD7-XD0	91, 92, 94-99	IO-TTL	Peripheral data bus - The bidirectional X data bus outputs data on an INTA cycle or I/O read cycle to any valid address within the VL82C331. It is configured as an input at all other times.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–SDSWAP	101	O	System Data Swap, active low during some 8-bit accesses - It indicates that the data on the SD bus must be swapped from low byte to high byte or vice versa depending on the state of the SDLH/–HL pin. –SDSWAP is active for 8-bit DMA cycles when an odd address access occurs for data more than one byte wide. For non-DMA accesses, –SDSWAP is active for any bus cycle to an 8-bit peripheral that is addressing the odd byte.
SDLH/–HL	102	O	System Data Low to High, or High to Low - This signal is used to determine which direction data bytes must be swapped when –SDSWAP is active. When SDLH/–HL is high, it indicates that data on the low byte must be transferred to the high byte. When SDLH/–HL is low, it indicates that data on the high byte must be transferred to the low byte. SDLH/–HL is low for 8-bit DMA memory read cycles. For non-DMA accesses, SDLH/–HL is low for any memory write or I/O write when –SBHE is low. SDLH/–HL is high at all other times.
–XDREAD	103	O	Peripheral Data Read - This output is active low any time an INTA cycle occurs or an I/O read occurs to the address space from 0000h to 00F7h, which is defined as being resident on the peripheral bus.
–LATLO	104	O	Latch Low byte - This output is generated for all I/O read and memory read bus accesses to the low byte. It is active with the same timing as the read command and returns high at the same time as the read command. This signal latches the data into the data buffer chip so that it can be presented to the CPU at a later time. This step is required due to the asynchronous interface between the System Controller and VL82C331.
–LATHI	105	O	Latch High byte - This output is generated for all I/O read and memory read bus accesses to the high byte. It is active with the same timing as the read command and returns high at the same time as the read command. This signal latches the data into the data buffer chip so that it can be presented to the CPU at a later time. This step is required due to the asynchronous interface between the System Controller and VL82C331.
–PCK	111	I-TPU	Parity Check input, active low with pull-up - Indicates that a parity error has occurred in the on-board memory array. Assertion of this signal (if enabled) generates an NMI to the processor. The state of the –PCK signal is read as data bit D7 of the Port B register.
–HIDRIVE	113	I-TPU	High Drive Enable - This pin is a wire strap option. When this input is low, all bus drivers defined with an IOL spec of 24 mA will sink the full 24 mA of current. When this input is high, all pins defined as 24 mA have the output low drive capability cut in half to 12 mA.
TEST MODE PIN			
–TRI	114	I-TPU	Three-state - This pin is used to control the three-state drive of all outputs and bidirectional pins on the chip. If this pin is pulled low, all pins on the chip except XTALOUT are in a high impedance mode. This is useful during system test when test equipment or other chips drive the signals or for hardware fault tolerant applications. –TRI has an internal pull-up.
POWER AND GROUND PINS			
VDD	19, 59, 79, 100, 139	PWR	Power connection, nominally +5 volts. These pins should each have 0.1 µF bypass capacitors.
VSS	10, 20, 30, 40, 60, 80, 81, 93, 106, 120, 130, 140, 150, 160	GND	Ground connection, 0 volts.

SIGNAL TYPE LEGEND

Signal Code	Signal Type
I-TTL	TTL level input
I-TPU	Input with 30k ohm pull-up resistor
I-TSPU	TTL Schmitt-trigger input with 30k ohm pull-up resistor
I-CSPU	CMOS Schmitt-trigger input with 30k ohm pull-up resistor
I-CMOS	CMOS level input
IO-TTL	TTL level input/output
IO-TPU	TTL level input/output with 30k ohm pull-up resistor
IT-OD	TTL level input/open drain output
O	CMOS and TTL level compatible output
O-TS	Three-state level output
GND	Ground
PWR	Power

FUNCTIONAL DESCRIPTION

DETAILED SUBSYSTEM SPECIFICATION

The sections that follow cover detailed operational information for the various logical groupings of VL82C331 ISA Bus Controller subsystems. In most of these sections, the effect of any applicable configurable elements that can be controlled via indexed configuration registers is discussed at length. Operation of these registers is repeated in summary form in the "Configuration Register Operational Summary" section. However, some lesser configurable functions are described only in this section. Do not assume that the information in that section is discussed elsewhere.

MAJOR LOGIC BLOCK CHIP SELECT GENERATION

The VL82C331 ISA Bus Controller utilizes six VLSI Technology megacells; two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 counter/timer, and one real-time clock. Programmable I/O access is required for these and other internal logic blocks. The logic block chip select subsection consists of decodes of the signals –MASTER, HLDA and the address bus A15-A0. This decode is used to generate the chip select signals to each major logic block within the Bus Controller.

Data Port 00EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
ROMDMA	ROM Wait States		**8-Bit DMA Wait States**		**16-Bit DMA Wait States**		**DMA Clock**	**MEMR Timing**

The DMA subsection consists of two 8237 megacells, two 8-bit latches to hold the middle range address bits during a DMA cycle and 1.25 74LS612 page register equivalents to generate the upper range address bits during a DMA operation. The DMA subsection also has logic to allow separate programming of the number of wait states for 8- and 16-bit DMA cycles. Defaults are standard AT-compatible wait states. The timing for the leading edge of the –MEMR signal is also programmable. The DMA subsection provides a total of seven external DMA channels. Four of these channels are used for 8-bit I/O adapters and the other three are used for 16-bit I/O adapters. All channels are capable of addressing all memory locations in a 64 Mbyte address space.

The interrupt controller subsection consists of two 8259 megacells cascaded together to allow for 15 possible interrupt sources. IRQ2 is used internally. –IRQ8 is available externally only when the internal RTC is disabled.

The counter/timer subsection contains a single 8254 megacell. This megacell has three internal counters. All of the counters are driven by a common clock input. The output of Counter 0 is routed to the interrupt controller subsection to be used as interrupt request zero. The output from Counter 1 drives the OUT1 pin to initiate refresh cycles. Counter 2's output is gated with a signal from the Port B register and is then output as SPKR to drive the speaker.

The RTC megacell (82C018) is a direct replacement for the 146818A real-time clock component. Clock functions include the following:

- Time of day clock
- Alarm function
- 100 year calendar function
- Programmable periodic interrupt output
- 114 bytes of User RAM

TABLE 1. A15-A0 ADDRESS DECODES

A15-A8	A7	A6	A5	A4	A3	A2	A1	A0	Address	Chip Select Generated
0	0	0	0	0	X	X	X	X	0000-00F	DMA1 (8237)
0	0	0	1	X	X	X	X	X	0020-03F	Interrupt 1 (8259)
0	0	1	0	0	0	0	X	X	0040-043	Counter (8254)
0	0	1	1	0	X	X	X	1	0061-06F	Port B (Odd Only)
0	0	1	1	1	0	0	0	0	0070	NMI Logic
0	0	1	1	1	0	0	0	X	0070-071	Real Time Clock Access Ports
0	1	0	0	0	X	X	X	X	0080-08F	DMA Page Registers
0	1	0	0	1	0	0	1	0	0092	Port A*
0	1	0	1	X	X	X	X	X	00A0-0BF	Interrupt 2 (8259)
0	1	1	0	X	X	X	X	X	00C0-0DE	DMA2
0	1	1	1	X	X	X	X	X	00E0-0EF	Configuration Registers*
0	1	1	1	X	X	X	X	X	00F0-0FF	Coprocessor CS and RESET*
0	0	1	1	0	0	X	0	0	60, 64	–CS8042

* These entries are shown for completeness only. They are decoded and controlled by the System Controller except for ECh and EDh, which are also used by the V82C331's configuration registers.

Notes: 1. Address bits A15-A0 are used to generate chip selects for each of the individual megacells. A map of the address decode is shown in Table 1.

2. For all the address decodes shown, the inputs HLDA or –MASTER must be low to generate a megacell chip select.

DMA SUBSECTION

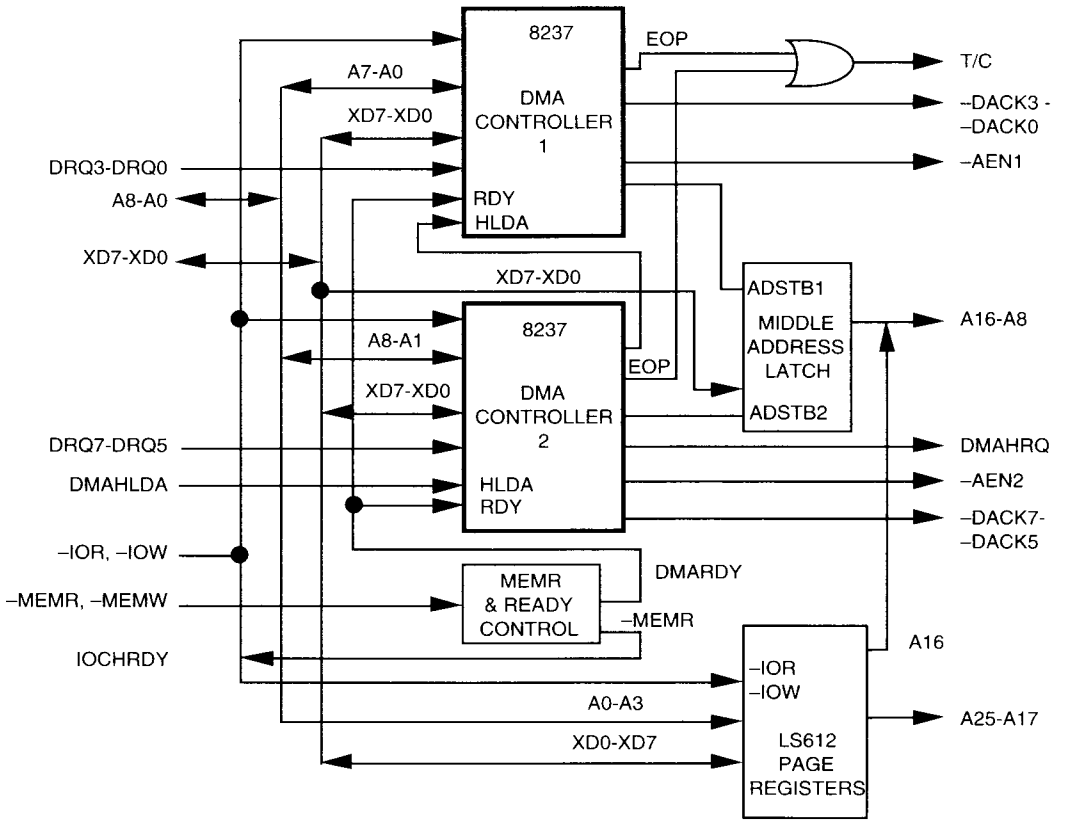
The DMA subsection controls DMA transfers between an I/O channel and on- or off-board memory. It generates a hold request to the CPU when an I/O channel requests a DMA operation. Once the hold has been acknowledged, the DMA Controller will drive the CPU and the slot address buses. DMAs can occur over the full 16M range available on the slot bus and the 64M range of system board DRAM and drive the appropriate bus command signals depending on whether the DMA is a memory read or write. The DMA Controllers are 8237-compatible. Internal latches are provided for latching the middle address bits output by the 8237 megacells on the data bus, and 1.25 74LS612 memory mappers are provided to generate the upper address bits. Since a single 74LS612 is only capable of accessing 16 Mbytes in an AT-compatible fashion, two additional bits are required to extend the architecture for a 64 Mbyte system. Therefore, an extra 1/4 of a 74LS612 is implemented. This is discussed in the section "Page Registers" and is functional only when used with the VL82C386 chip set.

DMA Controllers

The Bus Controller supports seven DMA channels using two 8237 equivalent megacells capable of running at SYSCLK or SYSCLK/2. This option is programmable via the indexed configuration register, ROMDMA. DMA Controller 1 contains channels 0-3. These channels support 8-bit I/O adapters. Channels 0-3 are used to transfer data between 8-bit peripherals and 8- or 16-bit memory. A full 26-bit address is output for each channel so they can all transfer data throughout the entire 64 Mbyte system address space when used with the VL82C386 chip set. Each channel can transfer data in 64 kilobyte pages.

DMA Controller 2 contains channels 4-7. Channel 4 is used to cascade DMA Controller 1, so it is not available externally. Channels 5-7 support 16-bit I/O adapters to transfer data between 16-bit I/O adapters and 16-bit system memory. A full 26-bit address is output for each channel so they can all transfer data throughout the entire 64 Mbyte system address space. Each channel can transfer data in 128 kilobyte pages. Channels 5, 6, and 7 are meant to transfer 16-bit words only and cannot address odd bytes in system memory.

FIGURE 1. DMA SUBSECTION BLOCK DIAGRAM



DMA Controller Registers
The 8237 megacells can be programmed any time HLDA is inactive. Table 2 lists the addresses of all registers which can be read or written in the 8237 megacells. Addresses under DMA2 are for the 16-bit DMA channels and DMA1 corresponds to the 8-bit channels. When writing to a channel's address or word count register, the data is written into both the base register and current register simultaneously. When reading a channel's address or word count register only, the current address or word count can be read. The base address and base word count are not accessible for reading.

The address and word count registers for each channel are 16-bit registers. The value on the data bus is written into the upper or lower byte depending on the state of the internal addressing flip-flop. This flip-flop can be cleared by the clear byte pointer flip-flop command. After this command, the first read/write to an address or word count register will read/write to the low byte of the 16-bit register and the byte pointer flip-flop will toggle to a one. The next read/write to an address or word count register will read/write to the high byte of the 16-bit register and the byte pointer flip-flop will toggle back to a zero. Refer to the 8237 data sheet for more information on programming the 8237 megacell.

The 8237 DMA Controller megacells allow the user to program the active level (low or high) of the DREQ and –DACK signals. Since the two megacells are cascaded together internally on the chip, these signals should always be programmed with the DREQ signals active high and the –DACK signals active low.

When programming the 16-bit channels (channels 5, 6, and 7), the address which is written to the base address register must be the real address divided by two. Also, the base word count for the 16-bit channels is the number of 16-bit words to be transferred, not the number of bytes as is the case for the 8-bit channels.

It is recommended that all internal locations, especially the mode registers, in the 8237 megacells be loaded with some valid value. This should be done even if the channels are not used.

Middle Address Bit Latches
The middle DMA address bits are held in an internal 8-bit register. The DMA Controller will drive the value to be loaded onto the internal data bus and then issue an address strobe signal to latch the data bus value into this register. An address strobe is issued at the beginning of a DMA cycle and any time the lower 8-bit address increments across the 8-bit subpage boundary during block transfers. This register cannot be written to or read externally. It is loaded only from the address strobe signals from the megacells and the outputs go only to the A16-A8 pins.

TABLE 2. 8237 READ/WRITE ADDRESS

Hex Address		
DMA2	DMA1	Register Function
00C0	0000	Channel 0 Base and Current Address Register
00C2	0001	Channel 0 Base and Current Word Count Register
00C4	0002	Channel 1 Base and Current Address Register
00C6	0003	Channel 1 Base and Current Word Count Register
00C8	0004	Channel 2 Base and Current Address Register
00CA	0005	Channel 2 Base and Current Word Count Register
00CC	0006	Channel 3 Base and Current Address Register
00CE	0007	Channel 3 Base and Current Word Count Register
00D0	0008	Read Status Register/Write Command Register
00D2	0009	Write Request Register
00D4	000A	Write Single Mask Register Bit
00D6	000B	Write Mode Register
00D8	000C	Clear Byte Pointer Flip-flop
00DA	000D	Read Temporary Register/Write Master Clear
00DC	000E	Clear Mask Register
00DE	000F	Write All Mask Register Bits

Page Registers

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
612AXS (82)	Enable FF	4XX Enable	1	1	1	1	1	FF PTR

An extended 74LS612 cell is used in the Bus Controller to generate the page registers for each DMA channel. The page registers provide the upper address bits during a DMA cycle. DMA addresses do no increment or decrement across page boundaries. Page boundaries for the 8-bit channels (channels 0 through 3) are every 64 kilobytes and page boundaries for the 16-bit channels (channels 5, 6, and 7) are every 128 kilobytes. There are a total of 16 8-bit registers and eight 2-bit registers in the extended 612 megacell.

The indexed configuration register ROMDMA is used to program the extended DMA features. In addition to the description below, see the section "Configuration Register Operational Summary" for more information. Bit 7 enables the extended DMA functions. The VL82C386 chip set contains a superset of the PC/AT DMA design which allows full access to the entire 64M range of the VL82C386 chip set. In order to do this, a second 612 memory mapper subset is added to allow access to the two required upper address bits, A24 and A25. When bit 7 = 0, the extended functionality is disabled. Any previously stored values for A24 and A25 are disabled and both bits are forced to 0. This mode is fully compatible with the PC/AT-standard. When bit 7 = 1, the extended mode is enabled. A24 and A25 can be set in the memory mapper page register by setting bit 0 of this register to 1 and writing the data to the same address used for the lower page register byte. Resetting bit 0 to 0 allows access to the lower page registers. See the bit 0 discussion below for more detail. At power-on reset, this bit defaults to 0 for complete AT compatibility.

Bit 6 enables EISA compatibility when set to 1 by allowing access to the upper DMA page address bits at I/O addresses 4XX in accordance with Table 3. When set to 1, it also enables the extended DMA system and allows the contents of the upper page register's A24 and A25 to be used.

Bit 0 allows access to either the lower address bits, A16-A23 of the DMA page register when set to 0 or allows access to the upper address bits A24 and A25 when set to 1. The state of this bit has no effect unless bit 7 of this register has been previously set to 1. As an example, when bit 7 = 1 and bit 0 = 0, a write to address 08Ah will update A16-A23 in the lower DMA page register space. Bit 0 auto-increments on any write to the DMA register space between 0080h and 008Fh. Therefore, if the next operation is a write to 008Ah, the upper address bits A24 and A25 are updated. The next access to this register space automatically accesses the lower byte of that address. Whenever D7 = 0, this bit is reset and held at logic 0. This bit is reset to 0 on POR.

These registers must be written to select the correct page for each DMA channel before any DMA operations are performed. The other address locations between 0080h and 008Fh not shown in Table 4 and are not used by the DMA channels, but can be read or written to by the CPU. Address 008Fh (and 0048Fh) is used to drive a value onto the upper address bits A25-A17 of the CPU's address bus during a refresh cycle.

Important Difference for VL82C286 Chip Set Users

The VL82C286 chip set for use in 286- and 386SX-based systems has a 32 Mbyte limit for its largest memory map.

TABLE 3. DMA PAGE REGISTER ACCESS OPTION 1

A25-A24 Address		A23-A16 Address	DMA Channel
B6=1	B6=0	B6=X	
0487h	NA	0087h	0
0483h	NA	0083h	1
0481h	NA	0081h	2
0482h	NA	0082h	3
048Bh	NA	008Bh	5
0489h	NA	0089h	6
048Ah	NA	008Ah	7
048Fh	NA	008Fh	–REFRESH

TABLE 4. DMA PAGE REGISTER ACCESS OPTION 2

A25-A24 Address	A23-A16 Address	DMA Channel
B0=1, B7=1	B0=0, B7=1	
0087h	0087h	0
0083h	0083h	1
0081h	0081h	2
0082h	0082h	3
008Bh	008Bh	5
0089h	0089h	6
008Ah	008Ah	7
008Fh	008Fh	–REFRESH

However, only the standard DMA operation below 16 Mbytes is supported. When the Bus Controller is strapped for 286/386SX mode via no connect or external pull-up on the (C286) –386DX pin, bits 6 and 7 of the 612AXS indexed register are held low. This disables extended DMA mode. Attempts to write a 1 to these bits via software has no effect and subsequent reads of the bits will return a 0.

Address Generation

The DMA addresses are set up such that there is an upper address portion, used to select a specific page, a middle address portion used to select a block within the page and a lower address portion.

The upper address portion is generated by the page registers, in the 74LS612 equivalent megacell. The page registers for each channel must be set up by the CPU before a DMA operation. DMA addresses do not increment or decrement across page boundaries. Page sizes are 64 kilobytes for 8-bit channels (channels 0 through 3) and 128 kilobytes for 16-bit channels (channels 5, 6 and 7). The DMA page register values are output on A25-A16 for 8-bit channels and A25-A17 for 16-bit channels.

The middle address portion, used to select a block within the page, is generated by the 8237 megacells at the beginning of a DMA operation and any time the DMA address increments or decrements through a block boundary. Block sizes are, 256 bytes for 8-bit channels (channels 0 through 3) and 512 bytes for 16-bit channels (channels 5, 6 and 7). This middle address portion is output by the 8237 megacells onto the internal data bus during state S1. The internal middle address bit latches will latch this value in. The middle address bit latches are output on A15-A8 for 8-bit channels and A16-A9 for 16-bit channels.

The lower address portion is generated directly by the 8237 megacells during DMA operations. The lower address bits are output on A7-A0 for 8-bit channels and A8-A1 for 16-bit channels. A0 and –SBHE are forced low during 16-bit DMA operations. –SBHE is forced to the opposite value of A0 for 8-bit DMA.

–SBHE is configured as an output during all DMA operations and will be driven as the inversion of A0 during 8-bit DMA cycles and forced low for all 16-bit DMA cycles.

Table 5 shows the mapping from the DMA subsystem signals to slot bus signals for both the VL82C386 and VL82C286 chip sets. For the latter chip set, the equivalent signals are also driven onto the local address bus.

TABLE 5. DMA ADDRESSING FOR SLOT BUS ACCESSES

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 8237	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9				
M8				
M7			LA23	LA23
M6			LA22	LA22
M5			LA21	LA21
M4			LA20	LA20
M3			S/LA19	S/LA19
M2			S/LA18	S/LA18
M1			S/LA17	S/LA17
M0			SA16	
	D7		SA15	SA16
	D6		SA14	SA15
	D5		SA13	SA14
	D4		SA12	SA13
	D3		SA11	SA12
	D2		SA10	SA11
	D1		SA9	SA10
	D0		SA8	SA9
		A7	SA7	SA8
		A6	SA6	SA7
		A5	SA5	SA6
		A4	SA4	SA5
		A3	SA3	SA4
		A2	SA2	SA3
		A1	SA1	SA2
		A0	SA0	SA1
		VSS		SA0
		–A0	–SBHE	
		VSS		–SBHE

Table 6 shows the mapping of DMA subsystem signals to local address bus signals for the VL82C386 system.

Ready Control

The ready input to each of the 8237 megacells is driven from the same source within the ready control logic. The Bus Controller ready control logic forces the preprogrammed number of wait states on every DMA transfer. POR defaults to one wait state for both 8- and 16-bit transfers. Other options can be programmed after POR in the indexed configuration register ROMDMA. The external signal IOCHRDY goes into the ready control logic to further extend transfer cycles if needed. To add extra wait states, an external device should pull IOCHRDY low within the setup time before the second phase of the internal DMA clock no later than the last forced wait state cycle. The current DMA cycle will then be extended by inserting wait states until IOCHRDY is returned high. IOCHRDY going high must meet the setup time at the beginning of a wait state cycle or an extra wait state will be inserted before the DMA Controller transitions to state S4.

External Cascading

An external DMA Controller or Bus Master can be attached to an AT-compatible design through the VL82C331's DMA Controllers. To add an external DMA Controller, one of the seven available DMA channels must be programmed in cascade mode. That channels DRQ signal should then be connected to the external DMA Controller's HRQ output. The corresponding –DACK signal for that channel should be connected to the external DMA Controller's HLDA input. When one of the seven channels is programmed in cascade mode and that channel is acknowledged, the Bus Controller will not drive the data bus, the command signals or the address bus.

TABLE 6. DMA ADDRESSING IN 386DX MODE

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 8237	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9			A25	A25
M8			A24	A24
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			A16	
	D7		A15	A16
	D6		A14	A15
	D5		A13	A14
	D4		A12	A13
	D3		A11	A12
	D2		A10	A11
	D1		A9	A10
	D0		A8	A9
		A7	A7	A8
		A6	A6	A7
		A5	A5	A6
		A4	A4	A5
		A3	A3	A4
		A2	A2	A3
		A1	*	A2
		A0	*	**

*Byte Enables –BE0- –BE3 Controlled:

Case	A0	A1	–BE3	–BE2	–BE1	–BE0
1	0	0	High	High	High	Low
2	0	1	High	High	Low	High
3	1	0	High	Low	High	High
4	1	1	Low	High	High	High

**Byte Enables –BE0- –BE3 Controlled:

Case	A0	–BE3	–BE2	–BE1	–BE0
1	0	High	High	Low	Low
2	1	Low	Low	High	High

An external device can become a Bus Master and control the system address, data and command buses in much the same manner. One of the external channels must be programmed in cascade mode. The external device then asserts the DRQ line for that channel. When that channel's –DACK line goes active, the external device can then pull the –MASTER signal low. As in the DMA Controller cascading, the VL82C331 does not drive the address, data and command signals while the cascaded channel's –DACK signal is active.

TABLE 7. DMA ADDRESSING SYSTEM BOARD MEMORY IN 286/386SX MODE

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 8237	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9				
M8				
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			A16	
	D7		A15	A16
	D6		A14	A15
	D5		A13	A14
	D4		A12	A13
	D3		A11	A12
	D2		A10	A11
	D1		A9	A10
	D0		A8	A9
		A7	A7	A8
		A6	A6	A7
		A5	A5	A6
		A4	A4	A5
		A3	A3	A4
		A2	A2	A3
		A1	A1	A2
		A0	A0/–BLE	A1
		VSS		A0/–BLE
		–A0	–BHE	
		VSS		–BHE

Programming DMA Options

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
ROMDMA (81)	ROM Wait States		8 Bit DMA Wait States		16 Bit DMA Wait States		DMA Clk	MEMR Timing

The original PC/AT DMA specification is lacking in the true speed one normally associates with DMA activity. For compatibility, the Bus Controller fully supports that specification as its POR defaults. However, a variety of programmable options are provided in order to enhance DMA performance, if desired. The extended DMA support for 64 Mbyte memory space in the VL82C386 chip set has previously been addressed in the "Page Registers" section. In the following sections, programmable wait state, DMA clock, and –MEMR timing are discussed. Actual programming of the ROMDMA registers in order to effect the desired system performance changes is covered in the "Configuration Register Operational Summary" section.

DMA Wait States
Zero, one, or two wait states can be independently programmed for 8-bit and 16-bit DMA transfers. (Default = one wait state.)

DMA Clock
The DMA clock can be programmed to occur at the normal SYSCLK/2 rate (bit 1 = 0) or at SYSCLK rate (bit 1 = 1). (Default = 0)

–MEMR Delay
To maintain an AT-compatible design, the VL82C331 POR default inserts a one DMA clock cycle delay in the falling edge of the –MEMR signal. –MEMR will go low one DMA clock later than the –MEMR signal coming out of the 8237 megacell. The rising edge is not altered and will go high at the same time the –MEMR signal from the megacell goes high. This maybe reprogrammed to remove this one clock cycle delay on the falling edge of –MEMR by setting bit 0 of ROMDMA to a 1. (Default = 0)

INTERRUPT CONTROLLER SUBSECTION
The interrupt controller subsection is made up of two 8259 megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally on the VL82C331 and two of the interrupt request inputs are connected to internal circuitry. This nominally allows a total of 13 external interrupt requests or 14 when the internal RTC is disabled.

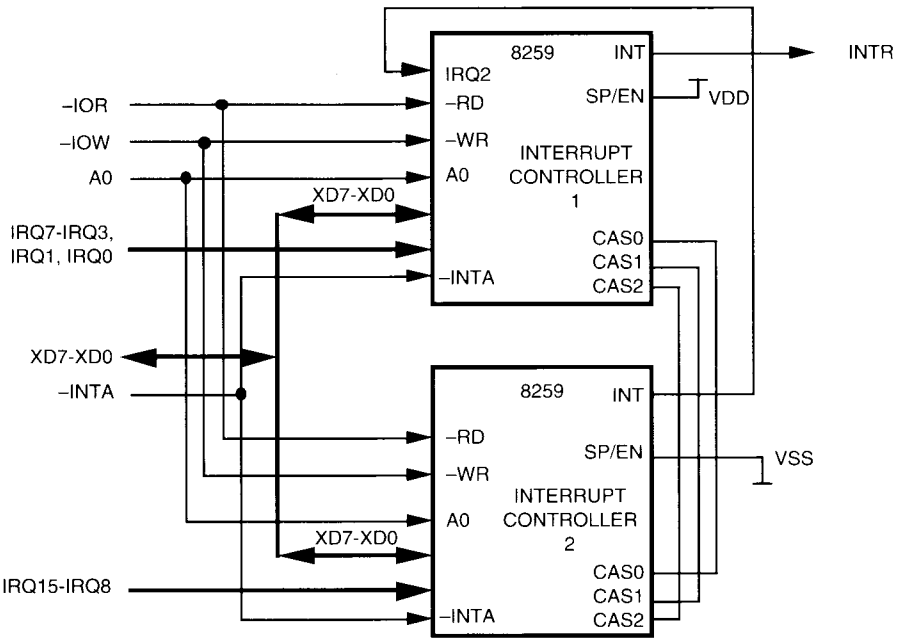
All external interrupt request signals have an internal pull-up resistor to eliminate noise on unconnected request pins.

The following interrupt request signals are different from the standard interrupt request in some way.

IRQ0 This interrupt is connected to the OUT0 of the 8254 megacell and is not available as an external input.

4

FIGURE 2. INTERRUPT CONTROLLER BLOCK DIAGRAM



IRQ2 IRQ2 is used to cascade the two 8259 megacells together and is not available as an external input.

–IRQ8 –IRQ8 input is internally connected to the real-time clock megacell's interrupt pin when bit 6 of configuration register BUSCTL = 0. When BUSCTL6 is set to 1, the Interrupt Controller's –IRQ8 input pin is connected to the VL82C331's pin 117 for connection to the –IRQ pin of an external RTC.

A typical interrupt sequence would be as follows. Any unmasked interrupt will generate the INTR signal to the CPU. The interrupt controller megacells will then respond to the –INTA pulses from the CPU. On the first –INTA cycle the cascading priority is resolved to determine which of the two 8259 megacells will output the interrupt vector onto the data bus. On the second –INTA cycle the appropriate 8259 megacell will drive the data bus with the correct interrupt vector for the highest priority interrupt.

Because the two megacells are cascaded internally on the VL82C331, they should never be programmed to operate in the buffered mode. See the section "ISA Bus Controller/System Controller Interchip Communication" for special use of interrupt control during sleep mode.

TABLE 8. INTERRUPT CONTROLLER WRITE OPERATIONS

INT1	INT2	XD4	XD3	Register Function
0020h	00A0h	1	X	Write ICW1
0021h	00A1h	X	X	Write ICW2
0021h	00A1h	X	X	Write ICW3
0021h	00A1h	X	X	Write ICW4 (if needed)
0021h	00A1h	X	X	Write OCW1
0020h	00A0h	0	0	Write OCW2
0020h	00A0h	0	1	Write OCW3

TABLE 9. INTERRUPT CONTROLLER READ OPERATIONS

INT1	INT2	Register Function
0020h	00A0h	Interrupt Request Register, In-Svc Register or Poll Command
0021h	00A1h	Interrupt Mask Register

Interrupt Controller Registers
The internal registers of the 8259 megacells are written to in the same way as in the standard part. Table 8 shows the correct addressing for each of the 8259 registers.

Before normal operation can begin, each 8259 megacell must follow an initialization sequence. The sequence is started by writing Initialization Command Word 1 (ICW1). After ICW1 has been written, the 8259 megacell expects the next writes to follow in the sequence ICW2, ICW3 and ICW4 if it is needed. The Operation Control Words (OCW) can be written at any time after initialization.

In the standard 8259 megacell, ICW3 is optional. But since the two 8259's in this chip are cascaded together they should always be programmed in cascade mode and ICW3 will always be needed. Refer to the 8259 data sheet for more information on programming the 8259 megacell.

When reading at address 0020h or 00A0h, the register read will depend on how Operation Control Word 3 was set up prior to the read.

COUNTER/TIMER SUBSECTION

The timer subsection consists of one 8254 counter/timer megacell configured as shown in Figure 3. The clocks for each of the three internal counters are tied to the 14.318 MHz oscillator through a divide by 12 counter. The gate inputs of Counters 0 and 1 are tied high to enable those Counters at all times. The gate input of Counter 2 is tied to bit 0 of the Port B register inside the VL82C331.

One of the 8254 megacell counter outputs is directly available at an external pin. Counter 0's output is connected to the IRQ0 input of interrupt controller one. Counter 1's output goes to the pin OUT1. Finally, Counter 2's output goes to an AND gate which drives the output pin SPKR. The other input on this AND gate is connected to bit 1 of the Port B register.

Counter/Timer Registers

The internal registers of the 8254 counter/timer megacell are written to in the same way as in the standard part. Table 10 shows the correct addressing for each of the 8254 registers.

The write control word at address 0043 hex could also be the counter latch command or read back command depending on the values on the data bus. Refer to the 8254 data sheet for more information on programming the 8254 megacell.

FIGURE 3. COUNTER/TIMER BLOCK DIAGRAM

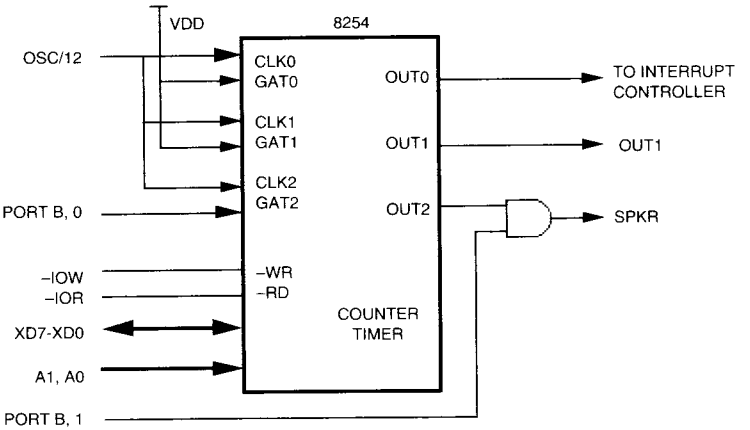


TABLE 10. COUNTER/TIMER ADDRESSING REGISTERS

Addr	–IOR	–IOW	Register Function
0040h	1	0	Write Initial Count to Counter
0040h	0	1	Read Count/Status from Counter 0
0041h	1	0	Write Initial Count to Counter 1
0041h	0	1	Read Count/Status from Counter 1
0042h	1	0	Write Initial Count to Counter 2
0042h	0	1	Read Count/Status from Counter 2
0043h	1	0	Write Control Word
0043h	0	1	No Operation

REAL-TIME CLOCK

The VL82C331 contains VLSI Technology's real-time clock megacell. It is 100% compatible with the 146818A and contains additional battery backed RAM within its address space in order to support non-volatile configuration register storage. Enough storage is provided to store the VL82C331's and System Controller's configuration data. Additional storage is provided in order to support future chip set enhancements and other planned VLSI Technology peripherals.

Real-Time Clock Programmer's Model

The RTC memory consists of ten RAM bytes which contain the time, calendar, and alarm data, four control and status bytes, and 114 general purpose RAM bytes. The address map of the real-time clock is shown in Table 11.

All 128 bytes are directly readable and writeable by the processor program except for the following:

1) Registers C and D are read-only.

2) Bit 7 of Register A is read-only.

This RTC configuration represents an extension to the 146818A architecture. An additional 64 bytes of standby RAM have been added to the RTC memory map. This area provides space to store chip set configuration data and provides ample additional storage in order to support future chip set versions and extra BIOS scratch pad memory.

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the ten time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

Time of Day Register Descriptions

The contents of the time of day registers can be either in binary or BCD format. They are relatively straightforward, but are detailed here for completeness. The address map of these registers is shown in Table 11 and following.

TABLE 11. REAL TIME CLOCK ADDRESS MAP

Hex Addr	Function	Range
00	Seconds (Time)	0-59
01	Seconds (Alarm)	0-59
02	Minutes (Time)	0-59
03	Minutes (Alarm)	0-59
04	Hours (Time)	1-12; 12 Hour Mode
04	Hours (Time)	0-23; 24 Hour Mode
05	Hours (Alarm)	0-23
06	Day of Week	1-7
07	Date of Month	1-31
08	Month	1-12
09	Year	0-99
0A	RTC Register A	(Read/Write)
0B	RTC Register B	(Read/Write)
0C	RTC Register C	(Read-only)
0D	RTC Register D	(Read-only)
0E-7F	User RAM (Standby)	

Address 00 - Seconds:
The range of this register is 0-60 in BCD mode, and 0-3Bh in binary mode.

Address 01 - Seconds Alarm:
The range of this register is 0-60 in BCD mode, and 0-3Bh in binary mode.

Address 02 - Minutes:
The range of this register is 0-60 in BCD mode, and 0-3Bh in binary mode.

Address 03 - Minutes Alarm:
The range of this register is 0-60 in BCD mode, and 0-3Bh in binary mode.

Address 4 - Hours:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01h-0Ch	Binary	AM
81h-8Ch	Binary	PM

Address 05 - Hours Alarm:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01h-0Ch	Binary	AM
81h-8Ch	Binary	PM

Address 06 - Day of Week:
The range of this register is 1-7 in BCD mode, and 1-7h in binary mode.

Address 07 - Date:
The range of this register is 1-31 in BCD mode, and 1-1Fh in binary mode.

Address 08 - Month:
The range of this register is 1-12 in BCD mode, and 1-0Ch in binary mode.

Address 09 - Year:
The range of this register is 0-99 in BCD mode, and 0-63h in binary mode.

RTC Control Register Descriptions
The RTC megacell has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Hex Addr	Function	Type
0A	RTC Register A	R/W
0B	RTC Register B	R/W
0C	RTC Register C	R-O
0D	RTC Register D	R-O
0E-7F	User RAM (Standby)	R/W

Register A Description
This register contains control bits for the selection of periodic interrupt, input divisor, and the update in progress status bit. The bits in the register are defined as follows:

Bit	Description	Abbr
0	Rate Select Bit 0	RS0
1	Rate Select Bit 1	RS1
2	Rate Select Bit 2	RS2
3	Rate Select Bit 3	RS3
4	Divisor Bit 0	DV0
5	Divisor Bit 1	DV1
6	Divisor Bit 2	DV2
7	Update in Progress	UIP

Bits 3-0 - The four rate selection bits (RS3 to RS0) select one of 15 taps on the 15-stage divider, or disable the divider output. The tap selected may be used to generate a periodic interrupt. These four bits are read/write bits which are not affected by RESET. The periodic interrupt rate that results from the selection of various tap values is as follows:

RS Value	Periodic Interrupt Rate
00	None
01	3.90625 ms
02	7.8125 ms
03	122.070 µs
04	244.141 µs
05	488.281 µs
06	976.562 µs
07	1.953125 ms
08	3.90625 ms
09	7.8125 ms
0Ah	15.625 ms
0Bh	31.25 ms
0Ch	62.5 ms
0Dh	125 ms
0Eh	250 ms
0Fh	500 ms

Bits 6-4 - The three divisor selection bits (DV2-DV0) are fixed to provide for only a 15-stage divider chain, which would be used with a 32 KHz external crystal. Only bit 6 of this register can be changed allowing control of the reset for the divisor chain. When the divider reset is removed, the first update cycle begins one-half second later. These bits are not affected by power-on reset (external pin).

DV Value	Condition
2	Operation Mode, Divider Running
6	Reset Mode, Divider in Reset State

Bit 7 - The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a 1, the update cycle is in progress or will soon begin. When UIP is a 0, the update cycle is not in progress and will not be for at least 244 µs. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is 0. The UIP bit is a read-only bit, and is not affected by RESET. Writing the SET bit in register B to a 1 will inhibit any update cycle and then clear the UIP status bit.

Register B Description
Register B contains command bits to control various modes of operations and interrupt enables for the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Daylight Savings Enable	DSE
1	24/12 Mode	24/12
2	Data Mode (Binary or BCD)	DM
3	Not Used	
4	Update End Interrupt Enable	UIE
5	Alarm Interrupt Enable	AIE
6	Periodic Interrupt Enable	PIE
7	Set Command	SET

Bit 0 - The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is 1). On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is 0. DSE is not changed by any internal operations or reset.

Bit 1 - The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (1) or the 12-hour mode (0). This is a read/write bit, which is affected only by software.

Bit 2 - The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or reset. A 1 in DM signifies binary data, while a 0 signifies BCD data.

Bit 3 - This bit is unused.

Bit 4 - The UIE (update end interrupt enable) bit is a read/write bit which enables the update-end flag (UF) bit in Register C to assert an IRQ. The RESET pin being asserted or the SET bit going high, clears the UIE bit.

Bit 5 - The alarm interrupt enable (AIE) bit is a read/write bit which when set to a 1 permits the alarm flag (AF) bit in register C to assert an IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including "don't care" alarm code of 11XXXXXXb). When the AIE bit is a 0, the AF bit does not initiate an IRQ signal. The RESET pin clears AIE to 0. The internal functions do not affect the AIE bit.

Bit 6 - The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic interrupt flag (PF) bit in register C to cause the IRQ pin to be driven low. A program writes a 1 to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in register A. A 0 in PIE blocks IRQ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by an internal functions, but is cleared to 0 by a reset.

Bit 7 - When the SET bit is a 0, the update cycle functions normally be advancing the counts once-per-second. When the SET bit is written to a 1, any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. Also, all time and calendar bytes should be initialized when the SET bit is written to a 1. SET is a read/write bit which is not modified by reset or internal functions.

Register C Description

Register C contains status information about interrupts and internal operation of the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Not Used, Read as 0	
1	Not Used, Read as 0	
2	Not Used, Read as 0	
3	Not Used, Read as 0	
4	Update Ended Flag	UF
5	Alarm Interrupt Flag	AF
6	Periodic Interrupt Flag	PF
7	IRQ Pending Flag	IRQF

Bits 3-0 - The unused bits of status Register C are read as 0's and can not be written.

Bit 4 - The update ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a 1, the 1 in UF causes the IRQF bit to be a 1, asserting the IRQ. UF is cleared by a Register C read or a reset.

Bit 5 - A 1 in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A 1 in the AF causes the IRQ pin to go low, and a 1 to appear in the IRQF bit, when the AIE bit also is a 1. A reset or a read of Register C clears AF.

Bit 6 - The periodic interrupt flag (PF) is a read-only bit which is set to a 1 when a particular edge is detected on the selected tap of the divider chain. The RS3-RS0 bits establish the periodic rate. PF is set to a 1 independent of the state of the PIE bit. PF being a 1 initiates an IRQ signal and sets the IRQF bit when PIE is also a 1. The PF bit is cleared by a reset or a software read of Register C.

Bit 7 - The interrupt request flag (IRQF) is set to a 1 when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

The logic can be expressed in equation form as:

IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a 1, the IRQ pin is asserted. All flag bits are cleared after Register C is read by the program or when the RESET pin is asserted.

Register D Description

This register contains a bit that indicates the status of the on-chip standby RAM. The contents of the registers are described as the following:

Bit	Description	Abbr
0	Not Used, Read as 0	
1	Not Used, Read as 0	
2	Not Used, Read as 0	
3	Not Used, Read as 0	
4	Not Used, Read as 0	
5	Not Used, Read as 0	
6	Not Used, Read as 0	
7	Valid RAM Data and Time	VRT

Bits 6-0 - The remaining bits of Register D are unused. They cannot be written, but are always read as 0's.

Bit 7 - When = 0, the time and RTC CMOS RAM contents are invalid.

CMOS Standby RAM Description

The 114 general purpose RAM bytes are not dedicated to RTC use within the RTC. They are fully available during the update cycle.

General Operational Notes

Set Operation:
Before initializing the internal registers, the SET bit in Register B should be set to a 1 to prevent time/calendar updates from occurring. The program initializes the ten locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All ten time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized, the RTC makes all updates in the selected data mode. The data mode can not be changed without reinitializing the ten data bytes.

BCD VS Binary Format:
The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high order bit of the hours byte represents PM when it is a 1.

Update Operation:
The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the ten bytes are switched to the update logic

to be advanced by one second and to check for an alarm condition. If any of the ten bytes are read at this time, the data outputs are undefined. The update lockout time is 1948 µs for the 32.768 KHz time base. The update cycle section shows how to accommodate the update cycle in the processor program.

Alarm Operation:
The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is in any byte from C0h to FFh. An alarm interrupt each hour is created with "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Interrupts:
The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from one-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 µs. The update ended interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A 0 in the interrupt enable bit prohibits the IRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enable, the IRQ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to a 1 in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

Divider Control
The divider control bits are fixed for only 32.768 KHz operation. The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one-half second later. The divider control bits are also used to facilitate testing the RTC.

Periodic Interrupt Selection
The periodic interrupt allows the IRQ pin to be triggered from once every 500 ms to once every 30.517 µs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Update Cycle
The RTC executes an update cycle one-per-second, assuming one of the proper time bases is in place, the DV2-DV0 divider is not clear, and the SET bit in Register B is clear. The SET bit in the 1 state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the second byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 32.768 KHz time base update cycle takes 1984 µs, during which, the time, calendar, and alarm bytes are not accessible by the processor program, protecting the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be undefined. The update is progress (UIP) status bit is set during the interval. Three methods of accommodating non-availablity during update are usable by the program. In discussing the three methods, it is assumed that at random points, user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update in progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. After the UIP bit goes high, the update cycle begins 244 µs later. Therefore, if a low is a read in the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. If a 1 is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C.

To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the roll-over will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

Power-down Mode
The passive components that are critical for low power operation are shown in the Figure 4.

In Figure 4, the POWERGOOD signal from the power supply is used to control the power-down mode of the RTC.

When POWERGOOD is low, the RTC enters power-down mode. In this mode, all outputs are three-stated and read or write operations are inhibited. Any operation in progress (address entered but the data not yet accessed) is terminated and must restart from the

beginning of the bus cycle for proper operation. A write operation in progress is aborted and the data path is double buffered to prevent data corruption. The Power Sense signal is used to reset the state of the Valid RAM and Time (VRT) bit and to clear all internal RAM. This input must be asserted after power is applied to the RTC to set the state of the VRT bit properly.

With a power consumption target specification of 5 µA, and a lithium battery with a capacity of 100 mA-Hr, time will be properly kept for approximately 2.25 years.

Disabling Internal RTC

The fully compatible internal real-time clock saves the designer money and board space versus use of an external RTC. However, sometimes a stand-alone RTC is preferred. To allow this option, the internal RTC may be disabled by setting bit 6 of the configuration register BUSCTL to a logic 1. In this mode, the PS/–RCLR/–IRQ8 pin becomes the –IRQ8 input. This routes the external RTC's interrupt signal through an internal inverter to the IRQ8 input of the VL82C331's interrupt service logic. When the internal RTC is disabled by setting BUSCTL6 = 1, the VL82C331's –CS8042/–RTC output also becomes active during RTC I/O address decodes to 70h or 71h. The system designer must externally generate the required three signals for an external RTC;

- RTCAS,
- RTCDS, and
- RTCRW.

If a stand-alone Keyboard Controller is used, the –CS8042/–RTC signal must also be decoded from the VL82C331's composite chip select output. These external decodes can easily be performed using the 74HC139.

BUS CONTROLLER REFRESH SUBSYSTEM

The System Controller performs on-board DRAM refresh and controls both on- and off-board refresh timing in all modes. The VL82C331 actually performs the off-board refresh when commanded by the System Controller. Refresh may be performed in a coupled or decoupled mode. In coupled mode, refresh timing for both system board and slot bus refreshes is performed in a synchronous manner. In decoupled mode, the VL82C330 has complete control over the timing of on-board DRAM refresh and and off-board refresh but the timing of each is independent. Note: The VL82C320 does not support decoupled refresh mode. See the section "System Board DRAM Refresh" in the VL82C320 or VL82C330 data sheet for more information.

PORT B AND NMI LOGIC

The Bus Controller generates the Non-Maskable Interrupt (NMI) output pin for the CPU. NMI is enabled by a write to I/O address 0070h with D7 low. Once enabled, an NMI can be generated by the IOCHCK input going low or the –PARERROR input going low. Each of these NMI sources has an enable bit in the Port B register to allow these inputs to cause an NMI when set high, or ignore the input if the bit is low.

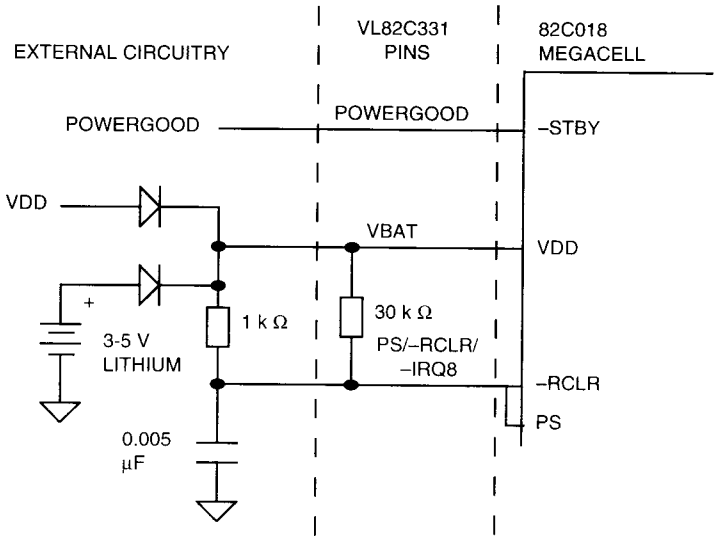
The Port B register at I/O address 0061 hex is included in the Bus Controller chip. This register contains bits to control the speaker output and NMI circuitry. Bits 3-0 are read/write bits, while bits 7-4 are read-only. Each bit of the register is defined below. Bits 3-0 are all set low by a reset.

Port B, 0 Speaker Timer 2 Gate (TIM2GAT_SPK). This bit goes to the gate 2 input on the 8254 megacell to enable Counter 2 to produce a speaker frequency.

Port B, 1 Speaker Data (SPK_DAT). This bit is gated with the output of Counter 2 from the 8254 megacell. When this bit is high, it allows the OUT2 frequency to be passed out on the SPKR pin. When this bit is low, the SPKR output is forced low.

Port B, 2 Enable RAM Parity Check (–ENA_RAM_PCK). When this bit is set low, it allows parity errors from the on-board RAM memory to cause an NMI. When high, on-board RAM parity errors will not cause an NMI.

FIGURE 4. RTC LOW POWER OPERATION CIRCUIT



Port B, 3 Enable I/O Check (–ENA_IO_CK). When this bit is set low, it allows an NMI to be generated if the IOCHCK input is pulled low. Otherwise, the IOCHCK input is ignored and can not generate an NMI.

Port B, 4 Refresh Detect (REFDET). This bit is tied to a toggle flip-flop which is clocked by OUT1. It will toggle to the opposite state every time an OUT1 pulse occurs.

Port B, 5 Timer Output bit 2 state (OUT2). This bit indicates the current state of the OUT2 signal from the 8254 megacell.

Port B, 6 Channel Check (CHAN_CHK). This bit indicates that a peripheral device is reporting an error. It can only be set if –ENA_IO_CK is set low. IOCHERR should be cleared by writing a high to ENA_IO_CK.

Port B, 7 Parity Check (PCK). This bit indicates that an on-board RAM parity error has occurred. It can only be set if –ENA_RAM_PCK is set 0. –PCK should be cleared by writing a 1 to –ENA_RAM_PCK.

ISA BUS INTERFACE SUBSECTION

The VL82C331 ISA Bus Interface can be controlled from four possible sources. Three of these sources are generated in the Bus Controller chip. They are CPU mode, DMA mode, and refresh mode. The fourth possible source is a Bus Master.

In CPU mode, the Bus Controller receives bus cycle commands from the System Controller, executes them and responds back to the System Controller when the bus cycle is complete. When in this mode, the 288 megacell is responsible for generating the command (–IOR, –IOW, –MEMR, –MEMW, –SMEMR, and –SMEMW) signals, BALE and the timing for when the SA bus will be valid. The Bus Controller samples the inputs –MEMCS16, –IOCS16, IOCHRDY, and –WS0 and combines these with internally defined definitions to determine the length in wait states of each bus cycle.

Refresh modes are initiated as described above. During refresh the Bus Controller will drive the –REFRESH signal, a refresh address and –MEMR command onto the bus to implement the refresh cycle. The refresh circuit samples IOCHRDY to determine if the –MEMR and –REFRESH pulses need to be extended. The outputs AEN and BALE are both driven high during the refresh cycles.

In DMA mode, the Bus Controller is driven from one of the 8237 DMA Controller megacells. The DMA Controllers generate the command and address signals. BALE is forced high for all DMA cycles. The Bus Controller asserts the AEN signal to indicate that the current address on the bus is for memory only and not to be decoded as an I/O address. The DMA section samples IOCHRDY to extend bus cycles longer than the internally defined cycle length.

Bus Master mode is an extension of DMA mode. A Master can get control of the bus by requesting a DMA operation. Once the DMA is acknowledged, the –MASTER signal is pulled active and the Bus Controller relinquishes control of the bus to the Master. While in master mode, the Bus Controller buffers the address lines and drives them onto the local address bus (A bus) to be used to address on-board memory.

A Bus Master can perform a refresh by releasing the bus, then asserting –REFRESH. The VL82C331 will drive the refresh address and –MEMR as described above.

Extended Slot Bus Timing Options

Data Port 00EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
BUSCTL (84)	1	RTC Ctrl	1	1	ADDLY	RLX Timing	16 WS	8 WS

Four bus control options are provided and are programmable via the indexed BUSCTL register. On reset, the four control bits are reset to 0. This specifies the full PC/AT compatibility mode.

When bit 0 = 1, an extra wait state is added for 8-bit slot bus accesses. This yields five rather than the normal four wait states. This allows slower boards to operate with equivalent performance when higher bus speeds are used.

When bit 1 = 1, an extra wait state is added for 16-bit slot bus accesses. This yields two instead of the normal one for I/O accesses and one instead of zero for memory accesses.

When bit 2 = 1, an extra command delay is added for 16-bit memory cycles.

When bit 3 = 1, an extra command delay is added for 8- and 16-bit I/O cycles and for 8-bit memory cycles.

Note: Zero wait state is possible on extremely fast boards that can pull the 0WS line fast enough and more than five wait states are possible if IOCHRDY is pulled low before the last normal wait state. However, –MEMCS16 or –IOCS16 must be pulled low before the last normal wait state even if IOCHRDY has previously been activated.

ROM ACCESS CONTROL SUBSECTION

Data Port 00EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
ROMDMA (81)	ROM Wait States		8-Bit DMA Wait States		16-Bit DMA Wait States		DMA Clock	MEMR Timing

Bits 6 and 7 of the ROMDMA configuration register allow programming the number of slot bus wait states for BIOS ROM accesses. Range is from one to three wait states. The POR default is three wait states. Shadow RAM features of the Sytem Controller are recommended to speed BIOS access. ROM decode logic in the Bus Controller provides a single ROM chip select for this BIOS region. A chip select also results from decode of the middle BIOS address space between FE0000h and FFFFFFh and also the upper BIOS space from FFFE0000h to FFFFFFFFh.

ISA BUS CONTROLLER/SYSTEM CONTROLLER INTERCHIP COMMUNICATION

The asynchronous interface to the Bus Controller is handled by a group of signals from the System Controller. –CHS0, –CHS1 and CHM/–IO define which type of cycle is to be executed as follows:

CHM/–IO	–CHS1	–CHS0	Bus Cycle
0	0	0	–INTA
0	0	1	–IOR
0	1	0	–IOW
0	1	1	Reserved
1	0	0	–REFRESH
1	0	1	–MEMR
1	1	0	–MEMW
1	1	1	Reserved

POWER SAVING SLEEP MODE

Data Port 00EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
SLEEP	Enable	1	1	1	1	1	1	SYSCLK

Bit 7 of the sleep register is set to 1 in order to enable sleep function. It is write-only at indexed register port 13h because it duplicates the address and bit position of the sleep enable function in the System Controller. (For test purposes, the Bus Controller register can be read and written at indexed location 83h.) The Bus Controller sleep mode features work together with System Controller sleep features to provide a low power system idle state for extension of battery life in portable systems. When activated by the CPU via an I/O write to bit 7 of the sleep register, the the interrupt controllers and the timers continue to operate. When an interrupt occurs due to an external source or internal Timer 0, the Bus Controller passes it to the CPU. The CPU then resets bit 7 of the sleep register. This brings both the System Controller and the Bus Controller out of the sleep state.

Setting bit 0 = 0 disables the SYSCLK oscillator (BUSCLK/2) if bit 7 is set to 1. Returning bit 7 to 0 re-enables the oscillator signal. If bit 0 = 1, the oscillator is always enabled even in sleep mode.

In operation, bit 0 is set for the desired operational mode by the BIOS on power-up. Bit 7 is then controlled as required to jump in and out of sleep mode during operation.

IN-CIRCUIT TEST LOGIC

During In-Circuit Test (ICT) all of the outputs can be toggled by one or more inputs. This allows for a board level tester to test the solder connections for each signal pin.

The sequence for enabling ICT is as follows:

1) Tester drives POWERGOOD high, then pulses the BUSCLK input at least two times. Maintain POWERGOOD high while in ICT mode.
2) Tester drives –TRI signal low.
3) Tester drives the XD bus to FFh.
4) Tester pulses –IOR and –IOW low for 100 ns (minimum).
5) Tester drives –TRI signal high. (ICT input to output mapping now active.) Maintain –TRI high while in ICT mode.

There are two ways to disable ICT:

1) Drive POWERGOOD low, then pulse BUSCLK at least two times.
2) Repeat steps 2-5 with the XD bus = 00h rather than with FFh in step #3.

The only pins not included in the ICT input to output mappings are:

- VSS pins which must all be grounded.
- VDD pins which must all be 5 V ±5%.
- POWERGOOD and –ICT which have other dedicated functions in ICT mode.

XD7-0, –IOR, and –IOW are used to enter and exit ICT mode. However, they are included in the input to output mapping scheme while ICT is active.

IN-CIRCUIT TEST DESCRIPTION

ICT INPUT		ICT OUTPUT	
Signal Name	Pin #	Signal Name	Pin #
SA6	1	–DACK2	2
SA5	3	T/C	4
SA4	5	BALE	6
SA3	7	SA2	8
OSC	9	SA1	11
–MEMCS16	13	SA0	12
–IOCS16	15	–SBHE	14
IRQ10	17	LA23	16
IRQ11	21	LA22	18
IRQ12	23	LA21	22
IRQ15	25	LA20	24
IRQ14	27	LA19	26
LA18	28	–DACK0	29
DRQ0	32	LA17	31
–MEMR	33	–DACK5	34
DRQ5	36	–MEMW	35
DRQ6	38	–DACK6	37
DRQ7	41	–DACK7	39
MASTER	42	A25	43
A23	45	A24	44
A22	46	A21	47
A20	48	A19	49
A18	50	A17	51
A16	52	A15	53
A14	54	A13	55
A12	56	A11	57
A10	58	A9	61
A8	62	A7	63
A6	64	A5	65
A4	66	A3	67
A2	68	–BE3	69
–BE2 (A1)	70	–BE1 (–BHE)	71
(C286) –386DX	73	–BE0 (A0)	72
HLDA +	74	INTR	75

ICT INPUT		ICT OUTPUT	
Signal Name	Pin #	Signal Name	Pin #
–CHS0/–MW	77	NMI	76
–CHS1/–MR	78	CHM/–IO *	82
XD4	95	–EALE U	83
–BLKA20	87	–BRDRAM *	84
BUSCLK	86	–CHREADY	85
XD5	94	DMAHLDA *	88
XD6	92	DMAHRQ	89
XD7	91	OUT1	90
XD3	96	–LATLO	104
XD2	97	–XDREAD	103
XD1	98	SDHL/–HL	102
XD0	99	–SDSWAP	101
–PCK	111	–LATHI	105
IRQ13	110	SPKR	107
IRQ1	109	–CS8042	108
–ROM8	112	–DACK1	142
–HIDRIVE	113	SA16	137
PS/–RCLR/–IRQ8	117	SA18	133
–IOCHK	121	RSTDRV	122
IRQ9	123	SA19	131
DRQ2	124	–SMEMR	129
–WS0	125	AEN	128
IOCHDY	126	–SMEMW	127
–IOW	132	–DACK3	136
–IOR	134	SA17	135
DRQ3	138	SA15	141
DRQ1	144	SA14	143
–REFRESH	146	SA13	145
SA12	147	SYSCLK	148
IRQ7	151	SA11	149
IRQ6	153	SA10	152
IRQ5	155	SA9	154
IRQ4	157	SA8	156
IRQ3	159	SA7	158

+ Keep the HLDA input low during ICT mode. Otherwise, the –CHS0/–MW and –CHS1/–MR inputs will become outputs and cause contention problems with the In-Circuit Tester. This comment pertains only to ICT mode.

***CAUTIONARY NOTE:** These signals are normally outputs but are mapped as inputs during ICT. Board design must take this into account if In-Circuit mode is used.

CONFIGURATION REGISTER ACCESS

CONFIGURATION ENABLE/DISABLE REGISTERS (I/O Addresses 00FBh and 00F9h)

00FBh	D7	D6	D5	D4	D3	D2	D1	D0
ENABLE	X	X	X	X	X	X	X	X

00F9h	D7	D6	D5	D4	D3	D2	D1	D0
DISABLE	X	X	X	X	X	X	X	X

When enabled and used as described below, the configuration registers are protected from unauthorized accesses that might garble the system configuration and either crash the system or change its operational characteristics in an unwanted manner. A write to 00FBh enables the configuration registers. A write to 00F9h disables the configuration registers. When disabled, the system is locked out from any access to the configuration and control ports from address 00E8h through 00EFh. This includes the indexed configuration registers described in the "Index Register" section.

If MISCSET=1, the configuration enable/disable feature is disabled. See the description under MISCET in the "Data Port Register" section.

A read operation on 00F9h or 00FBh will not cause the VL82C331 to drive the XD bus.

CONFIGURATION REGISTER OPERATIONAL SUMMARY

Table 13 at end of this section shows a mapping of the VL82C331 ISA Bus Controller indexed configuration registers. These registers are accessed through a single port address as described in the "Index Register" section that follows.

Other configuration register sets exist in the Bus Controller. The DMA Controllers, Interrupt Controllers, and Counter/Timers have separate I/O registers at the PC/AT-compatible locations.

Index Register (00ECh) (Write-Only)
The value written to this register is the 8-bit address of the data port which is accessed through the data port register at I/O address 00EDh. All subsequent data port reads and writes will access the register at this address until the index register is written with a new 8-bit address. This register is write-only. The index register and data port register, described below, share common addresses with the index and data port registers located in the System Controller. A write to the index register at 00ECh is latched into both the System Controller and Bus Controller. Only the System Controller index register is readable in order to avoid bus collisions.

Data Port Register (I/O Address 00EDh)
Each register accessible through I/O address 00EDh is functionally described next. It is accessed first by writing its address to the index register at I/O address 00ECh, then by accessing the data port at I/O address 00EDh. All data ports in the Bus Controller are located in the range 80h to FFh to avoid contention with data ports located in the System Controller. However, there is one exception. See the section "Sleep Register" for details.

Version (80h) (Read-Only) (Default = F4h)
D2-D7 will contain a code which indicates that this part is a VLSI Technology, Inc., PC/AT-compatible ISA Bus Controller. D0 and D1 contain the version number of this chip. By using this byte, a smart BIOS can compensate for "feature" differences based on the version number. The code 00F4h is used in the initial version of this chip. By breaking the code in two bit pieces, it is revealed to be "331" Rev. "0."

ROMDMA (81h) (Default = FCh)
Bits 7-6 indicate the number of ROM wait states. These wait states are timed in slot bus cycles. The valid range is 1 to 3.
00 = 3 wait states
01 = 1 wait state
10 = 2 wait states
11 = 3 wait states (Default)

Bits 5-4 are encoded with the number of clocks the command is active for 8-bit DMA cycles:
00 = 2 DMA clocks
01 = 4 DMA clocks
10 = 3 DMA clocks
11 = 3 DMA clocks (Default)

Bits 3-2 are encoded with the number of 1 clocks the command is active for 16-bit DMA cycles:
00 = 2 DMA clocks
01 = 4 DMA clocks
10 = 3 DMA clocks
11 = 3 DMA clocks (Default)

Bit 1 = 1 for DMA clock = SYSCLK. Bit 1 = 0 for SYSCLK/2. (Default = 0.)

Bit 0 specifies the delay for the –DMAMEMR signal. When bit 0 = 0, –DMAMEMR is active at the same time as in the original PC/AT design. This is the default case. When bit 0 = 1, the falling edge of –DMAMEMR occurs one DMACLK earlier. In this latter case, the –DMAMEMR timing during a memory to I/O DMA cycle is the same as that of the –IOR signal during an I/O to memory DMA cycle. (Default = 0.)

612AXS (82h) (Default = 3Eh)
Bit 7 enables the extended DMA functions when set to 1 by allowing access to the two required upper address bits, A24 and A25. When bit 7 = 0, the extended functionality is disabled. Any previously stored values for A24 and A25 are disabled and both bits are forced to 0. This latter mode is fully compatible with the PC/AT-standard. When bit 7 = 1, the extended mode is enabled. A24 and A25 can be set in the memory mapper page register by setting bit 0 of this register to 1 and writing the data to the same address used for the lower page register byte. Resetting bit 0 to 0 allows access to the lower page registers. See the bit 0 discussion below for more detail. (Default = 0.)

Bit 6 enables EISA I/O access compatibility when set to 1 by allowing access to the upper DMA page address bits at I/O addresses 4XX where XX = the same address as the lower page register byte. When set to 1, it also enables the extended DMA system and allows the contents of the upper page register's A24 and A25 to be used. (Default = 0.)

Note - When the external 286/–386 pin is not tied to ground, bits 6 and 7 are held low disabling the extended DMA mode. Attempts by software to write logic 1's to these bits has no effect and subsequent reads will return 0. The extended DMA function is not supported when the VL82C331 ISA Bus Controller is used with the VL82C320 System Controller in 286- or 386SX-based systems.

Bit 0 allows access via the same I/O addresses to the lower address bits, A16-A23 of the DMA page register when set to 0 or to the upper address bits A24 and A25 when set to 1. The state of this bit has no effect unless bit 7 of this register has been previously set to 1. (Default = 0.)

Sleep (13h) (Write-only)
SLPTST (83h) Read/Write for Factory or Post Test) (Default = 7Fh)
This special case register overlays the sleep register at the same indexed register location as in the VL82C320 and VL82C330 System Controllers. D7 and D0 are the only active bits in the ISA Bus Controller. In standard operation, a read of indexed register 13h will return the register's contents as last written and latched into the VL82C330. For test purposes, the Bus Controller sleep register can be read and written at indexed location 83h. In normal operation, however, all reads and writes should be performed through indexed register 13h.

Bit 7- Power-down enable
0 = Default setting. Normal PC/AT-compatible operation
1 = DMA clock disabled. Bus Quiet mode active. SYSCLK stopped is bit 0 = 0.

This bit is reset to 0 and normal operation resumes when rewritten or when a hardware reset of the Bus Controller occurs.

Bit 0 can be used to disable the SYSCLK signal to the slot bus. When set to 0 and bit 7 is set to 1, the SYSCLK signal is shut down until bit 7 is reset to 0. If bit 0 = 1, SYSCLK is enabled to the slot bus regardless of the state of bit 7. (Default = 1.)

BUSCTL (84h) (Default = B0h)
Bit 6 allows the internal RTC to be disabled if use of an external RTC is preferred. Bit 6 = 1 disables the internal RTC and redefines the PS/–RCLR/ –IRQ8 pin as –IRQ8 in. Default = 0, internal RTC is operational.

Bit 4 selects between the standard IRQx input functionality and the sampled IRQ mode. The latter feature was added to reduce the chance for noise to generate spurious interrupts. When set to logic 1, the 14.318 MHz oscillator is used to sample each IRQ input. An IRQ input must remain high from the rising edge of the 14.318 MHz clock through the next falling edge in order to be passed through to the 8259 Interrupt Controllers. The default value of 1 selects this mode. A value of 0 removes the sampling circuitry and passes the IRQx inputs directly to the 8259s.

Bit 3 allows addition of one extra command delay for 8- and 16-bit I/O cycles and for 8-bit memory cycles. (Default = 0, no added command delays.)

Bit 2 determines whether to use the PC/AT-compatible zero command delays on 16-bit memory cycles or whether to add one. (Default = 0, no command delays on 16-bit memory cycles.)

Bit 1 determines whether to use zero or one wait states for 16-bit slot bus accesses. When bit 1 = 0, the PC/AT-compatible zero wait states are used. When set to 1, one wait state is used to allow robust operation of add-in cards at faster slot speeds. (Default = 0, zero wait states on 16 slot bus accesses.)

Bit 0 determines whether to use four or five wait states for 8-bit slot bus accesses. When bit 1 = 0, the PC/AT-compatible four wait states are used. When set to 1, five wait states are used to allow robust operation of add-in cards at faster slot speeds. (Default = 0; four wait states on 8-bit slot bus accesses.)

MISCSET (14h) (Write-only)
Bit 7 is used to enable or disable the SF options mapped into the coprocessor chip set I/O space between F0h and FFh. This register is used to monitor writes to MISCSET7 in the VL82C330 System Controller. When monitored in conjunction with writes to FBh and F9h, the VL82C331 can enable or disable access to these configuration registers. This is described in more detail in the "Detailed Internal Control Register" section. 0 = enabled, 1 = disabled. (Default = 0)

RAMMAP (03h) (Write-only)
Bit 7 determines Bus Controller response to memory accesses between E0000h-EFFFFh and FE0000h-FEFFFFh. When set to a logic 1, a ROM access is performed for read cycles. When set to logic 0, slot bus accesses is performed for read cycles. In either case, write cycles are performed to the slot bus. This feature allows systems not using a 128K BIOS to access memory devices on the slot bus in these two areas. (Default = 1)

All other bits at data port 03h in the VL82C331 are inactive. See the definition of REGTEST (85h) that follows.

REFCTL (06h) (Write-only)
Bit 3 controls internal I/O decode. When set to 0, full 16-bit decode is performed. When set to 1, 10-bit decode is performed. The latter option provides less system flexibility but is compatible with the original PC design. This function has been restructured since the latest published specification such that a write to this single bit control both VL82C331 and Bus Controller I/O decodes. This prevents the possibility of having one component in 16-bit mode and the other in 10-bit mode. (Default = 0)

All other bits at data port 06h in the VL82C331 are inactive. An attempted read of this location will not cause the bus to be driven by the VL82C331. The System Controller will drive the bus. See the definition of REGTEST (85h) below.

REGTEST (85h) This register is intended for test purposes only. (Default = 77h)
Bit 7 is the same as MISCSET7 at data port 14h. A write to REGTEST7 is the same as a write to bit 7 of data port 14h in the VL82C331. However, this bit can also be read at REGTEST7. This allows testing of this bit at this data port address something not possible at data port 14h since the bit is write-only at that address.

Bit 6 is the same as RAMMAP7 at data port 03h. A write to REGTEST6 is the same as a write to bit 7 of data port 03h in the VL82C331. However, this bit can also be read at REGTEST6. This allows testing of this bit at this data port address; something not possible at data port 03h since the bit is write-only at that address.

Bit 3 is the same as REFCTL3 at data port 06h. A write to REGTEST3 is the same as a write to bit 3 of data port 06h in the VL82C331. However, this bit can also be read at REGTEST3. This allows testing of this bit at this data port address, something not possible at data port 06h since the bit is write-only at that address.

TABLE 13. ISA BUS CONTROLLER CONFIGURATION REGISTER MAP

Index Port		D7	D6	D5	D4	D3	D2	D1	D0
00ECh (W-O)		A7	A6	A5	A4	A3	A2	A1	A0
Data Port 00EDh		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
80	VER (R-O)	1	1	1	1	0	1	0	0
81	ROMDMA (R/W)	ROM Wait States		8-Bit DMA Wait States		16-Bit DMA Wait States		DMA Clock	MEMR Time
82	612AXS (R/W)	Enable FF	4XX Enable	1	1	1	1	1	FF PTR
13	SLEEP (W/O)	Enable	1	1	1	1	1	1	SYSCLK
83	SLPTST (R/W)	ENABLE	1	1	1	1	1	1	SYSCLK
84	BUSCTL (R/W)	1	RTC Ctrl	1	SAMPINT	ADDLY	RLX Timing	16 WS	8 WS
14	MISCSET (W/O)	FX Enable	–	–	–	–	–	–	–
03	RAMMAP (W/O)	ROMSLOT	–	–	–	–	–	–	–
06	REFCLT (W/O)	–	–	–	–	10/16 IO	–	–	–
85	REGTEST (R/W)	FX Enable	ROMSLOT	1	1	10/16 IO	1	1	1

Note: A "1" indicates reserved register bits that read back as logic 1.
Registers containing bits with a "–" are write-only registers. The bus will not be driven during a read.

TABLE 14. CONFIGURATION REGISTER DEFAULTS ON RESET

Data Port 00EDh		D7	D6	D5	D4	D3	D2	D1	D0
80	VER (R-O)	1R	1R	1R	1R	0R	1R	0R	0R
81	ROMDMA (R/W)	1	1	1	1	1	1	0	0
82	612AXS (R/W)	0	0	1R	1R	1R	1R	1R	0
13	SLEEP (W/O)	0*	–	–	–	–	–	–	1*
83	SLPTST (R/W)	0*	1R	1R	1R	1R	1R	1R	1*
84	BUSCTL (R/W)	1R	0	1R	1	0	0	0	0
14	MISCSET (W/O)	0+	–	–	–	–	–	–	–
03	RAMMAP (W/O)	1+	–	–	–	–	–	–	–
06	REFCTL (W/O)	–	–	–	–	0+	–	–	–
85	REGTEST (R/W)	0	1	1R	1R	0	1R	1R	1R

* These two bits are read/write at address 83h and write-only at address 13h. All other sleep register bits are inactive at 13h and read-only at 83h.

\+ These three bits are read/write at address 85h and write-only at address 03h, 06h and 14h. All other bits are inactive a 03h, 06h and 14h and read-only at 85h.

– Registers containing bits with a "–" are write-only registers. The bus will not be driven during a read.

AC CHARACTERISTICS: TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
CPU Mode					
t1	BUSCLK Period	31		ns	
t2	BUSCLK High Time	12		ns	1.5 V
t3	BUSCLK Low Time	12		ns	1.5 V
t7	SYSCLK Fall Time		10	ns	0.8 V to 2.0 V @ CL=200
t8	SYSCLK Rise Time		10	ns	0.8 V to 2.0 V @ CL=200
tD9	BUSCLK to SYSCLK Delay	3	35	ns	CL=200 pF
tSU10	–CHSO, –CHS1, CHM/–IO to BUSCLK Setup Time	7		ns	(Note 2)
tH11	–CHS0, –CHS1, CHM/–IO fro BUSCLK Hold Time	4		ns	(Note 2)
tD12	BALE from BUSCLK Delay	3	28	ns	CL=200 pF
t13	BALE Pulse Width	31		ns	
tD14	–CHREADY from BUSCLK Delay	3	25	ns	CL=50 pF
tSU15	A23-A2, –BE3- –BE0 to –EALE Setup Time	12		ns	
tH16	A23-A2, –BE3- –BE0 from –EALE Hold Time	4		ns	
tD17	LA Bus Valid from A Bus	3	35	ns	Standard Bus Cycles. CL=200 pF (Note 3)
tD17a	LA Bus Valid from –EALE Delay	3	40	ns	First cycle following decoupled refresh. CL=200 pF (Note 3)
tD18	SA Bus, –SBHE Valid from BUSCLK Delay	3	40	ns	CL=200 pF (Note 4)
tD19	–CMD from BUSCLK Delay	3	35	ns	CL=200 pF (Note 5)
tSU20	–MEMCS16 to BUSCLK Setup Time	12		ns	
tH21	–MEMCS16 from BUSCLK Hold Time	5		ns	
tSU22	–WS0 to BUSCLK Setup Time	15		ns	
tH23	–WS0 from BUSCLK Hold Time	5		ns	
tD24	–XDREAD from BUSCLK Delay	3	40	ns	CL=50 pF
tD25	–SCMD Valid from BUSCLK Delay	3	35	ns	CL=200 pF (Note 6)
tD26	–SCMD Active from BUSCLK Delay	3		ns	CL=200 pF
tD27	–SCMD Float from BUSCLK Delay		40	ns	CL=200 pF
tSU28	IOCHRDY to BUSCLK Setup Time	12		ns	
tH29	IOCHRDY from BUSCLK Hold Time	5		ns	
tSU30	–IOCS16 to BUSCLK Setup Time	18		ns	
tH31	–IOCS16 from BUSCLK Hold Time	5		ns	
tD32	–LATLO, –LATHI Delay from BUSCLK	3	40	ns	CL=50 pF
tD33	–SDSWAP Delay from BUSCLK	3	45	ns	CL=50 pF
tD34	–SDSWAP Delay from –IOCS16	3	25	ns	Late –IOCS16. Read cycles only. CL=50 pF
tD35	SDLH/–HL Delay from BUSCLK	3	45	ns	CL=50 pF

AC CHARACTERISTICS (Cont.): TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
CPU Mode (Cont.)					
tD36	XD Bus Delay from BUSCLK	3	150	ns	CL=50 pF (Note 7)
tD38	XD Bus Float from BUSCLK	3	55	ns	CL=50 pF (Note 7)
tSU39	XD Bus to BUSCLK Setup Time	75		ns	(Note 7)
tH40	XD Bus from BUSCLK Hold Time	30		ns	(Note 7)
tD41	CS8042/–RTC Delay from BUSCLK	3	50	ns	CL=50 pF
tD42	SPKR, NMI Delay from BUSCLK	3	60	ns	Following write to Port B. CL=50 pF
Bus Arbitration Timing					
tD43	AEN from HLDA Delay	3	35	ns	CL=200 pF
tD44	ALE from HLDA Delay	3	35	ns	CL=200 pF
tD45	–MR/–MW Active from HLDA Delay	3		ns	CL=50 pF
tD46	–MR/–MW Float from HLDA Delay		30	ns	CL=50 pF
tD47	SA/LA Bus, –SBHE, –MEMR Active from –REFRESH	3		ns	CL=200 pF (Notes 3, 4)
tD48	SA/LA Bus, –SBHE, –MEMR Float from –REFRESH		50	ns	CL=200 pF (Notes 3, 4)
Interrupt Timing					
t50	External Interrupt Request Pulse Width Low	90		ns	
tD51	INTR Active Delay from External IRQ	3	130	ns	CL=50 pF
tD52	INTR Inactive from BUSCLK	3	110	ns	Following 2nd interrupt acknowledge pulse. CL=50 pF
Miscellaneous Timing					
tD55	NMI Delay from –PCK, –IOCHK	3	50	ns	CL=50 pF
tD56	LA20 from –BLKA20 Delay	3	35	ns	CL=200 pF
tD57	–TRI Delay (Three State All Outputs, I/Os)		160	ns	AC timing not 100% tested.
tD58	INTR Active Delay from XTALIN	3	350	ns	When source is internal IRQ8 (RTC) interrupt. CL=50 pF
tD59	PS Pulse Width	1		µs	
tH60	PS Hold Following VBAT > VBAT (min.)	1		µs	
tD61	VRT Bit Delay		1	µs	Following read of RTC register D.
tH62	POWERGOOD Active Hold from VDD > VDD (min.)	1		µs	
tH63	VDD > VDD (min.) Hold after POWERGOOD Low	1		µs	To ensure RTC data integrity.
tSU64	POWERGOOD to BUSCLK Setup Time	25		ns	(Note 2)
tH65	POWERGOOD from BUSCLK Hold Time	10		ns	(Note 2)
tD66	RSTDRV from BUSCLK Delay		35	ns	

AC CHARACTERISTICS (Cont.): TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
Timer/Counter Timing					
t67	OSC Period	50		ns	
t68	OSC High Time	20		ns	0.8 V to 2.0 V
t69	OSC Low Time	20		ns	0.8 V to 2.0 V
tD70	OUT1, SPKR Delay from OSC	3	120	ns	CL=50 pF
tD71	INTR Delay from OSC	3	200	ns	When source is from internal IRQ0. CL=50 pF
DMA Mode					
tSU73	DRQ to BUSCLK Setup Time	0		ns	
tD74	–DACK from BUSCLK Delay	3	100	ns	CL=100 pF
tD75	–CMD Valid from BUSCLK Delay	3	85	ns	CL=200 pF (Note 5)
tD76	–MR/–MW Valid from BUSCLK Delay	3	80	ns	CL=50 pF
tD77	A Bus, –BE3- –BE0 Valid from BUSCLK Delay	3	125	ns	CL=50 pF
tD78	A Bus, –BE3- –BE0 Active from BUSCLK Delay	3		ns	CL=50 pF
tD79	A Bus, –BE3- –BE0 Float from BUSCLK Delay		80	ns	CL=50 pF
tD80	SA, –SBHE Valid from BUSCLK Delay	3	115	ns	CL=200 pF
tD81	LA23-LA17 Valid from BUSCLK Delay	3	130	ns	CL=200 pF
tD82	DMAHRQ from BUSCLK Delay	3	70	ns	CL=50 pF
tSU83	DMAHLDA to BUSCLK Setup Time	25		ns	(Note 2)
tH83a	DMAHLDA from BUSCLK Hold Time	20		ns	(Note 2)
tD84	T/C from BUSCLK Delay	3	85	ns	CL=50 pF
tSU85	IOCHRDY to BUSCLK Setup Time	15		ns	
tH86	IOCHRDY from BUSCLK Hold Time	20		ns	
tD87	–SCMD Valid from BUSCLK Delay	3	85	ns	CL=200 pF (Note 6)
tD88	–SCMD Active from BUSCLK Delay	3		ns	CL=200 pF (Note 6)
tD89	–SCMD Float from BUSCLK Delay		135	ns	CL=200 pF (Note 6)
tD90	–SDSWAP Delay from BUSCLK	3	125	ns	CL=50 pF
tD90a	–SDSWAP Delay from –MEMCS16	3	35	ns	CL=50 pF
tD90b	–SDSWAP Delay from –BRDRAM	3	35	ns	CL=50 pF
tD91	SDLH/–HL Delay from BUSCLK	3	130	ns	CL=50 pF
tD91a	SDLH/–HL Delay from –MEMCS16	3	35	ns	CL=50 pF
tD91b	SDLH/–HL Delay from –BRDRAM	3	35	ns	CL=50 pF

AC CHARACTERISTICS (Cont.): TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
Master Mode					
tD96	SA/LA Bus, –CMD Float from –MASTER Low		30	ns	CL=200 pF (Notes 3, 4)
tD97	SA/LA Bus, –CMD Active from –MASTER High	3		ns	CL=200 pF (Notes 3, 4)
tD98	A Bus, –BE3- –BE0 Active from –MASTER Low	3		ns	CL=50 pF
tD99	A Bus, –BE3- –BE0 Float from –MASTER High		25	ns	CL=50 pF
tD100	AEN Delay from –MASTER	3	35	ns	CL=200 pF
tSU101	LA/SA Bus, –SBHE to –CMD Setup Time	75		ns	(Notes 3, 4, 7)
tH102	LA/SA Bus, –SBHE to –CMD Hold Time	20		ns	(Notes 3, 4, 7)
t103	–CMD Pulse Width	187		ns	(Notes 5)
tD104	–MR/–MW Delay from –MEMW/–MEMR	3	20	ns	CL=50 pF
tSU105	XD to –IOW Setup Time	100		ns	(Note 7)
tH106	XD to –IOW Hold Time	20		ns	(Note 7)
tD107	XD from –IOR Delay Time	3	135	ns	CL=50 pF (Note 7)
tD108	XD Float Delay from –IOR Inactive	3	40	ns	CL=50 pF (Note 7)
tD109	LA/SA Bus, –SBHE to A Bus, –BE Delay	3	35	ns	CL=50 pF (Notes 3, 4)
tD110	–CS8042 Delay from SA, LA Bus Valid	3	40	ns	CL=50 pF (Notes 3, 4)
tD111	SPKR, NMI Delay from –IOW Inactive	3	45	ns	Following write to Port B. CL=50 pF
tD112	–XDREAD from –IOR Delay	3	30	ns	CL=50 pF
tD114	–SDSWAP Delay from –CMD	3	35	ns	CL=50 pF (Note 5)
tD115	–SDSWAP Delay from CONTROL	3	35	ns	CL=50 pF (Note 8)
tD119	SDLH/–HL Delay from –CMD	3	35	ns	CL=50 pF (Note 5)
tD120	SDLH/–HL Delay from CONTROL	3	35	ns	CL=50 pF (Note 8)
tD124	–SCMD Valid from –MEMW/–MEMR Delay	3	30	ns	CL=200 pF (Note 6)
tD125	–SCMD Active from LA Bus Delay	3		ns	CL=200 pF (Notes 3, 6)
tD126	–SCMD Float from LA Bus Delay		30	ns	CL=200 pF (Notes 3, 6)
tD127	LA Bus Valid, –SBHE Low from –REFRESH	3	70	ns	CL=200 pF (Note 3)
tD128	–MEMR from BUSCLK Delay	3	50	ns	CL=200 pF (Note 9)
tD129	–MR from BUSCLK Delay	3	45	ns	CL=50 pF (Note 9)
tSU130	–REFRESH to BUSCLK Setup Time	20		ns	(Note 2)
tD131	–REFRESH from BUSCLK Delay (Release)	3	50	ns	Until refresh is no longer driven. CL=200 pF (Note 9)
tD132	–SMEMR Valid from BUSCLK Delay	3	50	ns	CL=200 pF (Note 9)
tD133	–SMEMR Active from –REFRESH Delay	3		ns	CL=200 pF

AC CHARACTERISTICS (Cont.): TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
Master Mode (Cont.)					
tD134	–SMEMR Float from BUSCLK Delay		60	ns	CL=200 pF (Note 9)
tSU135	IOCHRDY Setup to BUSCLK	5		ns	(Note 9)
tH136	IOCHRDY Hold from BUSCLK	20		ns	(Note 9)
tD137	SA Bus Valid from BUSCLK Delay	3	60	ns	CL=200 pF (Notes 4, 9)
Decoupled REFRESH Mode					
tD138	LA Bus Valid, –SBHE Low from –BUSCLK	3	80	ns	CL=200 pF (Note 3)
tD139	–REFRESH from BUSCLK Delay (Active)	3	40	ns	CL=200 pF (Note 2)
tD140	–SCMD Active from BUSCLK Delay	3		ns	CL=200 pF (Note 6)
tD141	AEN Delay from BUSCLK	3	55	ns	CL=200 pF
tD142	ALE Delay from BUSCLK	3	55	ns	CL=200 pF

Notes:
2. Asynchronous input, for test purposes only.
3. LA bus refers to LA23-LA17.
4. SA bus refers to the signal pins SA19-SA0.
5. –CMD refers to the signals –MEMR, –MEMW, –IOR, –IOW.
6. –SCMD refers to the signals –SMEMR, –SMEMW.
7. Internal register accesses.
8. –CONTROL refers to –MEMCS16, –IOCS16, SA0, –BRDRAM.
9. Specification also applies to decoupled refresh mode cycles.

FIGURE 5. 16 TO 8 CONVERSION - I/O READS

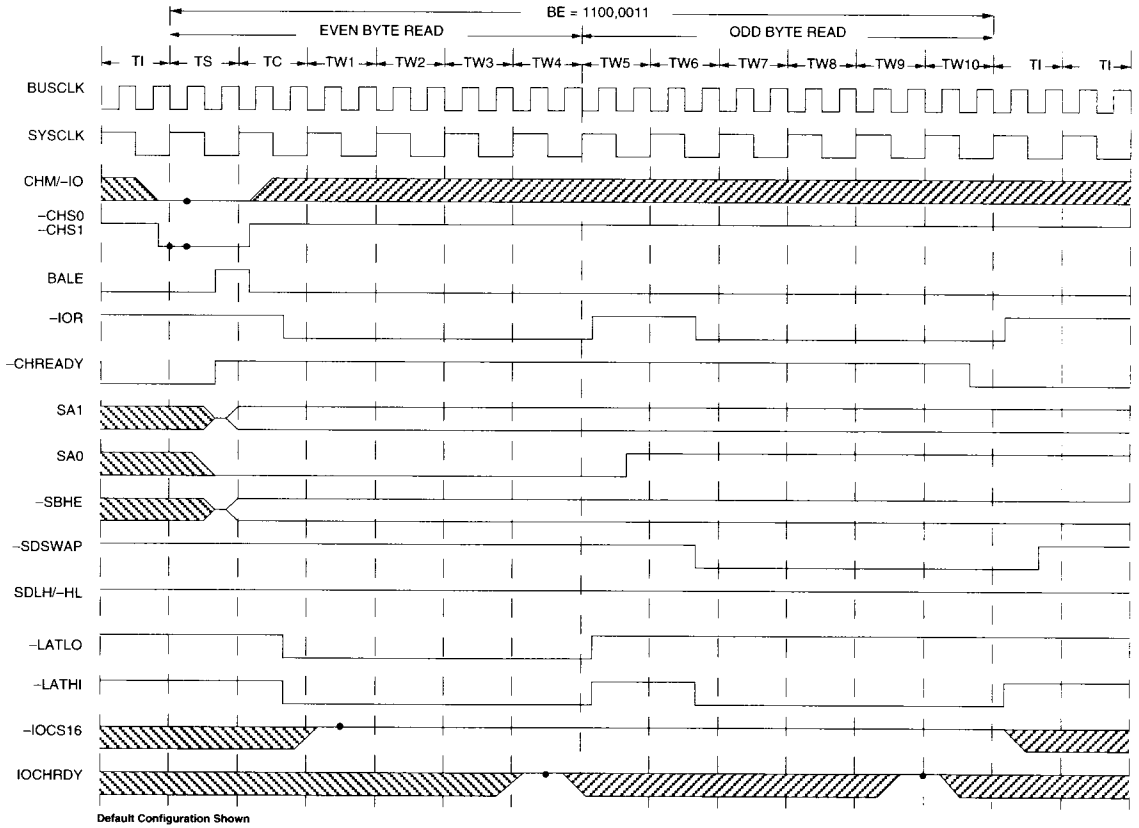


FIGURE 6. 16 TO 8 CONVERSION - I/O WRITES

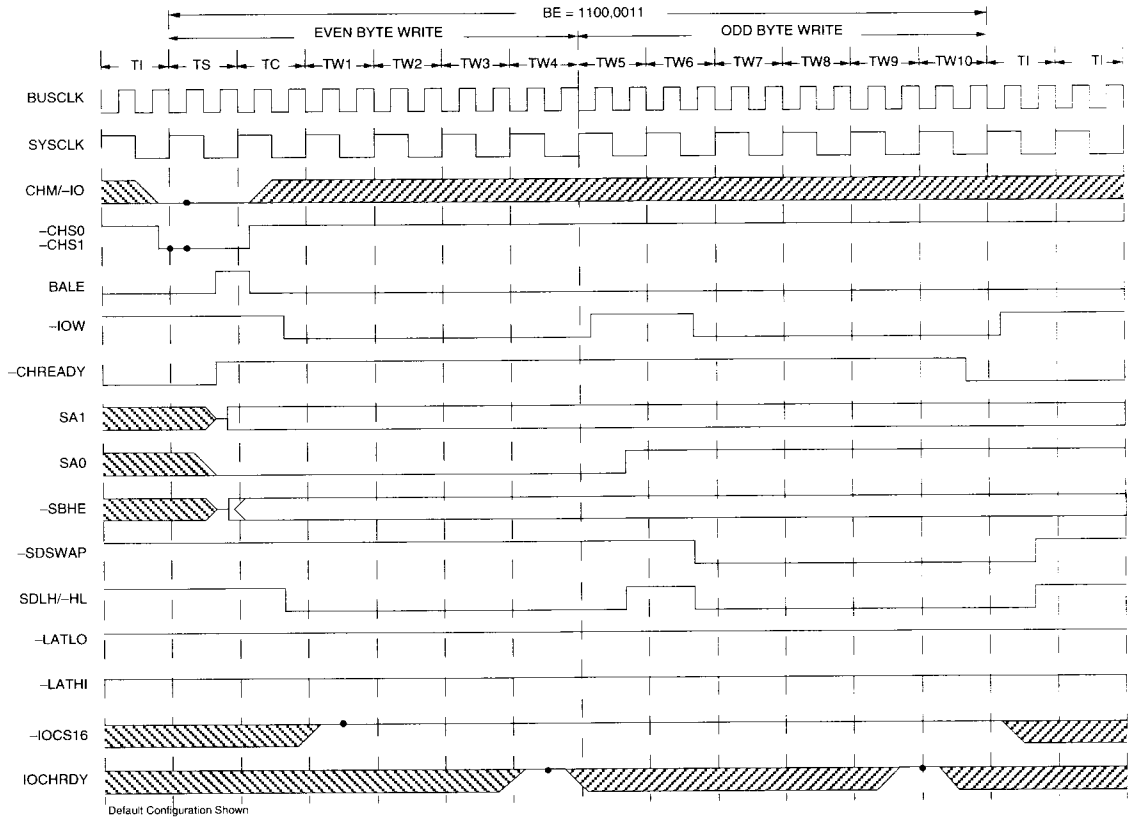


FIGURE 7. 16 TO 8 CONVERSION - MEMORY READS

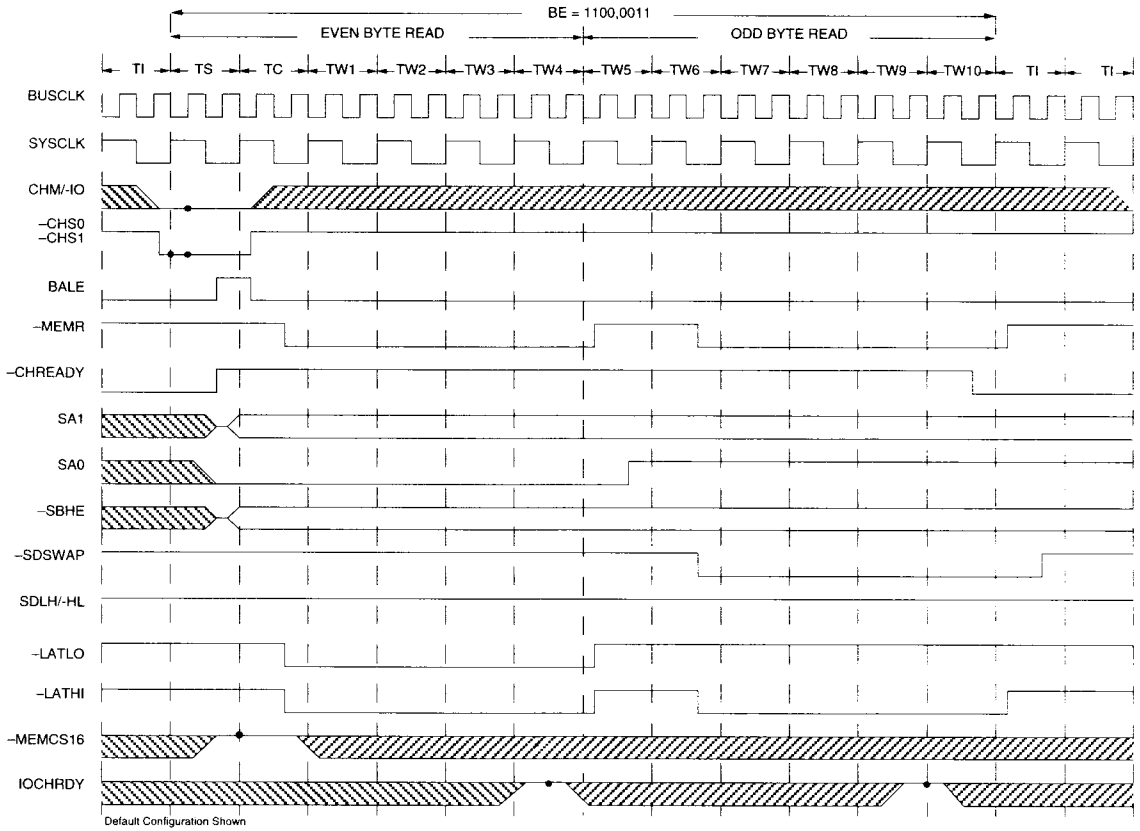


FIGURE 8. 16 TO 8 CONVERSION - MEMORY WRITES

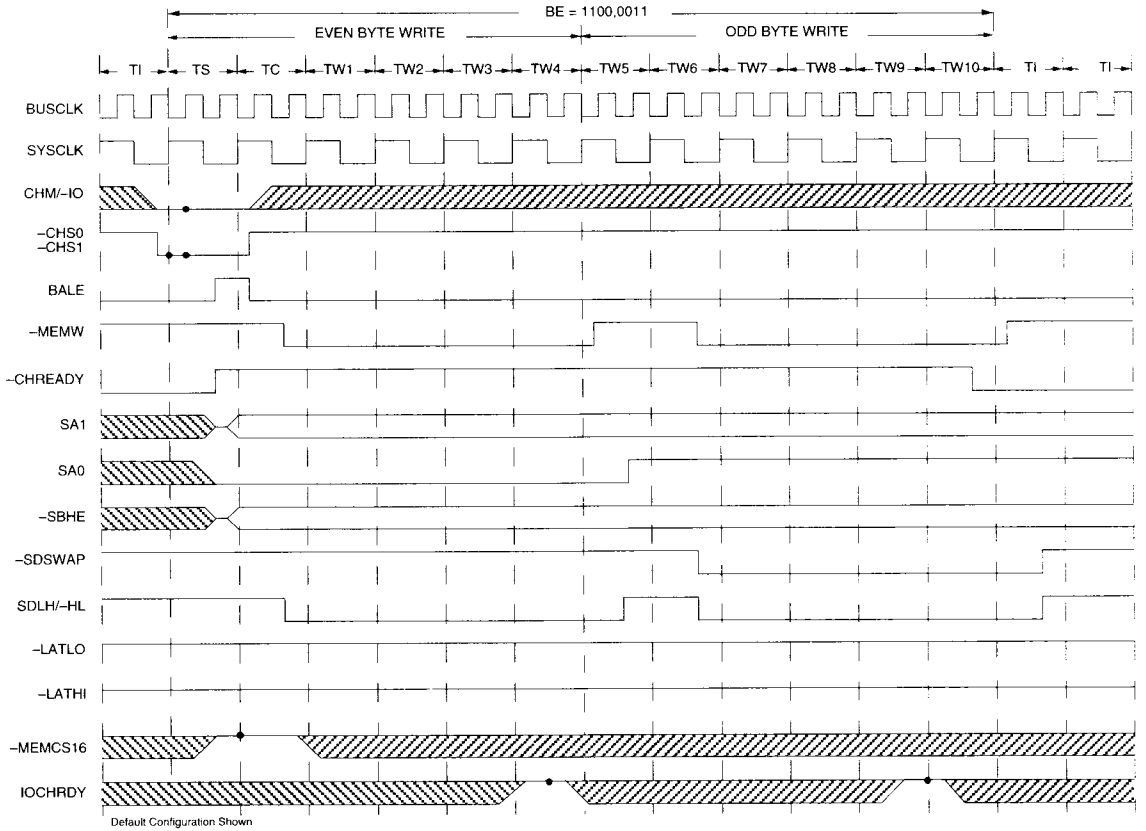


FIGURE 9. 24 TO 8 CONVERSION - I/O READ

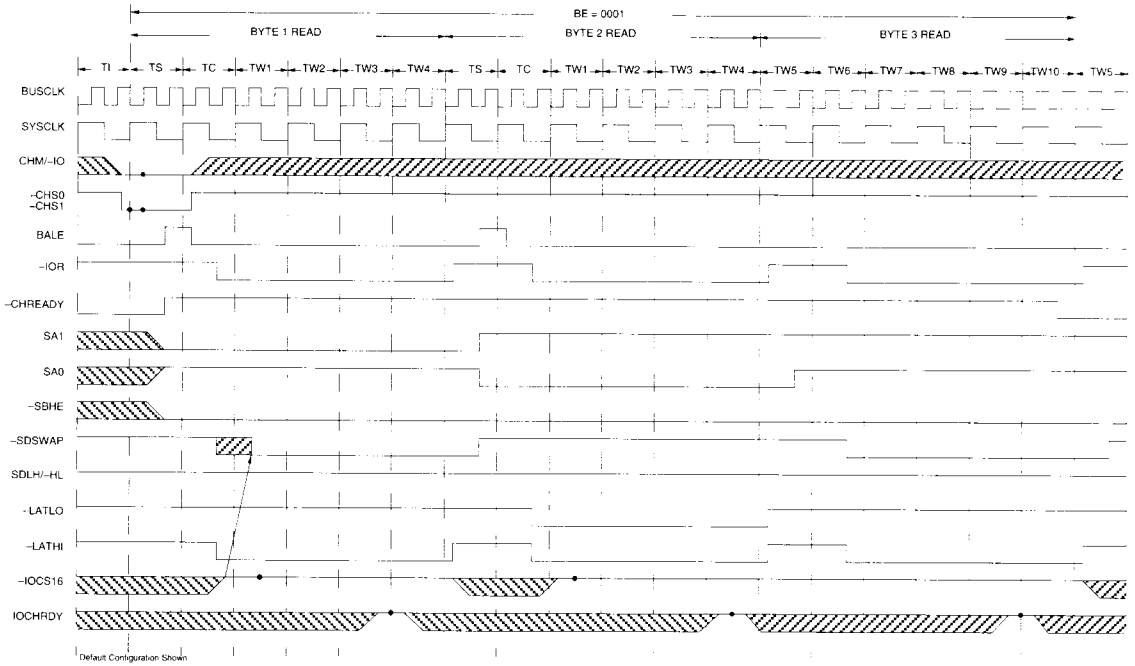


FIGURE 10. 24 TO 8 CONVERSION - I/O WRITE

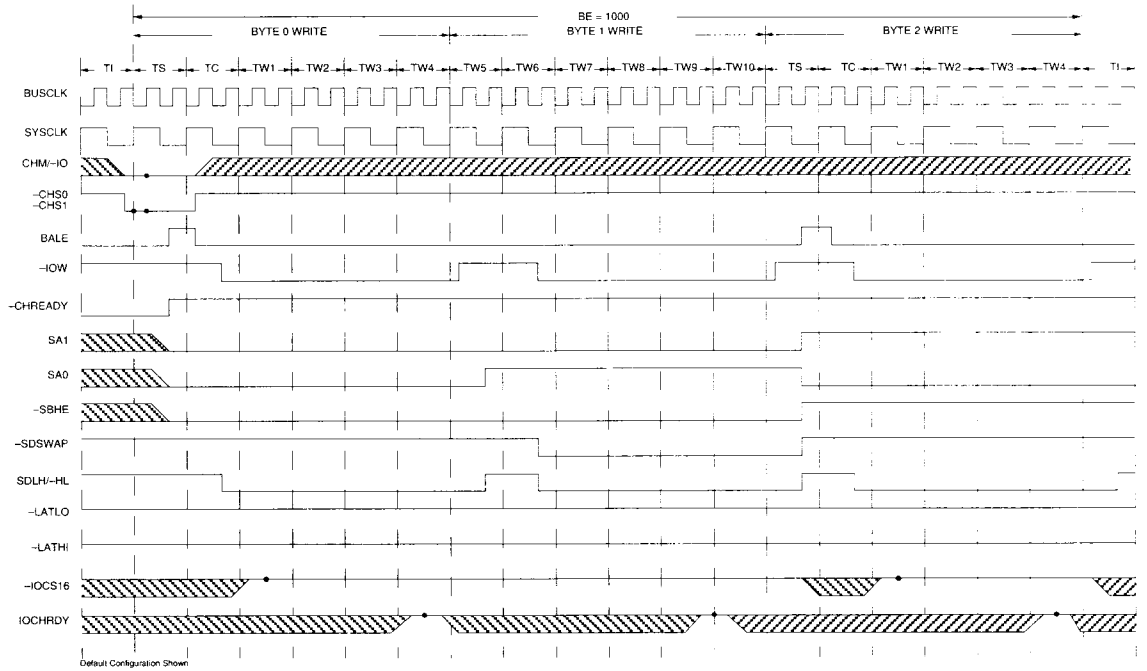


FIGURE 11. 32 TO 8 CONVERSION - MEMORY READ

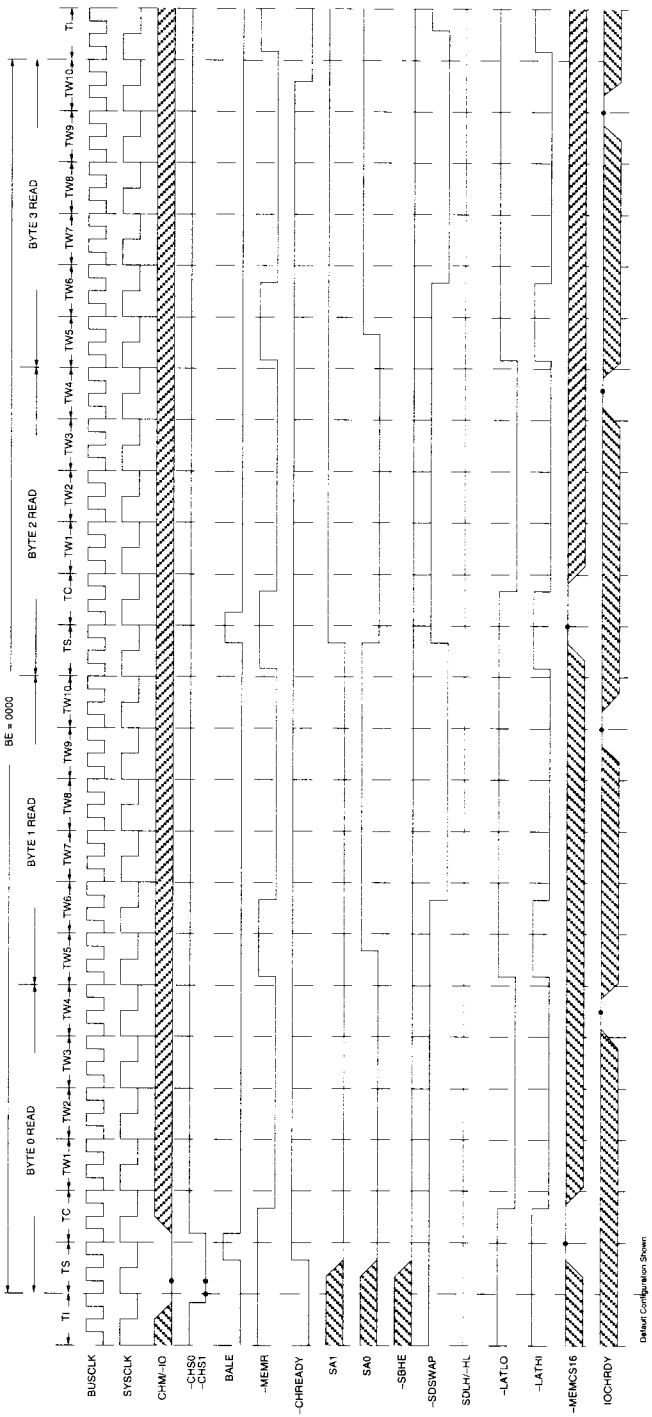


FIGURE 12. 32 TO 8 CONVERSION - MEMORY WRITE

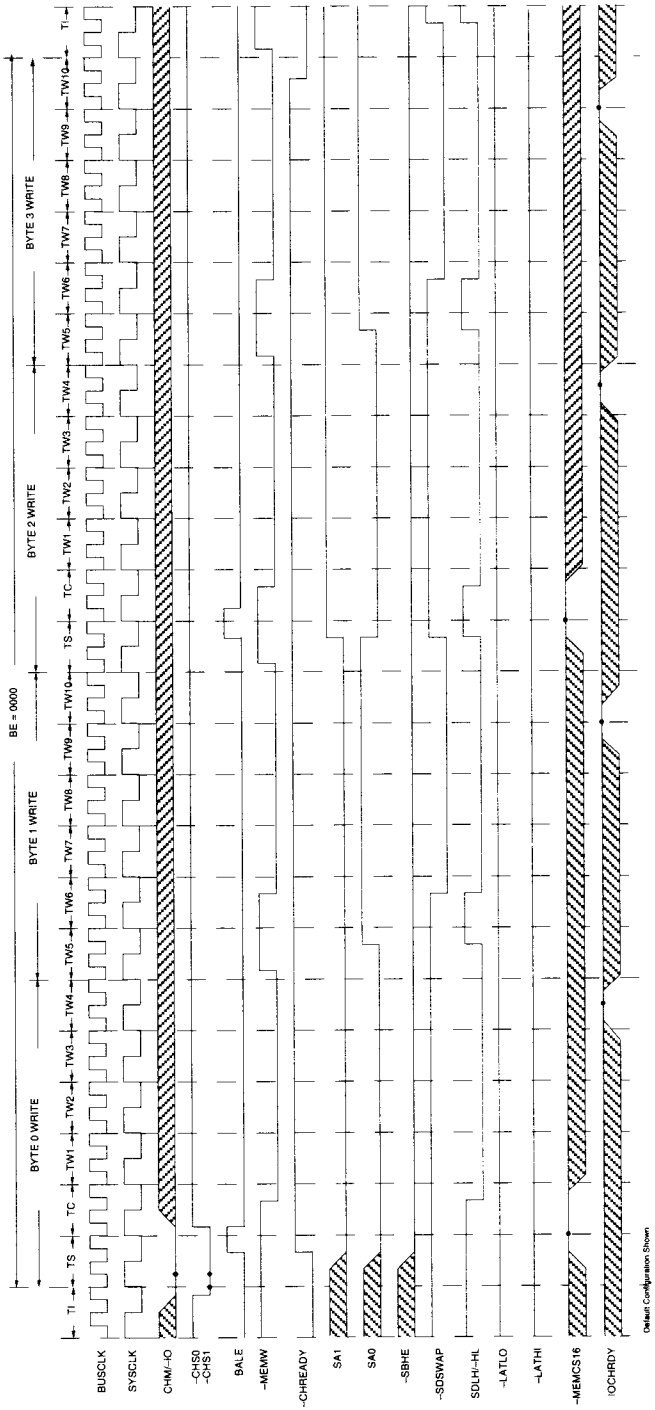


FIGURE 13. 24 TO 16 CONVERSION - MEMORY READS

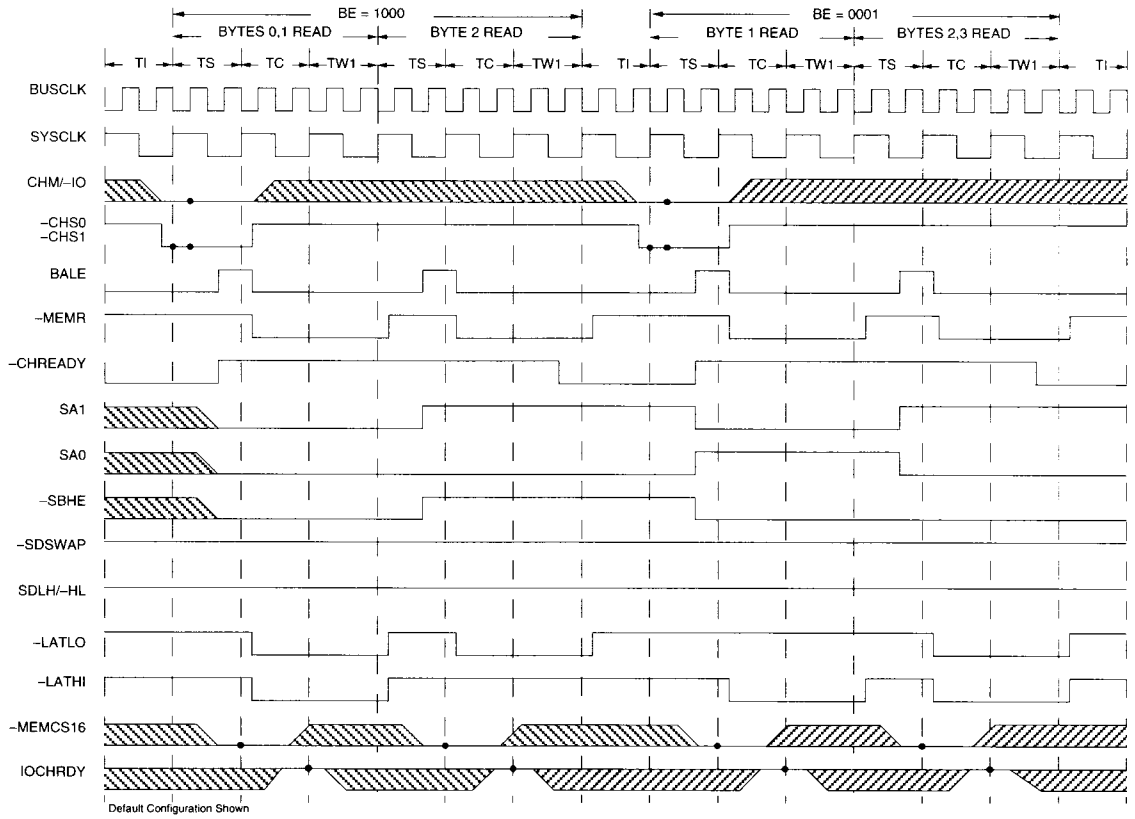


FIGURE 14. 24 TO 16 CONVERSION - MEMORY WRITES

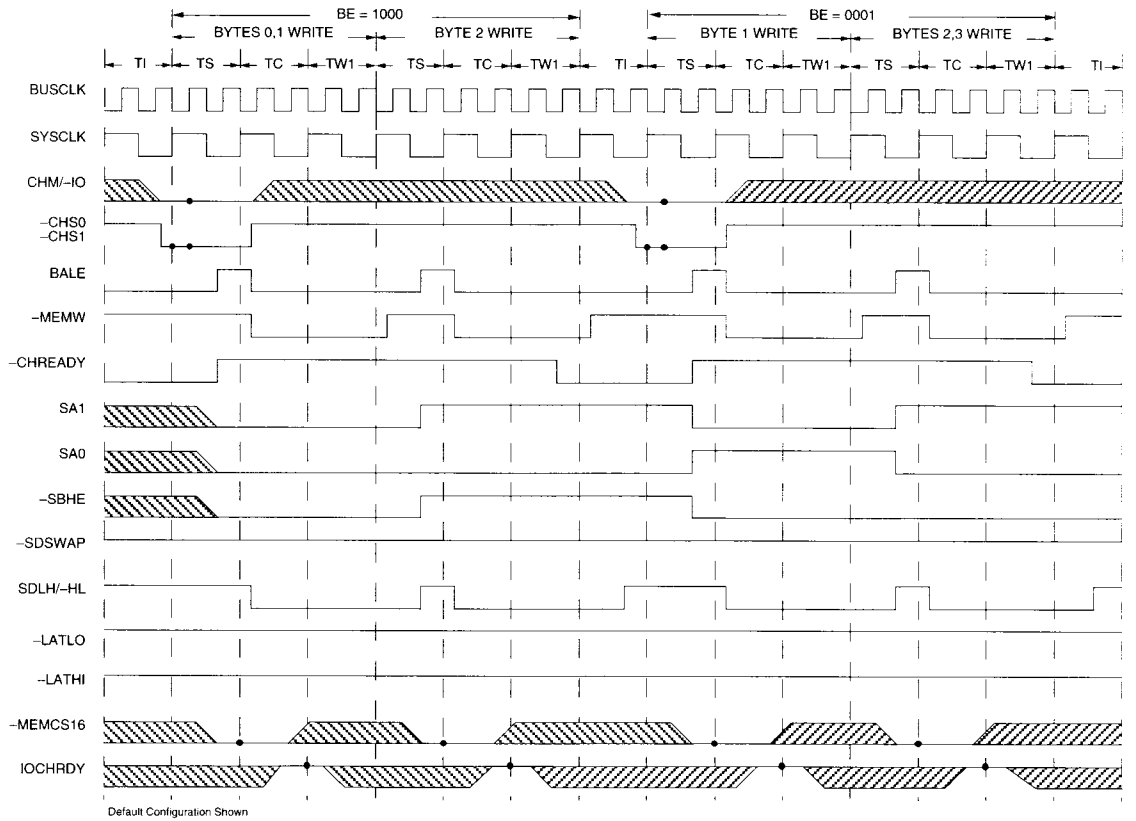


FIGURE 15. 32 TO 16 CONVERSION - MEMORY READS

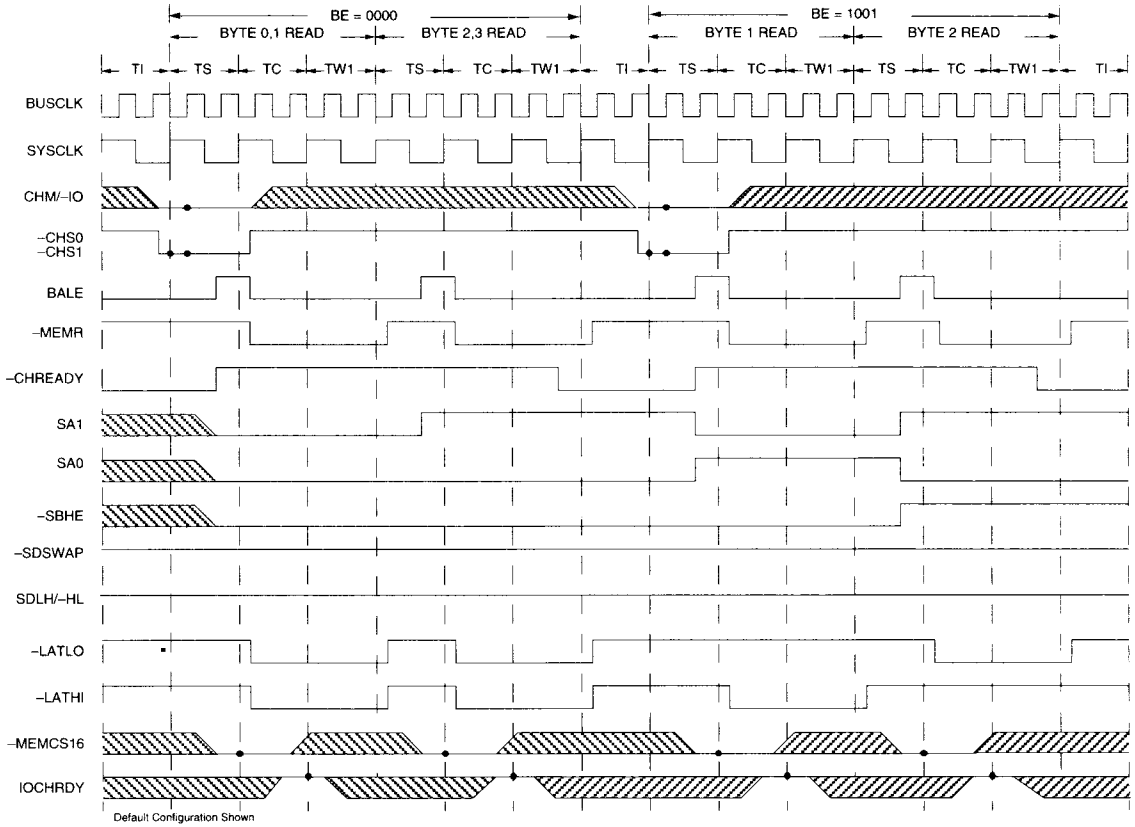


FIGURE 16. 32 TO 16 CONVERSION - MEMORY WRITES

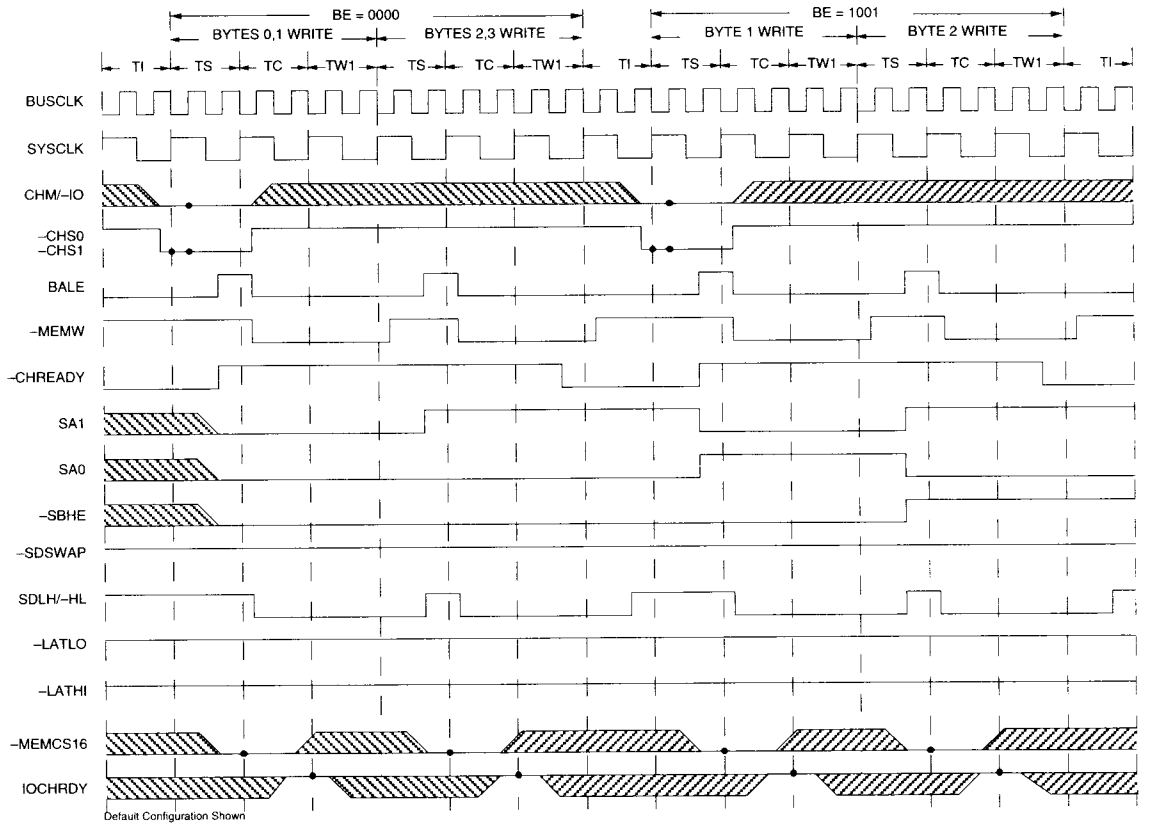


FIGURE 17. 32 TO 16 CONVERSION - I/O READS

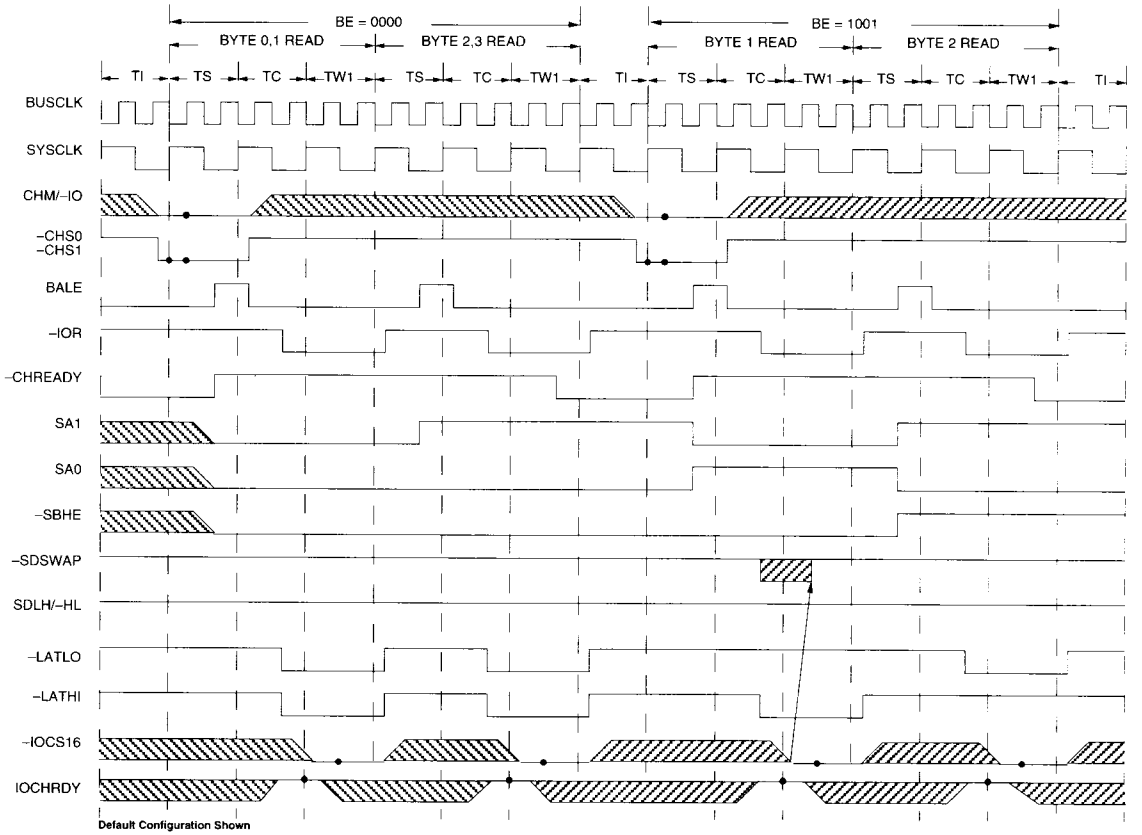


FIGURE 18. 32 TO 16 CONVERSION - I/O WRITES

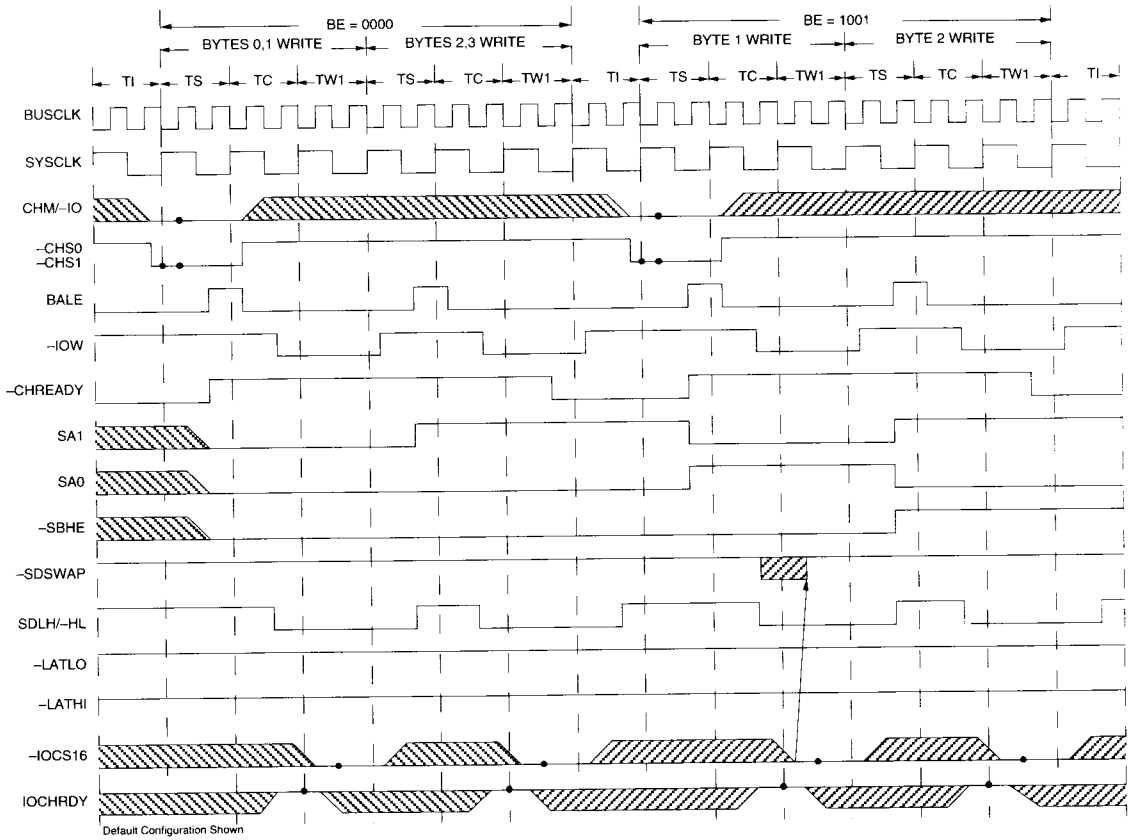
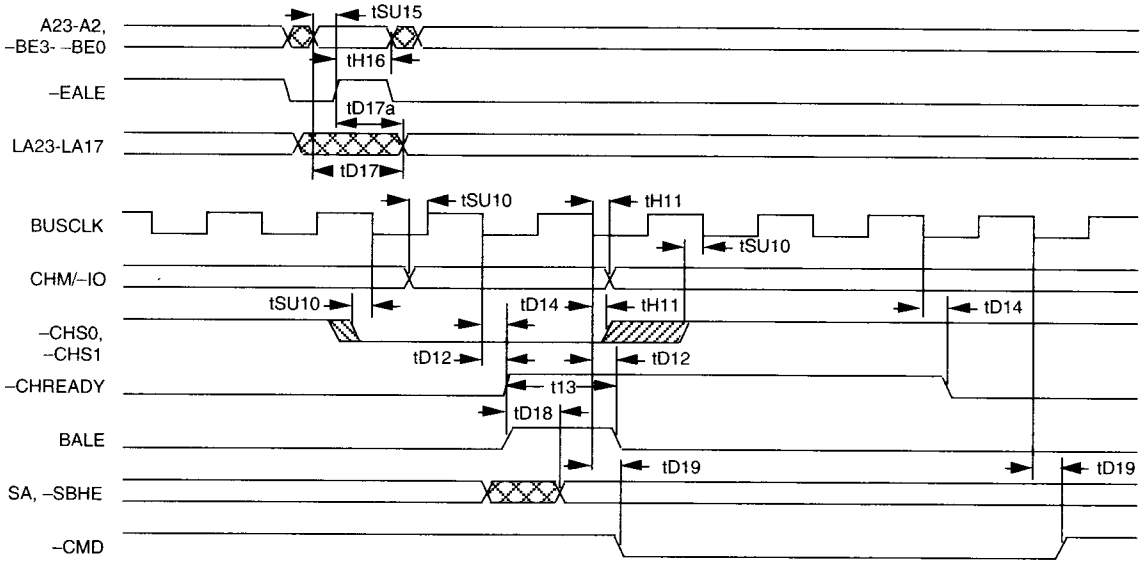


FIGURE 19. ASYNCHRONOUS BUS INTERFACE



Note: 16-bit memory cycle shown.

FIGURE 20. CPU MODE I/O CYCLE (16/8-BIT)

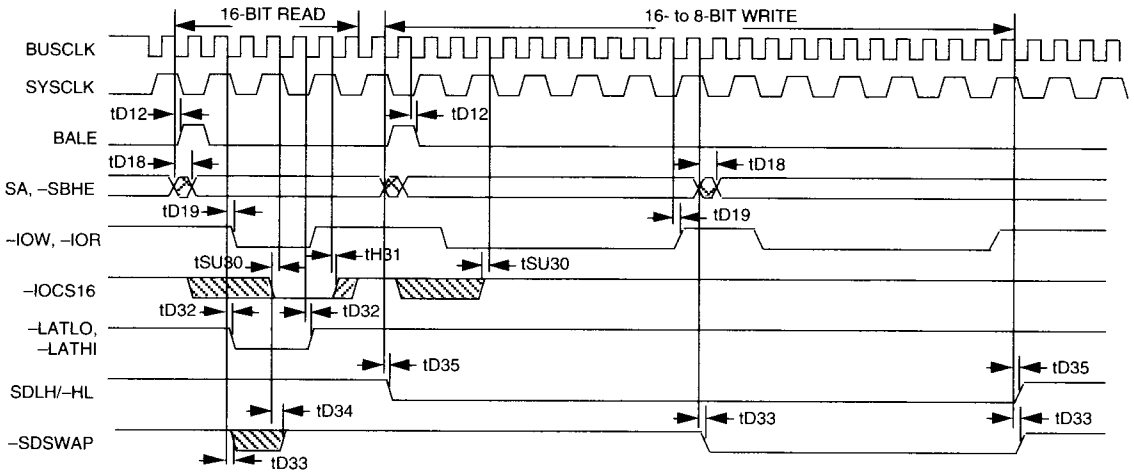
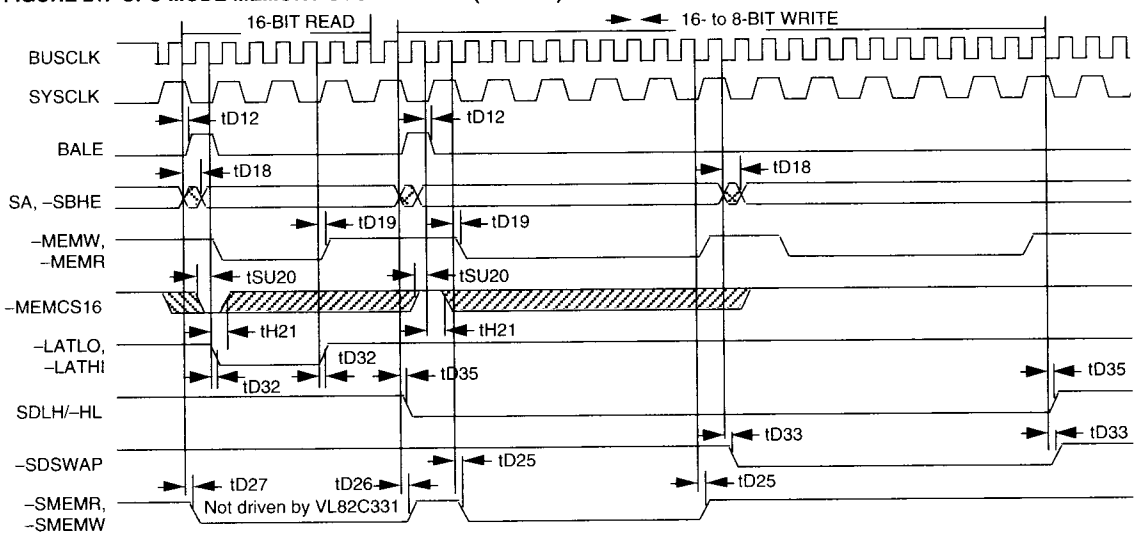


FIGURE 21. CPU MODE MEMORY CYCLE TIMING (16/8-BIT)



Note: -SMEMR and -SMEMW are three-stated for addresses above 1 meg. These should be pulled up externally with a 10k resistor.

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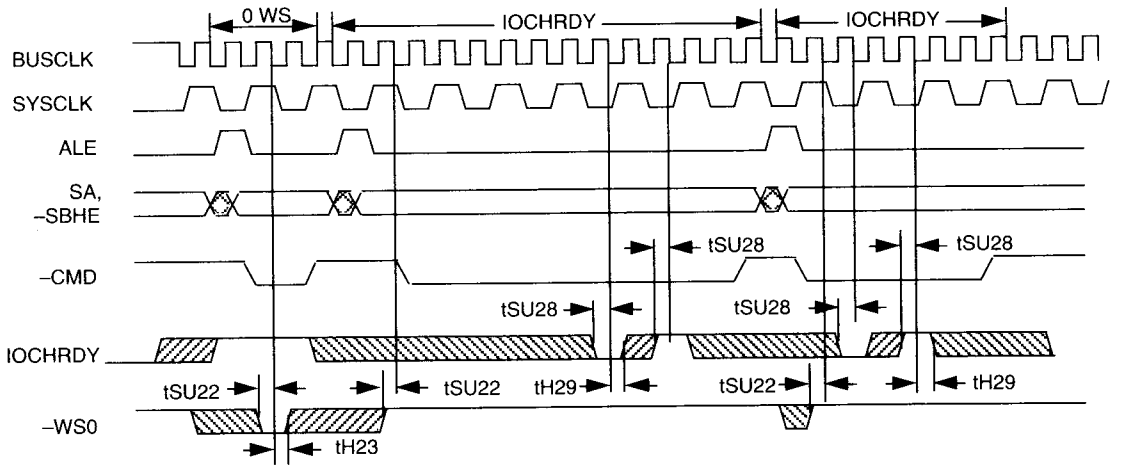
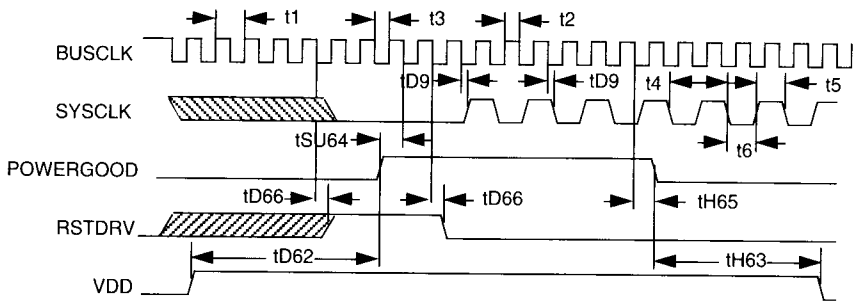
FIGURE 22. CPU MODE WS0 AND IOCHRDY



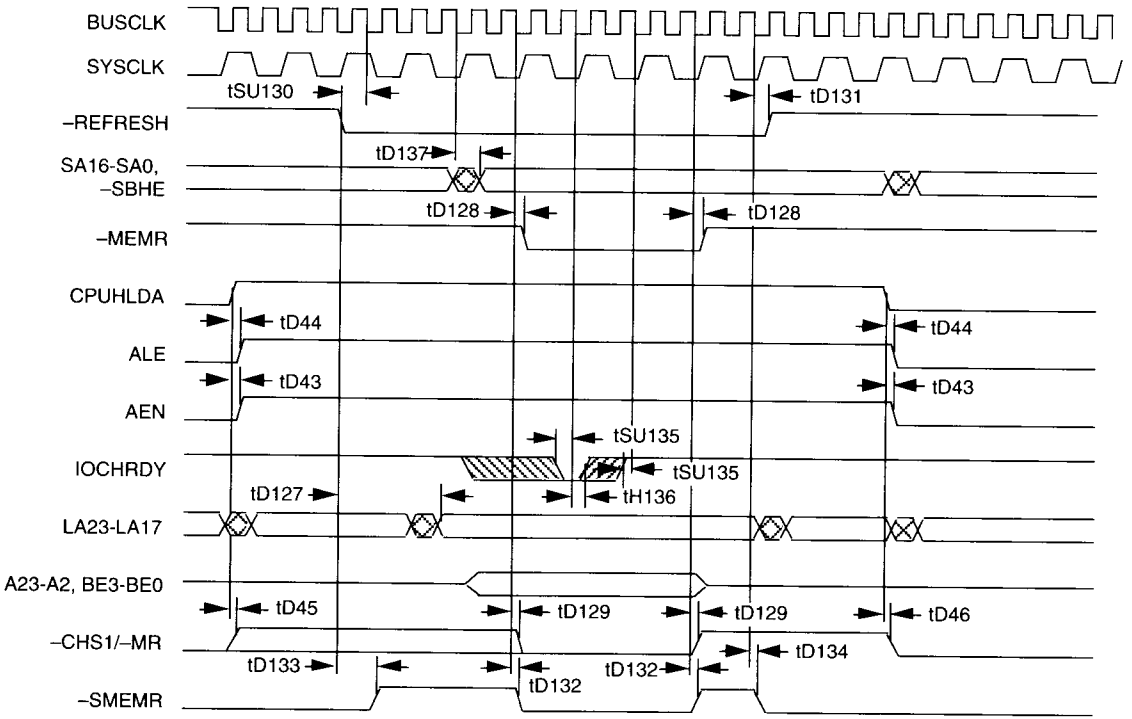
Note: 1. Zero wait state cycle shown is a 16-bit memory cycle. IOCHRDY cycles are 8-bit and 16-bit memory cycles.
2. IOCHRDY and WS0 should not be asserted at the same time. WS0 takes precedence over IOCHRDY.

FIGURE 23. CLOCK/RESET



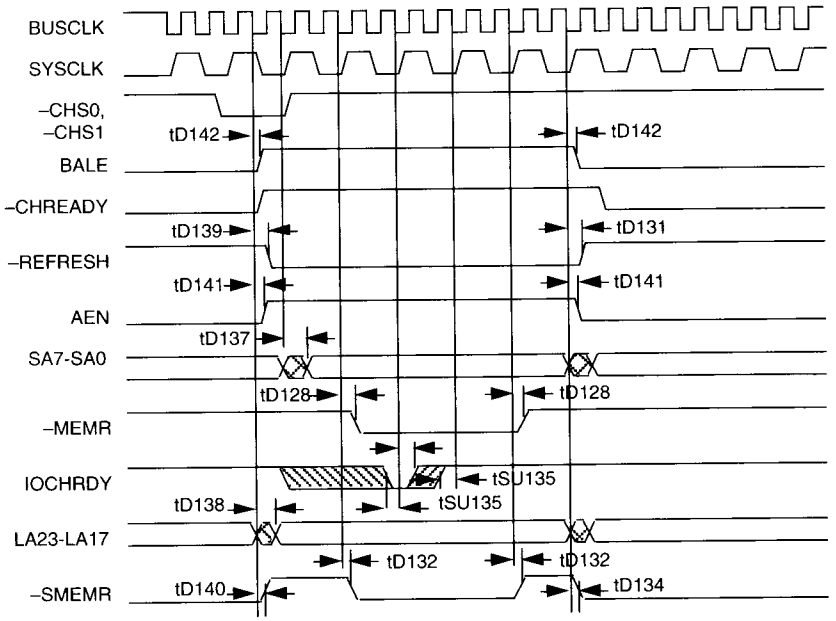
Note: POWERGOOD is an asynchronous input. This specification is given for testing purposes only. The specifications on POWERGOOD with respect to VDD are given to ensure predictable behavior. They also guarantee protection of the RTC battery-backed registers.

FIGURE 24. COUPLED REFRESH



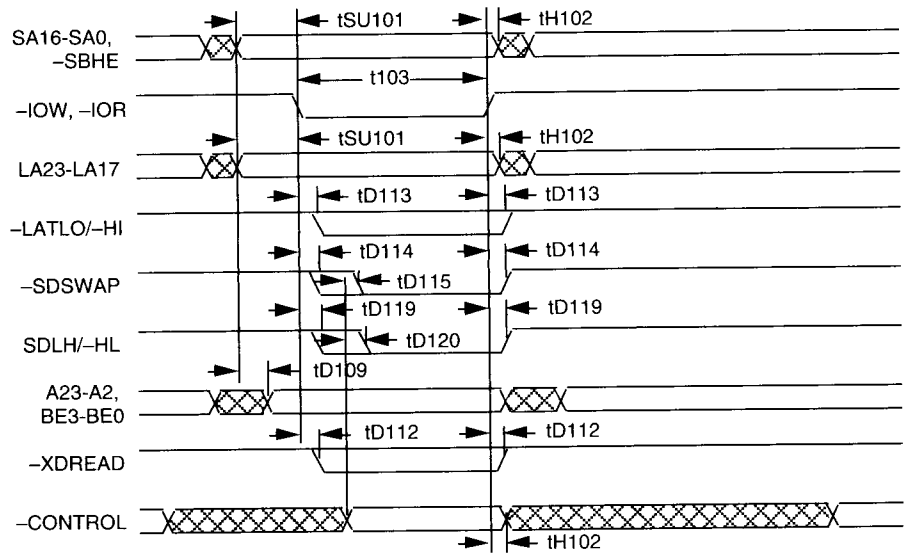
Note: –SMEMR is three-stated for addresses above 1 meg. It should be pulled up externally with a 10k resistor.

FIGURE 25. DECOUPLED REFRESH



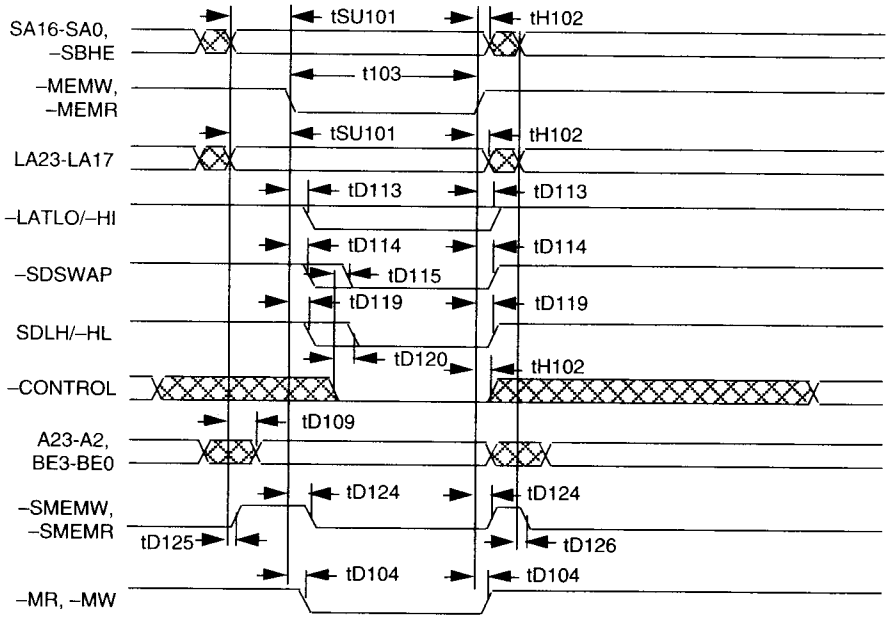
Note: –SMEMR is three-stated for addresses above 1 meg. It should be pulled up externally with a 10k resistor.

FIGURE 26. MASTER MODE CYCLE (I/O ACCESS)



Note: –CONTROL refers to the signals –IOCS16, –MEMCS16, –BRDRAM and SA0.

FIGURE 27. MASTER MODE CYCLE (MEMORY ACCESS)



Note: –CONTROL refers to the signals –IOCS16, –MEMCS16, –BRDRAM and SA0.

FIGURE 28. DMA MODE CYCLE (8-BIT)

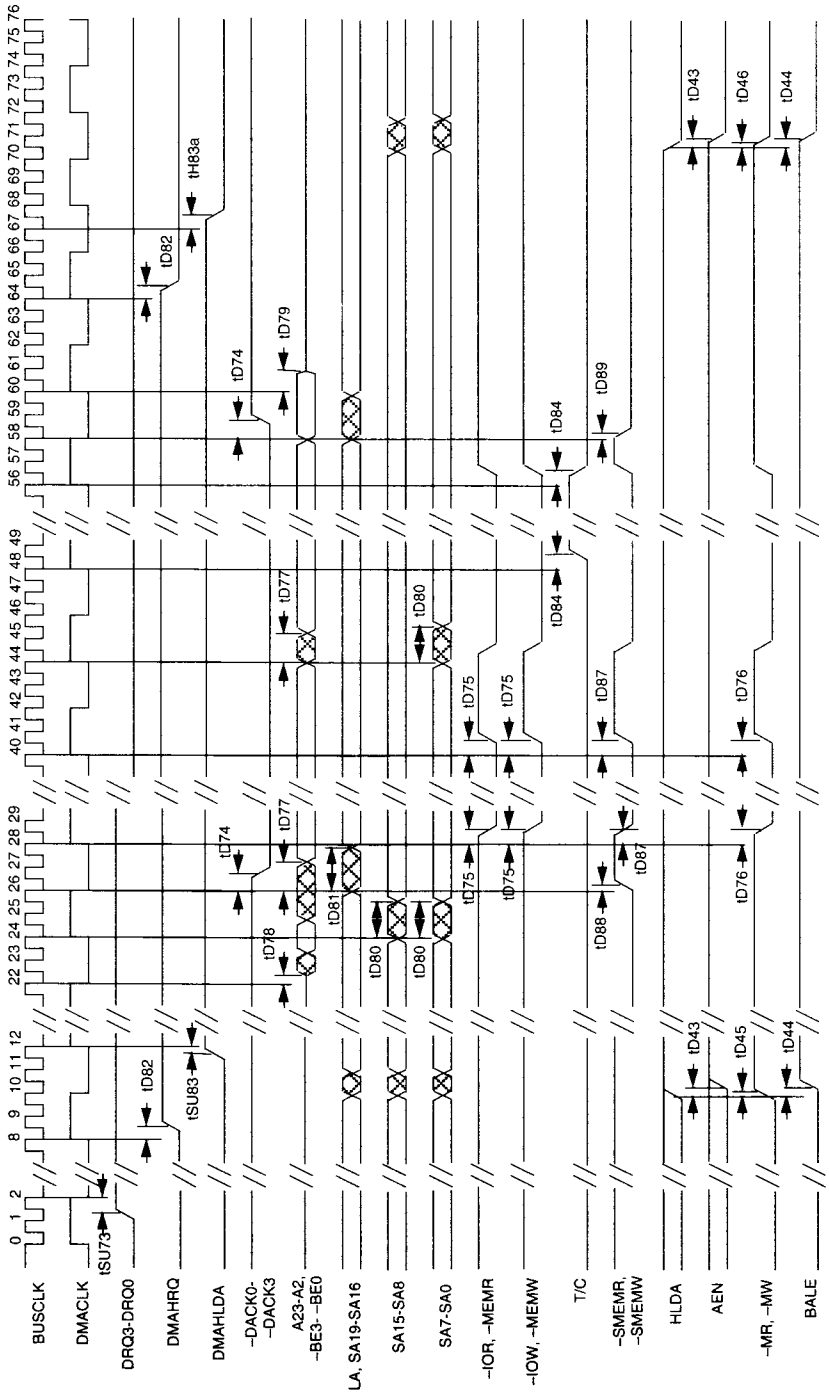


FIGURE 29. DMA MODE CYCLE (16-BIT)

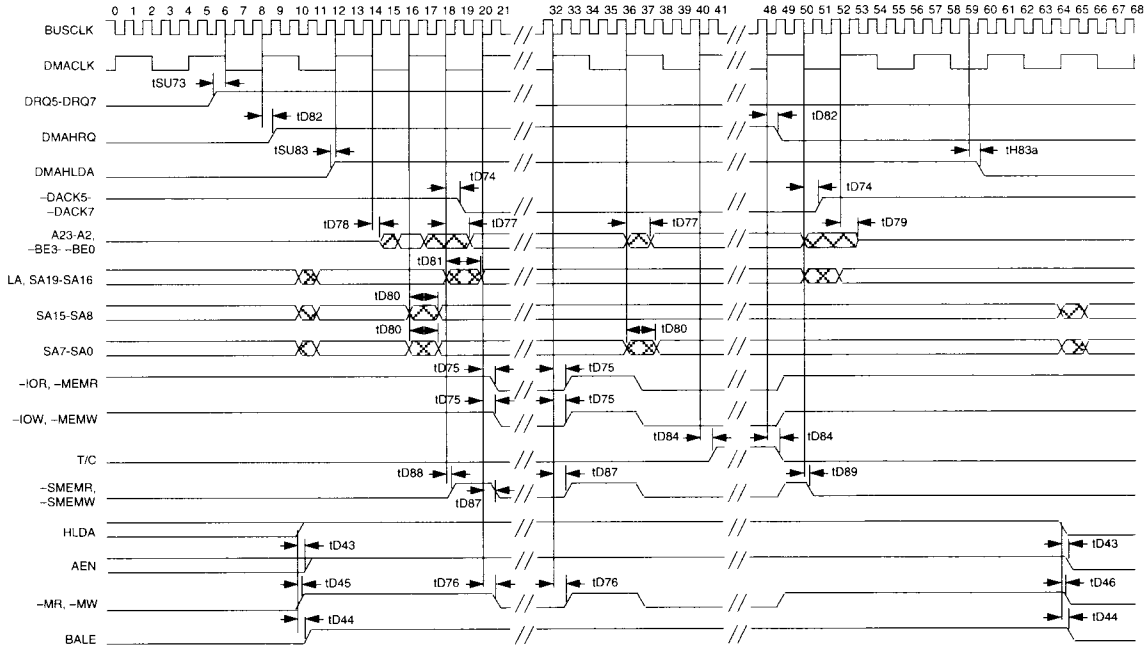


FIGURE 30. MASTER MODE ARBITRATION

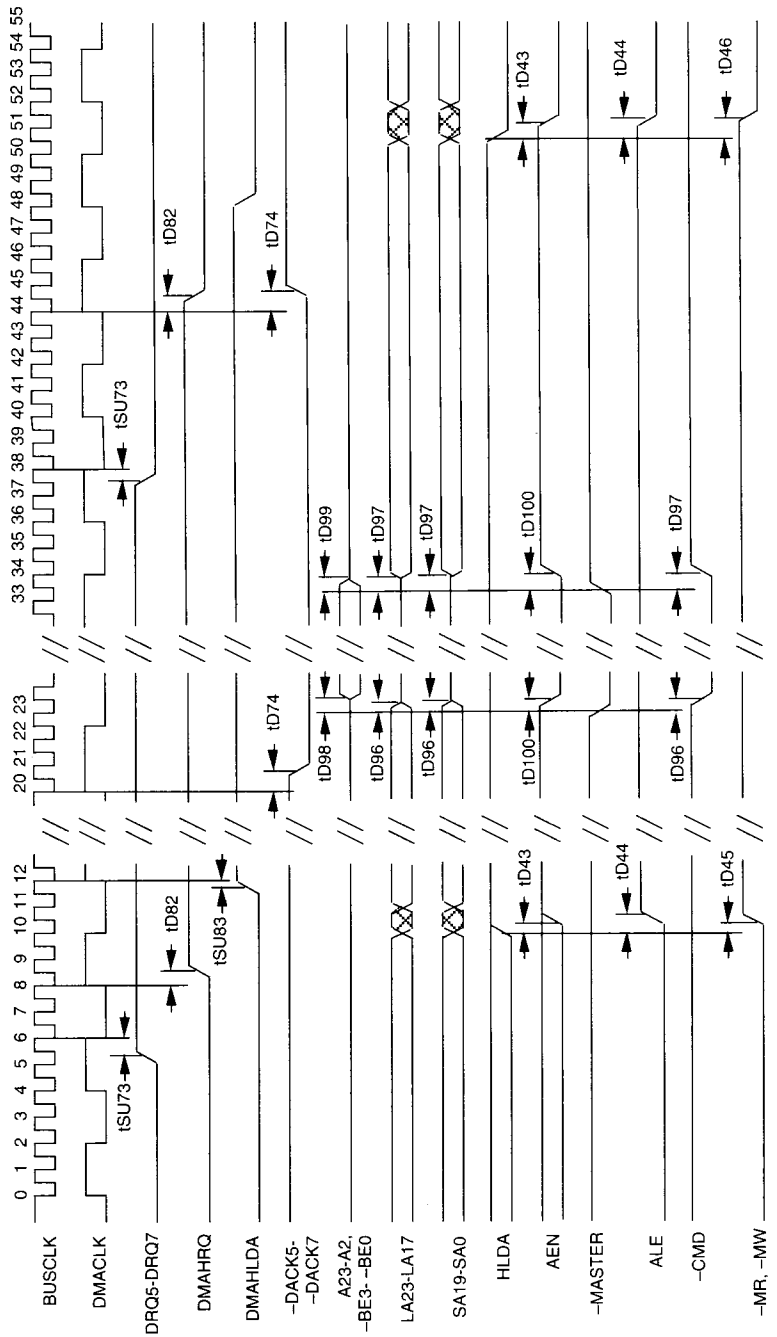


FIGURE 31. INTERRUPT/ACKNOWLEDGE CYCLE

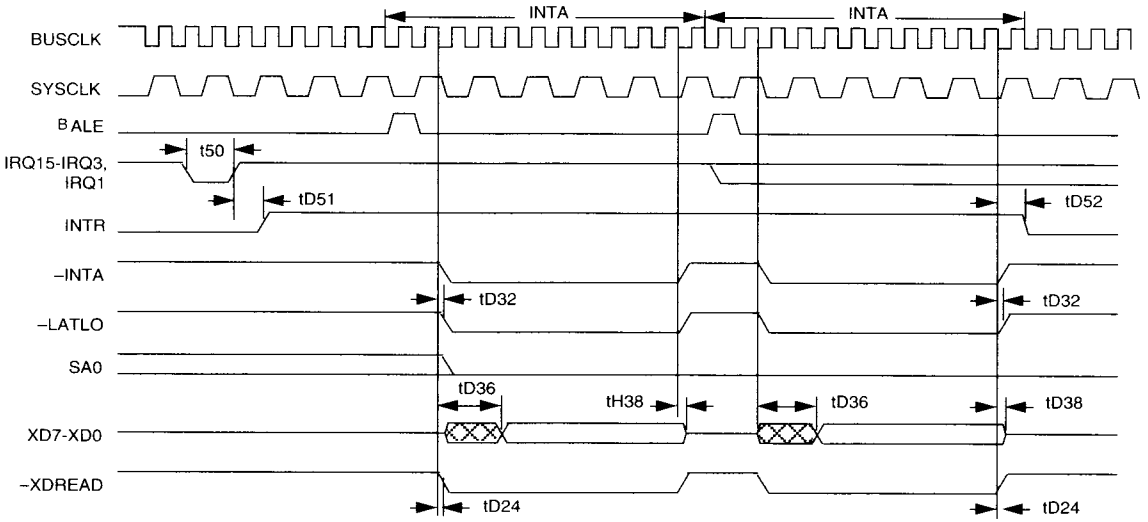
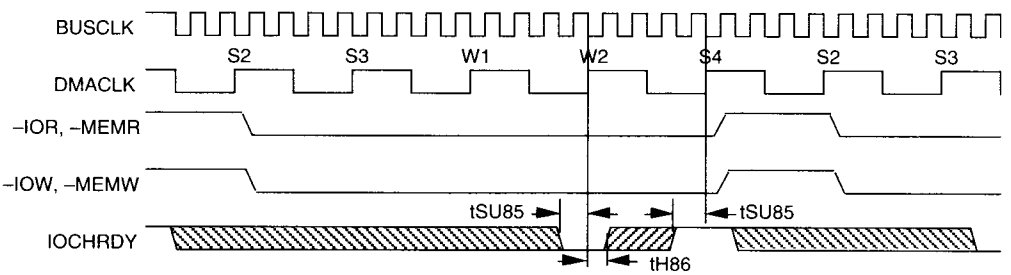


FIGURE 32. IOCHRDY (DMA CYCLES)



Note: The first wait state is automatically inserted by internal circuitry for all DMA cycles. Any additional wait states must be inserted using IOCHRDY.

FIGURE 33. CPU MODE ACCESS (INTERNAL REGISTERS)

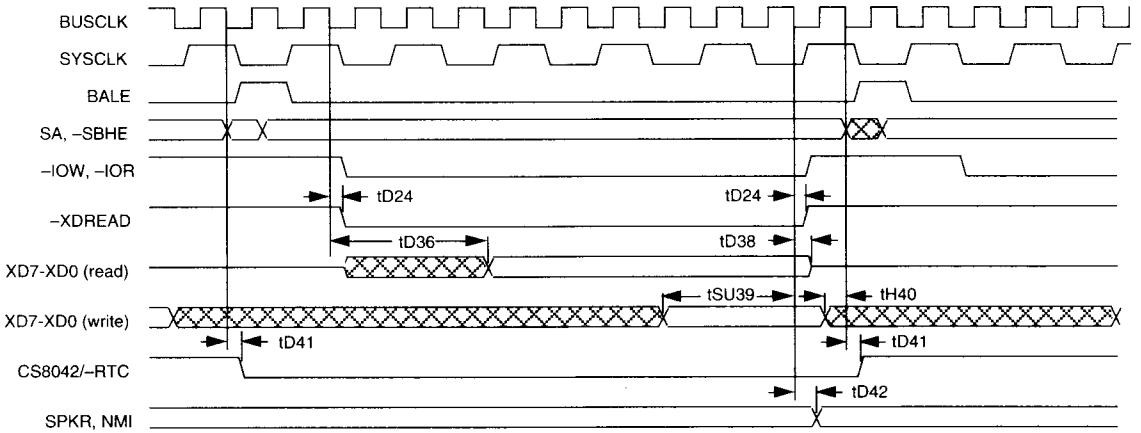


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FIGURE 34. MISCELLANEOUS/PERIPHERAL

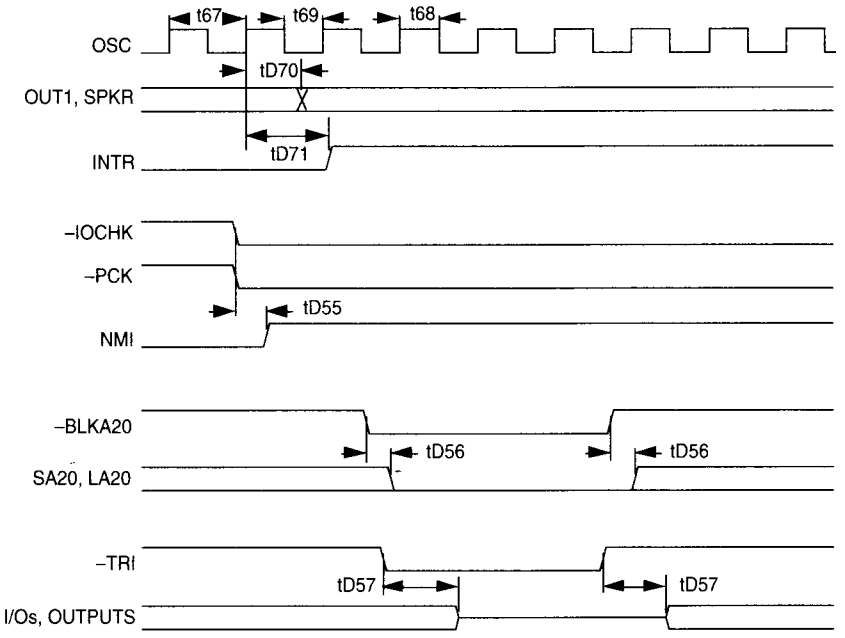
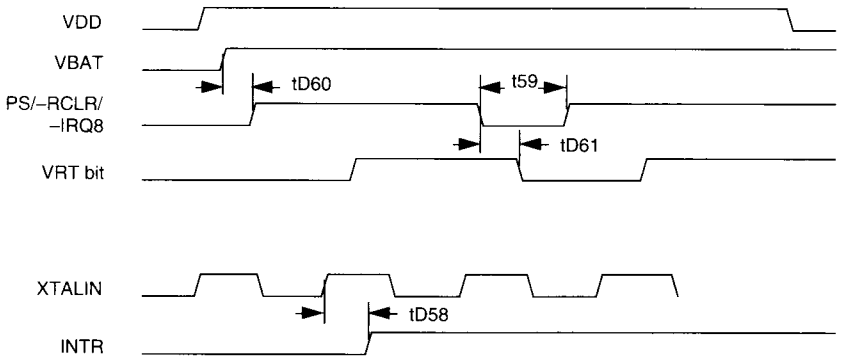


FIGURE 35. RTC INTERFACE



Note: The VRT bit is set to a "1" by reading Register D. The VRT can only be cleared by pulling the PS pin low. (See RTC description, Register D ($0D)).

FIGURE 36. MASTER MODE ACCESS (INTERNAL REGISTERS)

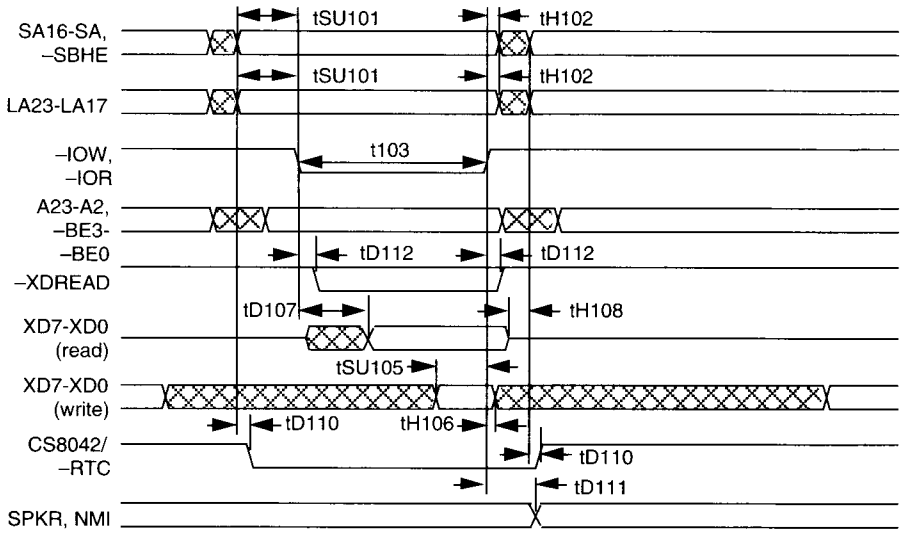


FIGURE 37. DMA MODE DATA STEERING

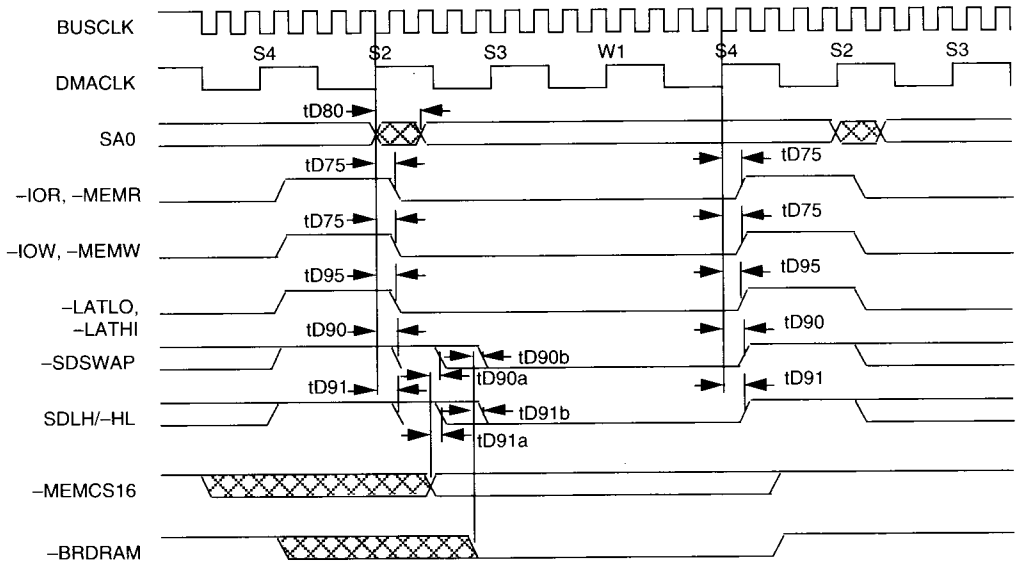
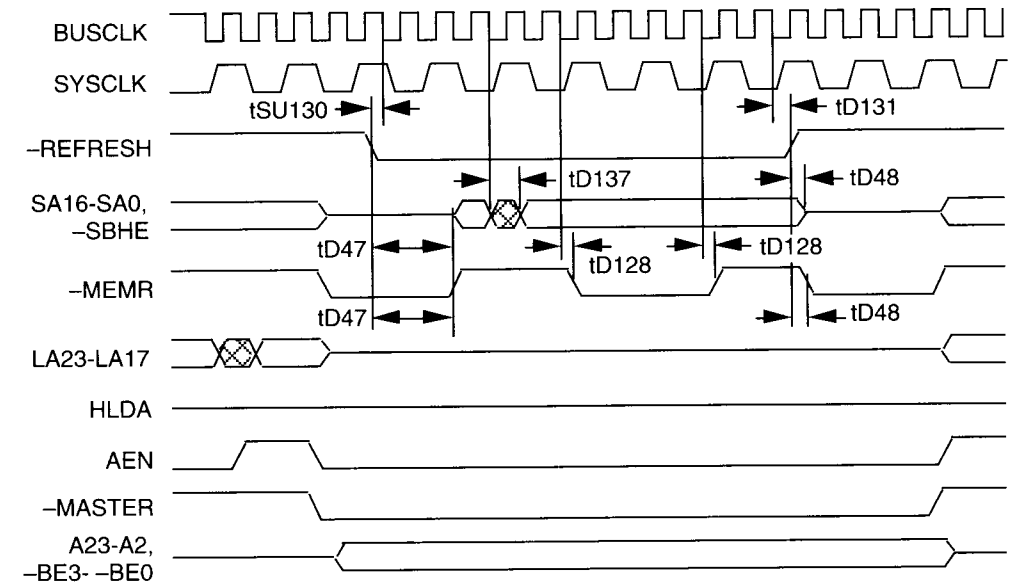


FIGURE 38. MASTER MODE REFRESH



Note: –SMEMR is three-stated for addresses above 1 meg. It should be pulled up externally with a 10k ohm resistor.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground	–0.5 V to 7.0 V
Applied Output Voltage	–0.5 V to VDD + 0.3 V
Applied Input Voltage	–0.5 V to VDD + 0.3 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C TO +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIL	Input Low Voltage	–0.5	0.8	V	TTL Level Inputs
VIH	Input High Voltage	2.0	VDD + 0.5	V	TTL Level Inputs
VILC	Input Low Voltage	–0.5	0.8	V	CMOS Level Inputs
VIHC	Input High Voltage	VDD – 0.8	VDD + 0.5	V	CMOS Level Inputs
VOL1	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOH1	Output High Voltage	VDD – 0.45		V	IOH = 1 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 8 mA, Note 2
VOH2	Output High Voltage	VDD – 0.45		V	IOH = –2 mA, Note 2
VOL3	Output Low Voltage		0.45	V	IOL = 12 mA, –HIDRIVE=1 IOL = 24 mA, –HIDRIVE=0, Note 3
VOH3	Output High Voltage	VDD – 0.45		V	IOH = –6 mA, Note 3
VOL4	Output Low Voltage		0.45	V	IOL = 24 mA, Note 4
ILI	Input Leakage Current	–10	10	µA	Note 5
IIL	Input Leakage Current	–500	–20	µA	Note 6
ILO	Output Leakage Current	–100	100	µA	
IDDSB	Static Power Supply Current		500	µA	
IDDOP	Dynamic Power Supply Current		4	mA/MHz	Based on BUSCLK frequency
IBAT	RTC Power Supply Current		5	µA	At VBAT=2.4 V, 32.768 KHz
IBAT	RTC Power Supply Current		50	µA	At VBAT=5 V, 32.768 KHz
VBAT	RTC Power Supply Voltage	2.4	5.25	V	
CI	Input or I/O Capacitance		10	pF	
CO	Output Capacitance		10	pF	

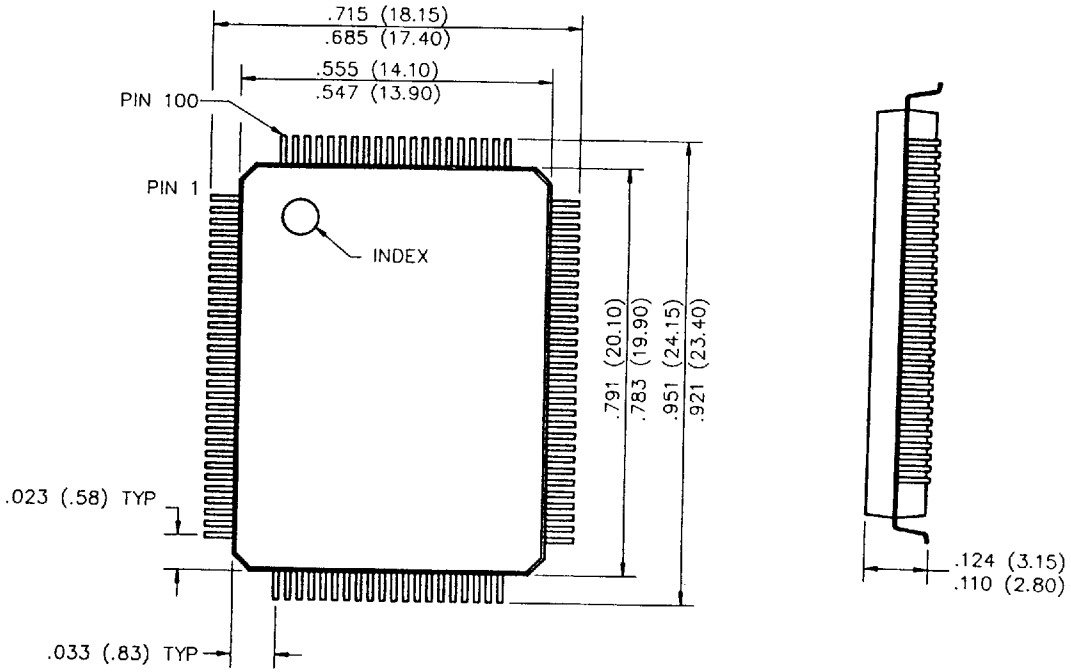
Notes appear on the following page.

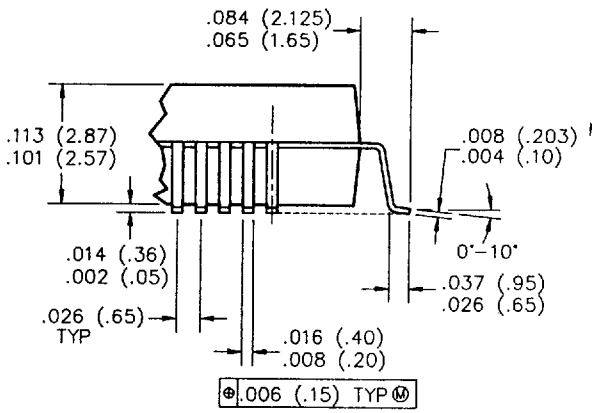
NOTES FOR DC CHARACTERISTICS

Notes:
1. Pins: A25-A2, –BE3- –BE0, XD7-XD0, INTR, NMI, –CHS0, –CHS1, –CHREADY, DMAHRQ, OUT1, –SDSWAP, SDLH/–HL, –XDREAD, SPKR, –CS8042
2. Pins: –DACK7- –DACK0, T/C, –LATLO, –LATHI
3. Pins: SA19-SA0, LA23-LA17, –IOW, –IOR, –MEMW, –MEMR, –SBHE, RSTDRV, –SMEMW, –SMEMR, SYSCLK, AEN, BALE
4. Pins: –REFRESH
5. All inputs except those listed in Note 6.
6. Pins: IRQ15-IRQ9, IRQ7-IRQ3, IRQ1, DRQ7-DRQ5, DRQ3-DRQ0, –BE3, C286/–386, –EALE, –PCK, –ROM8, –HIDRIVE, –TRI, POWERGOOD, PS/–RCLR/–IRQ8

100-PIN PLASTIC QUAD FLAT PACK

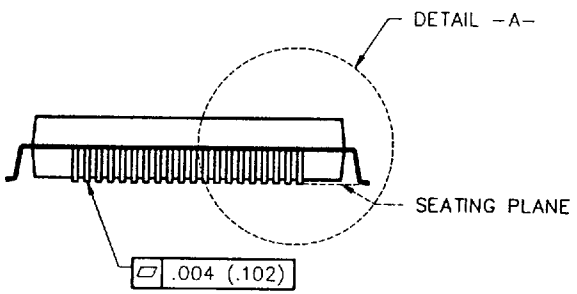
V L S I TECHNOLOGY INC





DETAIL –A–

NOTES:
1. CONTROLLING DIMENSION IS MM.



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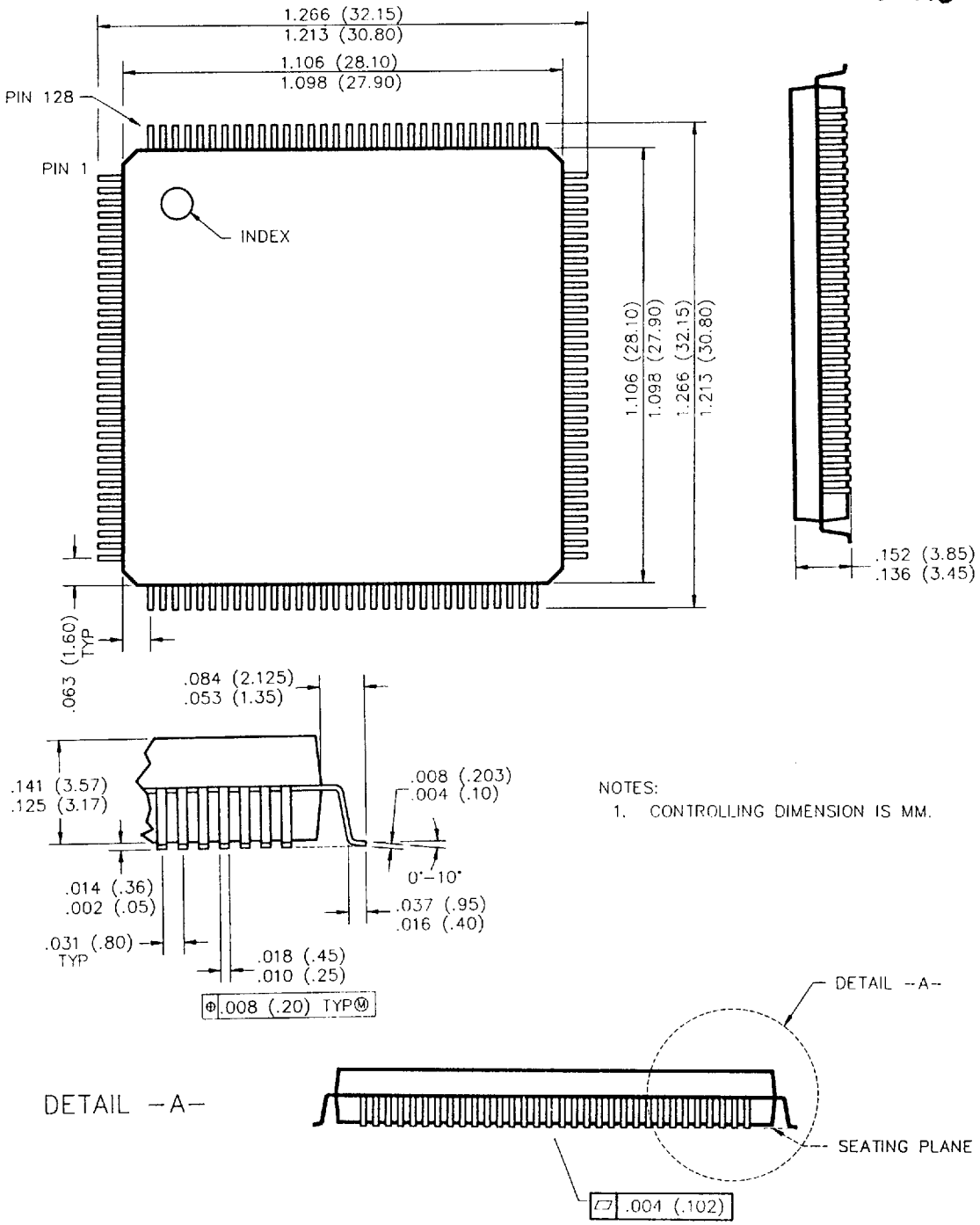
128-PIN PLASTIC FLAT PACK

V L S I TECHNOLOGY INC T-90-20

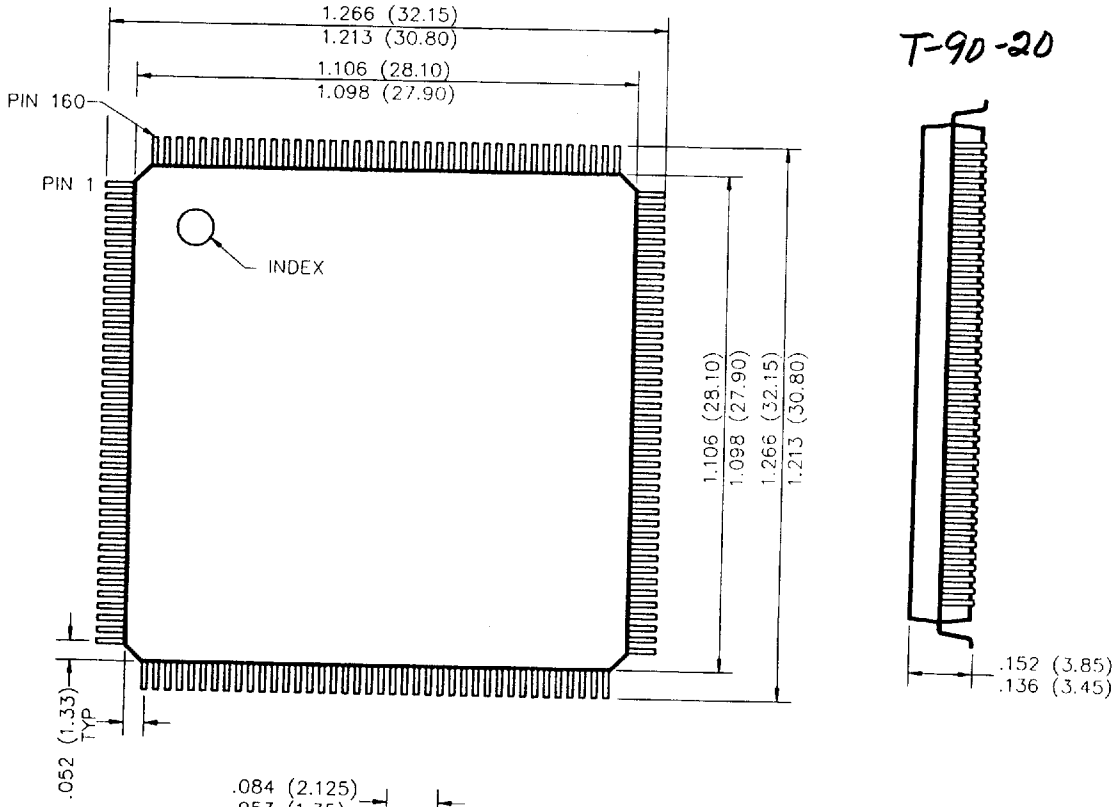


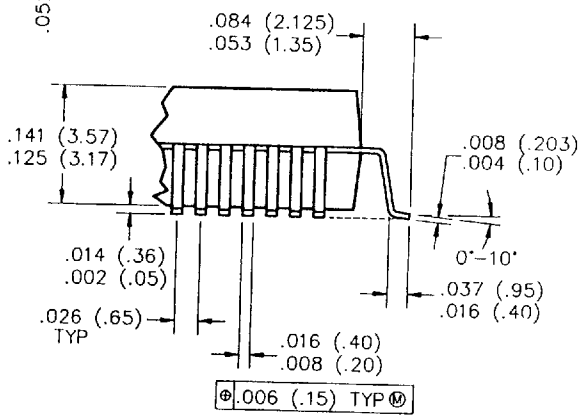
NOTES:
1. CONTROLLING DIMENSION IS MM.

160-PIN PLASTIC QUAD FLAT PACK

V L S I TECHNOLOGY INC

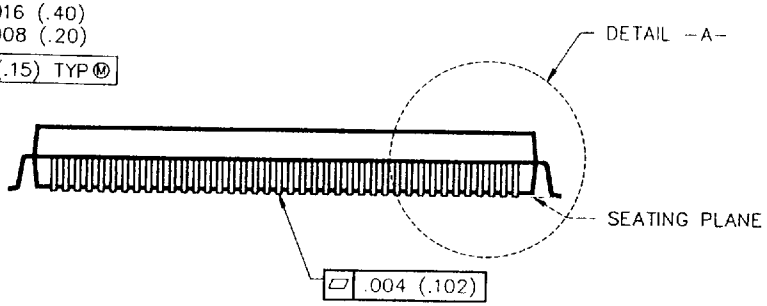
T-90-20





NOTES:
1. CONTROLLING DIMENSION IS MM.

DETAIL –A–



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