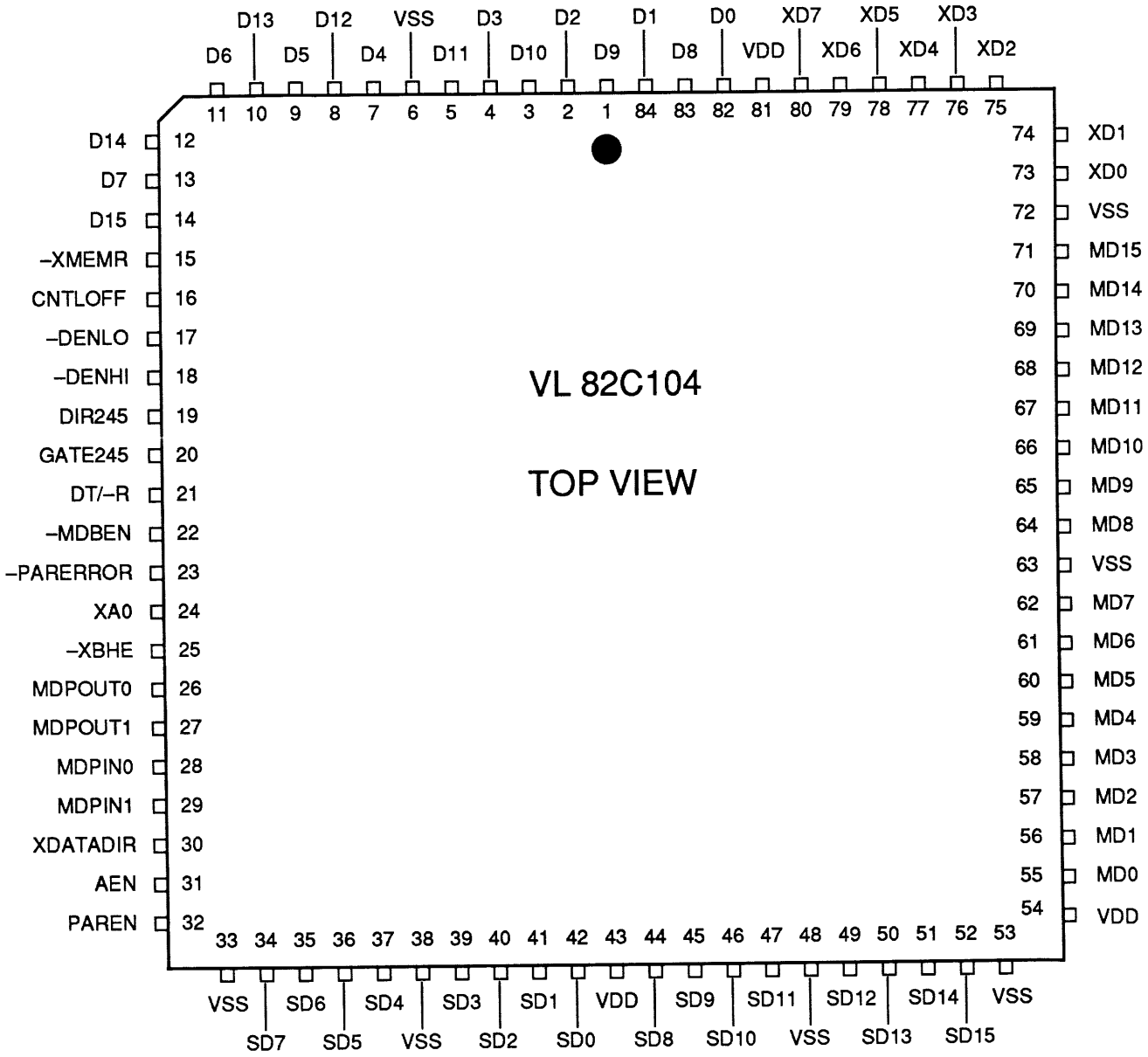
PIN DIAGRAM


VL 82C104
TOP VIEW
1 D6
2 D5
3 D4
4 D11
5 D10
6 D9
7 D8
8 VDD
9 XD6
10 XD4
11 XD2
12 XD3
13 XD5
14 XD7
15 D0
16 D1
17 D2
18 D3
19 VSS
20 D12
21 D13
22 D14
23 D7
24 D15
25 -XMEMR
26 CNTLOFF
27 -DENLO
28 -DENHI
29 DIR245
30 GATE245
31 DT/-R
32 -MDBEN
33 -PARERROR
34 XA0
35 -XBHE
36 MDPOUT0
37 MDPOUT1
38 MDPIN0
39 MDPIN1
40 XDATADIR
41 AEN
42 PAREN
43 VSS
44 SD7
45 SD6
46 SD5
47 SD4
48 VSS
49 SD3
50 SD2
51 SD1
52 SD0
53 VDD
54 SD8
55 SD9
56 SD10
57 SD11
58 VSS
59 SD12
60 SD13
61 SD14
62 SD15
63 VSS
64 VDD
65 MD0
66 MD1
67 MD2
68 MD3
69 MD4
70 MD5
71 MD6
72 MD7
73 MD8
74 MD9
75 MD10
76 MD11
77 MD12
78 MD13
79 MD14
80 MD15
81 VSS
82 XD0
83 XD1

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CNTLOFF	16	I	CNTLOFF - This input is used as a clock to latch the current data on the low byte of the system data bus. Data is latched on the rising edge of CNTLOFF and is independent of the status of DT/–R, XA0, or –DENLO.
DT/–R	21	I	Data Transmit (high)/Receive (low) - This input is a signal from the 82C288. It establishes the direction of data flow to or from the system data bus.
–DENLO	17	I	Data Enable Low - An active low input that enables a low byte data transfer on the CPU data bus low byte transceiver.
XA0	24	I	Peripheral Address Bus Bit 0 - This is the LSB of the peripheral address bus. The signal is used throughout the system to indicate low or high byte data transfers. It is used to enable the low byte memory data transceiver and to select latched or immediate data out of the CPU low byte bus transceiver. It is also used to enable low byte parity checking.
–MDBEN	22	I	Memory Data Bus Enable - An active low input that is used to set the direction of the memory data bus transceiver. –MDBEN = 0 indicates a memory write cycle while –MDBEN = 1 is a memory read cycle.
XDATADIR	30	I	Transceiver Data Direction - This input is used to select the direction of the peripheral data bus transceiver. XDATADIR = 0 indicates a DMA write to the system data bus while XDATADIR = 1 is used for a DMA read from the system data bus.
AEN	31	I	Address Enable - An active high input that is used to disable the DMA data bus transceiver while the DMA controller is using the peripheral data bus for address information.
DIR245	19	I	Direction 245 - An input control signal used to set the direction of the high/low system data bus transceiver. This is used for high to low, or low to high data byte moves.
GATE245	20	I	Gate 245 - An active low input that enables the high/low system data transceiver.
–DENHI	18	I	Data Enable High - An active low input that enables a high byte data transfer on the CPU data bus high byte transceiver.
–XBHE	25	I	Transfer Bus High Enable - An active low that indicates a transfer of data on the upper byte of the memory data bus. It is used to enable the high byte memory data tranceiver and to enable high byte parity checking.
–XMEMR	15	I	Memory Read Enable - An active low input signal that indicates when a memory read cycle is occurring. It is used to disable the MDPOUTx signals during a memory write and to latch in the detected parity error signal during a memory read.
MDPOUT0	26	I	Memory Data Parity Out 0 - An active high input that is the output of the stored memory parity data. It is checked for parity errors with the low byte of data read from memory.
MDPOUT1	27	I	Memory Data Parity Out 1 - An active high input that is the output of the stored memory parity data. It is checked for parity errors with the high byte of data read from memory.
MDPIN0	28	O	Memory Data Parity In 0 - An active high output that is the parity input to the system board memory. It is generated from the current low byte data on the memory data bus.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MDPIN1	29	O	Memory Data Parity In 1 - An active high output that is the parity input to the system board memory. It is generated from the current high byte data on the memory data bus.
PAREN	32	I	Parity Enable - This active high input is used to enable the parity data latch. It is used to prevent false parity errors when ROM memory access occur.
–PARERROR	23	O	Parity Error - An active low output that is used to indicate that a memory parity error has occurred. This signal is latched by –XMEMR and is valid until the next memory access.
MD0-MD15	55-62, 64-71	I/O	DRAM Memory Data bus bits 0-15 - These are I/O signals.
XD0-XD7	73-80	I/O	Peripheral Data Bus Bits 0-7 - I/O's used to control the coprocessor, keyboard, ROM memory and the DMA controllers.
D0-D15	82, 84, 2, 4, 7, 9,11,13 83,1, 3, 5, 8 10,12,14	I/O	CPU Data Bus Bits 0-15 - This is a bidirectional bus controlled by the DT/–R input.
SD0-SD15	42-39, 37-34 44-47, 49-52	I/O	System Data Bus Bits 0-15 - These are I/O signals.
VDD	43, 54, 81		System Power: 5 V
VSS	6, 33, 38, 48 53, 63, 72		System Ground

FUNCTIONAL DESCRIPTION

The VL82C104 is part of a five chip set which together perform all of the on-board logic required to construct an IBM PC/AT-compatible system. The PC/AT-Compatible Data Buffer replaces several bus transceivers and a CPU lower byte data latch located within the PC/AT-type system.

The primary function of the Data Buffer is to multiplex the 80286 microprocessor data lines D0-D15 to the system data bus SD0-SD15, the peripheral data bus XD-XD17 and the memory data bus MD0-MD15. This is accomplished through six sets of 8-bit wide data multiplexors. The lower data byte of the CPU data bus transceiver has a byte wide register which is clocked by the rising edge of CNTLOFF. The data is latched in the direction from the System Data Bus to the CPU Data bus only. XA0 is used to control data flow to the CPU Data Bus. When XA0 = 0, real time data is passed to the CPU data bus. When XA0 = 1, latched data is passed to the CPU Data Bus. The six groups of transceivers can be seen in the block diagram of the device. The data parity encoder/decoder logic is also located within this device. All data present upon the memory data bus passes through the parity logic. The outputs of the parity encoder/decoders, MDPIN0 and MDPIN1, are enabled via PAREN to prevent decoding a ROM access and are gated with –XMEMR. The –PARERROR signal is fed back to the Memory Controller chip where it is gated with other logic to produce the NMI signal for the 80286.

The logic controlling the bus transceivers has been optimized for speed and as such there are no provisions to prevent internal bus collisions. In a standard PC/AT type application using the full VL82CPCAT chip set this is not a problem as the control signals which enable the transceivers are decoded in such a fashion as to prevent this from happening. In the case where only the VL82C104 is used care must be taken as to ensure that the control signals will not cause an internal bus collision. From the block diagram it can be seen that every bus transceiver has an A and B I/O port. The DIR input to the transceiver controls the direction of data flow through the transceiver. A high (1) input into the DIR pin causes data to flow from A to B. A low (0) causes data to flow from B to A. All transceiver enables are low true causing the output of the particular transceiver to be active.

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

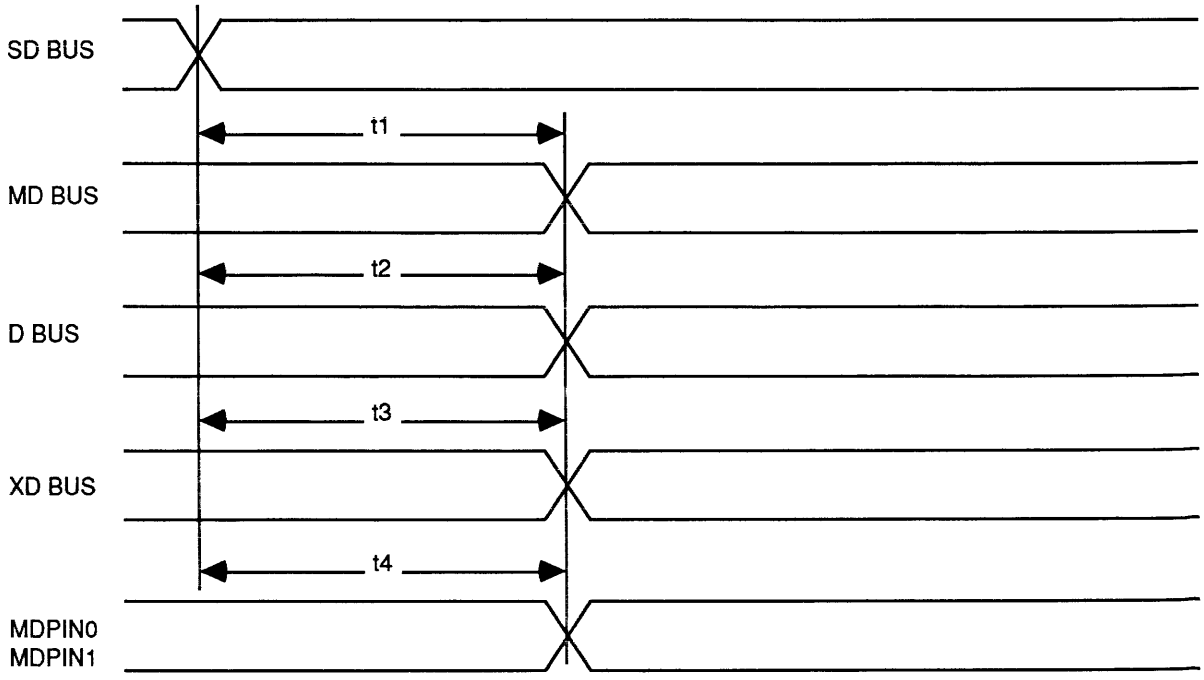
DATA BUS I/O MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t1	SD Bus In to MD Bus Out		40	ns	CL = 100 pF
t2	SD Bus In to D Bus Out		40	ns	CL = 50 pF
t3	SD Bus In to XD Bus Out		40	ns	CL = 100 pF
t4	SD Bus In to MDPIN0 and MDPIN1 Out		55	ns	CL = 50 pF
t5	D Bus In to MD Bus Out		30	ns	CL = 100 pF
t6	D Bus In to SD Bus Out		35	ns	CL = 200 pF
t7	D Bus In to XD Bus Out		30	ns	CL = 100 pF
t8	D Bus In to MDPIN0 and MDPIN1 Out		55	ns	CL = 50 pF
t9	MD Bus In to D Bus Out		19	ns	CL = 50 pF
t10	MD Bus In to SD Bus Out		35	ns	CL = 200 pF
t11	MD Bus In to XD Bus Out		30	ns	CL = 100 pF
t12	XD Bus In to D Bus Out		50	ns	CL = 50 pF
t13	XD Bus In to SD Bus Out		50	ns	CL = 200 pF
t14	XD Bus In to MD Bus Out		50	ns	CL = 100 pF
t15	XD Bus In to MDPIN0, MDPIN1 Out		45	ns	CL = 50 pF, Note

Note: This function is not available in a standard PC/AT system. It is specified here because the system can be configured to accommodate this function, although it is not tested for.

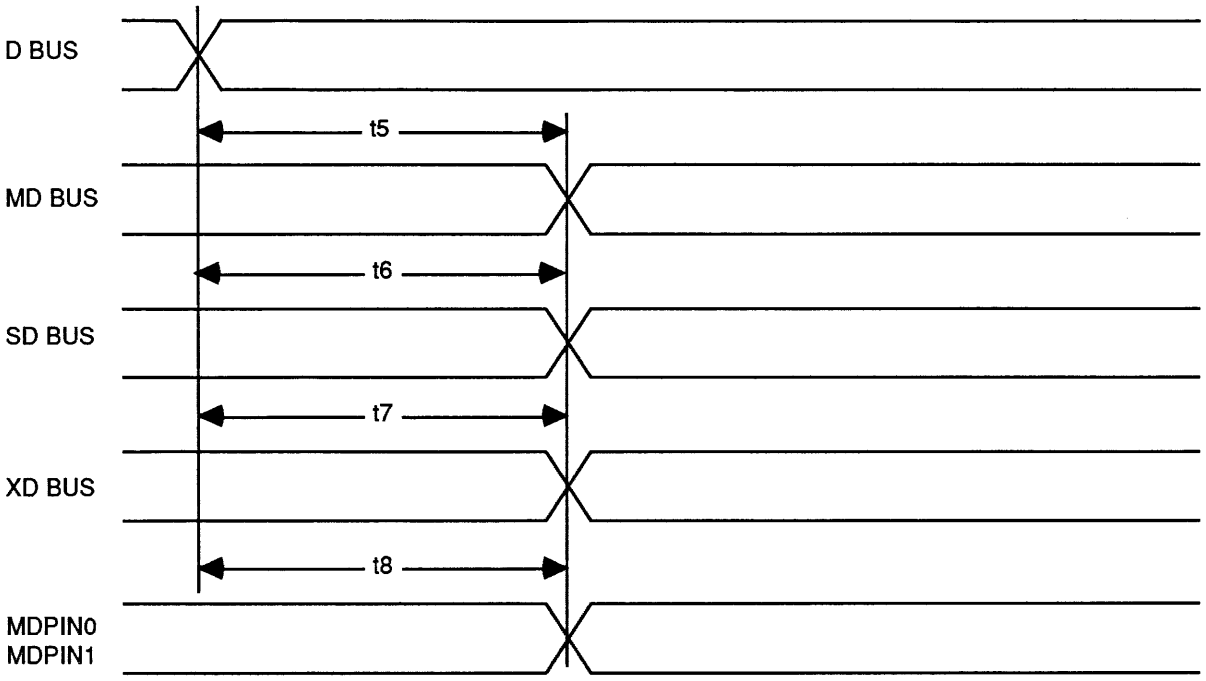
DATA BUS I/O MODE TIMING WAVEFORMS

System Data Bus Timing Waveform

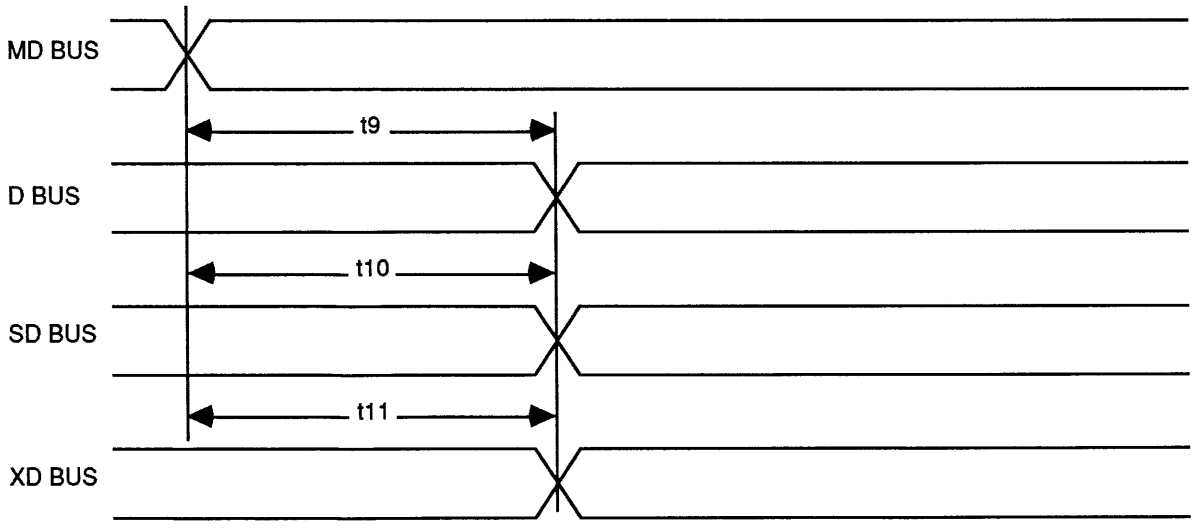


DATA BUS I/O MODE TIMING WAVEFORMS (Cont.)

CPU Data Bus Input Timing Waveform

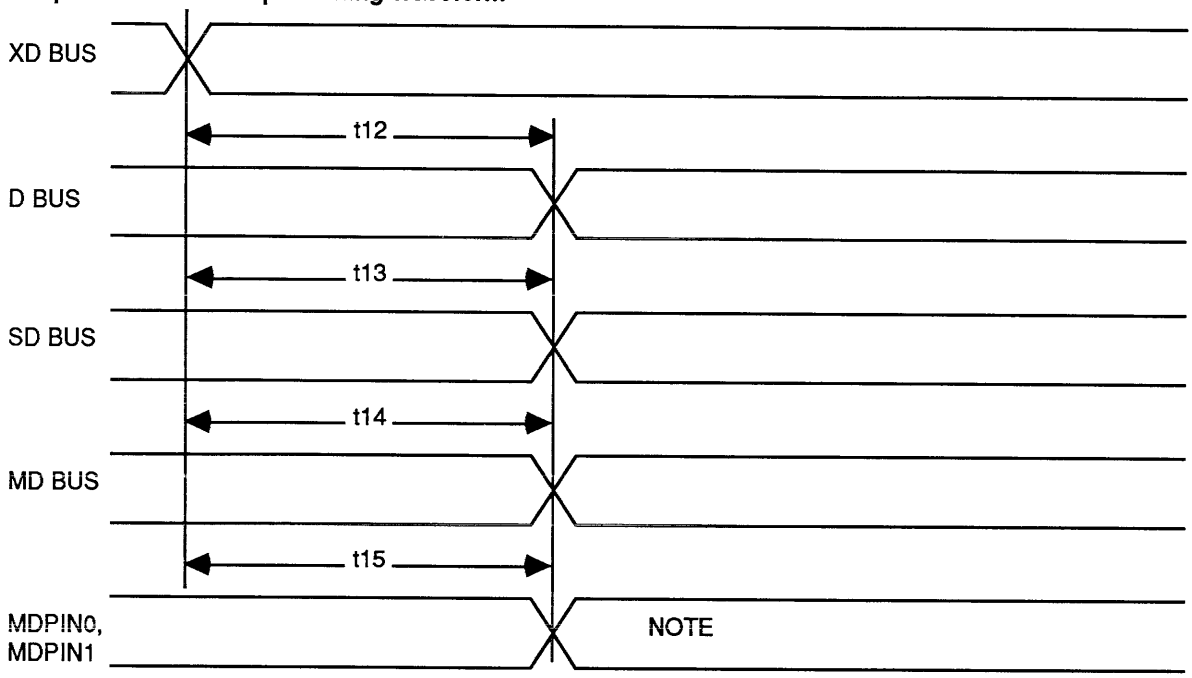


Memory Data Bus Input Timing Waveform



DATA BUS I/O MODE TIMING WAVEFORMS (Cont.)

Peripheral Data Bus Input Timing Waveform

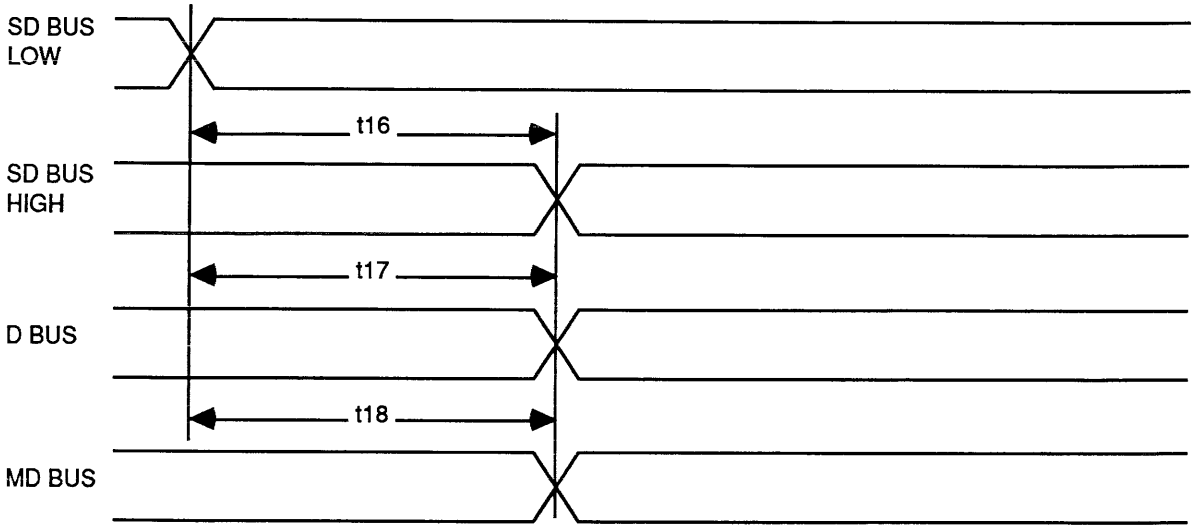


Note: This function is not available in a standard PC/AT system. It is specified here because the system can be configured to accommodate this function, although it is not tested for.

LOW BYTE TO HIGH BYTE CONVERSION MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t16	SD Low to SD High Data Out		55	ns	CL = 200 pF
t17	SD Low to D Bus High Data Out		45	ns	CL = 50 pF
t18	SD Low to MD Bus High Data Out		45	ns	CL = 100 pF

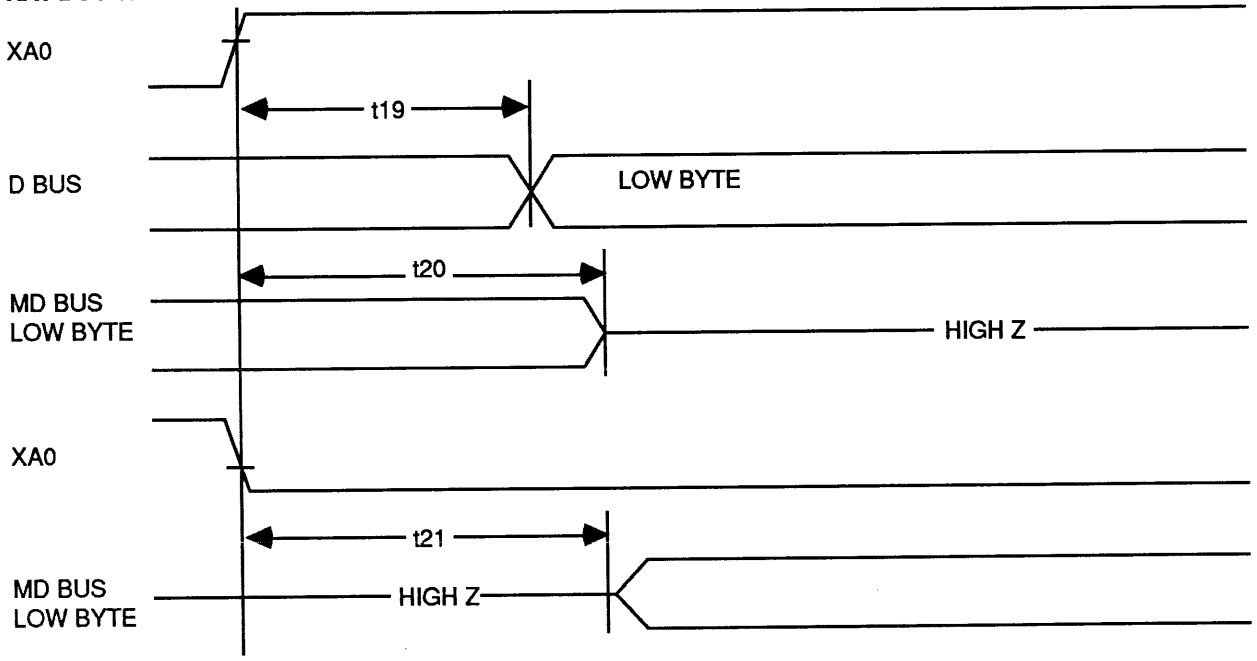
LOW BYTE TO HIGH BYTE CONVERSION TIMING WAVEFORM



XA0 BUS MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t19	XA0 to D Bus Data Out		30	ns	CL = 50 pF
t20	XA0 to MD Bus Low Byte Out to High Z		35	ns	
t21	XA0 to MD Bus Low Byte Out from High Z		35	ns	

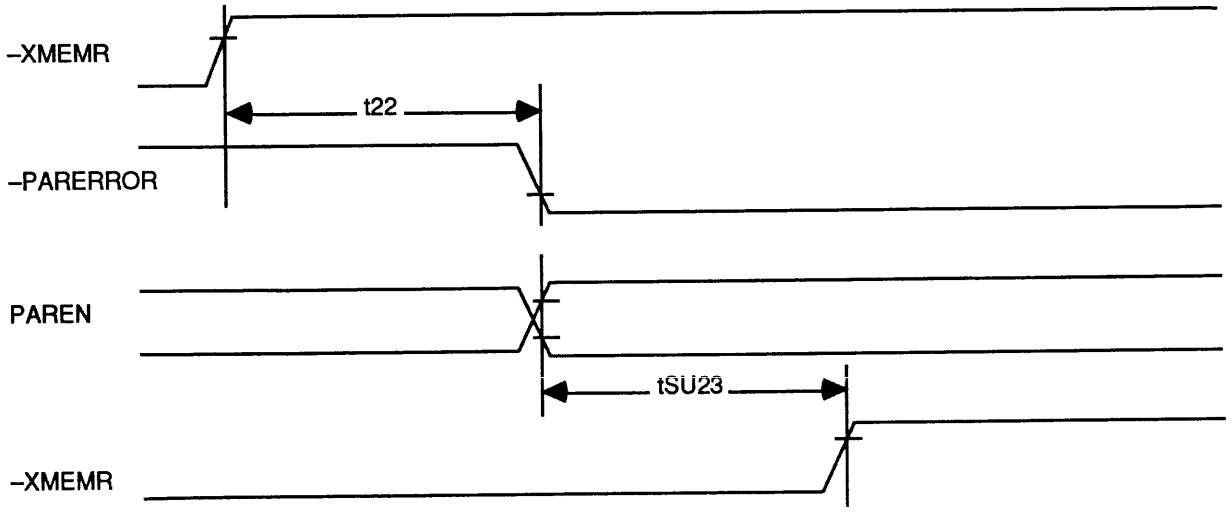
XA0 BUS TIMING WAVEFORM



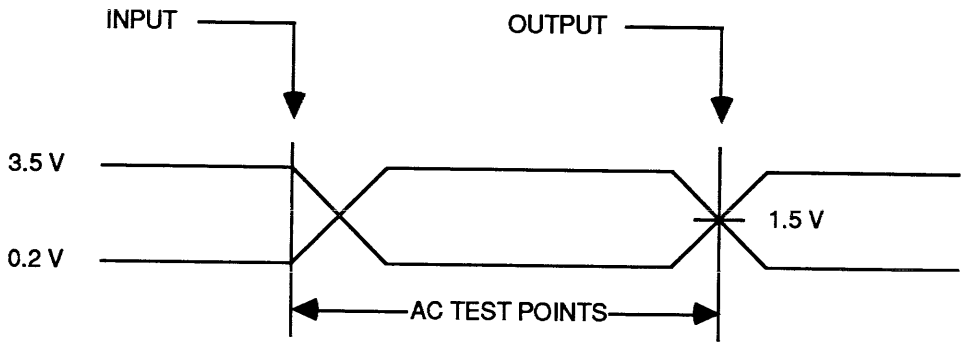
MEMORY READ MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t22	–XMEMR High to –PARERROR Out		25	ns	CL = 50 pF
tSU23	Setup PAREN to –XMEMR High	15		ns	

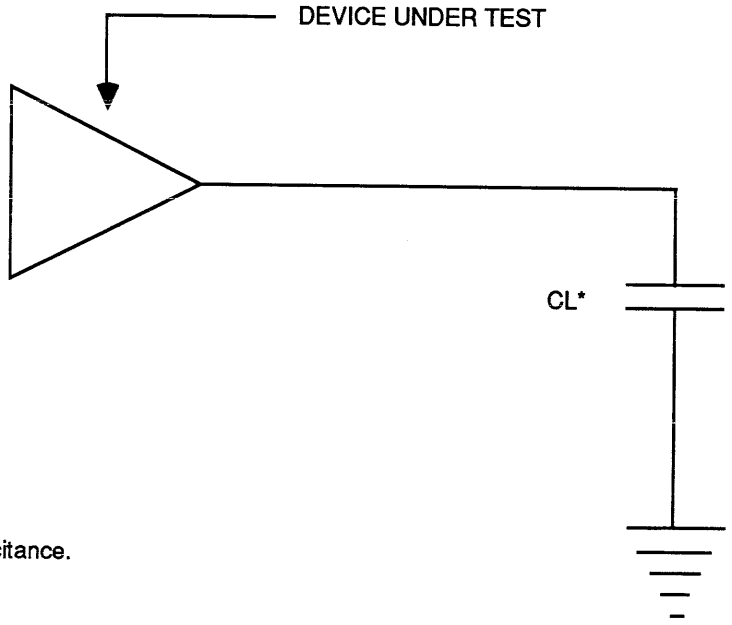
MEMORY READ MODE TIMING WAVEFORM



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
34-37, 39-42, 44-47, 49-52	200
55-62, 64-71, 73-80	100
1-5, 7-14, 23, 28-29	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5.0 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	IOL = 8 mA, Notes 1 & 3
VOL2	Output Low Voltage		0.45	V	IOL = 20 mA, Notes 2 & 3
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIHC	Input High Voltage	3.8	VDD + 0.5	V	CNTLOFF
VILC	Input Low Voltage	–0.5	0.6	V	CNTLOFF
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		100	mA	

Notes: 1. Pins 55-62, 64-71, and 73-80.
2. Pins 34-37, 39-42, 44-47, and 49-52.
3. Output low current on all other outputs not mentioned in Note 1 or 2 have IOL (max) = 2 mA.

VL82C104

PC/AT-COMPATIBLE DATA BUFFER

FEATURES

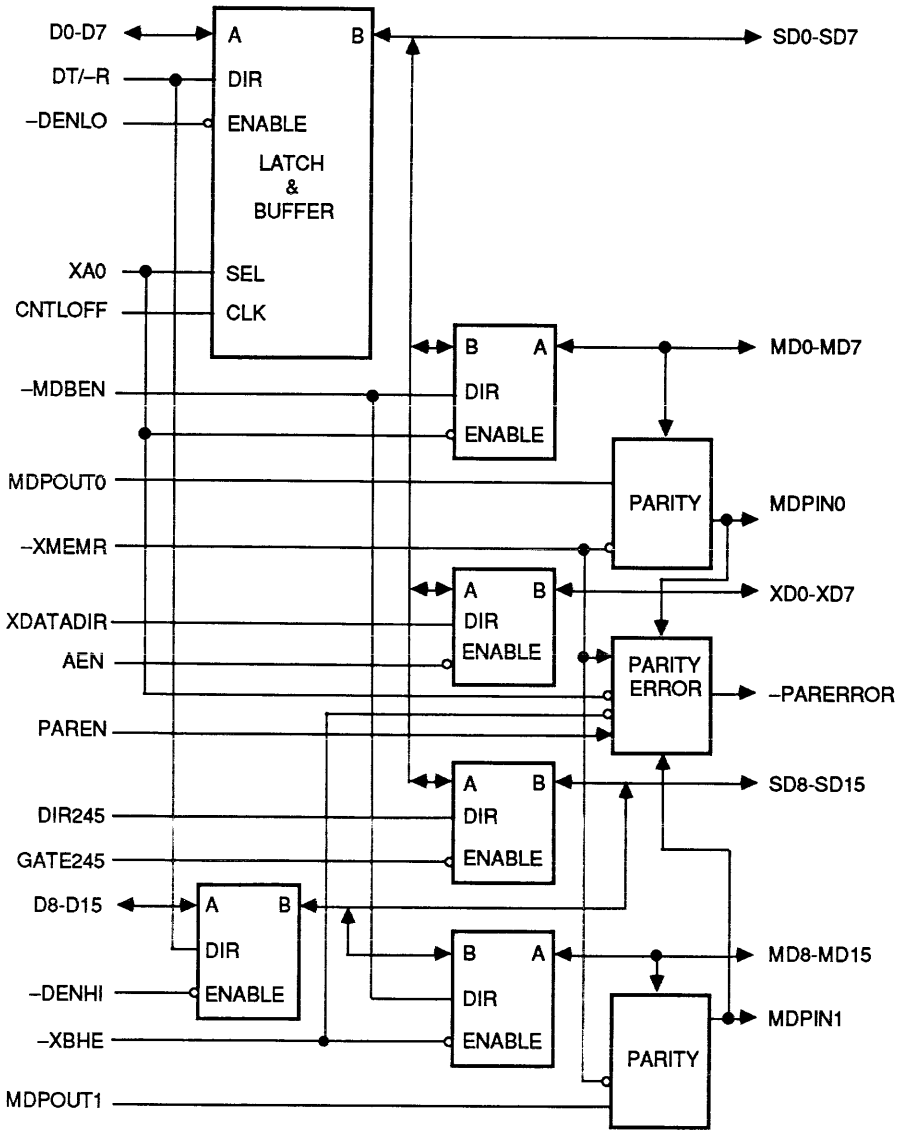
- Fully compatible with IBM PC/AT-type designs
- Completely performs data buffer function in IBM PC/AT-compatible systems
- Replaces several buffers, latches and other logic devices
- Supports up to 12 MHz system clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C104 PC/AT-Compatible Data Buffer provides a 16-bit CPU data bus I/O as well as 40 buffered drivers. The buffered drivers consist of 16 bidirectional system data bus drivers, each capable of sinking 20 mA (50 'LS loads) of current; eight bidirectional peripheral bus drivers, each capable of sinking 8 mA (20 'LS loads) of current; and 16 memory data bus drivers, each capable of sinking 8 mA (20 'LS loads) of current. The VL82C104 also generates the parity error signal for the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C104 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C104-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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