VL82C100

PC/AT-COMPATIBLE PERIPHERAL CONTROLLER

FEATURES

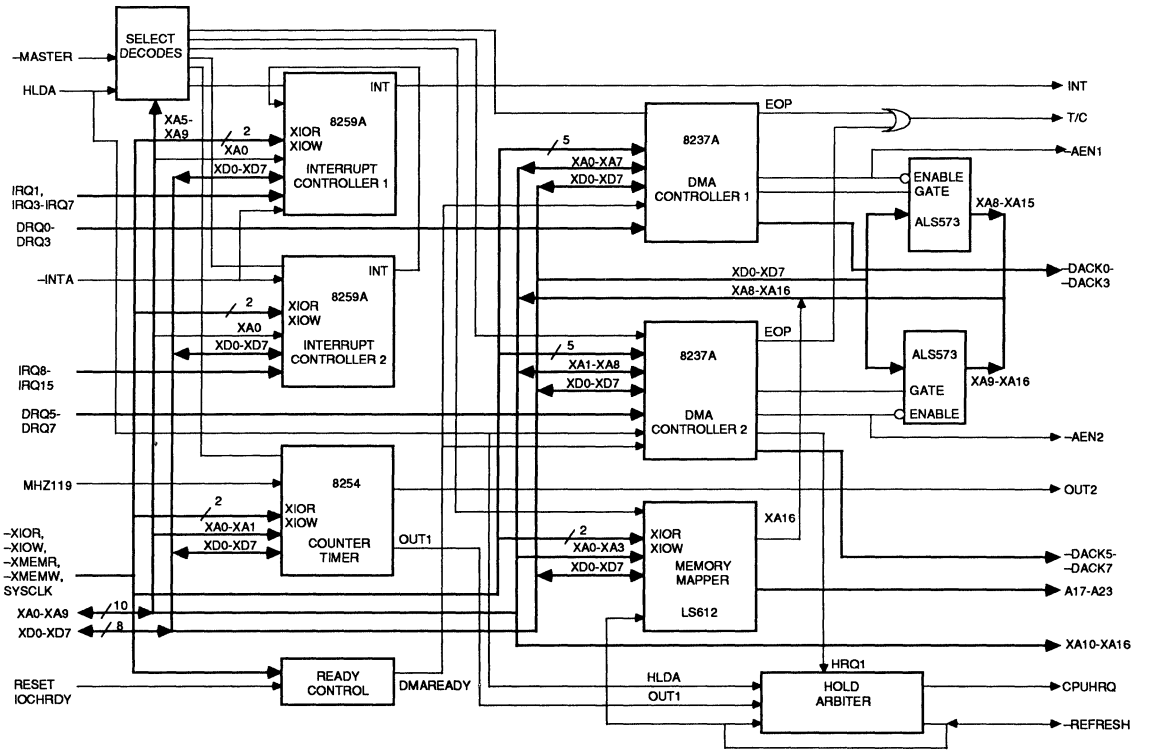
- Fully compatible with IBM PC/AT-type designs
- Replaces 19 logic devices
- Supports up to 20 MHz system clock
- Device is available as "cores" for user-specific designs
- Seven DMA channels
- 14 external interrupt requests
- Three timer/counter channels
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C100 PC/AT-Compatible Peripheral Controller replaces two 82C37A Direct Memory Access Controllers, two 82C59A Interrupt Controllers, an 82C54 Programmable Counter, a 74LS612 AT Memory Mapper, two 74ALS573 Octal Three-State Latches, a 74ALS138 3-to-8 Decoder, and five other less-complex integrated circuits. Using this internal functionality, the VL82C100 provides all 24 address bits for 16M bits of DMA address space. It also interfaces directly to the CPU to handle all interrupts. Timing for refresh cycles, and arbitration, between refresh and DMA hold requests, are also controlled by the VL82C100.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C100 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM

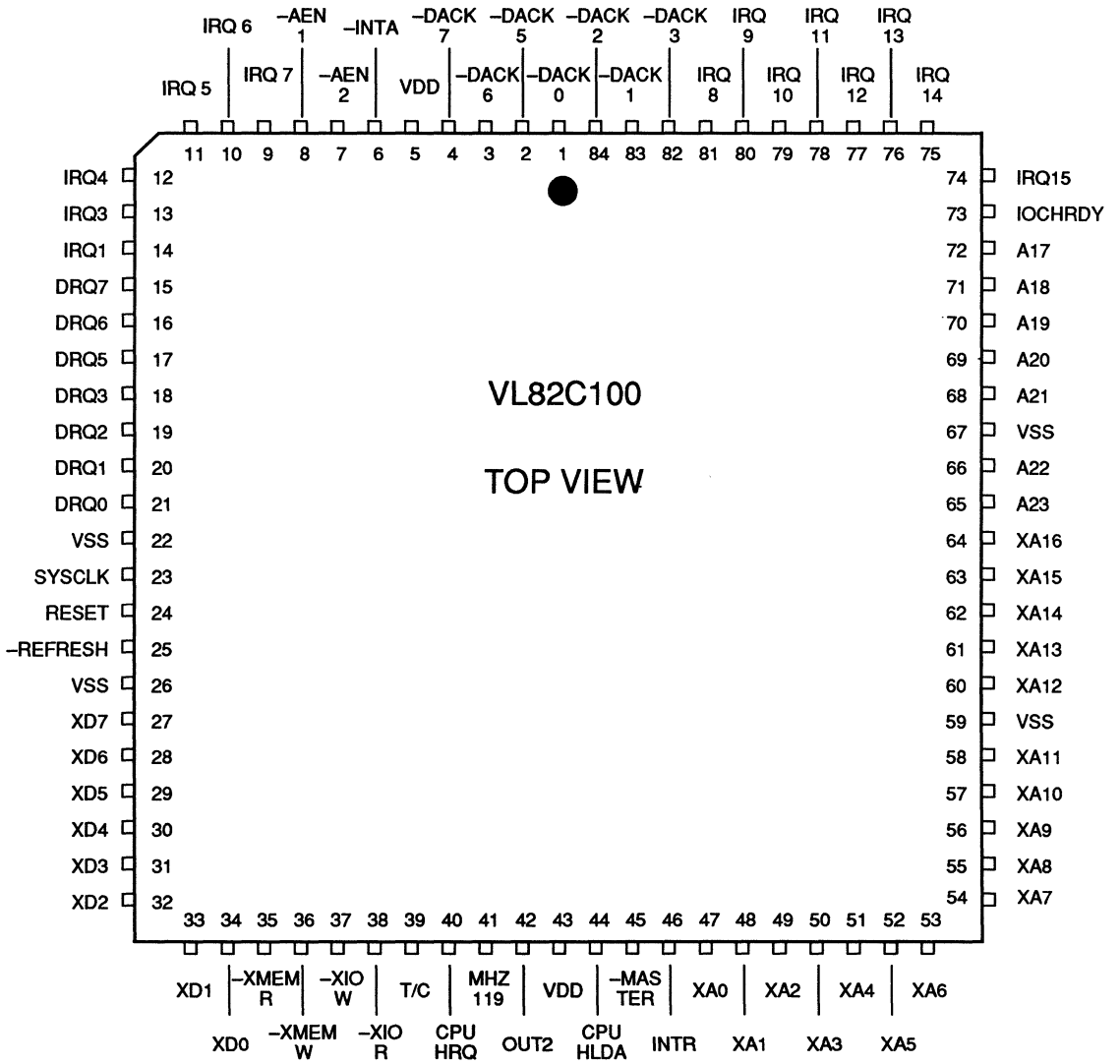


ORDER INFORMATION

Part Number	Clock Freq.	Package
VL82C100-QC VL82C100-QI	12/16 MHz	Plastic Leaded Chip Carrier (PLCC)
VL82C100-20QC VL82C100-20QI	20 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range:
QC = 0°C to +70°C
QI = –40°C to +85°C.

PIN DIAGRAM


VL82C100
TOP VIEW
11 IRQ 6
10 IRQ 5
9 IRQ 7
8 -AEN 1
7 -AEN 2
6 -INTA
5 VDD
4 -DACK 7
3 -DACK 6
2 -DACK 5
1 -DACK 0
84 -DACK 2
83 -DACK 1
82 -DACK 3
81 IRQ 8
80 IRQ 9
79 IRQ 10
78 IRQ 11
77 IRQ 12
76 IRQ 13
75 IRQ 14
12 IRQ4
13 IRQ3
14 IRQ1
15 DRQ7
16 DRQ6
17 DRQ5
18 DRQ3
19 DRQ2
20 DRQ1
21 DRQ0
22 VSS
23 SYSCLK
24 RESET
25 -REFRESH
26 VSS
27 XD7
28 XD6
29 XD5
30 XD4
31 XD3
32 XD2
74 IRQ15
73 IOCHRDY
72 A17
71 A18
70 A19
69 A20
68 A21
67 VSS
66 A22
65 A23
64 XA16
63 XA15
62 XA14
61 XA13
60 XA12
59 VSS
58 XA11
57 XA10
56 XA9
55 XA8
54 XA7
33 XD1
34 XD0
35 -XMEM R
36 -XMEM W
37 -XIO W
38 -XIO R
39 T/C
40 CPU HRQ
41 MHZ 119
42 OUT2
43 VDD
44 CPU HLDA
45 -MAS TER
46 INTR
47 XA0
48 XA1
49 XA2
50 XA3
51 XA4
52 XA5
53 XA6

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
SYSCLK	23	I	System Clock Input - This pin is divided by two internally to generate DMACLK for the 8237 DMA controllers. It is also used in the hold request arbiter. SYSCLK can be driven at a frequency of up to 20 MHz.
RESET	24	I	Reset - An active high input used to clear the DMA controller megacells and hold request arbiter.
XD0-XD7	34-27	I/O	Peripheral Data Bus Bits 0-7 - These lines are three-state bidirectional signals connected to the peripheral data bus. (X data bus in PC/AT-type designs.)
XA0-XA9	47-56	I/O	Peripheral Address Bus Bits 0-9 - The ten least significant address bits on the XA bus are bidirectional. They are outputs during DMA cycles and are inputs all other times. As inputs they are used to generate chip selects for the megacells and address internal registers within each megacell.
XA10, XA11 XA12-XA16	57, 58 60-64	O	Peripheral Address Bus Bits 10-16 - The seven most significant address bits on the XA bus are three-state outputs only. They actively drive the XA bus during DMA cycles.
A17-A21 A22, A23	72-68 66, 65	O	CPU Address Bus Bits 17-23 - These address bits are connected to the CPU's address bus and are driven from the LS612 memory mapper any time CPUHLDA is active (high) and –MASTER is inactive (high). They are in a three-state condition during all other times.
–XIOW	37	I/O	I/O Write – This is a bidirectional active low three-state line. It is an output during a DMA cycle and will be an input at all other times.
–XIOR	38	I/O	I/O Read - This is a bidirectional active low three-state line. It is an output during a DMA cycle and will be an input at all other times.
–XMEMW	36	I/O	Memory Write - This is a bidirectional active low three-state line. It is an output during a DMA cycle and will be an input at all other times. In the input mode –XMEMW is used to enable the hold request arbiter after an interrupt acknowledge cycle.
–XMEMR	35	O	Memory Read - This is a three-state output which will be active during a DMA cycle.
IRQ1, IRQ3-IRQ7 IRQ8-IRQ15	14, 13-9, 81-74	I	Interrupt Request Bits 1, 3-7, 8-15 - These are asynchronous inputs and are the interrupt request inputs to the 8259 megacells. IRQ2 and IRQ0 are not available as inputs to the chip. IRQ2 is used to cascade the two 8259's together and IRQ0 is connected to the output of the 8254 counter 0.
INTR	46	O	Interrupt Request - INTR is an output used to interrupt the CPU and is generated whenever a valid IRQ is received.
–INTA	6	I	Interrupt Acknowledge - This input is used to enable the 8259 interrupt controllers to vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
DRQ0-DRQ3 DRQ5-DRQ7	21-18 17-15	I	DMA Request Bits 0-3, 5-7 - These input signals are the individual asynchronous requests for DMA service connected to the 8237 megacells. DRQ0 through DRQ3 support transfers from 8 bit I/O adapters to/from 8 or 16 bit system memory. DRQ5 through DRQ7 support transfers from 16 bit I/O adapters to/from 16 bit system memory. DRQ4 is not available as it is used to cascade the two DMA controllers together.
–DACK0- –DACK3 –DACK5- –DACK7	1, 83, 84, 82, 2-4	O	DMA Acknowledge Bits 0-3, 5-7 - These output signals are the acknowledge signals for the corresponding DMA requests. The active polarity of these lines is programmable and is set to active low on reset.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
CPUHRQ	40	O	CPU Hold Request - This output is the hold request to the CPU and is used to request control of the system bus. It can be issued by a request from the DMA controllers or the timer when it is time for a refresh cycle.
CPUHLDA	44	I	CPU Hold Acknowledge - This input from the CPU indicates that it is acknowledging the hold request and is no longer driving the system bus. It indicates that the VL82C100 can now drive the address and control buses.
–AEN1	8	O	Address Enable 1 - This active low signal indicates when DMA Controller 1 is enabling addresses onto the peripheral address bus for a DMA transfer.
–AEN2	7	O	Address Enable 2 - This active low signal indicates when DMA Controller 2 is enabling addresses onto the peripheral address bus for a DMA transfer.
T/C	39	O	Terminal Count - Indicates one of the DMA channels terminal count has been reached.
–MASTER	45	I	Master - An external device will pull this input low to disable the DMA controllers and get access to the system bus. It indicates an I/O channel controls the system buses.
IOCHRDY	73	I	I/O Channel Ready - An input used to extend the memory read and write pulses from the 8237 to accommodate slow devices.
MHZ119	41	I	This is the 1.19 MHz clock input for the 8254 counter.
OUT2	42	O	Out 2 - The output of counter 2 in the 8254 megacell.
–REFRESH	25	I/O	Refresh - This I/O signal will be pulled low by the VL82C100 whenever the 8254 counter 1 issues a CPUHRQ to the CPU and a hold acknowledge is received from the CPU. It is used internally to select a location in the memory mapper which drives the upper address bus A17-A23. –REFRESH can also be used as an input if the refresh timing is to come from a source other than the 8254 channel 1 counter. –REFRESH is an open drain output capable of sinking 20 mA and requires an external pull-up resistor.
VDD	5, 43		System Power: 5 V
VSS	22, 26, 59, 67		System Ground

FUNCTIONAL DESCRIPTION

The VL82C100 Peripheral Controller integrates two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 counter/timer and a 74LS612 equivalent along with support logic onto a single chip. The peripheral controller will replace all the logic on the X bus of an AT-compatible design except the keyboard controller and real time clock.

The VL82C100 is broken up into five major subsections. The megacell chip select subsection consists of decodes of the signals –MASTER, CPUHLDA, and the address bus XA0-XA9. This decode is used to generate the chip select signals to each of the megacells within the VL82C100.

The DMA subsection consists of two 8237 megacells, two 8 bit latches to hold the middle range address bits during a DMA cycle and a 74LS612 equivalent megacell to generate the upper range address bits during a DMA operation. The DMA subsection also has logic to force all DMA cycles to have one wait state inserted and some logic to delay the leading edge of the –XMEMR signal for one DMA clock cycle. These groups of logic are used to maintain AT-compatibility. The DMA subsection provides a total of seven external DMA channels. Four of these channels are used for 8 bit I/O adapters and the other three are used for 16 bit I/O adapters. All channels are capable of addressing all memory locations in a 16 megabyte address space.

The interrupt controller subsection consists of two 8259 megacells cascaded together to allow for 15 possible interrupt sources. One of these interrupt request lines is used internally, so there are a total of 14 possible external interrupts.

The counter/timer subsection contains a single 8254 megacell. This megacell has three internal counters. All of the counters run off a common clock input. The output of Counter 0 is routed to the interrupt controller subsection to be

TABLE 1. ADDRESS DECODE FOR CHIP SELECTS

XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	Address Range	Chip Select Generated
0	0	0	0	0	X	X	X	X	X	000-01F	DMA Controller 1 (8237)
0	0	0	0	1	X	X	X	X	X	020-03F	Int. Controller 2 (8259)
0	0	0	1	0	X	X	X	X	X	040-05F	Counter/Timer (8254)
0	0	0	1	1	0	X	X	X	1	061	Port B (TMGAT2)
0	0	1	0	0	X	X	X	X	X	080-09F	DMA Page Reg. (74LS612)
0	0	1	0	1	X	X	X	X	X	0A0-0BF	Int. Controller 2 (8259)
0	0	1	1	0	X	X	X	X	X	0C0-0DF	DMA Controller 2 (8237)

used as interrupt request 0. The output from Counter 1 is routed to the hold request arbiter to initiate refresh cycles. Counter 2's output is available as an external pin. The counter/timer subsection also contains a flip-flop which can be written to with an –XIOW command to control the gate input to Counter 2.

The hold request arbiter and refresh subsection is used to arbitrate between a possible hold request from the DMA subsection or Counter 2 of the counter/timer subsection. This block of logic also controls the –REFRESH output signal.

MEGACELL CHIP SELECTS

Address bits XA0-XA9 are used to generate chip selects for each of the individual megacells. A map of the address decode is shown in Table 1.

For all the address decodes shown the chip selects are disabled if both CPUHLDA and –MASTER are high.

The address decode at address 061 hex goes to a single flip-flop used to clock in the value of TMGAT2 in an AT-compatible design. This flip-flop will clock in the value on XD0 on the rising edge of –XIOW whenever that address decode is valid. The output of the flip-flop is used to gate counter 2 in the 8254 megacell on and off. This is the only bit of Port B in the VL82C100 and it cannot be read externally. The entire Port B is located in the Memory Controller Device of the chip set. Bit 0 is duplicated in the VL82C100 only to save an input pin.

DMA SUBSECTION

The DMA subsection controls DMA transfers between an I/O channel and on-board or off-board memory. It generates a hold request to the CPU when an I/O channel requests a DMA operation. Once the hold has been acknowledged the DMA controller will drive all 24 address bits for a total addressing capability of 24 megabytes, and drive the appropriate bus command signals depending on whether the DMA is a memory read or write. The DMA controllers are 8237 compatible, internal latches are provided for latching the middle address bits output by the 8237 megacells on the data bus, and the function of a 74LS612 memory mapper is provided to generate the upper address bits.

DMA CONTROLLERS

The VL82C100 supports seven DMA channels using two 8237 equivalent megacells capable of running at a 10 MHz DMA clock (20 MHz SYSCLK) rate. DMA Controller 1 contains channels 0 through 3. These channels support 8 bit I/O adapters. Channels 0 through 3 are used to transfer data between 8 bit peripherals and 8 or 16 bit memory. A full 24 bit address is output for each channel so they can all transfer data throughout the entire 16 megabyte system address space. Each channel can transfer data in 64 kilobyte pages.

DMA Controller 2 contains channels 4 through 7. Channel 4 is used to cascade DMA Controller 1, so it is not available externally. Channels 5 through 7 support 16 bit I/O adapters to transfer data between 16 bit I/O adapters and 16 bit system memory. A full 24 bit address is output for each channel so they can all transfer data throughout the entire 16 megabyte system address space. Each channel can transfer data in 128 kilobyte pages. Channels 5, 6, and 7 are meant to transfer 16 bit words only and cannot address single bytes in system memory.

DMA CONTROLLER REGISTERS

The 8237 megacells can be programmed any time CPUHLDA is inactive. Table 2 lists the addresses of all registers which can be read or written in the 8237 megacells. Addresses under DMA 2 are for the 16 bit DMA channels and DMA 1 corresponds to the 8 bit channels. When writing to a channel's address or word count register the data is written into both the base register and current register simultaneously. When reading a channel's address or word count register only the current address or word count can be read. The base address and base word count are not accessible for reading.

The address and word count registers for each channel are 16 bit registers. The value on the data bus is written into the upper byte or lower byte depending on the state of the internal addressing flip-flop. This flip-flop can be cleared by the Clear Byte Pointer Flip-Flop command. After this command the first read/write to an address or word count register will read/write to the low byte of the 16 bit register and the byte pointer flip-flop will toggle to a one. The next read/write to an address or word count

FIGURE 1. DMA SUBSECTION

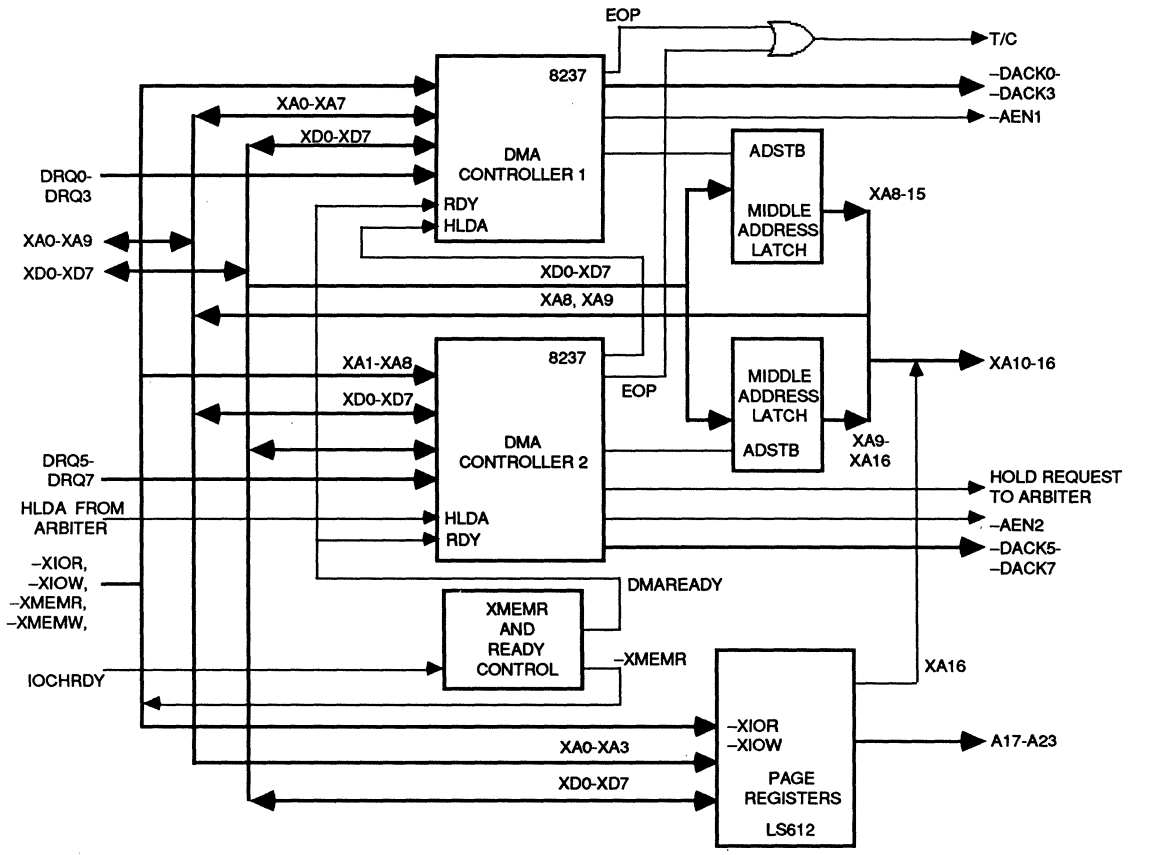


TABLE 2. DMA CONTROLLER REGISTERS ADDRESSES

Hex Address		
DMA2	DMA1	Register Function
0C0	000	Channel 0 Base and Current Address Register
0C2	001	Channel 0 Base and Current Word Count Register
0C4	002	Channel 1 Base and Current Address Register
0C6	003	Channel 1 Base and Current Word Count Register
0C8	004	Channel 2 Base and Current Address Register
0CA	005	Channel 2 Base and Current Word Count Register
0CC	006	Channel 3 Base and Current Address Register
0CE	007	Channel 3 Base and Current Word Count Register
0D0	008	Read Status Register/Write Command Register
0D2	009	Write Request Register
0D4	00A	Write Single Mask Register Bit
0D6	00B	Write Mode Register
0D8	00C	Clear Byte Pointer Flip-Flop
0DA	00D	Read Temporary Register/Write Master Clear
0DC	00E	Clear Mask Register
0DE	00F	Write All Mask Register Bits

register will read/write to the high byte of the 16 bit register and the byte pointer flip-flop will toggle back to a zero. Refer to the 8237 data sheet for more information on programming the 8237 megacell.

The 8237 DMA controller megacells allow the user to program the active level (low or high) of the DRQ and –DACK signals. Since the two megacells are cascaded together internally on the chip, these signals should always be programmed with the DRQ signals active high and the –DACK signals active low.

When programming the 16 bit channels (channels 5, 6, and 7) the address which is written to the base address register must be the real address divided by two. Also, the base word count for the 16 bit channels is the number of 16 bit words to be transferred, not the number of bytes as is the case for the 8 bit channels.

It is recommended that all internal locations, especially the mode registers, in the 8237 megacells be loaded with some valid value. This should be done even if the channels are not used.

MIDDLE ADDRESS BIT LATCHES

The middle address bits of the 24 bit address range are held in two sets of 8 bit registers, one register for each DMA controller. The DMA controller will drive the value to be loaded onto the data bus and then issue an address strobe signal to latch the data bus value into these registers. An address strobe is issued at the beginning of a DMA cycle and any time the lower 8 bit address increments across the 8 bit subpage boundary during block transfers. These registers cannot be written to or read externally. They are loaded only from the address strobe signals from the megacells and the outputs go only to the XA8-XA16 pins.

PAGE REGISTERS

The equivalent of a 74LS612 is used in the VL82C100 to generate the page registers for each DMA channel. The page registers provide the upper address bits during a DMA cycle. DMA addresses do not increment or decrement across page boundaries. Page boundaries for the 8 bit channels (channels 0 through 3) are every 64 kilobytes and page boundaries for the 16 bit channels (channels 5, 6, and 7) are every 128 kilobytes. There are a total of 16 eight bit registers in the 74LS612 megacell. The page registers are in the I/O address space as shown.

Page Register	Hex I/O Address
DMA channel 0	087
DMA channel 1	083
DMA channel 2	081
DMA channel 3	082
DMA channel 5	08B
DMA channel 6	089
DMA channel 7	08A
Refresh	08F

These registers must be written to select the correct page for each DMA channel before any DMA operations are performed. The other address locations between 080 and 08F that are not shown, are not used by the DMA channels but can be read or written to by the CPU. Address 08F is used to drive a value onto the upper address bits A17-A23 of the CPU's address bus during a refresh cycle.

ADDRESS GENERATION

The DMA addresses are setup such that there is an upper address portion, used to select a specific page, a middle address portion, used to select a block within the page, and a lower address portion.

The upper address portion is generated by the page registers, in the 74LS612 equivalent megacell. The page registers for each channel must be setup by the CPU before a DMA operation. DMA addresses do not increment or decrement across page boundaries. Page sizes are 64 kilobytes for 8 bit channels (channels 0 through 3) and 128 kilobytes for 16 bit channels (channels 5, 6, and 7). The

TABLE 3. ADDRESS SOURCE GENERATION

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 8237	8 Bit DMA Address Bits	16 Bit DMA Address Bits
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			XA16	
	D7		XA15	XA16
	D6		XA14	XA15
	D5		XA13	XA14
	D4		XA12	XA13
	D3		XA11	XA12
	D2		XA10	XA11
	D1		XA9	XA10
	D0		XA8	XA9
		A7	XA7	XA8
		A6	XA6	XA7
		A5	XA5	XA6
		A4	XA4	XA5
		A3	XA3	XA4
		A2	XA2	XA3
		A1	XA1	XA2
		A0	XA0	XA1
		VSS	---	XA0

DMA page register values are output on A17-A23 and XA16 for 8 bit channels, and A17-A23 for 16 bit channels.

The middle address portion, used to select a block within the page, is generated by the 8237 megacells at the beginning of a DMA operation and any time the DMA address increments or decrements through a block boundary. Block sizes are 256 bytes for 8 bit channels (channels 0 through 3) and 512 bytes for 16 bit channels (channels 5, 6, and 7). This middle address portion is output by the 8237 megacells onto the data bus during state S1. The internal middle address bit latches will latch in this value. The middle address bit latches are output on XA8-XA15 for 8 bit channels, and XA9-XA16 for 16 bit channels.

The lower address portion is generated directly by the 8237 megacells during DMA operations. The lower address bits are output on XA0-XA7 for 8 bit channels, and XA1-XA8 for 16 bit channels. XA0 is forced low during 16 bit DMA operations.

Table 3 is shown to illustrate the source for all address bits during both 8 and 16 bit transfers.

READY CONTROL

The ready input to each of the 8237 megacells is driven from the same source within the ready control logic. To maintain an AT-compatible design, the VL82C100 ready control logic forces one wait state on every DMA transfer. The external signal IOCHRDY goes into the ready control logic to extend transfer cycles to longer than one wait state if needed. To add extra wait states, an external device should pull IOCHRDY low within the setup time before the second phase of the internal DMA clock during the forced wait state. The current DMA cycle will then be extended by inserting wait states until IOCHRDY is returned high. IOCHRDY going high must meet the setup time before the second phase of a wait state cycle or an extra wait state will be inserted before the DMA controller transitions to state S4 (see timing diagrams).

XMEMR DELAY

To maintain an AT-compatible design, the VL82C100 inserts a DMA clock cycle delay in the falling edge of the –XMEMR signal. –XMEMR will go low one DMA clock (two SYSCLK's) later than the –MEMR signal coming out of the 8237 megacell. The rising edge is not altered and will go high at the same time the –MEMR signal from the megacell goes high.

EXTERNAL CASCADING

An external DMA controller or bus master can be attached to an AT-compatible design through the VL82C100's DMA controllers. To add an external DMA controller, one of the seven available DMA channels must be programmed in cascade mode. That channel's DRQ signal should then be connected to the external DMA controller's HRQ output. The corresponding –DACK signal for that channel should be connected to the external DMA controller's HLDA input. When one of the VL82C100's seven channels is programmed in cascade mode and that channel is acknowledged the VL82C100 will not drive the data bus, the command signals, or the XA address bus. However, the upper address bits A17-A23 will be driven with the value programmed into the page register for the channel programmed in cascade mode.

An external device can become a bus master and control the system address, data, and command buses in much the same manner. One of the DMA channels must be programmed in cascade mode. The external device then asserts the DRQ line for that channel. When that channel's –DACK line goes active, the external device can then pull the –MASTER signal low to force the system buses to a high impedance state. As in the DMA controller cascading, the VL82C100 will not drive the X buses while the cascaded channels –DACK signal is active. Also, the VL82C100 will force the upper address bits A17-A23 to a high impedance state while –MASTER is held low.

INTERRUPT CONTROLLER SUBSECTION

The interrupt controller subsection is made up of two 8259 megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally on the VL82C100 and one of the interrupt request inputs is internally connected to an output of the 8254 counter/timer megacell. This allows a total of 14 external interrupt requests.

A typical interrupt sequence would be as follows. Any unmasked interrupt will generate the INTR signal to the CPU. The interrupt controller megacells will then respond to the –INTA pulses from the CPU. On the first –INTA cycle the

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FIGURE 2. INTERRUPT CONTROLLER SUBSECTION

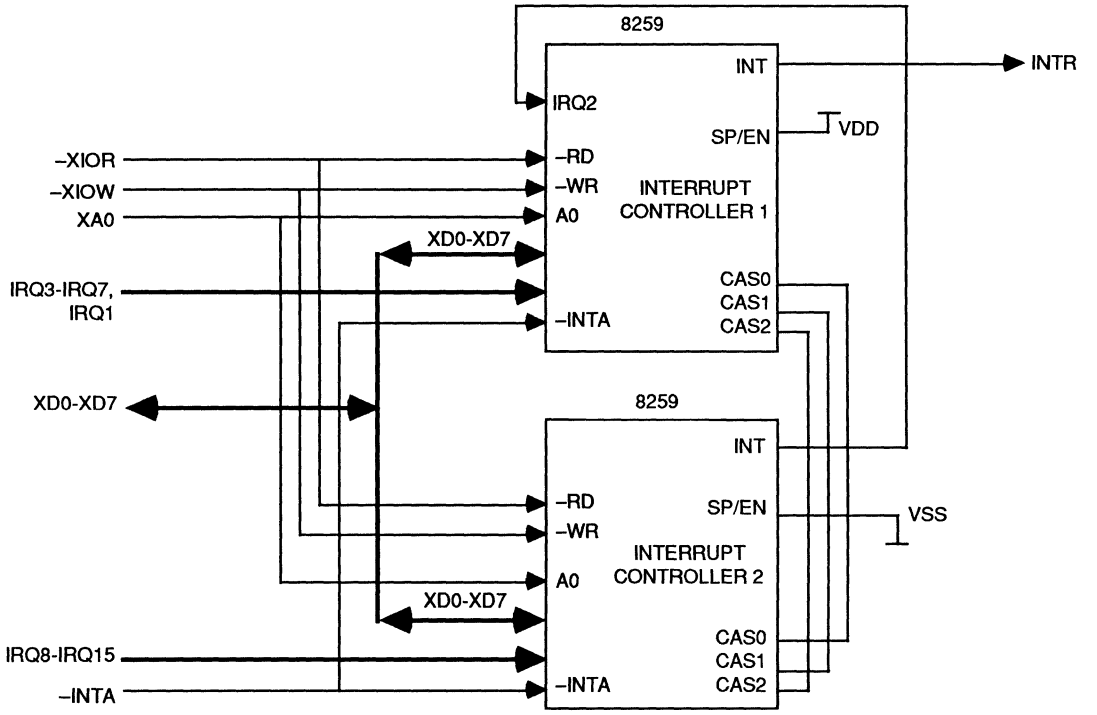


TABLE 4. WRITE OPERATIONS

Hex Address				
INT1	INT2	XD4	XD3	Register Function
020	0A0	1	X	Write ICW1
021	0A1	X	X	Write ICW2
021	0A1	X	X	Write ICW3
021	0A1	X	X	Write ICW4 (If Needed)
021	0A1	X	X	Write OCW1
020	0A0	0	0	Write OCW2
020	0A0	0	1	Write OCW3

TABLE 5. READ OPERATIONS

Hex Address		
INT1	INT2	Register Function
020	0A0	Interrupt Request Reg., In-Service Reg., or Poll Command
021	0A1	Interrupt Mask Register

cascading priority is resolved to determine which of the two 8259 megacells will output the interrupt vector onto the data bus. On the second –INTA cycle the appropriate 8259 megacell will drive the data bus with the correct interrupt vector for the highest priority interrupt.

Because the two megacells are cascaded internally on the VL82C100, they should never be programmed to operate in the buffered mode.

INTERRUPT CONTROLLER INTERNAL REGISTERS

The internal registers of the 8259 megacells are written to in the same way as in the standard part. Table 4 shows the correct addressing for each of the 8259 registers.

Before normal operation can begin, each 8259 megacell must follow an initialization sequence. The sequence is started by writing Initialization Command Word 1 (ICW1). After ICW1 has been written the 8259 megacell expects the next writes to follow in the sequence ICW2, ICW3, and ICW4 if it is needed. The Operation Control Words (OCW) can be written at any time after initialization.

In the standard 8259 megacell ICW3 is optional. But since the two 8259's in this chip are cascaded together, they should always be programmed in cascade mode and ICW3 will always be needed. Refer to the 8259 data sheet for more information on programming the 8259 megacell.

When reading at address 020 or 0A0 hex, the register read will depend on how Operation Control Word 3 was setup prior to the read.

TIMER/COUNTER SUBSECTION

The timer subsection consists of one 8254 counter/timer megacell configured as shown in the diagram. The clocks for each of the three internal counters are tied to the single input pin MHZ119. The gate inputs of Counters 0 and 1 are tied high to enable those Counters at all times. The gate input of Counter 2 is tied to the output of a flip-flop inside the

FIGURE 3. TIMER/COUNTER SUBSECTION

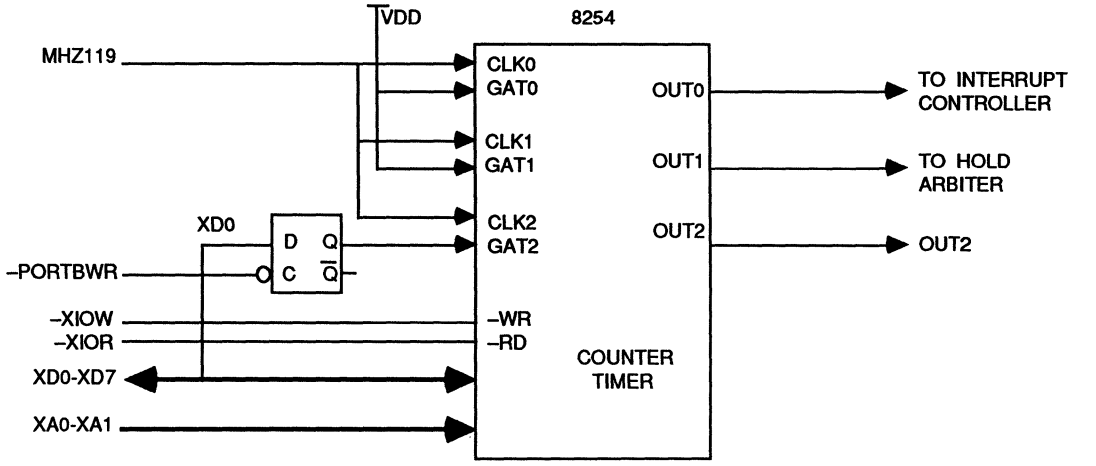


TABLE 6. TIMER/COUNTER REGISTERS

Hex Address	–XIOR	–XIOW	Register Function
040	1	0	Write Initial Count to Counter 0
040	0	1	Read Latched Count or Status from Counter 0
041	1	0	Write Initial Count to Counter 1
041	0	1	Read Latched Count or Status from Counter 1
042	1	0	Write Initial Count to Counter 2
042	0	1	Read Latched Count or Status from Counter 2
043	1	0	Write Control Word
043	0	1	No Operation

VL82C100. This flip-flop will clock in the value on XD0 during an I/O write to Port B. The output of the flip-flop is used to gate Counter 2 in the 8254 megacell on and off.

Only one of the 8254 megacell counter outputs is directly available at an external pin. Counter 0's output is connected to the IRQ0 input of interrupt controller 1. Counter 1's output goes to the hold request arbiter and refresh subsection to initiate a refresh cycle. Finally, Counter 2's output goes directly to the output pin OUT2.

TIMER/COUNTER INTERNAL REGISTERS

The internal registers of the 8254 counter/timer megacell are written to in the same way as in the standard part. Table 6 shows the correct addressing for each of the 8254 registers.

The write control word at address 043 hex could also be the counter latch command or read back command depending on the values on the data bus. Refer to the 8254 data sheet for more information on programming the 8254 megacell.

HOLD REQUEST ARBITER AND REFRESH SUBSECTION

The hold request arbiter and refresh subsection is used to select between the two possible sources for a hold request to the CPU. A hold request can be generated when DMA Controller 2 issues a hold request or when the output of counter 1 in the 8254 megacell makes a low to high transition. To provide equal weight to these two possible sources for a hold request, the hold request from the DMA controller is sampled on the rising edge of the internal DMA clock and the request from the counter/timer is sampled on the falling edge of the internal DMA clock. The request which is clocked in first will be granted by the arbiter and the other request inhibited until the first request is finished.

At the end of a hold request from either source the arbiter checks to see if the other source is still requesting a hold. If it is, the arbiter will give an acknowledge signal to that source and leave the CPUHRQ line active. This will continue as long as one of the two sources is requesting a hold. Only if neither source is requesting a hold will the arbiter negate the CPUHRQ signal and return control back to the CPU.

In the case of the DMA controller's hold request winning in the arbiter, the arbiter will assert the CPUHRQ output and wait for a CPUHLDA signal back from the CPU. The assertion of CPUHLDA will cause a hold acknowledge to be sent to the DMA controller. When the DMA controller is finished it will negate its hold request signal to the arbiter. The arbiter will then switch to a –REFRESH cycle, if a hold request is pending from the 8254 counter/timer, or negate the CPUHRQ line and return control to the CPU.

In the case of a refresh cycle winning the arbitration, the CPUHRQ output will be asserted and the arbiter subsection will wait for a CPUHLDA signal back from the CPU. The assertion of CPUHLDA will cause the VL82C100 to pull the –REFRESH pin low. –REFRESH will remain low for four SYSCLK rising edges. On the fourth rising edge of SYSCLK the –REFRESH pin will go to a high impedance state enabling it to be pulled up by an external resistor, and the CPUHRQ signal will be negated. If the hold request arbiter has a hold request from the DMA controller pending on the fourth rising edge of SYSCLK, the –REFRESH cycle is extended for one more SYSCLK cycle (see waveforms). The hold request arbiter will then acknowledge the hold request of the DMA controller.

Refresh cycles can be extended by an external source by forcing the IOCHRDY input low a setup time before the third rising edge of SYSCLK. –REFRESH will remain low until IOCHRDY is returned high.

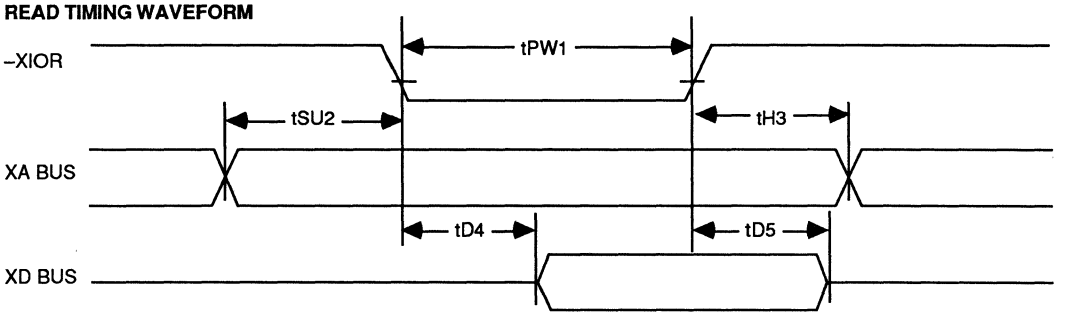
The pin –REFRESH is a bidirectional open drain I/O pin and requires an external pull-up. It can also be used as an input if a refresh cycle is to be initiated from an external source.

AC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

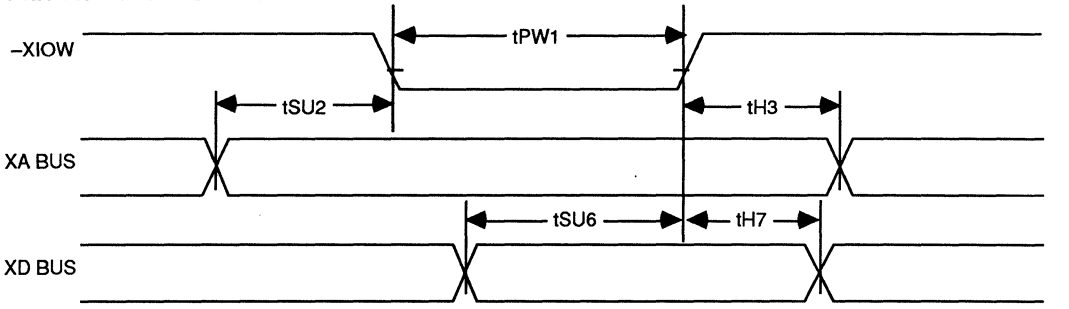
READ/WRITE MODE TIMING

Symbol	Parameter	12/16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tPW1	–XIOR or –XIOW Pulse Width Low	180		150		ns	
tSU2	XA Address Valid to –XIOR or –XIOW Low Setup Time	30		25		ns	
tH3	XA Address from –XIOR or –XIOW High Hold Time	15		15		ns	
tD4	XD Data Valid Delay from –XIOR Low		120		110	ns	
tD5	XD Data Float Delay from –XIOR High	0	80	0	75	ns	
tSU6	XD Data Valid to –XIOW High Setup Time	110		100		ns	
tH7	XD Data Valid from –XIOW High Hold Time	15		15		ns	
tPW8	RESET Pulse Width High	250		250		ns	
t9	RESET Inactive to first –XIOR or –XIOW Command	4		4		TCY	
tD10	Command Recovery Time Between Successive –XIOR or –XIOW Pulses	250		200		ns	

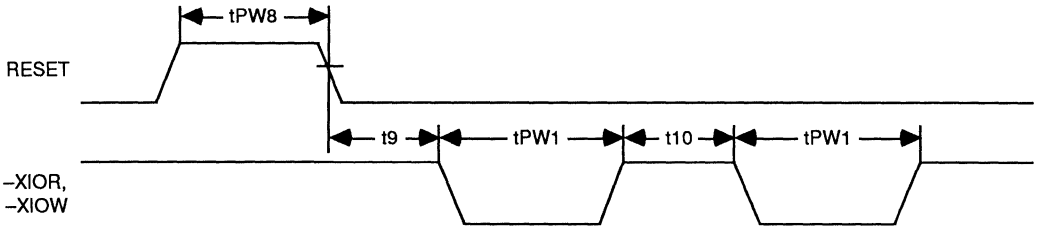
READ TIMING WAVEFORM



WRITE TIMING WAVEFORM



COMMAND AND RESET TIMING WAVEFORM

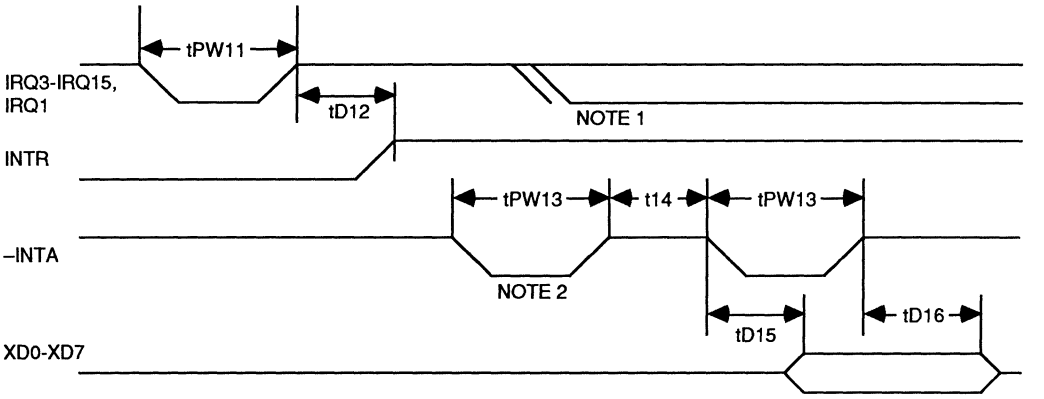


INTERRUPT MODE TIMING

Symbol	Parameter	12/16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tPW11	Interrupt Request Pulse Width Low	90		90		ns	
tD12	Interrupt Output Delay	130		130		ns	
tPW13	-INTA Pulse Width Low	180		180		ns	
t14	End of -INTA Pulse to next -INTA Pulse	180		180		ns	
tD15	XD Data Valid Delay from -INTA Low		120		110	ns	
tD16	XD Data Float Delay from -INTA High	0	50	0	45	ns	

4

INTERRUPT TIMING WAVEFORM

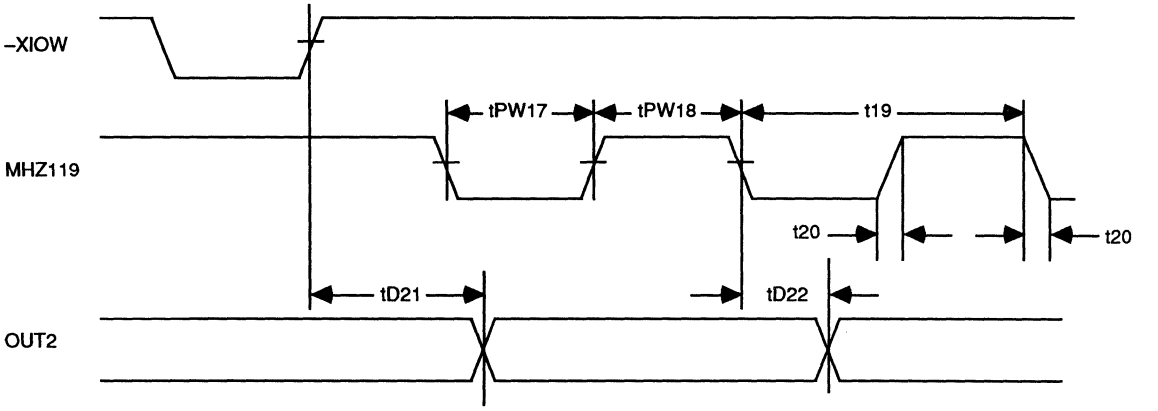


Notes: 1. IRQ must remain active until first -INTA pulse.
2. Cascade priority is resolved on this -INTA cycle.

TIMER/COUNTER TIMING

Symbol	Parameter	12/16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tPW11	MHZ119 Clock Pulse Width High	55		55		ns	
tPW18	MHZ119 Clock Pulse Width Low	55		55		ns	
t19	MHZ119 Clock Cycle Time	180		180		ns	
t20	MHZ119 Clock Rise/Fall Time	20		20		ns	
tD21	OUT2 Valid from –XIOW High Delay Time when writing to Counter 2 Mode Register or TMGATE2 in Port B		100		100	ns	
tD22	OUT2 Valid from MHZ119 Low Delay Time		100		100	ns	

TIMER/COUNTER TIMING WAVEFORM



DMA MODE TIMING

Symbol	Parameter	12/16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU23	DRQ to SYSCLK High Setup Time	0		0		ns	Note 1
tD24	CPUHRQ Valid from SYSCLK High Delay Time		70		70	ns	
tSU25	CPUHLDA to SYSCLK High Setup Time	25		25		ns	
tD26	–AEN1 Valid from SYSCLK High Delay Time		80		80	ns	
tD27	–DACK Valid from SYSCLK High Delay Time		100		100	ns	
tD28	XD Bus Valid from SYSCLK High Delay Time		110		110	ns	
tD30	A17-A23 Float from CPUHLDA High Delay Time	1	40	1	40	ns	
tD31	Upper Address Bits Valid from SYSCLK High Delay Time		130		115	ns	Note 2
tD32	A17-A23 Float from CPUHLDA Low Delay Time	1	25	1	25	ns	
tD33	Middle Address Bits Valid from SYSCLK High Delay Time		125		115	ns	Note 3
tD34	Lower Address Bits Valid from SYSCLK High Delay Time		90		90	ns	Note 4
tD35	XA Address Bus Float from SYSCLK High Delay Time	1	70	1	70	ns	8 Bit Cycles Only
tD36	–READ and –WRITE Active from SYSCLK High Delay Time		85		80	ns	
tD37	–READ and –WRITE Valid from SYSCLK High Delay Time		90		85	ns	
tD38	–READ and –WRITE Float from SYSCLK High Delay Time	1	70	1	70	ns	8 Bit Cycles Only
tD39	T/C Valid from SYSCLK High Delay Time		90		85	ns	8 Bit Cycles Only

Notes: 1. The DRQ signals are asynchronous inputs. Setup times are shown to assure recognition at a specific clock edge for testing.

2. Upper address bits are defined as A17-A23 for 16 bit DMA cycles, and A17-A23 plus XA16 for 8 bit DMA cycles.
3. Middle address bits are defined as XA9-XA16 for 16 bit DMA cycles and XA8-XA15 for 8 bit DMA cycles.
4. Lower address bits are defined as XA0-XA8 for 16 bit DMA cycles and XA0-XA7 for 8 bit DMA cycles.

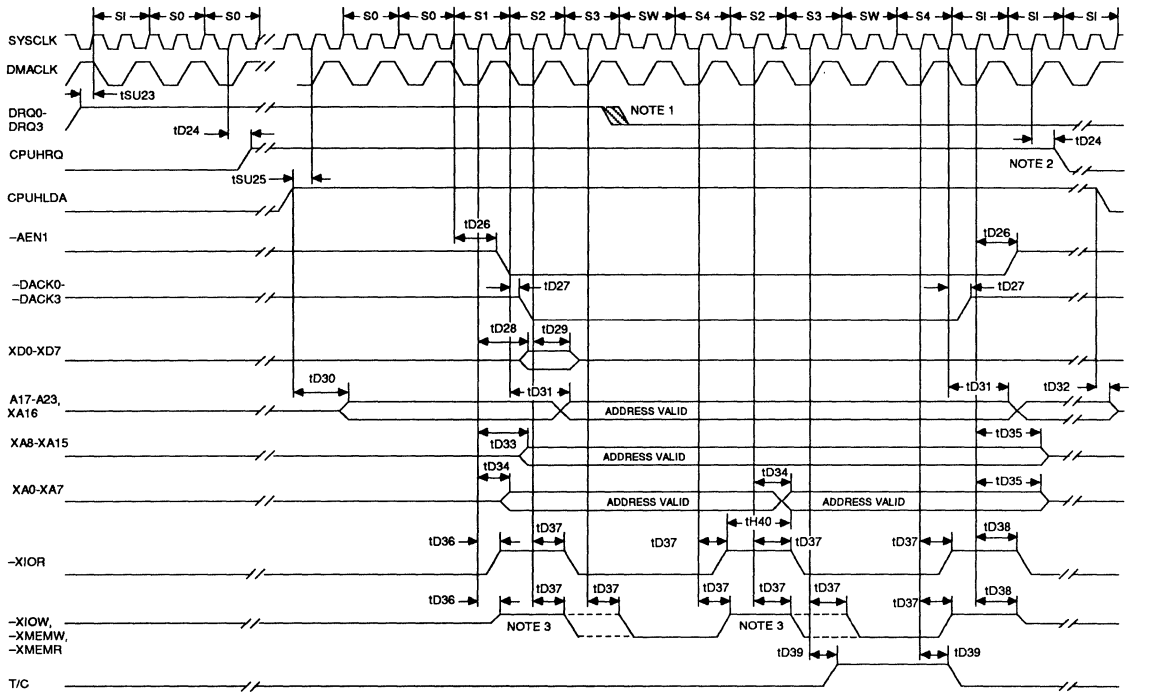
DMA MODE TIMING (Cont.)

Symbol	Parameter	12/16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tH40	XA Address from –READ or –WRITE High Hold Time	2 TCY –50		2 TCY –50		ns	TCY = SYSCLK Cycle Time
tD41	–AEN2 Low from SYSCLK High Delay Time		80		80	ns	
tD42	–AEN2 High From SYSCLK High		150		150	ns	
tD43	XA Address Bus Float from SYSCLK High Delay Time		140		140	ns	16 Bit DMA Cycles Only
tD44	–READ or –WRITE Float from SYSCLK High Delay Time		140		140	ns	16 Bit DMA Cycles Only
t45	–READ or –WRITE Float from –READ or –WRITE High at end of DMA Cycle	5		5		ns	16 Bit DMA Cycles Only
tSU46	IOCHRDY Valid to SYSCLK High Setup Time	25		20		ns	
tH47	IOCHRDY from SYSCLK High Hold Time	10		10		ns	
tD48	A17-A23 Float from –MASTER Low Delay Time	1	25	1	25	ns	
tD49	A17-A23 Float from –MASTER High Delay Time	1	40	1	40	ns	
tD50	–REFRESH Low from CPUHLDA High Delay Time		70		60	ns	
tD51	–REFRESH Inactive from SYSCLK High Delay Time		50		50	ns	Note 5
tSU52	–REFRESH Low to SYSCLK High Setup Time	25		25		ns	Note 6
tD53	A17-A23 Valid from –REFRESH Valid Delay Time		80		80	ns	
t54	SYSCLK Cycle Time	62		50		ns	
tPW55	SYSCLK Pulse Width Low	25		20		ns	
tPW56	SYSCLK Pulse Width High	25		20		ns	
t57	SYSCLK Rise/Fall Time	10		7		ns	

Notes: 5. –REFRESH is an open drain output. This specification is the time until the output is in an inactive state. Rise time of the external signal will depend on the external pull-up value and capacitive load.

6. When used as an input, –REFRESH is an asynchronous signal. Setup times are shown to assure recognition at a specific clock edge for testing.

8 BIT DMA TIMING WAVEFORM



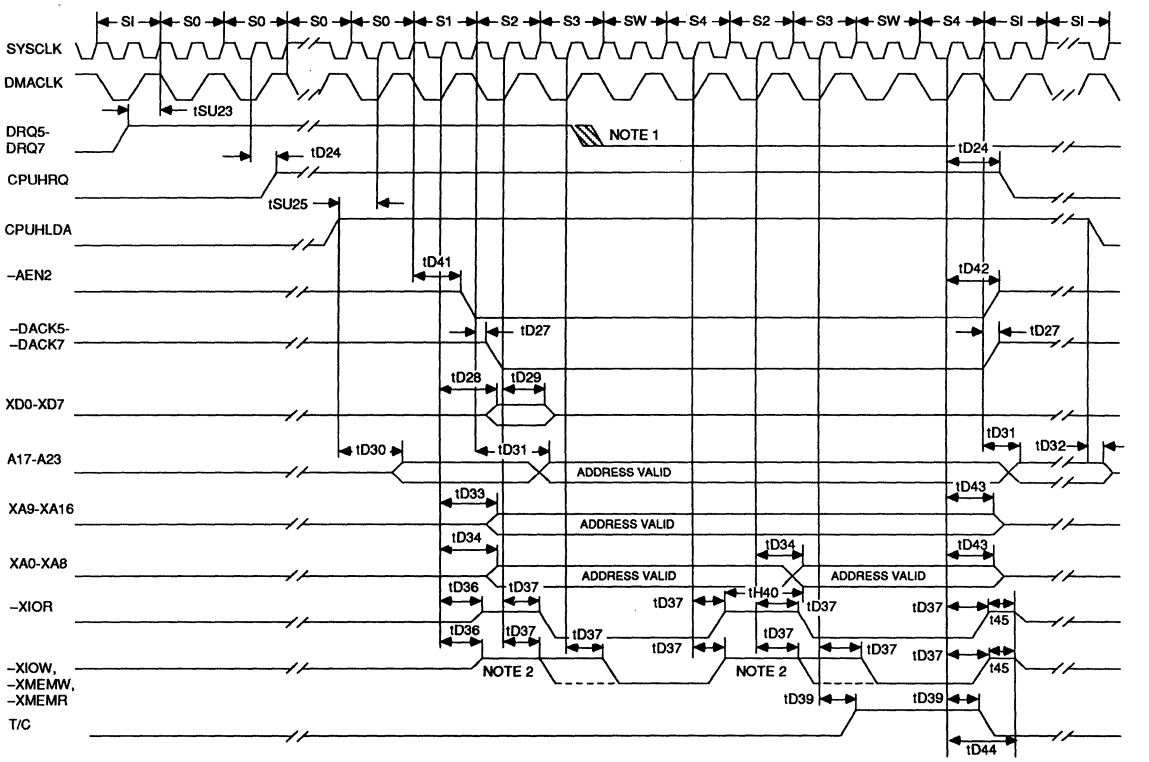
Notes: 1. DRQ should be held active until –DACK is returned.

2. The falling edge of CPUHRQ could occur one clock cycle earlier or later depending on how many bytes are transferred.

3. The first high to low transition shown here is for extended –XIOW and –XMEMW. The second high to low transition shown is for –XMEMR and late write on –XIOW and –XMEMW.

4

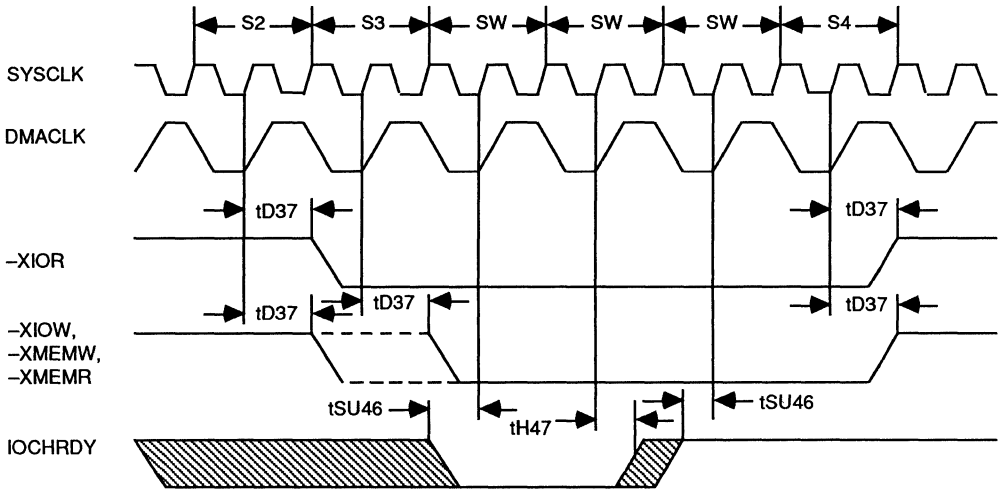
16 BIT DMA TIMING WAVEFORM



Notes: 1. DRQ should be held active until –DACK is returned.

2. The first high to low transition shown here is for extended –XIOW and –XMEMW. The second high to low transition shown is for –XMEMR and late write on –XIOW and –XMEMW.

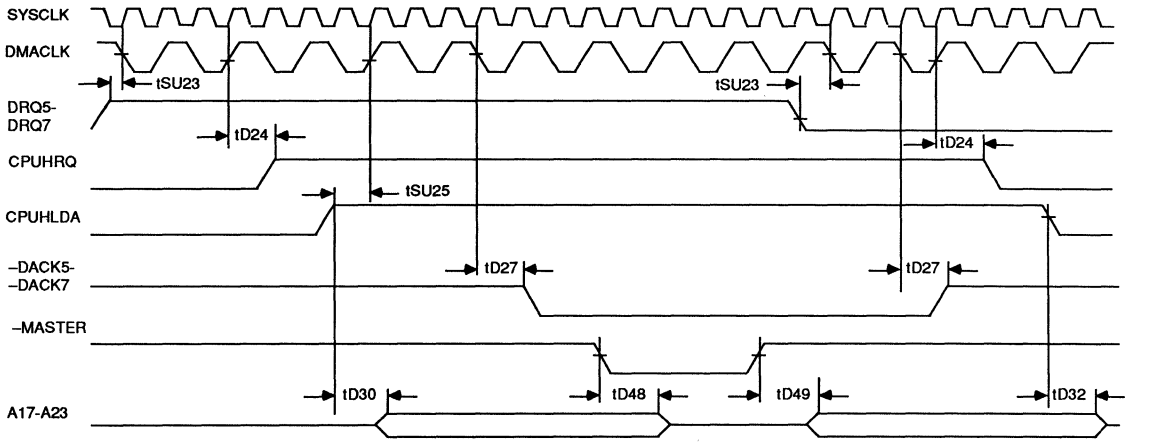
IOCHRDY TIMING WAVEFORM



Note: The first wait state is inserted by internal circuitry in the VL82C100 for all DMA cycles. Any additional wait states must be inserted using IOCHRDY.

4

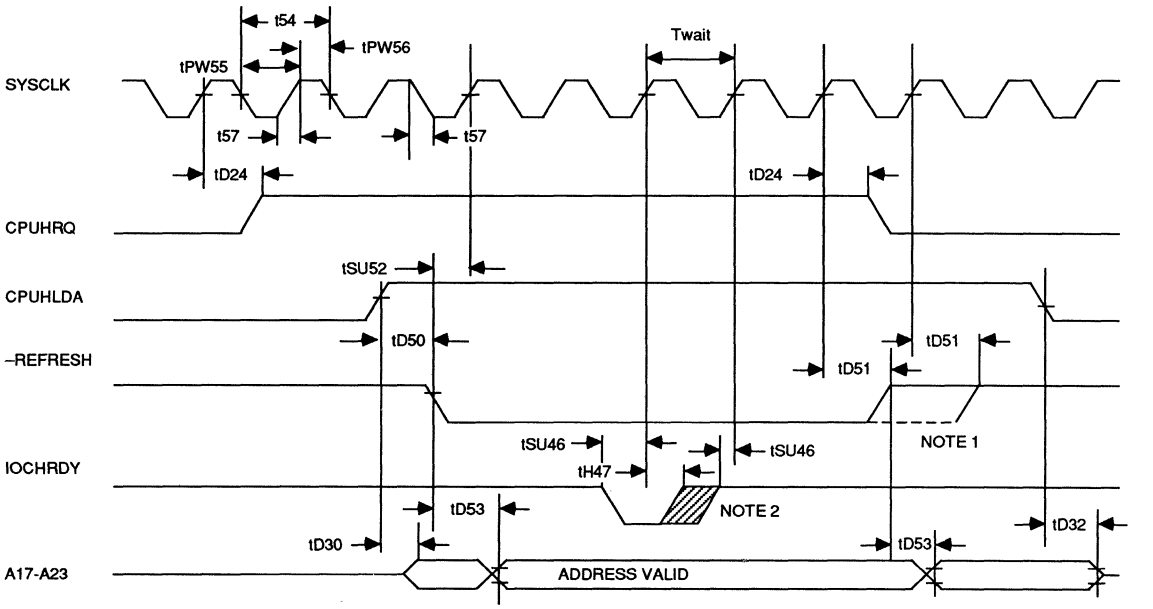
–MASTER TIMING WAVEFORM



Notes: 1. The DMA channel used for requesting control of the bus by a new bus master must be programmed in cascade mode. The new master should not pull –MASTER low until it has received the corresponding –DACK signal.

2. The timing shown is assuming one of the 16 bit DMA channels is used. There will be extra cycles between DRQ and CPUHRQ before and after the request cycle when using an 8 bit DMA channel. These extra cycles are caused by the cascade delay from the slave 8237 through the master 8237.

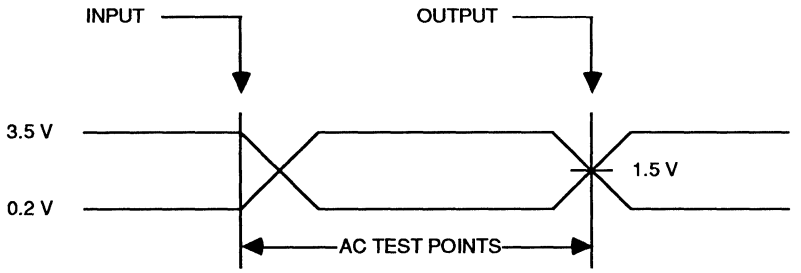
–REFRESH TIMING WAVEFORM



Notes: 1. A refresh pulse is normally three SYSCLK cycles long (with no wait states). Refresh pulses will be four SYSCLK cycles if a hold request is pending from the DMA controllers.

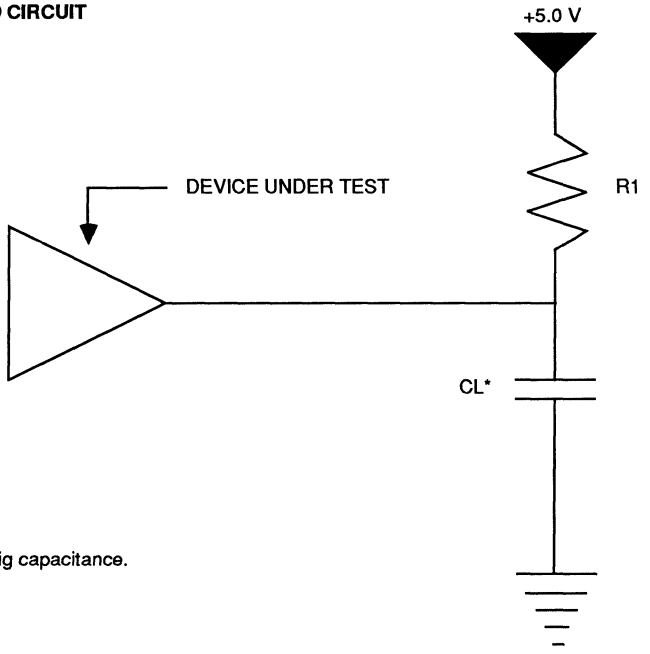
2. –REFRESH cycles can be extended by inserting wait states using IOCHRDY.

AC TESTING - INPUT, OUTPUT WAVEFORM



AC testing inputs are driven at 3.5 V for a logic 1 and 0.2 V for a logic 0. Clock inputs SYSCLK and MHZ119 are driven at 4.3 V and 0.2 V. Timing measurements are made at 1.5 V for both a logic 1 and 0.

AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)	R 1 (Ω)
–REFRESH	100	1K
All –DACKs, T/C	100	
All Other I/O and Output Pins	50	

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	QC = 0°C to +70°C QI = –40°C to +85°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –400 µA
VOL1	Output Low Voltage		0.45	V	IOL = 20 mA, –REFRESH
VOL2	Output Low Voltage		0.45	V	IOL = 2 mA, All Other Pins
VIH	Input High Voltage	2.0	VDD + 0.5	V	TTL
VIL	Input Low Voltage	–0.5	0.8	V	TTL
VIHC	Input High Voltage	3.8	VDD + 0.5	V	RESET, SYSCLK, MHZ119
VILC	Input Low Voltage	–0.5	0.6	V	RESET, SYSCLK, MHZ119
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
IF	Input Leakage Current		–0.5	mA	VIN = 0.45 V, All IRQ & DRQ Inputs
ILI	Input Leakage Current	–10	10	µA	All Other Inputs
ICC	Power Supply Current		30	mA	Note

Note: VIN = VDD or GND, VDD = 5.25 V, outputs unloaded.