Data Sheet

VT1708
High Definition Audio Codec

Revision 1.03
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VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	12/2/05	Initial public release	JE
1.01	12/21/05	Changed “surround back” to “side surround” from the document Removed “Application Circuit” section Modified figure 7	SV
1.02	12/27/05	Modified figure 1	JW
1.03	1/10/06	Removed S/PDIF RX support	EY

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

VT1708
High Definition Audio Codec

PRODUCT FEATURES

- **High Definition Audio Codec**
  - Intel High Definition Audio Specification Rev.1.0 Compliant
- **High Audio Quality**
  - Supports 44.1K/48K/96K/192KHz DAC Independent Sample Rate
  - All ADCs Support 48K/192KHz Independent Sample Rate
  - Built in High Quality Headphone Amplifier
  - Exceeds Microsoft PC2001 Requirements
- **Various Output Format**
  - 4 Stereo DACs Support 24-bit, 192KHz Samples
  - DAC with 100dB S/N Ratio
  - 2 Stereo ADCs Support 24-bit, 192KHz Samples
  - ADC with 95dB S/N Ratio
  - 8-Channels of DAC Support 16/20/24-bit PCM Format for 7.1 Audio Solution
  - 16/20/24 bit S/PDIF TX Supports 24-bit, 44.1K/48K/96KHz Samples
- **Added-on Function**
  - High Quality Differential CD Input
  - HPF In ADC Path for DC Removal
  - Analog CD Input Path for Compatibility
- **Power**
  - Supports EPAD (External Amplifier Power Down)
  - Power Management and Enhanced Power Saving Features
  - Digital: 3.3V; Analog: 3.3V/5.0V
- **Package**
  - Compatible with VT1618 8-Channel AC'97
  - 48-Pin LQFP Package

OVERVIEW

The VIA Technologies' VT1708 is a High Definition Audio Codec that conforms to the Intel High Definition Audio Specification Revision 1.0. It integrates Sample Rate Converters on all channels. This codec is designed with aggressive power management to achieve low power consumption. When used with a 3.3V analog supply, power consumption is further reduced. The primary applications for this part are desktop and portable personal computers multimedia subsystems.

Figure 1 shows the functional block diagram for VT1708 High Definition Audio Codec.

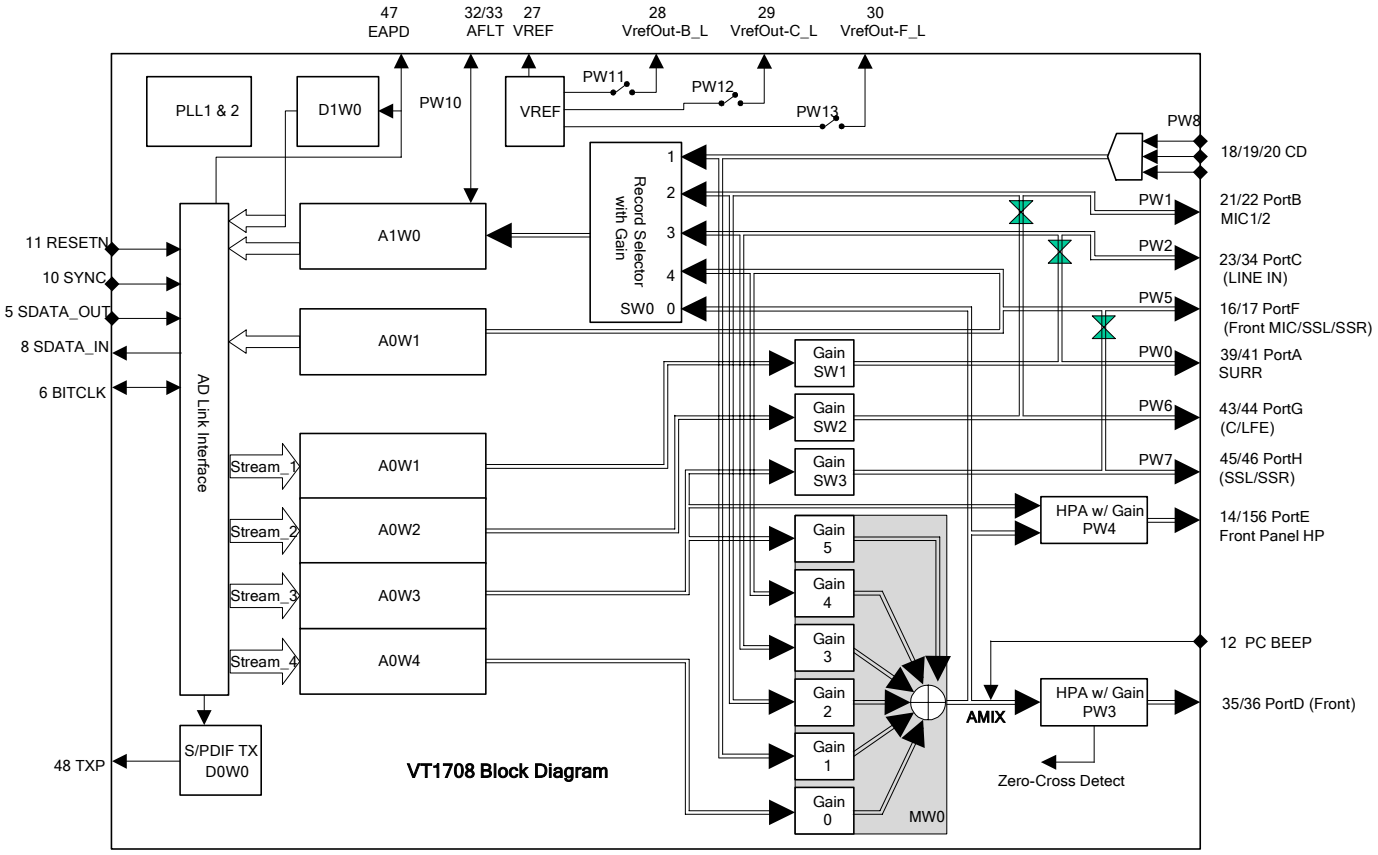


Figure 1. Functional Block Diagram

Pin Diagram

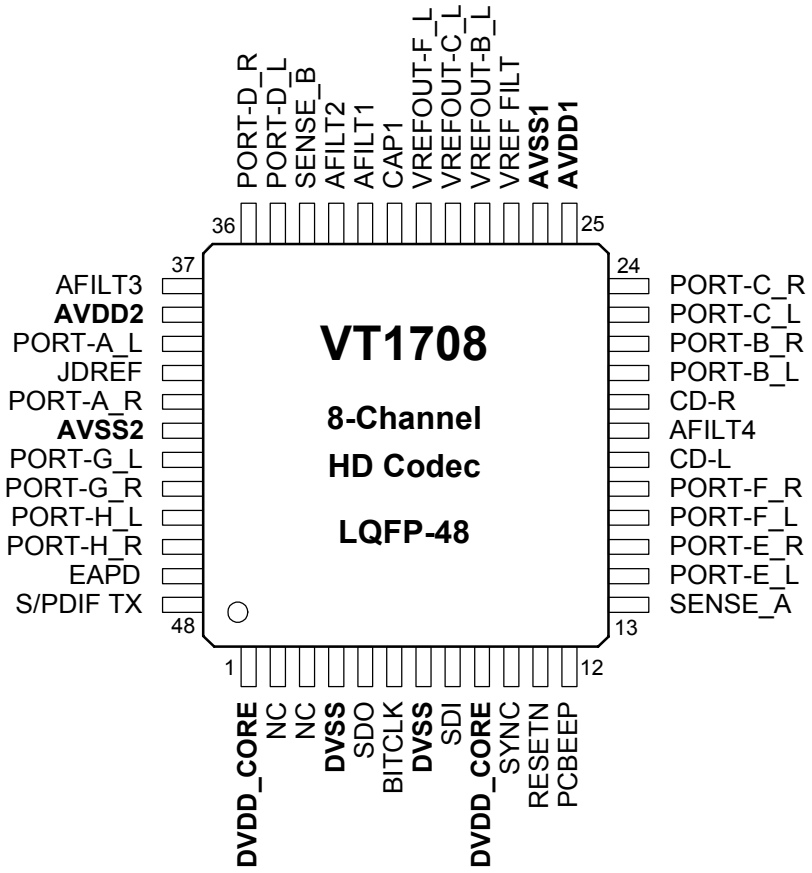


Figure 2. VT1708 Pin Diagram (Top View)

Pin List

Table 1. Pin List (Listed by Pin Name)

Pin Name	Pin#	Pin Name	Pin#
AFILT1	32	PORT-C_L	23
AFILT2	33	PORT-C_R	24
AFILT3	37	PORT-D_L	35
AFILT4	19	PORT-D_R	36
AVDD1	**25**	PORT-E_L	14
AVDD2	**38**	PORT-E_R	15
AVSS1	**26**	PORT-F_L	16
AVSS2	**42**	PORT-F_R	17
BITCLK	6	PORT-G_L	43
CAP1	31	PORT-G_R	44
CD-L	18	PORT-H_L	45
CD-R	20	PORT-H_R	46
DVDD_CORE	**1**	RESETN	11
DVDD_CORE	**9**	EAPD	47
DVSS	**4**	S/PDIF TX	48
DVSS	**7**	SDI	8
JDREF	40	SDO	5
NC	2	SENSE_A	13
NC	3	SENSE_B	34
PCBEEP	12	SYNC	10
PORT-A_L	39	VREF FILTER	27
PORT-A_R	41	VREFOUT-B_L	28
PORT-B_L	21	VREFOUT-C_L	29
PORT-B_R	22	VREFOUT-F_L	30

Pin Descriptions

Table 2. Pin Descriptions

Digital I/O Pins			
Signal Name	**Pin#**	**Type**	**Signal Description**
SDO	5	I	Serial data input from controller
BITCLK	6	I	24MHz bit clock from controller
SDI	8	I/O	Serial data output to controller
SYNC	10	I	Sample SYNC from controller
RESETN	11	I	Hardware reset from controller
EAPD	47	O	External Amplifier power-down
S/PDIF TX	48	O	S/PDIF output

Analog I/O Pins			
Signal Name	**Pin#**	**Type**	**Signal Description**
SENSE_A	13	I	Jack detect pin 1
SENSE_B	34	I	Jack detect pin 2
PORT-E_L	14	O	Analog Output for front panel HP out left
PORT-E_R	15	O	Analog Output for front panel HP out right
PORT-F_L	16	I/O	Default is input for front MIC
PORT-F_R	17	I/O	Default is input for front MIC
CD-L	18	I	CD input left channel
CD-R	20	I	CD input right channel
PORT-B_L	21	I/O	Default is input for MIC1 Left
PORT-B_R	22	I/O	Default is input for MIC1 Right
PORT-C_L	23	I/O	Default is input for Line-in Left
PORT-C_R	24	I/O	Default is input for Line-in Right
PORT-D_L	35	I/O	Default is output for Line-out Left
PORT-D_R	36	I/O	Default is output for Line-out Right
PORT-A_L	39	I/O	Default is output for Surround-out Left
PORT-A_R	41	I/O	Default is output for Surround-out Right
PORT-G_L	43	I/O	Default is output for Center
PORT-G_R	44	I/O	Default is output for LFE
PORT-H_L	45	I/O	Default is output for Side Surround Left
PORT-H_R	46	I/O	Default is output for Side Surround Right
PCBEEP	12	I	PC beep signal input
VREF FILTER	27	I/O	Reference voltage capacitor
VREFOUT-B_L	28	O	Reference voltage output for port B
VREFOUT-C_L	29	O	Reference voltage output for port C
VREFOUT-F_L	30	O	Reference voltage output for port F
CAP1	31	I/O	Optional capacitor for ADC reference
AFILT1	32	I/O	Optional anti-alias filter for ADC left channel
AFILT2	33	I/O	Optional anti-alias filter for ADC right channel
AFILT3	37	I/O	Optional anti-alias filter for 2nd ADC left channel
AFILT4	19	I/O	Optional anti-alias filter for 2nd ADC right channel
JDREF	40	I	External resistor for jack detect circuit

Power / Ground			
Signal Name	**Pin#**	**Type**	**Signal Description**
DVDD_CORE	1,9	P	Digital core power. 3.3V
DVSS	4,7	P	Digital VSS
AVDD1	25	P	Analog VDD
AVDD2	38	P	Analog VDD
AVSS1	26	P	Analog VSS
AVSS2	42	P	Analog VSS

Note: I = Input, O = Output, A = Analog, P = Power / Ground

HIGH DEFINITION AUDIO LINK PROTOCOL

Link Signaling

The link protocol defines the digital serial interface that connects High Definition Audio codecs to the audio controller, and is not compatible with the previous AC97 protocol. The link is controller synchronous, based on a fixed 24MHz BITCLK and is purely isochronous without any flow control.

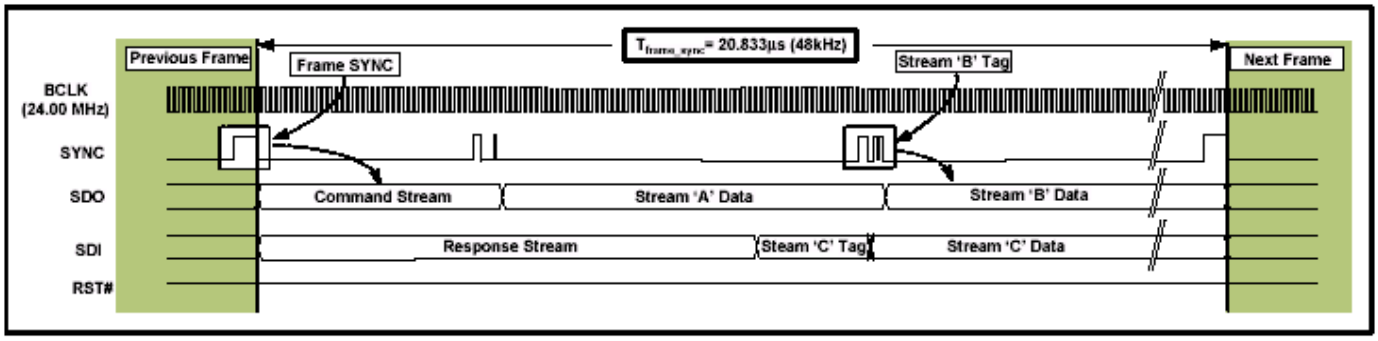


Figure 3. High Definition Audio Link Conceptual View

Signal Definitions

Table 3. Link Signal Description

Signal Name	Source	Type	Description
BITCLK	Controller	I	24MHz clock
SYNC	Controller	I	Global 48KHz Frame Sync and outbound tag signal
SDO	Controller	I	Bussed serial data output from controller
SDI	Codec & controller	I/O	Point-to-point serial data. Controller has a weak pull down
RESETN	Controller	I	Global active low reset signal

BITCLK is the 24MHz clock sourced from the controller and connecting to all codecs on the link.

SYNC marks input and output frame boundaries (Frame Sync) as well as identifying outbound data streams (stream tags). SYNC is always sourced from the controller and connects to all codecs on the link.

SDO is driven by the controller to all codecs on the link. Compared with AC97, the SDO is double pumped with respect to both rising and falling edges of BITCLK in order to increase the bandwidth required for High Definition Audio link.

SDI is a point-to-point data signal driven by the codec to the controller. Because the bandwidth requirement is not that high compared to SDO, data is single pumpled with respect to only the rising edge of BITCLK. The controller is required to implement weak pulldowns on all SDI signals.

RESETN is sourced from the controller and connects to all codecs on the link. Assertion of RESETN results install link interface logic being reset to default power on state.

Figure 4 shows the timing diagram of BITCLK, SYNC, SDO and SDI.

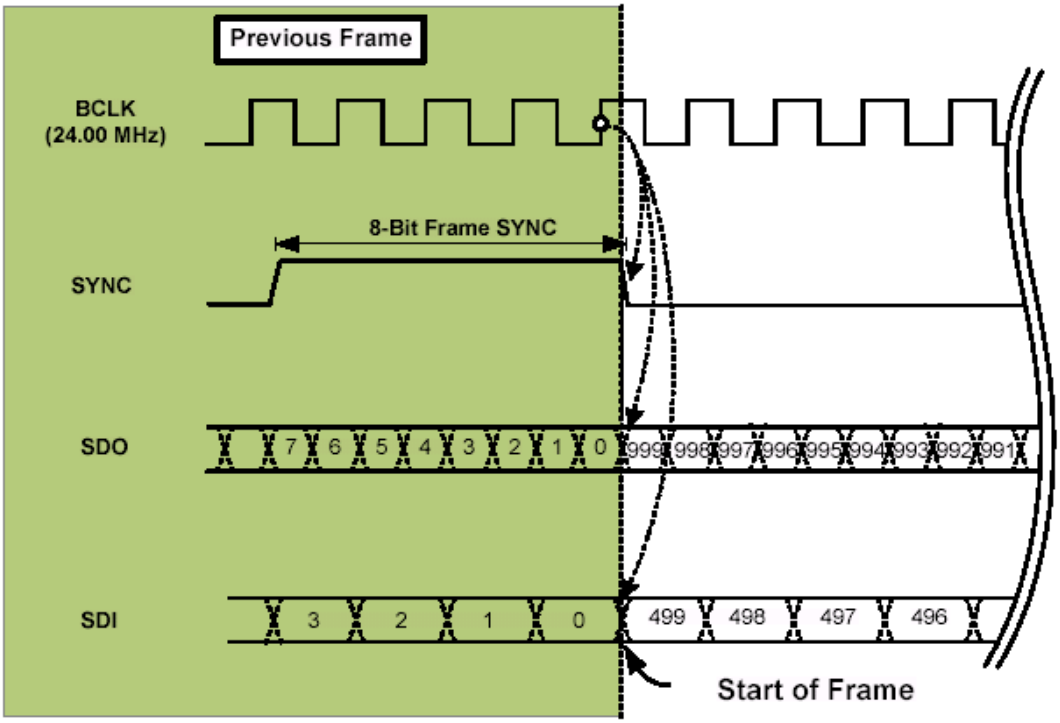


Figure 4. Bit Timing Diagram

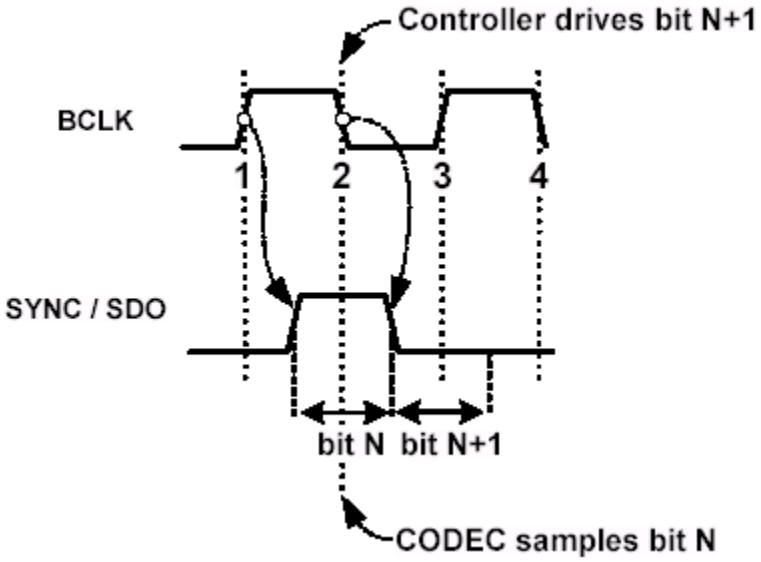


Figure 5. SYNC and SDO Timing Relative to BITCLK

Figure 5 shows that both SYNC and SDO may be toggled with respect to either edge of BITCLK. In particular, bit cell n+1 is driven by the controller on SDO with respect to clock edge #2, and is sampled by the codec with respect to the subsequent clock edge, #3 and so forth.

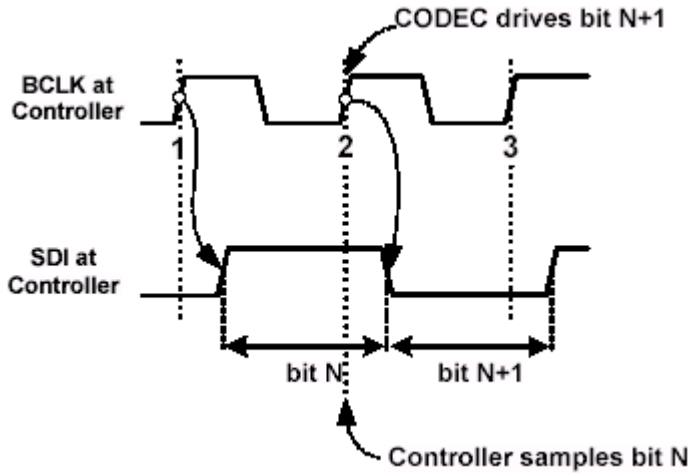


Figure 6. SDI Timing Relative to BITCLK

Figure 6 shows that SID may only be toggled with respect to the rising edge of BITCLK. In particular, bit cell n+1 is driven by the codec on SDI with respect to rising clock edge #2 and is sampled by the controller with respect to the subsequent rising clock edge, #3 and so forth.

Signaling Topology

The following diagram shows a typical system with one controller and its associated codecs.

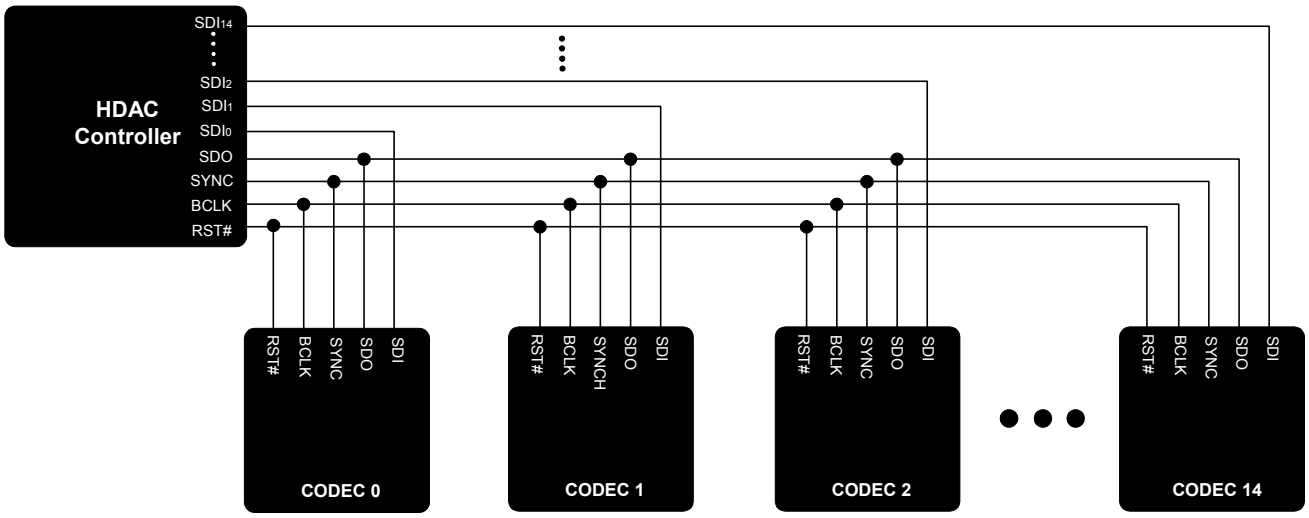


Figure 7. Basic High Definition Audio System

Frame Composition

A frame is defined as a 20.833us window of time marked by the falling edge of the Frame Sync marker, which identifies the start of each frame. The controller is responsible for generating the Frame Sync marker, which is a high-going pulse on SYNC, exactly four BITCLK in width.

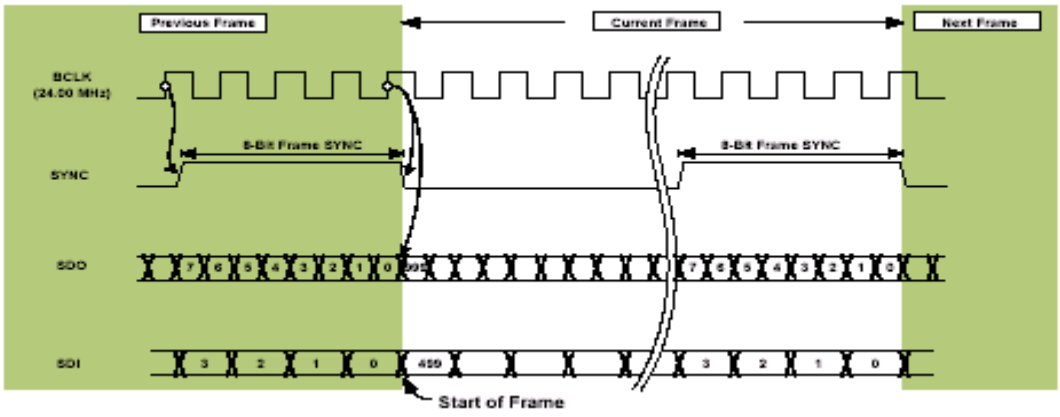


Figure 8. Frames Demarcation

Both inbound and outbound frames are made up of three major components, specifically:

- A single Command / Response Field
- Zero or more Stream Packets
- A Null Field to fill out the frame

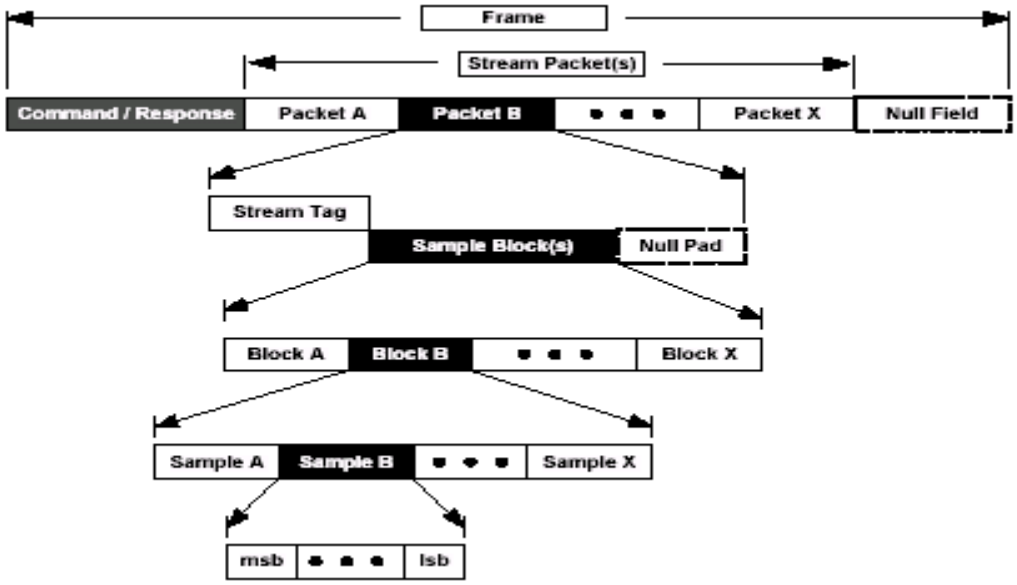


Figure 9. Frame Composition

Command / Response Field is used for link and codec management. One of these fields appears exactly once per frame, MSB first, and is always the first field in the frame. It is composed of a 40-bit Command Field on each outbound frame from the controller and a 36-bit Response Field on each inbound frame from the codec.

Stream Tag is the label at the beginning of each stream packet that provides the associated stream ID. All data in one stream packet belongs to a single stream.

Sample Block is a set of one or more samples, the number of which is specified by the "Channels" field of the Stream Descriptor Format registers. Samples in a given sample block are associated with a single given stream, have the same sample size and have the same time reference. And no padding is permitted between samples.

Ordering of samples within a block is always the same for all blocks in a given stream.

Sample is a set of bits providing a single sample point of a single analog waveform.

Null Field is used to fill up the remainder of the bits in each frame that are not used for Command/Response or packets. A null field must be transmitted as logical 0's.

Output Frame

Stream Tags

Outbound stream tags are 8 bits in length and are transmitted at a double pumped rate as side band information on SYNC. It is composed of a 4-bit preamble which is signaled as three SDO bit times high followed by one SDO bit time low. This is immediately followed by a 4-bit Stream ID. Outbound stream tags are transmitted on SYNC so as to align with the last eight data bits of the preceding stream packet or Command Field.

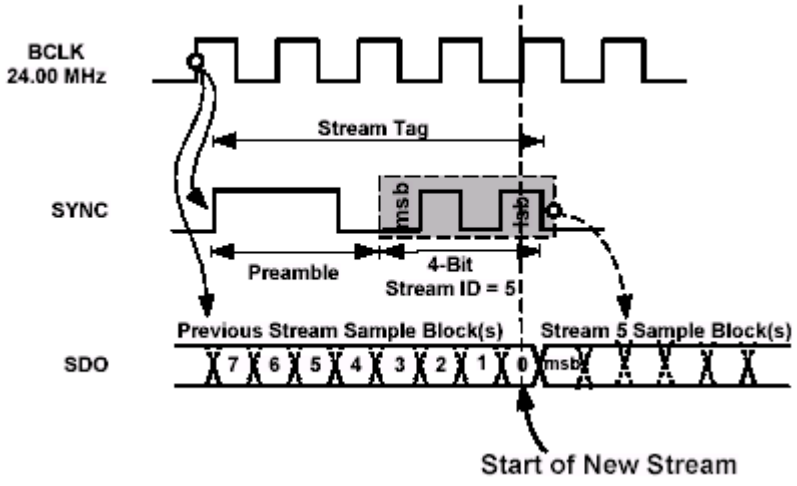


Figure 10. Outbound Stream Tag Format and Transmission

Outbound Frames

Outbound frames start and end between the falling edges of successive Frame Syncs. The first 40 bits are dedicated for the Command field and are sued to send commands to codecs. The controller transmits the tag for the first outbound packet on SYNC during the last eight bit times of the Command field. The sample blocks for the first packet are transmitted on SDO immediately following the Command field. There is no proscribed order in which the different stream packets are to be transmitted. Controllers are required to transmit a null field for the remaining bits within an outbound frame when the transmission of the stream packets completes before the end of the frame.

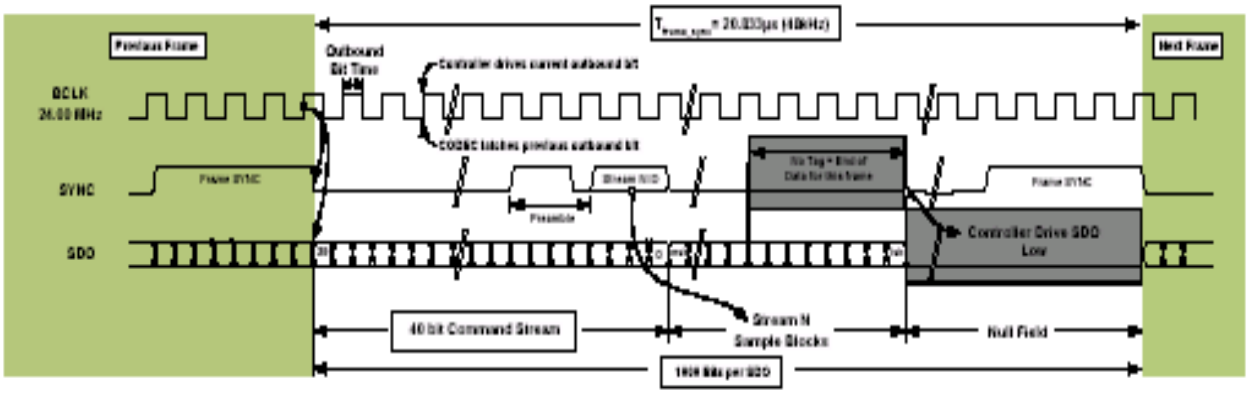


Figure 11. Outbound Frame with Null Field

Input Frame

Stream Tags

An inbound stream tag is 10 bits in length, and is transmitted "in-line" at a single pumped rate on SDI, immediately preceding the associated inbound sample blocks. It is composed of a 4-bit stream ID, followed by a 6-bit data length field that provides the length, in bytes, of all sample blocks with the given stream packet.

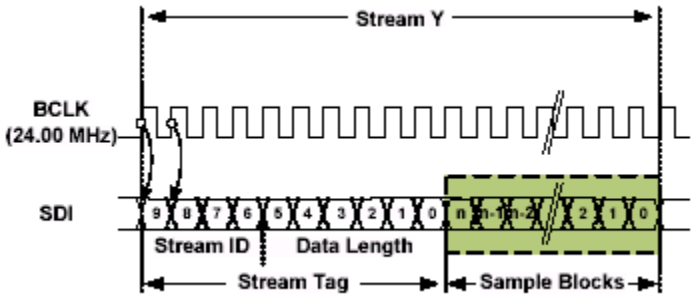


Figure 12. Inbound Tag Format and Transmission

Inbound Frames

Inbound frames start and end between the falling edges of successive Frame Syncs. The first 36 bits of an inbound frame are dedicated for the Response Field, which codecs use for sending responses to controller commands. The codec transmits the first stream packet on SID immediately following the Response Field. A stream tag indicating a packet length of zero must immediately follow the last stream packet to be transmitted. Such a stream tag marks the completion of data transmission within that frame, and the remaining valid bit positions are set to the null field. In the event there are less than 10 valid bit positions remaining in the frame after the last stream packet, then no termination tag is transmitted, and the remaining bits are the null field.

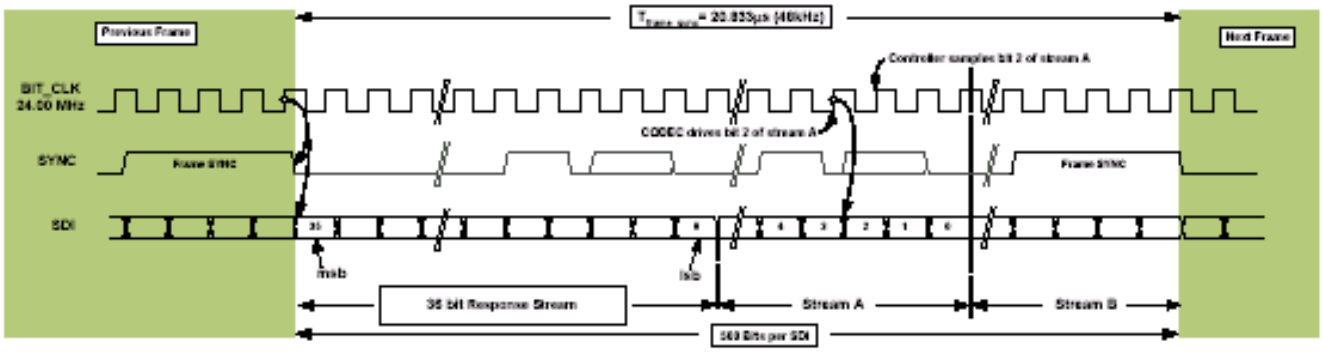


Figure 13. Inbound Frame with No Null Field

Reset and Initialization

Link Reset

A link reset is signaled on the link by assertion of the RESETN signal, and results in all Link interface logic in both codec and controller, including registers, being initialized to their default state. The controller drives all SDO and SYNC outputs low when entering or exiting link reset. A controller may only initiate the link reset entry sequence after completing any currently pending initialization or state change requests.

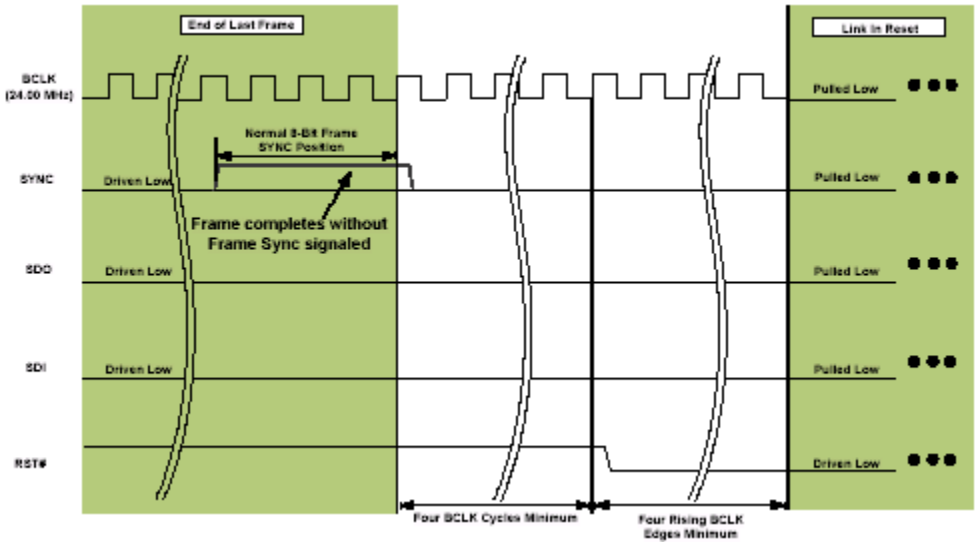


Figure 14. Link Reset Entry Sequence

The sequence when entering link reset is described in the following.

1. The controller synchronously completes the current frame but does not signal Frame Sync during the last eight SDO bit times.
2. The Controller synchronously asserts RESETN four or more BITCLK cycles after the completion of the current frame.
3. BITCLK is stopped a minimum of four clocks after the assertion of RESETN.

In the event of a host bus reset, the above sequence does not complete, and RESETN is asynchronously asserted immediately and unconditionally.

Regardless of the reason for entering Link Reset, it may be exited only under software control and in a synchronous manner.

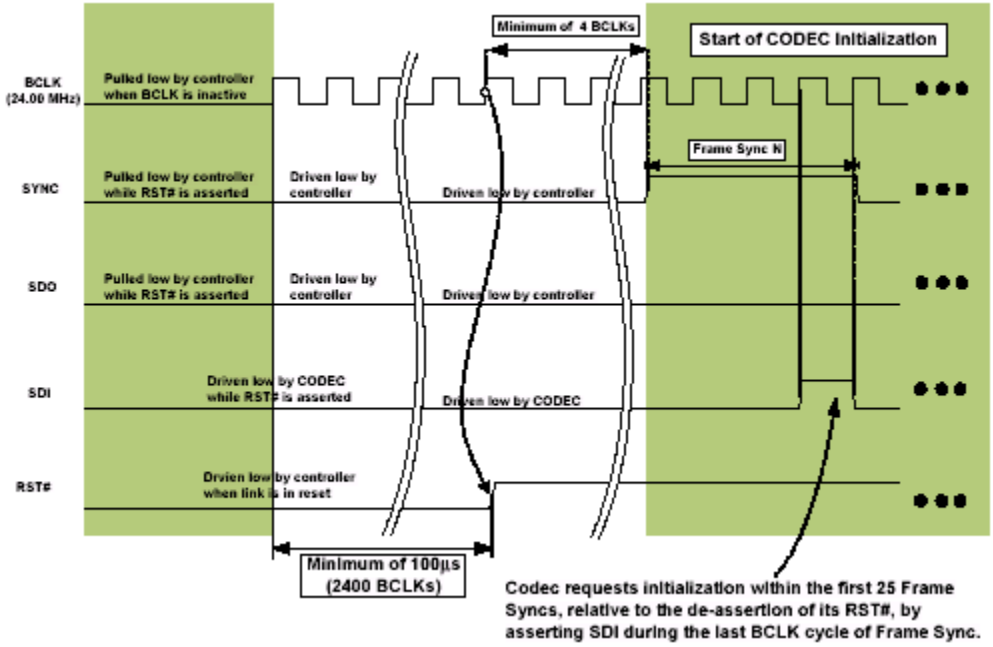


Figure 15. Link Reset Exit Sequence

The sequence when exiting link reset is described in the following:

1. The controller provides a properly running BITCLK for a minimum of 100us (2400 BITCLK cycles or more) before the de-assertion of RESETN. This allows time for codec PLLs to lock.
2. The RESETN signal is de-asserted.
3. The SYNC commences signaling valid frames on the link with the first Frame Sync occurring a minimum of four BITCLK cycles after the de-assertion of RESETN.
4. Codecs must signal an initialization request via SID within the first 25 Frame Syncs relative to the de-assertion of their respective RESETN signal.

Codec Function Group Reset

A codec function group reset is initiated via the Function_Reset verb and results in all logic within the targeted function group being driven to its default or reset state. By default VT1708 does not signal a state change and initialization request on SDI after the Function_Reset verb, and still keeps its codec address previously assigned by the controller. The behavior can be changed by setting a vendor defined register bit for backward compatible with the Rev. 0.7 High Definition Audio Spec. See the Vendor Defined verbs in the Audio Function Group for details.

Codec Initialization

With immediately following the completion of Link Reset sequence (or Function_Reset verb, if enabled by the vendor-defined verb), VT1708 proceeds through a codec initialization sequence, which provides each codec with a unique address by which it can thereafter be referenced with Commands on the SDO signal. During this sequence, the controller provides each requesting codec with a unique address using its attached SDI signals.

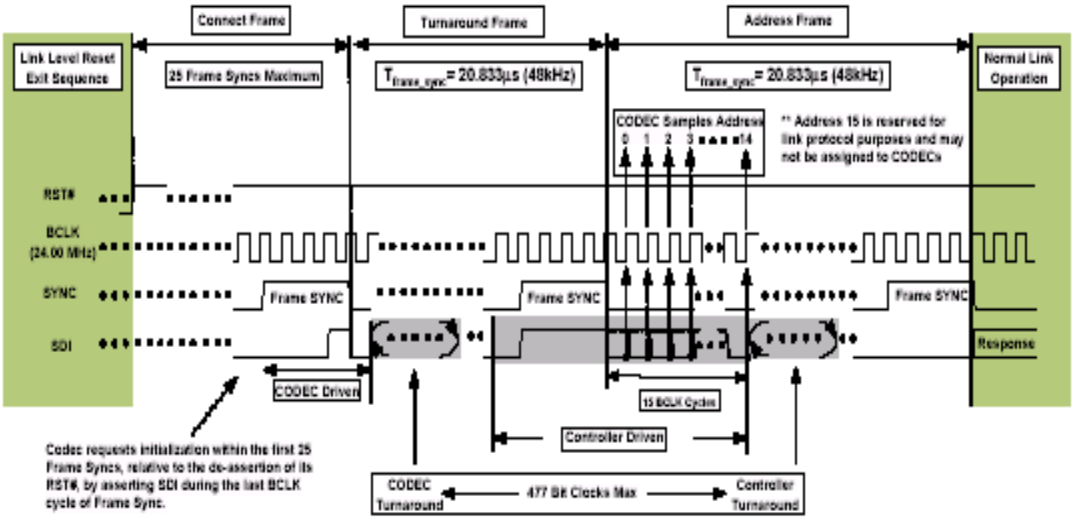


Figure 16. Codec Initialization Sequence

The codec initialization sequence occurs across three contiguous frames immediately following any reset sequence. During these three frames, codecs are required to ignore all outbound traffic present on SYNC & SDO. These three frames, labeled "Connect Frame", "Turnaround Frame" and "Address Frame", are described below.

Connect and Turnaround Frames

In the Connect and Turnaround Frames, the codec signals its request for initialization on SDI and then releases SDI (turnaround) to be driven by the controller in the subsequent address frame.

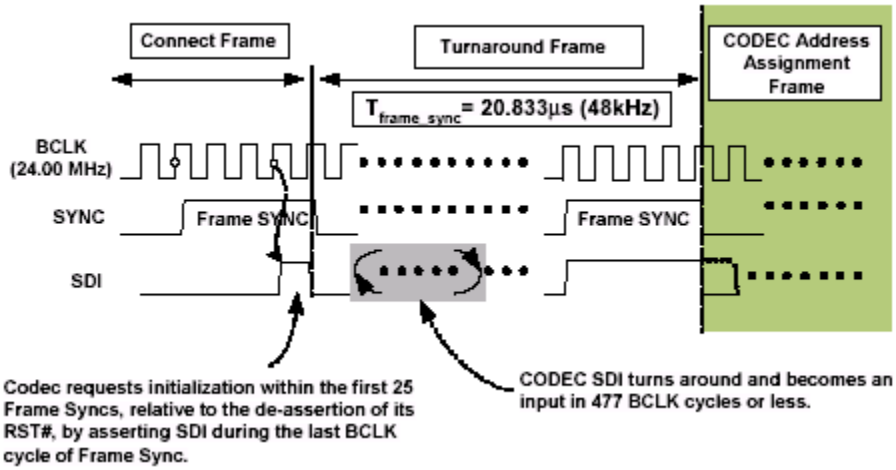


Figure 17. Connect and Turnaround Frames

The codec signals an initialization request by synchronously driving SDI high during last bit clock cycle of Frame Sync. SDI must be asserted for the entire BITCLK cycle and be synchronously de-asserted on the same rising edge of BITCLK as the de-assertion of the Frame Sync. Codecs are only permitted to signal an initialization request on a null input frame, in which no response stream or input streams are being sent.

In the Turnaround Frame, codecs and controllers are required to turn SDI around upon the completion of the Connect Frame. To do this, the codec actively drives SDI low for one BITCLK cycle immediately following the de-assertion of SYNC at the end of the Connect Frame. The codec then puts its SDI drivers in a high impedance state at the end of the first BITCLK cycle in the Turnaround Frame. Four BITCLK cycles before the end of the Turnaround Frame, SYNC and SID are driven high by the controller. The SDI remains driven high through the end of the Turnaround Frame in preparation for the subsequent address frame.

Address Frames

During the Address Frame, SDI is a codec input and driven by the controller beginning in the last four BITCLK periods (Frame Sync) of the Turnaround Frame. The falling edge of Frame Sync marks the start of codec address assignment. Address assignment is indicated by the controller holding each SDI high for the number of BITCLK cycles equal to the numeric ID of that particular SDI. Thus the unique address of the codec becomes the ID of its attached SDI.

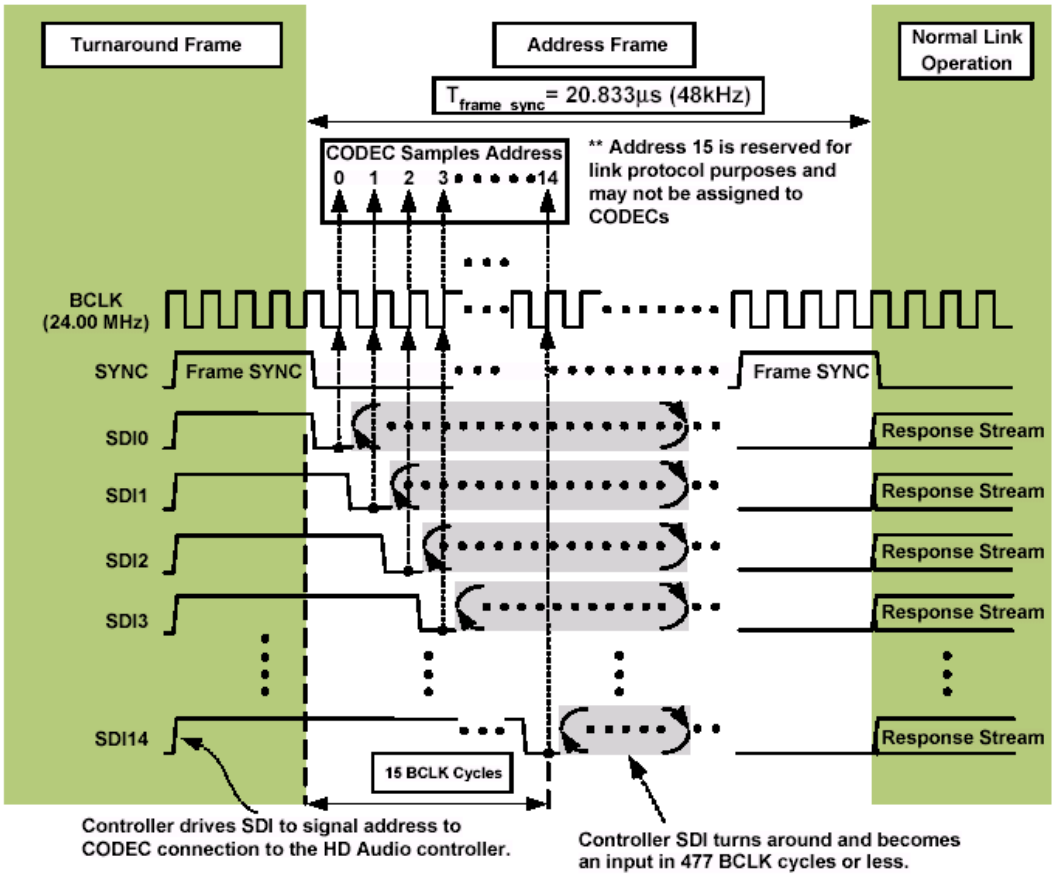


Figure 18. Address Frame

Codecs count from zero to fourteen starting on the rising edge of BITCKL following the de-assertion of Frame Sync, and sample the value of this count for their unique address on the first rising edge of BITCLK in which SYNC and SDI are both sampled low.

The controller must put its SDI drivers in a high impedance state by the rising edge of the 18th BITCLK of the address frame but not before driving each SDI low for at least one clock cycle. The SDI then becomes an input to the controller. Normal link operation starts on the frame following the completion of the Address Frame, and the codec is required to actively drive a valid response field and to be ready to accept commands in this and subsequent frames.

Handling Stream Independent Sample Rates

Unlike AC97, the Link is source synchronous and has no codec initiated flow control, the controller generates all sample transfer timing.

Codec Sample Rendering Timing

VT1708 supports all the multiples and submultiples of the base rates of 48K and 44.1K up to the maximum rate of DAC and ADC respectively. For DAC, up to 192K sample rate is supported. For ADC, the maximum rate is 96K.

Table 4. Sample Rates Supported

Multiple	Base Rate 48KHz	Base Rate 44.1KHz
1/6	8KHz	
¼		11.025KHz
1/3	16KHz	
½		22.05KHz
2/3	32KHz	
1	48KHz	44.1KHz
2	96KHz	88.2KHz
4	192KHz	176.4KHz

Link Sample Delivering Timing

For streams whose sample rate is a natural harmonic of 48KHz, the timing is relatively straightforward. The rates in multiple (N) of 48KHz are containing N sample blocks in one frame. For the rates in submultiple (1/N) of 48K, there must be one sample block transmitted every one in N frames, and the intervening N-1 frames will contain no sample for this stream.

Since the link frame rate is fixed at 48KHz, streams using a base rate of 44.1KHz must have samples transmitted on a cadence creating the slightly lower aggregate transmission rate to match the slightly lower rendering rate. For streams running at a sample rate of 44.1KHz, there are occasional frames that will not contain a sample generating the following cadence:

12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)
The dashes indicate frames that do not contain a sample block. The cadence repeats continuously generating exactly 147 sample blocks every 160 frames, and avoids any long-term drift between sample delivery and rendering clock.

Sample rates that are integral multiples of 44.1KHz apply the "12-11" cadence rule just as a 44.1KHz sample rate would, except that the non-empty frames contain multiple (2 or 4) sample blocks instead of just one.

For a sample rate of 22.05KHz, the transmission pattern becomes:
{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{11}-* (repeat)
where
{12} = 1*1*1*1*1*1*1*1*1*1*1*1*
{11} = 1*1*1*1*1*1*1*1*1*1*
and the asterisks * represent a frame in which there is no sample block.

For a sample rate of 11.025KHz, the transmission pattern becomes:
[12]-*[11]-***[11]-***[12]-***[11]-***[11]-***[12]-***[11]-***[11]-***[12]-***[11]-***[11]-***[11]-*** (repeat)**
where
[12] = 1*1***1***1***1***1***1***1***1***1***1***1*****
[11] = 1*1***1***1***1***1***1***1***1***1***1*****
and the asterisks * represent a frame in which there is no sample block.

These framing sequences apply only to the outbound (SDO) data from the controller. Inbound (SDI) data transmitted by the codec is permitted to deviate for minimizing codec buffer management.

Power Management

Whenever the Link is commanded to enter a low power state, it enters the link-reset state. This state is only exited in response to a software command and follows all link rules for exiting the link-reset state.

The Audio Function Group and the analog input / output converter widgets support power control. The whole chip power states can be controlled through the Audio Function Group, while individual DACs and ADCs can also be controlled through the corresponding power state control verbs. Below is the table describing the definition of the power states.

Table 5. Power States Definitions

Power States	Definitions	Referenced with AC97
D0	All power on. Individual ADCs & DACs can be controlled.	
D1	All amplifiers and analog converters are powered down. Register values maintained, and analog reference voltage is still on.	PR0 & PR1 & PR2
D2	Register values maintained, but analog reference voltage is also down.	PR3
D3	Register values maintained, but analog reference voltage is also down.	PR3

WIDGET DESCRIPTIONS

Node ID List

Table 6. Node ID List

Node ID	Name	Input Connection List	Note
00	Root Node	N/A	
01	AFG	N/A	Audio Function Group
10	AOW0	N/A	Analog Output Widget 0
11	AOW1	N/A	Analog Output Widget 1
12	AOW2	N/A	Analog Output Widget 2
13	AOW3	N/A	Analog Output Widget 3
14	DOW0	N/A	Digital Output Widget 0 for S/PDIF TX
15	AIW0	18	Analog Input Widget 0
16	N/A	N/A	N/A
17	MW0	10, 24, 1D, 1E, 21, 13	Analog Mixer
18	SW0	17, 24, 1D, 1E, 21	ADC Input Selection
19	SW1	11	AOW1 Volume
1A	SW2	12	AOW2 Volume
1B	SW3	13	AOW3 Volume
1C	PW0	19	Port A
1D	PW1	1A	Port B
1E	PW2	19	Port C
1F	PW3	17	Port D
20	PW4	13, 17	Port E
21	PW5	1B	Port F
22	PW6	1A	Port G
23	PW7	1B	Port H
24	PW8	N/A	Pin Widget 8 for CD Input
25	PW9	14	Pin Widget 9 for S/PDIF TX
26	PW10	N/A	Pin Widget 10
27	AIW1	21	Analog Input Widget 1

Root node (Node ID = 00)

Get Parameter Verb (Verb ID = F00h)

Get Vendor ID (Payload = 00h) **Response 32'h11061708**

Bit	Attr.	Description	Response Value
31:16	R	**Vendor ID**	16'h1106
15:0	R	**Device ID**	16'h1708

Get Revision ID (Payload = 02h) **Response 32'h00100000**

Bit	Attr.	Description	Response Value
31:24	R	**Reserved**	—
23:20	R	**MajRev.** The major revision number (left of the decimal) of the High Definition Audio specification to which the codec is fully compliant.	4'b0001
19:16	R	**MinRev.** The minor revision number (right of the decimal) of the High Definition Audio specification to which the codec is fully compliant.	4'b0000
15:8	R	**Revision ID**	8'b00000000
7:0	R	**Stepping ID**	8'b00000000

Get Subordinate Node Count (Payload = 04h) **Response 32'h00010001**

Bit	Attr.	Description	Response Value
31:24	R	**Reserved**	—
23:16	R	**Starting Node Number**	8'h01
15:8	R	**Reserved**	—
7:0	R	**Total Number of Nodes.** (Only 1 Audio Function Group in the codec)	8'h01

Audio Function Group (Node ID = 01)

Get Parameter Verb (Verb ID = F00h)

Get Subordinate Node Count (Payload = 04h) **Response 32'h00100018**

Bit	Attr.	Description	Response Value
31:24	R	**Reserved**	—
23:16	R	**Starting Node Number**	8'h10
15:8	R	**Reserved**	—
7:0	R	**Total Number of Nodes**	8'h18

Get Function Group Type (Payload = 05h) **Response 32'h00000001**

Bit	Attr.	Description	Response Value
31:9	R	**Reserved**	—
8	R	1'b0: Unsolicited Response not supported	
7:0	R	8'h01: Audio Function Group	

Get Function Group Capabilities (Payload = 08h) **Response 32'h00000000**

Bit	Attr.	Description	Response Value
31:17	R	**Reserved**	—
16	R	**Beep Gen**	1'b0
15:12	R	**Reserved**	—
11:8	R	**Input Delay**	
7:4	R	**Reserved**	—
3:0	R	**Output Delay**	

Get Supported Power States (Payload = 0Fh) **Response 32'h0000000F**

Bit	Attr.	Description	Response Value
31:4	R	**Reserved**	—
3	R	**D3Sup**	
2	R	**D2Sup**	
1	R	**D1Sup**	
0	R	**D0Sup**	

Subsystem ID Control Verbs (Verb ID = F20h & 720h – 723h)

		Verb ID	Payload
Get	Get Subsystem ID	F20h	8'b0
Set1	Set Subsystem ID[7:0]	720h	Subsystem ID [7:0]
Set2	Set Subsystem ID[15:8]	721h	Subsystem ID [15:8]
Set3	Set Subsystem ID[23:16]	722h	Subsystem ID [23:16]
Set4	Set Subsystem ID[31:24]	723h	Subsystem ID [31:24]

Response 32'h11060000

Bit	Attr.	Description	Response Value
31:16	R	**Manufacturer ID**	16'h1106
15:8	R	**Board SKU**	8'h00
7:0	R	**Assembly ID**	8'h00

Note: All 32 bits in the Subsystem ID register are writeable with the power-on default value of **32'h11060000.** The system board BIOS can change the values during power up sequence to precisely describe the information about the motherboard so that the OS can load the correct driver.

Power State Verbs (Verb ID = F05h & 705h)

For whole chip power down control.

		Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 8'h03: Power State is D3

Response

Bit	Attr.	Description
31:8	R	0
7:4	R	**PS-Act.** Same as PS-Set for AFG.
3:0	R	PS-Set

Function Reset Verb (Verb ID = 7FFh)

		Verb ID	Payload
Function Reset	Function Reset	7FFh	8'b0

Vendor Defined Verbs (Verb ID = F70h – F7Fh)

		Verb ID	Payload
Set	Set Vendor Defined Control Byte 0 **VDCB0**	F70h	
Set	Set Vendor Defined Control Byte 1 **VDCB1**	F71h	
Set	Set Vendor Defined Control Byte 2 **VDCB2**	F72h	
Set	Set Vendor Defined Control Byte 3 **VDCB3**	F73h	
Get	Get Status	F74h	8'b0

Bit	Attr.	Description
31	R/W1C	**Analog Signal Self-Test High Threshold Passed** Set to 1 if the amplitude of the ADC output is above the threshold value defined in **VDCB5.** Clear to 0 if **AST_ENABLE** is 0, or write 1 to this bit to clear.
30	R/W1C	**Analog Signal Self-Test Low Threshold Passed** Set to 1 if the amplitude of the ADC output is below the threshold value defined in **VDCB4.** Clear to 0 if **AST_ENABLE** is 0, or write 1 to this bit to clear.
29	R	**Analog Self Test Zero-Crossing Result** 1: Left channel and right channel are equal 0: Fail
28	R/W	**Vendor Defined S/PDIF Test Bit**
27	R/W	**Vendor Defined S/PDIF Test Bit**
26	R/W	**PLL Bypass** 1: the PLL outputs are bypassed, and BCLK / 2 is used as internal audio clock source for DACs and ADCs. 0: Normal operation
25	R/W	**Codec Function Group Reset Response Control** 0: Codec does not signal a state change and initialization request on SDI after the Function Group Reset verb. (default) The codec keeps the address previously assigned by the controller. 1: Codec signals a state change and initialization request on SDI after the Function Group Reset verb, as described in Rev. 0.7 of the High Definition Audio specification. This is for compatibility concern when interfacing some older HD controller chip. This bit is set by the driver after power up, and can only be cleared by the Link Reset. The Function Group Reset Verb cannot change its value.
24	R/W	**ADC DC-offset Removal Control** The default setting of "0" ensures that the circuit is disabled at power up. When set to "1", the DC-offset cancellation circuit will be enabled. This helps to maximize recording quality by removing white noise. The transfer function of this digital high-pass filter is: $H(z) = (1-Z^{-1}) / (1-0.9995Z^{-1})$
23:20	R	**Analog Self Test Zero-Crossing High Counter Value.** Reflects the number of zero-crossing events when the zero-crossing timer times out. Clear to 0 if **AST_ENABLE** is zero.
19:16	R/W	**Analog Self Test Zero-Crossing Low Counter Value.** Reflects the number of zero-crossing events 4 frames (8 frames if **ZC_ADJ** = 1) before the zero-crossing timer times out. Clear to 0 if **AST_ENABLE** is zero.
15	R/W	**ZC_ADJ.** For fine-tuning the zero-crossing detection timing.
14	R/W	1: PLL2 output is routed to pin 48 for testing purpose. 0: Normal operation.
13	R/W	1: PLL1 output is routed to pin 48 for testing purpose. 0: Normal operation.

12	R	**PLL Self-Test Status** 1: PLL self-test passed 0: PLL self-test failed Cleared to 0 if **PLLST_ENABLE** is 0.
11	R/W	**PLL Self-Test Mode Enable (PLLST_ENABLE)** When set to 1, the 2 internal PLL self-test counters start to count. Counter 1 is based on the 12.288MHz clock derived from PLL1 output, and counter 2 based on the 11.2896MHz derived from PLL2 output. When counter 1 reaches 960 (3C0h), the self-test circuit checks counter 2 value to see if it's between 880 (370h) to 884 (374h). If so, PLL self-test status in bit 13 is set to 1.
10	R/W	1: Enable both PLL1 & PLL2 regardless of the sample rate setting. 0: Normal operation.
9	R	When read as 1, AIW1 digital self test (left & right output comparison) is passed. Set to 1 by **INIT** bit.
8	R	When read as 1, AIW0 digital self test (left & right output comparison) is passed. Set to 1 by **INIT** bit.
7	R	When read as 1, AOW3 digital self test (left & right output comparison) is passed. Set to 1 by **INIT** bit.
6	R	When read as 1, AOW2 digital self test (left & right output comparison) is passed. Set to 1 by **INIT** bit.
5	R	When read as 1, AOW1 digital self test (left & right output comparison) is passed. Set to 1 by **INIT** bit.
4	R	When read as 1, AOW0 digital self test (left & right output comparison) is passed. Set to 1 by **INIT** bit.
3	R/W	**DAC to ADC Digital Loopback Enable.** (For testing purpose only.) When this bit is set to 1, AOW0 is looped back to AIW0, AOW1 is looped back to AIW1, in the digital domain.
2	R/W	**Initialization (INIT).** (This is for testing only and should not be set during normal operation.) When this bit is set to 1, the internal FIFOs, sigma-delta circuits & comb filters are reset to 0.
1:0	R/W	**Analog Current Setting Bits** Normally these bits should be left at default when analog operating is at 5V supply. The four possible settings adjust the power consumption of the analog section. The power-up default 00b sets the codec for the best overall analog performance at 5V. At 3.3V analog supply, 10b should be set for the lowest power instead of default 00b. This mode is desirable for system designs with limited power budget such as battery operated portable devices. Setting to 11b puts the codec to its best A- A mixer performance overall. 2'b00: Normal (1X) 2'b01: Reduced (4/5 X) 2'b10: Power Miser (2/3 X) 2'b11: Enhanced (4/3 X)

		Verb ID	Payload
Set	Set Vendor Defined Control Byte 4 **VDCB4**	F78h	
Set	Set Vendor Defined Control Byte 5 **VDCB5**	F79h	
Set	Set Vendor Defined Control Byte 6 **VDCB6**	F7Ah	
Set	Set Vendor Defined Control Byte 7 **VDCB7**	F7Bh	
Get	Get Status	F7Ch	8'b0

Bit	Attr.	Description
31	R/W	**Analog Signal Self-Test Enable (AST_ENABLE)**
30	R/W	**Analog Signal Self-Test Source Selection** 1: Use the output data from AIW1. 0: Use the output data from AIW0. (default)
29:26	R/W	**Vendor Defined Test Bits for Jack Detection Circuit**
25:16	R/W	**Analog Signal Self-Test Zero-Crossing Timer Threshold** If **AST_ENABLE** is set to 1, an internal timer starts to count and increments by 1 every frame. 4 frames before the timer reaches the threshold value defined here, the value of the zero-crossing detection counter is latched into **VDCB2[3:0].** When this timer reaches the threshold value defined here, the value of the zero-crossing detection counter is latched into **VDCB2[7:4].** **By carefully selected** zero-crossing timer threshold and the information returned from **VDCB2,** the pitch of the ADC output can be decided.
15:8	R/W	**Analog Signal Self-Test High Threshold Value VDCB5**
7:0	R/W	**Analog Signal Self-Test Low Threshold Value VDCB4**

		Verb ID	Payload
Set	Set Vendor Defined Control Byte 8 **VDCB8**	F80h	
Set	Set Vendor Defined Control Byte 9 **VDCB9**	F81h	
Set	Set Vendor Defined Control Byte 10 **VDCB10**	F82h	
Set	Set Vendor Defined Control Byte 11 **VDCB11**	F83h	
Get	Get Status	F84h	8'b0

Bit	Attr.	Description
31:16	R/W	**Reserved**
15:13	R/W	**Reserved**
12	R/W	**Internal Audio Clock Source from EAPD Pin**
11:10	R/W	**Internal Digital Loopback Source Selection for AIW0** 00: from AOW0 01: from AOW1 10: from AOW2 11: from AOW3
9	R/W	**Reserved**
8	R/W	**Power Down Jack Detect Circuit**
7:0	R/W	**SPDIF RX Test Bits VDCB8**

Audio Analog Output Converter Widget (Node ID = 10,11,12,13)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h00000411**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0000: Audio Output Converter Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	1: Power Control Supported
9	R	0: Analog widget, not digital
8	R	0: Connection List is not present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5	R	**Reserved**
4	R	1: Contains format information
3	R	0: No amplifier parameter
2	R	0: Out Amp not present
1	R	0: In Amp not present
0	R	1: Stereo

Supported PCM Size, Rates (Payload = 0Ah) **Response 32'h000A07E0**

Bit	Attr.	Description
31:21	R	**Reserved**
20	R	0: No 32-bit audio format support
19	R	1: 24-bit audio format support
18	R	0: 20-bit audio format support
17	R	1: 16-bit audio format support
16	R	0: 8-bit audio format support
15:12	R	**Reserved**
11	R	0: 384KHz not supported
10	R	1: 192KHz supported
9	R	1: 176.4KHz supported
8	R	1: 96KHz supported
7	R	1: 88.2KHz supported
6	R	1: 48KHz supported
5	R	1: 44.1KHz supported
4	R	0: 32KHz not supported
3	R	0: 22.05KHz not supported
2	R	0: 16KHz not supported
1	R	0: 11.025KHz not supported
0	R	0: 8KHz not supported

Supported Stream Formats (Payload = 0Bh) **Response 32'h00000001**

Bit	Attr.	Description
31:3	R	**Reserved**
2	R	0: No AC3 support
1	R	0: No Float32 support
0	R	1: PCM supported

Supported Power States (Payload = 0Fh) **Response 32'h00000003**

Bit	Attr.	Description
31:4	R	**Reserved**
3	R	0: D3Sup
2	R	0: D2Sup
1	R	1: D1Sup
0	R	1: D0Sup

Converter Format Verbs (Verb ID = Ah & 2h)

		Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Bit	Attr.	Description
15	R	**Stream Type** 0: PCM 1: Non-PCM (not supported)
14	R/W	**Sample Base Rate** 0: 48KHz 1: 44.1KHz
13:11	R/W	**Sample Base Rate Multiple** 000 = x1 : 48K or less 001 = x2 : 96K,88.2K 010 = x3 : Not supported 011 = x4 : 192K 100-111 : Reserved
10:8	R/W	**Sample Base Rate Divisor** 000 = /1 :48K Others: not supported
7	R	**Reserved**
6:4	R/W	**Bits per Sample** 000: 8-bit (not supported) 001: 16-bit 010: 20-bit (not supported) 011: 24-bit 100: 32-bit (not supported)
3:0	R/W	**Number of Channels (CHAN).** Number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

Power State Verbs (Verb ID = F05h & 705h)

For DAC power down control

		Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 (not supported) 8'h03: Power State is D3 (not supported)

Response

Bit	Attr.	Description
31:8	R	0
7:4	R	**PS-Act.** Reports the actual power state of the widget.
3:0	R	**PS-Set**

Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

		Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4] Channel is in bit[3:0]

Audio Digital Output Converter (S/PDIF TX) Widget (Node ID = 14)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h00000211**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0000: Audio Output Converter Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	0: Power Control Not Supported
9	R	1: Digital widget, not analog
8	R	0: Connection List is not present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5	R	**Reserved**
4	R	1: Contains format information
3	R	0: Contains no amplifier parameter
2	R	0: Out Amp Not Present
1	R	0: In Amp Not Present
0	R	1: Stereo

Supported PCM Size, Rates (Payload = 0Ah) **Response 32'h000A07E0**

Bit	Attr.	Description
31:21	R	**Reserved**
20	R	0: No 32-bit audio format support
19	R	1: 24-bit audio format support
18	R	0: 20-bit audio format support
17	R	1: 16-bit audio format support
16	R	0: 8-bit audio format support
15:12	R	**Reserved**
11	R	0: 384KHz not supported
10	R	1: 192KHz supported
9	R	1: 176.4KHz supported
8	R	1: 96KHz supported
7	R	1: 88.2KHz supported
6	R	1: 48KHz supported
5	R	1: 44.1KHz supported
4	R	0: 32KHz not supported
3	R	0: 22.05KHz not supported
2	R	0: 16KHz not supported
1	R	0: 11.025KHz not supported
0	R	0: 8KHz not supported

Supported Stream Formats (Payload = 0Bh) **Response 32'h00000005**

Bit	Attr.	Description
31:3	R	**Reserved**
2	R	1: AC3 support
1	R	0: No Float32 support
0	R	1: PCM supported

Converter Format Verbs (Verb ID = Ah & 2h)

		Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Bit	Attr.	Description
15	R/W	**Stream Type** 0: PCM 1: Non-PCM
14	R/W	**Sample Base Rate** 0: 48KHz 1: 44.1KHz
13:11	R/W	**Sample Base Rate Multiple** 000 = x1 :48K 001 = x2 :96K 010 = x3 :144KHz (not supported) 011 = x4 :192K 100-111: reserved
10:8	R/W	**Sample Base Rate Divisor** 000 = /1 :48K Others: not supported
7	R	**Reserved**
6:4	R/W	**Bits per Sample** 000: 8-bit 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit
3:0	R/W	**Number of Channels (CHAN).** Number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

S/PDIF Converter Control 1 & 2 Verbs (Verb ID = F0Dh & 70Dh, 70Eh)

		Verb ID	Payload
Get	Get Converter Control State	F0Dh	8'b0
Set	Set Converter Control 1	70Dh	SIC[7:0]
Set	Set Converter Control 2	70Eh	SIC[15:8]

S/PDIF IEC Control Bits Format

Bit	Description
15	**Reserved**
14:8	CC[6:0] Category Code
7	L: Generation Level
6	**PRO** 1: Professional mode 0: Consumer mode
5	**AUDIO** 1: Data is non PCM format 0: Data is PCM format
4	**Copy** 1: Copyright is asserted 0: Copyright is not asserted
3	**Pre** 1: Filter preemphasis is 50/15 usec 0: Preemphasis is none
2	**VCFG.** Determines S/PDIF transmitter behavior when data is not being transmitted.
1	**Validity Flag**
0	**DigEn** 1: S/PDIF TX enabled 0: S/PDIF TX disabled

Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

		Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4] Channel is in bit[3:0]

Audio Analog Input Converter Widget (Node ID = 15, 27)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h0010051B**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0001: Audio Input Converter Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	1: Power Control Supported
9	R	0: Analog widget, not digital
8	R	1: Connection List is present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5:	R	**Reserved**
4	R	1: Contains format information
3	R	1: Contains amplifier parameter
2	R	0: Out Amp not present
1	R	1: In Amp present
0	R	1: Stereo

Supported PCM Size, Rates (Payload = 0Ah) **Response 32'h000A0440**

Bit	Attr.	Description
31:21	R	**Reserved**
20	R	0: No 32-bit audio format support
19	R	1: 24-bit audio format support
18	R	0: 20-bit audio format support
17	R	1: 16-bit audio format support
16	R	0: 8-bit audio format support
15:12	R	**Reserved**
11	R	0: 384KHz not supported
10	R	1: 192KHz supported
9	R	0: 176.4KHz not supported
8	R	0: 96KHz not supported
7	R	0: 88.2KHz not supported
6	R	1: 48KHz supported
5	R	0: 44.1KHz not supported
4	R	0: 32KHz not supported
3	R	0: 22.05KHz not supported
2	R	0: 16KHz not supported
1	R	0: 11.025KHz not supported
0	R	0: 8KHz not supported

Supported Stream Formats (Payload = 0Bh) **Response 32'h00000001**

Bit	Attr.	Description
31:3	R	**Reserved**
2	R	0: No AC3 support
1	R	0: No Float32 support
0	R	1: PCM supported

Amplifier Capabilities (Payload = 0Dh) **Response 32'h80061400**

Bit	Attr.	Description
31	R	1: Mute capable
30:23	R	**Reserved**
22:16	R	**Step Size** 7'b0000110: Step size is 1.5dB
15	R	Reserved
14:8	R	**Number of Steps** 7'b0010100: Number of steps is 20 (0dB – 30dB)
7	R	**Reserved**
6:0	R	**Offset** 7'b0000000: Offset 00h is 0dB

Connection List Length (Payload = 0Eh) **Response 32'h00000001**

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Short form
6:0	R	7'b0000001: 1 input available

Supported Power States (Payload = 0Fh) **Response 32'h00000003**

Bit	Attr.	Description
31:4	R	**Reserved**
3	R	0: D3Sup
2	R	0: D2Sup
1	R	1: D1Sup
0	R‘	1: D0Sup

Connection List Entry Control Verbs (Verb ID = F02h)

		Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h00000018 or 32'h00000021

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Independent Node ID
6:0	R	7'b0011000: from SW0 (Node ID = 18h) for AIW0 7'b0100001: from PW5 (Node ID = 21h) for AIW1

Converter Format Verbs (Verb ID = Ah & 2h)

		Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Converter Format

Bit	Attr.	Description
15	R	**Stream Type** 0: PCM 1: Non-PCM (not supported)
14	R	**Sample Base Rate** 0: 48KHz 1: 44.1KHz (not supported)
13:11	R/W	**Sample Base Rate Multiple** 000 = x1 :48K 001 = x2 :96K, 88.2K or 32K (not supported) 010 = x3 :144KHz (not supported) 011 = x4 :192K 100-111: reserved
10:8	R/W	**Sample Base Rate Divisor** 000 = /1 :48K Others: not supported
7	R	**Reserved**
6:4	R/W	**Bits per Sample** 000: 8-bit (not supported) 001: 16-bit 010: 20-bit (not supported) 011: 24-bit 100: 32-bit
3:0	R/W	**Number of Channels (CHAN).** Number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

		Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Get Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being requested (ignored) 0: The input amplifier is being requested
14	W	0
13	W	1: The left amplifier is being requested 0: The right amplifier is being requested
12:4	W	0
3:0	W	**Index Ignored**

Get Response format

Bit	Attr.	Description
31:8	R	0
7	R	1: Amplifier is muted 0: Amplifier is unmuted
6:0	R	**Amplifier Gain Setting** Default is 7'b0000000

Set Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being set (ignored)
14	W	1: The input amplifier is being set
13	W	1: The left amplifier is being set
12	W	1: The right amplifier is being set
11:8	W	**Index Ignored**
7	W	1: Mute 0: Unmute
6:0	W	**Gain Setting**

Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

		Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4] Channel is in bit[3:0]

Power State Verbs (Verb ID = F05h & 705h)

		Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0 8'h01: Power State is D1 8'h02: Power State is D2 (not supported) 8'h03: Power State is D3 (not supported)

For ADC power down control **Response**

Bit	Attr.	Description
31:8	R	0
7:4	R	**PS-Act.** Reports the actual power state of the widget.
3:0	R	**PS-Set**

Mixer Widget (Node ID = 17h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h0020010B**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0010: Audio Mixer Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	0: Power Control not supported
9	R	0: Analog widget, not digital
8	R	1: Connection List is present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5:	R	**Reserved**
4	R	0: No format information
3	R	1: Amplifier parameter
2	R	0: Out Amp not present
1	R	1: In Amp present
0	R	1: Stereo

Input Amplifier Capabilities (Payload = 0Dh) **Response 32'h80061F17**

Bit	Attr.	Description
31	R	1: Mute capable
30:23	R	**Reserved**
22:16	R	**Step Size** 7'b0000110: Step size is 1.5dB (no effect)
15	R	**Reserved**
14:8	R	**Number of Steps** 7'b0011111: Number of steps is 31 (-34.5dB – 12dB)
7	R	**Reserved**
6:0	R	**Offset** 7'b0010111: Offset 17h is 0dB

Connection List Length (Payload = 0Eh) **Response 32'h00000006**

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Short form
6:0	R	7'b0000110: 6 inputs available

Connection List Entry Control Verbs (Verb ID = F02h)

		Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h1E1D2410 or 32'h00001321

Bit	Attr.	Description	
		Offset index n = 0	**Offset index n = 4**
31:24	R	**Connection List Entry n+3** 8'h1E (PW2, PortC)	8'h00
23:16	R	**Connection List Entry n+2** 8'h1D (PW1, PortB)	8'h00
15:8	R	**Connection List Entry n+1** 8'h24 (PW8, CD)	**Connection List Entry n+1** 8'h13 (AOW3)
7:0	R	**Connection List Entry n** 8'h10 (AOW0)	**Connection List Entry n** 8'h21 (PW5, PortF)

Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

		Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Get Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being requested (ignored) 0: The input amplifier is being requested
14	W	0
13	W	1: The left amplifier is being requested 0: The right amplifier is being requested
12:4	W	0
3:0	W	**Index**

Get Response format

Bit	Attr.	Description
31:8	R	0
7	R	1: Amplifier is muted 0: Amplifier is unmated
6:0	R	**Amplifier Gain Setting** Default is 7'b0001000

Set Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being set (ignored)
14	W	1: The input amplifier is being set
13	W	1: The left amplifier is being set
12	W	1: The right amplifier is being set
11:8	W	**Index Ignored**
7	W	1: Mute 0: Unmute
6:0	W	**Gain Setting**

Selector Widget SW0 (Node ID = 18h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h00300101**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0011: Audio Selector Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	0: Power Control Not Supported
9	R	0: Analog widget, not digital
8	R	1: Connection List is present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5	R	**Reserved**
4	R	0: No format information
3	R	0: Amplifier parameter
2	R	0: Out Amp not present
1	R	0: In Amp not present
0	R	1: Stereo

Connection List Length (Payload = 0Eh) **Response 32'h00000005**

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Short form
6:0	R	7'b0000101: 5 input available

Connection Select Control Verbs (Verb ID = F01h & 701h)

		Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The connection index value to be set

Connection List Entry Control Verbs (Verb ID = F02h)

		Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h1E1D2417 or 32'h00000021

Bit	Attr.	Description	
		Offset index n = 0	**Offset index n = 1**
31:24	R	**Connection List Entry n+3** 8'h1E (PW2, PortC)	8'h00
23:16	R	**Connection List Entry n+2** 8'h1D (PW1, PortB)	8'h00
15:8	R	**Connection List Entry n+1** 8'h24 (PW8, CD)	8'h00
7:0	R	**Connection List Entry n** 8'h17 (MW0)	**Connection List Entry n** 8'h21 (PW5, PortF)

Selector Widget SW1-SW3 (Node ID = 19h – 1Bh)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h0030010D**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0011: Audio Selector Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	0: Power Control Not Supported
9	R	0: Analog widget, not digital
8	R	1: Connection List is present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5	R	**Reserved**
4	R	0: No format information
3	R	1: Amplifier parameter
2	R	1: Out Amp present
1	R	0: In Amp not present
0	R	1: Stereo

Connection List Length (Payload = 0Eh) **Response 32'h00000001**

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Short form
6:0	R	7'b0000001: 1 input available

Amplifier Capabilities (Payload = 12h) **Response 32'h80061B1B**

Bit	Attr.	Description
31	R	1: Mute capable
30:23	R	**Reserved**
22:16	R	**Step Size** 7'b0000110: Step size is 1.5dB
15	R	**Reserved**
14:8	R	**Number of Steps** 7'b0011011: Number of steps is 27 (-40.5dB – 0dB)
7	R	**Reserved**
6:0	R	**Offset** 7'b0011011: Offset 1Bh is 0dB

Connection Select Control Verbs (Verb ID = F01h & 701h)

		Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The connection index value to be set

Connection List Entry Control Verbs (Verb ID = F02h)

		Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h00000011 or 32'h00000012 or 32'h00000013

Bit	Attr.	Description
31:24	R	8'h00
23:16	R	8'h00
15:8	R	8'h00
7:0	R	**Connection List Entry n** 8'h11 (AOW1) for SW1 8'h12 (AOW2) for SW2 8'h13 (AOW3) for SW3

Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

		Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Get Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being requested 0: The input amplifier is being requested (ignored)
14	W	0
13	W	1: The left amplifier is being requested 0: The right amplifier is being requested
12:4	W	0
3:0	W	**Index Ignored**

Get Response format

Bit	Attr.	Description
31:8	R	0
7	R	1: Amplifier is muted 0: Amplifier is unmuted
6:0	R	**Amplifier Gain Setting** Default is 7'b0000000

et Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being set
14	W	1: The input amplifier is being set (ignored)
13	W	1: The left amplifier is being set
12	W	1: The right amplifier is being set
11:8	W	**Index Ignored**
7	W	1: Mute 0: Unmute
6:0	W	**Gain Setting**

Pin Widget PW0 (Node ID = 1Ch)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h0040010D**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0100: Pin Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	**0: Power Control not Supported**
9	R	0: Analog widget, not digital
8	R	1: Connection List is present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5	R	**Reserved**
4	R	0: Doesn't contain format information
3	R	1: Contain amplifier parameter
2	R	1: Out Amp Present
1	R	0: In Amp not present
0	R	1: Stereo

Pin Capabilities (Payload = 0Ch) **Response 32'h0000001C**

Bit	Attr.	Description
31:17	R	**Reserved**
16	R	**EAPD capable**. Read as 0.
15:8	R	**VRef Control**. Read as 8'h00
7	R	**Reserved**
6	R	**Balanced I/O Pins**. Read as 0.
5	R	**INPUT CAPABLE. READ AS 0.**
4	R	**Output Capable**. Read as 1.
3	R	**Headphone Drive Capable**. Read as 1
2	R	**Presence Detect Capable**. Read as 1.
1	R	**Trigger Required**. Read as 0.
0	R	**Impedance Sense Capable**. Read as 0.

Connection List Length (Payload = 0Eh) **Response 32'h00000001**

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Short form
6:0	R	7'b0000001: Only 1 input available

Amplifier Capabilities (Payload = 12h) **Response 32'h00000000**

Bit	Attr.	Description
31	R	0: Mute not capable
30:23	R	**Reserved**
22:16	R	**Step Size** 7'b0000000: Step size fixed
15	R	**Reserved**
14:8	R	**Number of Steps** 7'b0000000: Number of steps is fixed
7	R	**RESERVED**
6:0	R	**Offset** 7'b0000000: Offset is 0dB

Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

		Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Get Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being requested 0: The input amplifier is being requested (ignored)
14	W	0
13	W	1: The left amplifier is being requested 0: The right amplifier is being requested
12:4	W	0
3:0	W	**Index**

Get Response format

Bit	Attr.	Description
31:8	R	0
7	R	0: Amplifier is unmuted
6:0	R	**Amplifier Gain Setting** Fixed at 7'b0000000

Set Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being set
14	W	1: The input amplifier is being set (ignored)
13	W	1: The left amplifier is being set
12	W	1: The right amplifier is being set
11:8	W	**Index Ignored**
7	W	1: Mute (not supported) 0: Unmute
6:0	W	**Gain Setting**

Connection List Entry Control Verbs (Verb ID = F02h)

		Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h00000019

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Independent Node ID
6:0	R	7'b0011001 (from SW1)

Pin Widget Control Verbs (Verb ID = F07h & 707h)

		Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attr.	Description
7	R/W	**Headphone Enable** 0: Disabled 1: Headphone enabled
6	R/W	**Output Enable** 0: Disabled 1: Output enabled
5	R	**Input Enable** 0: Disabled 1: Input enabled (not supported)
4:3	R	0
2:0	R	0: reserved

Pin Sense Control Verbs (Verb ID = F09h & 709h)

		Verb ID	Payload
Get	Get Pin Sense Control	F07h	8'b0
Set	Set Pin Sense Control	707h	PinCntl

PinCntl Format

Bit	Attr.	Description
7:1	R	**Reserved**
0	R	Right Channel Sense (not supported)

Response

Bit	Attr.	Description
31	R	**Presence Detect** 1: Jack plugged in 0: Nothing plugged in.
30:0	R	**Reserved**

Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

		Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format **Response 32'b00000011**

Bit	Attr.	Description
31:30	R/W	**Port Connectivity**, 2'b00 (Connected to a jack)
29:24	R/W	**Location**, 6'b000000
23:20	R/W	**Default Device**, 4'b0000 (Line-out)
19:16	R/W	**Connection Type**, 4'b0000
15:12	R/W	**Color**, 4'b0000 (unknown)
11:8	R/W	**Misc**, 4'b0000
7:4	R/W	**Default Association**, 4'b0001
3:0	R/W	**Sequence**, 4'b0001 (surround out in association # 1)

Pin Widget PW3, PW4 (Node ID = 1Fh, 20h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h0040010D**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0100: Pin Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	**0: Power Control not Supported**
9	R	0: Analog widget, not digital
8	R	1: Connection List is present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5	R	**Reserved**
4	R	0: Doesn't contain format information
3	R	1: Contain amplifier parameter
2	R	1: Out Amp Present
1	R	0: In Amp not present
0	R	1: Stereo

Pin Capabilities (Payload = 0Ch) **Response 32'h0000001C**

Bit	Attr.	Description
31:17	R	**Reserved**
16	R	**EAPD Capable**. Read as 0.
15:8	R	**VRef Control**. Read as 8'h00
7	R	**Reserved**
6	R	**Balanced I/O Pins**. Read as 0.
5	R	**INPUT CAPABLE. READ AS 0.**
4	R	**Output Capable**. Read as 1.
3	R	**Headphone Drive Capable**. Read as 1
2	R	**Presence Detect Capable**. Read as 1.
1	R	**Trigger Required**. Read as 0.
0	R	**Impedance Sense Capable**. Read as 0.

Connection List Length (Payload = 0Eh) **Response 32'h00000001 or 32'h00000002**

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Short form
6:0	R	7'b0000001: Only 1 input available for PW3 7'b0000010: 2 inputs available for PW4

Amplifier Capabilities (Payload = 12h) **Response 32'h80061B1B**

Bit	Attr.	Description
31	R	1: Mute capable
30:23	R	**Reserved**
22:16	R	**Step Size** 7'b0000110: Step size is 1.5dB
15	R	**Reserved**
14:8	R	**Number of Steps** 7'b0011011: Number of steps is 28 (-40.5dB – 0dB)
7	R	**Reserved**
6:0	R	**Offset** 7'b0011011: Offset 1Bh is 0dB

Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

		Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Get Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being requested 0: The input amplifier is being requested (ignored)
14	W	0
13	W	1: The left amplifier is being requested 0: The right amplifier is being requested
12:4	W	0
3:0	W	**Index**

Get Response format

Bit	Attr.	Description
31:8	R	0
7	R	1: Amplifier is muted 0: Amplifier is unmated
6:0	R	**Amplifier Gain Setting** Default is 7'b0000000

Set Payload Format

Bit	Attr.	Description
15	W	1: The output amplifier is being set
14	W	1: The input amplifier is being set (ignored)
13	W	1: The left amplifier is being set
12	W	1: The right amplifier is being set
11:8	W	**Index Ignored**
7	W	1: Mute 0: Unmute
6:0	W	Gain setting

Connection Select Control Verbs (Verb ID = F01h & 701h)

Note: For PW4 only.

		Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The connection index value to be set

Connection List Entry Control Verbs (Verb ID = F02h)

		Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h00000017 or 32'h00001317

Bit	Attr.	Description
31:16	R	**Reserved**
15:8		8'b00010011 (from AOW3) for PW4 only.
7	R	0: Independent Node ID
6:0	R	7'b0010111 (from MW0)

Pin Widget Control Verbs (Verb ID = F07h & 707h)

		Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attr.	Description
7	R/W	**Headphone Enable** 0: Disabled 1: Headphone enabled
6	R/W	**Output Enable** 0: Disabled 1: Output enabled
5	R	**Input Enable** 0: Disabled 1: Input enabled (not supported)
4:3	R	0
2:0	R	0: reserved

Pin Sense Control Verbs (Verb ID = F09h & 709h)

		Verb ID	Payload
Get	Get Pin Sense Control	F07h	8'b0
Set	Set Pin Sense Control	707h	PinCntl

PinCntl Format

Bit	Attr.	Description
7:1	R	**Reserved**
0	R	**Right Channel Sense** (not supported)

Bit	Attr.	Description
31	R	**Presence Detect** 1: Jack plugged in 0: Nothing plugged in.
30:0	R	**Reserved**

Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

		Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format **(Default: 32'h01000010 for PW3, 32'h02200020 for PW4)**

Bit	Attr.	Description
31:30	R/W	**Port Connectivity**, 2'b00
29:24	R/W	**Location** 6'b000001 for PW3 6'b000010 for PW4
23:20	R/W	**Default Device** 4'b0000 for PW3 4'b0010 for PW4
19:16	R/W	**Connection Type**, 4'b0000
15:12	R/W	**Color**, 4'b0000
11:8	R/W	**Misc**, 4'b0000
7:4	R/W	**Default Association** 4'b0001 for PW3 4'b0010 for PW4
3:0	R/W	**Sequence**, 4'b0000

Pin Widget PW6, PW7 (Node ID = 22h, 23h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h00400101**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0100: Pin Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	0: Power Control Supported
9	R	0: Analog widget, not digital
8	R	1: Connection List is present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5	R	**Reserved**
4	R	0: Doesn't contain format information
3	R	0: Contain amplifier parameter
2	R	0: Out Amp Present
1	R	0: In Amp not present
0	R	1: Stereo

Pin Capabilities (Payload = 0Ch) **Response 32'h00000014**

Bit	Attr.	Description
31:17	R	**Reserved**
16	R	**EAPD Capable**. Read as 0.
15:8	R	**VRef Control**. Read as 8'h00
7	R	**Reserved**
6	R	**Balanced I/O Pins**. Read as 0.
5	R	**Input Capable**. Read as 0.
4	R	**Output Capable**. Read as 1.
3	R	**Headphone Drive Capable**. Read as 0
2	R	**Presence Detect Capable**. Read as 1.
1	R	**Trigger Required**. Read as 0.
0	R	**Impedance Sense Capable**. Read as 0.

Connection List Length (Payload = 0Eh) **Response 32'h00000001**

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Short form
6:0	R	7'b0000001: Only 1 input available

Connection List Entry Control Verbs (Verb ID = F02h)

		Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h0000001A / 32'h0000001B

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Independent Node ID
6:0	R	7'b0011010 (from SW2) for PW6 7'b0011011 (from SW3) for PW7

Pin Widget Control Verbs (Verb ID = F07h & 707h)

		Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attr.	Description
7	R	**Headphone Enable** 0: Disabled
6	R/W	**Output Enable** 0: Disabled 1: Output enabled
5	R	**Input Enable** 0: Disabled
4:3	R	0
2:0	R	0: reserved

Pin Sense Control Verbs (Verb ID = F09h & 709h)

		Verb ID	Payload
Get	Get Pin Sense Control	F07h	8'b0
Set	Set Pin Sense Control	707h	PinCntl

PinCntl Format

Bit	Attr.	Description
7:1	R	**Reserved**
0	R	**Right Channel Sense** (not supported)

Response

Bit	Attr.	Description
31	R	**Presence Detect** 1: Jack plugged in 0: Nothing plugged in.
30:0	R	**Reserved**

Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

		Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format **(Default: 32'h00000012 for PW6, 32'h00000014 for PW7)**

Bit	Attr.	Description
31:30	R/W	**Port Connectivity**, 2'b00
29:24	R/W	**Location**, 6'b000000
23:20	R/W	**Default Device**, 4'b0000
19:16	R/W	**Connection Type**, 4'b0000
15:12	R/W	**Color**, 4'b0000
11:8	R/W	**Misc**, 4'b0000
7:4	R/W	**Default Association**, 4'b0001
3:0	R/W	**Sequence** 4'b0010 for PW6 4'b0100 for PW7

Pin Widget PW1, PW2, PW5 (Node ID = 1Dh, 1Eh, 21h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h00400101**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0100: Pin Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	0: Power Control not Supported
9	R	0: Analog widget, not digital
8	R	1: Connection List is present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5	R	**Reserved**
4	R	0: Doesn't contain format information
3	R	0: Contain amplifier parameter
2	R	0: Out Amp not Present
1	R	0: In Amp not present
0	R	1: Stereo

Pin Capabilities (Payload = 0Ch) **Response 32'h00003034**

Bit	Attr.	Description
31:17	R	**Reserved**
16	R	**EAPD Capable**. Read as 0.
15:8	R	**VRef Control**. Read as 8'h03 (50% & Hi-Z)
7	R	**Reserved**
6	R	**Balanced I/O Pins**. Read as 0.
5	R	**Input Capable**. Read as 1.
4	R	**Output Capable**. Read as 1.
3	R	**Headphone Drive Capable**. Read as 0.
2	R	**Presence Detect Capable**. Read as 1.
1	R	**Trigger Required**. Read as 0.
0	R	**Impedance Sense Capable**. Read as 0.

Connection List Length (Payload = 0Eh) **Response 32'h00000001**

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Short form
6:0	R	7'b0000001: Only 1 input available

Connection List Entry Control Verbs (Verb ID = F02h)

		Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h0000001A or 32'h00000019 or 32'h0000001B

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Independent Node ID
6:0	R	7'b0011010 (from SW2, Node ID = 1Ah) for PW1 7'b0011001 (from SW1, Node ID = 19h) for PW2 7'b0011011 (from SW3, Node ID = 1Bh) for PW5

Pin Widget Control Verbs (Verb ID = F07h & 707h)

		Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attr.	Description
7	R	**Headphone Enable** 0: Disabled
6	R/W	**Output Enable** (for Smart 5.1 configuration) 0: Disabled 1: Output enabled
5	R/W	**Input Enable** 0: Disabled 1: Input enabled
4:3	R	0
2:0	R/W	**VRef Enable.** These bits control the VRef signal associated with the pin widget. 3'b000: Hi-Z 3'b001: 50% (half of AVdd) 3'b010: 0V 3'b101: AVdd Others: reserved

Pin Sense Control Verbs (Verb ID = F09h & 709h)

		Verb ID	Payload
Get	Get Pin Sense Control	F07h	8'b0
Set	Set Pin Sense Control	707h	PinCntl

PinCntl Format

Bit	Attr.	Description
7:1	R	**Reserved**
0	R	**Right Channel Sense** (not supported)

Bit	Attr.	Description
31	R	**Presence Detect** 1: Jack plugged in 0: Nothing plugged in.
30:0	R	**Reserved**

Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

		Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format **(Default: 32'h00A00040 for PW1, 32'h00800050 for PW2, 32'h02A000C0 for PW5)**

Bit	Attr.	Description
31:30	R/W	**Port Connectivity**, 2'b00
29:24	R/W	**Location** 6'b000000 for PW1&2 6'b000010 for PW5
23:20	R/W	**Default Device** 4'b1010 for PW1 & PW5 4'b1000 for PW2
19:16	R/W	**Connection Type**, 4'b0000
15:12	R/W	**Color**, 4'b0000
11:8	R/W	**Misc**, 4'b0000
7:4	R/W	**Default Association** 4'b0100 for PW1 4'b0101 for PW2 4'b1100 for PW5
3:0	R/W	**Sequence**, 4'b0000

Pin Widget 8 for CD Analog Input (Node ID = 24h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h00400001**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0100: Pin Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	0: Power Control Not Supported
9	R	0: Analog widget, not digital
8	R	0: Connection List is not present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5	R	**Reserved**
4	R	0: Doesn't contain format information
3	R	0: Doesn't contain amplifier parameter
2	R	0: Out Amp Not Present
1	R	0: In Amp Not Present
0	R	1: Stereo

Pin Capabilities (Payload = 0Ch) **Response 32'h00000020**

Bit	Attr.	Description
31:17	R	**Reserved**
16	R	**EAPD Capable**. Read as 0
15:8	R	**VRef Control**. Read as 8'b0.
7	R	**Reserved**
6	R	**Balanced I/O Pins**. Read as 0.
5	R	**Input Capable**. Read as 1.
4	R	**Output Capable**. Read as 0.
3	R	**Headphone Drive Capable**. Read as 0.
2	R	**Presence Detect Capable**. Read as 0.
1	R	**Trigger Required**. Read as 0.
0	R	**Impedance Sense Capable**. Read as 0.

Pin Widget Control Verbs (Verb ID = F07h & 707h)

		Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attr.	Description
7	R	**Headphone Enable** 0: Disabled
6	R	**Output Enable** 0: Disabled
5	R/W	**Input Enable** 0: Disabled 1: Input enabled
4:3	R	0
2:0	R	**VRef Enable** 3'b000

Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

		Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format **(Default: 32'h10300060)**

Bit	Attr.	Description
31:30	R/W	**Port Connectivity**, 2'b00
29:24	R/W	**Location**, 6'b010000 (internal)
23:20	R/W	**Default Device**, 4'b0011 (CD)
19:16	R/W	**Connection Type**, 4'b0000
15:12	R/W	**Color**, 4'b0000
11:8	R/W	**Misc**, 4'b0000
7:4	R/W	**Default Association**, 4'b0110
3:0	R/W	**Sequence**, 4'b0000

Pin Widget 9 for S/PDIF TX Pin (Node ID = 25h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h00400301**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0100: Pin Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	0: Power Control Not Supported
9	R	1: Digital widget
8	R	1: Connection List is present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5	R	**Reserved**
4	R	0: Doesn't contain format information
3	R	0: Doesn't contain amplifier parameter
2	R	0: Out Amp not Present
1	R	0: In Amp not Present
0	R	1: Stereo

Pin Capabilities (Payload = 0Ch) **Response 32'h00000010**

Bit	Attr.	Description
31:17	R	**Reserved**
16	R	**EAPD Capable**. Read as 0
15:8	R	**VRef Control**. Read as 8'b0
7	R	**Reserved**
6	R	**Balanced I/O Pins**. Read as 0.
5	R	**Input Capable**. Read as 0
4	R	**Output Capable**. Read as 1.
3	R	**Headphone Drive Capable**. Read as 0
2	R	**Presence Detect Capable**. Read as 0
1	R	**Trigger Required**. Read as 0.
0	R	**Impedance Sense Capable**. Read as 0.

Connection List Length (Payload = 0Eh) **Response 32'h00000001**

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Short form
6:0	R	7'b0000001: Only 1 input available

Connection List Entry Control Verbs (Verb ID = F02h)

		Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h00000014

Bit	Attr.	Description
31:8	R	**Reserved**
7	R	0: Independent Node ID
6:0	R	7'b0010100 (from DOW0, Node ID = 14h)

Pin Widget Control Verbs (Verb ID = F07h & 707h)

		Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attr.	Description
7	R	**Headphone Enable** 0: Disabled
6	R/W	**Output Enable** 0: Disabled 1: Output enabled
5	R	**Input Enable** 0: Disabled
4:3	R	0
2:0	R	**VRef Enable** 3'b0

Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

		Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format **(Default: 32'h00400030)**

Bit	Attr.	Description
31:30	R/W	**Port Connectivity**, 2'b00
29:24	R/W	**Location**, 6'b000000
23:20	R/W	**Default Device**, 4'b0100 (SPDIF Out)
19:16	R/W	**Connection Type**, 4'b0000
15:12	R/W	**Color**, 4'b0000
11:8	R/W	**Misc**, 4'b0000
7:4	R/W	**Default Association**, 4'b0011
3:0	R/W	**Sequence**, 4'b0000

Pin Widget 10 (Node ID = 26h)

Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) **Response 32'h00400201**

Bit	Attr.	Description
31:24	R	**Reserved**
23:20	R	4'b0100: Pin Widget
19:16	R	4'b0000: Delay
15:12	R	**Reserved**
11	R	0: No L-R Swap
10	R	0: Power Control Not Supported
9	R	1: Digital widget
8	R	0: Connection List is not present
7	R	0: Does not support unsolicited response
6	R	0: No Processing control
5	R	**Reserved**
4	R	0: Doesn't contain format information
3	R	0: Doesn't contain amplifier parameter
2	R	0: Out Amp not Present
1	R	0: In Amp not Present
0	R	1: Stereo

Pin Capabilities (Payload = 0Ch) **Response 32'h00010030**

Bit	Attr.	Description
31:17	R	**Reserved**
16	R	**EAPD Capable**. Read as 1
15:8	R	**VRef Control**. Read as 8'b0
7	R	**Reserved**
6	R	**Balanced I/O Pins**. Read as 0.
5	R	**Input Capable**. Read as 1.
4	R	**Output Capable**. Read as 1.
3	R	**Headphone Drive Capable**. Read as 0.
2	R	**Presence Detect Capable**. Read as 0
1	R	**Trigger Required**. Read as 0.
0	R	**Impedance Sense Capable**. Read as 0.

Pin Widget Control Verbs (Verb ID = F07h & 707h)

		Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attr.	Description
7	R	**Headphone Enable** 0: Disabled
6	R/W	**Output Enable** 0: Disabled 1: Output enabled
5	R/W	**Input Enable** 0: Disabled 1: Input enabled
4:3	R	0
2:0	R	**VRef Enable** 3'b000

EAPD Enable Verbs (Verb ID = F0Ch & 70Ch)

		Verb ID	Payload
Get	EAPD Control	F07h	8'b0
Set		70Ch	Bit 1 is EAPD

Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

		Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format **(Default: 32'h00C00080)**

Bit	Attr.	Description
31:30	R/W	**Port Connectivity**, 2'b00
29:24	R/W	**Location**, 6'b000000
23:20	R/W	**Default Device**, 4'b1100 (SPDIF In)
19:16	R/W	**Connection Type**, 4'b0000
15:12	R/W	**Color**, 4'b0000
11:8	R/W	**Misc**, 4'b0000
7:4	R/W	**Default Association**, 4'b1000
3:0	R/W	**Sequence**, 4'b0000

ELECTRICAL SPECIFICATIONS

DIGITAL DC AND AC CHARACTERISTICS

DC Performance Characteristic

Parameter	Symbol	Min	Typ	Max	Units
Digital Power Supply	DVdd	3.135	3.3	3.465	V
Input Voltage Range	Vin	-0.3		DVdd + 0.3	V
Low Level Input Voltage	Vil			0.35 x DVdd	V
High Level Input Voltage	Vih	0.65 x DVdd			V
High Level Output Voltage	Voh	0.9 x DVdd			V
Low Level Output Voltage	Vol			0.1 x DVdd	V
Input Leakage Current (AC-Link inputs)		-10		10	uA
Output Leakage Current (Hi-Z'd AC-Link outputs)		-10		10	uA
Input / Output Pin Capacitance				7.5	pF

Analog Performance Characteristics

Analog Input

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage Line Inputs Mic Inputs with 20dB Gain Mic inputs with 0dB Gain		 1.0 0.1 1		Vrms
Input Impedance	10			Kohm
Input Capacitance		7.5		pF

Analog Output

Parameter	Min	Typ	Max	Units
Full Scale Output Voltage Line Output Headphone Output		 1.0	 1.41	Vrms
Analog S/N CD to LINE_OUT Other to LINE_OUT		 100 100		dB
Analog Frequency Response	20		20,000	Hz
Vrefout		2.25-2.75		V

ADC Converters

Parameter	Min	Typ	Max	Units
Digital S/N		96		dB
Total Harmonic Distortion			0.003	%
Frequency Response	20		19.200	Hz
Transition Band	19,200		28,800	Hz
Stop Band	28,800			Hz
Stop Band Rejection	-74			dB
Out-of-Band Rejection		-40		dB
Spurious Tone Reduction		-100		dB
Attenuation, Gain Step Size		1.5		dB

DAC Converters

Parameter	Min	Typ	Max	Units
Digital S/N		100		dB
Total Harmonic Distortion			0.003	%
Frequency Response	20		19.200	Hz
Transition Band	19,200		28,800	Hz
Stop Band	28,800			Hz
Stop Band Rejection	-74			dB
Out-of-Band Rejection		-40		dB
Channel Separation		-90		dB
Spurious Tone Reduction		-100		dB
Attenuation, Gain Step Size		1.5		dB

Note: The frequency response, transition band and stop band specified in the table is based on fs = 48KHz, and scale with fs.

FUNCTION DESCRIPTION

Clock Control

– One of the major differences between High Definition Audio and AC97 is the clock source. The High Definition Audio controller provides a 24MHz clock (BITCLK). An internal PLL (PLL1) in the codec uses BITCLK (24MHz) as the reference clock and generates 49.152MHz clocks for internal use. A second PLL (PLL2) also takes the 24MHz BITCLK and generates 22.5792MHz clock for 44.1KHz based rates. The PLLs can be powered down by the Power Widget for power management. **Both PLL output clocks can be routed to pin 48 by a vendor defined verb for testing.**

– The interface signals between digital block and the 2 PLLs are listed below.

PLL1 (49.152 MHz)		
Pin Name	**Direction (from PLL)**	**Pin Description**
REFCLK	I	Connects to a 24-MHz clock input.
CLK49152	O	49.152-MHz clock output.
RST	I	When RST is **high**, the PLL enters a low power mode and all internal states are reset.
PWRPD	I	When PWRPD is **high**, the PLL enters a power-down mode.
VDD	I/O	Digital power supply for PFD and Dividers. Nominally 3.3V.
GND	I/O	Ground for PFD and Dividers.
VCOPWR	I/O	Analog power supply for VCO. Nominally 3.3V.
VCOGND	I/O	Ground for VCO.
CHGPPWR	I/O	Analog power supply for Bias and Charge Pump. Nominally 3.3V.
CHGPGND	I/O	Ground for Bias and Charge Pump.
PLL2 (22.5792 MHz)		
Pin Name	**Direction (from PLL)**	**Pin Description**
REFCLK	I	Connects to a 24-MHz clock input.
CLK225792	O	22.5792-MHz clock output.
RST	I	When RST is **high**, the PLL enters a low power mode and all internal states are reset.
PWRPD	I	When PWRPD is **high**, the PLL enters a power-down mode.
VDD	I/O	Digital power supply for PFD and Dividers. Nominally 3.3V.
GND	I/O	Ground for PFD and Dividers.
VCOPWR	I/O	Analog power supply for VCO. Nominally 3.3V.
VCOGND	I/O	Ground for VCO.
CHGPPWR	I/O	Analog power supply for Bias and Charge Pump. Nominally 3.3V.
CHGPGND	I/O	Ground for Bias and Charge Pump.

HPF for ADC DC Removal

– The built-in high-pass filter for each ADC can remove the DC component in the ADC data.

Audio Jack Detection Circuits

– Based on the jack detection circuit defined in the High Definition Audio specification, the figure below summarizes the various resistances seen by the SENSE pin in different scenarios.

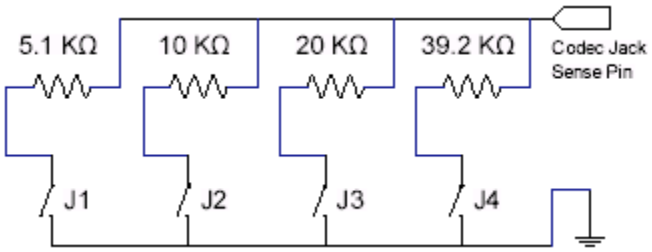
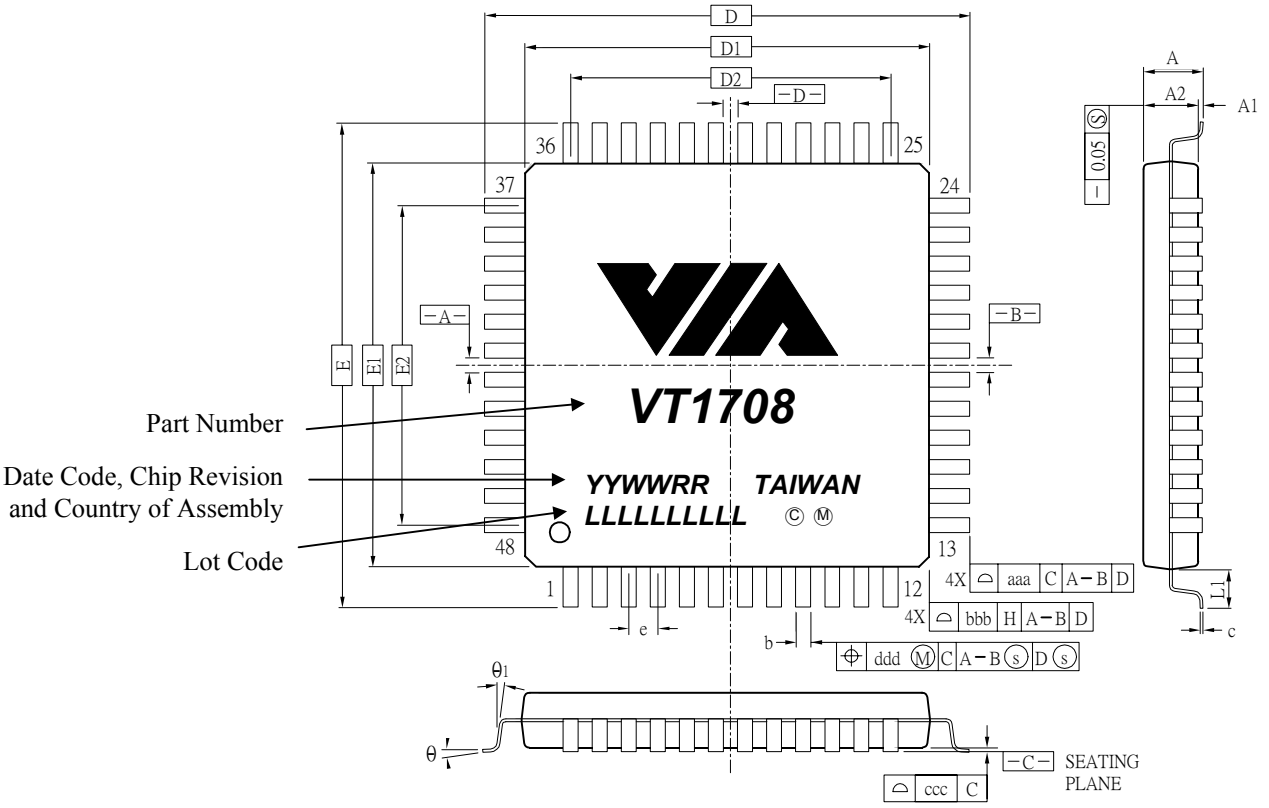


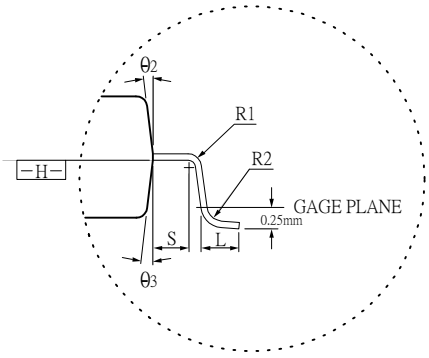
Figure 19. Jack Detect Circuit

Internal Loopback and Peak Detection for Low Cost Production Test

– Internal loopback paths can be used to test all DACs and ADCs functions. The output of each DAC can be routed back to the input of the ADC. The ADC output data is analyzed by a specially designed block to detect the zero-crossing point and the peak values. These information can be read back to decide whether the digital and analog functions are normal. Refer to the descriptions in the Vendor-Defined Verbs in the Audio Function Group.

PACKAGE MECHANICAL SPECIFICATIONS





NOTES :

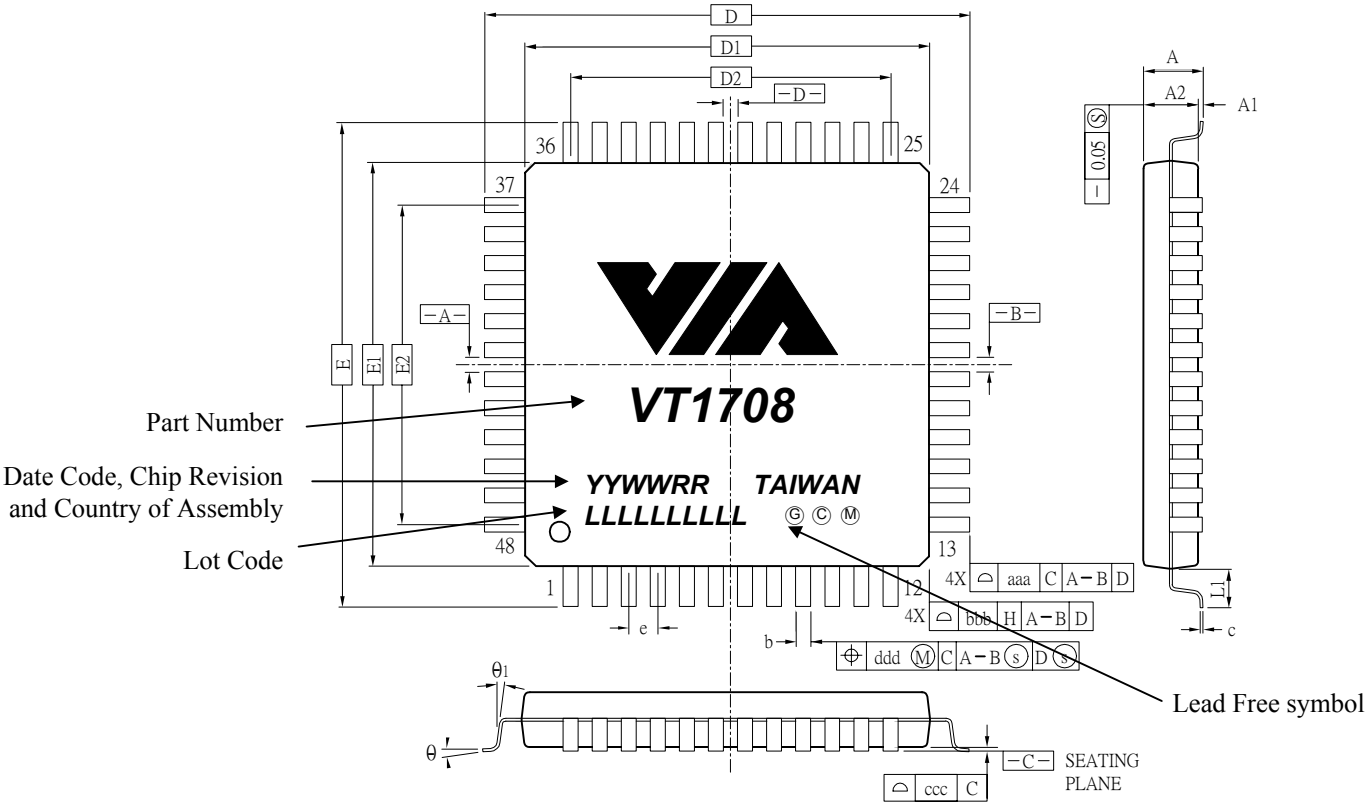
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 20. Mechanical Specification – 48-Pin LQFP



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 21. Mechanical Specification for Lead Free – 48-Pin LQFP