NEC

NEC Electronics Inc.

CMOS-6/6A/6V/6X 1.0-MICRON CMOS GATE ARRAYS

April 1992

Description

NEC's CMOS-6 gate array families (CMOS-6, CMOS-6A, CMOS-6V and CMOS-6X) are ultra-high performance, sub-micron effective channel length CMOS products created for high-integration ASIC applications.

The device processing includes 1.0-micron (drawn) silicon-gate CMOS technology and three-layer (CMOS-6) and two-layer (CMOS-6A, CMOS-6V, CMOS-6V) metallization. This technology features channelless (sea-of-gates) architecture in densities from 1,200 to 177,408 equivalent gates, with an internal gate delay of 270 ps (F/O=1; L = 0). Output drive is variable to 18 mA. Slew rate buffers are also available.

CMOS-6 products are fully supported by NEC's advanced ASIC design technology. NEC's OpenCAD® integration system lets the designer choose the most powerful design tools and services available. The CMOS-6/6A/6V macro cell (block) library is compatible with the powerful CMOS-5 block library, which contain over 300 cells and more than 100 interface options.

NEC offers advanced packaging solutions with both through-hole and surface-mount ceramic PGAs and flat packages. These heat-sink-equipped packages give CMOS-6 devices the performance edge in high-integration applications.

Features

- Channelless, 1.µm CMOS high-density architecture
- Variable output drive: 4.5, 9.0, 13.5, or 18.0 mA
- Slew rate output buffers
- Free size memory blocks to 64 Kbytes (16K x 4, µPD65676)
- Powerful block library with more than 400 macros
- 3V characterized block library
- New 0.65 mm 184-pin plastic QFP for cost effective designs
- High I/O to gate ratio for CMOS-6V and CMOS-6X

Publications

This data sheet contains preliminary specifications, package information, and operational data for the CMOS-6 gate array families. Additional design information is available in NEC's CMOS-6 Block Library and CMOS-6 Design Manual. Contact your local NEC Design Center or the NEC Literature Center for further ASIC design information; see the back of this data sheet for locations and phone numbers.

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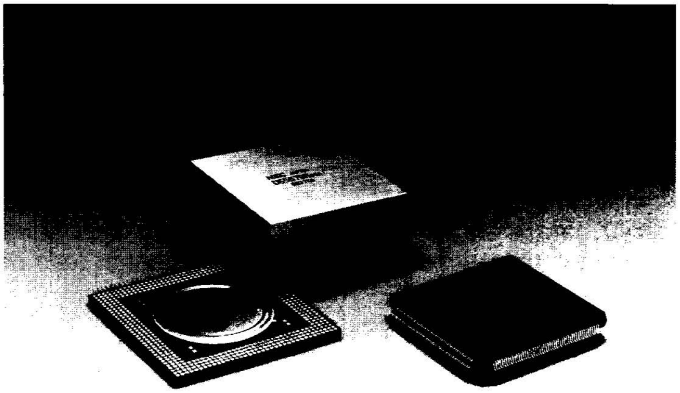
Figure 1. Sample CMOS-6/6A/6V/6X Packages



Gate Array Sizes

Device (µPD)	Available Gates	Estimated Usable Gates: Target Design = 50% Memory	Estimated Usable Gates: Target Design = All Random*	I/O Pads (Max.)
CMOS-6X Devices				
65612	1,200	1,000	800	64
65622	2,700	2,300	1,900	84
65626	3,900	3,300	2,700	104
65632	5,600	3,900	3,900	104
CMOS-6A Devices				
65630	5,376	4,600	3,800	84
65636	8,000	6,800	5,600	100
65640	11,520	9,800	8,100	120
65646	16,240	13,800	11,400	140
65650	21,120	18,000	14,800	160
65654	30,720	26,100	21,500	192
CMOS-6V Devices				
65631	5,544	4,700	3,900	140
65641	11,520	9,800	8,100	160
65644	14,040	11,900	9,800	160
65647	16,240	13,800	11,400	160
65648	18,600	15,800	13,000	160
65651	21,120	18,000	14,800	220
65652	26,640	22,600	18,600	220
65655	30,720	26,100	21,500	220
CMOS-6 Devices				
65658	42,240	37,000	21,700	220
65664	72,576	63,500	54,400	288
65672	119,232	104,300	89,400	368
65676	177,408	155,200	133,100	448

Actual gate utilitization may vary depending on circuit implementation.

Utilization is 75% for three-layer metal; 70% for two-layer metal.

Memory utilization is determined by 50% x available gates + (utilization x 50% available gates)

Depending on package and circuit specification, some pads are used for V_{DD} and GND and are unavailable as signal pads.

Circuit Architecture

CMOS-6 products are built with NEC's 1-micron channelless architecture. As shown in figure 2, CMOS gate array chips are divided into I/O and internal cell areas. The I/O cell area contains input and output buffers that isolate the internal cells from high-energy external signals. The internal cell area is an array of basic cells, each composed of two p-channel MOS transistors and two n-channel MOS transistors, as well as four additional n-channel MOS transistors for compact RAM design. A cell configured as a two-input NAND gate is shown in figure 3. These p-channel and n-channel transistors are sized to offer a superb ratio of speed to silicon area.

Figure 2. Chip Layout and Internal Cell Configuration

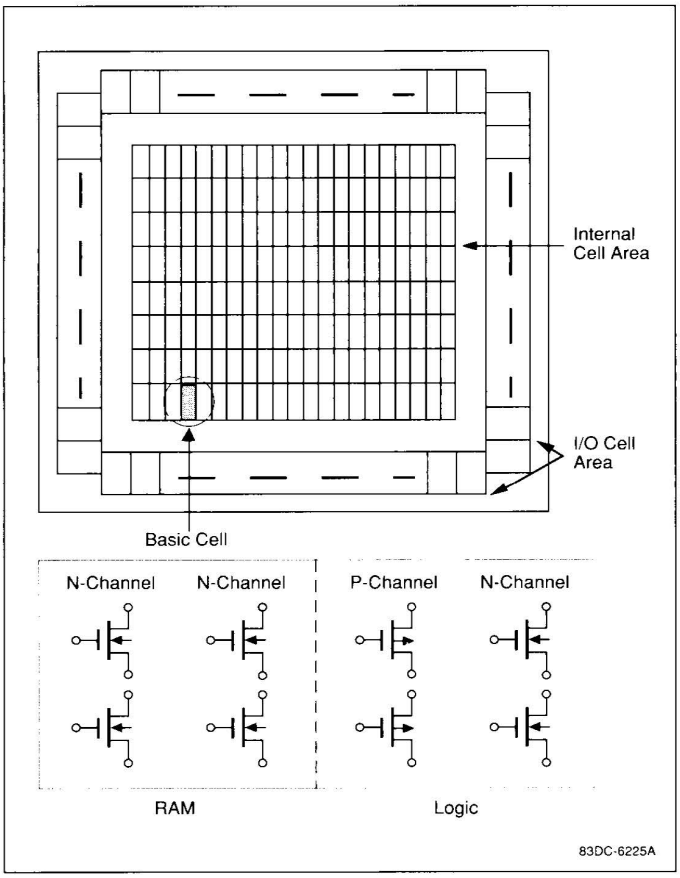
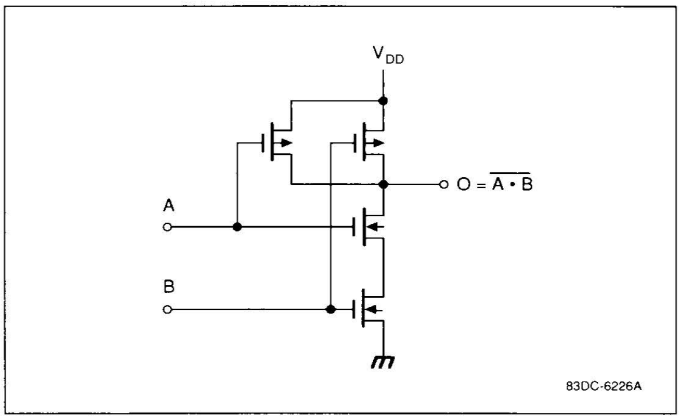


Figure 3. Cell Configured as a Two-Input NAND



Output Slew Rate Selection

Fast rise and fall times of CMOS output buffers can cause system noise and signal overshoot. When an unterminated line is being driven by a buffer, the maximum line length is determined by the rise and fall time of the output buffers and the round-trip signal delay of the line.

As a general rule, the round-trip delay of the line should not exceed the rise or fall time of the driving signal. Transmission lines that are longer than those determined by the above rule can cause system performance degradation because of reflections and ringing. One benefit of slew rate output buffers is that longer interconnections on a PC board (and routing flexibility) are possible with slew rate output buffers.

The ASIC designer can slow down the output edge rate by selecting the slew rate output buffer and thus allowing for a longer line.

Also, as the slew rate buffers inject less noise than their non-slew rate counterparts into the internal power and ground busses of the devices, the slew rate buffers require fewer power pairs for simultaneous switching outputs.

Absolute Maximum Ratings

Power supply voltage, V_{DD}	–0.5 to +6.5 V
Input/output voltage, V_I / V_O	–0.5 V to V_{DD} + 0.5 V
Latch-up current, I_{LATCH}	>1 A (typ)
Output current, I_O	
4.5-mA drive	10 mA
9-mA drive	20 mA
13.5-mA drive	30 mA
18-mA drive	40 mA
Operating temperature, T_{OPT}	–40 to +85°C
Storage temperature, T_{STG}	–65 to +150°C

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Input/Output Capacitance

$V_{DD} = V_I = 0$ V; f = 1 MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	25	pF
Output	C_{OUT}	10	25	pF
I/O	$C_{I/O}$	10	25	pF

Note:

(1) Values include package pin capacitance.

Power Consumption

Description	Limits (max)	Unit	Test Conditions
Internal cell	8	μW/MHz	F/O = 3; L = 3 mm
Input block	46	μW/MHz	F/O = 3; L = 3 mm
Output block	.98	mW/MHz	C_L = 15 pF

Recommended Operating Conditions

		CMOS Level		TTL Level		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Power supply voltage	V_{DD}	4.5	5.5	4.75	5.25	V
Ambient temperature	T_A	–40	+85	0	+70	°C
Low-level input voltage	V_{IL}	0	0.3 V_{DD}	0	0.8	V
High-level input voltage	V_{IH}	0.7 V_{DD}	V_{DD}	2.2	V_{DD}	V
Input rise or fall time	t_R, t_F	0	200	0	200	ns
Input rise or fall time, Schmitt	t_R, t_F	0	10	0	10	ms
Positive Schmitt-trigger voltage	V_P	1.8	4.0	1.2	2.4	V
Negative Schmitt-trigger voltage	V_N	0.6	3.1	0.6	1.8	V
Hysteresis voltage	V_H	0.3	1.5	0.3	1.5	V

AC Characteristics

V_{DD} = 5 V ± 10%; T_A = –40 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}	120			MHz	D-F/F; F/O = 2
Delay time, internal gate	t_{PD}		270		ps	F/O = 1; L = 0 mm
Delay time, 2-input NAND gate			700		ps	F/O = 3; L = 3 mm
Delay time, buffer						
Input (FI01)	t_{PD}		1.25		ns	F/O = 3; L = 3 mm
Output (FO01)	t_{PD}		2.0		ns	C_L = 15 pF
Output rise time	t_R		3.0		ns	C_L = 15 pF
Output fall time	t_F		2.0		ns	C_L = 15 pF

DC Characteristics

V_{DD} = 5 V ± 10%; T_A = −40 to +85 °C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current (Note 1)	I_L		0.1	400	μA	$V_I = V_{DD}$ or GND
Input leakage current						
Regular	I_I		10^{-5}	10	μA	$V_I = V_{DD}$ or GND
50 kΩ pull-up	I_I	−40	−100	−270	μA	V_I = GND
5 kΩ pull-up	I_I	−0.35	−1.0	−2.2	mA	V_I = GND
50 kΩ pull-down	I_I	45	120	300	μA	$V_I = V_{DD}$
Off-state output leakage current	I_{OZ}			10	μA	$V_O = V_{DD}$ or GND
Input clamp voltage	V_{IC}	−1.2			V	I_I = 18 mA
Output short circuit current (Note 2)	I_{OS}	−250			mA	V_O = 0 V
Low-level output current (CMOS)						
4.5 mA (Note 3)	I_{OL}	4.5			mA	V_{OL} = 0.4 V
9 mA (Note 3)	I_{OL}	9.0			mA	V_{OL} = 0.4 V
13.5 mA (Note 3)	I_{OL}	13.5			mA	V_{OL} = 0.4 V
18 mA (Note 3)	I_{OL}	18.0			mA	V_{OL} = 0.4 V
High-level output current (CMOS)						
4.5 mA (Note 3)	I_{OH}	−2.5			mA	$V_{OH} = V_{DD}$ −0.4 V
9 mA (Note 3)	I_{OH}	−5.0			mA	$V_{OH} = V_{DD}$ −0.4 V
13.5 mA (Note 3)	I_{OH}	−7.5			mA	$V_{OH} = V_{DD}$ −0.4 V
18 mA (Note 3)	I_{OH}	−10.0			mA	$V_{OH} = V_{DD}$ −0.4 V
Low-level output current (TTL)						
9 mA (Note 4)	I_{OL}	9.0			mA	V_{OL} = 0.4 V
18 mA (Note 4)	I_{OL}	18.0			mA	V_{OL} = 0.4 V
High-level output current (TTL)						
9 mA (Note 4)	I_{OH}	−0.5			mA	V_{OH} = 2.4 V
18 mA (Note 4)	I_{OH}	−1.0			mA	V_{OH} = 2.4 V
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 0 mA
High-level output voltage (CMOS) (Note 3)	V_{OH}	V_{DD}−0.1			V	I_{OH} = 0 mA
High-level output voltage (TTL) (Note 4)	V_{OH}	2.6	3.4		V	I_{OH} = 0 mA

Notes:

(1) The maximum value reflects the use of pull-up/pull-down resistors and oscillator blocks. Contact an NEC ASIC Design Center for assistance in calculation.

(2) Rating is for only one output operating in this mode for less than 1 second.

(3) CMOS-level output buffer (V_{DD} = 5 V ± 10%, T_A = −40 to +85°C).

(4) TTL-level output buffer (V_{DD} = 5 V ± 5%, T_A = 0 to +70°C).

Package Plan

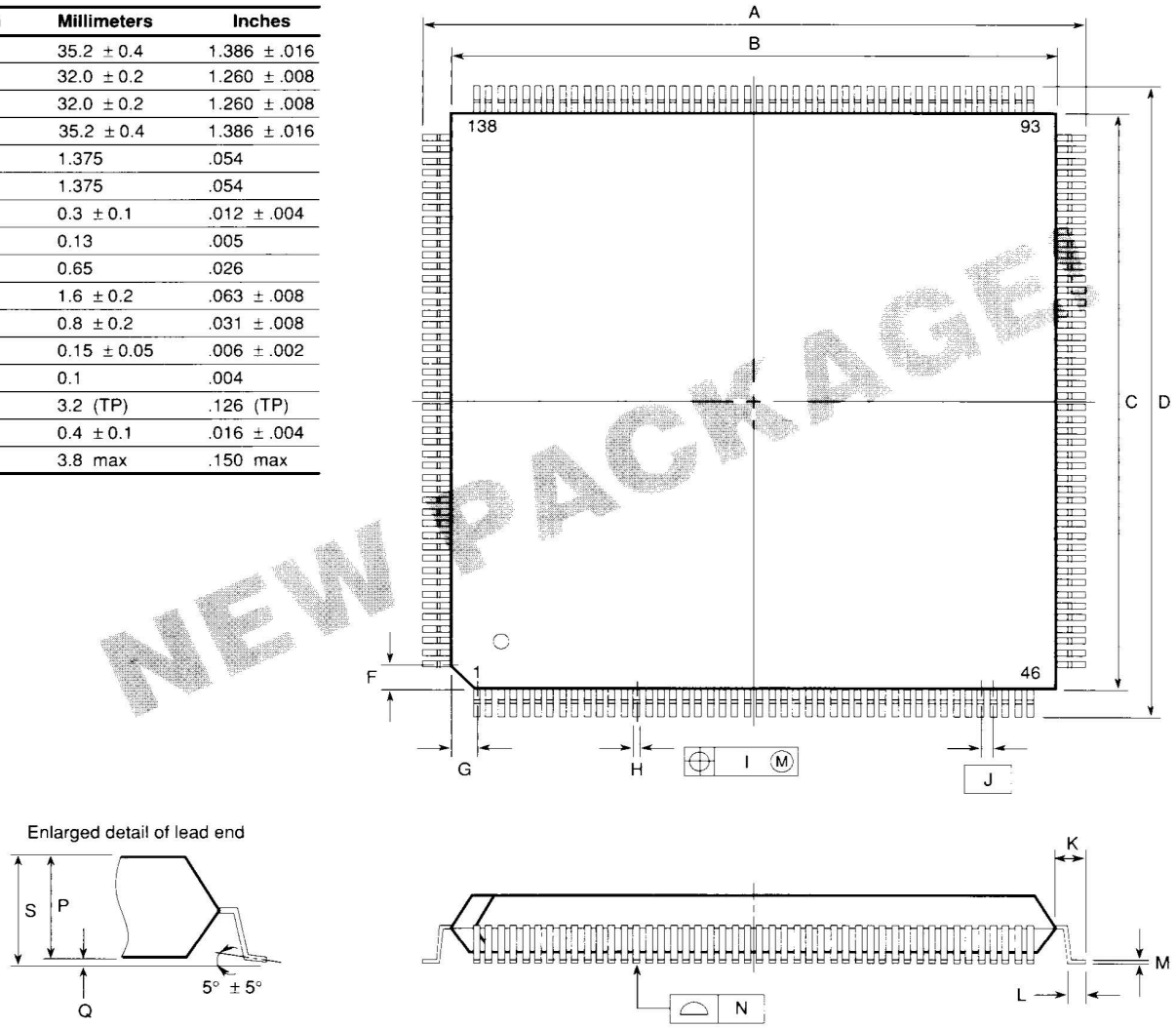
	CMOS-6X μPD65xxx				CMOS-6A μPD65xxx						CMOS-6V μPD65xxx								CMOS-6 μPD65xxx			
	612	622	626	632	630	636	640	646	650	654	631	641	644	647	648	651	652	655	658	664	672	676
K gates (usable w/o memory)	0.8	1.9	2.7	3.9	3.8	5.6	8.1	11.4	14.8	21.5	3.9	8.1	9.8	11.4	13.0	14.8	18.6	21.5	21.7	54.4	89.4	133
Maximum I/O Pins	64	84	104	104	84	100	120	140	160	192	140	160	160	160	160	220	220	220	220	288	368	448
Plastic Quad Flatpack (QFP)																						
44-pin	A	A	A		A	A	A	A	A													
52-pin	A	A	A		A	A	A	A	A	A												
64-pin		A	A		A	A	A	A	A	A												
80-pin			A		A	A	A	A	A[1]	A												
100-pin						A	A	A	A	A	A								A			
120-pin							A	A	A	A	A								A	A	A	
136-pin								A	A	A	A	A	A						A	A	A	
160-pin									A	A	E	A	A	A	A				A	A	A	A
184-pin										A						A	A		A	A	A	A
Thin Quad Flatpack (TQFP)																						
80-pin			A																			
Shrink Plastic Quad Flatpack (QFP-FP) (.5 mm Lead Pitch)																						
100-pin						A	A	A	A	A	A								A			
120-pin							A	A	A	A	A								A	A	A	
136-pin								A	A	A	A											
144-pin											E	A	A						A	A	A	
160-pin*									A	A		A	A	A	A				A	A	A	A
176-pin									A	A		A	A	A	A	A	A		A	A	A	A
208-pin*																A	A	A	A	A	A	A
304-pin																				E	E	E
Ceramic Pin Grid Array (PGA)																						
72-pin							A	A	A	A												
132-pin								A	A	A	A	A							A	A	A	A
176-pin										A						A	A		A	A	A	A
208-pin																			A	A	A	A
280-pin																				A	A	A
364-pin																					A	A
Ceramic Pin Grid Array (PGA) (Butt Lead)																						
288-pin																					A[1]	A[1]
528-pin (with heat sink)																						A
528-pin (without heat sink)																						A
Plastic Leaded Chip Carrier (PLCC)																						
68-pin																			A			
84-pin																			A			

A = Available
A[1] = Need advanced notice
E = Under Evaluation
* = Heat spreader under evaluation

NOTE: NEC reserves the right to alter the package plan based on the results of qualification. For current package availability, please contact your local NEC Design Center.

184-Pin (0.65 mm) Plastic QFP

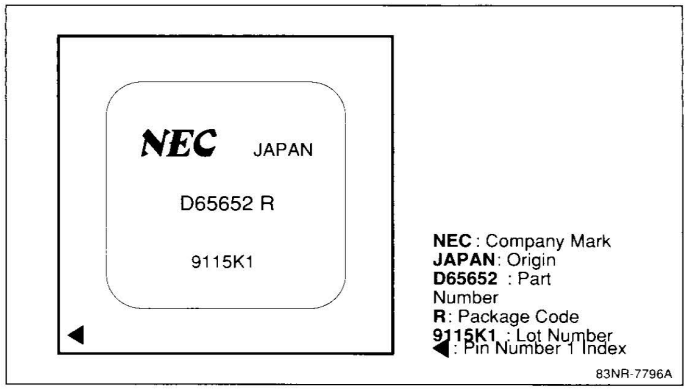
Item	Millimeters	Inches
A	35.2 ±0.4	1.386 ±.016
B	32.0 ±0.2	1.260 ±.008
C	32.0 ±0.2	1.260 ±.008
D	35.2 ±0.4	1.386 ±.016
F	1.375	.054
G	1.375	.054
H	0.3 ±0.1	.012 ±.004
I	0.13	.005
J	0.65	.026
K	1.6 ±0.2	.063 ±.008
L	0.8 ±0.2	.031 ±.008
M	0.15 ±0.05	.006 ±.002
N	0.1	.004
P	3.2 (TP)	.126 (TP)
Q	0.4 ±0.1	.016 ±.004
S	3.8 max	.150 max



NEW PACKAGE

The new 184-pin 0.65 mm QFP shown above is ideal for PC integrated chipsets. The package is available with a copper leadframe thereby allowing greater heat dissipation than standard 42 alloy leadframe packages. The 0.65 mm pin pitch allows the use of widely available, cost effective assembly equipment. It is currently available in two masterslices. The μPD65658 with 25,344 usable gates and the μPD65664 with 43,545 usable gates.

Typical Package Marking



NEC's ASIC Design System

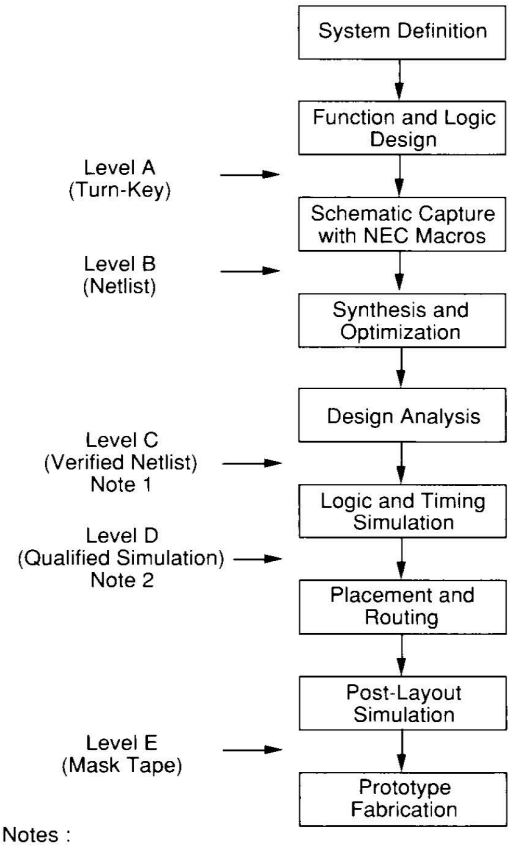
CMOS-6/6A/6V gate arrays are fully supported by NEC's network of ASIC Design Centers, listed on the back of this data sheet.

Design flow for CMOS-6/6A/6V gate arrays is shown in figure 4. Users can enlist Design Center support at any step in the design flow before actual manufacturing. Figure 4 shows the various levels at which Design Center support may begin — anywhere from level A through level E. Level C, "Verified Netlist," is the most popular interface.

NEC supports its ASIC products with a comprehensive CAD system that significantly reduces the time and expense usually associated with the development of semi-custom devices. NEC's OpenCAD integration system supports tools for floorplanning, logic synthesis, automatic test generation, accelerated fault grading and full timing simulation, and advanced place-and-route algorithms. These advanced CAD tools ensure accurate designs.

Sample design kits are available at no charge to qualified users: contact an NEC ASIC Design Center for more information. (Software licensing required—NEC reserves the right to prioritize support based on user requirements.)

Figure 4. Gate Array Design Flow



Notes :

(1) NEC supports the most popular workstations, including Mentor Graphics, Valid, DAZIX®, FutureNet, Viewlogic®, and HP9000 workstations, for the NEC ASIC product line. However, NEC does not support all workstations for all products. Please contact your nearest NEC ASIC Design Center for more information.

(2) NEC provides support of System HILO®, Verilog®, and MACH 1000/1500™ interface capability.

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Block Library List

The CMOS-6 families offer a variety of blocks, including gates, flip-flop circuits, and shift registers. The functions of these blocks are designed to be compatible with those of the CMOS-4 and CMOS-5 families.

In addition, such memory blocks as RAM and ROM and low-power gates are provided. The low-power block, in particular, was designed with low fan-out taken into consideration; the number of cells is less than that of the standard block, contributing to low power consumption and high efficiency.

Block List

Block Name	Description	I_{OL} (mA)	Cells
	Interface Blocks		
Inputs			
FI01	Input buffer, CMOS in	-	1 (3)
FID1	Input buffer, CMOS in, 50 kΩ pull-down res.	-	1 (3)
FIU1	Input buffer, CMOS in, 50 kΩ pull-up res.	-	1 (3)
FIW1	Input buffer, CMOS in, 5 kΩ pull-up res.	-	1 (3)
FI02	Input buffer, TTL in	-	1 (3)
FID2	Input buffer, TTL in, 50 kΩ pull-down res.	-	1 (3)
FIU2	Input buffer, TTL in, 50 kΩ pull-up res.	-	1 (3)
FIW2	Input buffer, TTL in, 5 kΩ pull-up res.	-	1 (3)
FIB1	Input buffer, CMOS in, high fanout for clock driver	-	1 (24)
FIB2	Input buffer, TTL in, high fanout for clock driver	-	1 (24)
FDS1	Input buffer, CMOS Schmitt in, 50 kΩ pull-down res.	-	1 (6)
FIS1	Input buffer, CMOS Schmitt in	-	1 (6)
FUS1	Input buffer, CMOS Schmitt in, 50 kΩ pull-up res.	-	1 (6)
FWS1	Input buffer, CMOS Schmitt in, 5 kΩ pull-up res.	-	1 (6)
FDS2	Input buffer, TTL Schmitt in, 50 kΩ pull-down res.	-	1 (6)
FIS2	Input buffer, TTL Schmitt in	-	1 (6)
FUS2	Input buffer, TTL Schmitt in, 50 kΩ pull-up res.	-	1 (6)
FWS2	Input buffer, TTL Schmitt in, 5 kΩ pull-up res.	-	1 (6)
Outputs			
FO01	Output buffer, CMOS out	9.0	1 (2)
FO02	Output buffer, CMOS out	13.5	1 (4)
FO03	Output buffer, CMOS out	18.0	1 (4)
FO04	Output buffer, CMOS out	4.5	1 (2)
FT01	Output buffer, TTL out	9.0	1 (4)
FT02	Output buffer, TTL out	18.0	2 (6)
B007	Output buffer, CMOS 3-state out	13.5	1 (6)
B0D7	Output buffer, CMOS 3-state out, 50 kΩ pull-down res.	13.5	1 (6)
B0U7	Output buffer, CMOS 3-state out, 50 kΩ pull-up res.	13.5	1 (6)
B0W7	Output buffer, CMOS 3-state out, 5 kΩ pull-up res.	13.5	1 (6)
B008	Output buffer, CMOS 3-state out	9.0	1 (5)
B0D8	Output buffer, CMOS 3-state out, 50 kΩ pull-down res.	9.0	1 (5)
B0U8	Output buffer, CMOS 3-state out, 50 kΩ pull-up res.	9.0	1 (5)
B0W8	Output buffer, CMOS 3-state out, 5 kΩ pull-up res.	9.0	1 (5)
B009	Output buffer, CMOS 3-state out	18.0	1 (6)
B0D9	Output buffer, CMOS 3-state out, 50 kΩ pull-down res.	18.0	1 (6)

Note: Number of internal cells required is shown in parentheses.

Block Name	Description	I_{OL} (mA)	Cells
Outputs (Cont.)			
B0U9	Output buffer, CMOS 3-state out, 50 kΩ pull-up res.	18.0	1 (6)
B0W9	Output buffer, CMOS 3-state out, 5 kΩ pull-up res.	18.0	1 (6)
B00E	Output buffer, CMOS 3-state out	4.5	1 (5)
B0DE	Output buffer, CMOS 3-state out, 50 kΩ pull-down res.	4.5	1 (5)
B0UE	Output buffer, CMOS 3-state out, 50 kΩ pull-up res.	4.5	1 (5)
B0WE	Output buffer, CMOS 3-state out, 5 kΩ pull-up res.	4.5	1 (5)
BT08	Output buffer, TTL 3-state out	9.0	1 (6)
BTU8	Output buffer, TTL 3-state out, 50 kΩ pull-up res.	9.0	1 (6)
BTW8	Output buffer, TTL 3-state out, 50 kΩ pull-up res.	9.0	1 (6)
BT09	Output buffer, TTL 3-state out	18.0	2 (12)
BTU9	Output buffer, TTL 3-state out, 50 kΩ pull-up res.	18.0	2 (12)
BTW9	Output buffer, TTL 3-state out, 50 kΩ pull-up res.	18.0	2 (12)
EXT1	Output buffer, N-ch open drain	9.0	1 (2)
EXT3	Output buffer, N-ch open drain, 50 kΩ pull-up res.	9.0	1 (2)
EXW3	Output buffer, N-ch open drain, 5 kΩ pull-up res.	9.0	1 (2)
EXT2	Output buffer, P-ch open drain	*9.0	1 (2)
EXT4	Output buffer, P-ch open drain, 50 kΩ pull-up res.	*9.0	1 (2)
EXT5	Output buffer, N-ch open drain	18.0	1 (2)
EXT7	Output buffer, N-ch open drain, 50 kΩ pull-up res.	18.0	1 (2)
EXW7	Output buffer, N-ch open drain, 5 kΩ pull-up res.	18.0	1 (2)
EXT6	Output buffer, P-ch open drain, 50 kΩ pull-up res.	*18.0	1 (2)
EXT8	Output buffer, P-ch open drain, 50 kΩ pull-down res.	*18.0	1 (2)
EXT9	Output buffer, N-ch open drain	13.5	1 (2)
EXTB	Output buffer, N-ch open drain, 50 kΩ pull-up res.	13.5	1 (2)
EXWB	Output buffer, N-ch open drain, 5 kΩ pull-up res.	13.5	1 (2)

* Indicates I_{OH}

Block Name	Description	I_{OL} (mA)	Cells
I/O Buffers			
B001	I/O buffer, CMOS in, CMOS 3-state out	13.5	1 (9)
B0D1	I/O buffer, CMOS in, CMOS 3-state out, 50 kΩ pull-down res.	13.5	1 (9)
B0U1	I/O buffer, CMOS in, CMOS 3-state out, 50 kΩ pull-up res.	13.5	1 (9)
B0W1	I/O buffer, CMOS in, CMOS 3-state out, 5 kΩ pull-up res.	13.5	1 (9)
B002	I/O buffer, TTL in, CMOS 3-state out	13.5	1 (9)
B0D2	I/O buffer, TTL in, CMOS 3-state out, 50 kΩ pull-down res.	13.5	1 (9)
B0U2	I/O buffer, TTL in, CMOS 3-state out, 50 kΩ pull-up res.	13.5	1 (9)
B0W2	I/O buffer, TTL in, CMOS 3-state out, 5 kΩ pull-up res.	13.5	1 (9)
B003	I/O buffer, CMOS in, CMOS 3-state out	9.0	1 (8)
B0D3	I/O buffer, CMOS in, CMOS 3-state out, 50 kΩ pull-down res.	9.0	1 (8)
B0U3	I/O buffer, CMOS in, CMOS 3-state out, 50 kΩ pull-up res.	9.0	1 (8)
B0W3	I/O buffer, CMOS in, CMOS 3-state out, 5 kΩ pull-up res.	9.0	1 (8)
B004	I/O buffer, TTL in, CMOS 3-state out	9.0	1 (8)
B0D4	I/O buffer, TTL in, CMOS 3-state out, 50 kΩ pull-down res.	9.0	1 (8)
B0U4	I/O buffer, TTL in, CMOS 3-state out, 50 kΩ pull-up res.	9.0	1 (8)
B0W4	I/O buffer, TTL in, CMOS out, 5 kΩ pull-up res.	9.0	1 (8)

Interface Blocks (Cont.)

I/O Buffers (Cont.)

Block Name	Description	I_{OL} (mA)	Cells
B005	I/O buffer, CMOS in, CMOS 3-state out	18.0	1 (9)
B0D5	I/O buffer, CMOS in, CMOS 3-state out, 50 kΩ pull-down res.	18.0	1 (9)
B0U5	I/O buffer, CMOS in, CMOS 3-state out, 50 kΩ pull-up res.	18.0	1 (9)
B0W5	I/O buffer, CMOS in, CMOS 3-state out, 5 kΩ pull-up res.	18.0	1 (9)
B006	I/O buffer, TTL in, CMOS 3-state out	18.0	1 (9)
B0D6	I/O buffer, TTL in, CMOS 3-state out, 50 kΩ pull-down res.	18.0	1 (9)
B0U6	I/O buffer, TTL in, CMOS 3-state out, 50 kΩ pull-up res.	18.0	1 (9)
B0W6	I/O buffer, TTL in, CMOS 3-state out, 5 kΩ pull-up res.	18.0	1 (9)
B00A	I/O buffer, TTL in, TTL 3-state out	9.0	1 (9)
B0UA	I/O buffer, TTL in, TTL 3-state out, 50 kΩ pull-up res.	9.0	1 (9)
B0WA	I/O buffer, TTL in, TTL 3-state out, 5 kΩ pull-up res.	9.0	1 (9)
B00B	I/O buffer, TTL in, TTL 3-state out	18.0	2 (15)
B0UB	I/O buffer, TTL in, TTL 3-state out, 50 kΩ pull-up res.	18.0	2 (15)
B0WB	I/O buffer, TTL in, TTL 3-state out, 5 kΩ pull-up res.	18.0	2 (15)
B00C	I/O buffer, CMOS in, CMOS 3-state out	4.5	1(8)
B0DC	I/O buffer, CMOS in, CMOS 3-state out, 50 kΩ pull-down res.	4.5	1(8)
B0UC	I/O buffer, CMOS in, CMOS 3-state out, 50 kΩ pull-up res.	4.5	1 (8)
B0WC	I/O buffer, CMOS in, CMOS 3-state out, 5 kΩ pull-up res.	4.5	1 (8)
B00D	I/O buffer, TTL in, CMOS 3-state out	4.5	1 (8)
B0DD	I/O buffer, TTL in, CMOS 3-state out, 50 kΩ pull-down res.	4.5	1 (8)
B0UD	I/O buffer, TTL in, CMOS 3-state out, 50 kΩ pull-up res.	4.5	1 (8)
B0WD	I/O buffer, TTL in, CMOS 3-state out, 5 kΩ pull-up res.	4.5	1 (8)
BSD1	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 50 kΩ pull-down res.	13.5	1 (12)
BSI1	I/O buffer, CMOS Schmitt in, CMOS 3-state out	13.5	1 (12)
BSU1	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 50 kΩ pull-up res.	13.5	1 (12)
BSW1	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 5 kΩ pull-up res.	13.5	1 (12)
BSD2	I/O buffer, TTL Schmitt in, CMOS 3-state out, 50 kΩ pull-down res.	13.5	1 (12)
BSI2	I/O buffer, TTL Schmitt in, CMOS 3-state out	13.5	1 (12)
BSU2	I/O buffer, TTL Schmitt in, CMOS 3-state out, 50 kΩ pull-up res.	13.5	1 (12)
BSW2	I/O buffer, TTL Schmitt in, CMOS 3-state out, 5 kΩ pull-up res.	13.5	1 (12)
BSD3	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 50 kΩ pull-down res.	9.0	1 (11)
BSI3	I/O buffer, CMOS Schmitt in, CMOS 3-state out	9.0	1 (11)
BSU3	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 50 kΩ pull-up res.	9.0	1 (11)
BSW3	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 5 kΩ pull-up res.	9.0	1 (11)

Note: Number of internal cells required is shown in parentheses.

Interface Blocks (Cont.)

I/O Buffers (Cont.)

Block Name	Description	I_{OL} (mA)	Cells
BSD4	I/O buffer, TTL Schmitt in, CMOS 3-state out, 50 kΩ pull-down res.	9.0	1 (11)
BSI4	I/O buffer, TTL Schmitt in, CMOS 3-state out	9.0	1 (11)
BSU4	I/O buffer, TTL Schmitt in, CMOS 3-state out, 50 kΩ pull-up res.	9.0	1 (11)
BSW4	I/O buffer, TTL Schmitt in, CMOS 3-state out, 5 kΩ pull-up res.	9.0	1 (11)
BSD5	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 50 kΩ pull-down res.	18.0	1 (12)
BSI5	I/O buffer, CMOS Schmitt in, CMOS 3-state out	18.0	1 (12)
BSU5	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 50 kΩ pull-up res.	18.0	1 (12)
BSW5	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 5 kΩ pull-up res.	18.0	1 (12)
BSD6	I/O buffer, TTL Schmitt in, CMOS 3-state out, 50 kΩ pull-down res.	18.0	1 (12)
BSI6	I/O buffer, TTL Schmitt in, CMOS 3-state out	18.0	1 (12)
BSU6	I/O buffer, TTL Schmitt in, CMOS 3-state out, 50 kΩ pull-up res.	18.0	1 (12)
BSW6	I/O buffer, TTL Schmitt in, CMOS 3-state out, 5 kΩ pull-up res.	18.0	1 (12)
BSIA	I/O buffer, TTL Schmitt in, TTL 3-state out	9.0	1 (12)
BSUA	I/O buffer, TTL Schmitt in, TTL 3-state out, 50 kΩ pull-up res.	9.0	1 (12)
BSWA	I/O buffer, TTL Schmitt in, TTL 3-state out, 5 kΩ pull-up res.	9.0	1 (12)
BSIB	I/O buffer, TTL Schmitt in, TTL 3-state out	18.0	2 (18)
BSUB	I/O buffer, TTL Schmitt in, TTL 3-state out, 50 kΩ pull-up res.	18.0	2 (18)
BSWB	I/O buffer, TTL Schmitt in, TTL 3-state out, 5 kΩ pull-up res.	18.0	2 (18)
BSDC	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 50 kΩ pull-down res.	4.5	1 (11)
BSIC	I/O buffer, CMOS Schmitt in, CMOS 3-state out	4.5	1 (11)
BSUC	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 50 kΩ pull-up res.	4.5	1 (11)
BSWC	I/O buffer, CMOS Schmitt in, CMOS 3-state out, 5 kΩ pull-up res.	4.5	1 (11)
BSDD	I/O buffer, TTL Schmitt in, CMOS 3-state out, 50 kΩ pull-down res.	4.5	1 (11)
BSID	I/O buffer, TTL Schmitt in, CMOS 3-state out	4.5	1 (11)
BSUD	I/O buffer, TTL Schmitt in, CMOS 3-state out, 50 kΩ pull-up res.	4.5	1 (11)
BSWD	I/O buffer, TTL Schmitt in, CMOS 3-state out, 5 kΩ pull-up res.	4.5	1 (11)

Slew Rate Output Buffers

FE03	18 mA CMOS level slew rate output buffer	1 (4)
BE09	18 mA CMOS 3-state slew rate output buffer	1 (5)
BED9	18 mA CMOS 3-state slew rate output buffer with 50K pull-down res.	1 (5)
BEU9	18 mA CMOS 3-state slew rate output buffer with 50K pull-up res.	1 (5)
BEW9	18 mA CMOS 3-state slew rate output buffer with 5K pull-up res.	1 (5)
BE05	18 mA I/O slew rate buffer (CMOS in / CMOS out)	1 (8)
BED5	18 mA I/O slew rate buffer (CMOS in / CMOS out) with 50K pull-down res.	1 (8)

Block Name	Description	Cells
	Interface Blocks (Cont.)	
Slew Rate Output Buffers (Cont.)		
BEU5	18 mA I/O slew rate buffer (CMOS in / CMOS out) with 50K pull-up res.	1 (8)
BEW5	18 mA I/O slew rate buffer (CMOS in / CMOS out) with 5K pull-up res.	1 (8)
BE06	18 mA I/O slew rate buffer (TTL in / CMOS out)	1 (8)
BED6	18 mA I/O slew rate buffer (TTL in / CMOS out) with 50K pull-down res.	1 (8)
BEU6	18 mA I/O slew rate buffer (TTL in / CMOS out) with 50K pull-up res.	1 (8)
BEW6	18 mA I/O slew rate buffer (TTL in / CMOS out) with 5K pull-up res.	1 (8)
BFI5	18 mA Schmitt I/O slew rate buffer (CMOS in / CMOS out)	1 (11)
BFD5	18 mA Schmitt I/O slew rate buffer (CMOS in / CMOS out) with 50K pull-down res.	1 (11)
BFU5	18 mA Schmitt I/O slew rate buffer (CMOS in / CMOS out) with 50K pull-up res.	1 (11)
BFW5	18 mA Schmitt I/O slew rate buffer (CMOS in / CMOS out) with 5K pull-up res.	1 (11)
BFI6	18 mA Schmitt I/O slew rate buffer (TTL in / CMOS out)	1 (11)
BFD6	18 mA Schmitt I/O slew rate buffer (TTL in / CMOS out) with 50K pull-down res.	1 (11)
BFU6	18 mA Schmitt I/O slew rate buffer (TTL in / CMOS out) with 50K pull-up res.	1 (11)
BFW6	18 mA Schmitt I/O slew rate buffer (TTL in / CMOS out) with 5K pull-up res.	1 (11)
Special Blocks		
FIB1	Input buffer, CMOS in, high fanout for clock driver	1 (24)
FIB2	Input buffer, TTL in, high fanout for clock driver	1 (24)
OSF1	Feedback resistance for oscillator (low freq.)	1
OSF2	Feedback resistance for oscillator (high freq.)	1
OSF3	Feedback resistance for oscillator with Enable (low freq.)	1
OSF4	Feedback resistance for oscillator with Enable (high freq.)	1
OSI1	Oscillator input buffer	1
OSI2	Oscillator input buffer with Enable	1
OSO1	Oscillator output buffer with feedback res. (low freq.)	1
OSO2	Oscillator output buffer with feedback res. (high freq.)	1
OSO3	Oscillator output buffer (low freq.)	1
OSO4	Oscillator output buffer (high freq.)	1
OSO7	Oscillator output buffer with feedback res. & Enable (low freq.)	1
OSO8	Oscillator output buffer with feedback res. & Enable (high freq.)	1
SHT1	Monostable multivibrator	1

Notes: Oscillator pins must be used in combination. Some valid combinations are:

OSI1 + OSO1	Low Frequency
OSI1 + OSO3 + OSF1	Low Frequency
OSI1 + OSO2	High Frequency
OSI2 + OSO7	Low Frequency with oscillator Enable
OSI2 + OSO3 + OSF3	Low Frequency with oscillator Enable
OSI2 + OSO8	High Frequency with oscillator Enable
OSI2 + OSO4 + OSF4	High Frequency with oscilator Enable

Block Name	Description	Cells
	Function Blocks - Normal Power	
Inverters		
F101	Inverter (F/O = 17)	1
F102	Inverter (F/O = 37)	2
F103	Inverter (F/O = 60)	3
F104	Inverter (F/O = 92)	4
F108	Inverter (F/O = 160)	12
Buffers		
F111	Non-inverting buffer (F/O = 17)	2
F112	Non-inverting buffer (F/O = 35)	3
F113	Non-inverting buffer (F/O = 54)	4
F114	Non-inverting buffer (F/O = 74)	5
F118	Non-inverting buffer (F/O = 180)	11
NOR Gates		
F202	2-input NOR	2
F203	3-input NOR	3
F204	4-input NOR	4
F208	8-input NOR	7
F222	2-input NOR, power	4
F223	3-input NOR, power	6
F224	4-input NOR, power	8
OR Gates		
F212	2-input OR	2
F213	3-input OR	3
F214	4-input OR	3
F232	2-input OR, power	3
F233	3-input OR, power	4
F234	4-input OR, power	4
NAND Gates		
F302	2-input NAND	2
F303	3-input NAND	3
F304	4-input NAND	4
F305	5-input NAND	5
F306	6-input NAND	5
F308	8-input NAND	6
F322	2-input NAND, power	4
F323	3-input NAND, power	6
F324	4-input NAND, power	8
AND Gates		
F312	2-input AND	2
F313	3-input AND	3
F314	4-input AND	3
F332	2-input AND, power	3
F333	3-input AND, power	4
F334	4-input AND, power	4
AND-NOR Gates		
F421	2-wide 1-2-input AND-OR inverter	3
F422	3-wide 1-1-2-input AND-OR inverter	4
F423	2-wide 1-3-input AND-OR inverter	4
F424	2-wide 2-2-input AND-OR inverter	4
F425	3-wide 2-2-2-input AND-OR inverter	6
F426	2-wide 3-3-input AND-OR inverter	6
F429	4-wide 2-2-2-2-input AND-OR inverter	8

Function Blocks – Normal Power (Cont.)

Block Name	Description	Cells
OR-NAND Gates		
F431	2-wide 1-2-input OR-AND inverter	3
F432	3-wide 1-1-2-input OR-AND inverter	4
F433	2-wide 1-3-input OR-AND inverter	4
F434	2-wide 2-2-input OR-AND inverter	4
F435	2-wide 2-3-input OR-AND inverter	5
F436	2-wide 3-3-input OR-AND inverter	6
F454	4-wide 2-2-2-2-input OR-AND inverter	8
Clock Drivers		
F501	Clock driver	0
F502	Dual clock driver	0
FCK1	Clock driver (F/O = 360)	40
FCK2	Clock driver (F/O = 720)	80
FCK3	Clock driver (F/O = 1080)	120
FCK4	Clock driver (F/O = 1440)	160
FCK5	Clock driver (F/O = 1800)	200
EX-OR Gate		
F511	Exclusive-OR	4
EX-NOR Gate		
F512	Exclusive-NOR	4
Adders		
F521	1-bit full-adder	9
F523	4-bit binary full-adder	32
Buffers		
F531	3-state buffer with Enable	5
F532	3-state buffer with Enable low	5
Decoders		
F561	2-to-4 decoder	10
F981	2-to-4 decoder with Enable low	13
F982	3-to-8 decoder with Enable low	26
Shift Registers		
F911	4-bit shift register with Reset	33
F912	4-bit serial/parallel shift register	35
F913	4-bit parallel shift register with Reset low, Load	39
F914	4-bit shift register	28
Multiplexers		
F569	8-to-1 multiplexer	18
F570	4-to-1 multiplexer	10
F571	2-to-1 multiplexer	6
F572	Quad 2-to-1 multiplexer	14
Latches		
F595	R-S latch	5
F601	D-latch	6
F602	D-latch with Reset	6
F603	D-latch with Reset low	7
F604	D-latch with G driver low	6
F605	D-latch with G low, Reset low	7
F901	4-bit D-latch	20
F902	8-bit D-latch	38

Function Blocks – Normal Power (Cont.)

Block Name	Description	Cells
Flip-Flops		
F596	Synchronous R-S F/F with Set-Reset	11
F611	D-F/F	8
F614	D-F/F with Set-Reset	10
F617	D-F/F with Set-Reset low	10
F631	D-F/F C low	8
F637	D-F/F C low with Set-Reset low	10
F641	D-F/F, buffered	8
F647	D-F/F with Set-Reset low, buffered	10
F661	D-F/F C low, buffered	8
F667	D-F/F C low with Set-Reset low, buffered	10
F714	Toggle F/F with Set-Reset	9
F717	Toggle F/F with Set-Reset low	9
F737	Toggle low F/F with Set-Reset low	9
F744	Toggle F/F with Set-Reset, buffered	9
F747	Toggle F/F with Set-Reset low, buffered	9
F767	Toggle low F/F with Set-Reset low, buffered	9
F771	J-K F/F, buffered	10
F774	J-K F/F with Set-Reset, buffered	12
F777	J-K F/F with Set-Reset low, buffered	12
F781	J-K F/F C low, buffered	10
F787	J-K F/F C low with Set-Reset low, buffered	12
F791	Toggle F/F with Set-Reset and Tog. Enable	12
F792	Toggle low F/F with Set-Reset and Tog. Enable low	12
F922	4-bit D-F/F with Reset	33
F924	4-bit D-F/F	28
Counters		
F961	4-bit synchronous binary counter with Reset low, buffered	52
F962	4-bit synchronous binary up counter with Reset low	38
Comparator		
F985	4-bit magnitude comparator	32
Scan		
S000	Scan path D-F/F with Set-Reset	11
S002	Scan path D-F/F	9
S050	Scan path D-F/F with Set-Reset, Hold	14
S052	Scan path D-F/F with Hold	12
S100	Scan path J-K F/F with Set-Reset	14
S102	Scan path J-K F/F	12
S150	Scan path J-K F/F with Set-Reset, Hold	17
S152	Scan path J-K F/F with Hold	15
S201	Scan path D-latch with Reset	12
S202	Scan path D-latch	11
S301	Scan path D-latch with Reset (ATG)	8
S302	Scan path D-latch (ATG)	7
S999	Scan path 2-to-1 data selector	4
Delays		
F130	Delay block (for monostable multivibrator)	8
F131	Delay gate	6
F132	Delay gate	1

Function Blocks – Low Power

Block Name	Description	Cells
Multiplexer		
L572	Quad 2-to-1 multiplexer	10
Latches		
L601	D-latch	3
L602	D-latch with Reset	4
L603	D-latch with Reset low	4
L604	D-latch with G low driver	3
L605	D-latch with G low, R low	4
L901	4-bit latch	10
L902	8-bit latch	18
Inverter		
L101	Inverter	1
Buffer		
L111	Non-inverting buffer	1
NOR Gates		
L202	2-input NOR	1
L203	3-input NOR	2
L204	4-input NOR	2
OR Gates		
L212	2-input OR	2
L213	3-input OR	2
L214	4-input OR	3
NAND Gates		
L302	2-input NAND	1
L303	3-input NAND	2
L304	4-input NAND	2
L305	5-input NAND	3
L306	6-input NAND	3
AND Gates		
L312	2-input AND	2
L313	3-input AND	2
L314	4-input AND	3
AND-NOR Gates		
L421	2-wide 1-2-input AND-OR inverter	2
L422	3-wide 1-1-2-input AND-OR inverter	2
L423	2-wide 1-3-input AND-OR inverter	2
L424	2-wide 2-2-input AND-OR inverter	2
L425	3-wide 2-2-2-input AND-OR inverter	3
L426	2-wide 3-3-input AND-OR inverter	3
L429	4-wide 2-2-2-2-input AND-OR inverter	4
L442	2-wide 4-4-input AND-OR inverter	4
L462	3-wide 1-2-3-input AND-OR inverter	3

Function Blocks – Low Power

Block Name	Description	Cells
OR-NAND Gates		
L431	2-wide 1-2-input OR-AND inverter	2
L432	3-wide 1-1-2-input OR-AND inverter	2
L433	2-wide 1-3-input OR-AND inverter	2
L434	2-wide 2-2-input OR-AND inverter	2
L435	2-wide 2-3-input OR-AND inverter	3
L436	2-wide 3-3-input OR-AND inverter	3
L454	4-wide 2-2-2-2-input OR-AND inverter	4
EX-OR Gate		
L511	EX-OR	3
EX-NOR Gate		
L512	EX-NOR	3
Decoders		
L561	2-to-4 decoder	6
L981	2-to-4 decoder with Enable low	8
L982	3-to-8 decoder with Enable low	17
Flip Flops		
L611	D-F/F	5
L614	D-F/F with Set-Reset	7
L617	D-F/F with Set-Reset low	7
L631	D-F/F with C low	5
L637	D-F/F with R low, S low, C low	7
L714	Toggle-F/F with Set-Reset	7
L717	Toggle-F/F with Set-Reset low	7
L737	Toggle low F/F with Set-Reset low	7
L922	4-bit D-F/F with Reset	23
L924	4-bit D-F/F	18
Shift Registers		
L911	4-bit shift register with Reset	23
L912	4-bit serial/parallel shift register	23
L913	4-bit parallel in shift register with Reset low	27
L914	4-bit shift register	18

Memory Blocks

High-Speed Basic RAM Blocks - Hard Macros

Block	Description	Basic RAM	BIST	Cells
KD49	Single-port RAM (32 word x 4 bit)	—	—	574
KD8B	Single-port RAM (64 word x 8 bit)	—	—	1672
KD8F	Single-port RAM (256 word x 8 bit)	—	—	5400
KDAB	Single-port RAM (64 word x 10 bit)	—	—	1976
KDAF	Single-port RAM (256 word x 10 bit)	—	—	6600
KE49	Dual-port RAM (32 word x 4 bit)	—	—	820
KE87	Dual-port RAM (16 word x 8 bit)	—	—	520
KE8B	Dual-port RAM (64 word x 8 bit)	—	—	2128
KE8F	Dual-port RAM (256 word x 8 bit)	—	—	6000
KEAB	Dual-port RAM (64 word x 10 bit)	—	—	2432
KEAF	Dual-port RAM (256 word x 10 bit)	—	—	7200

High-Speed Single Port RAM Blocks - Soft Macros

Block	Description	Basic RAM	BIST	Cells
RJ49	Single-port RAM (32 word x 4 bit)	KD49	RU49	778
RJ4B	Single-port RAM (64 word x 4 bit)	KD49	RU4B	1381
RJ4D	Single-port RAM (128 word x 4 bit)	KD49	RU4D	2556
RJ4F	Single-port RAM (256 word x 4 bit)	KD49	RU4F	4908
RJ89	Single-port RAM (32 word x 8 bit)	KD49	RU89	1384
RJ8B	Single-port RAM (64 word x 8 bit)	KD8B	RU8B	1924
RJ8D	Single-port RAM (128 word x 8 bit)	KD8B	RU8D	3632
RJ8F	Single-port RAM (256 word x 8 bit)	KD8B	RU8F	7009
RJ8H	Single-port RAM (512 word x 8 bit)	KD8B	RU8H	13781
RJAB	Single-port RAM (64 word x 10 bit)	KDAB	RUAB	2246
RJAD	Single-port RAM (128 word x 10 bit)	KDAB	RUAD	4262
RJAF	Single-port RAM (256 word x 10 bit)	KDAB	RUAF	8247
RJAH	Single-port RAM (512 word x 10 bit)	KDAB	RUAH	16249
RJC9	Single-port RAM (32 word x 16 bit)	KD49	RUC9	2602
RJCB	Single-port RAM (64 word x 16 bit)	KD8B	RUCB	3666
RJCD	Single-port RAM (128 word x 16 bit)	KD8B	RUCD	7062
RJCF	Single-port RAM (256 word x 16 bit)	KD8B	RUCF	13789
RJEB	Single-port RAM (64 word x 20 bit)	KDAB	RUEB	4306
RJED	Single-port RAM (128 word x 20 bit)	KDAB	RUED	8318
RJEF	Single-port RAM (256 word x 20 bit)	KDAB	RUEF	16265
RJH9	Single-port RAM (32 word x 32 bit)	KD49	RUH9	5030
RJHB	Single-port RAM (64 word x 32 bit)	KD8B	RUHB	7143
RJHD	Single-port RAM (128 word x 32 bit)	KD8B	RUHD	13915
RJKB	Single-port RAM (64 word x 40 bit)	KDAB	RUKB	8423
RJKD	Single-port RAM (128 word x 40 bit)	KDAB	RUKD	16427

High-Speed Dual Port RAM Blocks - Soft Macros

Block	Description	Basic RAM	BIST	Cells
RK49	Dual-port RAM (32 word x 4 bit)	KE49	RU49	1051
RK4B	Dual-port RAM (64 word x 4 bit)	KE49	RU4B	1910
RK4D	Dual-port RAM (128 word x 4 bit)	KE49	RU4D	3690
RK4F	Dual-port RAM (256 word x 4 bit)	KE49	RU4F	6944
RK87	Dual-port RAM (16 word x 8 bit)	KE87	RU87	
RK89	Dual-port RAM (32 word x 8 bit)	KE49	RU89	1904
RK8B	Dual-port RAM (64 word x 8 bit)	KE8B	RU8B	2413
RK8D	Dual-port RAM (128 word x 8 bit)	KE8B	RU8D	4587

Memory Blocks

High-Speed Dual-Port RAM Blocks - Soft Macros (Cont.)

Block	Description	Basic RAM	BIST	Cells
RK8F	Dual-port RAM (256 word x 8 bit)	KE8F	RU8F	8887
RK8H	Dual-port RAM (512 word x 8 bit)	KE8F	RU8H	17501
RKAB	Dual-port RAM (64 word x 10 bit)	KEAB	RUAB	2733
RKAD	Dual-port RAM (128 word x 10 bit)	KEAB	RUAD	5215
RKAF	Dual-port RAM (256 word x 10 bit)	KEAF	RUAF	10125
RKAH	Dual-port RAM (512 word x 10 bit)	KEAF	RUAH	19969
RKC9	Dual-port RAM (32 word x 16 bit)	KE49	RUC9	3612
RKCB	Dual-port RAM (64 word x 16 bit)	KE8B	RUCB	4609
RKCD	Dual-port RAM (128 word x 16 bit)	KE8B	RUCD	8927
RKCF	Dual-port RAM (256 word x 16 bit)	KE8F	RUCF	17491
RKEB	Dual-port RAM (64 word x 20 bit)	KEAB	RUEB	5249
RKED	Dual-port RAM (128 word x 20 bit)	KEAB	RUED	10183
RKEF	Dual-port RAM (256 word x 20 bit)	KE49	RUH9	19968
RKH9	Dual-port RAM (32 word x 32 bit)	KE8B	RUHB	7025
RKHB	Dual-port RAM (64 word x 32 bit)	KE8B	RUHD	8998
RKHD	Dual-port RAM (128 word x 32 bit)	KE8B	RUHD	17604
RKKB	Dual-port RAM (64 word x 40 bit)	KEAB	RUKB	10278
RKKD	Dual-port RAM (128 word x 40 bit)	KEAB	RUKD	20116

High-Density Single-Port RAM Blocks - Soft Macros

Block	Description	Basic RAM	BIST	Cells
RB4D	Single-port RAM (128 word x 4 bit)	—	—	1170
RB4F	Single-port RAM (256 word x 4 bit)	—	—	2133
RB4H	Single-port RAM (512 word x 4 bit)	—	—	4030
RB4M	Single-port RAM (1K word x 4 bit)	—	—	7826
RB4S	Single-port RAM (2K word x 4 bit)	—	—	15434
RB4U	Single-port RAM (4K word x 4 bit)	—	—	30532
RB8D	Single-port RAM (128 word x 8 bit)	—	—	2137
RB8F	Single-port RAM (256 word x 8bit)	—	—	3622
RB8H	Single-port RAM 512 word x 8 bit)	—	—	6999
RB8M	Single-port RAM (1K word x 8 bit)	—	—	11617
RB8S	Single-port RAM (2K word x 8 bit)	—	—	22958
RBAF	Single-port RAM (256 word x 10 bit)	—	—	4439
RBAH	Single-port RAM (512 word x 10 bit)	—	—	8619
RBAM	Single-port RAM (1K word x 10 bit)	—	—	14369
RBAS	Single-port RAM (2K word x 8 bit)	—	—	28450
RBCD	Single-port RAM (128 word x 16 bit)	—	—	4077
RBCF	Single-port RAM (256 word x 16 bit)	—	—	7032
RBCH	Single-port RAM (512 word x 16 bit)	—	—	13764
RBCM	Single-port RAM (1K word x 16 bit)	—	—	22989
RBHD	Single-port RAM (128 word x 32 bit)	—	—	7949
RBHF	Single-port RAM (256 word x 32 bit)	—	—	13844
RBHH	Single-port RAM (512 word x 32 bit)	—	—	27289
RBKF	Single-port RAM (256 word x 40 bit)	—	—	17109
RBKH	Single-port RAM (512 word x 40 bit)	—	—	33769

Memory Blocks (Cont.)

ROM Blocks

Block	Description	Basic RAM	BIST	Cells
J14D	128 word x 4 bit ROM	—	—	720
J14F	256 word x 4 bit ROM	—	—	1040
J14H	512 word x 4 bit ROM	—	—	1512
J14M	1K word x 4 bit ROM	—	—	2408
J14S	2K word x 4 bit ROM	—	—	3960
J14U	4K word x 4 bit ROM	—	—	6776
J18D	128 word x 8 bit ROM	—	—	1040
J18F	256 word x 8 bit ROM	—	—	1456
J18H	512 word x 8 bit ROM	—	—	2352
J18M	1K word x 8 bit ROM	—	—	3784
J18S	2K word x 8 bit ROM	—	—	6600
J18U	4K word x 8 bit ROM	—	—	11704
J18W	4K word x 8 bit ROM	—	—	21584
J1CD	128 word x 16 bit ROM	—	—	1456
J1CF	256 word x 16 bit ROM	—	—	2352
J1CH	512 word x 16 bit ROM	—	—	3696
J1CM	1K word x 16 bit ROM	—	—	6512
J1CS	2K word x 16 bit ROM	—	—	11400
J1CU	4K word x 16 bit ROM	—	—	21280
J1HF	256 word x 32 bit ROM	—	—	3696
J1HH	512 word x 32 bit ROM	—	—	6512
J1HM	1K word x 32 bit ROM	—	—	11248
J1HS	2K word x 32 bit ROM	—	—	21128

Memory Blocks (Cont.)

RAM Test (BIST)

Block	Description	Basic RAM	BIST
RU49	32 word x 4 bit	—	—
RU4B	64 word x 4 bit	—	—
RU4D	128 word x 4 bit	—	—
RU4F	256 word x 4 bit	—	—
RU87	16 word x 8 bit	—	—
RU89	32 word x 8 bit	—	—
RU8B	64 word x 8 bit	—	—
RU8D	128 word x 8 bit	—	—
RU8F	256 word x 8 bit	—	—
RU8H	512 word x 8 bit	—	—
RUAB	64 word x 10 bit	—	—
RUAD	128 word x 10 bit	—	—
RUAF	256 word x 10 bit	—	—
RUAH	512 word x 10 bit	—	—
RUC9	32 word x 16 bit	—	—
RUCB	64 word x 16 bit	—	—
RUCD	128 word x 16 bit	—	—
RUCF	256 word x 16 bit	—	—
RUEB	64 word x 20 bit	—	—
RUED	128 word x 20 bit		
RUEF	256 word x 20 bit	—	—
RUH9	32 word x 32 bit	—	—
RUHB	64 word x 32 bit	—	—
RUHD	128 word x 32 bit	—	—
RUKB	64 word x 40 bit	—	—
RUKD	128 word x 40 bit	—	—

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