UMC UM8881 HB4 Super Energy Star Green (reverse engineered)

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Created by: pc2005 (@vogons or @retroweb discord)

Additional data contributed by: mkarcher (@vogons), jakethompson1 (@vogons), Landau (@retroweb), computerguy096 (@retroweb), Battler (@vogons)

Introduction

UMC didn't make "UM8881 HB4 Super Energy Star Green" technical reference manual public, so I made my own. Pinout obtained *pain*stakingly by measuring a dead (electrically damaged ISA controller, leaked NiCd) ATC-1415 board with UM8881F 9536-ETA chip. Some pin definitions may be inaccurate, incomplete or missing (the board have only 2 SIMM slots, up to 512kB noninterleaved cache and no VLB - some manufacturers designed more features).

Register set will be checked on a working Biostar MB-8433UUD-A motherboard with Am5x86-133 CPU (some settings will probably be incomplete).

TODO

Further measurements would be appreciated. Especially for boards with:

- chip revisions for Biostar MB-8433UUD-A
- make chapter better logically sorted
- Is your cache + TAG address address routing compatible with pin description? My board's manual suggests jumper connection for an address line to TAG RAM pin, which is N/C for the suggested chip size.
- Which PCI AD pins are used for other IDSEL signals? There is probably 1 or 2 additional IDSEL on boards with integrated PCI chips or on board with 4+ PCI slots.
- Is pin 99 TURBO routed to some THT logic gate and to turbo led?
- Pin 170 should be routed to T/R (direction) pin of quad 74F245 buffers. Exact placing not know yet (between DRAM and cache/chipset/CPU, between DRAM/cache and chipset/CPU, ...). Also not know yet where /OE pin of 74F245 buffers is connected to.
- On boards without any 16-bit ISA device (no superIO, no ISA VGA, ...). Are falling/rising times of data pins fast, especially MSB (15 to 8)?
- If somebody volunteers to make a similar (and editable) pinout for UM8886 (F/AF/BF/N) southbridge. I'm definitelly listening :-D.
- IDSEL mapping (also to UM8886). Should clear AD pin names. Different mapping on different revisions. Also TODO unknown revision from AD27/AD29.
- TODO ras before CAS etc, there should be more settings

- TODO I/O port 040b, 04d6, 0481, 0482, 0483, 0487 (eisa 32bit DMA?)
- TODO I/O port 0c04, 0c05
- TODO can the whole system reset be generated in the software?

If you have it on your board, please check it.

References

DRAM pinout and naming used from wikipedia SIMM.

ISA bus pinout and naming used from wikipedia ISA.

PCI bus pinout and naming used from wikipedia Peripheral Component Interconnect.

486 pinout from 486-/PODP-Pinout and Differences. NOTICE A13 and A16 is swapped.

The retroweb discord UM8881 updates page.

Vogons discussion UMC8881/8886 Datasheet. Also MITAC 5023 used as a source of pin names.

Vogons discussion about UM8881 revisions.

Initial kicad symbol generated by Quick KICAD Library Component Builder.

PCI configuration can be listed from MSDOS with Ralf Brown's PCI bus device identifier or with `lspci -nn` command in linux (with `setpci` command you can access each register). There seems to be pciutils version compiled for MSDOS too.

Multiple patents: 5802555, 5737765 which mention "UMC Super Energy Star Green File, UM8881F/8886F".

UMC IDE/EIDE controller datasheets

Revisions

Hostbridge (or northbridge) comes in multiple revisions. EDO seems to be supported only from revision 4 and up. Manual for Pine Technology PT-432B refers to the EDO capable hostbridge as UM8881F/E, manual for Shuttle HOT-433 as UMC8881F-Exx.

Discussion about EDO support is located here.

An exhaustive search of photos resulted in these combinations ("?" marked lines are when view was obscured by a sticker or the photo was too blurry):

HB date-code	HB revision	HB serial	IBC suffix	IBC date-code	IBC revision	IBC serial	Motherboard
9512	BCS	R21614	AF	9514	AYS	R221E6	Aquarius Systems/BCOM MB-4DUPC
9611	ETT	137030	??				U-Board ST1A rev:B
??			AF	9510	AYS	R113E6	Soyo SY-027B2 / SY-027B5
9541	BTA	131510	AF	9527	BYA	R417B0	Shuttle HOT-433
9524	BTA	128910	AF	9544	FYO	MA03B0	QDI P4U880A/IO
9523	BCS	M42926	AF	9544	FYS	MA05C5	QDI P4U880A/IO
9521	BCA	N42649	AF	9521	AYS	M411D6	Protech PM486PU
9511	BCT	R20613	AF	9511	AYS	R205SA	PowerTech MB468
9535	ETA	133570	AF	9523	AYO	N429B6	Pine Technology PT-432A
9528	BTA	129620	AF	9523	AYA	N421F1	Pine Technology PT-431A
9548	ETS	134990	BF	9611	FXS	704050	PCPartner UMC Lite 486
9518	BCA	N30618	AF	9517	AYS	R314F1	PCPartner UMC Lite 486
95??	BTS	??	AF	9515	AYA?	??	PCPartner M486UPI
9606	ETS	134880	BF	9611	FXS	704050	PCChips M921

HB date-code	HB revision	HB serial	IBC suffix	IBC date-code	IBC revision	IBC serial	Motherboard
9535	ETO	133660	AF	9450	AYS	RA2548	PCChips M921
9524	BTO	128630	AF	9540	BYS	R525E6	PCChips M921
9540	BTO	131280	AF	6540	BYS	R603A6	PCChips M921
9524	DYA	R42526	AF	9540	FYA	N904E0	MiTAC/Trigon PL4600C
9519	DYS	R40460	AF	9525	AYS	N508B6	MiTAC/Trigon PH4500AU
9524	BTA	124300	AF	9525	AYS	N516J6	Gigabyte GA-486AM
9523	BCS	N42644	AF	9522	BYS	R423T6	Gigabyte GA-486AM
9520	BCO	R30703	AF	9519	AYS	N409D0	Gigabyte GA-486AM
9512	BCS	R11746	AF	9513	AYS	R222A7	Chicony CH-880C
9514	??	N22820	AF	9517	AYS	R329A6	Biostar MB-84xx-U
9515	BCA	N30513	AF	9514	AYA	R226F6	Biostar MB-8425UUC-A
9511	BCO	R20730	AF	9512	AYS	R215C6	Biostar MB-8425UUC
9620	ETT	13536B	BF	9618	FXS	KM3Z58	U-Board JK-042E
9631	EYA	R62913	BF	9633	FXA	KM4U53	U-Board JK-042E
9611	ETT	137030	??				U-Board JK-042E
9546	ETS	134640	BF	9547	DYS	RA26B5	A-Trend ATC-1415
9519	BCT	N32406	AF	9524	AYA	N428D0	A-Trend ATC-1415
9546	ETS	134350	BF	9547	DYS	RA25F0	A-Trend ATC-1415
9536	ETA	133680	BF	9545	DYS	R702B5	A-Trend ATC-1415
9631	EYS	R62921	BF	9625	FXA	KM4M62	Biostar MB-8425UUD-A
9634	EYT	R63009	BF	9634	FXS	RM5366	Biostar MB-8425UUD-A
9540	ETA	134740	BF	9545	DYS	R630B0	Biostar MB-8425UUD-A
9552	ETS	134630	BF	9602	DYS	RC02J0	Biostar MB-8425UUD-A
9609	ETO	136550	BF	9602	DYS	RB29C5	ECS UP8812 AIO
9645	EYS	MA0508	BF	9645	FXO	KM5T65	Ford Lian 9885AW
9506	BCS	RC2031	AF	9516	AYS	R320C1	MECER CORPORATION B885
9507	BCA	RC2708	??				MG PCI/ISA-UD 486 GRN
9549	BTA	130770	BF	9552	DYS	RB01E0	PCChips M915i
9524	BTS	129180	AF	9524	AYA	N511B6	PCChips M915i
9621	EYT	R42558	BF	9619	CYA	M322N0	PCChips M919 v1.x
9621	EYT	R42436	BF	9617	FXT	ZM3452	PCChips M919 VER 3.3B/F
9630	ETA	R62704	BF	9622	FXS	KM3Z62	PCChips M919 VER 3.4B/F
9623	EYT	R42841	BF	9622	FXT	KM4958	PCChips M919 VER 3.4B/F
9621	EYT	R42436	BF	9619	FXA	704060	PCChips M919 VER 3.4B/F
9642	EYT	M92205	BF	9641	FXA	KM5J73	Pine Technology PT-432B
9507	BCA	RC2033	AF	9509	AYS	RC24B6	Shuttle HOT-433 (Ver. 4.0)
9603	ETS	136560	BF	9602	DYS	RB15D0	Shuttle HOT-433 (Ver. 4.0)
9548	ETS	135830	BF	9604	DYS	SB29A5	Shuttle HOT-433 (Ver. 4.0)
9640	EYO	R80728	BF	9641	FXA	KM5Y53	Shuttle HOT-433 (Ver. 4.0)
9514	BCA	N30349	AF	9514	AYS	R301D1	Shuttle HOT-433 (REV. 1)
9623	EYT	R51027	BF	9636	FXA	RM5666	Sowah Research SR-M401-A
9540	ETA	134740	??				Sowah Research SR-M401-A
9651	EYA	MB1231	BF	9652	FXS	MMBM69	Sunnylab SYL8884PCI-EIC
9606	ETS	134880	BF	9611	FXS	704050	Trang Bow/Trangg Bow TB-486-OB
9614	ETT	??	BF	9615	FXT	KM3453	Trang Bow/Trangg Bow TB-486-OB
9622	EYT	R50934	AF?	9544	FYT	R911A0	Trang Bow/Trangg Bow TB-486-OB
9441	BA	R90519	F	9444	AS	R91328	ECS UM8810P-AIO
9444	BS	R91443	F	9445	BS	R93046	PowerTech MB467
9429	BS	R62582	F	9432	AS	R70166	QDI MP4-P4U880GRN V2
9511	BCT	R20613	F	9513	EYS	R11345	QDI MP4-P4U885G
9525	EYS	R62???	F	9527	EYS	??	Siemens Nixdorf System Board D882
9506	BCA	RC0620	F	9453	BS	RA0650	TK TK8880F/2066
9512	BCT	N21917	F	9513	EYS	R11345	TK TK8880F/2066A2

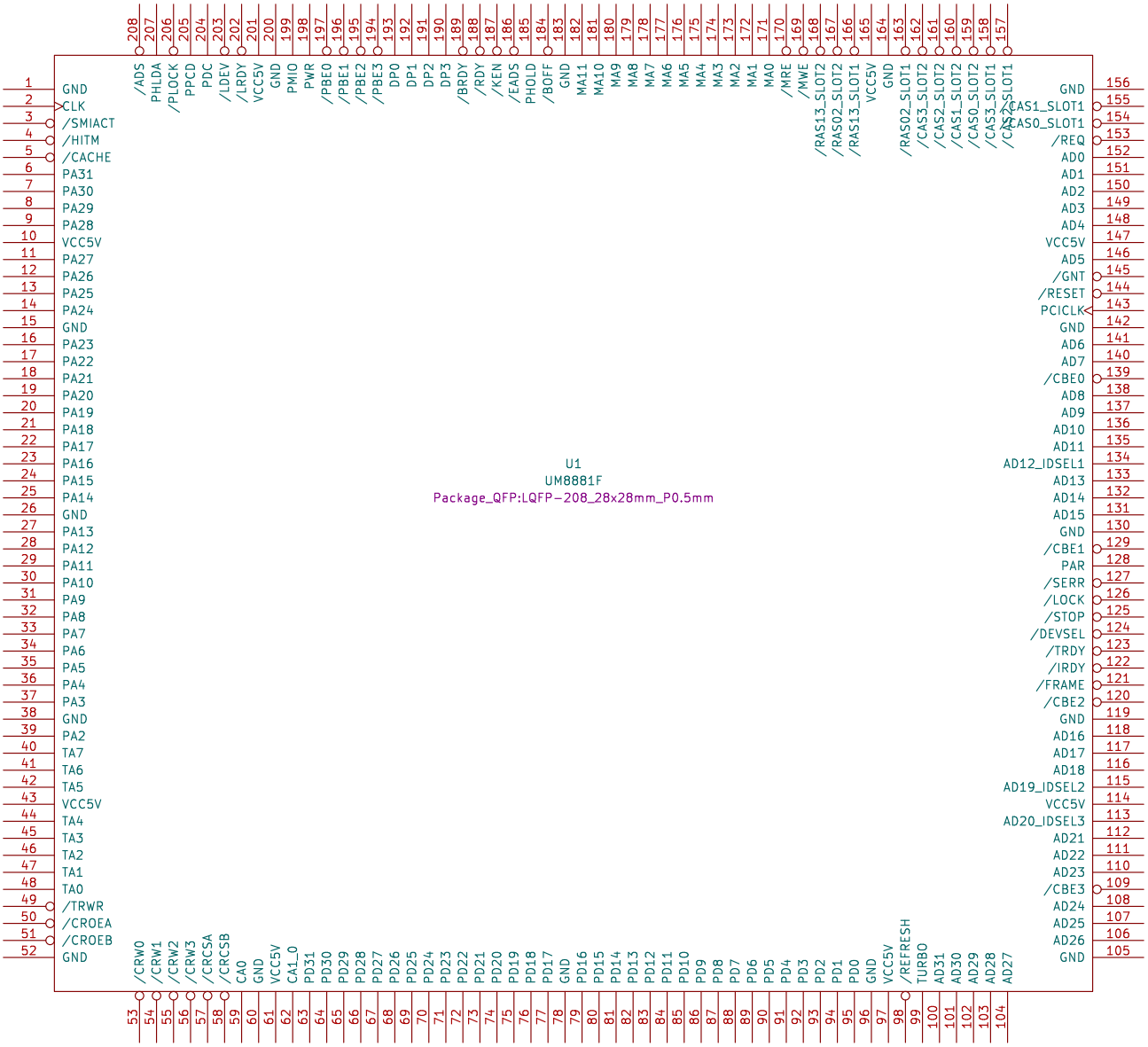
HB date-code	HB revi-sion	HB serial	IBC suf-fix	IBC date-code	IBC revi-sion	IBC serial	Motherboard
9636	EYT	R80720	F	9638	EYT	Z61550	AST Advantage! 575
9437	BA	R73013	F	9437	AA	R80235	Chaintech 4UPB
9435	BS	R72240	F	9437	AA	R80234	DataExpert EXP8046
9446	BCS	RA0844	F	9448	BS	RA2944	ECS UM8810P-AIO (rev 1.x)
9525	BTT	129700	F	9529	EYO	N61265	ECS UM8810P-AIO (rev 2.x)
9451	BCS	RA0433	F	9450	BS	RA3034	ECS UM8810P-AIO (rev 2.x)
9435	BS	R72336	F	9437	AA	R80540	Gigabyte GA-486IM
9448	BCA	RA2749	F	9445	BS	R92941	Gigabyte GA-486IM
9441	BS	R82721	F	9432	AS	R70569	Gigabyte GA-486IM
9449	BCS	RA0631	F	9448	BS	RA1344	Gigabyte GA-486IM
9435	BS	R72636	F	9437	AS	R73138	Gigabyte GA-486IM
9603	ETS	136100	BF	9552	DYS	RB15E0	Shuttle HOT-433 (Ver. 4.0)
9524	BTS	124020	AF	9544	FYT	MA03B5	QDI P4U880A/IO
9528	EYS	R52816	F	9526	EYS	N51484	Siemens Nixdorf System Board D882
9514	BCA	N22726	F	9513	EYS	RC0549	QDI MP4-P4U885G
9520	BCO	N30946	F	9520	EYS	R40554	QDI MP4-P4U885G
9519	BCS	N32215	AF	9519	AYS	N405M6	Pine Technology PT-431A
9620	EYS	R41235	BF	9618	FXA	RM3153	PCChips M919
9444	BS	R91445	F	9445	BS	R92841	PowerTech MB467
9544	ETA	133820	BF	9607	DYS	RB28D0	Sunnylab SYL8884PCI-EIC
9646	EYT	MA1815	BF	9651	FXS	MMBN60	PCChips M919
9540	ETA	133760	BF	9540	DYS	R618F6	Biostar MB-8433UUD-A
9512	BCT	N21918	AF	9516	AYS	R311M6	Shuttle HOT-433 (Ver. 1-3)

NOTICE “serial” code is always different. It could be speculated it may encode the production line, revision and date.

Production date after 1997 was not found anywhere.

Pin assignment and description

Schematic symbol



Pin list overview

1	GND
2	CLK
3	/SMIACT
4	/HITM
5	/CACHE
6	PA31
7	PA30
8	PA29
9	PA28
10	VCC5V
11	PA27
12	PA26
13	PA25
14	PA24
15	GND
16	PA23
17	PA22
18	PA21
19	PA20
20	PA19
21	PA18
22	PA17
23	PA16
24	PA15
25	PA14
26	GND
27	PA13
28	PA12
29	PA11
30	PA10
31	PA9
32	PA8
33	PA7
34	PA6
35	PA5
36	PA4
37	PA3
38	GND
39	PA2
40	TA7
41	TA6
42	TA5
43	VCC5V
44	TA4
45	TA3
46	TA2
47	TA1
48	TA0
49	/TRWR
50	/CROEA
51	/CROEB
52	GND

53	/CRW0
54	/CRW1
55	/CRW2
56	/CRW3
57	/CRCSA
58	/CRCSB
59	CA0
60	GND
61	VCC5V
62	CA1_0
63	PD31
64	PD30
65	PD29
66	PD28
67	PD27
68	PD26
69	PD25
70	PD24
71	PD23
72	PD22
73	PD21
74	PD20
75	PD19
76	PD18
77	PD17
78	GND
79	PD16
80	PD15
81	PD14
82	PD13
83	PD12
84	PD11
85	PD10
86	PD9
87	PD8
88	PD7
89	PD6
90	PD5
91	PD4
92	PD3
93	PD2
94	PD1
95	PD0
96	GND
97	VCC5V
98	/REFRESH
99	TURBO
100	AD31
101	AD30
102	AD29
103	AD28
104	AD27

105	GND
106	AD26
107	AD25
108	AD24
109	/CBE3
110	AD23
111	AD22
112	AD21
113	AD20_IDSEL3
114	VCC5V
115	AD19_IDSEL2
116	AD18
117	AD17
118	AD16
119	GND
120	/CBE2
121	/FRAME
122	/IRDY
123	/TRDY
124	/DEVSEL
125	/STOP
126	/LOCK
127	/SERR
128	PAR
129	/CBE1
130	GND
131	AD15
132	AD14
133	AD13
134	AD12_IDSEL1
135	AD11
136	AD10
137	AD9
138	AD8
139	/CBE0
140	AD7
141	AD6
142	GND
143	PCICLK
144	/RESET
145	/GNT
146	AD5
147	VCC5V
148	AD4
149	AD3
150	AD2
151	AD1
152	AD0
153	/REQ
154	/CAS0_SLOT1
155	/CAS1_SLOT1
156	GND

157	/CAS2_SLOT1
158	/CAS3_SLOT1
159	/CAS0_SLOT2
160	/CAS1_SLOT2
161	/CAS2_SLOT2
162	/CAS3_SLOT2
163	/RAS02_SLOT1
164	GND
165	VCC5V
166	/RAS13_SLOT1
167	/RAS02_SLOT2
168	/RAS13_SLOT2
169	/MWE
170	/MRE
171	MA0
172	MA1
173	MA2
174	MA3
175	MA4
176	MA5
177	MA6
178	MA7
179	MA8
180	MA9
181	MA10
182	MA11
183	GND
184	/BOFF
185	PHOLD
186	/EADS
187	/KEN
188	/RDY
189	/BRDY
190	DP3_/LGNT1
191	DP2_/LGNT2
192	DP1_/LREQ1
193	DP0_/LREQ2
194	/PBE3
195	/PBE2
196	/PBE1
197	/PBE0
198	PWR
199	PMIO
200	GND
201	VCC5V
202	/LRDY
203	/LDEV
204	PDC
205	PPCD
206	/PLOCK
207	PHLDA
208	/ADS

Pin description

Pin	Name	Type	Description
1	GND	power input	Ground
2	CLK	edge input	Chipset clock, via 10R + buffer to UM8886 pin 51
3	/SMIACT	inverted input	Jumper J27, (also near J21 BREQ)
4	/HITM	inverted input	multiple jumpers
5	/CACHE	inverted input	J12.1 (via J12.2 to CPU), connected to J13.2 (via J13.1 to J26.2)
6	PA31	bidir	CPU address 31
7	PA30	bidir	CPU address 30
8	PA29	bidir	CPU address 29
9	PA28	bidir	CPU address 28
10	VCC5V	power input	Power supply +5V
11	PA27	bidir	CPU address 27
12	PA26	bidir	CPU address 26
13	PA25	bidir	CPU address 25
14	PA24	bidir	CPU address 24
15	GND	power input	Ground
16	PA23	bidir	CPU address 23
17	PA22	bidir	CPU address 22
18	PA21	bidir	CPU address 21
19	PA20	bidir	CPU address 20
20	PA19	bidir	CPU/cache/tag address 19/17/15? TODO does 1MiB interleaved cache use pin for TAG address?
21	PA18	bidir	CPU/cache/tag address 18/16/14, cache pin A16, tag pin A13/CE2 (via 512k 1-2 J1 jumper – closer to U1)
22	PA17	bidir	CPU/cache/tag address 17/15/13, cache pin A15, tag pin A14/NC (via 256k 3-4 J1 jumper)
23	PA16	bidir	CPU/cache/tag address 16/14/12, cache pin A14, tag pin A11
24	PA15	bidir	CPU/cache/tag address 15/13/11, cache pin A13, tag pin A10
25	PA14	bidir	CPU/cache/tag address 14/12/10, cache pin A2, tag pin A2
26	GND	power input	Ground
27	PA13	bidir	CPU/cache/tag address 13/11/9, cache pin A3, tag pin A3
28	PA12	bidir	CPU/cache/tag address 12/10/8, cache pin A4, tag pin A4
29	PA11	bidir	CPU/cache/tag address 11/9/7, cache pin A5, tag pin A5
30	PA10	bidir	CPU/cache/tag address 10/8/6, cache pin A6, tag pin A6
31	PA9	bidir	CPU/cache/tag address 9/7/5, cache pin A7, tag pin A7
32	PA8	bidir	CPU/cache/tag address 8/6/4, cache pin A12, tag pin A12
33	PA7	bidir	CPU/cache/tag address 7/5/3, cache pin A0, tag pin A0
34	PA6	bidir	CPU/cache/tag address 6/4/2, cache pin A1, tag pin A1
35	PA5	bidir	CPU/cache/tag address 5/3/1, cache pin A8, tag pin A8
36	PA4	bidir	CPU/cache/tag address 4/2/0, cache pin A9, tag pin A9
37	PA3	output	CPU address 3
38	GND	power input	Ground
39	PA2	output	CPU address 2
40	TA7	bidir	Tag address, to tag data pin 7 (may have permutation)
41	TA6	bidir	Tag address, to tag data pin 6 (may have permutation)
42	TA5	bidir	Tag address, to tag data pin 5 (may have permutation)
43	VCC5V	power input	Power supply +5V
44	TA4	bidir	Tag address, to tag data pin 4 (may have permutation)
45	TA3	bidir	Tag address, to tag data pin 3 (may have permutation)
46	TA2	bidir	Tag address, to tag data pin 2 (may have permutation)
47	TA1	bidir	Tag address, to tag data pin 1 (may have permutation), bootstrap J5.2 via 2k2 to GND or VCC5V
48	TA0	bidir	Tag address, to tag data pin 0 (may have permutation), bootstrap J4.2 via 2k2 to GND or VCC5V

Pin	Name	Type	Description
49	/TRWR	inverted output	Cache tag write enable
50	/CROEA	inverted output	Cache output enable for bank A (or a single bank), via 33R
51	/CROEB	inverted output	Cache output enable for bank B, possibly also via 33R (reported by mkarcher)
52	GND	power input	Ground
53	/CRW0	inverted output	Cache write enable [7:0], to U5 SRAM
54	/CRW1	inverted output	Cache write enable [15:7], to U4 SRAM
55	/CRW2	inverted output	Cache write enable [23:16], to U3 SRAM
56	/CRW3	inverted output	Cache write enable [32:24], to U2 SRAM
57	/CRCSA	inverted output	Cache chip select for bank A (or a single bank), via 33R
58	/CRCSB	inverted output	Cache chip select for bank B, possibly also via 33R (reported by mkarcher)
59	CA0	output	Cache address 0 (single or first interleaved), pin A11
60	GND	power input	Ground
61	VCC5V	power input	Power supply +5V
62	CA1_0	output	Cache address 1 (single bank), address 0 (second interleaved), pin A10
63	PD31	bidir	CPU (host) data 31
64	PD30	bidir	CPU data 30
65	PD29	bidir	CPU data 29
66	PD28	bidir	CPU data 28
67	PD27	bidir	CPU data 27
68	PD26	bidir	CPU data 26
69	PD25	bidir	CPU data 25
70	PD24	bidir	CPU data 24
71	PD23	bidir	CPU data 23
72	PD22	bidir	CPU data 22
73	PD21	bidir	CPU data 21
74	PD20	bidir	CPU data 20
75	PD19	bidir	CPU data 19
76	PD18	bidir	CPU data 18
77	PD17	bidir	CPU data 17
78	GND	power input	Ground
79	PD16	bidir	CPU data 16
80	PD15	bidir	CPU data 15
81	PD14	bidir	CPU data 14
82	PD13	bidir	CPU data 13
83	PD12	bidir	CPU data 12
84	PD11	bidir	CPU data 11
85	PD10	bidir	CPU data 10
86	PD9	bidir	CPU data 9
87	PD8	bidir	CPU data 8
88	PD7	bidir	CPU data 7
89	PD6	bidir	CPU data 6
90	PD5	bidir	CPU data 5
91	PD4	bidir	CPU data 4
92	PD3	bidir	CPU data 3
93	PD2	bidir	CPU data 2

Pin	Name	Type	Description
94	PD1	bidir	CPU data 1
95	PD0	bidir	CPU data 0
96	GND	power input	Ground
97	VCC5V	power input	Power supply +5V
98	/REFRESH	inverted input	DRAM refresh, shared with ISA /REFRESH, via R22 (470R) to +5V, via R23 (33R) to UM8886 p145, via C7 to GND
99	TURBO	output	TODO, via R38 (10k) to +5V, to U18.2 (AND.I1), AND.I2 to UM8886 pin 54 (SMI2/LB2/KBCI), AND.Q via R88 to turbo LED
100	AD31	bidir	PCI Address/Data 31
101	AD30	bidir	PCI Address/Data 30
102	AD29	bidir	PCI Address/Data 29
103	AD28	bidir	PCI Address/Data 28
104	AD27	bidir	PCI Address/Data 27
105	GND	power input	Ground
106	AD26	bidir	PCI Address/Data 26
107	AD25	bidir	PCI Address/Data 25
108	AD24	bidir	PCI Address/Data 24
109	/CBE3	inverted bidir	PCI command/byte enable 3
110	AD23	bidir	PCI Address/Data 23
111	AD22	bidir	PCI Address/Data 22
112	AD21	bidir	PCI Address/Data 21
113	AD20_IDSEL3	bidir	PCI Address/Data 20, IDSEL slot 3
114	VCC5V	power input	Power supply +5V
115	AD19_IDSEL2	bidir	PCI Address/Data 19, IDSEL slot 2
116	AD18	bidir	PCI Address/Data 18
117	AD17	bidir	PCI Address/Data 17
118	AD16	bidir	PCI Address/Data 16
119	GND	power input	Ground
120	/CBE2	inverted bidir	PCI command/byte enable 2
121	/FRAME	inverted bidir	PCI frame signal
122	/IRDY	inverted bidir	PCI initiator ready, via R17 (33R)
123	/TRDY	inverted bidir	PCI target ready, via R18 (33R)
124	/DEVSEL	inverted bidir	PCI target selected
125	/STOP	inverted bidir	PCI target halt request
126	/LOCK	inverted bidir	PCI locked transaction
127	/SERR	inverted open collector	PCI system error
128	PAR	bidir	PCI parity
129	/CBE1	inverted bidir	PCI command/byte enable 1
130	GND	power input	Ground
131	AD15	bidir	PCI Address/Data 15
132	AD14	bidir	PCI Address/Data 14
133	AD13	bidir	PCI Address/Data 13
134	AD12_IDSEL1	bidir	PCI Address/Data 12, IDSEL slot 1
135	AD11	bidir	PCI Address/Data 11
136	AD10	bidir	PCI Address/Data 10
137	AD9	bidir	PCI Address/Data 9
138	AD8	bidir	PCI Address/Data 8
139	/CBE0	inverted bidir	PCI command/byte enable 0
140	AD7	bidir	PCI Address/Data 7
141	AD6	bidir	PCI Address/Data 6
142	GND	power input	Ground
143	PCICLK	edge input	PCI clock input driven via 10R and buffer from UM8886 pin 53
144	/RESET	inverted input	PCI bus + main reset, via inverter (U10) to ISA RESET and UM8886 pin 157

Pin	Name	Type	Description
145	/GNT	inverted input	CPU gets granted PCI bus, driven from UM8886 pin 121
146	AD5	bidir	PCI Address/Data 5
147	VCC5V	power input	Power supply +5V
148	AD4	bidir	PCI Address/Data 4
149	AD3	bidir	PCI Address/Data 3
150	AD2	bidir	PCI Address/Data 2
151	AD1	bidir	PCI Address/Data 1
152	AD0	bidir	PCI Address/Data 0
153	/REQ	inverted output	CPU requests PCI bus, sent to UM8886 pin 124
154	/CAS0_SLOT1	inverted output	DRAM column address strobe 0, SIMM slot 1 (possible permutations)
155	/CAS1_SLOT1	inverted output	DRAM column address strobe 1, SIMM slot 1 (possible permutations)
156	GND	power input	Ground
157	/CAS2_SLOT1	inverted output	DRAM column address strobe 2, SIMM slot 1 (possible permutations)
158	/CAS3_SLOT1	inverted output	DRAM column address strobe 3, SIMM slot 1 (possible permutations)
159	/CAS0_SLOT2	inverted output	DRAM column address strobe 0, SIMM slot 2 (possible permutations)
160	/CAS1_SLOT2	inverted output	DRAM column address strobe 1, SIMM slot 2 (possible permutations)
161	/CAS2_SLOT2	inverted output	DRAM column address strobe 2, SIMM slot 2 (possible permutations)
162	/CAS3_SLOT2	inverted output	DRAM column address strobe 3, SIMM slot 2 (possible permutations)
163	/RAS02_SLOT1	inverted output	DRAM row address strobe 0/2, via buffer to SIMM slot 1 (possible permutations)
164	GND	power input	Ground
165	VCC5V	power input	Power supply +5V
166	/RAS13_SLOT1	inverted output	DRAM row address strobe 1/3, via buffer to SIMM slot 1 (possible permutations)
167	/RAS02_SLOT2	inverted output	DRAM row address strobe 0/2, via buffer to SIMM slot 2 (possible permutations)
168	/RAS13_SLOT2	inverted output	DRAM row address strobe 1/3, via buffer to SIMM slot 2 (possible permutations)
169	/MWE	inverted output	DRAM write enable, via buffer and 10R to all SIMM slots
170	/MRE	output	Via 10R to 4x F245 pin T/R, optional buffer for DRAM data, (dual bank cache MB-4DUPC), TODO more tests
171	MA0	output	DRAM column/row address 0, via buffer
172	MA1	output	DRAM column/row address 1, via buffer
173	MA2	output	DRAM column/row address 2, via buffer
174	MA3	output	DRAM column/row address 3, via buffer
175	MA4	output	DRAM column/row address 4, via buffer
176	MA5	output	DRAM column/row address 5, via buffer
177	MA6	output	DRAM column/row address 6, via buffer
178	MA7	output	DRAM column/row address 7, via buffer
179	MA8	output	DRAM column/row address 8, via buffer
180	MA9	output	DRAM column/row address 9, via buffer
181	MA10	output	DRAM column/row address 10, via buffer
182	MA11	output	DRAM column/row address 11, via 10R
183	GND	power input	Ground

Pin	Name	Type	Description
184	/BOFF	inverted output	CPU backoff from bus
185	PHOLD	output	CPU bus hold, pin E15
186	/EADS	inverted output	CPU external address strobe
187	/KEN	inverted output	CPU cache enable
188	/RDY	inverted output	CPU non-burst ready, pin F16
189	/BRDY	inverted output	CPU burst ready, pin H15
190	DP3_/LGNT1	bidir	CPU data parity 3, VLB local grant 1 (output)
191	DP2_/LGNT2	bidir	CPU data parity 2, VLB local grant 2 (output)
192	DP1_/LREQ1	bidir	CPU data parity 1, VLB local request 1 (input)
193	DP0_/LREQ2	bidir	CPU data parity 0, VLB local request 2 (input)
194	/PBE3	inverted input	CPU byte enable 3
195	/PBE2	inverted input	CPU byte enable 2
196	/PBE1	inverted input	CPU byte enable 1
197	/PBE0	inverted input	CPU byte enable 0
198	PWR	input	CPU write/read bus cycle, goes to jumpers (J15 INV, J17)
199	PMIO	input	CPU memory/IO bus cycle
200	GND	power input	Ground
201	VCC5V	power input	Power supply +5V
202	/LRDY	input	VLB target ready, unimplemented with a pull up via 4k7 (RP12) to VCC5V, TODO direction
203	/LDEV	input	VLB device cycle, unimplemented with a pull up via 4k7 (R52) to VCC5V, TODO direction, (boards use 10k too)
204	PDC	input	CPU data/control bus cycle, pin M15
205	PPCD	input	Page cache disable, pin J17
206	/PLOCK	inverted input	CPU bus lock, pin N15
207	PHLDA	input	CPU hold acknowledge, pin P15
208	/ADS	inverted input	CPU address status

Registers

Both HB and IBC chips (and their revisions) may have lots of nondiscovered configuration registers. These could be probed by brute force R/W of port (often a pair 0x22/0x23) or the rest of the PCI space (both will eventually cause crashes), accesses from different BIOSes or from drivers. Feel free to send your discovery to the discussion.

NOTICE: bits in every Award BIOS can be edited in modbin (index is a value for PCI config access).

Following PCI devices exist, according to the linux database:

```
1060    United Microelectronics [UMC]
    0001    UM82C881
    0002    UM82C886
    0881    UM8881
    0886    UM8886F
    1001    UM886A
    673a    UM8886BF
    886a    UM8886A
    8881    UM8881F
    8886    UM8886F
    888a    UM8886A
```

```
    e881    UM8881N
    e886    UM8886N
    e88a    UM8886N
```

UM8881 host bridge (HB)

Memory map:

```
000e0000 - 000effff     Segment E, can be cacheable, writeable
000f0000 - 000fffff     Segment F, can be cacheable, writeable
fffe0000 - fffeffff     Segment E mirror, read only
ffff0000 - ffffffff     Segment F mirror, read only
```

Preliminary register reset values:

```
50: 00 00 01 00 | 00 40 ff 0f | ff 0f 00 00 | 00 0f 00 ff
60: 00 00 00
```

Register description:

```
40 to 4F
        Not implemented (each returns 0x00 after writing 0xff)

50.80   L2 cache enable
        not sure if really enable (redundancy with size=none)
        May have sequential behavior
50.40   L2 cache mode (WT/WB)
50.30   Cache read burst (3-2-2-2/3-1-1-1/2-2-2-2/2-1-1-1)
        0: 3-2-2-2
        1: 3-1-1-1
        2: 2-2-2-2
        3: 2-1-1-1
50.08   Two banks of cache
50.07   L2 cache size (none/64K/128K/256K/512K/1024K/resvd/resvd)
        6-7 could be 2MiB
        TODO how the size and bankiness relates
        L2 cache must be made coherent with RAM, code cannot be run from cacheable region
            safe region is most likely ffff0000
        L1 invd will trigger L2 cache

51.C0   Read wait state (3/2/1/0)
        0: 3 states
        1: 2 states
        2: 1 state
        3: 0 states
51.30   Write wait state (3/2/1/0)
        0: 3 states
        1: 2 states
        2: 1 state
        3: 0 states
51.08   UNKNOWN, resource lock enable
51.04   A0000-BFFFF(?) PCI write merge
        possible:
        0: vl bus
        1: pci
51.02   Set after memory test, cleared for L1WB
        possible L1 WB policy
        0: WB
        1: WT
```

```
51.01   Tag allocation (7Tag+1Dirty/8Tag+0Dirty)

52.80   CPU to PCI Post Write
        0: 1 WS
        1: 0 WS
52.70   Upper region total capacity
        Is enabled only if lower region is enabled
        Set capacity must be always lower or the same as lower region or excess capacity will be limited t
        Both banks in the region must have the same capacity (or limited or one disabled)
        If one is disabled, is must be again sorted from larger to smaller (0)
        Upper bank could theoretically be not matching and still be used if nonimplemented part marked as

        0: region disabled
        1/2/3/4/5/6/7 same as 52.07
52.08   Assign banks to lower and upper region
        0: lower region will define capacity for banks 0 and 1
            upper region will define capacity for banks 2 and 3
        1: lower region will define capacity for banks 2 and 3
            upper region will define capacity for banks 0 and 1
52.07   Lower region total capacity, physical memory address [0] to [L]
        sets capacity for a pair of banks (= SIMM slots)
        lower region _must_ have a larger capacity than upper region (use 52.08 if banks 2/3 are larger) -
        Lower region will always limit upper region to this capacity

        0: Both regions disabled (entire RAM inaccessible)
        1: 2 MiB
            ?? most likely 1x 9 cols, 10 rows, 61.30 = 00 (ignored)
        2: 4 MiB, 1M addresses
            1x 10 cols, 10 rows, 61.30 = 00
        3: 8 MiB, 2M addresses
            1x 10 cols, 11 rows, 61.30 = 00
            2x 10 cols, 10 rows, 61.30 = 00
        4: 16 MiB, 4M addresses
            1x 11 cols, 11 rows, 61.30 = 00
            2x 10 cols, 11 rows, 61.30 = 00
            1x 10 cols, 12 rows, 61.30 = 30
        5: 32 MiB
            2x 11 cols, 11 rows, 61.30 = 00
            2x 10 cols, 12 rows, 61.30 = 30
        6: 64 MiB
            NOTICE most likely too: 1x 12 cols, 12 rows, asymmetric
            4x 10 cols, 12 rows, 61.30 = 30
            4x 11 cols, 11 rows, 61.30 = 00
        7: 128 MiB
            NOTICE 4x 12 cols, 12 cols would make 256MiB for pair

        rest DRAMs untested (no samples)
        TODO how does older chipset revisions works here (probably no assymetric support)

        (incomplete) extrapolated map [address -> pin] 1x single sided bank
        2-20 static for any mode (exact mapping unknown, likely linear)
        non 4k/symmetric
            next address bit is at new col or row as capacity increases
        4k/12 rows
            next address bits first in "rows" and then in "cols"
```

```
        pin     col     row
        --------------------
        MA0     2       11
        MA1     3       12
        MA2     4       13
        MA3     5       14
        MA4     6       15
        MA5     7       16
        MA6     8       17
        MA7     9       18
        MA8     10      19
        MA9     A       20
        MA10    C       B
        MA11    E       D

        RxC[as] A   B   C   D   E
        10x10   21  NC  NC  NC  NC
        10x11   21  22  NC  NC  NC
        11x11   21  22  23  NC  NC
        10x12as 23  21  24  NC  NC
        12x12as 23  21  24  22  25

        === 1x 32MiB: 10 cols, 12 rows, 2 sides, EDO ===
        52.07 = 05
        61.30 = 30
        === 1x 16MiB: 11 cols, 11 rows, 1 side, FPM ===
        52.07 = 04
        61.30 = 00
        === 1x 16MiB: 11 cols, 11 rows, 1 side, EDO ===
        52.07 = 04
        61.30 = 00
        === 1x 8MiB: 10 cols, 11 rows, 1 side, EDO ===
        52.07 = 03
        53.02 = 00
        61.30 = 00
        === 2x 8MiB: 10 cols, 11 rows, 1 side, EDO ===
        52.07 = 04
        53.02 = 01
        61.30 = 00

53.80   CPU to PCI Burst Write
53.40   Burst copy back option
53.20   swap bank 2/3 (= only bank 3 is used)
53.10   swap bank 0/1 (= only bank 1 is used)
53.08   Upper region sides
        0: single sided
        1: double sided
53.04   Upper region number of banks
        0: 1 bank occupied
        1: 2 banks occupied
53.02   Lower region sides
        0: single sided
        1: double sided
53.01   Lower region number of banks
        0: 1 bank occupied
        1: 2 banks occupied
```

```
54.80   DC000-DFFFF shadow read enable
54.40   D8000-DBFFF shadow read enable
54.20   D4000-D7FFF shadow read enable
54.10   D0000-D3FFF shadow read enable
54.08   CC000-CFFFF shadow read enable
54.04   C8000-CBFFF shadow read enable
54.02   C0000-C7FFF shadow read enable
54.01   E0000-EFFFF shadow read enable

55.80   Global shadow read enable (AND with 54 bits)
        F0000-FFFFF shadow read enable
        0: reads from ROM, writes to RAM (unless readonly)
        1: reads from RAM, writes to RAM (unless readonly)
        L2 cache should be initialized before
55.40   Global shadow write protect
        Without this set, RAM will be always overwritten even if not shadowed
55.20   System BIOS cacheable
        only if shadow is enabled and write protection disabled
55.10   UNKNOWN, cleared in boot block (probably before flash)
55.08   UNKNOWN, cleared in boot block (probably before flash)
55.04   UNKNOWN, cleared in boot block (probably before flash)
55.02   UNKNOWN, cleared in boot block (probably before flash)
55.01   Video BIOS cacheable (TODO which addresses)

56.FF   Memory hole base (in 64K blocks)

57.80   Memory hole enabled/disabled
57.70   Memory hole size (64k/128k/256k/1M/2M/4M/8M/off)
        Can be used to "disable" caching (hole 0-2MiB)
57.0F   UNKNOWN

58.FF   0F if system BIOS cacheable

59.FF   00 if system BIOS cacheable
59.40   freezes linux if set

5A.80   UNKNOWN, crashes kernel
5A.40   Force L2 cache hit
        even if L2 is disabled (50.80)
        but not if RAM is disabled (probably needs computed cacheable range)
5A.20   UNKNOWN, setting seems to not affect L2
5A.10   Enable memory parity
5A.08   UNKNOWN, set to 1 if L2 cache disabled in BIOS (no effect on OS)
5A.04   UNKNOWN, set to 1 if L2 cache disabled in BIOS (no effect on OS)
5A.02   Some kind of deturbo
        could be always cache miss?
        all levels of memory seems to be slowed
        only if .08/04/01 is set
5A.01   Cleared during processor clock measurement

5B.FF   UNKNOWN, returns 0x2c on a booted linux, cannot be changed, but could be status

5C.FF   SMRAM base A27..A20

5D.80   Early Cache Write mode
```

```
5D.40   UNKNOWN
5D.20   UNKNOWN
5D.10   Slow Refresh
5D.0F   SMRAM base A31..A28, set to 0 in linux
        TODO enable PM in BIOS

5E.FF   UNKNOWN, writeable, set to 0x00 in linux

5F.FF   UNKNOWN, writeable, set to 0xff in linux

60.80   UNKNOWN
60.40   UNKNOWN
60.20   Set when enabling classic AMD SMRAM
60.10   UNKNOWN
60.08   UNKNOWN
60.04   UNKNOWN
60.02   Disable memory(?) parity
60.01   Open SMRAM space

61.C0   EDO mode? (no/resvd/resvd/yes)
61.20   Upper region asymmetric DRAM addressing
        Support for 12 columns (MA11)
        TODO document all modes (no 12x12 DRAM to test)
61.10   Lower region asymmetric DRAM addressing
        Support for 12 columns (MA11)
61.08   EDO speed (4-2-2-2/3-1-1-1)
61.04   UNKNOWN
61.02   Cyrix L1WB mode
61.01   UNKNOWN

62.FC   not implemented (cannot be set)
62.02   Burst mode (interleaved/linear)
        setting on am5x86 cause a crash
62.01   Set on early boot for revision "E"

63 to FF
        Not implemented (return 0x00 after writing 0xff)
```

When configured in linux, segment E and segment F are accessible at 0xe0000, 0xf0000, 0xfffe0000 and 0xffff0000. Setting registers 0x54 and 0x55 to 0, 0x58 to 0xff and 0x59 to 0x0f doesn't affect this.

UM8886 ISA bridge controller (IBC), southbridge

There seems to be a pinout difference between UM8886N (also UM886N) (from mitac schematic) and UM8886BF. On ATC-1415 board the keyboard clock is connected to UM8886BF pin 57 but UM8886N has this pin labeled as PGP1/LDEV#/GA20 and the keyboard input KBCLK is on pin 55 instead.

Also the keyboard data leads to pin 56, which is called PGP0(RC#*). UM8886N can have the keyboard input on pin 54, which is labeled "SMI2#/LB2#/KBCI".

UM8886AF seems to be pin to pin compatible with UM8886BF as some boards was sold with both variants. Pinout information about IDE-less UM8886F pin compatibility is not known.

UM8886AF was also found on a pentium board. It seems UM8886 is universal enough to be used as a generic PCI/ISA bridge. Does somebody has an UM8886N on a 486 board? :-D

The "N" version could also be a custom version for laptops/notebooks.

Data bus for BIOS and address/data bus for RTC is buffered via 74F245 and then connected to ISA data pins. BIOS/RTC cycle is distinguished from normal ISA by DIR and /OE pins of this buffer and further control signals. Direction pin 1 of 74F245 is driven from UM8886BF pin 41 XDIR/PGP3/TCWR. Output enable pin 19 is driven from UM8886BF pin 40 XDEN/PGP2/AS01.

IDE on UM8886BF has data pins connected via 74F245 buffer to ISA bus (both primary and secondary). The IDE bandwidth is shared with ISA bandwidth. IDE cycle (primary or secondary) is distinguished from an ISA cycle with /OE and DIR pins of F245 buffers.

It is possible i8042 controller doesn't support 0xD3 command (write byte to thr second PS/2 port output buffer). This will fail autodetection in linux kernel. It is possible BIOS emulates this in SMM handler.

Preliminary register reset values (BF):

```
40: 01 04 08 9a | bc 00 10 30 | 00 00 00 00 | 00 00 00 00
50: 00 02 00 00 | 00 00 00 00 | 00 00 00 00 | 00 00 00 00
rest is zeroed
```

Register description:

```
40.10   Set on B2 revision, but cleared if no PS/2 mouse
40.04   PCI posted memory write
40.03   IBC (ISA bridge controller) devsel decoding (medium/slow/fast/resvd?)
40.02   if set (0x14->0x16), linux freezes

41.40   Disable parity check (maybe PCI SERR#?)
41.20   Set during UM8886BF FIFO mode and restored to prior state afterward
41.04   PCI bus park option 0=enabled (alt "Enhance PCI performance")

43.F0   INTA target IRQ
43.0F   INTB target IRQ
        NOTICE resulting IRQ may collide if incorrectly shared (PS/2 mouse + PCI)
        probably level vs edge triggered

44.F0   INTC target IRQ
44.0F   INTD target IRQ

45.04   Set on B2 revision
45.01   Set on B2 revision, but cleared if no PS/2 mouse

46.80   PM IRQ (10/15)
46.40   PM interrupt method (SMI/IRQ)
46.10   Preempt PCI master option
46.08   INTD enabled
46.04   INTC enabled
46.02   INTB enabled
46.01   INTA enabled

47.40   Enable flash writes (0=enabled, 1=disabled). Interop with 57.4 unknown.
47.08   INTD level triggered
47.04   INTC level triggered
47.02   INTB level triggered
47.01   INTA level triggered

48-4F   UNKNOWN Doesn't retain written value

50.80   Set if PCI video BIOS is installed
        ??? is set even with ISA VGA
```

```
50.01   Set by bootblock after filling segment E and F

51.FE   Size of RAM in units of 4M (rounded down, exception: 4M if rounding down results in 0M)
51.01   Set by bootblock after filling segment E and F

56.80   UNKNOWN
56.60   Cleared by boot block, under some circumstances set by video card setup
56.0C   KBD clock (7MHz/by4/by3/by2)
56.03   ISA clock (by3/by4/by2/resvd?)

57.80   Enable segment C decode to ROM
        Will alias to segment E on 128kB flash
        Visible at FFFC0000
        Causes a bus conflict if ISA decodes too
57.40   Enable segment D decode to ROM
        Will alias to segment F on 128kB flash
        Visible at FFFD0000
        Causes a bus conflict if ISA decodes too
57.20   Enable segment E decode to ROM
        Visible at FFFE0000
        NOTICE segment F is always on
57.10   Set on B2 revision
57.08   Keyboard Emulation
57.04   Some bit used for flash write protection (Guessed: GPO, but seems wrong)
        8886AF/8886BF (Shuttle HOT433 and Biostar UUD8433)
            Set = Protected, Clear = Writeable
        8886F (Gigabyte GA486IM)
            Clear = Protected, Set = Writeable
57.03   IO recovery time (2BLCK/4BCLK/8BCLK/12BCLK)

58-6F   UNKNOWN Doesn't retain written value

70.80   Monitor PCI4 master activity
70.40   Monitor PCI3 master activity
70.20   Monitor PCI2 master activity
70.0F   Green Timer minutes (0.5/1/2/4/8/16/32/64/128/256/512/rsvd/rsvd/rsvd/disable/0.25)

71.80   Monitor PCI1 master activity
71.40   Monitor LPT access
71.20   Monitor COM access
71.10   Monitor ISA DMA master access
71.08   Monitor IDE access
71.04   Monitor Floppy access
71.02   Monitor Graphics card access

72.80   Monitor extra region A9
72.7E   Monitor extra region mask (1=don't care for A0..A5) Really A0?
72.01   Monitor VL slave access

73.FF   Monitor extra region A8-A1

74.01   Monitor ISA shared memory access (A0000-D0000)

76.40   Set in flash-related code
76.30   SMI interface mode (Intel/Cyrix classic/?/AMD classic)
76.08   Will be set by non-PCI VGA access? Cleared and probed in write-merge setup code
```

```
76.04   Cleared by APM init
76.02   Set by APM CPU idle, cleared by APM init

77-7F   UNKNOWN Doesn't retain written value

80.FF   unknown, accessible

81.FF   unknown, accessible

82.03   Set on B2 revision to 3

83.80   1: overloads system with spurious / irq 7
83.40   unknown, accessible, may freeze linux
83.7F   unknown

84-8F   UNKNOWN Doesn't retain written value

90.80   Wake-Up on IRQ7
90.40   Wake-Up on IRQ6
90.20   Wake-Up on IRQ5
90.10   Wake-Up on IRQ4
90.08   Wake-Up on IRQ3
90.04   maybe IRQ2 or gap (some IRQ are unusable)
90.02   maybe IRQ1 or gap (some IRQ are unusable)
90.01   maybe IRQ0 or gap (some IRQ are unusable)

91.80   Wake-Up on IRQ15
91.40   Wake-Up on IRQ14
91.20   maybe IRQ13 or gap (some IRQ are unusable)
91.10   Wake-Up on IRQ12
91.08   Wake-Up on IRQ11
91.04   Wake-Up on IRQ10
91.02   Wake-Up on IRQ9
91.01   Wake-Up on IRQ8

A0      Set to 0 by Boot Block
        Set to 34 by APM init (SMI mask?, 1 = enable)

A1      UNKNOWN
A1.20   if set, freezes linux until keyboard event o_O
A1.10   if set, freezes linux

A2.80   SMM event 7
A2.40   SMM event 6
A2.20   SMM event 5
A2.10   SMM event 4
A2.08   SMM event 3
A2.04   SMM event 2
A2.02   SMM event 1
A2.01   SMM event 0

A4.18   .18:  crash?
A4.03   CPU-to-PCI (2:1/1:1/3:2/resvd?)

A7.FF   unknown, seems to be set at random
        observed values 8f ef
```

```
        affected by IDE? 0->8 after disk access
        8f - ISA GPU, 0f - PCI GPU

A8.FF   Set to 0x28 on Biostar UUD8433
```

IDE controller (only on 8886BF)

The UM8886BF FIFO is 60 bytes in size. There is no intelligence of sector size, multiple sector transfers, ATA vs. ATAPI commands, etc. so the UM8886BF has to be told when to stop reading from the drive by flipping from filling to draining mode at the correct moment, then from draining to disabled when done, on every transfer. This requires changes to the IRQ 14/15 handler. The FIFO cannot just be enabled at boot.

The UM8886BF bus mastering does not support hardware scatter-gather I/O, limiting its utility in a multitasking OS as the driver has to watch register 58h count down to zero before loading the address of the next physical page. There are also alignment restrictions leading to an unaligned head/tail that gets accessed in FIFO PIO or plain PIO mode when doing a bus master read.

The UM8886AF FIFO is 8 bytes in size, and there is no bus mastering, and it doesn't use PCI configuration registers as was already shown above, and doesn't show up as a PCI IDE controller in the list of PCI devices, as if it were a VLB interface. The IDE portion of UM8886AF was also sold as a discrete UM8673 chip on a PCI card but with jumper configuration: Re: UMC IDE/EIDE controller datasheets

The UM8886F lacks IDE and on some boards, is paired with a CMD640 or other non-UMC PCI IDE chip.

It seems I/O ports are mirrored with 0x400 step (0x1f0, 0x5f0, 0x9f0 ... 0x11f0) over entire IO space (excluding decoded PCI BARs).

TODO maybe there is a bit which decode IO ports only at the original location?

```
40.40   Set when FIFO is being accessed using bus mastering, clear otherwise
40.20   Set when FIFO is being accessed using PIO, clear otherwise
40.10   Set when FIFO is filling, clear when draining or disabled
40.08   Set when secondary interface owns FIFO, clear for primary or FIFO disabled

41.80   Enable primary channel
41.40   Enable secondary channel
41.0F   Unknown, set to 0D if north bridge is UM8881N/UM8891N or 09 otherwise
41.04   Cleared above PCI33

42.FF   Set to 33 on boot if north bridge is NexGen/UM8881N/UM8891N or 30 otherwise

43.C0   Timing A, primary master
        0: PIO3, PIO4 (fastest)
        1: PIO2
        2: PIO1
        3: PIO0 (slowest)
        other drives has the same table
43.30   Timing A, primary slave
43.0C   Timing A, secondary master
43.03   Timing A, secondary slave

44.F0   Timing B, primary master
        2: PIO4 (fastest)
        3: PIO3
        4: PIO2
        5: PIO1
        6: PIO0 (slowest)
        other drives has the same table
```

```
44.0F   Timing B, primary slave

45.F0   Timing B, secondary master
45.0F   Timing B, secondary slave

46.F0   Timing C, primary master
        0: PIO4 (fastest)
        1: PIO3
        5: PIO2
        8: PIO1
        b: PIO0 (slowest)
        other drives has the same table
46.0F   Timing C, primary slave

47.F0   Timing C, secondary master
47.0F   Timing C, secondary slave

48-4B   UNKNOWN, writeable, only 0x55555555 observed
        could be some timing base?
4C-4D   UNKNOWN, writeable, only 0x8888 observed
        could be some timing base?
4E-4F   UNKNOWN, writeable, only 0xAAAA observed
        could be some timing base?

50-53   UNKNOWN, writeable, only 0 observed

54-57   Bus mastering physical memory address

58-59   Bus mastering number of DWORDs remaining to transfer

5A-FF   unimplemented (write 0xff, returns 0x00)
```

Pre-8886BF southbridge

Southbridge has a register window located at I/O port 0x108.

```
108     Index register
109     Read/write data register
```

Access needs to be unlocked by writing an unlock sequence. This sequence consists of writing a value 0x4a followed by 0x6c to index port. After that you can write following register indexes to index register and write/read data to/from the data register.

Access can then be locked again by writing a value of 0x34 to the index register.

```
B0.80   Enable primary IDE channel
B0.40   Enable secondary IDE channel

B2.F0   Something for primary master (0=fast, 4=slow)
B2.0F   Something for primary slave

B3.F0   Something for secondary master
B3.0F   Something for secondary slave

B4.F0   Another thing for primary master (3=fast, 12=slow)

B5.0F   Another thing for primary slave
```

```
B6.F0   Another thing for secondary master
B6.0F   Another thing for secondary slave

B7.F0   Third thing for primary master (2=fast, 12=slow)
B7.0F   Third thing for primary slave

B8.F0   Third thing for secondary master
B8.0F   Third thing for secondary slave
```

SuperIO UM8663

There are at least two revisions with AF and BF suffixes. Documentation and functionality difference is not available. It seems the SuperIO contains FDC, LPT, 2x COM, gameport and IDE controllers.

The direct predecessor seems to be um82c863f, which doesn't have a datasheet too, but the is a register description in INTERLOGIC INDUSTRIES ASC486 VER. C manual. The manual was found *after* disassembling the BIOS :-D.

It seems um82c863f has only CR0 and CR1 registers. The variant AF has additional register CR2 and the variant BF probably CR3 and CR4 (untested). BF variant probably supports IrDA on the serial port. If the functionality from F variant propagated to AF and BF there may be also pin strapping mechanism of hardware settings (aka jumpers on ISA card).

UARTs, LPTs (only tested) and probably the rest is decoded over the entire IO space (highers bits of port address are ignored). PCI ranges matching a PCI BAR are excluded.

Disassembling the BIOS for AF variant gained and manual for um82c863f confirmed this access method:

```
108     Index register
109     Read/write data register
```

Similar to IBC, SuperIO also needs to be unlocked first. This is done by writting 0xaa to the index port. Locking can be done in a similar way by writing 0x55. It seems *any* register access must be wrapped inside the lock/unlock sequence.

Poweron values:

```
C0: 2f
C1: 9f
C2: 81
C3: ff
C4: ff
```

It seems BIOS access following configuration registers (CRx):

```
C0.80   UNKNOWN, some kind of status bit?
C0.40   UNKNOWN, writeable to 1
C0.20   UNTESTED gameport enable
C0.10   IDE enable
C0.08   LPT enable
C0.04   COMB enable
C0.02   COMA enable
C0.01   floppy enable

C1.C0   LPT mode
        10 = SPP
        01 = EPP
        11 = ECP
        00 = disabled
        NOTICE may differ from um82c863f
```

```
C1.20   UNTESTED, IDE existence?, defaults to 0
        0: already IDE in the system
        1: no IDE in the system
        NOTICE may differ from um82c863f
C1.10   UNTESTED, IDE base
        0: 170  secondary
        1: 1f0  primary
C1.08   LPT base
        0: 278  LPT2
        1: 378  LPT1
C1.04   COMB base
        0: 2e8  COM4
        1: 2f8  COM2
C1.02   COMA base
        0: 3e8  COM3
        1: 3f8  COM1
C1.01   Floppy base
        0: 370
        1: 3f0

C2.80   Probably chip sleep, COM A/B, LPT, FDC become inoperative if poked with
        TODO init val is 1
C2.40   UNKNOWN
C2.20   setting to 1 disables FDC
C2.10   UNKNOWN
C2.08   UNKNOWN
C2.04   floppy 3 mode
C2.02   UNKNOWN
C2.01   UNKNOWN

C3.FF   UNKNOWN, unimplemented on AF

C4.FF   UNKNOWN, unimplemented on AF
```

TODO:

- pinout?
- Possible swap floppy drives A/B
- POST on LPT
- FDC on LPT
- Gameport
- IDE bases
- LPT/COM IRQ? (probably included in base change)
- BF version (if somebody has a board). There is most likely IR mode for UART.

```
There are three versions of PT-627 as below:
1) PT-627 A - Enhanced IDE + Standard I/O function
(UM8672 + UM82C863 + UM8667)
2) PT-627B - Enhanced IDE+ FIFO UART serial ports+ ECP, EPP or SPP
(UM8672 + UM8663 + UM8667)
3) PT-627C - Enhanced IDE+ FIFO UART serial ports+ ECP,EPP or SPP + 2.88M FDD
(UM8672 + UM8668 + UM8667)
4) PT-627D - Enhanced IDE+ FIFO UART serial port+ standard parallel port
(UM8672 + UM8662 + UM8667)
```

Code snippets

Fill segment E and F

```
HB  55.C0 = 00  unlock
fill
HB  54.01 = 1   ESEG shadow read
IBC 51.01 = 1
IBC 50.01 = 1
HB  55.C0 = C0  lock + FSEG shadow read
```