UMC

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UMC

UM82C451

Parallel/Asynchronous Communication Element

PRELIMINARY

Features

- IBM PC/AT compatible
- UM82C450 with on-board Centronix printer interface
- Completly pin-and upward-compatible with the dual serial channel UM82C452
- Independent control of transmit, receive, line status and data set interrupts
- Individual modem control signals
- Programmable Serial interface characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd-or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus

Description

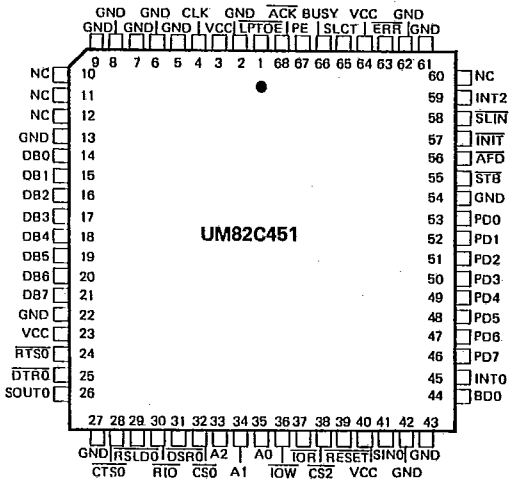
The UM82C451 is an enhanced version of the popular UM82C450 asynchronous communications element (ACE). The serial channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion of data characters transmitted by the CPU. The complete status of the Parallel/Asychronous Communications Element (P/ACE) can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions. It is fully pin-and upward-compatible with the dual serial channel UM82C452. The second serial channel of the UM82C452 occupies pins that are VCC, GND, or NC (not connected) on the UM82C451.

The UM82C451 also provides the user with a fully bi-directional parallel data port that fully supports the parallel Centronics type printer. This port allows information received from either serial communication port to be printed from the P/ACE. The parallel port, together with the serial port, provides IBM PC/AT compatible computers with a single device to serve the two system ports.

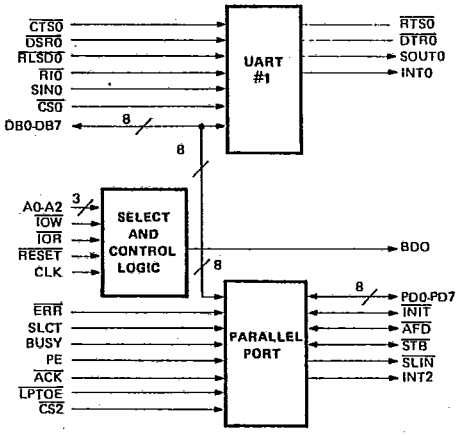
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and (2^{16}–1).

The UM82C451 is packaged in a 68-pin plastic leaded chip carrier.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
37	$\overline{IOR}$	I	Input/Output Read strobe: This is an active Low input signal used to cause the selected channel to output data to data bus (DB0-DB7).
36	$\overline{IOW}$	I	Input/Output Write strobe: This is an active Low input signal used to cause data input from data bus (DB0-DB7) to the channel selected.
33-35	A2-A0	I	Address lines A2-A0: The address lines are used to select the internal register in selected channels during CPU cycle.
32, 38	$\overline{CS0}$, $\overline{CS2}$	I	Chip Selects: Each chip select input acts as an enable of each channel during read and write, $\overline{CS0}$ selects Serial Channel 0 and $\overline{CS2}$ selects Parallel Port.
44	BDO	O	Bus Buffer Output: This active high output is asserted when any channel is selected. This output can be used to control the system bus driver device (74LS245).
14-21	DB0-DB7	I/O	Data Bit DB0-DB7: The data bus provides eight three-state I/O lines for the transfer of data, control and status information between CPU and UM82C451. These lines are normally in a high-impedance state except during read operation. D0 is the least significant bit (LSB) and is the first serial bit to be transmitted or received.
39	$\overline{RESET}$	I	Reset: When low, the reset input forces the UM82C451 into an idle state in which all serial data activities are suspended. The Registers and signals of the UM82C451 are all cleared to the state as indicated in Table 1.
26	SOUT0	O	Serial Data Output: This line is the serial data output of UART, used to transmit serial data to communication link. SOUT is held in marking (logic 1) state when the transmitter is disabled, reset, the Transmitter Register is empty, or when in the loop mode.
41	SIN0	I	Serial Data Input: This line is used to receive serial data from the communication line or modem into the UART. Data on serial data inputs is disabled during the loop mode.
24	$\overline{RTS0}$	O	Request To Send: This signal is an active low output for UART, When active, it informs the Modem or data set that the controller is ready to send data. This signal is set low by writing logic 1 to MCR (1) and reset to high by Reset.
25	$\overline{DTR0}$	O	Data Terminal Ready: This signal is an active low output for UART. When active, it informs the modem or data set that the controller is ready to communicate. This signal is set low by writing logic 1 to MCR (0) and reset to high by Reset.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
28	$\overline{CTS0}$	I	Clear to send: This signal is an active low input for UART. The logic state of this signal is reflected in MSR (4) and any change of state in either $\overline{CTS}$ pin will set DCTS bit MSR (0) of each Modem Status Register. When active, this pin informs that the Modem or data set is ready to receive data.
31	$\overline{DSR0}$	I	Data Set Ready: This signal is an active low input for UART. The logic state of this signal is reflected in MSR (5) and any change of state in either DSR pin will set DDSR bit MSR (1) of each Modem Status Register. When active, the signal informs that the Modem or data set is ready to establish communication.
29	$\overline{RLSD0}$	I	Receiver Line Signal Detect: This is an active low input for UART. The logic state of this signal is reflected in MSR (7) and any change of state in either DCD pin will set DDCD bit MSR (3) of each Modem Status Register. When active, this pin informs that the data carrier has been detected by Modem or data set.
30	$\overline{RI0}$	I	Ring Indicator: This signal is an active low input for UART. The logic state of this signal is reflected in MSR (6) and TERI bit MSR (2) will be set when the state of either RI pin is changed from low to high.
4	CLK	I	Clock Input: The external clock input from a crystal oscillator.
1	$\overline{LPTOE}$	I	Line Printer Output Enable: This input signal enables the data outputs of the parallel line printer when it is low. When it is high, the data pins of line printer are held in a high-impedance state. This pin may be tied to ground for normal line printer operation.
53-46	PD0-PD7	O	Parallel Data Bus: This bus provides a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when the port is not selected.
68	$\overline{ACK}$	I	Acknowledge: This signal goes low to indicate that the printer has already received a character and is ready to accept another.
67	PE	I	Paper Empty: This signal goes high when the line printer has run out of paper.
66	BUSY	I	Busy: This signal goes high when the line printer has a local operation in progress and cannot accept data.
65	SLCT	I	Selected: This signal goes high when the line printer has been selected.

Pin No.	Symbol	I/O	Description
63	$\overline{ERR}$	I	Error: This signal goes low when the line printer has encountered an error condition.
58	$\overline{SLIN}$	I/O	Line Printer Select: This signal is used to select the printer when it is low.
57	$\overline{INIT}$	I/O	Line Printer Initialize: When this signal goes low, it will allow the line printer initialization routine to be started.
56	$\overline{AFD}$	I/O	Line Printer Autofeed: When this signal goes low, it will cause the printer to line-feed after a line is printed.
55	$\overline{STB}$	I/O	Line Printer Strobe: When this signal is low, it provides the line printer a signal to latch the data currently on the parallel port. This signal should keep low at least 0.5 μs to ensure the completion of data latch.
45	INT0	O	Serial Channel Interrupt: Serial channel interrupt goes high when one of the following interrupts has an active condition and is enabled by the IER of its associated channel: Receiver Error Flag, Receiver Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset to low upon appropriate service. This pin will be held in a high-impedance state if the MCR (3) of each associated channel is programmed low (logic 0).
59	INT2	O	Line Printer Interrupt: This interrupt goes low when ACK goes low. This signal is enabled by Bit 4 of the Printer Control Register and will be held in a high-impedance state if Bit 4 of the printer Control Register is programmed low.
3, 23, 40, 64	V_{CC}	I	Power Supply: +5V
2, 5, 6-9, 13, 22, 27, 42, 43, 54, 61, 62	GND		Ground: 0V
10-12, 60	NC		No Connection

Functional Description:

Serial Channel Registers

Three types of internal registers are used in the serial channel of the UM82C451. They are used in the operation of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register. Interrupt Enable Register, and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR (7)] to select the register to be written to or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR (7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The UM82C451 data registers are double-buffered so that read and write operations can be performed at the same

Table 1. Serial Channel Internal Registers

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

Note: The Serial Channel 0 is accessed when $\overline{CS0}$ is low.

time the UART is performing the parallel-to-serial and serial-to-parallel conversion.

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described below.

LCR (0) Word Length Select Bit 0 (WLS0)
LCR (1) Word Length Select Bit 1 (WLS1)
LCR (2) Stop Bit Select (STB)
LCR (3) Parity Enable (PEN)
LCR (4) Even Parity Select (EPS)
LCR (5) Stick Parity
LCR (6) Set Break
LCR (7) Divisor Latch Access Bit (DLAB)

LCR (0) and LCR (1) word length select bit 1: The number of bits in each serial character is programmed as shown in the following chart:

LCR (1)	LCR (0)	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR (2) Stop Bit Select: LCR (2) specifies the number of stop bits in each transmitted character. If LCR (2) is a logic 0, one stop bit is generated in the transmitted data. If LCR (2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR (2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR (3) Parity Enable: When LCR (3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR (4) Even Parity Select: When parity is enabled (LCR (3) = 1). LCR (4)-0 selects odd parity, and LCR (4) = 1 selects even parity.

LCR (5) Stick Parity: When parity is enabled (LCR (3) = 1), LCR (5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR (4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR (6) Break Control: When LCR (6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR (6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT = 1, and clear break when normal transmission has to be restored.

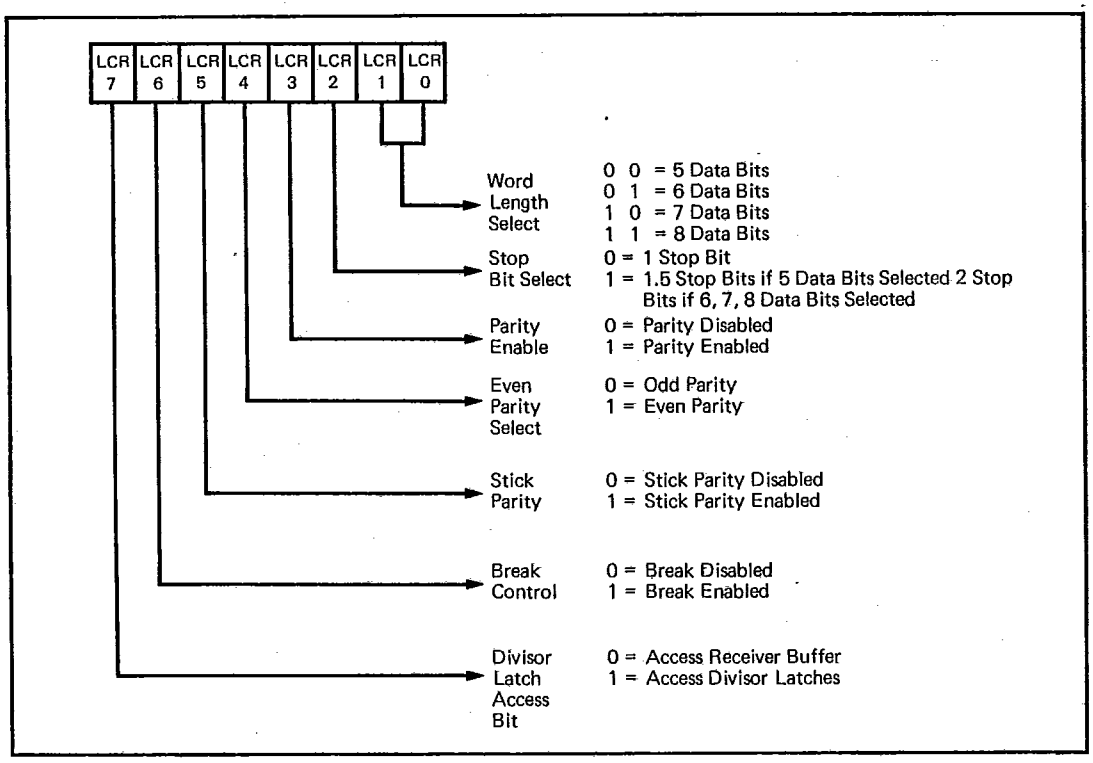


Figure 1. Line Control Register

LCR (7) Divisor Latch Access Bit (DLAB): LCR (7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR (7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the serial channel of the UM82C451.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error character in the Receiver Buffer Register has been over-written by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character. However, it is an entire character, including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER (1)] an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR (1) $\overline{\text{LSR}}$ (4). (OE, PE, FE, and BI.)

The contents of the Line Status Register shown in Table 2 are described as follows:

Table 2. Line Status Register Bits

LSR Bits	Logic 1	Logic 0
LSR (0) Data Ready (DR)	Ready	Not Ready
LSR (1) Overrun Error (OE)	Error	No Error
LSR (2) Parity Error (PE)	Error	No Error
LSR (3) Framing Error (FE)	Error	No Error
LSR (4) Break Interrupt (BI)	Break	No Break
LSR (5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7) Not Used		

LSR (0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR (0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR (1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR (2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit [LCR (4)]. The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR (3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR (3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR (4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR (1)-LSR (4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER (2) = 1 in the Interrupt Enable Register.

LSR (5) Transmitter Holding Register Empty (THRE): THRE indicates that the UM82C450 is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR (5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR (5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER (1) = 1). THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR (6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR (6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR (7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 3. MCR can be written and read. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR (0): When MCR (0) is set high, the $\overline{DTR}$ output is forced low. When MCR (0) is reset low, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR (1): When MCR (1) is set high, the RTS output is forced low. When MCR (1) is reset low, the RTS output is forced high. The $\overline{RTS}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR (3): When MCR (3) is set high, the INT output is enabled.

MCR (4): MCR (4) provides a local loopback feature for diagnostic testing of the channel. When MCR (4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift

Table 3. Modem Control Register Bits

MCR Bits	Logic 1	Logic 0
MCR (0) Data Terminal Ready (DTR)	$\overline{DTR}$ Output Low	$\overline{DTR}$ Output High
MCR (1) Request to Send (RTS)	$\overline{RTS}$ Output Low	$\overline{RTS}$ Output High
MCR (2) 0		
MCR (3) Interrupt (INT) Enable	INT Enabled	INT Disabled
MCR (4) Loop	Loop Enabled	Loop Disabled
MCR (5) 0		
MCR (6) 0		
MCS (7) 0		

Register is looped back into the Receiver Shift Register input. The three modem control inputs ($\overline{CTS}$, $\overline{DSR}$, and $\overline{RI}$) are disconnected. The modem control outputs ($\overline{DTR}$ and $\overline{RTS}$) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high).

In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR (5)-MCR (7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the UM82C451. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for each channel are $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{RLSD}$, $\overline{MSR}$ (4) $\overline{MSR}$ (7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER (3)], a change of state in a modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 4. Note that the states (high or low) of the status bits are inverted versions of the actual input pins.

MSR (0) Delta Clear to Send (DCTS): DCTS indicates that the $\overline{CTS}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR (1) Delta Data Set Ready (DDSR): DDSR indicates

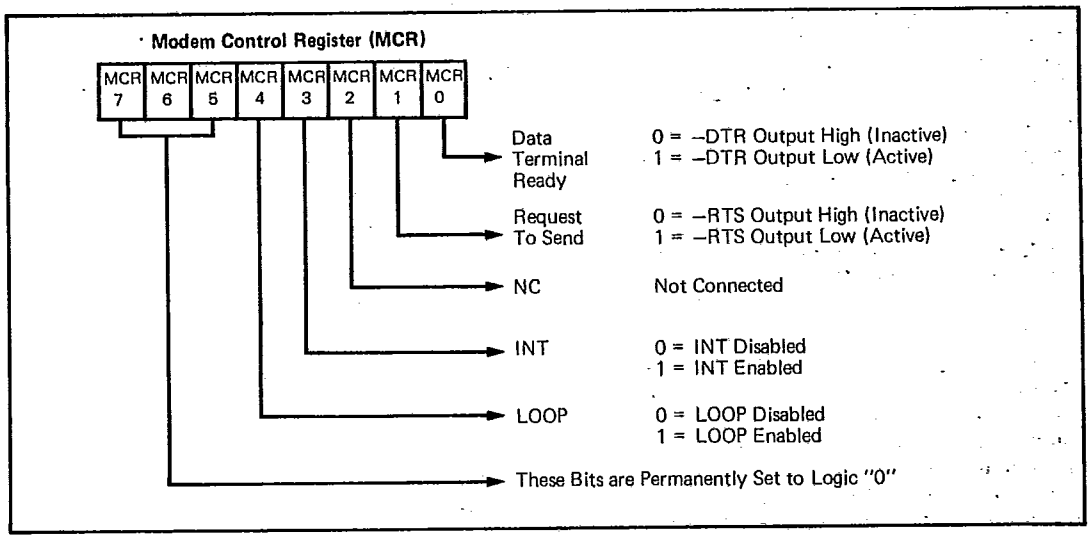


Figure 2. Modem Control Register

Table 4. Modem Status Register Bits

MSR Bit	Mnemonic	Description
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (0)	DCTS	Delta Clear to Send
MSR (3)	DRLSD	Delta Data Carrier Detect
MSR (4)	$\overline{CTS}$	Clear To Send
MSR (5)	$\overline{DSR}$	Data Set Ready
MSR (6)	$\overline{RI}$	Ring Indicator
MSR (7)	$\overline{RLSD}$	Receiver Line Signal Detect

that the $\overline{DSR}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR (2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the $\overline{RI}$ input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on $\overline{RIO}$ do not activate TERI.

MSR (3) Delta Data Carrier Detect (DRSLD): DRSLD indicates that the $\overline{RSLD}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR (4) Clear to Send (CTS): Clear to Send (CTS) is the status of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter, output (SOUT). If the serial channel is in loop mode [MSR (4) = 1]. MSR (4) is equivalent to $\overline{RTS}$ in the MCR.

MSR (5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the $\overline{DSR}$ input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR (4) = 1], MSR (5) is equivalent to DTR in the MCR.

MSR (6) Ring Indicator: Indicates the status to the RI input (pin 39). If the channel is in the loop mode [MCR (4) = 1], MSR (6) is not connected in the MCR.

MSR (7) Receive Line Signal Detect: Receive Line Signal Detect indicates the status of the Receive Line Signal Detect ($\overline{RLSD}$) input. If the channel is in the loop mode [MCR (4) = 1], MSR (4) is equivalent to OUT2 of the MCR.

The modem status inputs ($\overline{RI}$, $\overline{RLSD}$, $\overline{DSR}$, and $\overline{CTS}$) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DRLSD are true, and a state change occurs during a read operation ($\overline{DISTR}$), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read $\overline{DISTR}$ operations. If a status condition is generated during a read DISTR operation, the status bit is not set until the trailing edge of the read $\overline{DISTR}$.

If a status bit is set during a read $\overline{DISTR}$ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read $\overline{DISTR}$ instead of being set again.

The UM82C451 serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to $2^{16}-1$ (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in each serial channel of the UM82C451 is programmable for 5, 6, 7, or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR (0)]. Data Bit 0 of a data word [RBR (0)] is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character results in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7:

RBR (0)	Data Bit 0
RBR (1)	Data Bit 1
RBR (2)	Data Bit 2
RBR (3)	Data Bit 3

RBR (4)	Data Bit 4
RBR (5)	Data Bit 5
RBR (6)	Data Bit 6
RBR (7)	Data Bit 7

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 [THR (0)] is the first serial data bit transmitted. The THRE flag [LSR (5)] reflects the status of the THR. The TEMT flag [LSR (5)] indicates if both the THR and TSR are empty.

THR Bits 0 thru 7

THR (0)	Data Bit 0
THR (1)	Data Bit 1
THR (2)	Data Bit 2
THR (3)	Data Bit 3
THR (4)	Data Bit 4
THR (5)	Data Bit 5
THR (6)	Data Bit 6
THR (7)	Data Bit 7

The Scratchpad Register is an 8-bit Read/Write register that has no effect on either channel in the UM82C451. It is intended to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR (0)	Data Bit 0
SCR (1)	Data Bit 1
SCR (2)	Data Bit 2
SCR (3)	Data Bit 3
SCR (4)	Data Bit 4
SCR (5)	Data Bit 5
SCR (6)	Data Bit 6
SCR (7)	Data Bit 7

Interrupts

The Interrupt Identification Register (IIR) in the serial channel of the UM82C451 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 5 and are described below.

IIR (0): IIR (0) can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR (0) is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR (0) is high, no interrupt is pending.

IIR (1) and IIR (2) are used to identify the highest priority interrupt pending as indicated in Table 5.

IIR (3)-IIR (7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER (0)-IER (3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register is described in Table 6 and below.

IER (0): When programmed high [IER (0) = Logic 1], IER (0) enables Received Data Available Interrupt.

IER (1): When programmed high [IER (1) = Logic 1], IER (1) enables the Transmitter Holding Register Empty interrupt.

IER (2): When programmed high [IER (2) = Logic 1], IER (2) enables the Receiver Line Status interrupt.

IER (3): When programmed high [IER (3) = Logic 1], IER (3) enables the Modem Status Interrupt.

IER (4)-IER (7): These four bits of the IER are logic 0.

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR.

Table 5. Interrupt Identification Register

Interrupt Identification				Interrupt Set and Reset Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	–CTS, –DSR –RI, –RSLD	MSR Read

X = Not Defined.

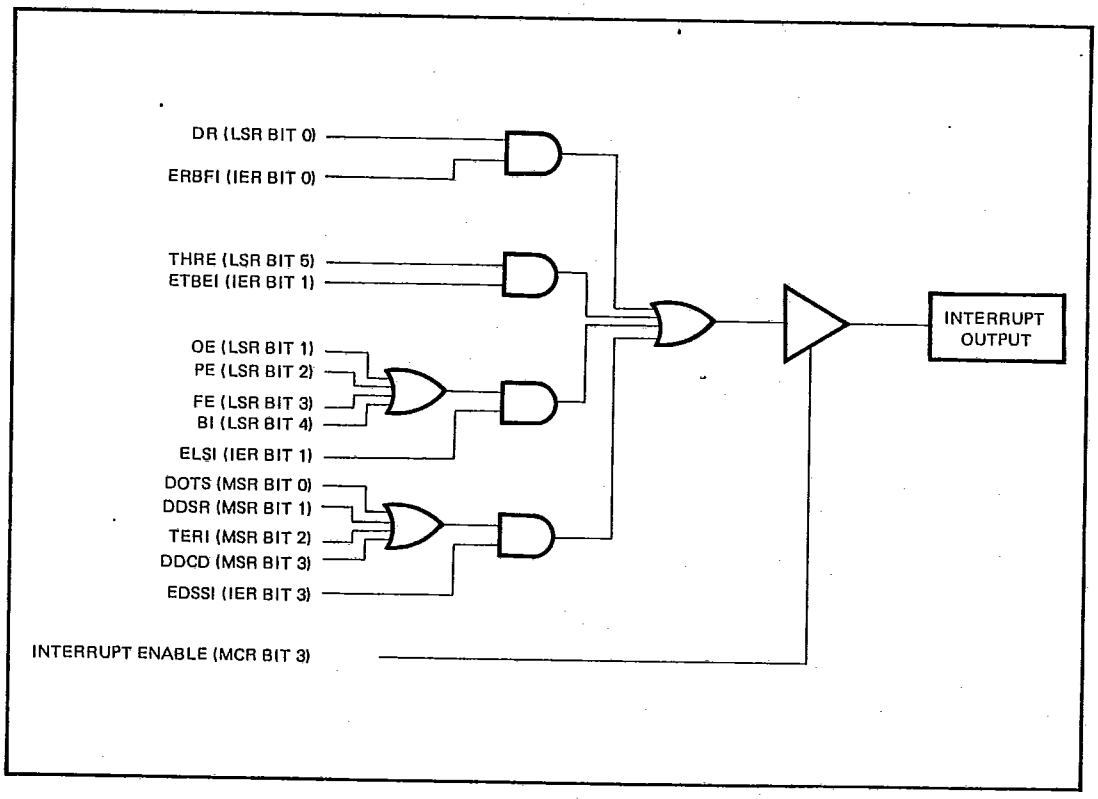


Figure 3. Interrupt Control Logic

Table 6. Serial Channel Accessible Registers

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRSLD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

To transmit a 5 to 8-bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, THRE and TEMT are high. The last word written causes THRE to be reset to 0. After the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSE transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7½, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR (0), LCR (1)), number of stop bits LCR (2), if parity is used LCR (3), and the polarity of parity LCR (4). If Status for the receiver is provided in the Line Status Register to the Receiver Buffer Register when the Data Received indication in LSR (0) is set high, the CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR (0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR (1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR (2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR (3).

The center of the start bit is defined as clock count 7½. If the data into SIN is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

Baud Rate Generator (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL = 1 and DLM = 0 selects the divisor to divide by 1 (divide by 1 gives the maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Tables 7, 8, and 9 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

Reset

After power up, the UM82C451 $\overline{\text{RESET}}$ input should be held low for 500 ns to reset the UM82C451 circuits to an idle mode until initialization. A low on $\overline{\text{RESET}}$ causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not affected.

Following removal of the reset condition (Reset high), the UM82C451 remains in the idle mode until programmed.

A hardware reset of the UM82C451 sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the UM82C451 is given in Table 10.

Programming

Each serial channel of the UM82C451 is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface. While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once a serial channel is programmed and operational, these registers can be updated any time the UM82C451 serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

Software Reset

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Clock Input Operation

The maximum input frequency of the external clock of the UM82C451 is 3.1 MHz.

Table 7. Baud Rates (1.8432 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Table 8. Baud Rates (2.4576 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	–
75	2048	–
110	1396	0.026
134.5	1142	0.0007
150	1024	–
300	512	–
600	256	–
1200	128	–
1800	85	0.392
2000	77	0.260
2400	64	–
3600	43	0.775
4800	32	–
7200	21	1.587
9600	16	–
19200	8	–
38400	4	–

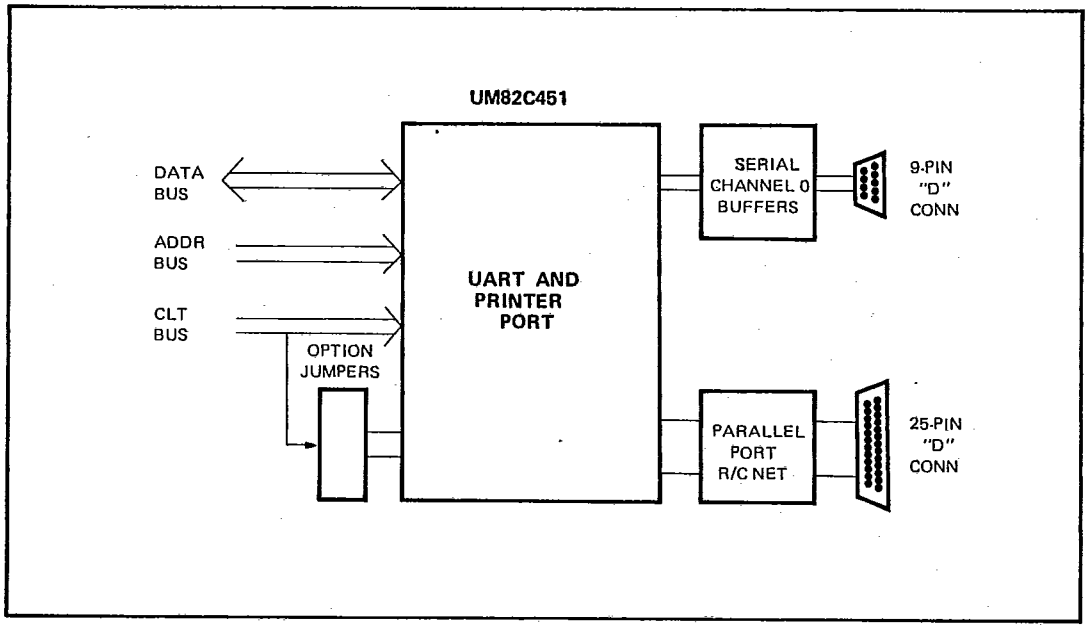
Table 9. Baud Rates (3.072 MHz Clock)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Table 10. Reset Control of Register and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All Bits low
Interrupt Identification Register	Reset	Bit 0 is high and Bits 1-7 are low
Line Control Register	Reset	All Bits low
Modem Control Register	Reset	All Bits low
Line Status Register	Reset	Bits 5, 6 are high, others are low
Modem Status Register	Reset	Bits 0-3 are low, Bits 4-7 are input signals
SOUT0,	Reset	High
$\overline{RTS0}$, $\overline{DTR0}$	Reset	High
INT0, INT2	Reset	High-Impedance
$\overline{STB}$, $\overline{AFD}$, $\overline{SLIN}$,	Reset	High
$\overline{INIT}$	Reset	Low

Device Application



Functional Description:

Parallel Port Register

The UM82C451's parallel port interfaces the device to a Centronics-style printer. When Chip Select 2 ($\overline{CS2}$) is low, ($\overline{IOR}$) and write ($\overline{IOW}$) pins are as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus. The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy ($\overline{BUSY}$), acknowledge ($\overline{ACK}$), which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error. ($\overline{ERROR}$). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines.

They are Interrupt Enable (IRQ ENB), Select In ($\overline{SLIN}$), Initialize the Printer ($\overline{INIT}$), Autofeed the Paper ($\overline{AUTOFD}$), and Strobe ($\overline{STROBE}$), which informs the printer of the presence of a valid byte on the parallel bus. The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

Table 12. Parallel Port Register Select

Control Pins					Register Selected
–IOR	–IOW	–CS2	A1	A0	
0	1	0	0	0	Read Data
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Data
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

Table 11. Parallel Port Registers

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	$\overline{SLIN}$	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$

I/O And Peripherals

AC Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 1, 5)

Serial

Symbol	Parameter	Min	Max	Unit	Conditions
t_{DIW}	$\overline{DISTR}$ Strobe Width	125		ns	
RC	Read Cycle	360		ns	
t_{DDD}	Delay from $\overline{DISTR}$ to Data		125	ns	100 pF Load
t_{HZ}	$\overline{DISTR}$ to Floating Data Delay	0	100	ns	100 pF Load, Note 4
t_{DOW}	$\overline{DOSTR}$ Strobe Width	100		ns	
WC	Write Cycle	360		ns	
t_{DS}	Data Setup Time	40		ns	
t_{DH}	Data Hold Time	40		ns	
t_{RA}	Address Hold Time from $\overline{DISTR}$	20		ns	Note 2
t_{RCS}	Chip Select Hold Time from $\overline{DISTR}$	20		ns	Note 2
tAR	$\overline{DISTR}$ Delay from Address	60		ns	Note 2

AC Characteristics (Continued)

Symbol	Parameter	Min	Max	Unit	Conditions
t_{CSR}	$\overline{DISTR}$ Delay from Chip Select	50		ns	Note 2
t_{WA}	Address Hold Time from $\overline{DOSTR}$	20		ns	Note 2
t_{WCS}	Chip Select Hold Time from $\overline{DOSTR}$	20		ns	Note 2
t_{AW}	$\overline{DOSTR}$ Delay from Address	60		ns	Note 2
t_{CSW}	$\overline{DOSTR}$ Delay from Select	50		ns	Note 2
t_{RW}	Reset Pulse Width	5		μs	
t_{XH}	Duration of Clock High Pulse	140		ns	External Clock
t_{XL}	Duration of Clock Low Pulse	140		ns	External Clock
Transmitter					
t_{HR1}	Delay from Rising Edge of $\overline{DOSTR}$ (WR THR) To Reset Interrupt		175	ns	100 pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start	8	24	CLK cycles	Note 3
t_{SI}	Delay from Initial Write to Interrupt	16	32	CLK cycles	Note 3
t_{STI}	Delay from Stop to Interrupt (THRE)	8	8	CLK cycles	Note 3
t_{IR}	Delay from $\overline{DISTR}$ (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
Modem Control					
t_{MDO}	Delay from $\overline{DISTR}$ (WR MCR) to Output		200	ns	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		200	ns	100 pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$ (RS MSR)		250	ns	100 pF Load
Receiver					
t_{SINT}	Delay from Stop to Set Interrupt	1	1	CLK cycles	Note 3
t_{RINT}	Delay from $\overline{DOSTR}$ (RD RBR/RDLSR) to Reset Interrupt		1	μs	100 pF Load

Parallel Port

WRITE					
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**	
T_{WW}	Write Pulse Width	200	–	ns	
T_{AW}	Address to $\overline{IOW}$ Set-up Time	20	–	ns	
T_{WA}	Address Hold Time after $\overline{IOW}$	20	–	ns	
T_{DW}	Data to $\overline{IOW}$ Set-up Time	70	–	ns	
T_{WD}	Data Hold Time after $\overline{IOW}$	30	–	ns	
T_{WOL}	$\overline{IOW}$ = 1 to Data Latched	–	90	ns	

READ

Symbol	Parameter	Min.	Max.	Unit
T_{RR}	Read Pulse Width	300	–	ns
T_{AR}	Address to $\overline{IOR}$ Set-up Time	20	–	ns
T_{RA}	Address Hold Time after $\overline{IOR}$	20	–	ns
T_{PR}	Printer Bus to $\overline{IOR}$ Set-up Time	0	–	ns
T_{RP}	Printer Bus Hold Time after $\overline{IOR}$	0	–	ns
T_{RDS}	$\overline{IOR}$ to D0 – D7 Output	–	70	ns
T_{RDR}	D0 – D7 Released after $\overline{IOR}$	–	30	ns

*Note: When the CPU reads the printer's status, output data may change if the printer signals are unstable.

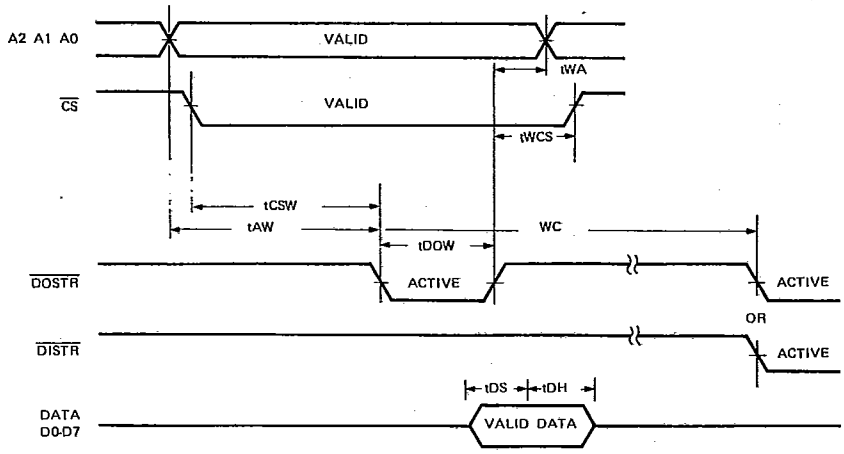
OTHERS

Symbol	Parameter	Min.	Max.	Unit
T_{RSW}	Reset Pulse Width	40	–	ns
T_{RSCH}	Reset to Control Bus = 1 ($\overline{STROB}$, $\overline{AUTOFD}$, $\overline{SLCT}$) Propagation Delay	–	90	ns
T_{RSIN1}	Reset to Control Bus $\overline{INIT}$ = 0 Propagation Delay	–	60	ns
T_{ID}	$\overline{ACK}$ to IRQ Propagation Delay	–	45	ns

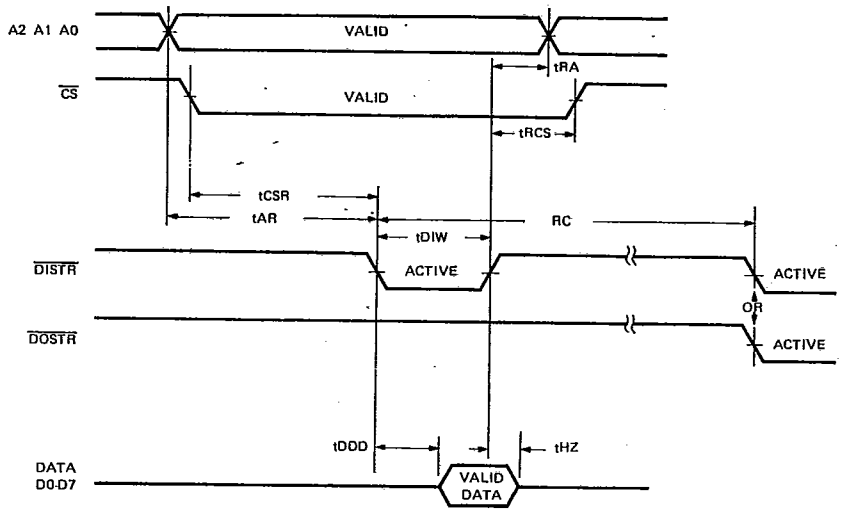
Notes:
1. All timing specifications apply to pins to both serial channels (e. g. Ri refers to both R10 and R11).
2. The internal address strobe is always active.
3. RCLK = t_{XH} and t_{XL}.
4. Charge and discharge time is determined by VOL, VOH, and the external loading.
5. All timings are referenced to valid 0 and valid 1 (see AC TEST POINTS).

Serial Port Timing:

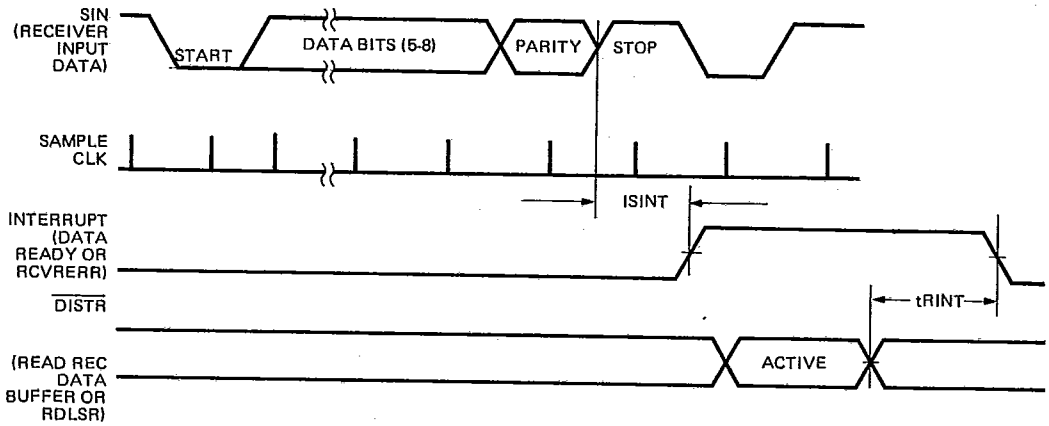
Write Cycle Timing



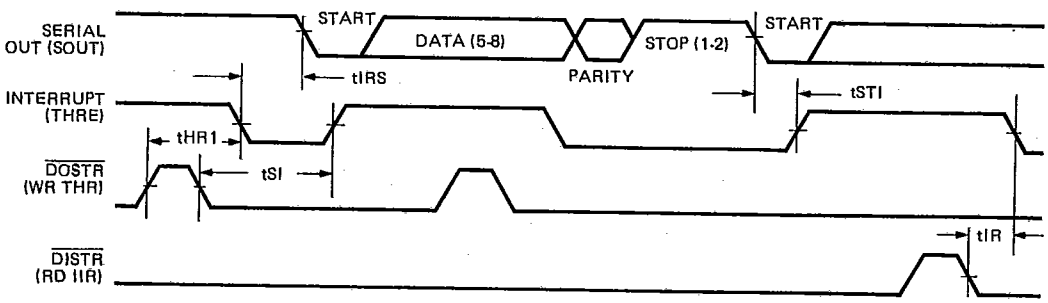
Read Cycle Timing



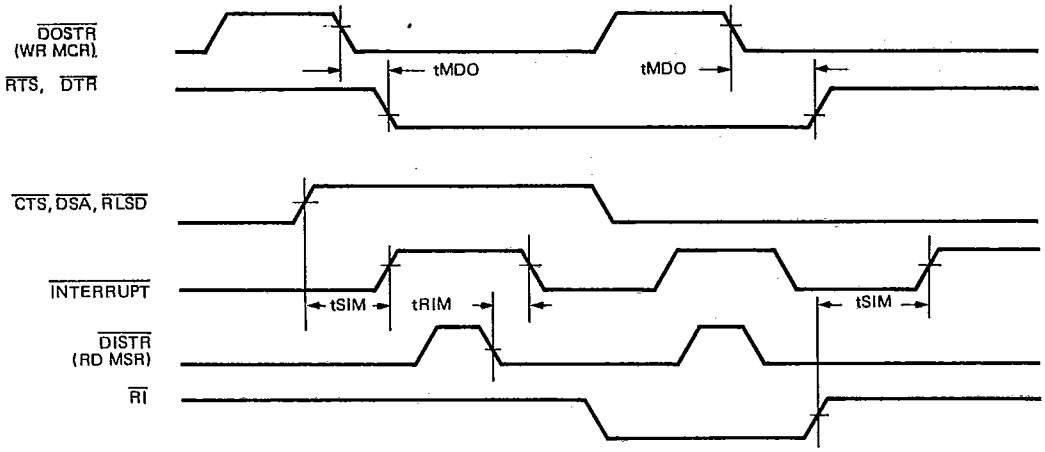
Receiver Timing



Transmitter Timing

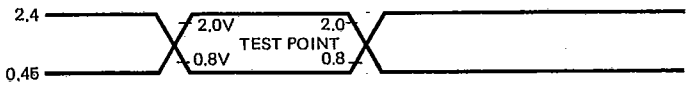


Modem Timing



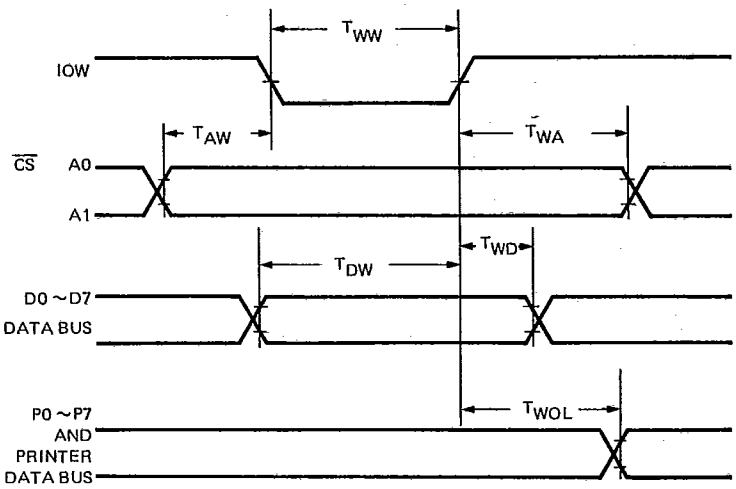
Parallel Port Timing:

A.C. Testing Input Waveform



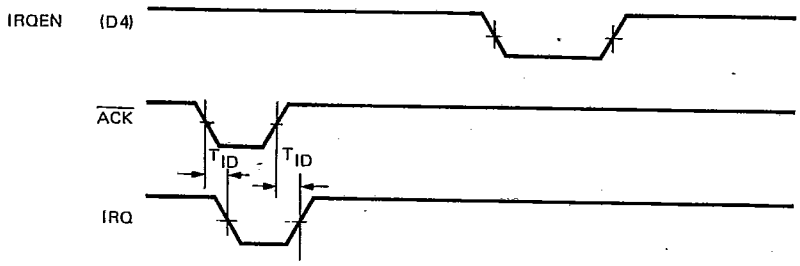
OUTPUT LOAD: 50 pF

Write Cycle Waveform

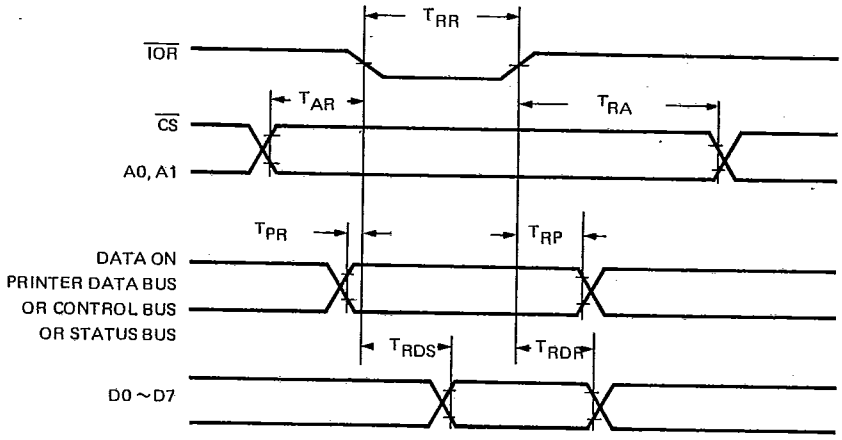


I/O And Peripherals

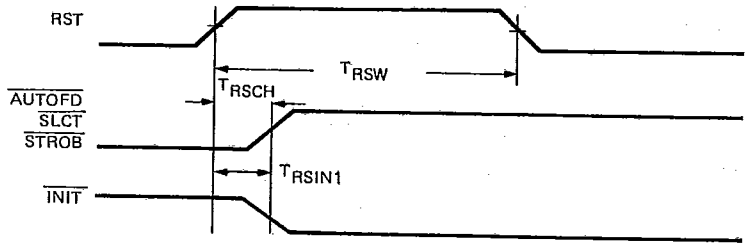
Interrupt Request Waveform



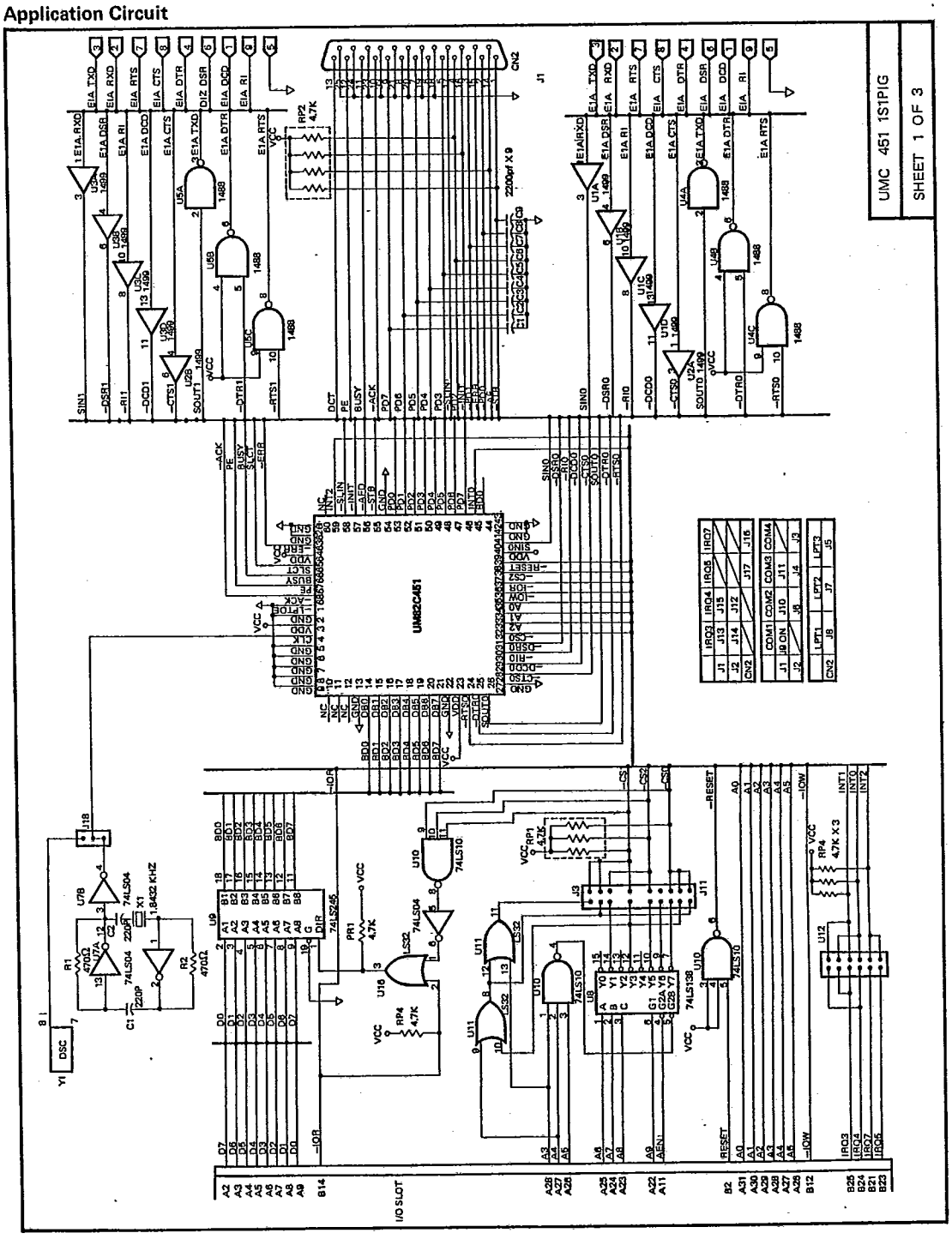
Read Cycle Waveform



Reset Waveform

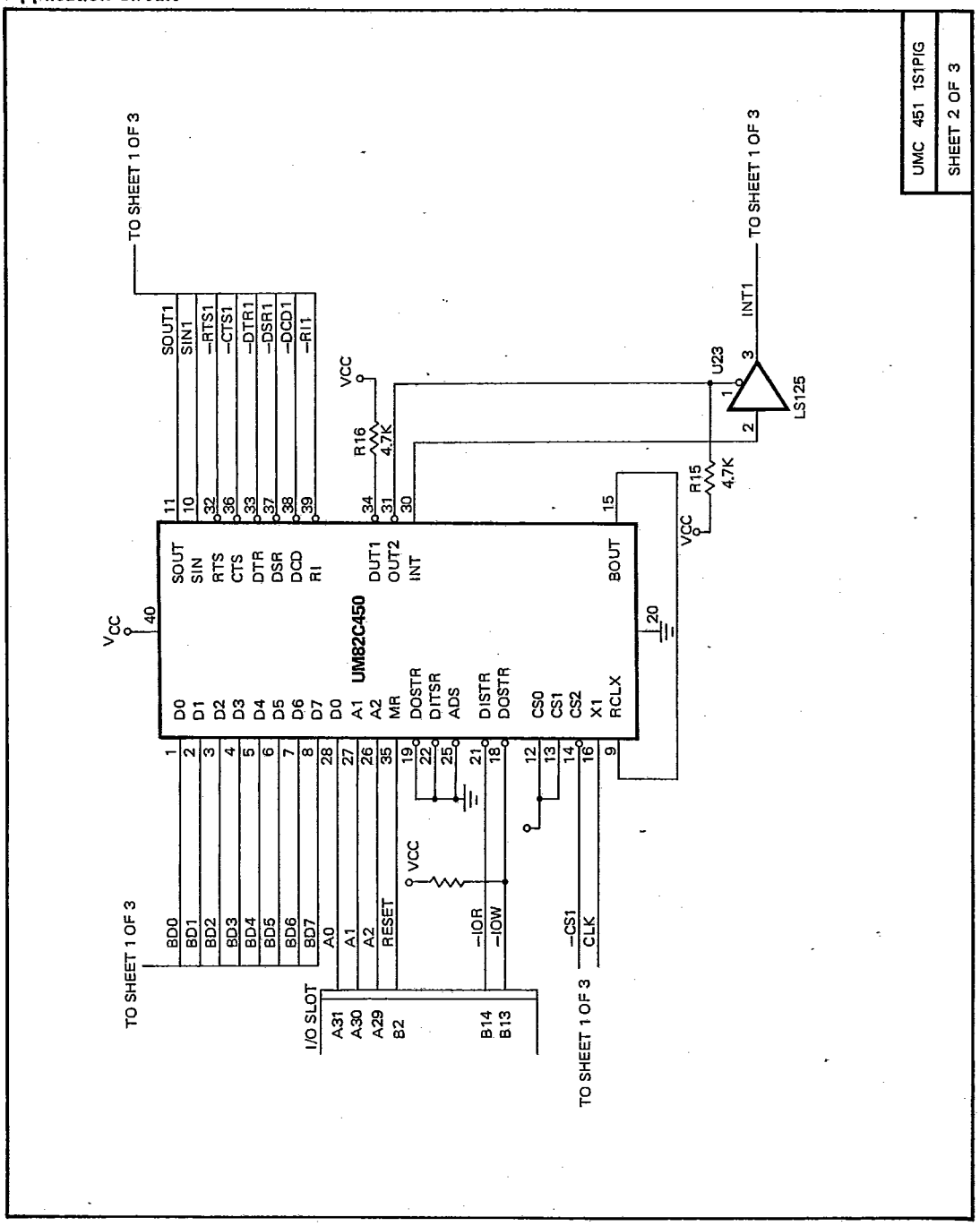


Application Circuit

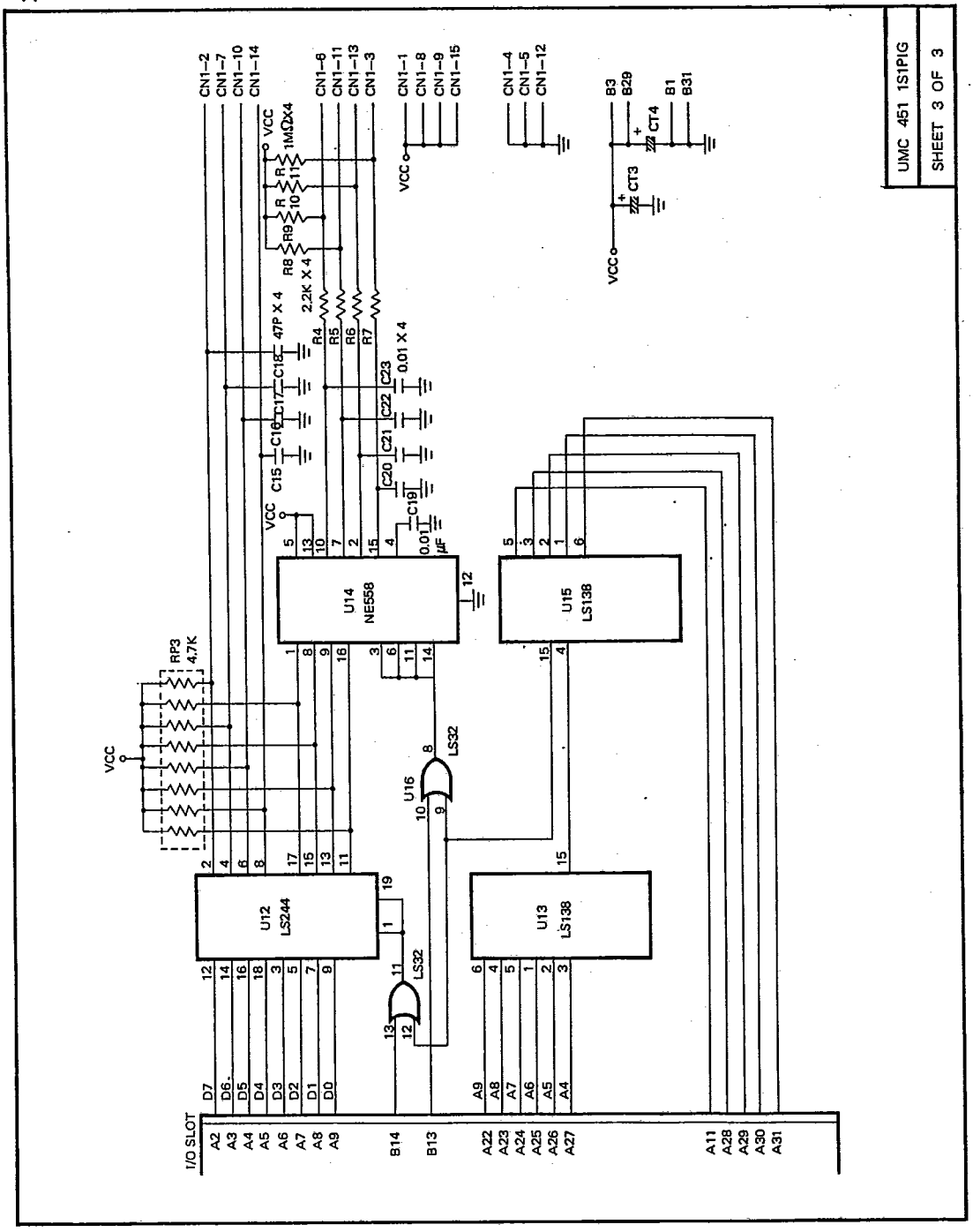


I/O And Peripherals

Application Circuit



Application Circuit



Absolute Maximum Ratings *

Ambient Operating Temperature . . . . . –10°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
Supply Voltage to Ground
Potential . . . . . –0.5V to V_{CC} + 0.3V
Applied Output Voltage . . . . . –0.5V to V_{CC} + 0.3V
Applied Input Voltage . . . . . –0.5V to + 7.0V
Power Dissipation . . . . . 500 mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{ILX}	Clock Input Low Voltage	–0.5	0.8	V	
V_{IHX}	Clock Input High Voltage	2.0	V_{CC}	V	
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4.0 mA on DB0-DB7, I_{OL} = 12 mA on PD0-PD7, I_{OL} = 10 mA on –INIT, –AFD, –STB, and –SLIN (see Note 1), I_{OL} = 2.0 mA on all other outputs
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –0.4 mA on DB0-DB7, I_{OH} = –2.0 mA on PD0-PD7, I_{OH} = –0.2 mA on –INIT, –AFD, –STB, and –SLIN, I_{OH} = –0.2 mA on all other outputs
I_{CC}	Power Supply Current		40	mA	V_{CC} = 5.25 V, No loads on SIN0, 1; –DISTR0, 1; –RLSD0, 1; –CTS0, 1; –RI0, –RI1 = 2.0V. Other = 0.8V, Baud rate generator = 4 MHz. Baud rate = 56K
I_{IL}	Input Leakage		10	μA	V_{CC} = 5.25 V, GND = 0V All other pins floating
I_{CL}	Clock Leakage		10	μA	V_{IN} = 0 V, 5.25V
I_{OZ}	3-State Leakage		20	μA	V_{CC} = 5.25V, GND = 0V, VOUT = 0V, 5.25V 1) Chip deselected 2) Chip and write mode selected
V_{IL} (RES)	Reset Schmitt V_{IL}		0.8	V	
V_{IH} (RES)	Reset Schmitt V_{IH}	2.0		V	

Note 1. $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ are open collector output pins that each have an internal pull-up resistor (2.5 kΩ 3.5 kΩ) to V_{CC}. This will generate a maximum of 2.0 mA of internal I_{OL}. In addition to this internal current, each pin will sink at least 10 mA, while maintaining the V_{OL} specification of 0.4V Max.