UMC

T-52-33-61

UMC

UM8272A/A-4

Floppy Disk Controller

Features

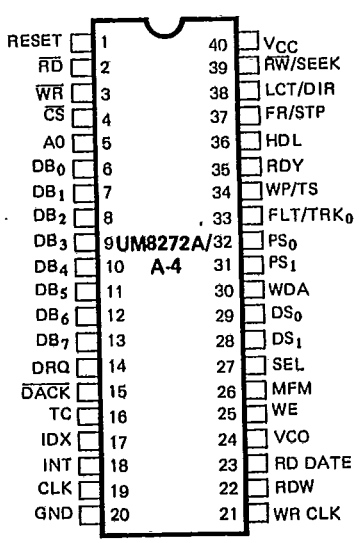
- IBM compatible in both single and double density recording formats
- Programmable data record lengths: 128, 256, 512, or 1024 bytes/sector
- Multi-sector and multi-track transfer capability
- Drives up to 4 floppy or mini-floppy disks
- Data transfers in DMA or Non-DMA mode
- Parallel seek operations on up to four drives
- Compatible with all INTEL and most other microprocessors
- Single-phase 8MHz/4MHz clock for UM8272A/UM8272A-4 respectively
- Single + 5 volt power supply (± 10%)

General Description

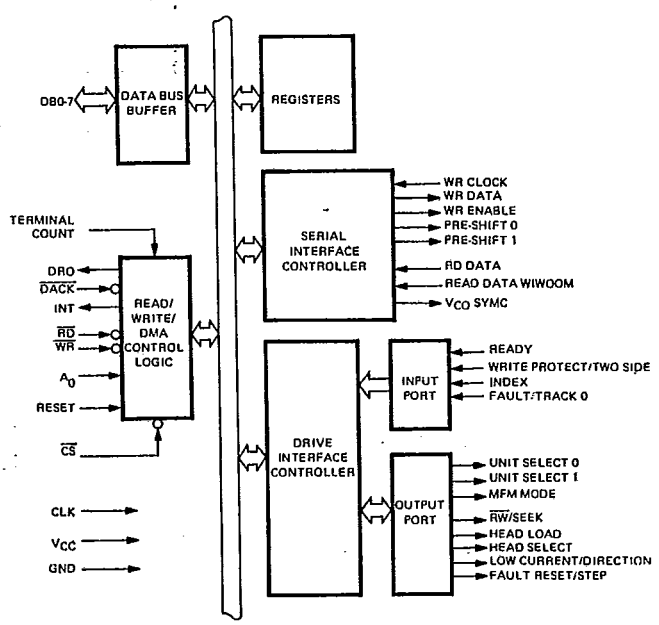
The UM8272A/A-4 is a LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 floppy disk drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 double density format (MFM) including double sided recording.

Storage

Pin Configuration



Block Diagram



The UM8272A/A-4 provides control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy disk drive interface. The UM8272A/A-4 is a pin-compatible upgrade of the 8272.

Hand-shaking signals are provided in the UM8272A/A-4 which make DMA operation easy to incorporate with the aid of an external DMA controller chip. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the UM8272A/A-4 and DMA controller.

There are 15 separate commands which the UM8272A/A-4 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

Read Data	Write Data
Read ID	Format a Track
Read Deleted Data	Write Deleted Data
Read a Track	Seek
Scan Equal	Recalibrate (Restore to Track 0)
Scan High or Equal	Sense Interrupt Status
Scan Low or Equal	Sense Drive Status
Specify	

Address mark detection circuitry is internal to the FDC, which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The UM8272A/A-4 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density models.

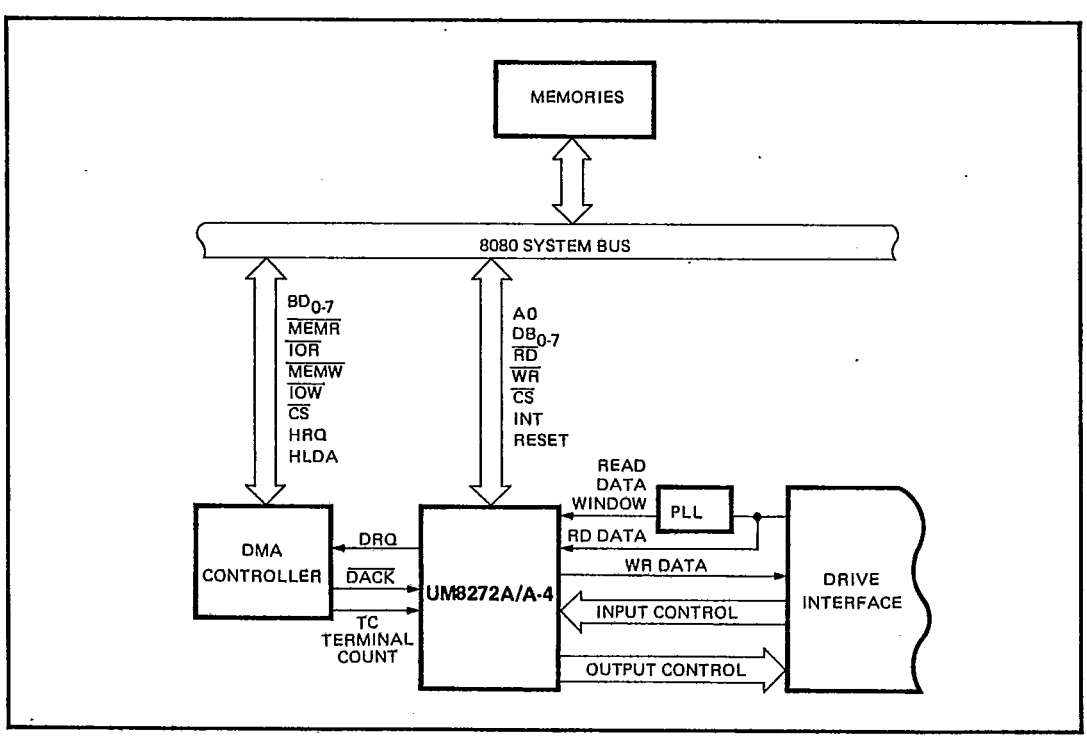


Figure 1. System Configuration

Absolute Maximum Ratings*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +150°C
All Output Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −0.5 to +7 Volts
Supply Voltage V_{CC} . . . . . −0.5 to +7 Volts
Power Dissipation . . . . . 1 Watt

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −400 μA
I_{CC}	V_{CC} Supply Current		120	mA	
I_{IL}	Input Load Current (All Input Pins)		10 −10	μA μA	V_{IN} = V_{CC} V_{IN} = 0 V
I_{LOH}	High Level Output Leakage Current		10	μA	V_{OUT} = V_{CC}
I_{OFL}	Output Float Leakage Current	−10	+10	μA	0.45 V ≤ V_{OUT} ≤ V_{CC}

Capacitance

(T_A = 25°C, f_c = 1 MHz, V_{CC} = 0V)

Symbol	Parameter	Limits		Unit	Conditions
		Min.	Max.		
$C_{IN}(\phi)$	Clock Input Capacitance		20	pF	All Pins Except Pin Under Test Tied to AC Ground
C_{IN}	Input Capacitance		10	pF	
$C_{I/O}$	Input/Output Capacitance		20	pF	

A.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = +5.0V ± 10%)

CLOCK TIMING

Symbol	Parameter	Min.	Max.	Units	Notes
T_{CY}	Clock Period	120	500	ns	Note 5
t_{CH}	Clock High Period	40		ns	Note 4, 5
t_{RST}	Reset Width	14		t_{CY}	

READ CYCLE

t_{AR}	Select Setup to $\overline{RD}\downarrow$	0		ns	
t_{RA}	Select Hold from $\overline{RD}\uparrow$	0		ns	
t_{RR}	$\overline{RD}$ Pulse width	250		ns	
t_{RD}	Data Delay from $\overline{RD}\downarrow$		200	ns	
t_{DF}	Output Float Delay	20	100	ns	

Storage

A.C. Characteristics (Continued) (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 10%)

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
t_{AW}	Select Setup to $\overline{WR}\downarrow$	0			ns	
t_{WA}	Select Hold from $\overline{WR}\uparrow$	0			ns	
t_{WW}	$\overline{WR}$ Pulse Width	250			ns	
t_{DW}	Data Setup to $\overline{WR}\uparrow$	150			ns	
t_{WD}	Data Hold from $\overline{WR}\uparrow$	10			ns	

INTERRUPTS

t_{RI}	INT Delay from $\overline{RD}\uparrow$			500	ns	Note 5
t_{WI}	INT Delay from $\overline{WR}\uparrow$			500	ns	Note 5

DMA

t_{ROCY}	DRQ Cycle Period	13			µs	Note 5
t_{AKRQ}	$\overline{DACK}\downarrow$ to DRQ↓			200	ns	
t_{ROR}	DRQ ↑ to $\overline{RD}\downarrow$	800			ns	Note 5
t_{ROW}	DRQ ↑ to $\overline{WR}\downarrow$	250			ns	Note 5
t_{RORW}	DRQ ↑ to $\overline{RD}\uparrow$ or $\overline{WR}\uparrow$			12	µs	Note 5

FDD INTERFACE

t_{WCY}	WCK Cycle Time		2 or 4 1 or 2		µs	MFM = 0 MFM = 1 Note 2
t_{WCH}	WCK High Time	80	250	350	ns	
t_{CP}	Pre-Shift Delay from WCK↑	20		100	ns	
t_{CD}	WDA Delay from WCK ↑	20		100	ns	
t_{WDD}	Write Data Width	t_{WCH}−50			ns	
t_{WE}	WE ↑ to WCK ↑ or WE ↓ to WCK ↓ Delay	20		100	ns	
t_{WWCY}	Window Cycle Time		2 1		µs	MFM = 0 MFM = 1
t_{WRD}	Window Setup to RDD ↑	15			ns	
t_{RDW}	Window Hold from RDD ↓	15			ns	
t_{RDD}	RDD Active Time (HIGH)	40			ns	

FDD SEEK/DIRECTION/STEP

t_{US}	$US_{0,1}$ Setup to $\overline{RW}$/SEEK ↑	12			µs	Note 5
t_{SU}	$US_{0,1}$ Hold after $\overline{RW}$/SEEK ↓	15			µs	Note 5
t_{SD}	$\overline{RW}$/SEEK Setup to LCT/DIR	7			µs	Note 5
t_{DS}	$\overline{RW}$/SEEK Hold from LCT/DIR	30			µs	Note 5
t_{DST}	LCT/DIR Setup to FR/STEP↑	1			µs	Note 5
t_{STD}	LCT/DIR Hold from FR/STER ↓	24			µs	Note 5
t_{STU}	$DS_{2,1}$ Hold from FR/Step ↓	5			µs	Note 5
t_{STP}	STEP Active Time (High)		5		µs	Note 5
t_{SC}	STEP Cycle Time	33			µs	Note 3, 5
t_{FR}	FAULT RESET Active Time (High)	8		10	µs	Note 5
t_{IDX}	INDEX Pulse Width		10		t_{CY}	
t_{TC}	Terminal Count Width	1			t_{CY}	

Notes:
1. Typical values for T_A are 25°C and nominal supply voltage.
2. The former values are used for standard floppy and the latter values for mini-floppies.
3. t_{SC} = 33 µs min for different drive units. In the case of same unit, t_{SC} can range from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.
4. At 4 MHz, the clock duty cycle may range from 16% to 76%. Using an 8 MHz clock the duty cycle can range from 32% to 52%. Duty cycle is defined as: D.C. = 100 ($t_{CH} \rightarrow t_{CY}$) with typical rise and fall times of 5 ns.
5. The specified values listed are for an 8 MHz clock period. Multiply timings by 2 when using a 4 MHz clock period.

Pin Description

Pin No.	Pin Symbol	Pin Name	Connection to	I/O	Description
1	RESET	Reset	Processor	I	Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not affect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1.024 ms later. To clear this interrupt use Sense Interrupt Status command.
2	$\overline{RD}$	Read	Processor	O ①	Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	$\overline{WR}$	Write	Processor	I ①	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Processor	I	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	AO	Data/Status Reg Select	Processor	I ①	Selects Data Reg (A_0 = 1) or Status Reg (A_0 = 0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Processor	I/O ①	Bi-Directional 8-Bit Data Bus.
14	DRQ	Data DMA Request	DMA	O	DMA Request is being made by FDC when DRW = "1".
15	$\overline{DACK}$	DMA Acknowledge	DMA	I	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	DMA	I	Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
17	IDX	Index	FDD	I	Indicates the beginning of a disk track.
18	INT	Interrupt	Processor	O	Interrupt Request generated by FDC.
19	CLK	Clock		I	Single phase 8-MHz square wave Clock.
20	GND	Ground			DC power return.
21	WRCLK	Write Clock		I	Write Data rate to FDD. FM = 500 kHz; MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	Phase Lock Loop	I	Generated by PLL, and used to sample data from FDD.

Pin Description (Continued)

Pin			Connection to	I/O	Description
No.	Symbol	Name			
23	RD DATE	Read Data	FDD	I	Reads data from FDD, containing clock and data bits.
24	VCO	VCO Sync	Phase Lock Loop	O	Inhibits VCO in PLL when "0" (low), enables VCO when "1".
25	WE	Write Enable	FDD	O	Enables write data into FDD.
26	MFM	MFM Mode	Phase Lock Loop	O	MFM mode when "1", FM mode when "0".
27	SEL	Head Select	FDD	O	Head 1 selected when "1" (high). Head 2 selected when "0" (low).
28, 29	DS_1, DS_0	Unit Select	FDD	O	FDD Unit Selected.
30	WDA	Write Data	FDD	O	Serial clock and data bits to FDD.
31, 32	PS_1, PS_0	Precompensation (pre-shift)	FDD	O	Writes Precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TRK$_0$	Fault/Track 0	FDD	I	Senses FDD fault condition in Read/Write mode, and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	FDD	I	Senses Write Protect Status in Read/ Write mode; and Two Side Media in Seek mode.
35	RDY	Ready	FDD	I	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	FDD	O	Causes read/write head in FDD to contact diskette.
37	FR/STP	Fit Reset/Stop	FDD	O	Resets fault F.F. in FDD in Read/ Write mode, contains stop pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	FDD	O	Lowers Write current on inner tracks in Read/Write mode, determines direction head will stop in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	$\overline{RW}$/SEEK	Read Write/SEEK	FDD	O	When "1" (high) Seek mode selected, when "0" (low) Read/Write mode selected.
40	V_{CC}	+5V			DC Power.

Note: (1) Disabled when $\overline{CS}$ = 1.

UM8272A/A-4 Enhancements

On the UM8272A/A-4, after detecting the Index Pulse, the VCO Sync output stays low for a shorter period of time. See Figure 2-A.

On the 8272 there can be a problem reading data when Gap 4A is 00 and there is no 1AM. This occurs on some older floppy formats. The UM8272A/A-4 solves this problem by adjusting the VCO Sync timing so that it is not low during the data field. See Figure 2.

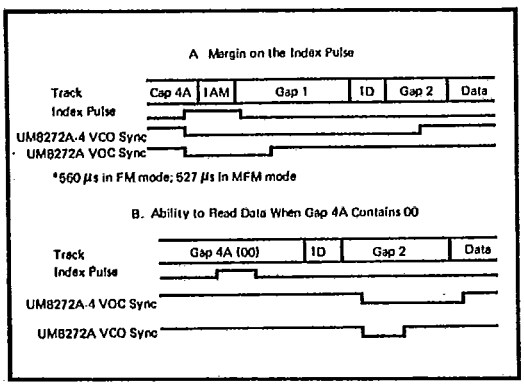


Figure 2. UM8272A/A-4 Enhancements over the 8272

UM8272A/A-4 Registers – CPU Interface

The UM8272A/A-4 contains two registers which may be accessed by the main system processor, a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (several registers in a stack with only one register presented to the data bus at a time) stores data, commands, parameters, and FDD status information. Data bytes are read out of or written into the Data Register in order to program or obtain the results after execution of a command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and UM8272A/A-4.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown in Table 1.

Table 1. A0, $\overline{RD}$, $\overline{WR}$ decoding for the selection of Status/ Data register functions.

A_0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read Main Status Register
0	1	0	Illegal (see note)
0	0	0	Illegal (see note)
1	0	0	Illegal (see note)
1	0	1	Read from Data Register
1	1	0	Write into Data Register

Note: Design must guarantee that the UM8272A/A-4 is not subjected to illegal inputs.

Storage

Table 2. Main Status Register Bit Description.

Bit Number	Name	Symbol	Description
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any of the bits are set FDC will not accept read or write command.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any of the bits are set FDC will not accept read or write command.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any of the bits are set FDC will not accept read or write command.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any of the bits are set FDC will not accept read,or write command.
DB_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended, and result phase has started. It operates only during NON-DMA modes of operation.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 µs. For this reason every time Main Status Register is read the CPU should wait 12 µs. The max time from the trailing edge of the last RD in the result phase to when DB, (FDC Busy) goes low is 12 µs.

Note: There is a 12µS or 24µS ROM flag delay when using an 8 or 4 MHz clock respectively.

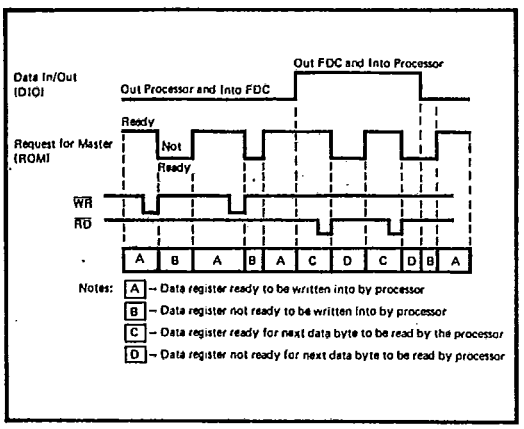


Figure 3. Status Register Timing

The UM8272A/A-4 is capable of executing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the UM8272A/A-4 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information is made available to the processor.

During Command or Result Phases the Main Status Register (described in Table 2) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the UM8272A/A-4. Many of the commands require multiple bytes, and as a result, the Main Status Register must be read prior to each byte transfer to the UM8272A/A-4. On the other hand, During the Result Phase, D6 and D7 in the Main Status Register must both be 1s (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note: this reading of the Main Status Register before each byte transfer to the UM8272A/A-4 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the UM8272A/A-4 is in the non-DMA Mode, then the receipt of each data byte (if UM8272A/A-4 is reading data from FDD) is indicated by an interrupt signal on pin 18 (INT = 1). The generation of a Read signal (RD = 0) will reset the interrupt as well as output the Data onto the Data Bus. For example, if the processor cannot handle Interrupts fast enough (every 13 μs for MFM mode) it may poll the Main Status Registers and bit D7 (RQM) will function just like the Interrupt signal. If a Write Command is in process, the WR signal performs the reset to the Interrupt signal.

The UM8272A/A-4 always operates in a multi-sector transfer mode. It continues to transfer data until the TC input is active. In Non-DMA Mode, the system must supply the TC input.

If the UM8272A/A-4 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The UM8272A/A-4 generates DRQs (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a RD = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The UM8272A/A-4 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The UM8272A/A-4 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent ot the UM8272A/A-4 to form the Command Phase, and are read out of the UM8272A/A-4 in the Result Phase, must occur in the order shown in Table 3. The Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the UM8272A/A-4, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the UM8272A/A-4 is ready for a new command. A command may be aborted by simply sending a Terminal Count signal to pin 16 (TC=1). This is a convenient means of ensuring that the processor can always get the UM8272A/A-4's attention even if the disk system hangs up in an abnormal manner.

Command Symbol Description

Symbol	Name	Description
A0	Address Line 0	A0 controls selection of Main Status Register (A0 = 0) or Data Register (A0 = 1).
C	Cylinder Number	C stands for the current selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for the most significant bit, and D_0 stands for the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final sector number on a Cylinder. During Read or Write operation FDC will stop data transfer after a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the number of data bytes written in Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data address mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0); ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

Storage

Table 3. UM8272A/A-4 Command Set

PHASE	R/W	DATABUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information prior to Command execution.
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			DTL				———	
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	———			ST 0				———	Status information after Command execution.
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution.
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
READ DELETED DATA										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information Prior to Command execution, The 4 bytes are commanded against header on Floppy Disk.
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			OTL				———	
Execution										Data-transfer between the FDD and main system
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
READ ID										
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register,
Result	R	———			ST 0				———	Status information after Command execution.
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information read during Execution Phase from Floppy Disk.
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
WRITE DATA										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information Prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			DTL				———	
Execution										Data transfer between the main system and FDD.
Result	R	———			ST 0				———	Status information after Command execution.
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution.
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
FORMAT A TRACK										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			N				———	Bytes/Sector
	W	———			SC				———	Sectors/Track
	W	———			GPL				———	Gap 3
	W	———			D				———	Filler Byte
Execution										FDC formats an entire track.
Result	R	———			ST 0				———	Status information after Command execution.
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	In this case, the ID information has no meaning.
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
WRITE DELETED DATA										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information Prior to Command execution, The 4 bytes are commanded against header on Floppy Disk.
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			DTL				———	
Execution										Data transfer between the FDD and main system.
Result	R	———			ST 0				———	Status information after Command execution.
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution.
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
SCAN EQUAL										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information Prior to Command execution.
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			STP				———	
Execution										Data compared between the FDD and main system.
Result	R	———			ST 0				———	Status information after Command execution.
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution.
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	

Note: 1 Symbols used in this table are described at the end of this section.
2 A0 should equal binary 1 for all operations.
3 X = Immaterial; usually made to equal binary 0.

Table 3. UM8272A/A-4 Command Set (Continued)

PHASE	R/W	DATABUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
SCAN LOW OR EQUAL			
Command	W	MT MF SK 1 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution,
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data compared between the FDD and main system
Result	R	ST 0	Status information after Command execution. Sector ID information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	
	R	H	
	R	R	
	R	N	
SCAN HIGH OR EQUAL			
Command	W	MT MF SK 1 1 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution,
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data compared between the FDD and main system.
Result	R	ST 0	Status information after Command execution. Sector ID information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	
	R	H	
	R	R	
	R	N	

PHASE	R/W	DATABUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
RECALIBRATE			
Command	W	0 0 0 0 0 1 1 1	Command Codes
	W	X X X X X 0 US1 US0	
Execution			Head retracted to Track 0
SENSE INTERRUPT STATUS			
Command	W	0 0 0 0 1 0 0 0	Command Codes
Result	R	ST 0	Status information at the end of seek operation about the FDC
	R	PCN	
SPECIFY			
Command	W	0 0 0 0 0 0 1 1	Command Codes
	W	SRT HUT	
	W	HLT ND	
SENSE DRIVE STATUS			
Command	W	0 0 0 0 0 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
Result	R	ST 3	Status information about FDD
SEEK			
Command	W	0 0 0 0 1 1 1 1	Command Codes
	W	X X X X X HD US1 US0	
	W	NCN	
Execution			Head is positioned over proper Cylinder on Diskette
INVALID			
Command	W	Invalid Codes	Invalid Command Codes (NoOp — FDC goes into Standby State)
Result	R	ST 0	ST 0 = 80 (16)

Polling Feature of the UM8272A/A-4

After power-up RESET, the Drive Select Lines DS0 and DS1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the UM8272A/A-4 polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the UM8272A/A-4 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the UM8272A/A-4 occurs continuously between instructions, thus notifying the processor which drives are on or off line. Approximate scan timing is shown in Table 4.

Table 4. Scan Timing

DS_1	DS_0	APPROXIMATE SCAN TIMING
0	0	220μS
0	1	220μS
1	0	220μS
1	1	440μS

Command Descriptions

During the Command Phase, the Main Status Register must be polled by the CPU before each byte is written into the Data Register. The DIO (DB_6) and RQM (DB_7) bits in the Main Status Register must be in the "0" and "1" states respectively, before each byte of the command may be written into the UM8272A/A-4. The beginning of the execution phase for any of these commands will cause DIO and RQM to switch to "1" and "0" respectively.

READ DATA

A set of nine (9) byte words is required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head setting time (defined in the Specify Command), and begins reading ID address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, the FDC outputs data (from the Data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command must

be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, checking CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminating the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MFM (MFM/FM), and N (Number of Bytes/Sector). Table 5 shows the Transfer Capacity. The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be

Table 5. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

transferred starting at Sector 1 Side 0 and completing at Sector L Side 1 (Sector L = last sector on the side). Note: This function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to OFFH.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another. If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set to 0, then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be served by the processor every 27 μs in the FM Mode, and every

13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 6 shows the values for C, H, R, and N, when the processor terminates the Command.

Table 6. ID Information When Processor Terminates Command

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	C + 1	NC	R = 01	NC
	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C + 1	NC	R = 01	NC
1	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	NC	LSB	R = 01	NC
	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C + 1	LSB	R = 01	NC

Note: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Storage

WRITE DATA

A set of nine (9) bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading the ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte by byte via the data bus, and outputs it to the FDD. After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count-signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (Incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The Following items are the same (refer to the Read Data Command for details):

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head load Time Interval
- ID Information when the processor terminates command (see Table 6)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command.

For Mini-floppies, multiple track writes are usually not permitted. This is because the turn-off time of the erase head coils the head switches tracks before the erase head turns off. Therefore the system should typically wait 1.3 mS before attempting to step or change sides.

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field with the SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

READ A TRACK

This command is similar to the READ DATA Command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering the INDEX HOLE the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multitrack or skip operations are not allowed with this command.

This command will terminate when EOT number of sectors has been read. If the FDC does not find an ID Address Mark on the diskette after it encounters the index hole for the second time, it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high) and the command is terminated.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the index hole is detected, Data is written on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Formats are recorded. The particular format which will be written is controlled by the values programmed into N: (number of bytes/secter), SC (sectors/cylinder), GPL (Gap Length) and D (Data Pattern). These are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor: four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the UM8272A/A-4 for each sector on the track. The contents of the R Register are incremented by one after each sector is formatted: the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the index hole for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes command termination.

Table 7 shows the relationship between N, SC, and GPL for various sector sizes:

Table 7. Sector Size Relationships

	8" STANDARD FLOPPY					5¼" MINI FLOPPY				
Format	**Sector Size**	**N**	**SC**	**GPL[1]**	**GPL[2]**	**Remarks**	**Sector Size**	**N**	**SC**	**GPL[1]**	**GPL[2]**
FM Mode	128 bytes/Sector	00	1A	07	1B	IBM Diskette 1D	128 bytes/Sector	00	12	07	09
	256	01	0F	0E	2A		128	00	10	10	19
	512	02	06	1B	3A	IBM Diskette 2D	256	01	06	18	30
	1024	03	04	47	8A		512	02	04	46	87
	2048	04	02	C8	FF		1024	03	02	D8	FF
	4096	05	01	C8	FF		2048	04	01	C8	FF
MFM Mode	256	01	1A	0E	36	IBM Diskette 2D	256	01	12	0A	0C
	512	02	0F	1B	54		256	01	10	20	32
	1024	03	08	35	74	IBM Diskette 2D	512	02	08	2A	50
	2048	04	04	99	FF		1024	03	04	80	F0
	4096	05	02	C8	FF		2048	04	02	CB	FF
	8192	06	01	C8	FF		4096	05	01	C8	FF

Notes: 1. Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in formal command.

Storage

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON-BUSY state. While the FDC is in the NON-BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

Note that the UM8272A/A-4 Read and Write Commands do not have implied Seeks. Any R/W command should be preceded by: 1) Seek Command, 2) sense Interrupt Status, and 3) Read ID.

RECALIBRATE

This command causes the read/write head within the FDD to retract to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 both to 1 (high), and terminates the command.

The ability to overlap RECALIBRATE Commands to multiple FDDs, and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC upon one of the following conditions:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 and identifies the cause of the interrupt.

Neither the Seek nor Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Table 8. Seek, Interrupt Codes

Seek End Bit 5	Interrupt Code		CAUSE
	Bit 6	Bit 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . . FE = 254 ms).

The step rate should be programmed for 1 ms longer than the minimum time required by the drive.

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock; if the clock is 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command. No interrupt is generated by the UM8272A/A-4 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high (1) indicating to the processor that the UM8272A/A-4 is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find an 80H indicating an invalid command was received.

A Sense interrupt Status Command must be sent after a Seek or Recalibrate interrupt; otherwise the FDC will consider the next command to be an invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

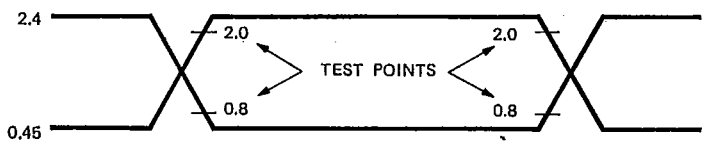
Table 9. Status Registers

Bit No.	Bit Name	Symbol	Description
	STATUS REGISTER 0		
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a
D_0	Unit Select 0	US 0	Drive Unit Number at Interrupt
	STATUS REGISTER 1		
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit is always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			While executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
	STATUS REGISTER 1 (CONT.)		
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the Index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
	STATUS REGISTER 2		
D_7			Not used. This bit is always 0 (low.)
D_6	Control Mark	CM	While executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution of the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	While executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related to the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
	STATUS REGISTER 3		
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

Storage

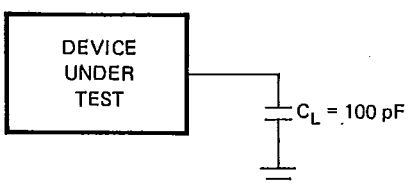
A.C. Testing Input, Output Waveform

INPUT/OUTPUT



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

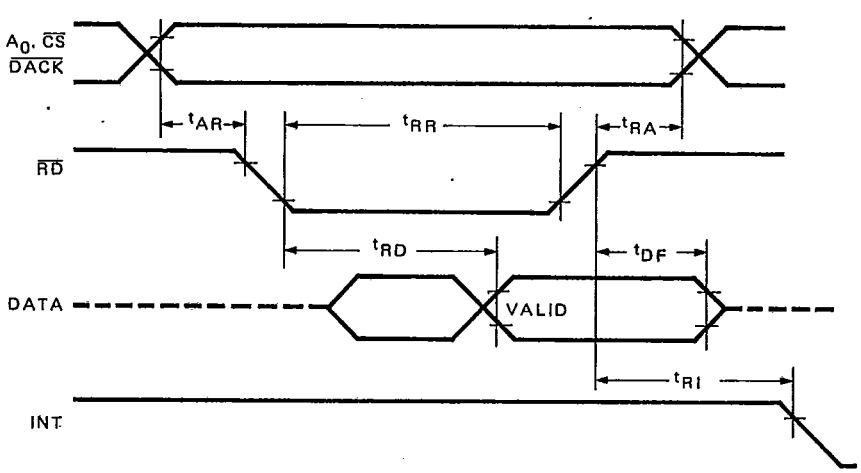
A.C. Testing Load Circuit



C_L INCLUDES JIG CAPACITANCE

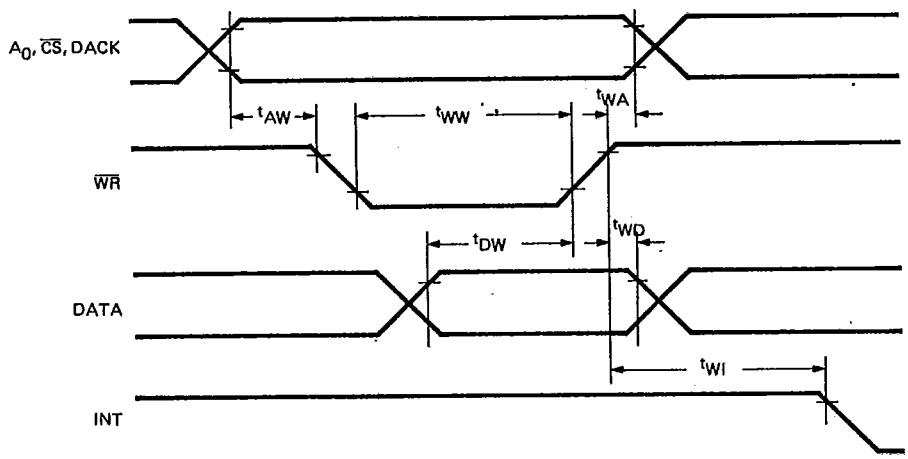
Waveforms

PROCESSOR READ OPERATION

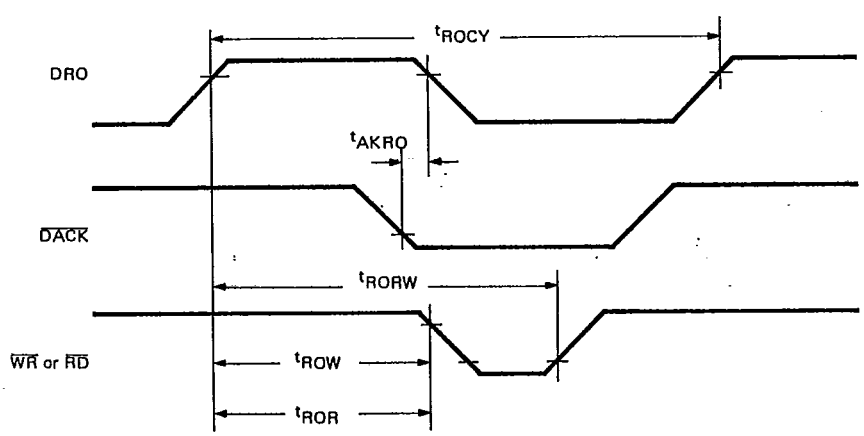


Waveforms (Continued)

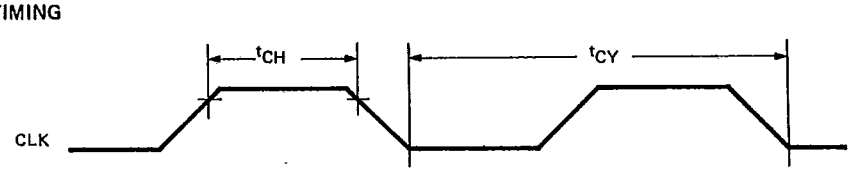
PROCESSOR WRITE OPERATION



DMA OPERATION



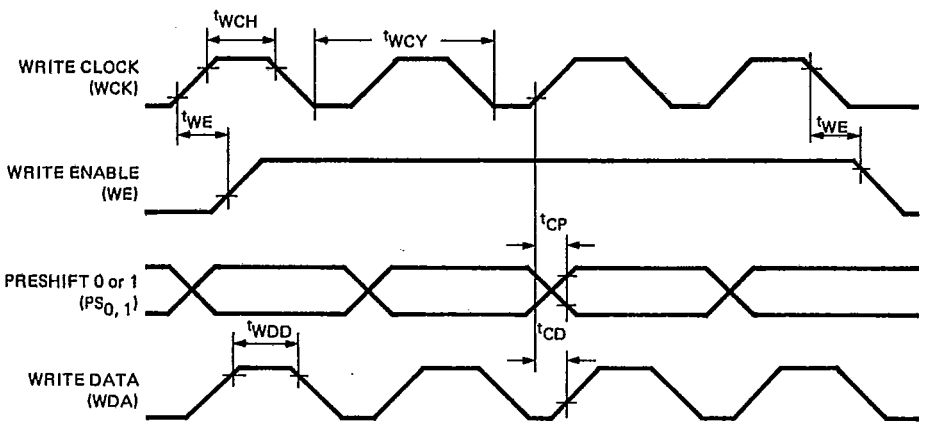
CLOCK TIMING



Storage

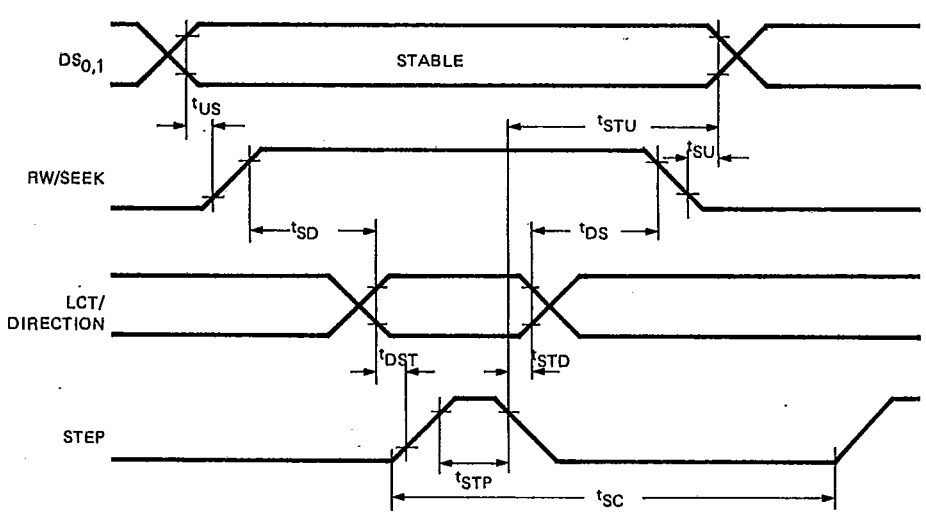
Waveforms (Continued)

FDD WRITE OPERATION

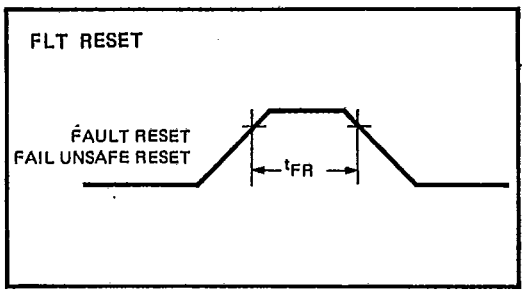


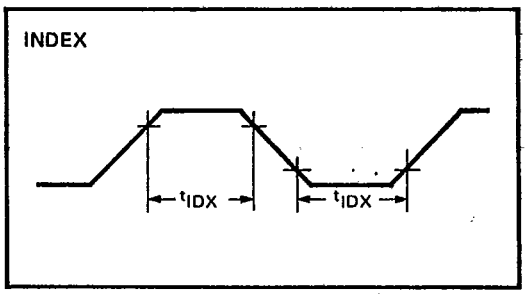
	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

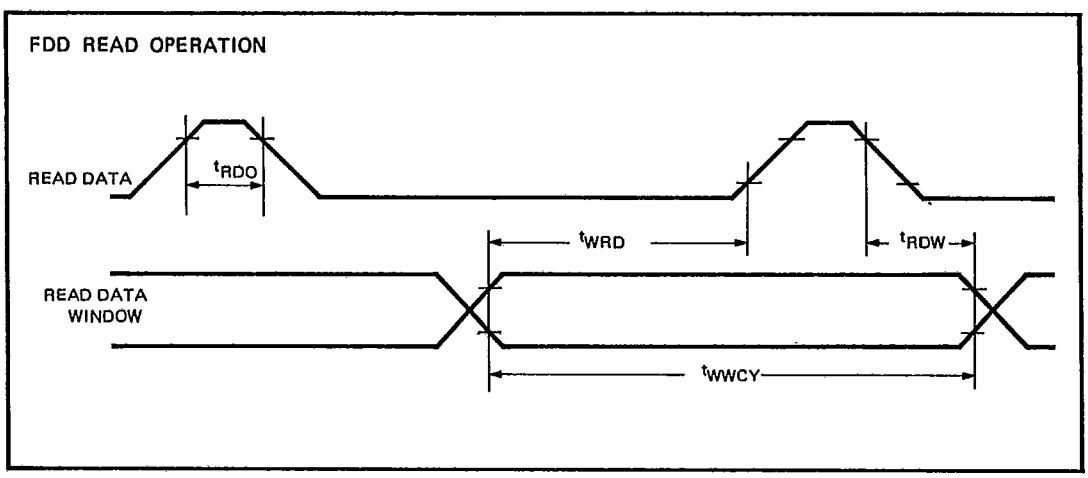
SEEK OPERATION

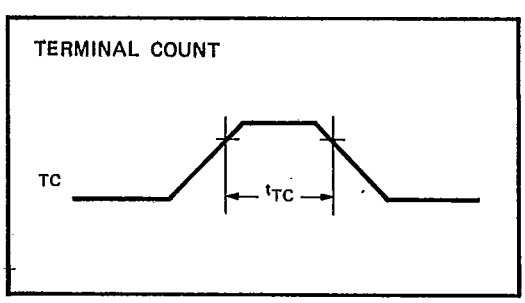


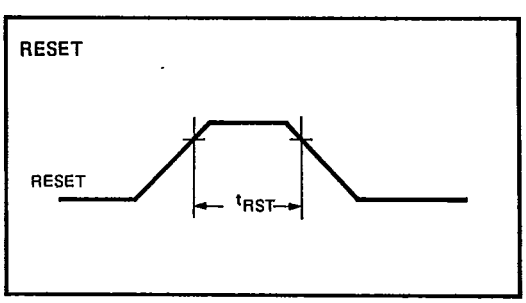
Waveforms (Continued)











Storage

Ordering Information

Part Number	Operational Clock	Package
UM8272A – 4	4 MHz	40L DIP
UM8272A	8 MHz	40L DIP