T-52-33-03

ST62C005-B
DADR: DMA Page Address Register

FEATURES:

- EMS port control
- DMA page address register circuit
- DMA high address latch circuit
- I/O address decoder circuit
- B-PORT circuit
- Non-mask interruption register circuit
- 80287 control circuit
- 2 µm CMOS technology
- 84 pin PLCC package

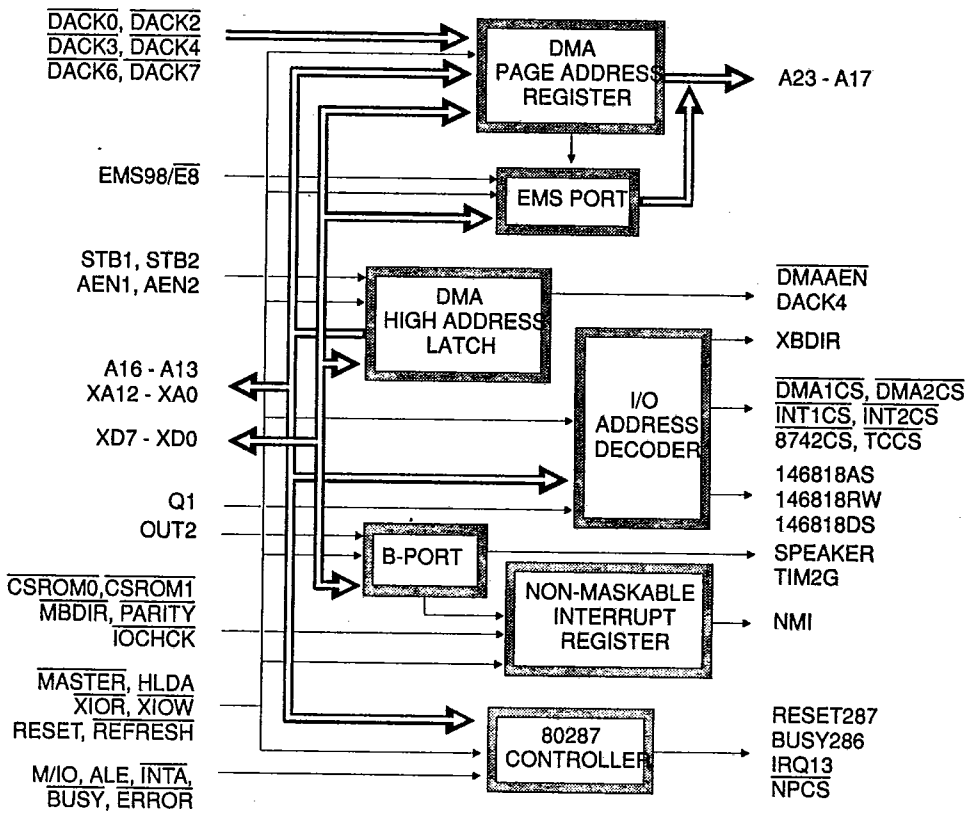
DESCRIPTION:

ST62C005-B consists of:

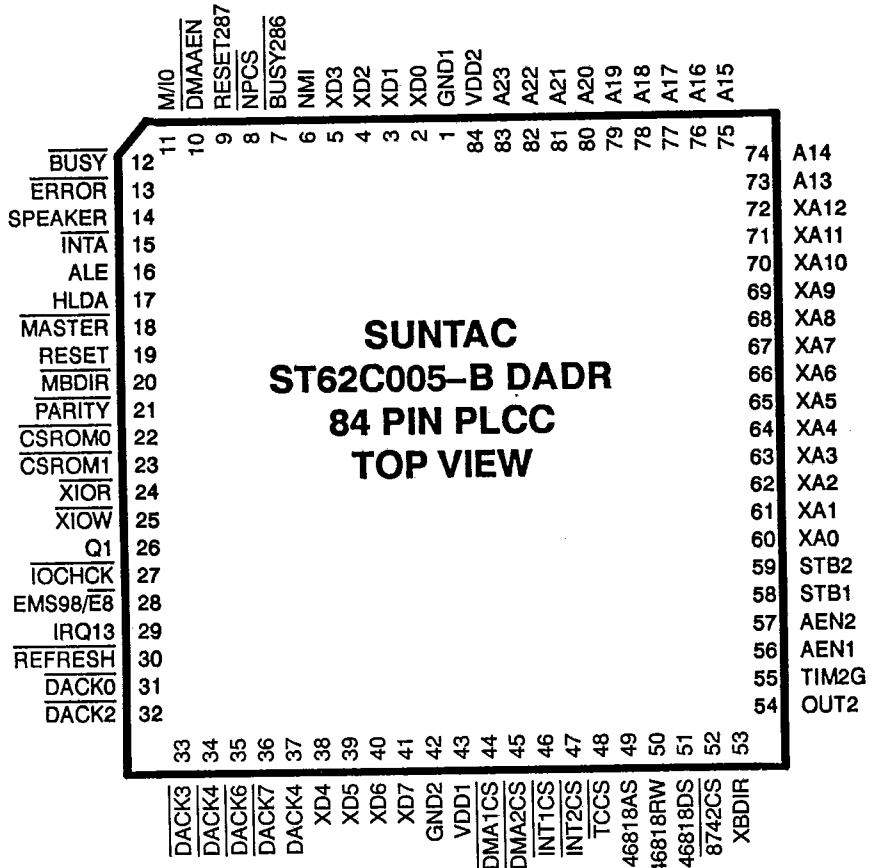
(1) 16 bytes DMA page address registers,
(2) an address latch circuit of DMA high addresses which output XD7- XD0 by DMA controller 8237 during DMA transfer,
(3) I/O address decoder for chip select signals for the peripheral I/Os, i.e., 82C37, 82C54, 82C59, 8742 and 146818,
(4) B-PORT control of refresh signal, speaker sound output, and parity check circuit,
(5) a non-maskable interruption register for the detection of parity error and
(6) 80287 control circuit.

Together with the registers on the ST62BC002-B, the SUNTAC chip set provides hardware-supported EMS functions.

ST62C005-B FUNCTIONAL BLOCK DIAGRAM



ST62C005-B PIN DIAGRAM



ST62C005-B
Pin Description

Symbol	Pin No.	Type	Functions
A13-A23	73-83	O	Output terminals of DMA page address and EMS control data.
XA0-XA7	60 -67	I	Address bus for internal I/O devices, XA0-XA7.
XA8, XA9	68, 69	I/O	Address bus for internal I/O devices, XA8, XA9.
XA10-XA12	70, 71, 72	O	Address bus for internal I/O devices, XA10-XA12.
XD0-XD7	2,3,4,5 38, 39 40, 41	I/O	I/O terminals to be connected with data bus for internal I/O devices, XD0-XD7.
146818DS	51	O	Output terminal to be connected to data strobe signal, "DS", of real time clock 146818.
146818RW	50	O	Output terminal to be connected to read/write signal, "RW", of real time clock 146818.
$\overline{8742CS}$	52	O	Active low output signal, selecting keyboard controller 8742.
$\overline{DMA1CS}$	44	O	Active low output signal, selecting DMA controller 8237 No. 1.
$\overline{DMA2CS}$	45	O	Active low output signal, selecting DMA controller 8237 No. 2.
$\overline{INT1CS}$	46	O	Active low output signal, selecting interrupt controller 8259 No. 1.
$\overline{INT2CS}$	47	O	Active low output signal, selecting interrupt controller 8259 No. 2.
$\overline{TCCS}$	48	O	Active low output signal, selecting programmable interrupt timer 8254.
$\overline{DACK0}$	31	I	Active low input signal, to acknowledge that DMA request for DMA controller (no. 1) "CH0" has been received.

Symbol	Pin No.	Type	Functions
$\overline{DACK2}$	32	I	Active low input signal, to acknowledge that the DMA request for DMA controller (No. 1) CH2 has been received.
$\overline{DACK3}$	33	I	Active low input signal, to acknowledge that the DMA request for DMA controller (No. 1) CH3 has been received.
$\overline{DACK4}$	34	I	Active low input signal, to acknowledge that the DMA request for DAM controller (No. 2) CH0 has been received.
$\overline{DACK6}$	35	I	Active low input signal, to acknowledge that the DMA request for DMA controller (No. 2) CH2 has been received.
$\overline{DACK7}$	36	I	Active low input signal, to acknowledge that the DMA request for DMA controller (No. 2) CH3 has been received.
STB1	58	I	Address strobe signal to latch high address for output to data bus from DMA controller (No. 1).
STB2	59	I	Address strobe signal to latch high address for output to data bus from DMA controller (No. 2).
AEN1	56	I	Input terminal to be connected to AEN of DMA controller 8237 (No. 1).
AEN2	57	I	Input terminal to be connected to AEN of DMA controller 8237 (No. 2).
TIM2G	55	O	Output terminal to be connected to GATE of programmable interval timer 8254. This is an active high signal.
SPEAKER	14	O	Output signal for speaker.
OUT2	54	I	Input terminal, connects to SOUND output OUT2 of programmable interval timer 8254.
$\overline{IOCHCK}$	27	I	Active low input signal, I/O check signal from I/O slot.
IRQ13	29	O	Active high output signal for 80287, interrupt request signal for programmable interrupt controller.

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Symbol	Pin No.	Type	Functions
$\overline{\text{CSROM0}}$	22	I	Chip select signal for BANK 0 of BIOS ROM.
$\overline{\text{CSROM1}}$	23	I	Chip select signal for BANK 1 of BIOS ROM.
146818AS	49	O	Output terminal to be connected to data strobe signal, "AS", of real time clock 146818.
ALE	16	I	Input terminal, connects to "ALE", for address latch enable.
$\overline{\text{REFRESH}}$	30	I	Input terminal of "$\overline{\text{REFRESH}}$" signal, indicating refresh cycle.
$\overline{\text{NPCS}}$	8	O	Active low output signal, for 80287 select signal.
$\overline{\text{ERROR}}$	13	I	Active low input signal, "$\overline{\text{ERROR}}$" input signal from 80287.
RESET287	9	O	Output signal to reset 80287.
$\overline{\text{XIOW}}$	25	I	Input terminal for "$\overline{\text{XIOW}}$" signal, indicating write mode for I/O device.
$\overline{\text{XIOR}}$	24	I	Input terminal for "$\overline{\text{XIOR}}$" signal, indicating read mode from I/O device.
RESET	19	I	System reset signal, "RESET".
$\overline{\text{BUSY}}$	12	I	Active low input "$\overline{\text{BUSY}}$" signal from 80287.
$\overline{\text{MASTER}}$	18	I	Input signal from I/O slot, "$\overline{\text{MASTER}}$".
HLDA	17	I	Input terminal to be connected to 80286 hold acknowledge signal, "HLDA".
M/IO	11	I	Input terminal to be connected to 80286 status signal, "M/IO".
$\overline{\text{BUSY286}}$	7	O	Active low output terminal, BUSY signal for 80286, indicating 80287 being BUSY.
$\overline{\text{INTA}}$	15	I	Interrupt acknowledge signal from ST62BC001-B. Active low input.
NMI	6	O	Active high output signal, to be connected with non-mask interrupt request signal, NMI of 80286.

Symbol	Pin No.	Type	Functions
XBDIR	53	O	Output terminal to control internal I/O data bus, XD0-XD7. To be connected to DIR of TTL ALS245 for XD bus.
DACK4	37	O	Active low to acknowledge that DMA request for DMA controller (No. 2) "CHO" has been received.
V_{DD}	84, 43	I	System power +5V.
GND	1, 42	I	System ground.
$\overline{MBDIR}$	20	I	Input terminal instructing system memory device to output data to data bus.
$\overline{PARITY}$	21	I	Input terminal, connects to "$\overline{PARITY}$" signal of ST62BC004-B.
Q1	26	I	Input terminal, connects to "Q1" signal of ST62BC001-B.
EMS98/ $\overline{E8}$	28	I	Input terminal for controlling EMS port address, 98H if "H", E8H if "L".