

T-52-33-03

ST62BC004-B
DTBC: Data Bus Controller

FEATURES:

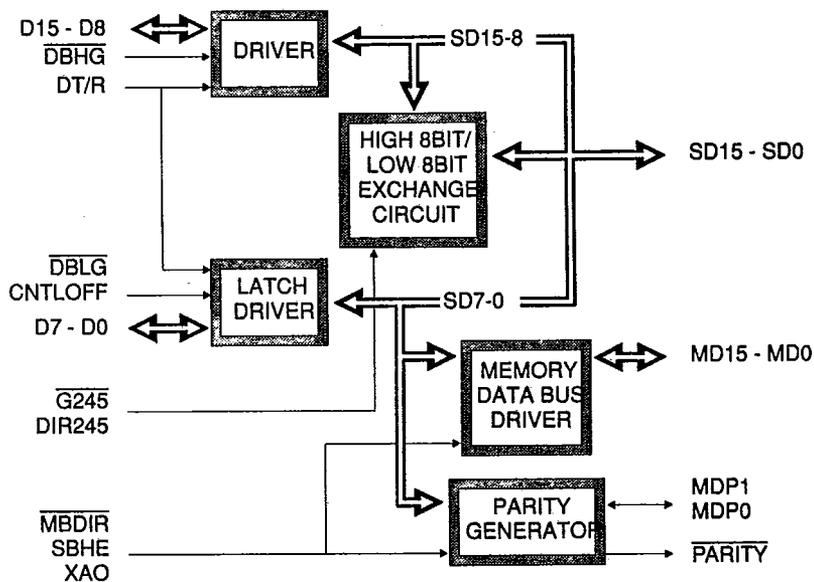
- System data bus driver circuit
- Memory data bus driver circuit
- Parity generator circuit
- Lower 8-bit local data bus latch circuit
- System data bus higher 8-bit, lower 8-bit data exchange circuit
- 1.5 μ m BiCMOS technology
- 68 pin PLCC package

DESCRIPTION:

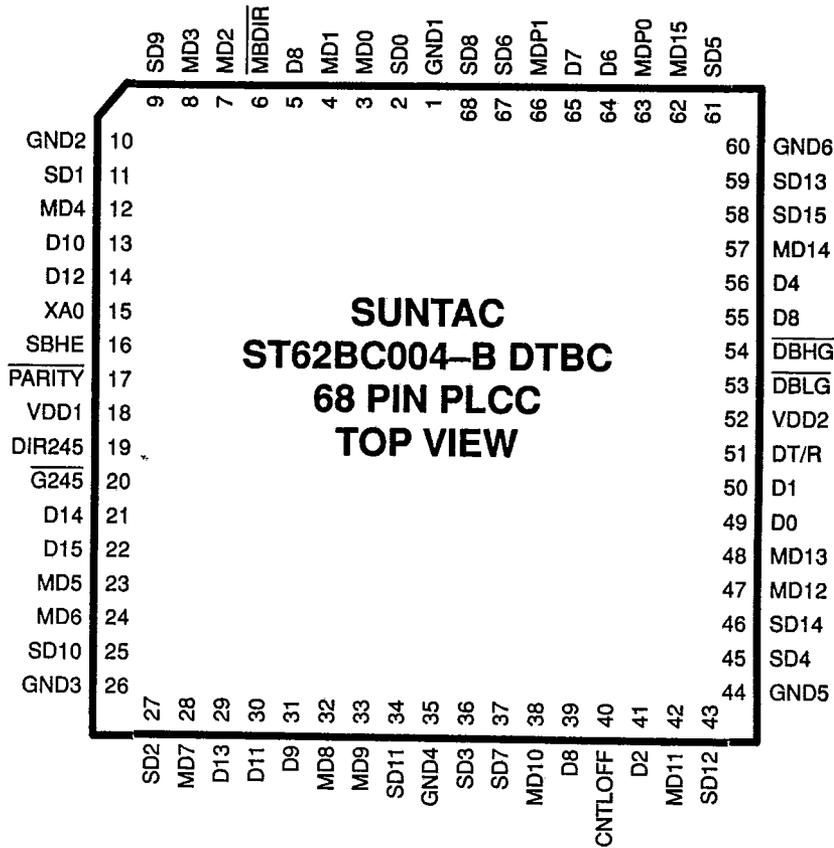
ST62BC004-B consists of:

- (1) two bus drivers which are central parts of this controller and perform the input/output operations between 16-bit data bus from 80286 CPU and system data bus, memory data bus,
- (2) a parity generator circuit for the system memories,
- (3) a lower 8-bit local data bus latch circuit and
- (4) a system data bus higher 8-bit, lower 8-bit exchange circuit.

ST62BC004-B FUNCTIONAL BLOCK DIAGRAM



ST62BC004-B PIN DIAGRAM





ST62BC004-B Pin Description

Symbol	Pin No.	Type	Functions
XA0	15	I	Input terminal to be connected to address bus for internal I/O, "XA0".
MDP0	63	I/O	I/O terminal to be connected to parity bit for lower 8-bit of memory data.
MDP1	66	I/O	I/O terminal to be connected to parity bit for higher 8-bit of memory data
D0-D15	49, 50 41 55 56, 64 39, 65 5, 31 13, 30 14, 29 21, 22	I/O	I/O terminal to be connected to 80286 data bus, D0-D15.
MD0-MD15	3,4,7,8 12, 23 24, 28 32, 33 38, 42 47,48 57,62	I/O	I/O terminal of data bus for on-board main memory (PROM, DRAM)
SD0-SD15	2,11,27 36, 45 61, 67 37, 68 9,25,34 43, 59 46, 58	I/O	I/O terminal to be connected with system data bus.
DBLG, DBHG	53, 54	I	Input control signals for system data bus "D0-D15, SD0-SD15, XD0-XD15".
CNTLOFF	40	I	Input control signals for system data bus "D0-D15, SD0-SD15, XD0-XD15".

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Symbol	Pin No.	Type	Functions
G245	20	I	Input control signals for system data bus "D0-D15, SD0-SD15, XD0-XD15".
DT/R	51	I	Input control signals for system data bus "D0-D15, SD0-SD15, XD0-XD15".
DIR245	19	I	Input control signals for system data bus "D0-D15, SD0-SD15, XD0-XD15".
V _{DD}	18, 52	I	System power +5V.
GND	1, 10 26, 35 44, 60	I	System ground.
$\overline{\text{M}}\text{B}\text{D}\text{I}\text{R}$	6	I	Input terminal, instructing system memory device to output data to data bus.
SBHE	16	I	Active low input signal indicating high SD8-SD15 of system data bus to be valid.
$\overline{\text{P}}\text{A}\text{R}\text{I}\text{T}\text{Y}$	17	O	Output terminal to connect " $\overline{\text{P}}\text{A}\text{R}\text{I}\text{T}\text{Y}$ " signal of ST62C005-B.